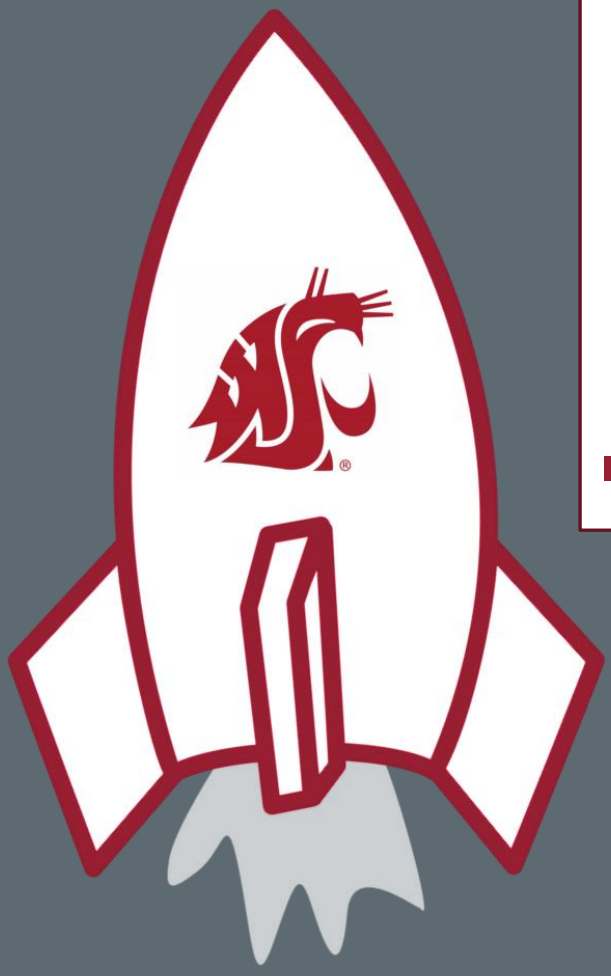
This document explains the function of the Backplane, its schematic level design, and its board level design

# Backplane

Backplane Design

Revision: 3.1.0



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# Table of Contents

# 1 Introduction

This document explains how the Backplane will fulfil the following Functions and Requirements. This document refers to the Backplane version 3.0.0.

## 1.1 Function

The Backplane connects all the subsystems of the satellite together via a parallel bus and interchangeable cards.

## 1.2 Requirements

The system requirements and EPS design requirements can be found on GitHub.

# 2 Detailed Description

This section references the Backplane schematic. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

## 2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

### 2.1.1 Card Slots

The Backplane has eight slots connected in parallel. Each slot is electrically identical. Any card is compatible with every slot.

### 2.1.2 Separation Switch

The separation switch connects via a connector to the Backplane.

## 2.2 Schematic

### 2.2.1 Isolated Grounds

On page 2 of the schematic (D1), are the two isolated grounds found on the Backplane. Power ground *(PGND)* is directly connected to the card. The other grounds are shorted to *PGND* using a $0\Omega$ resistor rated up to $2A$, the expected current is less than $50mA$ each. Chassis ground *(CHASSIS[1:2])* is connected to the conductive Mechanical Features including bolt holes.

### 2.2.2 Separation Switching

There are two identical connectors to connect to the separation switches. The CubeSat requirements specify at least one separation switch, either or both connectors can be used. The switch is normal open and shorts to *PGND* when depressed.

### 2.2.3 Card Connectors

Each card connector is a PCIe socket with 98 pins. See Table 1 for the pin allocation. Each power rail has two pins in parallel which allows loads rated up to $1A$. Each I2C and SPI data signal has two pins in parallel which increases redundancy[1].

*Table 1: Connector Pinout*

| Pins | Pin Name | Description |
|---|---|---|
| A1, B1 | PR_3.3V-0 | Power Rail 3.3V - Channel 0 |
| A2, B2 | PR_3.3V-1 | Power Rail 3.3V - Channel 1 |
| A3, B3 | PR_3.3V-2 | Power Rail 3.3V - Channel 2 |
| A4, B4 | PR_3.3V-3 | Power Rail 3.3V - Channel 3 |
| A5, B5 | PR_3.3V-4 | Power Rail 3.3V - Channel 4 |
| A6, B6 | PR_3.3V-5 | Power Rail 3.3V - Channel 5 |

[1] REQ-009

| Pins | Pin Name | Description |
|---|---|---|
| A7, B7 | PR_3.3V-6 | Power Rail 3.3V - Channel 6 |
| A8, B8 | PR_3.3V-7 | Power Rail 3.3V - Channel 7 |
| A9, B9 | PR_3.3V-8 | Power Rail 3.3V - Channel 8 |
| A10, B10 | PR_3.3V-9 | Power Rail 3.3V - Channel 9 |
| A11, B11 | PR_3.3V-10 | Power Rail 3.3V - Channel 10 |
| A12, B12 | PR_3.3V-11 | Power Rail 3.3V - Channel 11 |
| A13, B13 | PR_3.3V-12 | Power Rail 3.3V - Channel 12 |
| A14, B14 | PR_BATT-0 | Power Rail Vbatt - Channel 0 |
| A15, B15 | PR_BATT-1 | Power Rail Vbatt - Channel 1 |
| A16, B16 | PR_BATT-2 | Power Rail Vbatt - Channel 2 |
| A17, B17 | PR_BATT-3 | Power Rail Vbatt - Channel 3 |
| A18, B18 | PR_BATT-4 | Power Rail Vbatt - Channel 4 |
| A19, B19 | PR_BATT-5 | Power Rail Vbatt - Channel 5 |
| A20, B20 | PR_BATT-6 | Power Rail Vbatt - Channel 6 |
| A21-23<br>B21-29 | PGND | Global ground potential. Includes only the even pins from 82 to 184 |
| A40, B40 | PWR_CTRL_SW | Disconnects battery (active low), driven by deployment switch OR RBF pin |
| A43, B43 | BUS_I2C0_SDA | I2C interfaces for bidirectional data exchange among high priority devices |
| A44, B44 | BUS_I2C0_SCL | |
| A45, B45 | BUS_I2C0_IRQ | |
| A30, B30 | BUS_I2C1_SDA | I2C interfaces for bidirectional data exchange among low priority devices |
| A31, B31 | BUS_I2C1_SCL | |
| A32, B32 | BUS_I2C1_IRQ | |
| A37, B37 | BUS_SPI_SCK | SPI interface to subsystem or direct access to remote serial device |
| A38, B38 | BUS_SPI_MISO | |
| A39, B39 | BUS_SPI_MOSI | |
| A41, B41 | CTRL_RESET | Global reset (active low), *normal high* |
| A42, B42 | CTRL_SYNC | Global synchronization signal, driven by IHU |
| A33, B33 | COM_SPI_SCK | Serial interface for dedicated communication with the Comms |
| A34, B34 | COM_SPI_MISO | |
| A35, B35 | COM_SPI_MOSI | |
| A36, B36 | COM_SPI_CS | |
| A46 | BUS_JTAG_TCK | Shared JTAG interface for subsystem software update via IFJR. Max 1 device at a time, normally high impedance |
| A47 | BUS_JTAG_TDI | |
| A48 | BUS_JTAG_TDO | |
| A49 | BUS_JTAG_TMS | |
| B46 | BUS_JTAG_EN-0 | JTAG_SEL_COMMS |
| B47 | BUS_JTAG_EN-1 | JTAG_SEL_PMIC |
| B48 | BUS_JTAG_EN-2 | |
| B49 | BUS_JTAG_EN-3 | |
| A24 | GPIO-0 | SPI_EN_CAM0 |
| A25 | GPIO-1 | SPI_EN_CAM1 |
| A26 | GPIO-2 | |
| A27 | GPIO-3 | |
| A28 | GPIO-4 | |
| A29 | GPIO-5 | |

### 2.2.4 Mechanical Features

The Backplane mounts to the Structure using two bolts (page 5, D1) and the top and bottom edges. Each of the holes have a capacitor and resistor connecting to power ground which will absorb transients.

## 2.3 Board

The board shall be double layered with 2 $oz$ copper and ENIG finish.

### 2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default minimum parameters below. Signals in the following subsections do not include their sense signals unless specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

| | |
|---|---|
| Trace width: | $0.16mm$ |
| Vias: | $\emptyset 0.3mm$, unlimited count |
| Separation: | $0.16mm$ |
| Length: | unlimited |

Devices with specific placement and routing considerations are called out on the schematic, see "CAD Note:"

#### 2.3.1.1 Power Channels - PR_3.3V-[0:12], PR_BATT-[0:6]

Trace width: $0.5mm$

#### 2.3.1.2 Power Ground - PGND

Trace width: $3.0mm$

#### 2.3.1.3 Data Lines

Length: Each node shall be length matched $\pm 10.0mm$

Stubs: $< 10.0mm$

# 3 Testing

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test[2].

- Waveforms shall be captured whenever appropriate
- Have the event take fill the screen (for fast events, zoom in; for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-Backplane/Testing/Backplane.3.0

Common test instructions can be found on the wiki.

## 3.1 Separation Switching

**Results: Pass**
**Test Configuration: Elvis**

This test evaluates the circuit described in Separation Switching.

### 3.1.1 Test Instructions

Connect the separation switch to each connector. Measure the resistance between *PWR_CTRL_SW* and *PGND* in all switch states.

### 3.1.2 Test Data

| Measure the resistance between *PWR_CTRL_SW* and *PGND* in both switch states. | | | | |
|---|---|---|---|---|
| Switch State | | Resistance | Passing Criteria | Pass / Fail |
| J5 | J6 | | | |
| Released | Released | $> 100M\Omega$ | Resistance > $10M\Omega$ | Pass |
| Released | Depressed | $0.8\Omega$ | Resistance < $10\Omega$ | Pass |
| Depressed | Released | $0.8\Omega$ | Resistance < $10\Omega$ | Pass |
| Depressed | Depressed | $0.6\Omega$ | Resistance < $10\Omega$ | Pass |

## 3.2 Continuity

**Results: Pass**
**Test Configuration: Elvis**

[2] For test 3.1, place files in the subfolder *"3.1"* and so on

This test evaluates the circuit described in Card Connectors.

### 3.2.1 Test Instructions

Measure the resistance of each power channel and the power ground from Slot 0 to Slot 4 (from bottom to top slot). Measure on the card, at the connector.

### 3.2.2 Test Data

| Measure the resistance between each power channel and the power ground from Slot 0 to Slot 7. | | | |
|---|---|---|---|
| Power Channel | Resistance | Passing Criteria | Pass / Fail |
| PGND | $22m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-0 | $47m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-1 | $49m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-2 | $48m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-3 | $42m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-4 | $47m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-5 | $47m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-6 | $47m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-7 | $43m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-8 | $45m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-9 | $43m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-10 | $50m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-11 | $57m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_3.3V-12 | $50m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_BATT-0 | $51m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_BATT-1 | $45m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_BATT-2 | $44m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_BATT-3 | $56m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_BATT-4 | $48m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_BATT-5 | $44m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PR_BATT-6 | $46m\Omega$ | Resistance < $100m\Omega$ | Pass |
| PWR_CTRL_SW | $52m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_I2C0_SDA | $52m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_I2C0_SCL | $52m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_I2C0_IRQ | $52m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_I2C1_SDA | $47m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_I2C1_SCL | $45m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_I2C1_IRQ | $45m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_SPI_SCK | $48m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_SPI_MISO | $47m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_SPI_MOSI | $48m\Omega$ | Resistance < $300m\Omega$ | Pass |
| CTRL_RESET | $46m\Omega$ | Resistance < $300m\Omega$ | Pass |
| CTRL_SYNC | $46m\Omega$ | Resistance < $300m\Omega$ | Pass |
| COM_SPI_SCK | $52m\Omega$ | Resistance < $300m\Omega$ | Pass |
| COM_SPI_MISO | $48m\Omega$ | Resistance < $300m\Omega$ | Pass |
| COM_SPI_MOSI | $52m\Omega$ | Resistance < $300m\Omega$ | Pass |
| COM_SPI_CS | $51m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_JTAG_TCK | $170m\Omega$ | Resistance < $300m\Omega$ | Pass |

| Measure the resistance between each power channel and the power ground from Slot 0 to Slot 7. | | | |
|---|---|---|---|
| Power Channel | Resistance | Passing Criteria | Pass / Fail |
| BUS_JTAG_TDI | $169m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_JTAG_TDO | $165m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_JTAG_TMS | $171m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_JTAG_EN-0 | $176m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_JTAG_EN-1 | $174m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_JTAG_EN-2 | $174m\Omega$ | Resistance < $300m\Omega$ | Pass |
| BUS_JTAG_EN-3 | $175m\Omega$ | Resistance < $300m\Omega$ | Pass |
| GPIO-0 | $163m\Omega$ | Resistance < $300m\Omega$ | Pass |
| GPIO-1 | $163m\Omega$ | Resistance < $300m\Omega$ | Pass |
| GPIO-2 | $159m\Omega$ | Resistance < $300m\Omega$ | Pass |
| GPIO-3 | $158m\Omega$ | Resistance < $300m\Omega$ | Pass |
| GPIO-4 | $159m\Omega$ | Resistance < $300m\Omega$ | Pass |
| GPIO-5 | $174m\Omega$ | Resistance < $300m\Omega$ | Pass |

## 3.3 Isolation

**Results: Pass**
**Test Configuration: Elvis**

This test evaluates the circuit described in Card Connectors.

### 3.3.1 Test Instructions

Measure the resistance of each net on the card connector to every other net.

### 3.3.2 Test Data

| Measure the resistance of each net on the card connector to every other net. | | |
|---|---|---|
| Net | Passing Criteria | Pass / Fail |
| PR_3.3V-0 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-1 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-2 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-3 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-4 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-5 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-6 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-7 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-8 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-9 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-10 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-11 | All resistances > $10M\Omega$ | Pass |
| PR_3.3V-12 | All resistances > $10M\Omega$ | Pass |
| PR_BATT-0 | All resistances > $10M\Omega$ | Pass |
| PR_BATT-1 | All resistances > $10M\Omega$ | Pass |
| PR_BATT-2 | All resistances > $10M\Omega$ | Pass |
| PR_BATT-3 | All resistances > $10M\Omega$ | Pass |
| PR_BATT-4 | All resistances > $10M\Omega$ | Pass |
| PR_BATT-5 | All resistances > $10M\Omega$ | Pass |

| Measure the resistance of each net on the card connector to every other net. | | |
|---|---|---|
| Net | Passing Criteria | Pass / Fail |
| PR_BATT-6 | All resistances > $10M\Omega$ | Pass |
| PGND | All resistances > $10M\Omega$ | Pass |
| PWR_CTRL_SW | All resistances > $10M\Omega$ | Pass |
| BUS_I2C0_SDA | All resistances > $10M\Omega$ | Pass |
| BUS_I2C0_SCL | All resistances > $10M\Omega$ | Pass |
| BUS_I2C0_IRQ | All resistances > $10M\Omega$ | Pass |
| BUS_I2C1_SDA | All resistances > $10M\Omega$ | Pass |
| BUS_I2C1_SCL | All resistances > $10M\Omega$ | Pass |
| BUS_I2C1_IRQ | All resistances > $10M\Omega$ | Pass |
| BUS_SPI_SCK | All resistances > $10M\Omega$ | Pass |
| BUS_SPI_MISO | All resistances > $10M\Omega$ | Pass |
| BUS_SPI_MOSI | All resistances > $10M\Omega$ | Pass |
| CTRL_RESET | All resistances > $10M\Omega$ | Pass |
| CTRL_SYNC | All resistances > $10M\Omega$ | Pass |
| COM_SPI_SCK | All resistances > $10M\Omega$ | Pass |
| COM_SPI_MISO | All resistances > $10M\Omega$ | Pass |
| COM_SPI_MOSI | All resistances > $10M\Omega$ | Pass |
| COM_SPI_CS | All resistances > $10M\Omega$ | Pass |
| BUS_JTAG_TCK | All resistances > $10M\Omega$ | Pass |
| BUS_JTAG_TDI | All resistances > $10M\Omega$ | Pass |
| BUS_JTAG_TDO | All resistances > $10M\Omega$ | Pass |
| BUS_JTAG_TMS | All resistances > $10M\Omega$ | Pass |
| BUS_JTAG_EN-0 | All resistances > $10M\Omega$ | Pass |
| BUS_JTAG_EN-1 | All resistances > $10M\Omega$ | Pass |
| BUS_JTAG_EN-2 | All resistances > $10M\Omega$ | Pass |
| BUS_JTAG_EN-3 | All resistances > $10M\Omega$ | Pass |
| GPIO-0 | All resistances > $10M\Omega$ | Pass |
| GPIO-1 | All resistances > $10M\Omega$ | Pass |
| GPIO-2 | All resistances > $10M\Omega$ | Pass |
| GPIO-3 | All resistances > $10M\Omega$ | Pass |
| GPIO-4 | All resistances > $10M\Omega$ | Pass |
| GPIO-5 | All resistances > $10M\Omega$ | Pass |