This document explains the function of the Solar Panel, its schematic level design, and its board level design

Solar Panel

Solar Panel Design

Revision: 2.0.3

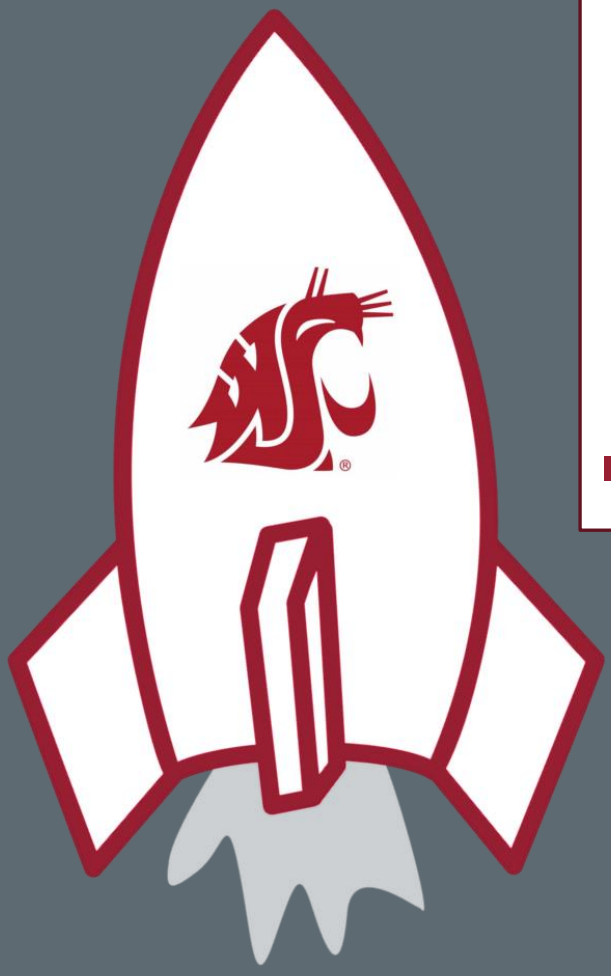

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Table of Contents

1 Introduction

This document explains how the solar panel will fulfill the following Functions and conform to the following Requirements. This document refers to the Solar Panel version 2.0.

1.1 Functions

The Solar Panel is responsible for the following:

- Harvest energy
- Providing power to charge the batteries located on the EPS

1.2 Requirements

The system requirements and EPS design requirements can be found here.

2 Detailed Description

This section references the Solar Panel schematic[1]. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Energy Collection

Energy is captured from the sun by the photovoltaic cells. There are two cells on each panel. Each PV is connected to its own battery charger with MPPT[2].

2.1.2 Power Output

Power is output via two $4.1V$, $500mA$ current limited rails from the battery chargers, one from each battery charger.

2.1.3 GPIO Expander

The GPIO expander allows the PMIC to switch on/off the battery chargers.

2.1.4 ADC

The ADC allows the PMIC to monitor temperature and power at various locations on the board. Sensor locations are indicated on the block diagram.

2.1.5 Magnetorquer

The magnetorquer is controlled by the ADCS.

2.1.6 Connector

The connector connects the solar panel to the EPS and the ADCS to the magnetorquer.

2.2 Schematic

2.2.1 Isolated Grounds

The four isolated grounds are found on page 2 of the schematic. Power ground *(PGND)* is connected to pins 6 and 7 of the connector. All other grounds are shorted to *PGND* with a 0Ω resistor rated for up to $2A$. Digital ground *(DGND)* is connected to the digital components of the board, including the GPIO. Analog ground *(AGND)* is connected to the analog components, including the ADC, its voltage reference, and the thermistors. Chassis ground *(CHASSIS)* is connected to the conductive mechanical components of the board, including the bolt holes.

[1] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-PowerBoard/Documentation/SolarPanel.pdf

[2] Maximum Power Point Tracking adjusts the output voltage and current to maximize the power taken from the solar cells

2.2.2 Battery Charger

Page 2 of the schematic contains the battery chargers. Each battery charger has a single $4.1V$ output, current limited to $500mA$. The battery charger. The batteries are capable of charging at up to $4.2V$, but by charging at $4.1V$ the battery health can be preserved. The active low shutdown pin *(X_SHUT)* is pulled up to the PV output by $10k\Omega$ and $1k\Omega$ resistors in series. *X_SHUT* is connected to the GPIO. The output voltage and current are monitored by the ADC.

2.2.3 GPIO Expander

Page 3 of the schematic contains the GPIO expander. The GPIO expander has 16 inputs/output. Only two of them are being used to let the PMIC shut off the battery chargers. The GPIO expander's address can be configured by selectively placing the stuff resistors connected to the address pins. Each pin can be set to either high or low. Addresses of the four GPIO expanders can be found in the EPS design document.

2.2.4 ADC

Page 3 of the schematic contains the ADC. The ADC has 16 single-ended inputs, or 8 differential inputs, or a combination of the two. The solar panel contains one ADC. The ADC's address can be configured by selectively stuffing[3] the resistors connected to the address pins. Each pin can be set to either high, low, or left floating. Specific addresses can be found in the EPS design document. The ADC measures differential for each PV input, and each $4.1V$ output. Measured as single ended is the temperature at five different locations, the $4.1V$ outputs from each battery charger, and the analog voltage rail *(AVDD)*.

2.2.5 Magnetorquer

The magnetorquer can be found on page 3 of the schematic. The magnetorquer is directly connected to pins 8 and 9 on the connector. These will go directly to the ADCS. The magnetorquer shall only be installed on the +Z, -Y, and -X boards, as only three axes are necessary to control the orientation of the satellite.

2.2.6 Voltage Reference

The high-precision buffered voltage reference can be found on page 2 of the schematic (A5). This chip produces a high precision reference voltage *(AVREF)*, nominally $1.800V$. *AVREF* is used as the absolute voltage reference for calibrating the ADC.

2.3 Board

The board shall be double layered with $1oz$ copper and ENIG finish.

[3] Stuffing refers to populating a component during assembly

2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters specified below. Signals in the following subsections do not include their sense signals unless specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width:	$0.2mm$
Vias:	$\emptyset 0.3mm$, unlimited count
Separation:	$0.2mm$
Length:	unlimited

Devices with specific placement and Routing considerations are called out in the schematic, see "CAD Note"

2.3.1.1 I²C - I2C_[SDA, SCL]

Length:	Each node shall be length matched $\pm 1.0mm$
Stubs:	$< 10.0mm$

2.3.1.2 Solar Panel Outputs - PV_IIN_P-[A:B], PV_IIN_P-[A:B], PGND

PGND Applied between the solar panel and output connector

Trace width: $0.6mm$

2.3.1.3 MPPT Inputs - MPPT_LX-[A:B], PGND

PGND applies between the battery charger and the output connector

Trace Width: $0.6mm$

2.3.1.4 Power Outputs - MPPT_VOUT-[A:B], VOUT-[A:B]

Trace width: $0.6mm$

2.3.1.5 Magnetorquer Inputs - MAGNETORQUER_[P, N]

Trace width: $0.6mm$

2.3.1.6 Input/Output Capacitors - PGND

PGND applies between the input/output capacitors and the output connector

Trace width: $0.6mm$