Bradley Davis

This document explains the function of the Comms, its schematic level design, its board level design, and its functional testing

Comms

In-Orbit Communication Subsystem Design

Revision: 1.2.0





Table of Contents

[1 Introduction 5](#_Toc30375396)

[1.1 Function 5](#_Toc30375397)

[1.2 Requirements 5](#_Toc30375398)

[1.3 Open Systems Interconnection (OSI) Model 5](#_Toc30375399)

[1.3.1 Layers 5](#_Toc30375400)

[1.3.2 CougSat Communication Subsystem 6](#_Toc30375401)

[1.4 Link Budget 6](#_Toc30375402)

[2 Detailed Description 7](#_Toc30375403)

[2.1 Functional Block Diagram 7](#_Toc30375404)

[2.1.1 Comms µController 7](#_Toc30375405)

[2.1.2 RF Clock Generators 7](#_Toc30375406)

[2.1.3 700mm Receiver Radio 7](#_Toc30375407)

[2.1.4 700mm Transmitter Radio 7](#_Toc30375408)

[2.1.5 5V Boost Converter 8](#_Toc30375409)

[2.2 Schematic 8](#_Toc30375410)

[2.2.1 Isolated Grounds 8](#_Toc30375411)

[2.2.2 Power Rails 8](#_Toc30375412)

[2.2.3 Comms µController 8](#_Toc30375413)

[2.2.4 I²C Bus 8](#_Toc30375414)

[2.2.5 SPI Bus 9](#_Toc30375415)

[2.2.6 Current Monitoring 9](#_Toc30375416)

[2.2.7 Voltage Monitoring 9](#_Toc30375417)

[2.2.8 Temperature Monitoring 10](#_Toc30375418)

[2.2.9 Analog Voltage Supply 10](#_Toc30375419)

[2.2.10 5.0V Regulation 10](#_Toc30375420)

[2.2.11 Low Drop-Out Regulators 10](#_Toc30375421)

[2.2.12 RF Clock Generators 10](#_Toc30375422)

[2.2.13 DAC 11](#_Toc30375423)

[2.2.14 RF Modulator 11](#_Toc30375424)

[2.2.15 RF Demodulator 11](#_Toc30375425)

[2.2.16 Low Noise Amplifier / Pre-Amplifiers 12](#_Toc30375426)

[2.2.17 700mm Power Amplifier 12](#_Toc30375427)

[2.2.18 Mechanical Features 12](#_Toc30375428)

[2.3 Board 12](#_Toc30375429)

[2.3.1 Layer Stack-Up 12](#_Toc30375430)

[2.3.2 Layout Constraints 13](#_Toc30375431)

[3 Testing 15](#_Toc30375432)

[3.1 Before First Power-On Check 15](#_Toc30375433)

[3.1.1 Test Instructions 15](#_Toc30375434)

[3.1.2 Test Data 15](#_Toc30375435)

[3.2 Power Rail Switching 15](#_Toc30375436)

[3.2.1 Test Instructions 16](#_Toc30375437)

[3.2.2 Test Data 16](#_Toc30375438)

[3.2.3 Test Notes 16](#_Toc30375439)

[3.3 I²C Bus 16](#_Toc30375440)

[3.3.1 Test Instructions 16](#_Toc30375441)

[3.3.2 Test Data 16](#_Toc30375442)

[3.4 SPI Flash 16](#_Toc30375443)

[3.4.1 Test Instructions 16](#_Toc30375444)

[3.4.2 Test Data 17](#_Toc30375445)

[3.4.3 Test Notes 17](#_Toc30375446)

[3.5 Current Monitoring 17](#_Toc30375447)

[3.5.1 Test Instructions 17](#_Toc30375448)

[3.5.2 Test Data 17](#_Toc30375449)

[3.5.3 Test Notes 17](#_Toc30375450)

[3.6 Voltage Monitoring 17](#_Toc30375451)

[3.6.1 Test Instructions 17](#_Toc30375452)

[3.6.2 Test Data 18](#_Toc30375453)

[3.6.3 Test Notes 18](#_Toc30375454)

[3.7 Temperature Monitoring 18](#_Toc30375455)

[3.7.1 Test Instructions 18](#_Toc30375456)

[3.7.2 Test Data 18](#_Toc30375457)

[3.7.3 Test Notes 18](#_Toc30375458)

[3.8 Analog Voltage Reference 18](#_Toc30375459)

[3.8.1 Voltage 19](#_Toc30375460)

[3.8.2 Ripple and Noise 19](#_Toc30375461)

[3.9 µController Programming 19](#_Toc30375462)

[3.9.1 Test Instructions 20](#_Toc30375463)

[3.9.2 Test Data 20](#_Toc30375464)

[3.9.3 Test Notes 20](#_Toc30375465)

[3.10 5.0V and 9.0V Regulator 20](#_Toc30375466)

[3.10.1 Output Voltage 20](#_Toc30375467)

[3.10.2 Output Ripple and Noise 21](#_Toc30375468)

[3.10.3 Output Efficiency 21](#_Toc30375469)

[3.10.4 Current Limit 22](#_Toc30375470)

[3.10.5 Load Response 22](#_Toc30375471)

[3.11 Low Drop-Out Regulators 24](#_Toc30375472)

[3.11.1 Output Voltage 24](#_Toc30375473)

[3.11.2 Output Ripple and Noise 25](#_Toc30375474)

[3.12 RF Clock Generators 25](#_Toc30375475)

[3.12.1 Reference Clock Supply 25](#_Toc30375476)

[3.12.2 Reference Clock Frequency 26](#_Toc30375477)

[3.12.3 Output Frequency 26](#_Toc30375478)

[3.13 Differential Drivers 26](#_Toc30375479)

[3.13.1 Test Instructions 27](#_Toc30375480)

[3.13.2 Test Data 27](#_Toc30375481)

[3.14 RF Chain – 700mm Downlink 27](#_Toc30375482)

[3.14.1 Isolation Switch 27](#_Toc30375483)

[3.14.2 Digital Modulation 27](#_Toc30375484)

[3.14.3 Analog Modulation 28](#_Toc30375485)

[3.15 RF Chain – 700mm Uplink 29](#_Toc30375486)

[3.15.1 Test Instructions 29](#_Toc30375487)

[3.15.2 Test Data 29](#_Toc30375488)

[3.15.3 Test Notes 29](#_Toc30375489)

# Introduction

This document explains how the Comms will fulfil the following Functions and conform to the following Requirements. This document refers to the Comms version 1.1, +X Panel version 1.0, and -Z Panel version 1.0.

## Function

The In-Orbit Communication Subsystem (Comms) is responsible for the following:

* Transferring telemetry to the ground station
* Transferring payload data to the ground station
* Transferring commands from the ground station
* Transmitting a locating beacon

## Requirements

The system requirements and Comms design requirements can be found [on GitHub](https://github.com/CougsInSpace/CougSat1-Readme/blob/master/CougSat1-Requirements.pdf).

## Open Systems Interconnection (OSI) Model

The OSI model[[1]](#footnote-1) is a conceptual model that can be applied to any communication system. It has eight layers; each layer serves the layer above it and is served by the layer below it.

### Layers

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Layer | | | Protocol Data Unit | Function |
| Host layers | 7 | Application | Data | High-level APIs |
| 6 | Presentation | Translation of data between a networking service and an application |
| 5 | Session | Managing communication sessions |
| 4 | Transport | Segment | Reliable transmission of data segments between points on a network |
| Media layers | 3 | Network | Packet | Structuring and managing a multi-node network |
| 2 | Data link | Frame | Reliable transmission of data frames between two nodes connected by a physical layer |
| 1 | Physical | Symbol | Transmission and reception of raw bit streams over a physical medium |
| 0 | Medium | Electrons, Photons | The physical medium: copper, fiber, wireless |

### CougSat Communication Subsystem

The communication subsystem, formed from the in-orbit and ground subsystems, fulfils layers 0 through 4 of the OSI model. The Comms serves the Command and Data Handling (C&DH) subsystem which fulfils layers 5 and up. The Ground serves itself for layers 5 and up which results in a graphical representation of the exchanged information. The in-orbit and ground subsystems are very similar as they are required to be compatible. For details on the ground subsystem, see its [design document](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-GroundStation/Documentation/GroundStation-Design.pdf).

The hardware described here translates baseband signals generated by the Comms µController into RF signals and vice versa. The translation of the baseband signals to digital data happens in the Comms µController.

For more information on how each layer is structured see [CougSatNet](https://github.com/CougsInSpace/CougSat1-Software/blob/master/CougSat1-Comms/docs/CougSatNet.pdf) from a software perspective and details on the RF modulation techniques.

#### Layer 0

The communication subsystem is using wireless transmission, in the radio frequency band. The band utilized is .

#### Layer 1

The modulation scheme used is Quadrature Phase Shift Keying (QPSK)[[2]](#footnote-2). Each symbol is a change in the phase constant of the RF wave. The radios are software defined radios which allows reconfiguration of this layer if necessary. Other modulation schemes can be developed if the hardware supports it.

#### Layer 2 and Up

See [CougSatNet](https://github.com/CougsInSpace/CougSat1-Software/blob/master/CougSat1-Comms/docs/CougSatNet.pdf).

## Link Budget

A [link budget](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-RadioBoard/Documentation/Comms-LinkBudget.pdf) for downlink and uplink was tabulated indicating a transmit power of is sufficient for up to . Downlink is marginal at this high data rate near the horizon[[3]](#footnote-3). Uplink has no problems thanks to access to high gain and high-power transmitters on the ground.

# Detailed Description

This section references the Comms [schematic](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-RadioBoard/Documentation/Comms.pdf). Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

## Functional Block Diagram

The block diagram can be found on the first page of the schematic.

### Comms µController

The Comms µController is responsible for interfacing the radio signals and the Command and Data Handling subsystem[[4]](#footnote-4). This fulfils OSI model[[5]](#footnote-5) layers 1 through 4. It samples and synthesizes the baseband signals which are mixed with the carrier wave. This constitutes a software defined radio. The µController has non-volatile storage in the form of SPI Flash to store configurations and reference waveforms.

### RF Clock Generators

Each radio has a configurable clock generator used to synthesize the carrier waves. For the transmission of the beacon, the generator is the direct source without any modulation to the antenna[[6]](#footnote-6).

### 700mm Receiver Radio

Its RF diagram is the top row on page 2. The RF signal from the antenna is connected to the receiver radio via a high isolation RF switch. This switch prevents the transmitter from overdriving the sensitive receiver components and inducing damage. The signal is then amplified by low noise amplifiers which add very little noise to the signal to maintain the highest signal to noise ratio. The signal is then connected to the demodulator which removes the carrier frequency and splits that baseband signal into its in-phase and quadrature signals which are then sampled by the Comms µController and demodulated into digital data. The receiver radio is designed for continuous operation and low power[[7]](#footnote-7).

### 700mm Transmitter Radio

Its RF diagram is the middle row on page 2. The Comms µController generates in-phase and quadrature baseband signals using a digital to analog converter. This allows arbitrary waveform including voice signals[[8]](#footnote-8). These signals feed the modulator which puts the baseband signals on the carrier wave. This modulated RF gets amplified with a power amplifier to transmit the desired , see the Link Budget.

### 5V Boost Converter

The RF chains require a 5V supply which come from boost converters. The converters are sourced from the battery rail.

## Schematic

### Isolated Grounds

On page 3 of the schematic (D1 & D2), are the four isolated grounds found on the Comms. Power ground *(PGND)* is directly connected to the backplane and the boost converters. Most of the other grounds are shorted to *DGND* using a resistor rated up to , the expected current is less than each. Digital ground *(DGND)* connects to the digital circuity including the Comms µController and connects to *PGND*. Analog ground *(AGND)* connects to analog circuits including the ADCs, the voltage references, the thermistors, and the operational amplifiers. *AGND* connects to *DGND*. Chassis ground *(CHASSIS)* is connected to the Mechanical Features including bolt holes and the card rails. The layout preserves proper grounding techniques.

### Power Rails

Page 3 of the schematic illustrates all the power rails on the Comms. Each RF chain can be turned off to save power and as a radio inhibit[[9]](#footnote-9).

### Comms µController

The Comms µController (page 4) is a microcontroller from the STM32 low power family[[10]](#footnote-10). It was chosen for its ease of programming, and low power consumption. It needed fast ADCs for sampling, large amounts of RAM for storing buffers, and a fast CPU for modulation/demodulation math.

#### Programming Connections

During testing, the Comms µController is programmed via Serial Wire Debug[[11]](#footnote-11) (SWD, page 4, A1). The process of programming is made simple with just a single six pin header and a robust software utility. In orbit, the µController can be programmed via JTAG[[12]](#footnote-12). The [In-Flight JTAG Reprogrammer](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-AvionicBoard/Documentation/IFJR-Design.pdf) (IFJR) connects via the backplane, through tri-state buffers/logic level converters[[13]](#footnote-13) (page 5, C3:D3). The IFJR can enable or disable the tri-state buffer which essentially disconnects the JTAG interface from the Comms µController (it outputs high impedance), allowing the SWD to program. The logic level conversion feature is not used.

### I²C Bus

The Comms µController has one I²C bus (page 4, C4). It connects to the monitoring ADCs.

#### ADCs

There are ADCs[[14]](#footnote-14) connected to the Comms µController, each with single-ended inputs. The ADC was chosen for its low power, SAR architecture, small package, and up to addresses. The list of address (7b) follow:

* [0x2B] ADC-0 (page 6, A2), temperature
* [0x2F] ADC-1 (page 6, A5), temperature
* [0x2A] ADC-2 (page 6, C2), voltage and current

The two voltage sensing inputs have voltage dividers (page 6, C1) that reduces the voltage of every input to place their level within the sensing range of . Using paired resistors helps match the gain across temperature.

### SPI Bus

The Comms µController has two SPI buses[[15]](#footnote-15). One connects to the C&DH to transfer packets and telemetry. One connects to the RF Clock Generators, and SPI Flash.

#### Backplane to the C&DH

The Comms µController is a slave to the C&DH, see the [interface document](https://github.com/CougsInSpace/CougSat1-Software/blob/master/CougSat1-Comms/docs/CommsInterface.pdf) for details. Tri-state buffers isolate the bus when Comms is off as to not disturb the backplane side.

#### RF Clock Generators

The Comms µController is a transmit only master to the RF Clock Generators. Each generator has tri-state buffers which only connects the bus if the generator’s rail is on. Without this, when the generator is turned off, its ESD diodes would prevent the bus from moving above *GND* effectively disabling the bus.

The Comms µController is a master to two SPI Flash chips[[16]](#footnote-16) (page 4, A5:B6) that provides of mirrored storage or of striped storage.

### Current Monitoring

At various locations, the power chain has shunt resistors connected to ADCs in through a differential amplifier[[17]](#footnote-17) monitor the current. Those locations are:

* 5V Regulator output (page 7, C2)
* Each RF chain input (page 8)

### Voltage Monitoring

The regulator output and PA output are measured using the ADCs. Those locations are:

* 5V Regulator output (page 6, B6)
* 700mm PA power output Regulator output (page 11, C2)

### Temperature Monitoring

At various locations, the temperature is monitored using thermistors and the ADCs. Those locations are:

* 5V Regulator (page 7, A3)
* Comms µController (page 4, B3)
* RF clock generators (page 9, A4; page 10, A4)
* DAC (page 8, D4)
* 700mm downlink RF chain (page 11, B3, & C3)
* 700mm uplink RF chain (page 12, D4; page 13, C4)

### Analog Voltage Supply

The Comms has an analog voltage supply (page 6, C5) which is fed by the *3.3V* rail filtered with a ferrite bead and capacitors. Precision is not required as all ADCs use the precision voltage reference for calibration. This is the source for the Temperature Monitoring thermistors and operational amplifiers.

### 5.0V Regulation

The 5.0V regulator (page 7) is switching mode, boost topology. The converter[[18]](#footnote-18) automatically senses the output voltage and adjusts the switching parameters to keep the output at . The converter has an integrated switching MOSFET. The converter was chosen for its small size and high efficiency.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

The converter and inductor (page 7, B2:B3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

### Low Drop-Out Regulators

The sensitive RF components are supplied through low drop-out (LDO) regulators[[19]](#footnote-19) (page 8, B3, & D3). These are linear regulators that require a small drop-out[[20]](#footnote-20) for proper regulation. They are used to reject the switching noise from the switching mode power supplies.

### RF Clock Generators

The RF Clock Generators[[21]](#footnote-21) (page 9, A4; page 10, A4) have a voltage-controlled oscillator and a phase-locked loop to take a reference clock and synthesize a RF wave. The reference clocks[[22]](#footnote-22) (page 9, A3; page 10, A3) have high frequency stability and are supplied with ferrite beads to further increase frequency stability. The supporting circuitry for the generators was created using Analog Device’s [ADIsimPLL](https://form.analog.com/Form_Pages/RFComms/ADISimPll.aspx). The design files can be found under the [documentation folder](https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-RadioBoard/Documentation/Native). The output of the generators is designed to drive a load.

The 700mm Receiver Radio’s demodulator divides its clock input by two, so the RF clock generator needs to output double the carrier frequency.

### DAC

The Comms µController outputs a parallel bus for the DAC[[23]](#footnote-23) which feeds the RF Modulator. The DACs have a built-in interpolation filter to reduce high frequency spurs from the input signal.

The DACs output a current source of magnitude , set by *FSADJ* resistors to *GND*, differentially. Each modulator has a differential voltage and common mode voltage for these baseband signals which is set by the output resistors to *GND* and between the differential pair. This circuit was simulated in [LTSpice](https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html) and can be found under [electrical design](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-RadioBoard/ElectricalDesign/LTSpice/ModulatorDriver/ModulatorDriver.asc). Precision resistors are used to reduce any common mode offset or gain imbalance. A capacitor in this output creates a low pass filter to help with bandwidth limiting.

### RF Modulator

The 700mm Transmitter Radio’s modulator[[24]](#footnote-24) (page 13, A3) has the RF Clock Generators AC coupled into their local oscillator input, and the DAC are directly connected to the baseband inputs. The RF output is AC coupled to the next element in the RF chain. Output filters bandpass around the carrier to reduce unwanted spurs from being amplified.

### RF Demodulator

The 700mm Receiver Radio’s demodulator[[25]](#footnote-25) (page 15, B3:B4) has the RF Clock Generators AC coupled into its local oscillator input. The termination resistor is used to match a input into the demodulator. The RF signal is connected to the modulator’s input through a balun (page 13, B2) to match a input into the demodulator’s . The gain of the demodulator is set by a DAC output of the Comms µController.

The demodulator outputs differential baseband signals . this amplified and translated to single ended for input to the Comms µController’s ADC by op-amps[[26]](#footnote-26) (page 11, C1:D3). This circuit was simulated in LTSpice and can be found under [electrical design](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-RadioBoard/ElectricalDesign/LTSpice/IQAmplifier/IQAmplifier.asc).

### Low Noise Amplifier / Pre-Amplifiers

The low noise amplifiers (LNA)[[27]](#footnote-27) (page 11, A5; page 12, B2, B5, & C3) amplify the RF signal for the next component in the RF chain. They were chosen for their low noise figure, broadband response, and high gain. For the 700mm Receiver Radio’s LNAs, the bias voltage can be shorted to ground which disables the amplifier. This is required, along with toggling the RF switch, when transmitting on to not damage the demodulator. The output is biased via a ferrite bead to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the next component.

### 700mm Power Amplifier

The 700mm power amplifier[[28]](#footnote-28) (page 13, C3) is the final amplifiers for the RF signal. It drives the antennas and output the desired , see the Link Budget. It was chosen for the output power, high efficiency, and appropriate frequency band. The output is biased via an inductor to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the antenna.

The amplifier has a power detector (page 13, C1) that is sampled by the Voltage Monitoring, to measure the power being sent to the antenna.

### Mechanical Features

The 5V Boost Converter heatsink (page 6, D1) and RF chain heatsinks (page 11, D1) mount directly to the Comms board using bolts. These holes are conductive and connected directly to *CHASSIS*, see Isolated Grounds. The Comms also slots into the structure using rails[[29]](#footnote-29) which are also conductive and connected directly to *CHASSIS*. Each of the holes have a capacitor and resistor connecting to power ground which will absorb and dissipate transients.

## Board

The board shall also conform to the dimensions specified by the [CougSat Module Standard](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-Backplane/Documentation/CougSatModuleStandard.pdf).

### Layer Stack-Up

The board shall be four layered with ENIG finish, see Figure 1. Only through vias shall be used. The external copper weight shall be and the internal copper weight shall be .

| Layer | Thickness | Primary Function |
| --- | --- | --- |
| 1 (top) |  | SMD components, RF & signal traces |
| Prepreg |  | JLC2313: |
| 2 |  | Ground planes |
| Core |  |  |
| 3 |  | Power planes |
| Prepreg |  | JLC2313: |
| 4 (bottom) |  | Signal traces |

Figure 1: Stack-Up

### Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless otherwise specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width:

Vias: , unlimited count

Separation:

Length: unlimited

Devices with specific placement and routing considerations are called out on the schematic, see “CAD Note:”

#### All 50Ω Impedance Traces

This applies to all RF traces expect the demodulator’s RF input. These traces shall be a coplanar waveguide with ground[[30]](#footnote-30).

Trace width:

Gap width:

Vias: none

Length: minimize

#### All 200Ω Impedance Traces

This applies to the demodulator’s RF input. These traces shall be an edge coupled microstrip[[31]](#footnote-31) with differential impedance of . Ground located on second layer below ( substrate thickness).

Trace width:

Gap width:

Vias: none

Length: minimize

#### All Differential Signals / Parallel Bus

This applies to the modulators’ inputs. Single ended to/from differential shall occur as close to the single ended side as possible.

Trace width:

Gap width:

Length: Length match

Vias: minimize

#### Regulator Input – VBATT, PGND

This applies to *VBATT* and *PGND* between the backplane and the inputs to the regulators and their input capacitors.

Trace width: ( on internal layers)

#### Regulator Output – 5.0V, PGND

*PGND* applies to between the regulator, its output capacitors, and the backplane.

Trace width: ( on internal layers)

#### Regulator Channels – 3.1V\_[1:2], 5.0V\_1, PGND

*PGND* applies to between the regulator, their loads, and the backplane.

Trace width: ( on internal layers)

#### SPI Buses – SPI\_[SCK, MOSI, MISO, CS], COM\_SPI\_[SCK, MOSI, MISO, CS]

Length: Each node shall be length matched

Stubs:

#### JTAG – JTAG\_[TCK, TDI, TDO, TMS], BUS\_JTAG-[TCK, TDI, TDO, TMS]

Length: Each node shall be length matched

Stubs:

#### I²C – I2C\_[SCL, SDA]

Length: Each node shall be length matched

Stubs:

# Testing

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board’s test folder for each test[[32]](#footnote-32).

* Waveforms shall be captured whenever appropriate
* Have the event take fill the screen (for fast events, zoom in; for slow events, zoom out)
* Label each channel accurately
* Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
* If ringing or overshoot occurs, use a ground spring or differential probe

Results location: <https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-PowerBoard/Testing/Comms.1.1>

Common test instructions can be found on the [wiki](http://cougs.space/wiki).

## Before First Power-On Check

**Test Configuration:**

This test is required to be executed before any external power is applied to the Comms.

### Test Instructions

Measure the resistance of various points in reference to *PGND* located at the backplane. This is informational only.

### Test Data

| Node | Resistance |  | Node | Resistance |
| --- | --- | --- | --- | --- |
| VBATT |  |  | 3.3V\_6 |  |
| 3.1V-1 |  |  | 3.1V-2 |  |
| 5.0V |  |  | 5.0V-1 |  |
| I2C\_SCL |  |  | I2C\_SDA |  |
| MOD\_LNA\_700\_RFOUT |  |  | ANTENNA\_700\_COAX |  |

## Power Rail Switching

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in Power Rails.

### Test Instructions

Hold the µController in reset or program a blank image, verify the power rails are powered off. Have the µController enable the power rail, verify the power rails are powered on, ensuring the rail turns on only with its control signal.

### Test Data

| Hold the µController in reset, measure the voltage of each power rail | | | |
| --- | --- | --- | --- |
| Rail | Voltage | Passing Criteria | Pass / Fail |
| 3.1V-1 |  | Voltage < |  |
| 3.1V-2 |  | Voltage < |  |
| 5.0V-1 |  | Voltage < |  |

| Have the µController enable the power rail, measure the voltage of each power rail. Ensure the rail turns on only with its control signal | | | | |
| --- | --- | --- | --- | --- |
| Rail | Control Signal | Voltage | Passing Criteria | Pass / Fail |
| 3.1V-1 | PC\_3.1V-1 |  | Voltage > |  |
| 3.1V-2 | PC\_3.1V-2 |  | Voltage > |  |
| 5.0V-1 | PC\_5.0V-1 |  | Voltage > |  |

### Test Notes

Delete me if not required

## I²C Bus

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in I²C Bus.

### Test Instructions

At the pull up resistors of the *I2C* bus, validate signal integrity. The µController should generate random I2C traffic on the bus.

### Test Data

| At the pull up resistors of the *I2C* bus, validate the following timing parameters | | |
| --- | --- | --- |
| Capture the *SDA* and *SCL* lines | Passing Criteria | Pass / Fail |
|  | Signal Integrity | Pass |

## SPI Flash

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in SPI Bus.

### Test Instructions

Perform write and read operations to the SPI Flash chips. Verify functionality.

### Test Data

| Perform write and read operations to the SPI Flash chips. Verify functionality. | | | |
| --- | --- | --- | --- |
| Chip | Direction | Passing Criteria | Pass / Fail |
| A | Read | Functionality |  |
| A | Write | Functionality |  |
| B | Read | Functionality |  |
| B | Write | Functionality |  |

### Test Notes

Delete me if not required

## Current Monitoring

**Results: Pass / Fail**

This test evaluates the circuit described in Current Monitoring.

### Test Instructions

Apply a resistive load to a *5.0V-1*. Compare the current measured by the Comms and a DMM.

Note:

### Test Data

| Apply a resistive load to a single output channel. Compare the current measured by the Comms and a DMM | | | | | |
| --- | --- | --- | --- | --- | --- |
| Load | EPS Current | DMM Current | Error | Passing Criteria | Pass / Fail |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

### Test Notes

Delete me if not required

## Voltage Monitoring

**Results: Pass / Fail**

This test evaluates the circuit described in Voltage Monitoring.

### Test Instructions

Compare the voltage measured by the Comms and a DMM on the following signals:

* *I\_3.3V-0N*
* *I\_3.3V-1P*
* *5.0V*

Note:

### Test Data

| Compare the voltage measured by the Comms and a DMM | | | | | |
| --- | --- | --- | --- | --- | --- |
| Signal | Comms Voltage | DMM Voltage | Error | Passing Criteria | Pass / Fail |
| *PA\_PDET\_700* |  |  |  |  |  |
| *5.0V* |  |  |  |  |  |

### Test Notes

Delete me if not required

## Temperature Monitoring

**Results: Pass / Fail**

This test evaluates the circuit described in Temperature Monitoring.

### Test Instructions

Compare the temperature measured by the Comms and a thermometer on the following temperature sensors:

* 5.0V Regulator
* µController
* +X+Y

Note:

### Test Data

| Compare the temperature measured by the Comms and a thermometer | | | | | |
| --- | --- | --- | --- | --- | --- |
| Sensor | Comms Temperature | Thermometer Temperature | Error | Passing Criteria | Pass / Fail |
| 5.0V Regulator |  |  |  |  |  |
| µController |  |  |  |  |  |

### Test Notes

Delete me if not required

## Analog Voltage Reference

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in Analog Voltage Supply. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources.

### Voltage

#### Test Instructions

Measure the voltage of each analog reference.

Note: Measure the DC component with PLC[[33]](#footnote-33) > 100

#### Test Data

| Measure the voltage of the following signals | | | |
| --- | --- | --- | --- |
| Signal | Voltage | Passing Criteria | Pass / Fail |
| ADC\_VREF-0 |  |  |  |
| ADC\_VREF-1 |  |  |  |
| ADC\_VREF-2 |  |  |  |
| AVREF-0 |  |  |  |
| AVREF-1 |  |  |  |
| DAC\_REFIO-700 |  |  |  |

#### Test Notes

Delete me if not required

### Ripple and Noise

#### Test Instructions

Measure the ripple and noise of each analog reference.

Note: Measure the RMS AC component with

#### Test Data

| Measure the RMS voltage ripple and noise of the following signals | | | |
| --- | --- | --- | --- |
| Signal | Voltage | Passing Criteria | Pass / Fail |
| ADC\_VREF-0 |  |  |  |
| ADC\_VREF-1 |  |  |  |
| ADC\_VREF-2 |  |  |  |
| AVREF-0 |  |  |  |
| AVREF-1 |  |  |  |
| DAC\_REFIO-700 |  |  |  |

#### Test Notes

Delete me if not required.

## µController Programming

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in Programming Connections.

### Test Instructions

Connect a SWD programmer to the SWD header and upload an image, validate the µController is properly programmed. Connect a JTAG programmer to the backplane and upload an image, validate the µController is properly programmed.

Note: Follow the programming instructions on the [wiki](http://cougs.space/wiki).

### Test Data

| Program the µController via SWD and JTAG, validate the µController is properly programmed | | |
| --- | --- | --- |
| Programmer | Passing Criteria | Pass / Fail |
| SWD | µController properly programmed |  |
| JTAG | µController properly programmed |  |

### Test Notes

Delete me if not required

## 5.0V and 9.0V Regulator

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in 5.0V Regulation. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources

### Output Voltage

#### Test Instructions

Apply 3.7V to VBATT. Measure the voltage of the 5.0V regulator under no load and under a resistive load.

Note: Measure the DC component with PLC[[34]](#footnote-34) > 100

#### Test Data

| Measure the voltage of the 5.0V regulator under no load and under a resistive load | | | | |
| --- | --- | --- | --- | --- |
| Regulator | No Load Voltage | Load Voltage | Passing Criteria | Pass / Fail |
| 5.0V |  |  |  |  |

#### Test Notes

Delete me if not required

### Output Ripple and Noise

#### Test Instructions

Apply 3.7V to VBATT. Measure the ripple and noise of the 5.0V regulator whilst under a resistive load.

Note: Measure the RMS AC component with

#### Test Data

| Measure the ripple and noise of the 5.0V regulator whilst under a resistive load. | | | |
| --- | --- | --- | --- |
| Regulator | Capture the ripple and noise | Passing Criteria | Pass / Fail |
| 5.0V |  |  | Pass |

### Output Efficiency

#### Test Instructions

Measure the efficiency of the 5.0V regulator whilst under a resistive loads and with input voltage on VBATT.

Note: , measure the power across the input and output current shunt resistors.

#### Test Data – 5.0V

| Measure the efficiency of the 5.0V regulator whilst under a resistive load and input voltage. | | | | | |
| --- | --- | --- | --- | --- | --- |
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

| Measure the efficiency of the 5.0V regulator whilst under a resistive load and input voltage. | | | | | |
| --- | --- | --- | --- | --- | --- |
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

| Measure the efficiency of the 5.0V regulator whilst under a resistive load and input voltage. | | | | | |
| --- | --- | --- | --- | --- | --- |
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

| Measure the efficiency of the 5.0V regulator whilst under a resistive load and input voltage. | | | | | |
| --- | --- | --- | --- | --- | --- |
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

| Measure the efficiency of the 5.0V regulator whilst under a resistive load and input voltage. | | | | | |
| --- | --- | --- | --- | --- | --- |
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

| Measure the efficiency of the 5.0V regulator whilst under a resistive load and input voltage. | | | | | |
| --- | --- | --- | --- | --- | --- |
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

#### Efficiency Plot

Create a plot of current versus efficiency with each input voltage.

#### Test Notes

Delete me if not required

### Current Limit

#### Test Instructions

Apply 3.7V to VBATT. Apply an increasing load to the 5.0V output until the current no longer increases. Measure voltage and current of the rail.

Note: The load will likely be increased by adding more resistors in parallel or decrease the load resistance.

#### Test Data

| Apply an increasing load to *3.3V* outputs until the current no longer increases | | | |
| --- | --- | --- | --- |
| *Regulator* | Max Current | Passing Criteria | Pass / Fail |
| 5.0V |  |  |  |

#### Test Notes

Delete me if not required

### Load Response

#### Test Instructions

Apply 3.7V to VBATT. Apply the following loads to the regulator output:

* No load to resistive load
* resistive load to no load
* No load to MLCC
* resistive load adding MLCC
* No load to short circuit
* Short circuit to no load
* resistive load to short circuit
* Short circuit to resistive load
* Short circuit continuous

Capture the voltage, and current of the rail under test and the voltage of *VBATT*. Validate the Comms does not misoperate in any way.

#### Test Data

| To the regulator output, apply no load to resistive load | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

| To the regulator output, apply resistive load to no load | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

| To the regulator output, apply no load to MLCC | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

| To the regulator output, apply resistive load and add MLCC | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

| To the regulator output, apply no load to short circuit | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

| To the regulator output, apply short circuit to no load | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

| To the regulator output, apply resistive load to short circuit | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

| To the regulator output, apply short circuit to resistive load | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

| To the regulator output, apply short circuit continuous load | | | |
| --- | --- | --- | --- |
| Regulator | Capture voltage and current of the rail and the voltage of *VBATT* | Passing Criteria | Pass / Fail |
| 5.0V |  | No misoperation |  |

#### Test Notes

Delete me if not required

## Low Drop-Out Regulators

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in Low Drop-Out Regulators. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources

### Output Voltage

#### Test Instructions

Apply to VBATT and to 3.3V. Measure the voltage of the 3.1V-1 regulator under no load and under an resistive load.

Note: Measure the DC component with PLC[[35]](#footnote-35) > 100

#### Test Data

| Measure the voltage of the 3.1V-1 LDO regulator under no load and under a resistive load | | | | |
| --- | --- | --- | --- | --- |
| Regulator | No Load Voltage | Load Voltage | Passing Criteria | Pass / Fail |
| 3.1V-1 |  |  |  |  |

#### Test Notes

Delete me if not required

### Output Ripple and Noise

#### Test Instructions

Apply to VBATT and to 3.3V. Measure the ripple and noise of the 3.1V-1 LDO regulators whilst under a resistive load.

Note: Measure the rms AC component with

#### Test Data

| Measure the ripple of the 3.1V-1 LDO regulator whilst under a resistive load. | | | |
| --- | --- | --- | --- |
| Regulator | Measure the ripple | Passing Criteria | Pass / Fail |
| 3.1V-1 |  |  |  |

#### Test Notes

Delete me if not required

## RF Clock Generators

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in RF Clock Generators.

### Reference Clock Supply

#### Test Instructions

Measure the voltage of each reference clock’s supply. Ensure the voltage, including noise and ripple, is .

#### Test Data

| Measure the voltage of each reference clock’s supply. | | | |
| --- | --- | --- | --- |
| RF Chain | Voltage | Passing Criteria | Pass / Fail |
| 700mm Uplink |  |  |  |
| 700mm Downlink |  |  |  |

#### Test Notes

Delete me if not required

### Reference Clock Frequency

#### Test Instructions

Measure the frequency of each reference clock. Ensure the frequency is .

#### Test Data

| Measure the frequency of each reference clock output | | | |
| --- | --- | --- | --- |
| RF Chain | Oscillator output | Passing Criteria | Pass / Fail |
| 700mm Uplink |  |  |  |
| 700mm Downlink |  |  |  |

#### Test Notes

Delete me if not required

### Output Frequency

#### Test Instructions

Configure each generator to output its frequency as follows. Use a spectrum analyzer to measure the output. Ensure the frequency is within and bandwidth is less than .

* 700mm Uplink:
* 700mm Downlink:

Note: Measure the bandwidth at the point

#### Test Data

| Measure the frequency of each generator output with a spectrum analyzer | | | |
| --- | --- | --- | --- |
| RF Chain | Capture the generator output | Passing Criteria | Pass / Fail |
| 700mm Uplink |  |  |  |
| 700mm Downlink |  |  |  |

#### Test Notes

Delete me I not required

## Differential Drivers

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in DAC.

### Test Instructions

Have the µController generate a square wave on each modulator input with a frequency of . Validate the waveform and voltage levels at the gain resistors.

### Test Data

| Have the µController generate a square wave on each modulator input with a frequency of . | | | |
| --- | --- | --- | --- |
| Signal | Capture the single ended and differential signals | Passing Criteria | Pass / Fail |
| 700 ID |  | Within 3  Signal Integrity |  |
| 700 QD |  | Within 3  Signal Integrity |  |

## RF Chain – 700mm Downlink

**Results: Pass / Fail**

**Test Configuration:**

This test evaluates the circuit described in RF Modulator, Low Noise Amplifier, and 700mm Power Amplifier.

### Isolation Switch

#### Test Instructions

Have the µController gradually increase the power output of the downlink radio while the RF switch is set to downlink. Measure the power on the uplink radio input. Ensure this power does not exceed .

#### Test Data

| Have the µController gradually increase the power output of the downlink radio while the RF switch is set to downlink. Measure the power on the uplink radio input. Ensure this power does not exceed . | | |
| --- | --- | --- |
| Max power | Passing Criteria | Pass / Fail |
|  |  |  |

#### Test Notes

Delete me if not required.

### Digital Modulation

#### Test Instructions

Have the µController generate a QPSK modulated signal with pattern with a data rate of on the radio. Validate the following parameters:

* Power output of when power amplifier bias is set to maximum
* Spectral bandwidth of less than
* Distinct separation of symbols

#### Test Data

| Have the µController generate a QPSK modulated signal with pattern with a data rate of on the radio. | | | |
| --- | --- | --- | --- |
| Parameter | Value  (Scope or Spectrum Analyzer Capture) | Passing Criteria | Pass / Fail |
| Output Power |  |  |  |
| Spectral Bandwidth |  |  |  |

| Have the µController generate a QPSK modulated signal with pattern with a data rate of on the radio. Use an SDR to demodulate into symbols | | |
| --- | --- | --- |
| Capture the I/Q signals (waveforms and constellation) | Passing Criteria | Pass / Fail |
|  | Distinct Symbols |  |

#### Test Notes

Delete me if not required

### Analog Modulation

#### Test Instructions

Have the µController generate an amplitude modulated audio signal on the radio. Validate the following parameters:

* Power output of when power amplifier bias is set to maximum
* Spectral bandwidth of less than
* Recognizable demodulated audio

#### Test Data

| Have the µController generate an amplitude modulated audio signal on the radio. | | | |
| --- | --- | --- | --- |
| Parameter | Value  (Scope or Spectrum Analyzer Capture) | Passing Criteria | Pass / Fail |
| Output Power |  |  |  |
| Spectral Bandwidth |  |  |  |

| Have the µController generate an amplitude modulated audio signal on the radio. Use an SDR to demodulate into audio. | | |
| --- | --- | --- |
| Capture the I/Q signals (waveforms) | Passing Criteria | Pass / Fail |
|  | Recognizable audio |  |

#### Test Notes

Delete me if not required

## RF Chain – 700mm Uplink

**Results: Pass / Fail**

**Test Configuration: Doug**

This test evaluates the circuit described in RF Demodulator, and Low Noise Amplifier.

### Test Instructions

Have a radio generate a QPSK modulated signal with pattern with a data rate of to transmit to the radio with a received power of . Validate the following parameters:

* Signal to noise ratio (SNR)
* Output voltage of
* Distinct separation of symbols

### Test Data

| Have a radio generate a QPSK modulated signal with pattern with a data rate of to transmit to the radio with a received power of . | | | |
| --- | --- | --- | --- |
| Parameter or Signal | Value  (Scope or Spectrum Analyzer Capture) | Passing Criteria | Pass / Fail |
| SNR |  |  |  |
| DEMOD\_ID |  |  |  |
| DEMOD\_QD |  |  |  |

| Have a radio generate a QPSK modulated signal with pattern with a data rate of to transmit to the radio with a received power of . | | |
| --- | --- | --- |
| Capture the I/Q signals (waveforms and constellation) | Passing Criteria | Pass / Fail |
|  | Distinct Symbols |  |

### Test Notes

Delete me if not required.

1. For more information, read [Wikipedia’s article](https://en.wikipedia.org/wiki/OSI_model) on the OSI model [↑](#footnote-ref-1)
2. For more information, read [Wikipedia’s article](https://en.wikipedia.org/wiki/Phase-shift_keying) on Phase Shift Keying (PSK) [↑](#footnote-ref-2)
3. Slant height is larger at lower elevations therefore more free space loss [↑](#footnote-ref-3)
4. Requirements COMMS-008, COMMS-009 [↑](#footnote-ref-4)
5. Open Systems Interconnection (OSI) Model [↑](#footnote-ref-5)
6. Requirements COMMS-001 [↑](#footnote-ref-6)
7. Requirement COMMS-005 [↑](#footnote-ref-7)
8. Requirement COMMS-006 [↑](#footnote-ref-8)
9. Requirement REQ-005 [↑](#footnote-ref-9)
10. CIS PN: [61-0003](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/61%20-%20%C2%B5Controller%20(and%20CLPD%2C%20FPGA%2C%20%20etc.)/61-0003) [↑](#footnote-ref-10)
11. For more information, see [ARM’s article](https://developer.arm.com/products/system-ip/coresight-debug-and-trace/coresight-architecture/serial-wire-debug) on SWD [↑](#footnote-ref-11)
12. For more information, see [Wikipedia’s article](https://en.wikipedia.org/wiki/JTAG) on JTAG [↑](#footnote-ref-12)
13. CIS PN: [09-0001](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/09%20-%20Communication%20IC/09-0001) [↑](#footnote-ref-13)
14. CIS PN: [27-0003](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/27%20-%20Conversion%20IC/27-0003) [↑](#footnote-ref-14)
15. For more information, see [Wikipedia’s article](https://en.wikipedia.org/wiki/Serial_Peripheral_Interface) on SPI [↑](#footnote-ref-15)
16. CIS PN: [29-0002](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/29%20-%20Memory/29-0002) [↑](#footnote-ref-16)
17. CIS PN: [08-0004](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/08%20-%20Amplifier%20(excluding%20RF)/08-0004) [↑](#footnote-ref-17)
18. CIS PN: [65-0005](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/60%20-%20Power%20IC/60-0005) [↑](#footnote-ref-18)
19. CIS PN: [60-0009](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/60%20-%20Power%20IC/60-0009) [↑](#footnote-ref-19)
20. Voltage difference between input and output [↑](#footnote-ref-20)
21. CIS PN: [65-0005](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/65%20-%20RF/65-0005) [↑](#footnote-ref-21)
22. CIS PN: [42-206B](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/42%20-%20Oscillator%20SMT/42-206B) [↑](#footnote-ref-22)
23. CIS PN: [27-0006](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/27%20-%20Conversion%20IC/27-0006) [↑](#footnote-ref-23)
24. CIS PN: [65-0002](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/65%20-%20RF/65-0002) [↑](#footnote-ref-24)
25. CIS PN: [65-0004](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/65%20-%20RF/65-0004) [↑](#footnote-ref-25)
26. CSI PN: [08-0002](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/08%20-%20Amplifier%20(excluding%20RF)/08-0002) [↑](#footnote-ref-26)
27. CIS PN: [65-0008](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/65%20-%20RF/65-0008) [↑](#footnote-ref-27)
28. CIS PN: [65-0011](https://github.com/CougsInSpace/Resources/tree/master/SupplierDocuments/65%20-%20RF/65-0011) [↑](#footnote-ref-28)
29. See [backplane documentation](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-Backplane/Documentation/Backplane-Design.pdf) for details [↑](#footnote-ref-29)
30. For more information, read [Microwaves101’s article](https://www.microwaves101.com/encyclopedias/coplanar-waveguide) on CPW [↑](#footnote-ref-30)
31. For more information, see [Microwaves101’s article](https://www.microwaves101.com/encyclopedias/microstrip) on microstrips [↑](#footnote-ref-31)
32. For test 3.1, place files in the subfolder *“3.1”* and so on [↑](#footnote-ref-32)
33. Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet [↑](#footnote-ref-33)
34. Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet [↑](#footnote-ref-34)
35. Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet [↑](#footnote-ref-35)