This document explains the function of the Comms, its schematic level design, its board level design, and its functional testing

Comms

In-Orbit Communication Subsystem Design

Revision: 1.1.0

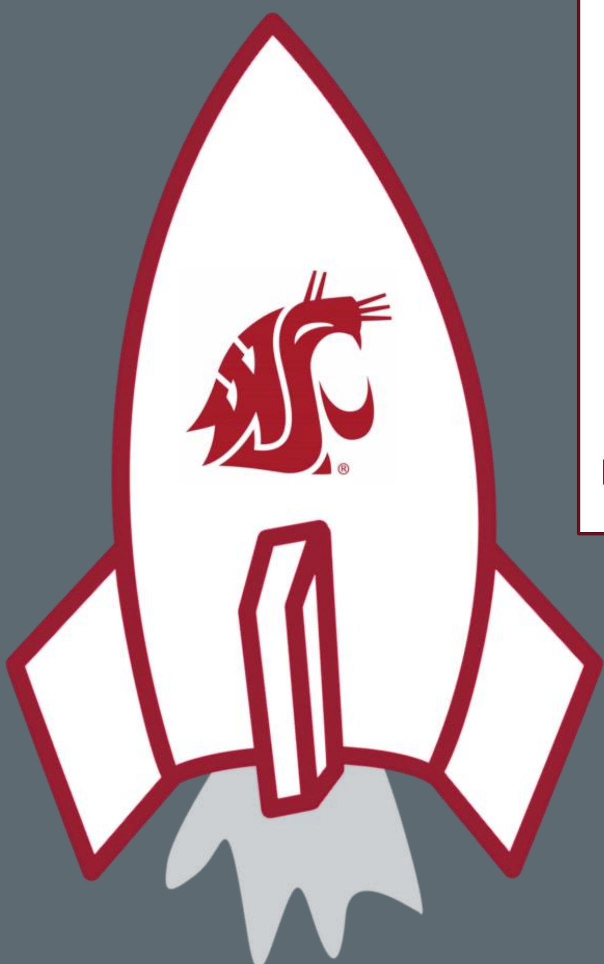

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Table of Contents

1 Introduction

This document explains how the Comms will fulfil the following Functions and conform to the following Requirements. This document refers to the Comms version 1.0, +X Panel version 1.0, and -Z Panel version 1.0.

1.1 Function

The In-Orbit Communication Subsystem (Comms) is responsible for the following:

- Transferring telemetry to the ground station
- Transferring payload data to the ground station
- Transferring commands from the ground station
- Transmitting a locating beacon

1.2 Requirements

The system requirements and Comms design requirements can be found on GitHub.

1.3 Open Systems Interconnection (OSI) Model

The OSI model[1] is a conceptual model that can be applied to any communication system. It has eight layers; each layer serves the layer above it and is served by the layer below it.

1.3.1 Layers

Layer			Protocol Data Unit	Function
Host layers	7	Application	Data	High-level APIs
	6	Presentation		Translation of data between a networking service and an application
	5	Session		Managing communication sessions
	4	Transport	Segment	Reliable transmission of data segments between points on a network
Media layers	3	Network	Packet	Structuring and managing a multi-node network
	2	Data link	Frame	Reliable transmission of data frames between two nodes connected by a physical layer
	1	Physical	Symbol	Transmission and reception of raw bit streams over a physical medium
	0	Medium	Electrons, Photons	The physical medium: copper, fiber, wireless

[1] For more information, read Wikipedia's article on the OSI model

1.3.2 CougSat Communication Subsystem

The communication subsystem, formed from the in-orbit and ground subsystems, fulfils layers 0 through 2 of the OSI model. The Comms serves the Command and Data Handling (C&DH) subsystem which fulfils layers 3 and up. The Ground serves itself for layers 3 and up which results in a graphical representation of the exchanged information. The in-orbit and ground subsystems are very similar as they are required to be compatible. For details on the ground subsystem, see its design document.

1.3.2.1 Layer 0

The communication subsystem is using wireless transmission, in the radio frequency band. There are two bands utilized: $700mm$ and $230mm$. The $700mm$ radio is the primary radio used for telemetry and beacon. The $230mm$ radio is the secondary radio used for payload data transfers and only operates in downlink mode.

1.3.2.2 Layer 1

The modulation scheme used is Quadrature Phase Shift Keying (QPSK)[2]. Each symbol is a change in the phase constant of the RF wave. The radios are software defined radios which allows reconfiguration of this layer if necessary. Other modulation schemes can be developed if the hardware supports it.

1.3.2.3 Layer 2

See the Comms µController's Framing Protocol.

1.3.2.4 Layer 3 and Up

See the Ground's Communication Protocol.

1.4 Link Budget

A link budget for downlink and uplink was tabulated indicating a transmit power of $1W$ is sufficient for up to $500kbps$ on the $230mm$ band. The $700mm$ band transmitter will incur less loses[3] and send slower data[4] so $1W$ is also sufficient. Uplink has no problems thanks to access to high gain and high-power transmitters on the ground.

[2] For more information, read Wikipedia's article on Phase Shift Keying (PSK)
[3] Free-space path loss is proportional to frequency squared
[4] A slower data rate has looser requirements for signal-to-noise ratio because there is more time to decode the symbol

2 Detailed Description

This section references the Comms schematic. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Comms µController

The Comms µController is responsible for interfacing the radio signals and the Command and Data Handling subsystem[5]. This fulfils OSI model[6] layers 1 and 2. It samples and synthesizes the baseband signals which are mixed with the carrier wave. This constitutes a software defined radio. The µController has non-volatile storage in the form of SPI Flash to store configurations and reference waveforms.

2.1.2 RF Clock Generators

Each radio has a configurable clock generator used to synthesize the carrier waves. For the transmission of the beacon, the generator is the direct source without any modulation to the antenna[7].

2.1.3 700mm Receiver Radio

Its RF diagram is the top row on page 2. The RF signal from the antenna is connected to the receiver radio via a high isolation RF switch. This switch prevents the transmitter from overdriving the sensitive receiver components and inducing damage. The signal is then amplified by low noise amplifiers which add very little noise to the signal to maintain the highest signal to noise ratio. The signal is then connected to the demodulator which removes the carrier frequency and splits that baseband signal into its in-phase and quadrature-phase signals which are then sampled by the Comms µController and demodulated into binary. The receiver radio is designed for continuous operation and low power[8].

2.1.4 700mm Transmitter Radio

Its RF diagram is the middle row on page 2. The Comms µController generates in-phase and quadrature-phase baseband signals using its digital to analog converter. This allows arbitrary waveform including voice signals[9]. These signals feed the modulator which puts the baseband signals on the carrier wave. This modulated RF gets amplified with a power amplifier to transmit the desired $1W$, see the Link Budget.

[5] Requirements COMMS-008, COMMS-009
[6] Open Systems Interconnection (OSI) Model
[7] Requirements COMMS-001
[8] Requirement COMMS-005
[9] Requirement COMMS-006

2.1.5 230mm Transmitter Radio

Its RF diagram is the bottom row on page 2. The Comms µController generates in-phase and quadrature-phase baseband signals using fast GPIO. This only allows each signal to be discrete positive or negative as found in QPSK modulation. If arbitrary waveforms are desired, an external DAC is needed. These signals feed the modulator which puts the baseband signals on the carrier wave. This modulated RF gets amplified with a power amplifier to transmit the desired $1W$, see the Link Budget.

2.1.6 5V & 9V Boost Converters

The RF chains require 5V and 9V supplies which come from boost converters. The converters are sourced from the battery rail.

2.2 Schematic

2.2.1 Isolated Grounds

On page 3 of the schematic (D1 & D2), are the six isolated grounds found on the Comms. Power ground *(PGND)* is directly connected to the backplane and the boost converters. Most of the other grounds are shorted to *PGND* using a 0Ω resistor rated up to $2A$, the expected current is less than $500mA$ each. Digital ground *(DGND)* connects to the digital circuity including the Comms µController. Analog ground *(AGND)* connects to analog circuits including the ADCs, the voltage references, the thermistors, and the operational amplifiers. *AGND* connects to *DGND*. Chassis ground *(CHASSIS)* is connected to the Mechanical Features including bolt holes and the card rails. The 230mm RF chain and the 700 RF chains each have their own RF grounds *(RFGND-0* and *RFGND-1,* respectively).

2.2.2 Power Rails

Page 3 of the schematic illustrates all the power rails on the Comms. Each RF chain can be turned off to save power and as a radio inhibit[10].

2.2.3 Comms µController

The Comms µController (page 4, A3, C1, C2, & C4) is a microcontroller from the STM32 low power family[11]. It was chosen for its ease of programming, and low power consumption. It needed fast ADCs and DACs for sampling and synthesizing the baseband signals.

The µController's reset pin is connected to the backplane such that if it or any subsystem needs to reset itself, all the subsystems reset. This is to put all the subsystems in a known state which reduces cause for error.

2.2.3.1 Programming Connections

During testing, the Comms µController is programmed via Serial Wire Debug[12] (SWD, page 4, A1). The process of programming is made simple with just a

[10] Requirement REQ-005
[11] STM32L476RG
[12] For more information, see ARM's article on SWD

single six pin header and a robust software utility. In orbit, the μController can be programmed via JTAG[13]. The In-Flight JTAG Reprogrammer (IFJR) connects via the backplane, through tri-state buffers/logic level converters[14] (page 4, C1:D2). The IFJR can enable or disable the tri-state buffer which essentially disconnects the JTAG interface from the Comms μController (it outputs high impedance), allowing the SWD to program. The logic level conversion feature is not used.

2.2.4 I²C Bus

The Comms μController has one I²C bus (page 4, C4). It connects to the monitoring ADCs.

2.2.4.1 ADCs

There are 3 ADCs[15] connected to the Comms μController, each with 16 single-ended inputs or eight differential inputs or a combination. The ADC was chosen for its low power, differential inputs, small package, and up to 27 addresses. The list of address follow:

- [`0xEE`] Global ADC address
- [`0x28`] ADC-0 (page 10, A2), voltage and current
- [`0x2A`] ADC-1 (page 10, A4), voltage and current
- [`0x2E`] ADC-2 (page 10, C2), voltage and current

The ADCs' mux output and ADC input have voltage dividers (page 10, B2, B4, & D2) that reduces the voltage of every input to place their level within the sensing range. Using paired resistors helps match the source impedance to the ADC across temperature. A mismatch results in an offset. The input range is $\frac{Vref}{2} * \frac{25k\Omega}{5k\Omega} = 4.5V$ but is limited by the IC's ESD diodes[16] to the supply rail of $3.3V$. To allow even high input voltages, those nets have series resistors (page 10, C1 & C3). With $20k\Omega, V = 3.3V * \frac{45k\Omega}{25k\Omega} = 5.9V$. With $50k\Omega, V = 3.3V * \frac{75k\Omega}{25k\Omega} = 9.9V$.

2.2.5 SPI Bus

The Comms μController has three SPI buses[17]. One connects to the C&DH to transfer packets and telemetry. One connects to the RF Clock Generators. One connects to the SPI Flash.

2.2.5.1 Backplane to the C&DH

The Comms μController is a slave to the C&DH, see the interface document for details.

[13] For more information, see Wikipedia's article on JTAG
[14] TXS0102
[15] LTC2499
[16] ESD diodes are reversed biased diodes between every pin and VCC and GND. When a pin is above VCC or below GND, these diodes conduct. The intent is to prevent ESD transients from harming the device, they are not designed for continuous conduction
[17] For more information, see Wikipedia's article on SPI

2.2.5.2 RF Clock Generators

The Comms µController is a transmit only master to the RF Clock Generators. Each generator has a tri-state buffer (page 8, A2, & C2; page 9, B2) which only connects the bus if the generator's rail is on. Without this, when the generator is turned off, its ESD diodes would prevent the bus from moving above *GND* effectively disabling the bus.

2.2.5.3 SPI Flash

The Comms µController is a master to two SPI Flash chips[18] (page 15) that provides $16Mb$ of mirrored storage or $32Mb$ of striped storage.

2.2.6 Current Monitoring

At various locations, the power chain has shunt resistors connected to ADCs in differential mode to monitor the current. Those locations are:

- 5V Regulator output (page 6, B6)
- 9V Regulator output (page 6, C6)
- Each RF chain input (page 7)

2.2.7 Voltage Monitoring

At various locations, the power chain is probed for the voltage using the ADCs in single ended mode. Those locations are:

- 5V Regulator output (page 6, B6)
- 9V Regulator output (page 6, C6)

2.2.8 Temperature Monitoring

At various locations, the temperature is monitored using thermistors and the ADCs in single ended mode. Those locations are:

- 5V Regulator (page 6, A3)
- 9V Regulator (page 6, C3)
- Comms µController (page 4, B4)
- RF clock generators (page 8, A4, C4; page 9, B4)
- 230mm downlink RF chain (page 11, B3, B5, & D4)
- 700mm downlink RF chain (page 12, B3, B5, & D5)
- 700mm uplink RF chain (page 13, B4 & C4; page 14, C4)

2.2.9 Analog Voltage Reference and Supply

The Comms has a precision voltage reference[19] (page 5, B6) for calibrating the ADCs. This is inputted into the ADCs' reference input.

The Comms has an analog voltage supply (page 5, C6) which is fed by the *3.3V* rail filtered with a ferrite bead and capacitors. Precision is not required as all ADCs use the precision voltage reference for calibration. This is the source for the Temperature Monitoring thermistors and operational amplifiers. A negative

[18] IS25LP016D
[19] MCP1501

voltage supply[20] for the op-amps takes the $3.3V$ rail and inverts it (page 10, C4:C6) to supply the op-amps' negative supply.

2.2.10 5.0V Regulation

The 5.0V regulator (page 6, B1:B6) is switching mode, boost topology. The converter[21] automatically senses the output voltage and adjusts the switching parameters to keep the output at $5.0V$. The converter has an integrated switching MOSFET. The converter was chosen for its small size and high efficiency. The output voltage is tuned to $5.1V$ to allow enough head room for the 5.0V Low Drop-Out Regulators to properly regulate.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

The converter and inductor (page 6, B2:B3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

2.2.11 9.0V Regulation

The 9.0V regulator (page 6, C1:C6) is switching mode, boost topology. The converter[22] automatically senses the output voltage and adjusts the switching parameters to keep the output at $9.0V$. The converter has an integrated switching MOSFET. The converter was chosen for its small size and high efficiency.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

The converter and inductor (page 6, C2:C3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

2.2.12 Low Drop-Out Regulators

The sensitive RF components are supplied through low drop-out (LDO) regulators[23] (page 7, B2, B4, B6, C2, C4, & C6). These are linear regulators that require a small drop-out[24] for proper regulation. They are used to reject the switching noise from the switching mode power supplies. The "3.3V" LDO regulators are might require the Electrical Power Subsystem to tune its 3.3V regulator to a higher voltage to allow enough head room for proper regulation.

[20] LM2776 and TPS732
[21] TPS61236
[22] TPS61089
[23] TPS73250 and LP5907
[24] Voltage difference between input and output

2.2.13 RF Clock Generators

The RF Clock Generators[25] (page 8, A3, & C3; page 9, B3) have a voltage-controlled oscillator and a phase-locked loop to take a reference clock and synthesize a RF wave. The reference clocks[26] (page 8, A3, & C3; page 9, C3) have high frequency stability and are supplied with ferrite beads to further increase frequency stability. The supporting circuitry for the generators was created using Analog Device's ADIsimPLL. The design files can be found under the documentation folder. The output of the generators is designed to drive a 50Ω load.

The 700mm Receiver Radio's demodulator divides its clock input by two, so the RF clock generator needs to output double the carrier frequency.

2.2.14 Differential Drivers

The Comms μController outputs its basebands signals $0\ to\ 3.3V$ single ended. The modulators' baseband signals are differential with a different amplitude. The differential output op-amps[27] (page 10, A1:D3) are used to perform this translation. The μController input is subtracted from a $1.65V$ reference (page 10, A4:A6) then multiplied by the proper gain to have the $3.3Vpp$ signal reduced to $1.0Vpp$ or $0.6Vpp$ as the modulator desires. This signal is then added to the proper common mode voltage reference (page 10, B4:B6, C4:C6). This circuit was simulated in LTSpice and can be found under electrical design. Precision resistors are used to reduce any common mode offset or gain imbalance.

2.2.15 RF Modulators

The 700mm Transmitter Radio's modulator (page 12, B3) and the 230mm Transmitter Radio's modulator (page 11, B3) have the RF Clock Generators AC coupled into their local oscillator input, and the Differential Drivers are directly connected to the baseband inputs. The RF output is AC coupled to the next element in the RF chain.

2.2.16 RF Demodulator

The 700mm Receiver Radio's demodulator (page 14, B3:B4) has the RF Clock Generators AC coupled into its local oscillator input. The 60.4Ω termination resistor is used to match a 50Ω input into the demodulator. The RF signal is connected to the modulator's input through a $1:4$ balun (page 13, B2) to match a 50Ω input into the demodulator. The gain of the demodulator is set by a voltage divider (page 14, B2) which is initially set to maximum gain.

The demodulator outputs differential baseband signals $1.0V \pm 500mV$. this amplified and translated to $1.65V \pm 1V$ single ended for input to the Comms

[25] ADF4360
[26] ECS-TXO-3225
[27] AD8137

µController's ADC by op-amps[28] (page 13, C2 & C5). This circuit was simulated in LTSpice and can be found under electrical design.

2.2.17 Low Noise Amplifier

The low noise amplifiers (LNA)[29] (page 11, B5; page 12, B5; page 13, B3 & C3) amplify the RF signal for the next component in the RF chain. They were chosen for their low noise figure, broadband response, and high gain. The gain is set by the bias voltage and is $19dB$. For the 700mm Receiver Radio's LNAs, the bias voltage can be shorted to ground which disables the amplifier. This is required, along with toggling the RF switch, when transmitting on $700mm$ to not damage the demodulator. The output is biased via a ferrite bead to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the next component.

2.2.18 Power Amplifiers

The power amplifiers[30] (page 10, C4; page 11, C4) are the final amplifiers for the RF signal. They drive the antennas and output the desired $1W$, see the Link Budget. They were chosen for the output power, linearity, and broadband response. The gain is set by the bias voltage of $-4\ to\ 0V$. The Comms µController outputs a PWM signal which is filtered and inverted to achieve an adjustable range of $-3.3V\ to\ 0V$. This is achieved by op-amps[31]. This circuit was simulated in LTSpice and can be found under electrical design. The output is biased via an inductor to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the antennae.

2.2.19 Mechanical Features

The 5V & 9V Boost Converters heatsink (page 6, D1:D2) and RF chain heatsinks (page 11, D1; page 12, A1) mount directly to the Comms board using bolts. These holes are conductive and connected directly to *CHASSIS*, see Isolated Grounds. The Comms also slots into the structure using rails[32] which are also conductive and connected directly to *CHASSIS*. Each of the holes have a capacitor and resistor connecting to power ground which will absorb and dissipate transients.

2.3 Board

The board shall also conform to the dimensions specified by the CougSat Module Standard.

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[28] AD8515
[29] MAAP-011229
[30] MAAP-011232
[31] AD8515
[32] See backplane documentation for details

2.3.1 Layer Stack-Up

The board shall be four layered with ENIG finish, see Figure 1. Only through vias shall be used. The external copper weight shall be $35\mu m$ and the internal copper weight shall be $18\mu m$.

Layer	Thickness	Primary Function
1 (top)	$35\mu m$ $(1oz)$	SMD components, RF & signal traces
Prepreg	$200\mu m$	
2	$18\mu m$ $(0.5oz)$	Ground planes
Core	$500\mu m$	
3	$18\mu m$ $(0.5oz)$	Power planes
Prepreg	$200\mu m$	
4 (bottom)	$35\mu m$ $(1oz)$	Signal traces

Figure 1: Stack-Up

2.3.2 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless otherwise specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width: $0.16mm$
Vias: $\emptyset 0.3mm$, unlimited count
Separation: $0.16mm$
Length: unlimited

Devices with specific placement and routing considerations are called out on the schematic, see "CAD Note:"

2.3.2.1 All 50Ω Impedance Traces

This applies to all RF traces expect the demodulator's RF input. These traces shall be a coplanar waveguide with ground[33].

Trace width: $0.35mm$
Gap width: $0.16mm$
Vias: none
Length: minimize

2.3.2.2 All 200Ω Impedance Traces

This applies to the demodulator's RF input. These traces shall be an edge coupled microstrip[34] with differential impedance of 200Ω. Ground located on second layer below ($0.8mm$ substrate thickness).

Trace width: $0.16mm$
Gap width: $0.4mm$
Vias: none
Length: minimize

[33] For more information, read Microwaves101's article on CPW
[34] For more information, see Microwaves101's article on microstrips

2.3.2.3 All Differential Signals
This applies to the modulators' inputs. Single ended to/from differential shall occur as close to the single ended side as possible.

Trace width: $0.16mm$
Gap width: $0.16mm$
Length: Length match $\pm 1.0mm$
Vias: minimize

2.3.2.4 Regulator Inputs – VBATT, PGND
This applies to *VBATT* and *PGND* between the backplane and the inputs to the regulators and their input capacitors.

Trace width: $1.0mm$ ($2.0mm$ on internal layers)

2.3.2.5 Regulator Outputs – 5.0V, 9.0V, PGND
PGND applies to between the regulators, their output capacitors, and the backplane.

Trace width: $0.5mm$ ($1.0mm$ on internal layers)

2.3.2.6 Regulator Channels – 3.3V_[0:3], 5.0V_[0:3], 9.0V_[0:1], PGND
PGND applies to between the regulators, their loads, and the backplane.

Trace width: $0.5mm$ ($1.0mm$ on internal layers)

2.3.2.7 SPI Buses – SPI_[SCK, MOSI, MISO, CS], RFCLK_[SCK, MOSI, CS], COM_SPI_[SCK, MOSI, MISO, CS]
Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

2.3.2.8 JTAG – JTAG_[TCK, TDI, TDO, TMS], BUS_JTAG-[TCK, TDI, TDO, TMS]
Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

2.3.2.9 I²C – I2C_[SCL, SDA]
Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

3 Testing

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test[35].

- Waveforms shall be captured whenever appropriate
- Have the event take fill the screen (for fast events, zoom in; for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-PowerBoard/Testing/Comms.1.0

Common test instructions can be found on the wiki.

3.1 Before First Power-On Check

Test Configuration: Doug

This test is required to be executed before any external power is applied to the Comms.

3.1.1 Test Instructions

Measure the resistance of various points in reference to *PGND* located at the backplane. This is informational only.

3.1.2 Test Data

Node	Resistance		Node	Resistance
VBATT	$33k\Omega$		3.3V	420Ω
3.3V-0	$3.8k\Omega$		3.3V-1	$3.8k\Omega$
3.3V-2	510Ω		5.0V	530Ω
5.0V-0	$3.3k\Omega$		5.0V-1	$3.4k\Omega$
5.0V-2	510Ω		9.0V	520Ω
9.0V-0	1.2Ω		9.0V-1	1.2Ω
I2C_SCL	$4.7k\Omega$		I2C_SDA	$4.6k\Omega$

3.1.3 Test Notes

Not measuring the shunt resistors as the DMM is not precise at that level.

[35] For test 3.1, place files in the subfolder *"3.1"* and so on

3.2 Power Rail Switching

Results: Fail
Test Configuration: Doug

This test evaluates the circuit described in Power Rails.

3.2.1 Test Instructions

Hold the µController in reset or program a blank image, verify the power rails are powered off. Have the µController enable the power rail, verify the power rails are powered on, ensuring the rail turns on only with its control signal.

3.2.2 Test Data

Hold the µController in reset, measure the voltage of each power rail			
Rail	Voltage	Passing Criteria	Pass / Fail
3.3V-0	$\approx 2mV$	Voltage < $50mV$	Pass
3.3V-1	$\approx 2mV$	Voltage < $50mV$	Pass
3.3V-2	$\approx 2mV$	Voltage < $50mV$	Pass
5.0V-0	$\approx 250mV$	Voltage < $50mV$	Fail
5.0V-1	$\approx 250mV$	Voltage < $50mV$	Fail
5.0V-2	$\approx 250mV$	Voltage < $50mV$	Fail
9.0V-0	$\approx 0.0mV$	Voltage < $50mV$	Pass
9.0V-1	$\approx 0.0mV$	Voltage < $50mV$	Pass

Have the µController enable the power rail, measure the voltage of each power rail. Ensure the rail turns on only with its control signal				
Rail	Control Signal	Voltage	Passing Criteria	Pass / Fail
3.3V-0	PC_LDO_3.3V	$\approx 3.3V$	Voltage > $3V$	Pass
3.3V-1	PC_LDO_3.3V	$\approx 3.3V$	Voltage > $3V$	Pass
3.3V-2	PC_LDO_3.3V	$\approx 3.3V$	Voltage > $3V$	Pass
5.0V-0	PC_MOD_230	$\approx 5.0V$	Voltage > $4V$	Pass
5.0V-1	PC_MOD_700	$\approx 5.0V$	Voltage > $4V$	Pass
5.0V-2	PC_DEMOD	$\approx 5.0V$	Voltage > $4V$	Pass
9.0V-0	PC_MOD_230	$\approx 9.0V$	Voltage > $8V$	Pass
9.0V-1	PC_MOD_700	$\approx 9.0V$	Voltage > $8V$	Pass

3.2.3 Test Notes

The backfeeding when off is from the inputs through the modulator and demodulator's ESD diodes. This can be fixed with the power down pin on the analog circuitry.

The 3.3V LDOs do responds properly to PC_LDO_3.3V but the software is not properly controlling that signal.

3.3 I²C Bus

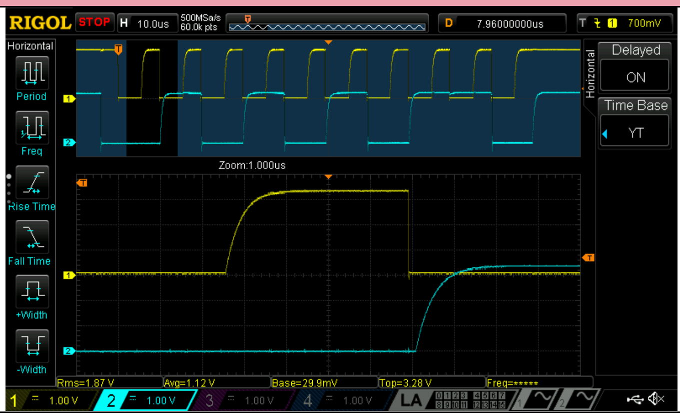
Results: Pass
Test Configuration: Doug

This test evaluates the circuit described in I²C Bus.

3.3.1 Test Instructions

At the pull up resistors of the *I2C* bus, validate signal integrity. The µController should generate random I²C traffic on the bus.

3.3.2 Test Data

At the pull up resistors of the *I2C* bus, validate the following timing parameters		
Capture the *SDA* and *SCL* lines	Passing Criteria	Pass / Fail
	Signal Integrity	Pass

3.4 SPI Flash

Results: Pass
Test Configuration: Doug

This test evaluates the circuit described in SPI Bus.

3.4.1 Test Instructions

Perform write and read operations to the SPI Flash chips. Verify functionality.

3.4.2 Test Data

Perform write and read operations to the SPI Flash chips. Verify functionality.			
Chip	Direction	Passing Criteria	Pass / Fail
U8	Read	Functionality	Pass
U8	Write	Functionality	Pass
U9	Read	Functionality	Pass
U9	Write	Functionality	Pass

3.5 Current Monitoring

Results: Fail

This test evaluates the circuit described in Current Monitoring.

3.5.1 Test Instructions

Apply a $10mA\ to\ 250mA$ resistive load to a *9.0V-0*. Compare the current measured by the Comms and a DMM.

Note: $Error = \frac{|I_{Comms} - I_{DMM}|}{I_{DMM}}$

3.5.2 Test Data

Apply a $10mA$ to $250mA$ resistive load to a single output channel. Compare the current measured by the Comms and a DMM					
Load	EPS Current	DMM Current	Error	Passing Criteria	Pass / Fail
$10mA$				$Error < 1.0\%$	
$25mA$				$Error < 1.0\%$	
$50mA$				$Error < 1.0\%$	
$100mA$				$Error < 1.0\%$	
$250mA$				$Error < 1.0\%$	

3.5.3 Test Notes

ADCs are being replaced.

3.6 Voltage Monitoring

Results: Fail

This test evaluates the circuit described in Voltage Monitoring.

3.6.1 Test Instructions

Compare the voltage measured by the Comms and a DMM on the following signals:

- *I_3.3V-0N*
- *I_3.3V-1P*
- *5.0V*

Note: $Error = \frac{|V_{Comms} - V_{DMM}|}{V_{DMM}}$

3.6.2 Test Data

Compare the voltage measured by the Comms and a DMM					
Signal	Comms Voltage	DMM Voltage	Error	Passing Criteria	Pass / Fail
I_3.3V-0N				$Error < 1.0\%$	
I_3.3V-1P				$Error < 1.0\%$	
5.0V				$Error < 1.0\%$	

3.6.3 Test Notes

ADCs are being replaced

3.7 Temperature Monitoring

Results: Fail

This test evaluates the circuit described in Temperature Monitoring.

3.7.1 Test Instructions

Compare the temperature measured by the Comms and a thermometer on the following temperature sensors:

- 5.0V Regulator
- µController
- +X+Y

Note: $Error = |T_{Comms} - T_{THERMOMETER}|$

3.7.2 Test Data

Compare the temperature measured by the Comms and a thermometer					
Sensor	Comms Temperature	Thermometer Temperature	Error	Passing Criteria	Pass / Fail
5.0V Regulator				$Error < 2°C$	
µController				$Error < 2°C$	
+X+Y				$Error < 2°C$	

3.7.3 Test Notes

ADCs are being replaced

3.8 Analog Voltage Reference

Results: Pass
Test Configuration: Doug

This test evaluates the circuit described in Analog Voltage Reference and Supply and Differential Drivers. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources.

3.8.1 Voltage

3.8.1.1 Test Instructions

Measure the voltage of the following signals:

- *AVREF*
- *VREF_CM_IN*
- *VREF_CM_OUT_230*
- *VREF_CM_OUT_700*

Note: Measure the DC component with PLC[36] > 100

3.8.1.2 Test Data

Measure the voltage of the following signals			
Signal	Voltage	Passing Criteria	Pass / Fail
AVREF	$1.80003V$	$1.7982V < V < 1.8018V$	Pass
VREF_CM_IN	$1.64596V$	$1.635V < V < 1.665V$	Pass
VREF_CM_OUT_300	$1.20014V$	$1.215V < V < 1.225V$	Pass

[36] Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

Measure the voltage of the following signals			
Signal	Voltage	Passing Criteria	Pass / Fail
VREF_CM_OUT_700	$0.69807V$	$0.695V < V < 0.705V$	Pass

3.8.2 Ripple and Noise

3.8.2.1 Test Instructions

Measure the ripple and noise of the following signals:

- *AVREF*
- *VREF_CM_IN*
- *VREF_CM_OUT_230*
- *VREF_CM_OUT_700*

Note: Measure the RMS AC component with $3Hz < f$

3.8.2.2 Test Data

Measure the RMS voltage ripple and noise of the following signals			
Signal	Voltage	Passing Criteria	Pass / Fail
AVREF	$0.295mV$	$\|V_{rms}\| < 1.80mV$	Pass
VREF_CM_IN	$1.223mV$	$\|V_{rms}\| < 1.60mV$	Pass
VREF_CM_OUT_300	$< 100nV$	$\|V_{rms}\| < 1.20mV$	Pass
VREF_CM_OUT_700	$< 100nV$	$\|V_{rms}\| < 0.70mV$	Pass

3.8.2.3 Test Notes

The large ripple of VREF_CM_IN is from it being a relative reference to the 3.3V rail instead of an absolute reference.

3.9 µController Programming

Results: Pass
Test Configuration: Doug

This test evaluates the circuit described in Programming Connections.

3.9.1 Test Instructions

Connect a SWD programmer to the SWD header and upload an image, validate the µController is properly programmed. Connect a JTAG programmer to the backplane and upload an image, validate the µController is properly programmed.

Note: Follow the programming instructions on the wiki.

3.9.2 Test Data

Program the µController via SWD and JTAG, validate the µController is properly programmed		
Programmer	Passing Criteria	Pass / Fail
SWD	µController properly programmed	Pass

Program the µController via SWD and JTAG, validate the µController is properly programmed		
Programmer	Passing Criteria	Pass / Fail
JTAG	µController properly programmed	

3.9.3 Test Notes
We do not have a JTAG programmer currently, it will be tested later.

3.10 5.0V and 9.0V Regulator
Results: Fail
Test Configuration: Doug

This test evaluates the circuit described in 5.0V Regulation and 9.0V Regulation. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources

3.10.1 Output Voltage

3.10.1.1 Test Instructions
Apply 3.7V to VBATT. Measure the voltage of the 5.0V and 9.0V regulators under no load and under a $200mA$ resistive load.

Note: Measure the DC component with PLC[37] > 100

3.10.1.2 Test Data

Measure the voltage of the 5.0V and 9.0V regulators under no load and under a $200mA$ resistive load				
Regulator	No Load Voltage	$200mA$ Load Voltage	Passing Criteria	Pass / Fail
5.0V	$5.2065V$	$5.1902V$	$5.05V < V < 5.25V$	Pass
9.0V	$9.0694V$	$8.9922V$	$8.55V < V < 9.45V$	Pass

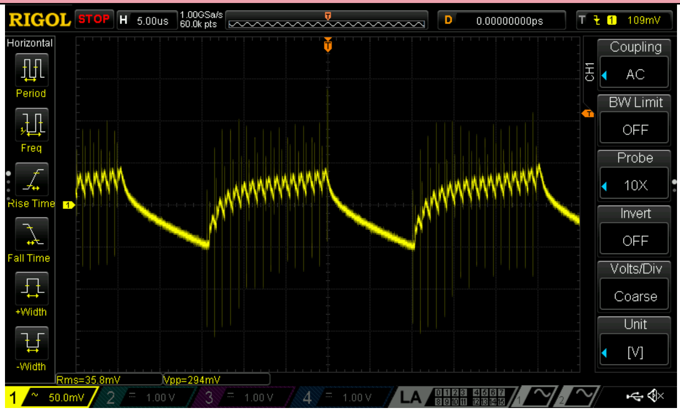
3.10.2 Output Ripple and Noise

3.10.2.1 Test Instructions
Apply 3.7V to VBATT. Measure the ripple and noise of the 5.0V and 9.0V regulators whilst under a $200mA$ resistive load.

Note: Measure the RMS AC component with $3Hz < f$

[37] Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

3.10.2.2 Test Data

Measure the ripple and noise of the 5.0V and 9.0V regulators whilst under a $200mA$ resistive load.			
Regulator	Capture the ripple and noise	Passing Criteria	Pass / Fail
5.0V	 DMM: $23.9mV$	$\|V_{rms}\| < 25mV$	Pass
9.0V	 DMM: $15.7mV$	$\|V_{rms}\| < 45mV$	Pass

3.10.3 Output Efficiency

3.10.3.1 Test Instructions

Measure the efficiency of the 5.0V and 9.0V regulators whilst under a $10mA\ to\ 200mA$ resistive loads and with $3.3V\ to\ 4.1V$ input voltage on VBATT.

Note: $Efficiency = \frac{P_{out}}{P_{in}}$, measure the power across the input and output current shunt resistors.

3.10.3.2 Test Data – 5.0V

Measure the efficiency of the 5.0V regulator whilst under a $10mA$ resistive load and $3.3V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$78.5\ mW$	$56.6\ mW$	72.1%	$Efficiency > 50\%$	Pass
$3.7V$	$78.3\ mW$	$57.0\ mW$	72.7%	$Efficiency > 50\%$	Pass
$4.1V$	$74.8\ mW$	$56.5\ mW$	75.4%	$Efficiency > 50\%$	Pass

Measure the efficiency of the 5.0V regulator whilst under a $20mA$ resistive load and $3.3V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$128.5\ mW$	$91.7\ mW$	71.3%	$Efficiency > 50\%$	Pass
$3.7V$	$127.3\ mW$	$91.9\ mW$	72.2%	$Efficiency > 50\%$	Pass
$4.1V$	$123.8\ mW$	$91.8\ mW$	74.2%	$Efficiency > 50\%$	Pass

Measure the efficiency of the 5.0V regulator whilst under a $50mA$ resistive load and $3.3V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$217.4\ mW$	$202.2\ mW$	93.0%	$Efficiency > 50\%$	Pass
$3.7V$	$215.7\ mW$	$202.2\ mW$	93.8%	$Efficiency > 50\%$	Pass
$4.1V$	$214.0\ mW$	$202.2\ mW$	94.5%	$Efficiency > 50\%$	Pass

Measure the efficiency of the 5.0V regulator whilst under a $100mA$ resistive load and $3.3V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$590.2\ mW$	$553.1\ mW$	93.7%	$Efficiency > 70\%$	Pass
$3.7V$	$585.4\ mW$	$554.1\ mW$	94.7%	$Efficiency > 70\%$	Pass
$4.1V$	$581.9\ mW$	$553.6\ mW$	95.1%	$Efficiency > 70\%$	Pass

Measure the efficiency of the 5.0V regulator whilst under a $200mA$ resistive load and $3.3V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$983.7\ mW$	$922.2\ mW$	93.8%	$Efficiency > 90\%$	Pass
$3.7V$	$980.9\ mW$	$927.0\ mW$	94.5%	$Efficiency > 90\%$	Pass
$4.1V$	$1149.2\ mW$	$1099.2\ mW$	95.6%	$Efficiency > 90\%$	Pass

3.10.3.3 Test Data – 9.0V

Measure the efficiency of the 9.0V regulator whilst under a $10mA$ resistive load and $3.3V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$135.3\ mW$	$101.7\ mW$	75.2%	$Efficiency > 50\%$	Pass
$3.7V$	$133.9\ mW$	$101.9\ mW$	76.1%	$Efficiency > 50\%$	Pass
$4.1V$	$133.2\ mW$	$102.4\ mW$	76.9%	$Efficiency > 50\%$	Pass

Measure the efficiency of the 9.0V regulator whilst under a $20mA$ resistive load and $3.3V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$212.5\ mW$	$178.3\ mW$	83.9%	$Efficiency > 50\%$	Pass
$3.7V$	$212.1\ mW$	$178.3\ mW$	84.0%	$Efficiency > 50\%$	Pass
$4.1V$	$213.0\ mW$	$178.1\ mW$	83.6%	$Efficiency > 50\%$	Pass

Measure the efficiency of the 9.0V regulator whilst under a $50mA$ resistive load and $3.3V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$471.9\ mW$	$425.2\ mW$	90.1%	$Efficiency > 50\%$	Pass
$3.7V$	$473.8\ mW$	$426.8\ mW$	90.1%	$Efficiency > 50\%$	Pass
$4.1V$	$471.4\ mW$	$427.9\ mW$	90.8%	$Efficiency > 50\%$	Pass

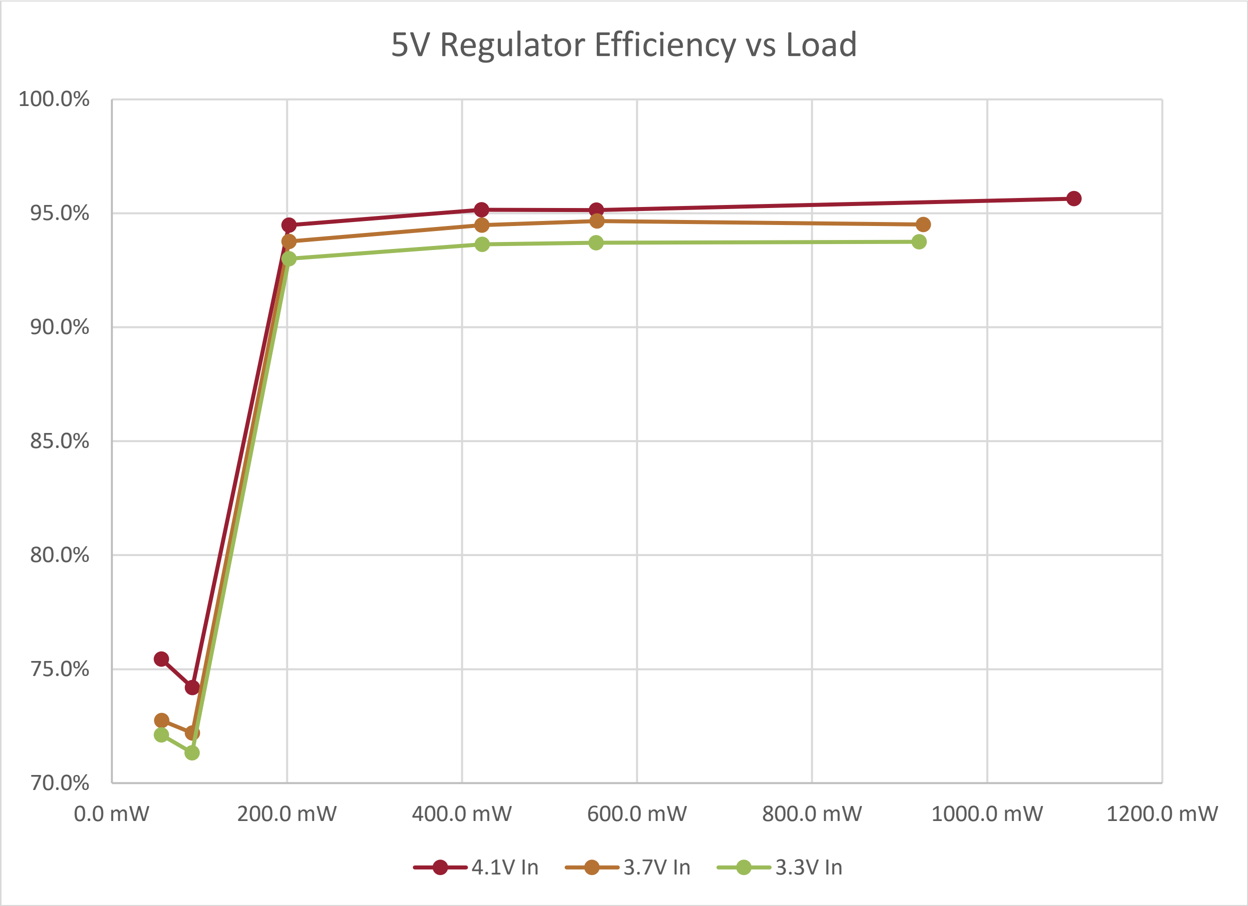
Measure the efficiency of the 9.0V regulator whilst under a $100mA$ resistive load and $3.3V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$928.4\ mW$	$857.8\ mW$	92.4%	$Efficiency > 80\%$	Pass
$3.7V$	$928.0\ mW$	$859.2\ mW$	92.6%	$Efficiency > 80\%$	Pass
$4.1V$	$922.1\ mW$	$858.4\ mW$	93.1%	$Efficiency > 80\%$	Pass

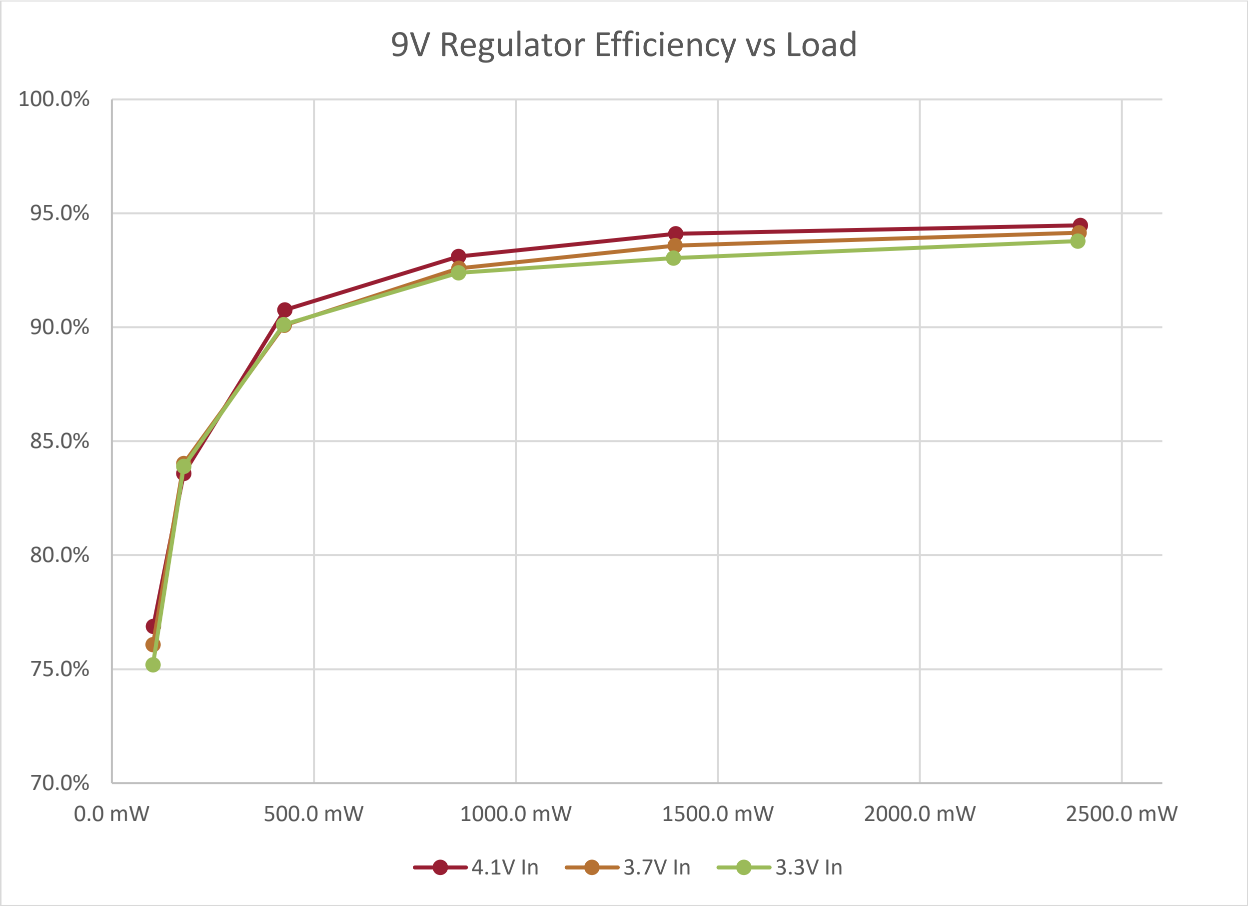
Measure the efficiency of the 9.0V regulator whilst under a $150mA$ resistive load and $3.3V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$1494\ mW$	$1390\ mW$	93.0%	$Efficiency > 80\%$	Pass
$3.7V$	$1489\ mW$	$1394\ mW$	93.6%	$Efficiency > 80\%$	Pass
$4.1V$	$1483\ mW$	$1396\ mW$	94.1%	$Efficiency > 80\%$	Pass

Measure the efficiency of the 9.0V regulator whilst under a $250mA$ resistive load and $3.3V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
$3.3V$	$2549\ mW$	$2391\ mW$	93.8%	$Efficiency > 90\%$	Pass
$3.7V$	$2543\ mW$	$2394\ mW$	94.2%	$Efficiency > 90\%$	Pass
$4.1V$	$2537\ mW$	$2397\ mW$	94.5%	$Efficiency > 90\%$	Pass

3.10.3.4 Efficiency Plot

Create a plot of current versus efficiency with each input voltage.


5V Regulator Efficiency vs Load
100.0%
95.0%
90.0%
85.0%
80.0%
75.0%
70.0%
0.0 mW
200.0 mW
400.0 mW
600.0 mW
800.0 mW
1000.0 mW
1200.0 mW
4.1V In
3.7V In
3.3V In



3.10.3.5 Test Notes

Note that the 5V regulator switches to PFM mode around 50mA which is the source of the cliff in the efficiency.

3.10.4 Current Limit

3.10.4.1 Test Instructions

Apply 3.7V to VBATT. For each regulator, apply an increasing load to its output until the current no longer increases. Measure voltage and current of the rail.

Note: The load will likely be increased by adding more resistors in parallel or decrease the load resistance.

3.10.4.2 Test Data

Apply an increasing load to *3.3V* outputs until the current no longer increases			
Regulator	Max Current	Passing Criteria	Pass / Fail
5.0V	$1.086A$	$500mA < I < 1.5A$	Pass
9.0V	2	$500mA < I < 1.5A$	Fail

3.10.4.3 Test Notes

Once the 5V regulator reached its limit, it stopped regulating. Any higher load would pull directly from VBATT.

The 9V regulator has a switching current limit not output current limit so it did not max out the current as desired. Also, increasing the load to $> 3A$ resulted in failure of the IC, not sure why.

3.10.5 Load Response

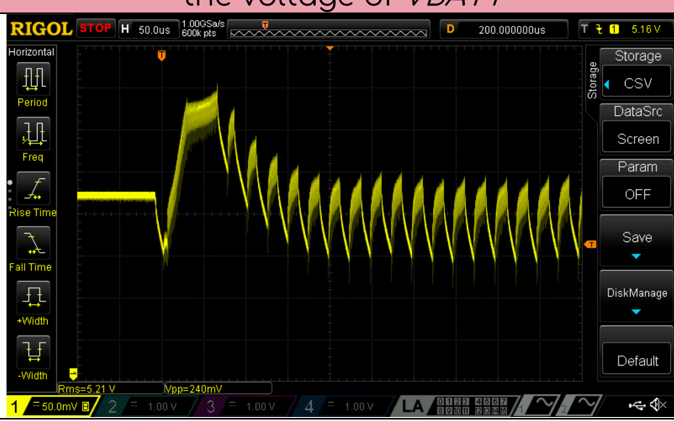
3.10.5.1 Test Instructions

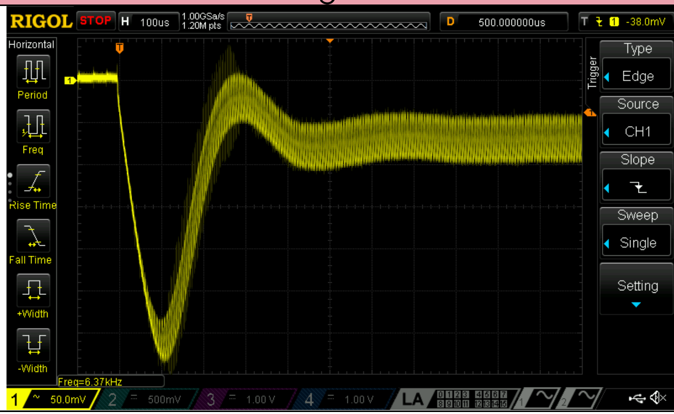
Apply 3.7V to VBATT. Apply the following loads to the both regulator outputs:

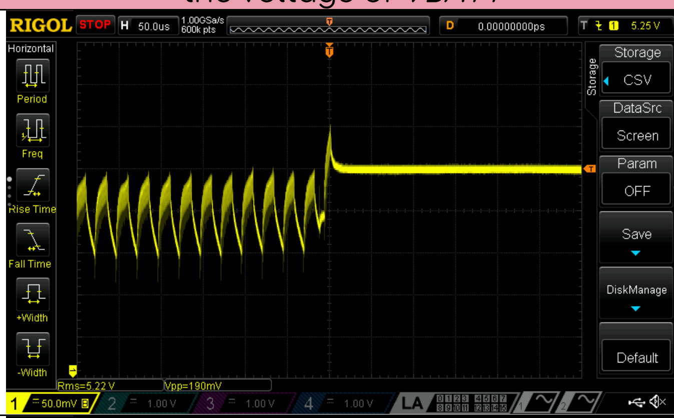
- No load to $200mA$ resistive load
- $200mA$ resistive load to no load
- No load to $10\mu F$ MLCC
- $200mA$ resistive load adding $10\mu F$ MLCC
- No load to short circuit
- Short circuit to no load
- $200mA$ resistive load to short circuit
- Short circuit to $200mA$ resistive load
- Short circuit continuous

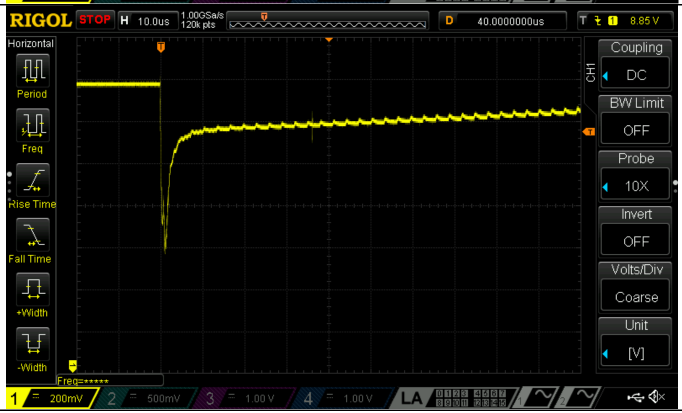
Capture the voltage, and current of the rail under test and the voltage of *VBATT*. Validate the Comms does not misoperate in any way.

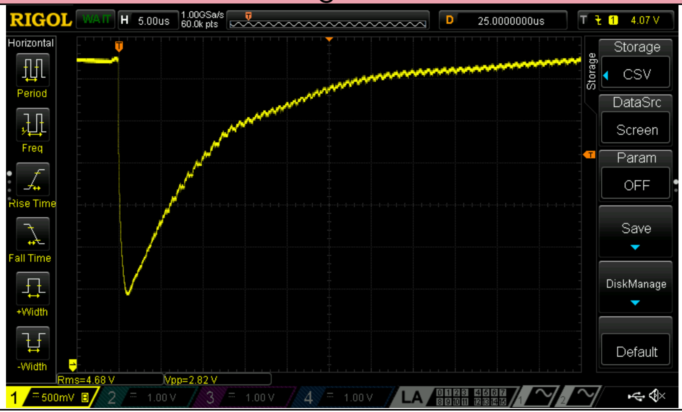
3.10.5.2 Test Data

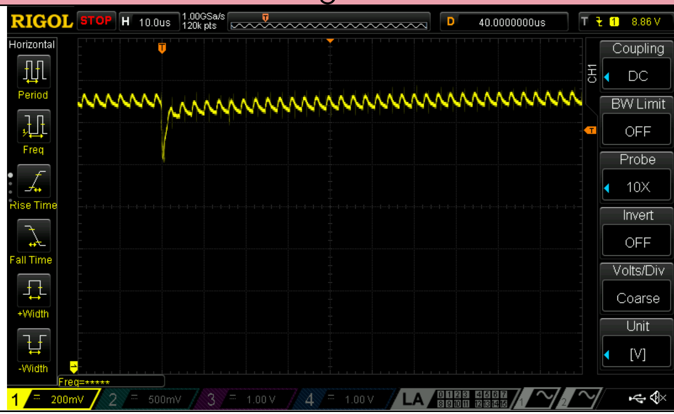
To each regulator output, apply no load to 200mA resistive load			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
5.0V		No misoperation	Pass

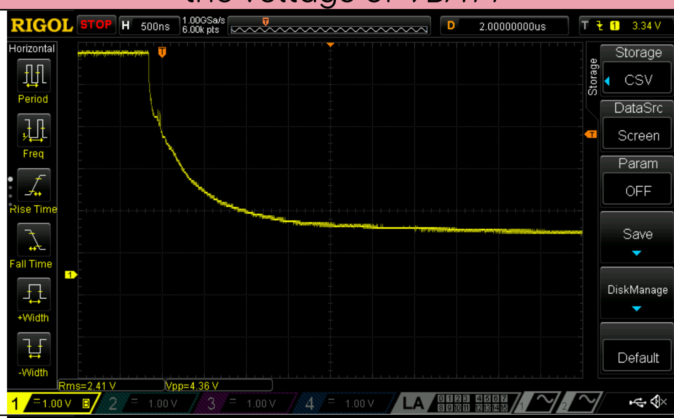
To each regulator output, apply no load to $200mA$ resistive load			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
9.0V		No misoperation	Pass

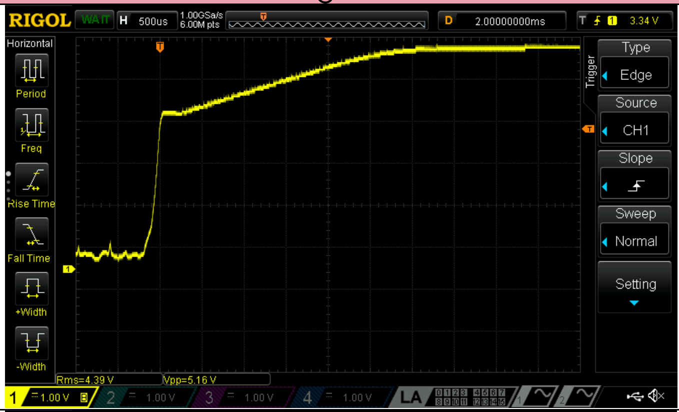
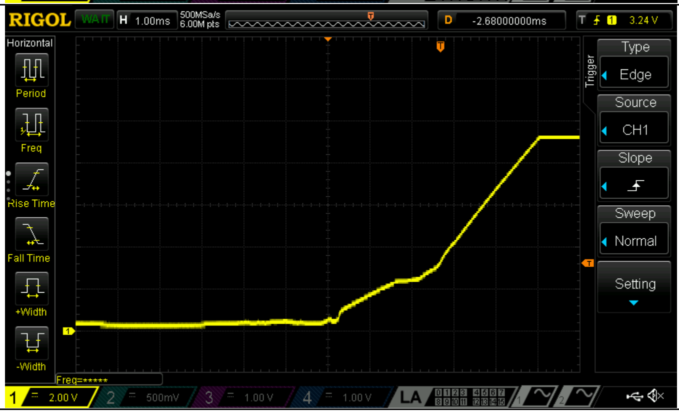
To each regulator output, apply $200mA$ resistive load to no load			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
5.0V		No misoperation	Pass
9.0V		No misoperation	Pass

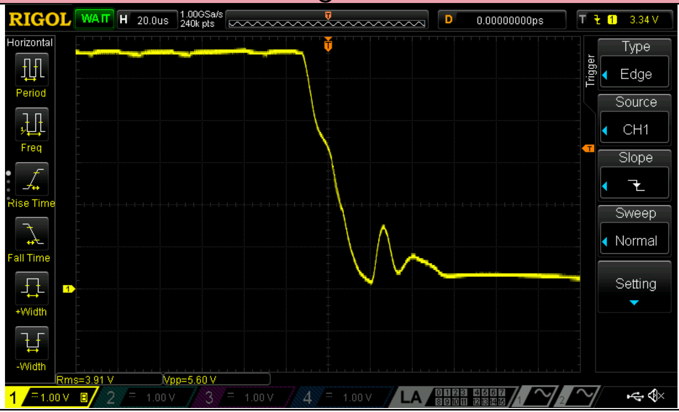
<table>
<tr><td colspan="4">To each regulator output, apply no load to $10\mu F$ MLCC</td></tr>
<tr><td>Regulator</td><td>Capture voltage and current of the rail and the voltage of VBATT</td><td>Passing Criteria</td><td>Pass / Fail</td></tr>
<tr><td>5.0V</td><td>
</td><td>No misoperation</td><td>Pass</td></tr>
<tr><td>9.0V</td><td>
</td><td>No misoperation</td><td>Pass</td></tr>
</table>

<table>
<tr><td colspan="4">To each regulator output, apply $200mA$ resistive load and add $10\mu F$ MLCC</td></tr>
<tr><td>Regulator</td><td>Capture voltage and current of the rail and the voltage of VBATT</td><td>Passing Criteria</td><td>Pass / Fail</td></tr>
<tr><td>5.0V</td><td>
</td><td>No misoperation</td><td>Pass</td></tr>
</table>

To each regulator output, apply $200mA$ resistive load and add $10\mu F$ MLCC			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
9.0V		No misoperation	Pass

To each regulator output, apply no load to short circuit			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
5.0V		No misoperation	Pass
9.0V		No misoperation	Pass

To each regulator output, apply short circuit to no load			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
5.0V		No misoperation	Pass
9.0V		No misoperation	Pass

To each regulator output, apply $200mA$ resistive load to short circuit			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
5.0V		No misoperation	Pass

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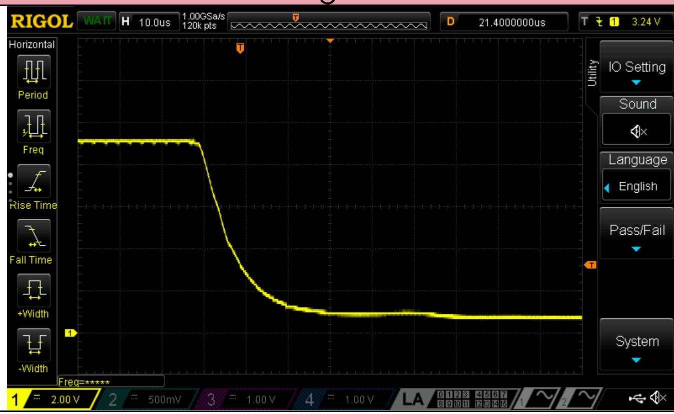
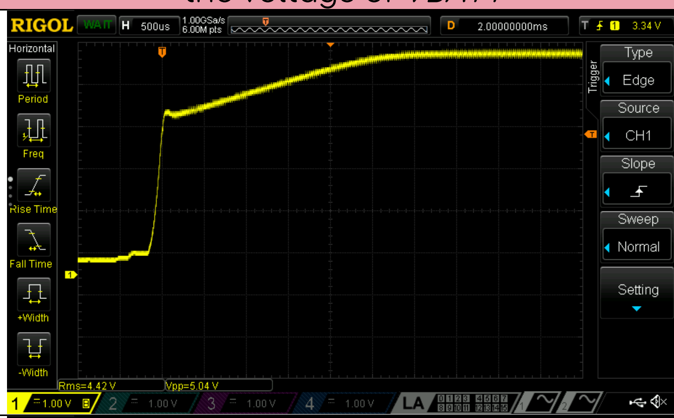
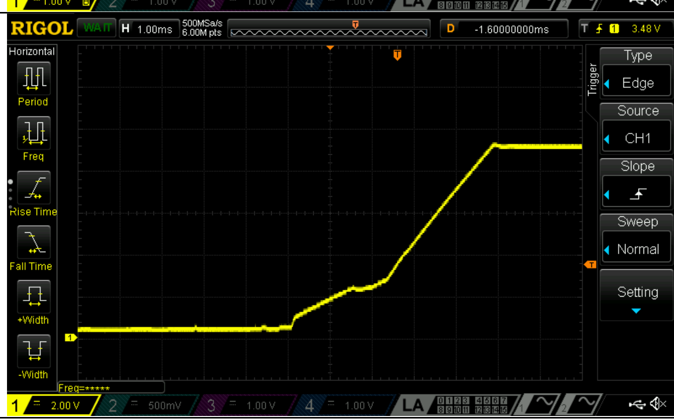
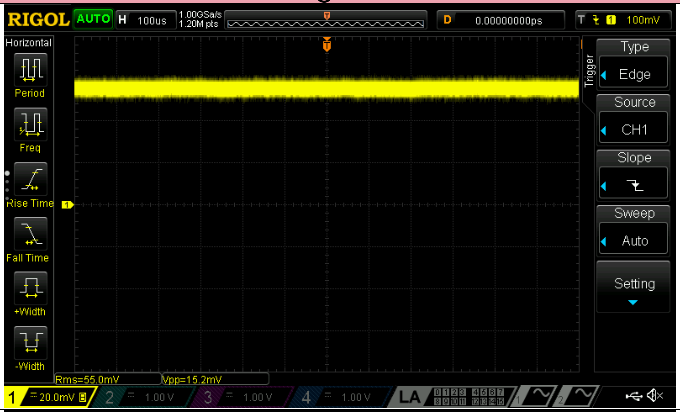
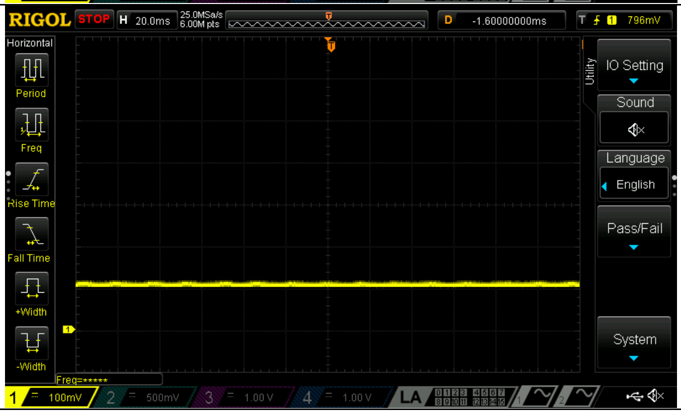
To each regulator output, apply $200mA$ resistive load to short circuit			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
9.0V		No misoperation	Pass

To each regulator output, apply short circuit to $200mA$ resistive load			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
5.0V		No misoperation	Pass
9.0V		No misoperation	Pass

To each regulator output, apply short circuit continuous load			
Regulator	Capture voltage and current of the rail and the voltage of *VBATT*	Passing Criteria	Pass / Fail
5.0V		No misoperation	Pass
9.0V		No misoperation	Pass

3.10.5.3 Test Notes

VBATT was sourced from the DC power supply set to $3.7V$ $1A$. The EPS has $1A$ overcurrent regulators on each power rail.

3.11 Low Drop-Out Regulators

Results: Pass
Test Configuration: Doug

This test evaluates the circuit described in Low Drop-Out Regulators. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources

3.11.1 Output Voltage

3.11.1.1 Test Instructions

Apply $3.7V$ to VBATT and $3.3V$ to 3.3V. Measure the voltage of the 3.3V-0 and 5.0V-0 LDO regulators under no load and under an $50mA$ resistive load.

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Note: Measure the DC component with PLC[38] > 100

3.11.1.2 Test Data

Measure the voltage of the 3.3V-0 and 5.0V-0 LDO regulators under no load and under a $50mA$ resistive load				
Regulator	No Load Voltage	$50mA$ Load Voltage	Passing Criteria	Pass / Fail
3.3V-0	$3.293V$	$3.255V$	$3.25V < V < 3.35V$	Pass
5.0V-0	Modulator always on	$4.992V$	$4.95V < V < 5.05V$	Pass

3.11.1.3 Test Notes

Modulator has its enable pin always tied high. It was drawing 75mA.

3.11.2 Output Ripple and Noise

3.11.2.1 Test Instructions

Apply 3.7V to VBATT and $3.3V$ to 3.3V. Measure the ripple and noise of the 3.3V-0 and 5.0V-0 LDO regulators whilst under a $50mA$ resistive load.

Note: Measure the rms AC component with $3Hz < f$

3.11.2.2 Test Data

Measure the ripple of the 3.3V-0 and 5.0V-0 LDO regulators whilst under a $50mA$ resistive load.			
Regulator	Measure the ripple	Passing Criteria	Pass / Fail
3.3V-0	$14.4mV$	$\|V_{rms}\| < 25mV$	Pass
5.0V-0	$5.82mV$	$\|V_{rms}\| < 45mV$	Pass

3.11.2.3 Test Notes

Modulator has its enable pin always tied high. It was drawing 75mA.

3.12 RF Clock Generators

Results: Fail
Test Configuration: Doug

This test evaluates the circuit described in RF Clock Generators.

3.12.1 Reference Clock Supply

3.12.1.1 Test Instructions

Measure the voltage of each reference clock's supply. Ensure the voltage, including noise and ripple, is $3.3V \pm 0.5\%$.

[38] Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

3.12.1.2 Test Data

Measure the voltage of each reference clock's supply.			
RF Chain	Voltage	Passing Criteria	Pass / Fail
700mm Uplink	$3.299V$	$3.28V < V < 3.32V$	Pass
700mm Downlink	$3.305V$	$3.28V < V < 3.32V$	Pass
230mm Downlink	$3.310V$	$3.28V < V < 3.32V$	Pass

3.12.2 Reference Clock Frequency

3.12.2.1 Test Instructions

Measure the frequency of each reference clock. Ensure the frequency is $20MHz \pm 5ppm$.

3.12.2.2 Test Data

Measure the frequency of each reference clock output			
RF Chain	Oscillator output	Passing Criteria	Pass / Fail
700mm Uplink	$20MHz$	$f = 20MHz \pm 5ppm$	Pass
700mm Downlink	$20MHz$	$f = 20MHz \pm 5ppm$	Pass
230mm Downlink	$20MHz$	$f = 20MHz \pm 5ppm$	Pass

3.12.2.3 Test Notes

We do not have a frequency counter, used oscilloscope.

3.12.3 Output Frequency

3.12.3.1 Test Instructions

Configure each generator to output its frequency as follows. Use a spectrum analyzer to measure the output. Ensure the frequency is within $10ppm$ and bandwidth is less than $200ppm$.

- 700mm Uplink: $880MHz$
- 700mm Downlink: $435MHz$
- 230mm Downlink: $1.25GHz$

Note: Measure the bandwidth at the $-3dB$ point

3.12.3.2 Test Data

Measure the frequency of each generator output with a spectrum analyzer			
RF Chain	Capture the generator output	Passing Criteria	Pass / Fail
700mm Uplink	$f = 880.000MHz$ $B = 20Hz$	$f = 880MHz \pm 10ppm$ $B < 176kHz$	Pass
700mm Downlink	$f = 440.0001MHz$ $B = 20Hz$	$f = 440MHz \pm 10ppm$ $B < 87kHz$	Pass
230mm Downlink	$f = 0Hz$	$f = 1.25GHz \pm 10ppm$ $B < 250kHz$	Fail

3.12.3.3 Test Notes

Inductance for the 230mm Downlink is too small and therefore cannot oscillate.

3.13 Differential Drivers

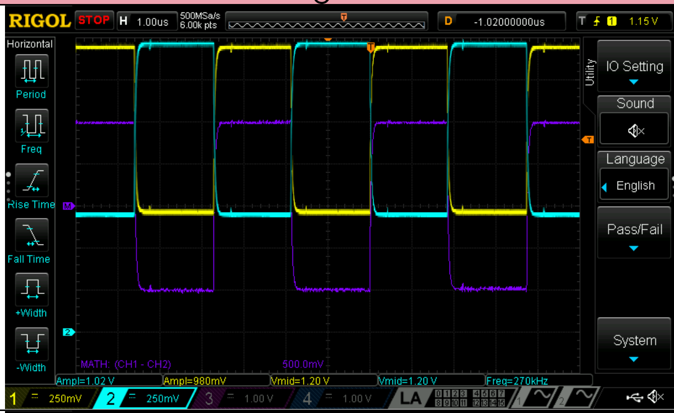
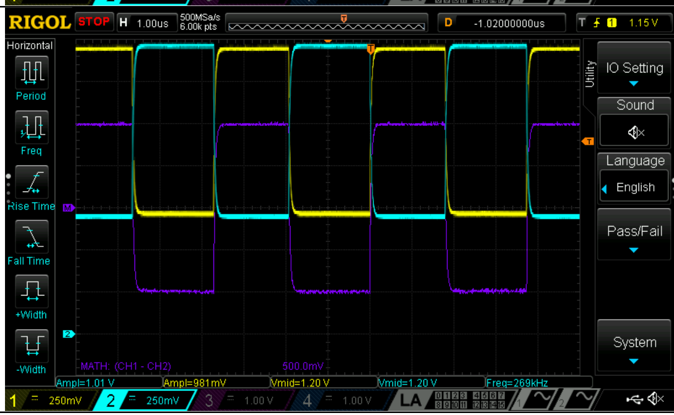
Results: Pass
Test Configuration: Doug

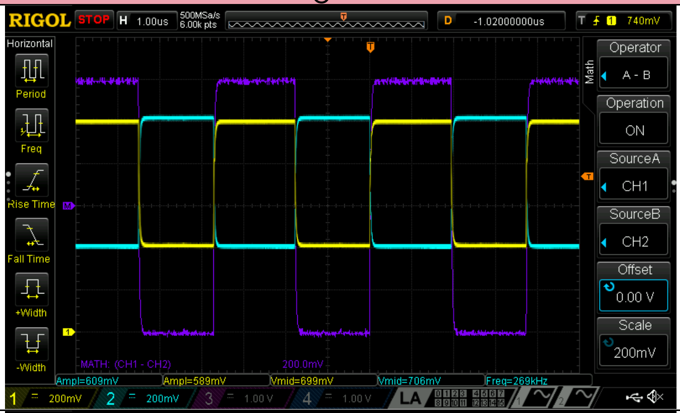
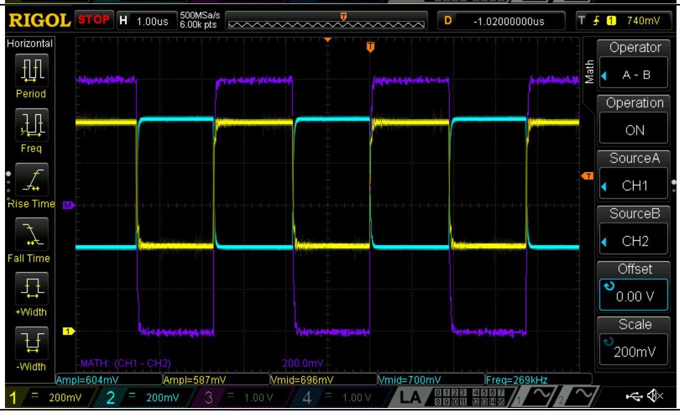
This test evaluates the circuit described in Differential Drivers.

3.13.1 Test Instructions

Have the µController generate a square wave on each modulator input with a frequency of $250kHz$. Validate the waveform and voltage levels at the gain resistors.

3.13.2 Test Data

Have the µController generate a square wave on each modulator input with a frequency of $250kHz$.			
Signal	Capture the single ended and differential signals	Passing Criteria	Pass / Fail
230 ID		$V = 1.2V \pm 0.5V$ Within 3% Signal Integrity	Pass
230 QD		$V = 1.2V \pm 0.5V$ Within 3% Signal Integrity	Pass

Have the µController generate a square wave on each modulator input with a frequency of $250kHz$.			
Signal	Capture the single ended and differential signals	Passing Criteria	Pass / Fail
700 ID		$V = 0.7V \pm 0.3V$ Within 3% Signal Integrity	Pass
700 QD		$V = 0.7V \pm 0.3V$ Within 3% Signal Integrity	Pass

3.14 Power Amplifier Bias

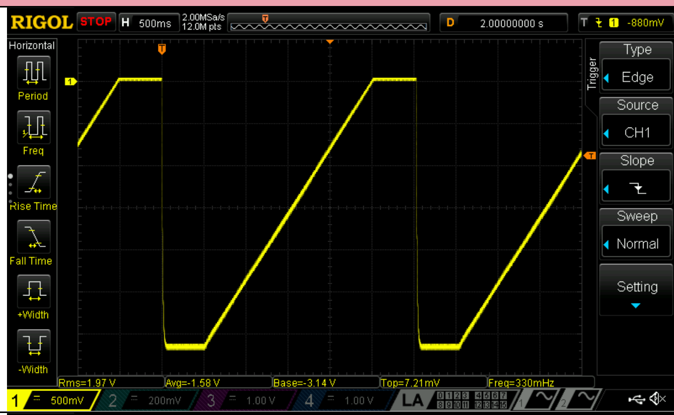
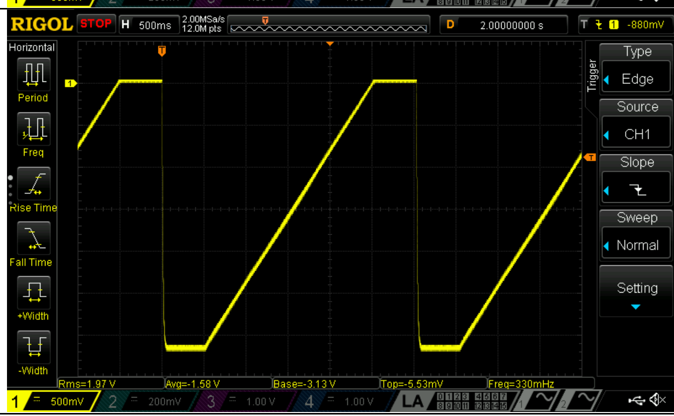
Results: Pass
Test Configuration: Doug

This test evaluates the circuit described in Power Amplifiers.

3.14.1 Test Instructions

Have the µController sweep each power amplifier bias from $0\% \; to \; 100\%$ duty cycle. Validate the output sweeps from $-3.3V \; to \; 0V$ with a linear relationship.

3.14.2 Test Data

Have the µController sweep each power amplifier bias from 0% *to* 100% duty cycle. Validate the output sweeps from $-3.3V$ *to* $0V$.			
RF Chain	Capture the sweep	Passing Criteria	Pass / Fail
230mm		$V(0 \rightarrow 1) = -3.3V \rightarrow 0V$	Pass
700mm		$V(0 \rightarrow 1) = -3.3V \rightarrow 0V$	Pass

3.15 RF Chain – 230mm Downlink

Results: Fail
Test Configuration: Doug

This test evaluates the circuit described in RF Modulators, Low Noise Amplifier, and Power Amplifiers.

3.15.1 Test Instructions

Have the µController generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $500kbps$. Validate the following parameters:

- Power output of $1W$ when power amplifier bias is set to maximum
- Spectral bandwidth of less than $250kHz$
- Distinct separation of symbols

3.15.2 Test Data

Have the μController generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $500kbps$ on the $230mm$ radio.			
Parameter	Value (Scope or Spectrum Analyzer Capture)	Passing Criteria	Pass / Fail
Output Power		$P = 1W \pm 0.2W$	
Spectral Bandwidth		$B < 250kHz$	

Have the μController generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $500kbps$ on the $230mm$ radio. Use an SDR to demodulate into symbols		
Capture the I/Q signals (waveforms and constellation)	Passing Criteria	Pass / Fail
	Distinct Symbols	

3.15.3 Test Notes

RF clock generator does not oscillate, see 3.12.2.

3.16 RF Chain – 700mm Downlink

Results: Fail
Test Configuration: Doug

This test evaluates the circuit described in RF Modulators, Low Noise Amplifier, and Power Amplifiers.

3.16.1 Isolation Switch

3.16.1.1 Test Instructions

Have the μController gradually increase the power output of the $700mm$ downlink radio while the RF switch is set to downlink. Measure the power on the $700mm$ uplink radio input. Ensure this power does not exceed $0dBm$.

3.16.1.2 Test Data

Have the μController gradually increase the power output of the $700mm$ downlink radio while the RF switch is set to downlink. Measure the power on the $700mm$ uplink radio input. Ensure this power does not exceed $0dBm$.		
Max power	Passing Criteria	Pass / Fail
$-10dBm$	$P < 0dBm$	Pass

3.16.2 Digital Modulation

3.16.2.1 Test Instructions

Have the μController generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $50kbps$ on the $700mm$ radio. Validate the following parameters:

- Power output of $1W$ when power amplifier bias is set to maximum
- Spectral bandwidth of less than $25kHz$
- Distinct separation of symbols

3.16.2.2 Test Data

Have the µController generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $50kbps$ on the $700mm$ radio.			
Parameter	Value (Scope or Spectrum Analyzer Capture)	Passing Criteria	Pass / Fail
Output Power	$26dBm = 0.4W$	$P = 1W \pm 0.2W$	Fail
Spectral Bandwidth	Too large	$B < 25kHz$	Fail

Have the µController generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $50kbps$ on the $700mm$ radio. Use an SDR to demodulate into symbols		
Capture the I/Q signals (waveforms and constellation)	Passing Criteria	Pass / Fail
	Distinct Symbols	

3.16.2.3 Test Notes

Need filtering on baseband and carrier signals to reduced spur power and bandwidth.

3.16.3 Analog Modulation

3.16.3.1 Test Instructions

Have the µController generate an amplitude modulated audio signal on the $700mm$ radio. Validate the following parameters:

- Power output of $1W$ when power amplifier bias is set to maximum
- Spectral bandwidth of less than $20kHz$
- Recognizable demodulated audio

3.16.3.2 Test Data

Have the µController generate an amplitude modulated audio signal on the $700mm$ radio.			
Parameter	Value (Scope or Spectrum Analyzer Capture)	Passing Criteria	Pass / Fail
Output Power		$P = 1W \pm 0.2W$	
Spectral Bandwidth		$B < 20kHz$	

Have the µController generate an amplitude modulated audio signal on the $700mm$ radio. Use an SDR to demodulate into audio.		
Capture the I/Q signals (waveforms)	Passing Criteria	Pass / Fail
	Recognizable audio	

3.16.3.3 Test Notes
440Hz tone sounded correct. Need filtering on baseband and carrier signals

3.17 RF Chain – 700mm Uplink
Results: Fail
Test Configuration: Doug

This test evaluates the circuit described in RF Demodulator, and Low Noise Amplifier.

3.17.1 Test Instructions
Have a radio generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $50kbps$ to transmit to the $700mm$ radio with a received power of $-150dBm$. Validate the following parameters:

- Signal to noise ratio (SNR) $> 30dBm$
- Output voltage of $1.65V \pm 1V$
- Distinct separation of symbols

3.17.2 Test Data

Have a radio generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $50kbps$ to transmit to the $700mm$ radio with a received power of $-150dBm$.			
Parameter or Signal	Value (Scope or Spectrum Analyzer Capture)	Passing Criteria	Pass / Fail
SNR		$SNR > 30dBm$	
DEMOD_ID	$1.71V \pm 0.6V$	$V = 1.65V \pm 1V$	Fail
DEMOD_QD	$1.71V \pm 0.6V$	$V = 1.65V \pm 1V$	Fail

Have a radio generate a QPSK modulated signal with pattern $00\ 01\ 11\ 10$ with a data rate of $50kbps$ to transmit to the $700mm$ radio with a received power of $-150dBm$.		
Capture the I/Q signals (waveforms and constellation)	Passing Criteria	Pass / Fail
	Distinct Symbols	

3.17.3 Test Notes
Implement AGC and double the gain of differential to single ended amplifier. Connected a source of $-60dBm$ with LNA off, adjusted the input to be $-54dBm$.