This document explains the function of the EPS, its schematic level design, its board level design, and its functional testing

EPS

Electrical Power Subsystem Design

Revision: 3.0.2

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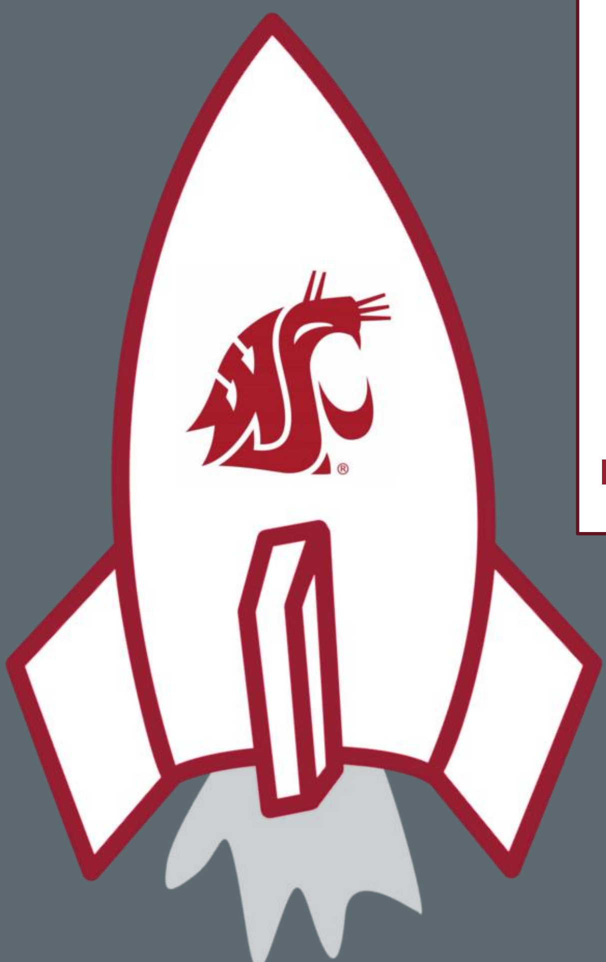

Table of Contents

1 Introduction

This document explains how the EPS will fulfil the following Functions and conform to the following Requirements. This document refers to the EPS version 3.0 and Solar Panel version 2.0.

1.1 Function

The Electrical Power Subsystem (EPS) is responsible for the following:

- Accumulating energy
- Regulating voltage
- Distributing power

1.2 Requirements

The system requirements and EPS design requirements can be found on GitHub.

2 Detailed Description

This section references the EPS schematic. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Power Input

Energy is captured from the Sun using an array of photovoltaic cells[1]. These cells are mounted onto solar panels that adjust the voltage and current to acceptable levels for direct charging of lithium-ion batteries[2]. These criteria are up to $4.1V$ and up to $0.5C$[3] per battery. Furthermore, power can be inputted from the umbilical[4] using the same criteria as the solar panels. The umbilical will only be used whilst on the ground. The PMIC will automatically monitor the charging and disable current paths to follow the prescribed charging, see Energy Storage for more details. Most lithium-ion charging curves indicate voltage up to $4.2V$ and current up to $1C$; however, the EPS will limit to $4.1V$ and $0.5C$ to preserve battery health[5]. Replacing the batteries on the EPS whilst in orbit is very difficult.

The solar panel and umbilical inputs are routed through a balance switching matrix before entering the batteries. This allows the PMIC to switch every cell going to either or both batteries[6].

2.1.2 Energy Storage

The EPS stores energy from the solar panels in batteries to fulfil high instantaneous power demands and any power demands during periods of eclipse[7]. Each battery has a protection IC that protects against the following faults:

- Overcharge
- Over-discharge
- Charge overcurrent
- Discharge overcurrent
- Load short-circuit detection

[1] Requirement EPS-010
[2] For details on charging lithium-ion batteries, http://batteryuniversity.com/learn/article/charging_lithium_ion_batteries
[3] 1C is equal to the charge of the battery divide by 1 hour (Take the Ah of the battery and drop the "h")
[4] Requirement EPS-021
[5] Requirement REQ-009
[6] Requirement EPS-008
[7] Requirements EPS-005, EPS-006, EPS-009

The PMIC will monitor and regulate the temperature of the batteries. The batteries (and power inputs) disconnect from the rest of the EPS via separation switches and the RBF switch[8].

2.1.3 Power Output

The EPS has two separate rails for distribution: unregulated from the batteries and $3.3V$[9]. There are two regulators[10], one per battery. Most loads are connected via the backplane and are individually switched between either source (power chain A or B) or turned off, and current monitored[11]. The PMIC controls these turning on and off, the switch for chain A or B is automatically performed.

There is a single load that cannot be disconnected from the regulators: the PMIC[12]. This ensures there is at least one processor that can turn on the rest of the satellite. The outputs' default states are off such that the PMIC must turn the loads on, this prevents glitching as the PMIC boots up. The power rail going to the In-Flight JTAG Reprogrammer (IFJR) is logical ORed with *JTAG_EN_PMIC* such that if the IFJR is programming the PMIC, its GPIO goes high impedance but the IFJR remains powered on to avoid corruption.

2.1.4 PMIC

The Power Management IC (PMIC) is the microprocessor monitoring and operating the EPS[13]. Only one PMIC exist as adding redundant processors adds complexity that could reduce reliability. It communicates over I²C to Command and Data Handling subsystem (C&DH)[14] via the backplane and to its monitoring sensors directly. It collects sensor information and transfers this to the C&DH to be included in a telemetry packet to Ground[15]. The C&DH may also send commands. For example, enter safe mode by switching off specific subsystems[16].

2.1.5 Monitoring

The PMIC, through ADCs, monitors current, and voltage at various locations and temperature of various components, indicated on the block diagram[17].

2.2 Schematic

2.2.1 Isolated Grounds

On page 2 of the schematic (D1), are the four isolated grounds found on the EPS. Power ground *(PGND)* is directly connected to the backplane and most of the power chain. The other grounds are shorted to *PGND* using a 0Ω resistor

[8] Requirements EPS-020
[9] Requirement EPS-001
[10] Requirement EPS-008
[11] Requirements EPS-008, EPS-011, EPS-012
[12] Requirements EPS-013
[13] Requirement EPS-022
[14] Requirement EPS-018
[15] Requirement EPS-019
[16] Requirement EPS-014
[17] Requirements EPS-011, EPS-015, EPS-016, EPS-017

rated up to $2A$, the expected current is less than $50mA$ each. Digital ground *(DGND)* connects to the digital circuity including the PMIC and Monitoring circuits. Analog ground *(AGND)* connects to analog monitoring circuits including the ADCs, their voltage reference, and the thermistors. Chassis ground *(CHASSIS)* is connected to the Mechanical Features including bolt holes and the card rails.

2.2.2 Power Rails

Page 2 of the schematic illustrates all the power rails on the EPS. Notice how most components of the power chain can be routed to the other chain to increase redundancy. The expected current consumptions are derived from the energy budget. The limit of less than $1A$ per rail is imposed by the backplane with current limiters[18].

2.2.2.1 Always-On Rail

There is one rail that is always-on and cannot be switched off, except with the Separation Switching. This provide power for the PMIC as the PMIC cannot be allowed to turn off or other subsystems may not be able to be turned on. It is *3.3V* (page 5, B5). They use "ideal diodes"[19] to OR the power together from both power chains, whichever rail has a higher voltage provides the current.

2.2.3 Input Switching

A matrix of ideal diodes[20] (page 3) switch the solar panel inputs and umbilical input to either battery. The lower voltage battery receives the current first until both batteries have the same voltage. Their enable pin are connected to the PMIC for enabling or disabling charging. To reduce the number of enable pins, cells on the opposite side of the satellite share an enable. The increased control over individual cells is not important as the opposite side cell will be in shadow and okay if disabled.

As the GPIO of the PMIC defaults to high impedance input during boot up (every reset will enter this state). The IC includes an active pullup on its enable pin so an external one is not needed for when the PMIC is off.

The power inputs are placed in parallel with the batteries such that the loads will draw from the power inputs before drawing from the batteries.

2.2.4 Battery & Battery Protection

The batteries[21] (page 4, B2 & B5) are 18650 lithium-ion. The chemistry was chosen for its high volumetric and mass energy densities. A specific cell has not been chosen; a long-term study is required. The EPS will be compatible with most cells.

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[18] CIS PN: 60-0014
[19] CIS PN: 60-0015
[20] CIS PN: 60-0015
[21] CIS PN: 01-0001

The batteries are protected by dedicated lithium-ion single-cell protection ICs[22] (page 4, B2 & B5). They measure the current passing through the battery by measuring the voltage between pins 4 & 6. With the Rds(on) of the MOSFET[23] and the shunt resistor, the IC prevents against $\frac{90\ to\ 110mV}{(6.4+6.4+10)m\Omega} = \ 4\ to\ 4.8A$ of overcurrent. The IC also prevents against $4.275V$ of over-voltage and $2.800V$ of under-voltage.

The batteries are thermally connected to a heater and Temperature Monitoring thermistor. The heater is a TO-220 10Ω resistor which generates up to $\frac{(3.7V)^2}{10\Omega} \approx 1.4W$ of heat. A lower resistance resistor may be exchanged for more heating capabilities, a thermal test will indicate this need. The heater can be driven at lower duty cycle, through PWM, to reduce the average output power.

2.2.5 Separation Switching

The separation switches (connected via the backplane) or the RBF pin switch (page 4, D3) disconnect the batteries and power input from the rest of the power chain. Either of the switches apply a pull down to the gate of a MOSFET that inverts the signal to another MOSFET that interrupts the power chain. When the umbilical is connected, and voltage is applied, it drives the MOSFETs the opposite way to connect the power chain. In the default state (no switches depressed or umbilical connected) a weak pull up to the batteries (through ORing diodes) keeps the MOSFETS driven to connect the power chain.

Connected to the separation switches and RBF pin switch is a capacitor and limiting resistor such that the time constant is $(220\mu F)(158k\Omega) \approx 35s$ buffered with a unity gain buffer[24]. The PMIC measures the voltage across the capacitor. When the PMIC boots up, it will check this voltage is decide if it is powering up after a reset (the capacitor will still be charged) or after a deployment (the capacitor will be discharged).

2.2.6 3.3V Regulation

The 3.3V regulators (page 5) are switching mode, buck topology. The controller[25] automatically senses the output voltage and adjusts the switching parameters to keep the output at $3.3V$. The controller was chosen for its small package and ability to output 100% duty cycle such that when the input drops below $3.3V$, the output will follow the voltage of the input.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

[22] CIS PN: 60-0006
[23] CIS PN: 56-0005
[24] CIS PN: 08-0002
[25] CIS PN: 06-0004

On the drain of the switching MOSFETs (page 5, A3 & C3) are snubber circuits that absorb and suppress transients thus reducing the output noise.

The switching MOSFETs and inductors (page 5, A3 & C3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

2.2.7 Output Switching

The output switching (pages 6, 7) uses ideal diodes[26] that automatically switch between power chain A or B, whichever is higher voltage, and have an integrated current limit. The PMIC controls each one individual between off and on with automatic switching. All rail's default state is off for when the PMIC is off and not driving the enable signals. Th IFJR's power rail is also (logical OR) enabled when the *JTAG_EN_PMIC* is on as described in Power Input.

Most outputs go into the backplane for distribution to their connected subsystem. The *PR_DEPLOY* output (for releasing deployable mechanisms) and *PV_3.3V* (for the solar panel monitoring circuits) connect to their load via wire harness (page 3).

2.2.8 Current Monitoring

At various locations, the power chain has shunt resistors with current shunt amplifiers[27] connected to ADCs to monitor the current. Those locations are:

- Batteries: charging/discharging (page 4, B2 & B5)
- Power chain input (page 4, A2 & A5)
- 3.3V regulator input (page 5, A3 & C3)
- 3.3V regulator output (page 5, A5 & C5)

Output switching ideal diodes[28] have a current limit set by resistor whose current is proportional to the diode's current. This voltage is measured by an ADC to sense the current.

The solar panels monitor their own current and the PMIC communicates to them via the wire harness (page 3).

2.2.9 Voltage Monitoring

At various locations, the power chain is probed for the voltage using one of the ADCs. Those locations are:

- Batteries (page 4, A3 & A4)
- 3.3V regulator output (page 5, A6 & C6)
- Umbilical input (page 3, C2)

The solar panels monitor their own voltages and the PMIC communicates to them via the wire harness (page 3).

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[26] CIS PN: 60-0014
[27] CIS PN: 08-0003 and 08-0004
[28] CIS PN: 60-0014

2.2.10 Temperature Monitoring

At various locations, the temperature is monitored using thermistors and one of the ADCs. Those locations are:

- Batteries (page 4, B3 & B4)
- 3.3V regulator switching components (page 5, A4 & C4)
- Input switching (page 3, D3)
- Output switching (page 6, D4; page 7, D4)
- PMIC (page 9, C4)
- Various locations of the PCB (page 11, A5:A6)
- Each ADC has an integrated temperature sensor

2.2.11 PMIC

The PMIC (page 9) is a microcontroller from the STM32 low power family[29]. It was chosen for its ease of programming, and low power consumption. Since the PMIC is essentially just controlling GPIO and talking over two I²C Buses and a SPI Bus, the features of higher end processors are not needed.

2.2.11.1 Programming Connections

During testing, the PMIC is programmed via Serial Wire Debug[30] (SWD, page 9, D5). The process of programming is made simple with just a single 6 pin header and a robust software utility. In orbit, the PMIC can be programmed via JTAG[31]. The In-Flight JTAG Reprogrammer (IFJR) connects via the backplane, through a tri-state buffer/logic level converter[32] (page 8, A1:B2). The IFJR can enable or disable the tri-state buffer which essentially disconnects the JTAG interface from the PMIC (it outputs high impedance), allowing the SWD to program. The logic level conversion feature is not used.

2.2.12 I²C Bus

The PMIC has two I²C buses (page 9). One is for the EPS monitoring and control devices. The other is to communicate with the C&DH. On the EPS bus, the PMIC is the master served by the attached devices. Busses that communicate with devices on different power rails go through a tri-state buffer[33], such that when the device is powered off, its ESD diodes do not hold the bus low preventing communication with the other devices on the bus.

2.2.12.1 ADCs

There are nine ADCs[34] connected to the PMIC, each with eight single-ended inputs. Four are on the EPS (page 11). There is one on each solar panel. The ADC was chosen for its low power, small package, SAR architecture and up to nine addresses. The list of address follow:

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[29] CIS PN: 61-0002
[30] For more details on SWD, https://developer.arm.com/products/system-ip/coresight-debug-and-trace/coresight-architecture/serial-wire-debug
[31] For more details on JTAG, https://en.wikipedia.org/wiki/JTAG
[32] CIS PN: 09-0001
[33] CIS PN: 09-0001
[34] CIS PN: 27-0003

- [`0x58`] EPS-0 (page 11, A2)
- [`0x5C`] EPS-1 (page 11, B2)
- [`0x5E`] EPS-2 (page 11, C2)
- [`0x56`] EPS-3 (page 11, B5)
- [`0x40`] EPS-4 (page 11, C5)
- [`0x54`] PV0 (+Z) (page 3, A1)
- [`0x50`] PV1 (-Y) (page 3, A3)
- [`0x44`] PV2 (-X) (page 3, B1)
- [`0x46`] PV3 (+Y) (page 3, B3)

2.2.12.2 Backplane to C&DH

The PMIC is a slave to the C&DH. See the interface document for details.

2.2.13 SPI Bus

The PMIC has one SPI bus (page 9) to communicate with three ADCs[35]. These ADCs have a high bit count for resolution when measuring critical nodes including power chain currents and power chain voltages. Each ADC has its own select pin.

2.2.14 Analog Voltage Reference and Supply

Each ADC has its own analog reference of $2.5V$ with high temperature stability, not requiring a high precision external reference. For the thermistors, they are sourced from this analog reference with a unity gain buffer[36] to allow higher current draw (page 11, B4 & D4).

The EPS has an analog voltage supply (page 11, D2) which is fed by the always-on *3.3V* rail filtered with a ferrite bead and capacitors. Precision is not required as all ADCs use the precision voltage reference for calibration. This is the source for the analog unity gain buffers and ADCs.

2.2.15 Mechanical Features

The RBF pin holder (page 4, D1) and 3.3V Regulation heatsink (page 5, B1 & D1) mount directly to the EPS board using bolts. These holes are conductive and connected directly to *CHASSIS*, see Isolated Grounds. The EPS also slots into the structure using rails[37] which are also conductive and connected directly to chassis ground. Each of the holes have a capacitor and resistor connecting to power ground which will absorb transients.

2.3 Board

The board shall conform to the dimensions specified by the CougSat Module Standard.

[35] CIS PN: `27-0004`
[36] CIS PN: `08-0002`
[37] See backplane documentation for details

2.3.1 Layer Stack-Up

The board shall be four layered with ENIG finish, see Figure 1. Only through vias shall be used. The external copper weight shall be $35\mu m$ and the internal copper weight shall be $18\mu m$.

Layer	Thickness	Primary Function
1 (top)	$35\mu m\ (1oz)$	SMD components, signal traces
Prepreg	$200\mu m$	
2	$18\mu m\ (0.5oz)$	Ground planes
Core	$500\mu m$	
3	$18\mu m\ (0.5oz)$	Power planes
Prepreg	$200\mu m$	
4 (bottom)	$35\mu m\ (1oz)$	Signal traces

Figure 1: Stack-Up

2.3.2 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless otherwise specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width: $0.16mm$
Vias: $\emptyset 0.3mm$, unlimited count
Separation: $0.16mm$
Length: unlimited

Devices with specific placement and routing considerations are called out on the schematic, see "CAD Note:"

2.3.2.1 Solar Panel Inputs – PV_IN[0:3][A:B], PGND

PGND applies to between the solar panel headers and the backplane

Trace width: $0.3mm$ ($0.6mm$ on internal layers)

2.3.2.2 Umbilical Input – UMB_IN, PGND

PGND applies to between the umbilical header and the backplane

Trace width: $0.8mm$ ($1.6mm$ on internal layers)

2.3.2.3 Battery Input – VIN-[A:B], PGND

PGND applies to between the solar panel headers and the backplane

Trace width: $2.0mm$ ($4.0mm$ on internal layers)

2.3.2.4 Battery Connections – BP_VSS-[A:B], BP_VSS-I[A:B], VBATT-[A:B], PGND

PGND applies to between the low side battery protection MOSFETs and the backplane.

Trace width: $5.5mm$ ($11mm$ on internal layers)
Vias: $\emptyset 0.3mm$ five per layer change

2.3.2.5 SMPS Switching Node – 3.3V_ISENS-[A:B], 3.3V_REG_BUCK_NODE-[A:B]

Trace width: $3.5mm$
Vias: No vias
Minimize RF emission

2.3.2.6 SMPS Output – 3.3V_I-[A:B], 3.3V-[A:B]

The traces can taper down once loads branch off and less than three loads remain.

Trace width: $3.5mm$ ($7mm$ on internal layers)
Vias: $\emptyset 0.3mm$ three per layer change

2.3.2.7 SMPS Ground – PGND

PGND applies to between the filtering capacitors and the backplane.

Trace width: $0.8mm$ ($1.6mm$ on internal layers)

2.3.2.8 Rail Output Channels – PR_3.3V-[0:12], PR_BATT-[0:6], PR_BH-[0:1]

Trace width: $0.8mm$ ($1.6mm$ on internal layers)

2.3.2.9 Deployables Output – PR_DEPLOY

Trace width: $0.8mm$ ($1.6mm$ on internal layers)

2.3.2.10 JTAG – JTAG-[TCK, TDI, TDO, TMS], BUS_JTAG-[TCK, TDI, TDO, TMS]

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

2.3.2.11 I^{2}C – I2C_[SDA, SCL], BUS_I2C_[SDA, SCL, IRQ]

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

3 Testing – V3.0

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test[38].

- Waveforms shall be captured whenever appropriate
- Have the event take fill the screen (for fast events, zoom in; for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-PowerBoard/Testing/EPS.2.1

Common test instructions can be found on the wiki.

Note: In the following sections, applying a $4.1V, 300mA$ source means to connect a power supply limited to $4.1V$ and $300mA$. The actual voltage and current may be less than this.

3.1 Before First Power-On Check

Configuration:

This test is required to be executed before batteries are attached and before any external power is applied to the EPS.

3.1.1 Test Instructions

Measure the resistance of various points in reference to *PGND* located at the backplane. Measure the resistance across each current shunt resistor before installing. This is informational only; the resistance of the current shunt resistor is used to calibrate the Current Monitoring.

Measure low value resistors via a constant current source and voltmeter in a four-wire setup to minimize noise. Measure current limit set resistor via a constant current source through the limiter and a voltmeter on the resistor, this compensates the limiter's gain.

3.1.2 Test Data

Node	Resistance		Node	Resistance
VIN-A			*VIN-B*	
VBATT-A			*VBATT-B*	

[38] For test 3.1, place files in the subfolder *"3.1"* and so on

Node	Resistance		Node	Resistance
VBATT			*3.3V*	
3.3V-A			*3.3V-B*	
AVREF			*AVDD*	
I2C_SCL			*I2C_SDA*	
BUS_I2C_SCL			*BUS_I2C_SDA*	

Net	Resistor	Value		Net	Resistor	Value
Battery A	R1			*Battery B*	R8	
VIN-A	R2			*VIN-B*	R7	
3.3V Input A	R61			*3.3V Input B*	R11	
3.3V Output A	R82			*3.3V Output B*	R22	
PR_3.3V-0	R81			*PR_3.3V-1*	R79	
PR_3.3V-2	R76			*PR_3.3V-3*	R73	
PR_3.3V-4	R71			*PR_3.3V-5*	R70	
PR_3.3V-6	R67			*PR_3.3V-7*	R65	
PR_3.3V-8	R63			*PR_3.3V-9*	R60	
PR_3.3V-10	R59			*PR_3.3V-11*	R58	
PR_3.3V-12	R57			*PR_BATT-0*	R56	
PR_BATT-1	R55			*PR_BATT-2*	R54	
PR_BATT-3	R51			*PR_BATT-4*	R50	
PR_BATT-5	R45			*PR_BATT-6*	R39	
PR_BH-0	R38			*PR_BH-1*	R26	
PR_DEPLOY-0	R74			*PR_DEPLOY-1*	R10	
3.3V	R24					

3.1.3 Test Notes

Delete me if no notes are required.

3.2 Separation Switching

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Separation Switching.

3.2.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Insert the RBF pin, wait at least $2min$, remove the RBF pin. Measure *PWR_CTRL_SW, VBATT-A, VBATT-B,* and *EJECT_TIMER_BUF.*

3.2.2 Test Data

Insert the RBF pin, wait at least $2min$, remove the RBF pin.			
Operation	Capture *PWR_CTRL_SW, VBATT-A, VBATT-B,* and *EJECT_TIMER*	Passing Criteria	Pass / Fail
Insertion		*VBATT-A* and *VBATT-B* fall < $10mV$ within $10ms$, *EJECT_TIMER* falls < $500mV$ within $2min$	
Removal		*VBATT-A* and *VBATT-B* rise > $3V$ within $10ms$, *EJECT_TIMER* rises > $2V$ between $30s$ and $2min$	

3.2.3 Test Notes
Delete me if no notes are required.

3.3 Power Rails
Results: Pass / Fail

This test evaluates the circuit described in Power Rails.

3.3.1 Test Instructions
Discharge or charge the batteries to $3.7V$ before executing this test. With the PMIC not running code, upload a blank image or assert its reset pin, and the RBF pin inserted, apply power to each input one at a time as follows:

- $4.1V, 300mA$ to the solar panel inputs
- $4.1V, 1.0A$ to the umbilical input

Ensure that both batteries are receiving the power.

3.3.2 Test Data

Apply $4.1V, 300mA$ to PV_IN-0					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-1					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-2					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-2					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-3					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-4					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-5					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-6					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-7					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 1.0A$ to UMB_IN					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $1.5W$	
B				Power > $1.5W$	

3.3.3 Test Notes

Delete me if no notes are required.

3.4 Input Switching

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Input Switching.

3.4.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Drive each input switch to the following states while applying a $4.1V, 300mA$ source:

- *Both Off*
- *A On*

- *B On*
- *Both Off*

Ensure each channel is properly routing the power.

3.4.2 Test Data

Configure each input channel to *Both Off*. Apply a $4.1V, 300mA$ source to the input under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_IN-0A			$A < 10mW$ & $B < 10mW$	
PV_IN-0B			$A < 10mW$ & $B < 10mW$	
PV_IN-1A			$A < 10mW$ & $B < 10mW$	
PV_IN-1B			$A < 10mW$ & $B < 10mW$	
PV_IN-2A			$A < 10mW$ & $B < 10mW$	
PV_IN-2B			$A < 10mW$ & $B < 10mW$	
PV_IN-3A			$A < 10mW$ & $B < 10mW$	
PV_IN-3B			$A < 10mW$ & $B < 10mW$	
UMB_IN			$A < 10mW$ & $B < 10mW$	

Configure each input channel to *A On*. Apply a $4.1V, 300mA$ source to the input under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_IN-0A			$A > 800mW$ & $B < 10mW$	
PV_IN-0B			$A > 800mW$ & $B < 10mW$	
PV_IN-1A			$A > 800mW$ & $B < 10mW$	
PV_IN-1B			$A > 800mW$ & $B < 10mW$	
PV_IN-2A			$A > 800mW$ & $B < 10mW$	
PV_IN-2B			$A > 800mW$ & $B < 10mW$	
PV_IN-3A			$A > 800mW$ & $B < 10mW$	
PV_IN-3B			$A > 800mW$ & $B < 10mW$	
UMB_IN			$A > 800mW$ & $B < 10mW$	

Configure each input channel to *B On*. Apply a $4.1V, 300mA$ source to the input under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_IN-0A			$A < 10mW$ & $B > 800mW$	
PV_IN-0B			$A < 10mW$ & $B > 800mW$	
PV_IN-1A			$A < 10mW$ & $B > 800mW$	
PV_IN-1B			$A < 10mW$ & $B > 800mW$	
PV_IN-2A			$A < 10mW$ & $B > 800mW$	
PV_IN-2B			$A < 10mW$ & $B > 800mW$	
PV_IN-3A			$A < 10mW$ & $B > 800mW$	
PV_IN-3B			$A < 10mW$ & $B > 800mW$	
UMB_IN			$A < 10mW$ & $B > 800mW$	

Configure each input channel to *Both On*. Apply a $4.1V, 300mA$ source to the input under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_IN-0A			$A > 400mW$ & $B > 400mW$	
PV_IN-0B			$A > 400mW$ & $B > 400mW$	
PV_IN-1A			$A > 400mW$ & $B > 400mW$	
PV_IN-1B			$A > 400mW$ & $B > 400mW$	
PV_IN-2A			$A > 400mW$ & $B > 400mW$	
PV_IN-2B			$A > 400mW$ & $B > 400mW$	
PV_IN-3A			$A > 400mW$ & $B > 400mW$	
PV_IN-3B			$A > 400mW$ & $B > 400mW$	
UMB_IN			$A > 400mW$ & $B > 400mW$	

3.4.3 Test Notes
Delete me if no notes are required.

3.5 Output Switching
Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Output Switching.

3.5.1 Test Instructions
Discharge or charge the batteries to $4.1V$ before executing this test. Drive each output switch to the following states while applying a 10Ω resistive load:

- *Off*
- *On*

Note: *PR_BH-[0,1]* already have a 10Ω resistive load and do not need an external load applied.

3.5.2 Test Data

Configure each output channel to *Both Off*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_3.3V-0			$A < 10mW$ & $B < 10mW$	
PV_3.3V-1			$A < 10mW$ & $B < 10mW$	
PV_3.3V-2			$A < 10mW$ & $B < 10mW$	
PV_3.3V-3			$A < 10mW$ & $B < 10mW$	
PR_3.3V-0			$A < 10mW$ & $B < 10mW$	
PR_3.3V-1			$A < 10mW$ & $B < 10mW$	
PR_3.3V-2			$A < 10mW$ & $B < 10mW$	
PR_3.3V-3			$A < 10mW$ & $B < 10mW$	
PR_3.3V-4			$A < 10mW$ & $B < 10mW$	
PR_3.3V-5			$A < 10mW$ & $B < 10mW$	
PR_3.3V-6			$A < 10mW$ & $B < 10mW$	

Configure each output channel to *Both Off*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PR_3.3V-7			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-8			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-9			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-10			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-11			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-12			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-0			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-1			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-2			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-3			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-4			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-5			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-6			$A < 10mW \,\&\, B < 10mW$	
PR_DEPOLY-0			$A < 10mW \,\&\, B < 10mW$	
PR_DEPOLY-1			$A < 10mW \,\&\, B < 10mW$	
PR_BH-0			$A < 10mW \,\&\, B < 10mW$	
PR_BH-1			$A < 10mW \,\&\, B < 10mW$	

Configure each output channel to *On*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_3.3V-0			$A + B > 750mW$	
PV_3.3V-1			$A + B > 750mW$	
PV_3.3V-2			$A + B > 750mW$	
PV_3.3V-3			$A + B > 750mW$	
PR_3.3V-0			$A + B > 750mW$	
PR_3.3V-1			$A + B > 750mW$	
PR_3.3V-2			$A + B > 750mW$	
PR_3.3V-3			$A + B > 750mW$	
PR_3.3V-4			$A + B > 750mW$	
PR_3.3V-5			$A + B > 750mW$	
PR_3.3V-6			$A + B > 750mW$	
PR_3.3V-7			$A + B > 750mW$	
PR_3.3V-8			$A + B > 750mW$	
PR_3.3V-9			$A + B > 750mW$	
PR_3.3V-10			$A + B > 750mW$	
PR_3.3V-11			$A + B > 750mW$	
PR_3.3V-12			$A + B > 750mW$	
PR_BATT-0			$A + B > 750mW$	
PR_BATT-1			$A + B > 750mW$	
PR_BATT-2			$A + B > 750mW$	
PR_BATT-3			$A + B > 750mW$	
PR_BATT-4			$A + B > 750mW$	

Configure each output channel to *On*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PR_BATT-5			$A + B > 750mW$	
PR_BATT-6			$A + B > 750mW$	
PR_DEPOLY-0			$A + B > 750mW$	
PR_DEPOLY-1			$A + B > 750mW$	
PR_BH-0			$A + B > 750mW$	
PR_BH-1			$A + B > 750mW$	

3.5.3 Test Notes

Delete me if no notes are required.

3.6 Battery Charging

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Battery & Battery Protection.

3.6.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the PMIC not running code, upload a blank image or assert its reset pin, and the RBF pin inserted, apply a $4.1V, 1.0A$ source to the umbilical input. Measure the change in voltage after $30\ minutes$ and validate the battery is charging.

Note: Measure the voltage without the external source applied

3.6.2 Test Data

Apply a $4.1V, 1.0A$ source to the umbilical input Measure the change in voltage after $30\ minutes$					
Battery	Initial Voltage	Final Voltage	ΔV	Passing Criteria	Pass / Fail
A				$\Delta V > 20mV$	
B				$\Delta V > 20mV$	

3.6.3 Test Notes

Delete me if no notes are required.

3.7 Battery Protection

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Battery & Battery Protection.

3.7.1 Discharge Overcurrent

3.7.1.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply an increasing load to *VBATT* until *DOUT* transitions low. Decrease the load until the *DOUT* transitions high. Measure the battery current, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: Connect all the power outputs together to share the overcurrent.

3.7.1.2 Test Data

Apply an increasing load to *PR_BATT* outputs until *DOUT* transitions low				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A			$3.5A < I < 5.4A$	
B			$3.5A < I < 5.4A$	

Decrease a high load on *PR_BATT* outputs until *DOUT* transitions high				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A			$I < 3.5A$	
B			$I < 4A$	

3.7.1.3 Test Notes

Delete me if no notes are required.

3.7.2 Load Short Circuit

3.7.2.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply a short between *VBATT* and *PGND*. Remove this short. Measure the battery current, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

3.7.2.2 Test Data

Apply a short between *VBATT* and *PGND*				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Delay	Passing Criteria	Pass / Fail
A			$125\mu s < t < 375\mu s$	
B			$125\mu s < t < 375\mu s$	

Remove a short between *VBATT* and *PGND*				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Delay	Passing Criteria	Pass / Fail
A			$t < 1s$	
B			$t < 1s$	

3.7.2.3 Test Notes

Delete me if no notes are required.

3.7.3 Charge Overcurrent

3.7.3.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply a $4.1V$ source to the power inputs with increasing current until *COUT* transitions low. Decrease the current until *COUT* transitions high. Measure the battery current, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: Connect all the power inputs together to share the overcurrent.

3.7.3.2 Test Data

Apply a $4.1V$ source to the power inputs with an increasing current until *COUT* transitions low				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A			$3A < I < 5A$	
B			$4A < I < 5A$	

Decrease the current from the previous source until *COUT* transitions low				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A			$I < 4A$	
B			$I < 4A$	

3.7.3.3 Test Notes

Delete me if no notes are required.

3.7.4 Charge Overvoltage

3.7.4.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. For each battery, apply a $4.1V, 100mA$ source to the umbilical with increasing voltage until *COUT* transitions low. Remove the source and apply a 20Ω resistive load until *COUT* transitions high. Measure the battery voltage, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: The overvoltage protection delay is typically 1.25s

3.7.4.2 Test Data

Apply a $4.1V, 100mA$ source to the umbilical input with an increasing voltage until *COUT* transitions low				
Battery	Capture battery voltage, *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A			$4.265V < V < 4.285V$	
B			$4.265V < V < 4.285V$	

During overvoltage protection, apply a 20Ω resistive load until *COUT* transitions high				
Battery	Capture battery voltage, *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A			$4.145V < V < 4.205V$	
B			$4.145V < V < 4.205V$	

3.7.4.3 Test Notes

Delete me if no notes are required.

3.7.5 Discharge Undervoltage

3.7.5.1 Test Instructions

Discharge or charge the batteries to $3.0V$ before executing this test. For each battery, apply a 20Ω resistive load to *VBATT* until *DOUT* transitions low. Remove the load and apply a $4.1V, 100mA$ source to the umbilical input until *DOUT* transitions high. Measure the battery voltage, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: The undervoltage protection delay is typically 144ms

3.7.5.2 Test Data

Apply a 20Ω resistive load to *VBATT* until D*OUT* transitions low				
Battery	Capture battery voltage, *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A			$2.75V < V < 2.85V$	
B			$2.75V < V < 2.85V$	

During undervoltage protection, apply a $4.1V, 100mA$ source to the umbilical input until *DOUT* transitions high				
Battery	Capture battery voltage, *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A			$2.8V < V < 3.0V$	
B			$2.8V < V < 3.0V$	

3.7.5.3 Test Notes

Delete me if no notes are required.

3.8 3.3V Regulator

Results: Pass / Fail

Configuration:

This test evaluates the circuit described in 3.3V Regulation. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Power Team page of the Wiki under Tutorials and Resources

3.8.1 Voltage

3.8.1.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. With the RBF pin removed, measure the voltage of each 3.3V regulator under no load and under a $1.5A$ resistive load. Ensure the output switches are configured to the correct regulator.

Note: Measure the DC component with PLC[39] > 100

3.8.1.2 Test Data

Measure the voltage of each 3.3V regulator under no load and under a $1.5A$ resistive load				
Regulator	No Load Voltage	$1.5A$ Load Voltage	Passing Criteria	Pass / Fail
A			$3.135V < V < 3.465V$	
B			$3.135V < V < 3.465V$	

3.8.1.3 Test Notes

Delete me if no notes are required.

3.8.2 Ripple and Noise

3.8.2.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. With the RBF pin removed, measure the ripple of each 3.3V regulator whilst under a $1.5A$ resistive load.

Note: Measure the RMS value of the AC component with $3Hz < f$

3.8.2.2 Test Data

Measure the RMS voltage ripple and noise of each 3.3V regulator whilst under a $1.5A$ resistive load.			
Regulator	Capture the ripple	Passing Criteria	Pass / Fail
A		$\left\|V_{ripple}\right\| < 17mV$	Pass
B		$\left\|V_{ripple}\right\| < 17mV$	Pass

3.8.2.3 Test Notes

Delete me if no notes are required.

[39] Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

3.8.3 Efficiency

3.8.3.1 Test Instructions

Measure the efficiency of 3.3V regulator A whilst under a $10mA\ to\ 2.5A$ resistive loads and with $3.0V\ to\ 4.1V$ input voltage.

Note: $Efficiency = \frac{P_{out}}{P_{in}}$, measure the power across the input and output current shunt resistors.

3.8.3.2 Test Data

Measure the efficiency of 3.3V regulator A whilst under a $10mA$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 50\%$	
3.3V				$Efficiency > 50\%$	
3.7V				$Efficiency > 50\%$	
4.1V				$Efficiency > 50\%$	

Measure the efficiency of 3.3V regulator A whilst under a $100mA$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 70\%$	
3.3V				$Efficiency > 70\%$	
3.7V				$Efficiency > 70\%$	
4.1V				$Efficiency > 70\%$	

Measure the efficiency of 3.3V regulator A whilst under a $300mA$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 90\%$	
3.3V				$Efficiency > 90\%$	
3.7V				$Efficiency > 90\%$	
4.1V				$Efficiency > 90\%$	

Measure the efficiency of 3.3V regulator A whilst under a $600mA$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 85\%$	
3.3V				$Efficiency > 85\%$	
3.7V				$Efficiency > 85\%$	
4.1V				$Efficiency > 85\%$	

Measure the efficiency of 3.3V regulator A whilst under a $1.0A$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 80\%$	
3.3V				$Efficiency > 80\%$	
3.7V				$Efficiency > 80\%$	

Measure the efficiency of 3.3V regulator A whilst under a $1.0A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
4.1V				$Efficiency > 80\%$	

Measure the efficiency of 3.3V regulator A whilst under a $1.5A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 75\%$	
3.3V				$Efficiency > 75\%$	
3.7V				$Efficiency > 75\%$	
4.1V				$Efficiency > 75\%$	

Measure the efficiency of 3.3V regulator A whilst under a $2.5A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 70\%$	
3.3V				$Efficiency > 70\%$	
3.7V				$Efficiency > 70\%$	
4.1V				$Efficiency > 70\%$	

3.8.3.3 Efficiency Plot

Create a plot of current versus efficiency with each input voltage.

3.8.3.4 Test Notes

Delete me if no notes are required.

3.8.4 Current Limit

3.8.4.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. For each regulator, apply an increasing load to *3.3V* until the current no longer increases. Measure voltage and current of the rail. Ensure the output switches are configured to the correct battery.

Note: Connect all the power outputs together to share the overcurrent. The load will likely be increased by adding more resistors in parallel or decrease the load resistance. Be sure to not exceed $1A$ per channel.

3.8.4.2 Test Data

Apply an increasing load to *3.3V* outputs until the current no longer increases			
3.3V	Max Current	Passing Criteria	Pass / Fail
A		$4.5A < I < 6A$	
B		$4.5A < I < 6A$	

3.8.4.3 Test Notes

Delete me if no notes are required.

3.9 Load Response - Battery

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Output Switching and Battery & Battery Protection.

3.9.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Apply the following loads to both *VBATT* rails:

- No load to $1A$ resistive load
- $1A$ resistive load to no load
- No load to $10\mu F$ MLCC[40]
- $1A$ resistive load adding $10\mu F$ MLCC

Capture the voltage of the rail under test. Validate the EPS does not misoperate in any way. Ensure the output switches are configured to the correct battery.

3.9.2 Test Data

To each *VBATT* rail, apply no load to $1A$ resistive load			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

To each *VBATT* rail, apply $1A$ resistive load to no load			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

To each *VBATT* rail, apply no load to $10\mu F$ MLCC			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

[40] Multilayer Ceramic Capacitor, CIS PN 13-106A

To each *VBATT* rail, apply $1A$ resistive load and add $10\mu F$ MLCC			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

3.9.3 Test Notes
Delete me if no notes are required.

3.10 Load Response – 3.3V Regulator
Results: Pass / Fail
Configuration: Auden

This test evaluates the circuit described in Output Switching and 3.3V Regulation.

3.10.1 Test Instructions
Discharge or charge the batteries to $3.7V$ before executing this test. Apply the following loads to both *3.3V* rails:

- No load to $1A$ resistive load
- $1A$ resistive load to no load
- No load to $10\mu F$ MLCC
- $1A$ resistive load adding $10\mu F$ MLCC
- No load to short circuit
- Short circuit to no load
- $1A$ resistive load to short circuit
- Short circuit to $1A$ resistive load
- Short circuit continuous

Capture the voltage, and current of the rail under test and the voltage of the sourcing *VBATT* rail. Validate the EPS does not misoperate in any way. Ensure the output switches are configured to the correct battery.

3.10.2 Test Data

To each *3.3V* rail, apply no load to $1A$ resistive load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

To each *3.3V* rail, apply $1A$ resistive load to no load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	

To each *3.3V* rail, apply $1A$ resistive load to no load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
B		No misoperation	

To each *3.3V* rail, apply no load to $10\mu F$ MLCC			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

To each *3.3V* rail, apply $1A$ resistive load and add $10\mu F$ MLCC			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

To each *3.3V* rail, apply no load to short circuit			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

To each *3.3V* rail, apply short circuit to no load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

To each *3.3V* rail, apply $1A$ resistive load to short circuit			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

To each *3.3V* rail, apply short circuit to $1A$ resistive load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	

To each *3.3V* rail, apply short circuit to $1A$ resistive load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
B		No misoperation	

To each *3.3V* rail, apply short circuit continuous load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	

3.10.3 Test Notes

Delete me if no notes are required.

3.11 I²C Bus

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in I²C Bus.

3.11.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. At the test points of each I²C bus, validate signal integrity. The PMIC should generate random I²C traffic on each bus. A slave device might need to be added to execute this test.

3.11.2 Test Data

At the test points of the *I2C* bus, validate the following timing parameters			
Bus	Capture the *SDA* and *SCL* lines	Passing Criteria	Pass / Fail
I2C		Signal Integrity	
PV_I2C		Signal Integrity	
BUS_I2C0		Signal Integrity	
BUS_I2C		Signal Integrity	

3.11.3 Test Notes

Delete me if no notes are required.

3.12 Current Monitoring

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Current Monitoring.

3.12.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Apply a $10mA\ to\ 1.0A$ resistive load to a *PR_BATT-0*. Compare the current measured by the EPS and a DMM.

Note: $Error = \frac{|I_{EPS} - I_{DMM}|}{I_{DMM}}$

3.12.2 Test Data

Apply a $10mA\ to\ 1.0A$ resistive load to a single output channel. Compare the current measured by the EPS and a DMM					
Load	EPS Current	DMM Current	Error	Passing Criteria	Pass / Fail
$10mA$				$Error < 1.0\%$	
$25mA$				$Error < 1.0\%$	
$50mA$				$Error < 1.0\%$	
$100mA$				$Error < 1.0\%$	
$250mA$				$Error < 1.0\%$	
$500mA$				$Error < 1.0\%$	
$1.0A$				$Error < 1.0\%$	

3.12.3 Test Notes

Delete me if no notes are required.

3.13 Voltage Monitoring

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Voltage Monitoring.

3.13.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Compare the voltage measured by the EPS and a DMM on the following signals:

- *UMB_IN*
- *VBATT-A*
- *3.3V-A*

Note: $Error = \frac{|V_{EPS} - V_{DMM}|}{V_{DMM}}$

3.13.2 Test Data

Compare the voltage measured by the EPS and a DMM					
Signal	EPS Voltage	DMM Voltage	Error	Passing Criteria	Pass / Fail
UMB_IN				$Error < 1.0\%$	
VBATT-A				$Error < 1.0\%$	
3.3V-A				$Error < 1.0\%$	

3.13.3 Test Notes
Delete me if no notes are required.

3.14 Temperature Monitoring
Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Temperature Monitoring.

3.14.1 Test Instructions
Discharge or charge the batteries to $3.7V$ before executing this test. Compare the temperature measured by the EPS and a thermometer on the following temperature sensors:

- Battery A
- PMIC
- +X+Y

Note: $Error = |T_{EPS} - T_{THERMOMETER}|$

3.14.2 Test Data

Compare the temperature measured by the EPS and a thermometer					
Sensor	EPS Temperature	Thermometer Temperature	Error	Passing Criteria	Pass / Fail
Battery A				$Error < 2°C$	
PMIC				$Error < 2°C$	
Regulator A				$Error < 2°C$	

3.14.3 Test Notes
Delete me if no notes are required.

3.15 Analog Voltage Reference
Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Analog Voltage Reference and Supply.

3.15.1 Voltage

3.15.1.1 Test Instructions
Discharge or charge the batteries to $3.7V$ before executing this test. With the RBF pin removed, measure the voltage of *VREF*.

Note: Measure the DC component with PLC[41] > 100

[41] Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

3.15.1.2 Test Data

Measure the voltage of each voltage reference				
Signal	Test Point	Voltage	Passing Criteria	Pass / Fail
ADC_REF-0	*TP41*		$2.4925V < V < 2.5075V$	
ADC_REF-1	*TP14*		$2.4925V < V < 2.5075V$	
ADC_REF-2	*TP30*		$2.4925V < V < 2.5075V$	
ADC_REF-3	*TP5*		$2.4925V < V < 2.5075V$	
ADC_REF-4	*TP9*		$2.4925V < V < 2.5075V$	
ADC_REF-5	*TP24*		$2.4925V < V < 2.5075V$	
ADC_REF-6	*TP10*		$2.4925V < V < 2.5075V$	
ADC_REF-7	*TP39*		$2.4925V < V < 2.5075V$	
AVREF-0	*TP13*		$2.48V < V < 2.52V$	
AVREF-1	*TP38*		$2.48V < V < 2.52V$	

3.15.1.3 Test Notes

Delete me if no notes are required.

3.15.2 Ripple and Noise

3.15.2.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the RBF pin removed, measure the ripple of *VREF*.

Note: Measure the RMS value of the AC component with $3Hz < f$

3.15.2.2 Test Data

Measure the RMS voltage ripple and noise of each voltage reference				
Signal	Test Point	Voltage	Passing Criteria	Pass / Fail
ADC_REF-0	*TP41*		$\lvert V_{ripple} \rvert < 250\mu V$	
ADC_REF-1	*TP14*		$\lvert V_{ripple} \rvert < 250\mu V$	
ADC_REF-2	*TP30*		$\lvert V_{ripple} \rvert < 250\mu V$	
ADC_REF-3	*TP5*		$\lvert V_{ripple} \rvert < 250\mu V$	
ADC_REF-4	*TP9*		$\lvert V_{ripple} \rvert < 250\mu V$	
ADC_REF-5	*TP24*		$\lvert V_{ripple} \rvert < 250\mu V$	
ADC_REF-6	*TP10*		$\lvert V_{ripple} \rvert < 250\mu V$	
ADC_REF-7	*TP39*		$\lvert V_{ripple} \rvert < 250\mu V$	
AVREF-0	*TP13*		$\lvert V_{ripple} \rvert < 2.5mV$	
AVREF-1	*TP38*		$\lvert V_{ripple} \rvert < 2.5mV$	

3.15.2.3 Test Notes

Delete me if no notes are required.

3.16 PMIC Programming

Results: Pass / Fail
Configuration:

This test evaluates the circuit described in Programming Connections.

3.16.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Connect a SWD programmer to the SWD header and upload an image, validate the PMIC is properly programmed. Connect a JTAG programmer to the backplane and upload an image, validate the PMIC is properly programmed.

Note: Follow the programming instructions on the wiki.

3.16.2 Test Data

Program the PMIC via SWD and JTAG, validate the PMIC is properly programmed		
Programmer	Passing Criteria	Pass / Fail
SWD	PMIC properly programmed	
JTAG	PMIC properly programmed	

3.16.3 Test Notes

Delete me if no notes are required.