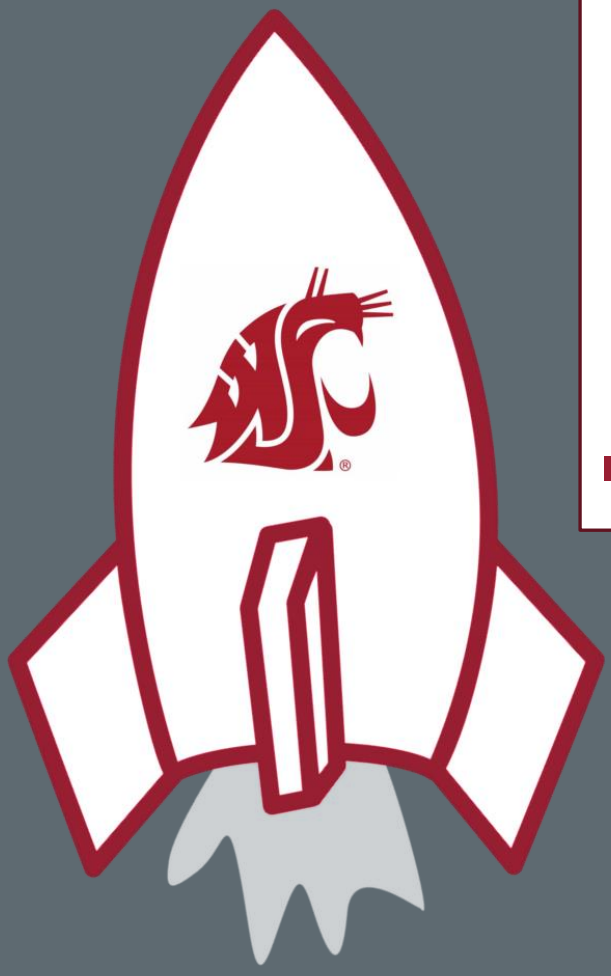
This document explains the function of the -Z Panel, its schematic level design, its board level design, and its functional testing

-Z Panel

High Gain Communication Antenna

Revision: 1.0.0



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1 Introduction

This document explains how the -Z Panel will fulfill the following Functions and conform to the following Requirements. This document refers to the -Z Panel version 1.0.

1.1 Functions

The -Z Panel is responsible for the following:

- Provide the high gain communication antenna
- Provide a Sun sensor for the ADCS

1.2 Requirements

The system requirements and -Z panel requirements can be found here.

2 Detailed Description

This section references the -Z panel schematic.

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 High Gain 230mm Antenna

The high gain antenna is responsible for transmitting large data files and is controlled by the Comms system.

2.1.2 Antenna Deploy Release

The antenna deploy release is responsible for deployment of the high gain antenna and is controlled by the EPS system.

2.1.3 Photodiodes

The photodiodes are used as sun sensors for the ADCS system to determine the location of the sun. There is one photodiode on the -Z Panel.

2.1.4 Analog-to-Digital Converter

The analog to digital converter (ADC) is meant to convert the photodiode analog signal to a digital signal for the ADCS system.

2.2 Schematic

2.2.1 Isolated Grounds

On page 2 of the schematic (D1), are the four isolated grounds found on the board. Power ground (PGND) is directly connected to the backplane and most of the power chain. The other grounds are shorted to PGND using a 0Ω resistor rated up to $2A$, the expected current is less than $50mA$ each. Digital ground (DGND) connects to the digital circuity including the PMIC and Monitoring circuits. Analog ground (AGND) connects to analog monitoring circuits including the ADCs, their voltage reference, and the thermistors. Chassis ground (CHASSIS) is connected to the Mechanical Features including bolt holes and the card rails.

2.2.2 Photodiode

The photodiode can be found on page 2 of the schematic connected to the ADC. This photodiode is connected through the ADC to the ADCS system. This photodiode has a spectral sensitivity of $6.3nA/lx$ and the expected illuminance is on the order of $< 1Mlx$. This makes the expected voltage drop across the load resistor about $0.9V$.

2.2.3 Analog-to-Digital Converter

The ADC is located on page 2 of the schematic. The ADC connects the photo diode to the ADCS system so the ADCS system can determine the location of the sun.

2.2.4 Antenna Deploy Release

The deploy release system is located on page 2 of the schematic. Four flaps function to hold the antenna down before release that are loaded with springs. There are contacts on the springs to verify if the flaps have been opened. The deployment system functions by cutting the plastic line used to tie the flaps together with high temperature 15Ω resistors. When the line is cut the springs push the flaps to swing out and the antenna is deployed.

2.2.5 High Gain 230mm Antenna

The antenna contact is located on page 2 of the schematic. The antenna is helically shaped with a circular polarization. The antenna is held down by 4 flaps ready for an irreversible deployment. Directivity of the antenna is 48.5669 and the gain is 11.8.

2.3 Board

The board shall be double layered with 1oz copper and ENIG finish.

2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters specified below. Signals in the following subsections do not include their sense signals unless specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width:	$0.2mm$
Vias:	$0.3mm$, unlimited count
Separation:	$0.2mm$
Length:	unlimited

2.3.1.1 I^2C-I2C_[SDA, SCL]

Length:	Each node shall be length matched $\pm 1.0mm$
Stubs:	$< 10.0mm$