This document explains the function of the Comms, its schematic level design, its board level design, and its functional testing

Comms

In-Orbit Communication Subsystem Design

Revision: 1.0.0

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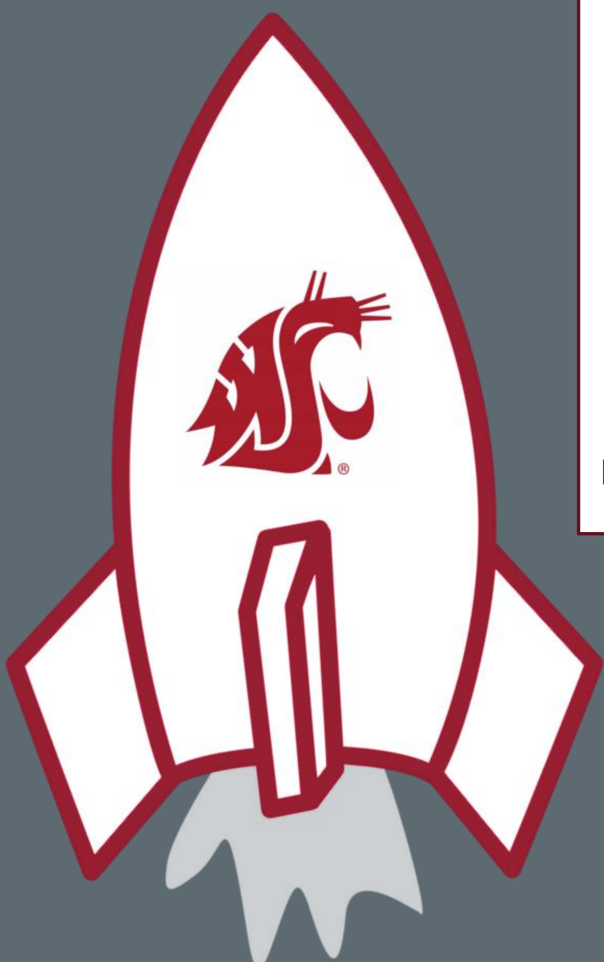

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1 Introduction

This document explains how the Comms will fulfil the following Functions and conform to the following Requirements. This document refers to the Comms version 1.0, +X Panel version 1.0, and -Z Panel version 1.0.

1.1 Function

The In-Orbit Communication Subsystem (Comms) is responsible for the following:

- Transferring telemetry to the ground station
- Transferring payload data to the ground station
- Transmitting a locating beacon

1.2 Requirements

The system requirements and Comms design requirements can be found on GitHub.

1.3 Open Systems Interconnection (OSI) Model

The OSI model[1] is a conceptual model that can be applied to any communication system. It has seven layers; each layer serves the layer above it and is served by the layer below it.

1.3.1 Layers

Layer			Protocol data unit	Function
Host layers	7	Application	Data	High-level APIs
	6	Presentation		Translation of data between a networking service and an application
	5	Session		Managing communication sessions
	4	Transport	Segment	Reliable transmission of data segments between points on a network
Media layers	3	Network	Packet	Structuring and managing a multi-node network
	2	Data link	Frame	Reliable transmission of data frames between two nodes connected by a physical layer
	1	Physical	Symbol	Transmission and reception of raw bit streams over a physical medium
	0	Medium	Electrons, Photons	The physical medium: copper, fiber, wireless

[1] For more information, read Wikipedia's article on the OSI model

1.3.2 CougSat Communication Subsystem

The communication subsystem, formed from the in-orbit and ground subsystems, fulfils layers 0 through 2 of the OSI model. It serves the Command and Data Handling (C&DH) subsystem which fulfils layers 3 and up. The in-orbit and ground subsystems are very similar as they are required to be compatible. For details on the ground subsystem, see its design document.

1.3.2.1 Layer 0

The communication subsystem is using wireless transmission, in the radio frequency band. There are two bands utilized: $700mm$ and $230mm$. The $700mm$ radio is the primary radio used for telemetry and beacon. The $230mm$ radio is the secondary radio used for payload data transfers and only operates in downlink mode.

1.3.2.2 Layer 1

The modulation scheme used is Quadrature Phase Shift Keying (QPSK)[2]. Each symbol is a change in the phase constant of the RF wave. The radios are software defined radios which allows reconfiguration of this layer if necessary. Other modulation schemes can be developed if the hardware supports it.

1.3.2.3 Layer 2

See the Comms µController's Framing Protocol.

1.3.2.4 Layer 3 and Up

See the C&DH's Communication Protocol.

1.4 Link Budget

A link budget for downlink and uplink was tabulated indicating a transmit power of $1W$ is sufficient for up to $500kbps$ on the $230mm$ band. The $700mm$ band transmitter with incur less loses and send slower data so $1W$ is also sufficient. Uplink has no problems thanks to access to high gain and high-power transmitters on the ground.

[2] For more information, read Wikipedia's article on Phase Shift Keying (PSK)

2 Detailed Description

This section references the Comms schematic. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Comms µController

The Comms µController is responsible for interfacing the radio signals and the Command and Data Handling subsystem[3]. This fulfils OSI model[4] layers 1 and 2. It samples and synthesizes the baseband signals which are mixed with the carrier wave. This constitutes a software defined radio. The µController has non-volatile storage in the form of µSD cards to store configurations and reference waveforms.

2.1.2 RF Clock Generators

Each radio has a configurable clock generator used to synthesize the carrier waves. For the transmission of the beacon, the generator is the direct source to the antenna[5].

2.1.3 700mm Receiver Radio

The RF diagram is the top row on page 2. The RF signal from the antenna is connected to the receiver radio via a high isolation RF switch. This switch prevents the transmitter from overdriving the sensitive receiver components and inducing damage. The signal is then amplified by low noise amplifiers which add very little noise to the signal to maintain the highest signal to noise ratio. The signal is then connected to the demodulator[6] which removes the carrier frequency and splits that baseband signal into in-phase and quadrature-phase signals which are then sampled by the Comms µController and demodulated into binary. The receiver radio is designed for continuous operation and low power[7].

2.1.4 700mm Transmitter Radio

The RF diagram is the middle row on page 2. The Comms µController generates in-phase and quadrature-phase baseband signals using its digital to analog converter. This allows arbitrary waveform including voice signals[8]. These signals feed the modulator[9] which puts the baseband signals on the carrier wave. This modulated RF gets amplified with a power amplifier to transmit the desired $1W$, see the Link Budget.

[3] Requirements COMMS-008, COMMS-009
[4] Open Systems Interconnection (OSI) Model
[5] Requirements COMMS-001
[6] The IC called a demodulator is actually a mixer and phase splitter
[7] Requirement COMMS-005
[8] Requirement COMMS-006
[9] The IC called a modulator is actually a mixer and a phase splitter

2.1.5 230mm Transmitter Radio

The Comms µController generates in-phase and quadrature-phase baseband signals using fast GPIO. This only allows each signal to be discrete positive or negative as found in QPSK modulation. If arbitrary waveforms are desired, an external DAC is needed. These signals feed the modulator which puts the baseband signals on the carrier wave. This modulated RF gets amplified with a power amplifier to transmit the desired $1W$, see the Link Budget.

2.1.6 5V & 9V Boost Converters

The RF chains require 5V and 9V supplies which come from boost converters. The converters are sourced from the battery rail.

2.2 Schematic

2.2.1 Isolated Grounds

On page 3 of the schematic (D1), are the six isolated grounds found on the Comms. Power ground *(PGND)* is directly connected to the backplane and most of the boost converters. The other grounds are shorted to *PGND* using a 0Ω resistor rated up to $2A$, the expected current is less than $500mA$ each. Digital ground *(DGND)* connects to the digital circuity including the Comms µController. Analog ground *(AGND)* connects to analog circuits including the ADCs, their voltage reference, the thermistors, and the operational amplifiers. Chassis ground *(CHASSIS)* is connected to the Mechanical Features including bolt holes and the card rails. The 230mm RF chain and the 700 RF chains each have their own RF grounds *(RFGND-0* and *RFGND-1)*.

2.2.2 Power Rails

Page 3 of the schematic illustrates all the power rails on the Comms. Each RF chain can be turned off to save power and as a radio inhibit[10].

2.2.3 Comms µController

The Comms µController (page 4, A3, B1, B2, & B4) is a microcontroller from the STM32 low power family[11]. It was chosen for its ease of programming, and low power consumption. It needed fast ADCs and DACs for sampling and synthesizing the baseband signals.

The µController's reset pin is connected to the backplane such that if it or any subsystem needs to reset itself, all the subsystems reset. This is to put all the subsystems in a known state which reduces cause for error.

2.2.3.1 Programming Connections

During testing, the Comms µController is programmed via Serial Wire Debug[12] (SWD, page 4, A1). The process of programming is made simple with just a single 6 pin header and a robust software utility. In orbit, the µController can be

[10] Requirement REQ-005
[11] STM32L476RG
[12] For more information, see ARM's article on SWD

programmed via JTAG[13]. The In-Flight JTAG Reprogrammer (IFJR) connects via the backplane, through a tri-state buffer/logic level converter[14] (page 4, C1:D2). The IFJR can enable or disable the tri-state buffer which essentially disconnects the JTAG interface from the Comms μController (it outputs high impedance), allowing the SWD to program. The logic level conversion feature is not used.

2.2.4 I²C Bus

The Comms μController has one I²C bus (page 4, C4). It connects to the monitoring ADCs.

2.2.4.1 ADCs

There are 3 ADCs[15] connected to the Comms μController, each with 16 single-ended inputs or eight differential inputs or a combination. The ADC was chosen for its low power, differential inputs, small package, and up to 27 addresses. The list of address follow:

- [`0xEE`] Global ADC address
- [`0x28`] ADC-0 (page 10, A2), voltage and current
- [`0x2A`] ADC-1 (page 10, A4), voltage and current
- [`0x2E`] ADC-2 (page 10, C2), voltage and current

2.2.5 SPI Bus

The Comms μController has three SPI buses[16]. One connects to the C&DH to transfer packets and telemetry. One connects to the RF Clock Generators. One connects to the μSD cards.

2.2.5.1 Backplane to the C&DH

The Comms μController is a slave to the C&DH, see the interface document for details.

2.2.5.2 RF Clock Generators

The Comms μController is a transmit only master to the RF Clock Generators.

2.2.5.3 μSD Cards

The Comms μController is a master to two μSD cards.

2.2.6 Current Monitoring

At various locations, the power chain has shunt resistors connected to differential ADCs to monitor the current. Those locations are:

- 5V Regulator output (page 6, B6)
- 9V Regulator output (page 6, C6)
- Each RF chain input (page 7)

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[13] For more information, see Wikipedia's article on JTAG
[14] SN74LVC244AR
[15] LTC2499
[16] For more information, see Wikipedia's article on SPI

2.2.7 Voltage Monitoring

At various locations, the power chain is probed for the voltage using one of the ADCs in single ended mode. Those locations are:

- 5V Regulator output (page 6, B6)
- 9V Regulator output (page 6, C6)

2.2.8 Temperature Monitoring

At various locations, the temperature is monitored using thermistors and one of the ADCs in single ended mode. Those locations are:

- 5V Regulator (page 6, A3)
- 9V Regulator (page 6, C3)
- Comms µController (page 4, B4)
- RF clock generators (page 8, A2, B5, & C2)
- 230mm downlink RF chain (page 10, B3, B5, & D4)
- 700mm downlink RF chain (page 11, B3, B5, & D5)
- 700mm uplink RF chain (page 12, B4 & C4; page 13, C4)

2.2.9 Analog Voltage Reference and Supply

The Comms has a precision voltage reference (page 5, B6)[17] for calibrating the ADCs. This is inputted into one of the channels which provide calibration through linear math. The ADCs have the analog voltage supply inputted into the reference input. They also have a voltage divider between the channel inputs and the actual ADC input (page 5, B2, B4, & D2) which allows 5.64 times the voltage for a total range of $(\pm 1.65V * 5.64) = \pm 9.3V$ and a resolution at $16b$ of $\frac{9.3V}{2^{16}} = 142\mu\frac{V}{LSB}$.

The Comms has an analog voltage supply (page 5, C6) which is fed by the *3.3V* rail filtered with a ferrite bead and capacitors. Precision is not required as all ADCs use the precision voltage reference for calibration. This is the source for the Temperature Monitoring thermistors and op-amplifiers. A negative voltage supply[18] for the op-amps takes the *3.3V* rail and inverts it (page 9, C4:C6).

2.2.10 5.0V Regulation

The 5.0V regulator (page 6, B1:B6) is switching mode, boost topology. The converter[19] automatically senses the output voltage and adjusts the switching parameters to keep the output at $5.0V$. The converter has an integrated switching MOSFET. The converter was chosen for its small size and high efficiency.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

[17] MCP1501
[18] LM2776
[19] TPS61236

The converter and inductor (page 6, B2:B3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

2.2.11 9.0V Regulation

The 9.0V regulator (page 6, C1:C6) is switching mode, boost topology. The converter[20] automatically senses the output voltage and adjusts the switching parameters to keep the output at $9.0V$. The converter has an integrated switching MOSFET. The converter was chosen for its small size and high efficiency.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

The converter and inductor (page 6, C2:C3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

2.2.12 Low Drop-Out Regulators

The sensitive RF components are supplied through low drop-out (LDO) regulators[21]. These are linear regulators that require a small drop-out[22] for proper regulation. They are used to reject the switching noise from the switching mode power supplies.

2.2.13 RF Clock Generators

The RF Clock Generators[23] have a voltage-controlled oscillator and a phase-locked loop to take a reference clock and synthesize a RF wave. The reference clocks[24] (page 8, A1, B4, & C1) have high frequency stability and are supplied with ferrite beads to further increase frequency stability. The supporting circuitry for the generators was created using Analog Device's ADIsimPLL. The design files can be found under the documentation folder. The output of the generators is designed to drive a 50Ω load.

The 700mm Receiver Radio's demodulator divides its clock input by two, so the RF clock generator needs to output double the carrier frequency.

2.2.14 Differential Drivers

The Comms µController outputs its basebands signals $0 - 3.3V$ single ended. The modulators' baseband signals are differential with a different amplitude. The differential output op-amps[25] (page 9, A1:D3) are used to perform this translation. The µController input is subtracted from a $1.65V$ reference (page 9, A4:A6) then multiplied by the proper gain to have the $3.3Vpp$ signal reduced to

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20 TPS61089
21 TPS73250 and LP5907
22 Voltage difference between input and output
23 ADF4360
24 ECS-TXO-3225
25 AD8137

$1.0Vpp$ or $0.6Vpp$ as the modulator desires. This signal is then added to the proper common mode voltage reference (page 9, B4:B6, C4:C6). This circuit was simulated in LTSpice and can be found under electrical design. Precision resistors are used to reduce any common mode offset or gain imbalance.

2.2.15 RF Modulators

The 700mm Transmitter Radio's modulator (page 11, B3) and the 230mm Transmitter Radio's modulator (page 10, B3) have the RF Clock Generators AC coupled into their local oscillator input, and the Differential Drivers are directly connected to the baseband inputs. The RF output is AC coupled to the next element in the RF chain.

2.2.16 RF Demodulator

The 700mm Receiver Radio's demodulator (page 13, B3:B4) has the RF Clock Generators AC coupled into its local oscillator input. The 60.4Ω termination resistor is used to match a 50Ω input into the demodulator. The RF signal is connected to the modulator's input through a $1:4$ balun (page 13, B2) to match a 50Ω input into the demodulator. The gain of the demodulator is set by a voltage divider (page 13, B2).

The demodulator outputs differential baseband signals $1.0V \pm 500mV$. this amplified and translated to $1.65V \pm 1V$ single ended for input to the Comms µController's ADC by op-amps[26] (page 13, C2 & C5). This circuit was simulated in LTSpice and can be found under electrical design.

2.2.17 Low Noise Amplifier

The low noise amplifiers (LNA)[27] (page 10, B5; page 11, B5; page 12, B3 & C3) amplify the RF signal for the next component in the RF chain. They were chosen for their low noise figure, broadband response, and high gain. The gain is set by the bias voltage and is $19dB$. For the 700mm Receiver Radio's LNAs, the bias voltage can be shorted to ground which disables the amplifier. This is required, along with toggling the RF switch, when transmitting on $700mm$ to not damage the demodulator. The output is biased via a ferrite bead to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the next component.

2.2.18 Power Amplifier

The power amplifiers[28] (page 10, C4; page 11, C4) are the final amplifiers for the RF signal. They drive the antennas and output the desired $1W$, see the Link Budget. They were chosen for the output power, linearity, and broadband response. The gain is set by the bias voltage of $-4\ to\ 0V$. The Comms µController outputs a PWM signal which is filtered and inverted to achieve an adjustable range of $-3.3V\ to\ 0V$. This is achieved by op-amps[29]. This circuit was simulated in

[26] AD8515
[27] MAAP-011229
[28] MAAP-011232
[29] AD8515

LTSpice and can be found under electrical design. The output is biased via an inductor to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the antenna.

2.2.19 Mechanical Features

The 5V & 9V Boost Converters heatsink (page 6, D1:D2) and RF chain heatsinks (page 10, D1; page 11, A1) mount directly to the Comms board using bolts. These holes are conductive and connected directly to *CHASSIS*, see Isolated Grounds. The Comms also slots into the structure using rails[30] which are also conductive and connected directly to chassis ground. Each of the holes have a capacitor and resistor connecting to power ground which will absorb and dissipate transients.

2.3 Board

The board shall also conform to the dimensions specified by the CougSat Module Standard.

2.3.1 Layer Stack-Up

The board shall be four layered with ENIG finish, see Figure 1. Only through vias shall be used. The external copper weight shall be $35\mu m$ and the internal copper weight shall be $18\mu m$.

Layer	Thickness	Primary Function
1 (top)	$35\mu m$ $(1oz)$	SMD components, RF & signal traces
Prepreg	$200\mu m$	
2	$18\mu m$ $(0.5oz)$	Ground planes
Core	$500\mu m$	
3	$18\mu m$ $(0.5oz)$	Power planes
Prepreg	$200\mu m$	
4 (bottom)	$35\mu m$ $(1oz)$	Signal traces

Figure 1: Stack-Up

2.3.2 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless otherwise specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width: $0.16mm$
Vias: $\emptyset 0.3mm$, unlimited count
Separation: $0.16mm$
Length: unlimited

Devices with specific placement and routing considerations are called out on the schematic, see "CAD Note:"

[30] See backplane documentation for details

2.3.2.1 All 50Ω Impedance Traces
This applies to all RF traces expect the demodulator's RF input. These traces shall be a coplanar waveguide with ground[31].

Trace width:	$0.4mm$
Gap width:	$0.5mm$
Vias:	none
Length:	minimize

2.3.2.2 All 200Ω Impedance Traces
This applies to the demodulator's RF input. These traces shall be an edge coupled microstrip[32] with differential impedance of 200Ω. Ground located on second layer below ($0.8mm$ substrate thickness).

Trace width:	$0.16mm$
Gap width:	$0.4mm$
Vias:	none
Length:	minimize

2.3.2.3 All Differential Signals
This applies to the modulators' inputs. Single ended to/from differential shall occur as close to the single ended side as possible.

Trace width:	$0.16mm$
Gap width:	$0.16mm$
Length:	Length match $\pm 1.0mm$
Vias:	minimize

2.3.2.4 Regulator Inputs - VBATT, PGND
This applies to *VBATT* and *PGND* between the backplane and the inputs to the regulators and their input capacitors.

Trace width:	$1.0mm$ ($2.0mm$ on internal layers)

2.3.2.5 Regulator Outputs - 5.0V, 9.0V, PGND
PGND applies to between the regulators, their output capacitors, and the backplane.

Trace width:	$0.5mm$ ($1.0mm$ on internal layers)

2.3.2.6 Regulator Channels - 3.3V_[0:3], 5.0V_[0:3], 9.0V_[0:1], PGND
PGND applies to between the regulators, their loads, and the backplane.

Trace width:	$0.5mm$ ($1.0mm$ on internal layers)

2.3.2.7 SPI Buses - SPI_[SCK, MOSI, MISO, CS], RFCLK_[SCK, MOSI, CS], COM_SPI_[SCK, MOSI, MISO, CS]

Length:	Each node shall be length matched $\pm 1.0mm$
Stubs:	$< 10.0mm$

[31] For more information, read Microwaves101's article on CPW
[32] For more information, see Microwaves101's article on microstrips

2.3.2.8 JTAG - JTAG_[TCK, TDI, TDO, TMS], BUS_JTAG-[TCK, TDI, TDO, TMS]

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

2.3.2.9 I²C - I2C_[SCL, SDA]

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

3 Testing

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test[33].

- Waveforms shall be captured whenever appropriate
- Have the event take fill the screen (for fast events, zoom in; for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-PowerBoard/Testing/Comms.1.0

Common test instructions can be found on the wiki.

[33] For test 3.1, place files in the subfolder *"3.1"* and so on