This document explains the function of the Solar Panel, its schematic level design, and its board level design

# Solar Panel

Solar Panel Design

Revision: 2.1.0

Hendrik Melse



## **Table of Contents**

1	Intr	roduct	tion3	,
	1.1	Fun	ctions3	,
	1.2	Req	uirements3	,
2	Det	tailed	Description4	۲
	2.1	Fun	ctional Block Diagram4	ŀ
	2.1	.1	Energy Collection	ŀ
	2.1	.2	Power Output4	ŀ
	2.1	.3	ADC4	ŀ
	2.1	.4	Magnetorquer4	ŀ
	2.1	.5	Connector4	Ļ
	2.2	Sche	ematic4	Ļ
	2.2	.1	Isolated Grounds4	Ļ
	2.2	.2	Battery Charger4	Ļ
	2.2	.3	ADC5	,
	2.2	.4	Magnetorquer5	,
	2.2	.5	Voltage Reference5	,
	2.3	Boa	rd5	)
	2.3	.1	Layout Constraints5	,
3	Tes	ting	7	,
	3.1	Befo	ore First Power-On Check7	,
	3.1	.1	Test Instructions	,
	3.1	.2	Test Data	,
	3.1	.3	Test Notes	,
	3.2	Batt	tery Chargers7	,
	3.2	.1	Output Voltage8	;
	3.2	.2	Output Efficiency8	;
	3.2	.3	Output Current Limiting9	)
	3.3	ADC	<u> </u>	į
	3.3	.1	Current Monitoring9	)
	3.3	.2	Voltage Monitoring9	)





3.3.3 Temperature Monitoring ......10





## 1 Introduction

This document explains how the solar panel will fulfill the following Functions and conform to the following Requirements. This document refers to the Solar Panel version 2.0.

#### 1.1 Functions

The Solar Panel is responsible for the following:

- Harvest energy
- Providing power to charge the batteries located on the EPS

## 1.2 Requirements

The system requirements and EPS design requirements can be found <u>here</u>.





## 2 Detailed Description

This section references the Solar Panel <u>schematic</u><sup>1</sup>. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

## 2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

## 2.1.1 Energy Collection

Energy is captured from the sun by the photovoltaic cells. There are two cells on each panel. Each PV is connected to its own battery charger with MPPT<sup>2</sup>.

#### 2.1.2 Power Output

Power is output via two 4.1V, 500mA current limited rails from the battery chargers, one from each battery charger.

#### 2.1.3 ADC

The ADC allows the PMIC to monitor temperature and power at various locations on the board. Sensor locations are indicated on the block diagram.

#### 2.1.4 Magnetorquer

The magnetorquer is controlled by the ADCS.

#### 2.1.5 Connector

The connector connects the solar panel to the EPS and the ADCS to the magnetorquer.

#### 2.2 Schematic

#### 2.2.1 Isolated Grounds

The four isolated grounds are found on page 2 of the schematic. Power ground (PGND) is connected to pins 6 and 7 of the connector. All other grounds are shorted to PGND with a  $0\Omega$  resistor rated for up to 2A. Digital ground (DGND) is connected to the digital components of the board. Analog ground (AGND) is connected to the analog components, including the ADC, its voltage reference, and the thermistors. Chassis ground (CHASSIS) is connected to the conductive mechanical components of the board, including the bolt holes.

#### 2.2.2 Battery Charger

Page 2 of the schematic contains the battery chargers. Each battery charger has a single 4.1V output, current limited to 500mA. The battery charger. The batteries are capable of charging at up to 4.2V, but by charging at 4.1V the

<sup>&</sup>lt;sup>2</sup> Maximum Power Point Tracking adjusts the output voltage and current to maximize the power taken from the solar cells





<sup>&</sup>lt;sup>1</sup> https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-PowerBoard/Documentation/SolarPanel.pdf

battery health can be preserved. The active low shutdown pin (X\_SHUT) is pulled up to the PV output by  $10k\Omega$  and  $1k\Omega$  resistors in series. output voltage and current are monitored by the ADC.

#### 2.2.3 ADC

Page 4 of the schematic contains the ADC. The ADC has 16 single-ended inputs, or 8 differential inputs, or a combination of the two. The solar panel contains one ADC. The ADC's address can be configured by selectively stuffing³ the resistors connected to the address pins. Each pin can be set to either high, low, or left floating. Specific addresses can be found in the EPS design document. The ADC measures differential for each PV input, and each 4.1V output. Measured as single ended is the temperature at five different locations, the 4.1V outputs from each battery charger, and the analog voltage rail (AVDD).

The ADC's MUXOUT[P,N] pins are fed into the voltage divider, cutting the voltage in half before being routed back into ADCIN[P,N] in order to bring the voltage down to the range that the ADC is capable of measuring. The total resistance of the voltage divider is  $40k\Omega$ , which is the resistance required by the thermistors to function properly. The

#### 2.2.4 Magnetorquer

The magnetorquer can be found on page 3 of the schematic. The magnetorquer is directly connected to pins 8 and 9 on the connector. These will go directly to the ADCS. The magnetorquer shall only be installed on the +Z, -Y, and -X boards, as only three axes are necessary to control the orientation of the satellite.

#### 2.2.5 Voltage Reference

The high-precision buffered voltage reference can be found on page 2 of the schematic (A5). This chip produces a high precision reference voltage (AVREF), nominally 1.800V. AVREF is used as the absolute voltage reference for calibrating the ADC.

#### 2.3 Board

The board shall be double layered with 1oz copper and ENIG finish.

#### 2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters specified below. Signals in the following subsections do not include their sense signals unless specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width: 0.2mm

Vias:  $\emptyset 0.3mm$ , unlimited count

Separation: 0.2mm

<sup>&</sup>lt;sup>3</sup> Stuffing refers to populating a component during assembly





Length: unlimited

Devices with specific placement and Routing considerations are called out in the schematic, see "CAD Note"

#### 

Length: Each node shall be length matched  $\pm 1.0mm$ 

Stubs: < 10.0mm

#### 2.3.1.2 Solar Panel Outputs - PV\_IIN\_P-[A:B], PV\_IIN\_P-[A:B], PGND

PGND Applied between the solar panel and output connector

Trace width: 0.6mm

#### 2.3.1.3 MPPT Inputs - MPPT\_LX-[A:B], PGND

PGND applies between the battery charger and the output connector

Trace Width: 0.6mm

#### 2.3.1.4 Power Outputs - MPPT\_VOUT-[A:B], VOUT-[A:B]

Trace width: 0.6mm

#### 2.3.1.5 Magnetorquer Inputs - MAGNETORQUER\_[P, N]

Trace width: 0.6mm

#### 2.3.1.6 Input/Output Capacitors - PGND

PGND applies between the input/output capacitors and the output connector

Trace width: 0.6mm





## 3 Testing

All tests shall eb performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test. All tests shall be performed prior to attaching the solar cells to the solar panel.

- Waveforms shall be captured whenever appropriate.
- Have the event take fill the screen (for fast events, zoom in, for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: <a href="https://github.com/CougsInSpace/CougSat1-">https://github.com/CougsInSpace/CougSat1-</a> Hardware/tree/master/CougSat1-PowerBoard/Testing/SolarPanel.2.0

Common test instructions can be found on the wiki.

#### 3.1 Before First Power-On Check

This test is required to be executed before batteries are attached and before any external power is applied to the Solar Panel.

#### 3.1.1 Test Instructions

Measure the resistance of various points in reference to PGND located at the output connector.

#### 3.1.2 Test Data

Node	Resistance	Node	Resistance
I2C_SDA_PMIC		VOUT-A	
I2C_SCL_PMIC		VOUT-B	
I2C_SDA_ADCS		AVDD	
I2C_SCL_ADCS		AVREF	
PV_IIN_P-A		3.3V	
PV_IIN_P-B			

#### 3.1.3 Test Notes

Delete me if no notes are required

#### 3.2 Battery Chargers

Results: Pass / Fail





This test evaluates the Battery Charger.

#### 3.2.1 Output Voltage

#### 3.2.1.1 Test Instructions

Apply 3.3V to the input connector before executing this test. Apply 2.5V at the solar cell output and measure the voltages of VOUT-A and VOUT-B under no load and a 300mA resistive load.

#### 3.2.1.2 Test Data

Αρρίγ 2.5 <i>V</i> 1	Apply 2.5V to PV_IIN_P-A and measure the voltage of VOUT-A at the output						
	connector.						
Load	Load Measured Voltage VOUT-A Passing Criteria Pass / Fail						
No Load		3.9V < V < 4.3V					
300mA		3.9V < V < 4.3V					

Αρρly 2.5 <i>V</i> 1	Apply 2.5V to PV_IIN_P-B and measure the voltage of VOUT-B at the output						
	connector.						
Load	Measured Voltage VOUT-B	Passing Criteria	Pass / Fail				
No Load		3.9V < V < 4.3V					
300mA		3.9V < V < 4.3V					

#### *3.2.1.3 Test Notes*

Delete me if no notes are required

#### 3.2.2 Output Efficiency

#### 3.2.2.1 Test Instructions

Apply 3.3V to the input connector before executing this test. Apply 2.5V at the solar cell outputs. Measure the efficiency of the Battery Chargers under 10mA to 300mA resistive load.

Note:  $Efficiency = \frac{P_{out}}{P_{in}}$ , measure the power across the input and output current shunt resistors.

#### 3.2.2.2 Test Data

Measu	Measure the efficiency of battery charger A under a $10mA$ to $300mA$ resistive								
	load.								
Load Power in Power out Efficiency Passing Criteria Pass									
10mA			Efficiency > 90%						
40mA			Efficiency > 90%						
120mA				Efficiency > 90%					
300mA Efficiency >									





#### 3.2.2.3 Test Notes

Delete me if there are no notes

## 3.2.3 Output Current Limiting

#### 3.2.3.1 Test Instructions

Apply 3.3V to the input connector before executing this test. Apply 2.5V at the solar panel output. Apply an increasing load to the Battery Charger output until the current no longer increases.

#### 3.2.3.2 Test Data

Apply an increas	Apply an increasing load to the output until the current no longer increases.							
Output	ıt Max Current Passing Criteria Pass / Fa							
VOUT-A		500mA < I < 700mA						
VOUT-B		500mA < I < 700mA						

#### 3.3 ADC

Results: Pass / Fail

## 3.3.1 Current Monitoring

#### 3.3.1.1 Test Instructions

Connect the EPS to the Solar Panel with a cable connecting only I2C and GND and charge or discharge the batteries to 3.7V, and apply 2.5V to the solar panel outputs before executing this test. Apply a 10mA to 300mA resistive load to the solar panel output and compare the currents measured by the EPS and a DMM.

#### 3.3.1.2 Test Data

Αρρly 2.5 <i>V</i>	Apply 2.5V at the solar panel output and measure the current across VOUT-A for $10mA$ to $300mA$ resistive loads.							
Current EPS current DMM current Error Passing Criteria Pass / Fai								
10mA								
40mA								
120mA								
300mA								

#### 3.3.1.3 Test Notes

Delete me if no notes are required.

#### 3.3.2 Voltage Monitoring

#### 3.3.2.1 Test Instructions

Connect the EPS to the Solar Panel with a cable connecting only I2C and GND and charge or discharge the batteries to 3.7V, and apply 2.5V to the solar panel





outputs before executing this test. Apply a 40mA resistive load to the solar panel output and compare the output voltages measured by the EPS and a DMM.

#### 3.3.2.2 Test Data

Apply a 4	Apply a $40mA$ resistive load to VOUT-A and measure the voltage at various signals.							
Signal	Signal EPS Voltage DMM Voltage Error Passing Criteria Pass / Fail							
VOUT-A	VOUT-A Error < 1.0%							
VOUT-B	VOUT-B   <i>Error</i> < 1.0%							

#### *3.3.2.3 Test Notes*

Delete me if no notes are required.

#### 3.3.3 Temperature Monitoring

#### 3.3.3.1 Test Instructions

Connect the EPS to the Solar Panel and charge or discharge the batteries to 3.7V before executing this test. Compare the temperature measured by the EPS and a thermometer at the following thermistors:

- FRONT\_TOP
- MPPT-A

#### 3.3.3.2 Test Data

Compare the temperature measured by the EPS and aa thermometer							
Sensor	EPS Temperature	Thermometer Temperature	Error	Passing Criteria	Pass / Fail		
FRONT_TOP				Error < 2°C			
MPPT-A				Error < 2°C			

#### 3.3.3.3 Test Notes

Delete me if no notes are required



