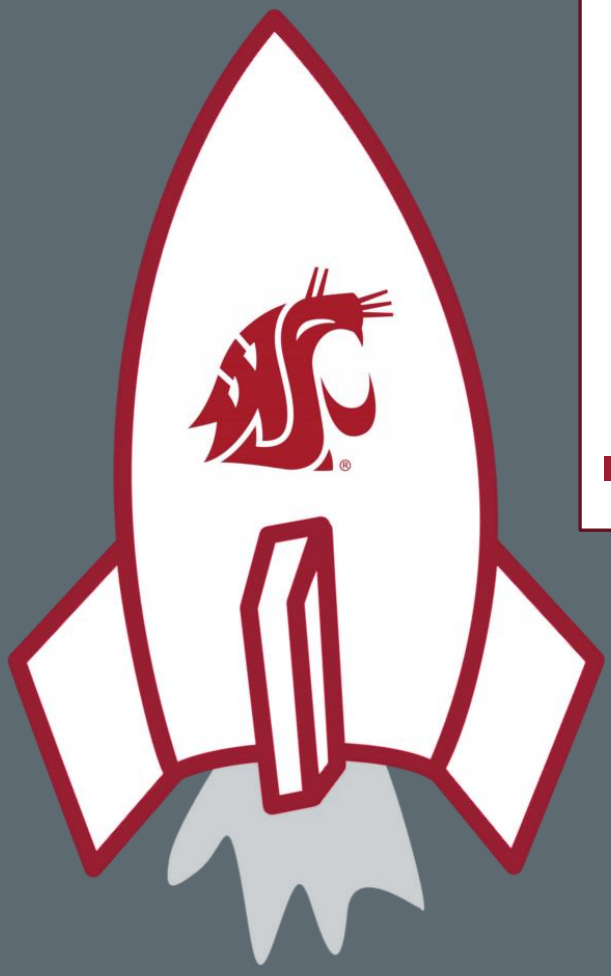
This document explains the function of the Solar Panel, its schematic level design, and its board level design

# Solar Panel

Solar Panel Design

Revision: 2.1.8



Hendrik Melse

# Table of Contents

# 1 Introduction

This document explains how the solar panel will fulfill the following Functions and conform to the following Requirements. This document refers to the Solar Panel version 2.1.

## 1.1 Functions

The Solar Panel is responsible for the following:

- Harvest energy from the sun
- Providing power to charge the batteries located on the EPS

## 1.2 Requirements

The system requirements and EPS design requirements can be found here.

# 2 Detailed Description

This section references the Solar Panel schematic[1]. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

## 2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

### 2.1.1 Energy Collection

Energy is captured from the sun by the photovoltaic (PV) cells. There are two cells on each panel. Each PV cell is connected to its own battery charger with MPPT[2].

### 2.1.2 Power Output

Power is output via two $4.1V$ rails from the battery chargers.

### 2.1.3 Analog-to-Digital Converter

The ADC allows the power management IC (PMIC) to monitor temperature and power at various locations on the board. Sensor locations are indicated on the block diagram.

### 2.1.4 Magnetorquer

The magnetorquer is controlled by the Attitude and Determination Control Subsystem (ADCS).

### 2.1.5 Connector

The connector connects the solar panel to the EPS and the ADCS to the magnetorquer. Each connector also has an I2C bus for communication with the ADCs.

## 2.2 Schematic

### 2.2.1 Isolated Grounds

The four isolated grounds are found on page 2 (D2) of the schematic. Power ground *(PGND)* is connected to pins 6 and 7 of the connector. All other grounds are shorted to *PGND* with a $0\Omega$ resistor rated for up to $2A$. Digital ground *(DGND)* is connected to the digital components of the board. Analog ground *(AGND)* is connected to the analog components, including the ADC, its voltage reference, and the thermistors. Chassis ground *(CHASSIS)* is connected to the conductive mechanical components of the board, including the bolt holes.

[1] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-PowerBoard/Documentation/SolarPanel.pdf

[2] Maximum Power Point Tracking adjusts the output voltage and current to maximize the energy harvested from the solar cells

### 2.2.2 Battery Charger

Page 2 of the schematic contains the battery chargers[3]. Each battery charger has a single $4.1V$ output, contains MPPT technology and a boost converter. The batteries are capable of charging at up to $4.2V$, but by charging at $4.1V$ the battery health can be preserved. The active low shutdown pin *(X_SHUT)* is pulled up to the PV output by $10k\Omega$ and $1k\Omega$ resistors in series. The output current limit is disabled, as each solar cell is incapable of generating more than about $330mA$. Output voltage and current are monitored by the ADC.

### 2.2.3 Analog-to-Digital Converter

Page 4 of the schematic contains the ADCs[4]. The ADCs have 8 inputs each, and there are two ADCs on each solar panel. The ADCs' address can be configured by selectively stuffing[5] the resistors connected to the address pins. Each pin can be set to either high, low, or left floating. Specific addresses can be found in the EPS design document. One ADC connects to the output connector to the EPS. This ADC measures current and voltage at the solar panel output and at the battery charger output. The other ADC is connected to the ADCS and measures the photodiode and the temperature at 7 different locations around the board, including the temperature of both battery chargers.

### 2.2.4 Photodiode

The photodiode[6] can be found on page 3 (A4) of the schematic. There is one per solar panel, and it is placed in the center of the board facing outward. This particular photodiode has a spectral sensitivity of $0.17\ A/W$ and the expected intensity is $1353\ W/m^2$ over a $2.56x2.56\ mm$ sensitive area. This makes the expected current $1.5mA$, so a $1.33k\Omega$ resistor will correspond to a maximum voltage of about $2.0V$.

### 2.2.5 Thermistors

Each solar panel contains 7 thermistors[7]. Two monitor the temperature of the battery chargers, while five monitor the temperature of the satellite in various locations on the solar panel. The thermistors use a $10k\Omega$ voltage divider sourced from *AVREF*.

### 2.2.6 Magnetorquer

The magnetorquer can be found on page 3 (C5) of the schematic. The magnetorquer is directly connected to pins 8 and 9 on the connector. These will go directly to the ADCS. The magnetorquer shall only be installed on the +Z, -Y, and -X boards, as only three axes are necessary to control the orientation of the satellite.

---

[3] CIS PN: 60-0001
[4] CIS PN: 27-0003
[5] Stuffing refers to populating a component during assembly
[6] CIS PN: 66-0003
[7] CIS PN: 26-0004

### 2.2.7 Voltage Reference

The voltage reference is generated by the ADCs at $2.5V$. This voltage is buffered and used as the source for the thermistors. Each ADC generates its own reference voltage for its own thermistors.

## 2.3 Board

The board shall be $1.0mm$ double layered with $1oz$ copper and ENIG finish.

### 2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters specified below. Signals in the following subsections do not include their sense signals unless specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

| | |
|---|---|
| Trace width: | $0.2mm$ |
| Vias: | $\emptyset 0.3mm$, unlimited count |
| Separation: | $0.2mm$ |
| Length: | unlimited |

Devices with specific placement and Routing considerations are called out in the schematic, see "CAD Note"

#### *2.3.1.1 I²C - I2C_[SDA, SCL]*

| | |
|---|---|
| Length: | Each node shall be length matched $\pm 1.0mm$ |
| Stubs: | $< 10.0mm$ |

#### *2.3.1.2 Solar Panel Outputs - PV_IIN_P-[A:B], PV_IIN_P-[A:B], PGND*

PGND applies between the solar panel and the output connector

Trace width: $0.6mm$

#### *2.3.1.3 MPPT Inputs - MPPT_LX-[A:B], PGND*

PGND applies between the battery charger and the output connector. This includes the input capacitors.

Trace Width: $0.6mm$

#### *2.3.1.4 Power Outputs - MPPT_ VOUT-[A:B], VOUT-[A:B], PGND*

PGND applies between the battery charger and the output connector. This includes the output capacitors.

Trace width: $0.6mm$

#### *2.3.1.5 Magnetorquer Inputs - MAGNETORQUER_[P, N]*

Trace width: $0.6mm$

# 3 Testing

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test. All tests shall be performed prior to attaching the solar cells to the solar panel.

- Waveforms shall be captured whenever appropriate.
- Have the event take fill the screen (for fast events, zoom in, for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-PowerBoard/Testing/SolarPanel.2.1

Common test instructions can be found on the wiki.

## 3.1 Before First Power-On Check

**Test Configuration:**

This test is required to be executed before batteries are attached and before any external power is applied to the Solar Panel.

### 3.1.1 Test Instructions

Measure the resistance of various points in reference to PGND located at the output connector.

### 3.1.2 Test Data

| Node | Resistance | | Node | Resistance |
|---|---|---|---|---|
| I2C_SDA_PMIC | | | VOUT-A | |
| I2C_SCL_PMIC | | | VOUT-B | |
| I2C_SDA_ADCS | | | AVDD | |
| I2C_SCL_ADCS | | | AVREF | |
| PV_IIN_P-A | | | 3.3V | |
| PV_IIN_P-B | | | | |

## 3.2 Battery Chargers

**Result:**
**Test Configuration:**

This test evaluates the Battery Charger.

### 3.2.1 Output Voltage

#### *3.2.1.1 Test Instructions*

Attach a battery charged to $3.7V$ to the output. Apply $2.5V$ at the solar cell output and wait until the current into the battery drops below $100mA$. Measure the final battery voltage. Adjust the voltage divider (R109, R105, R120, R126) as necessary.

#### *3.2.1.2 Test Data*

| Apply $2.5V$ to PV_IIN_P-A and measure the final battery voltage on VOUT-A. | | |
|---|---|---|
| Measured Voltage VOUT-A | Passing Criteria | Pass / Fail |
| | $4.0\,V < V < 4.2V$ | |

| Apply $2.5V$ to PV_IIN_P-B and measure the final battery voltage on VOUT-B. | | |
|---|---|---|
| Measured Voltage VOUT-B | Passing Criteria | Pass / Fail |
| | $4.0V < V < 4.2V$ | |

#### *3.2.1.3 Test Notes*

Delete me if no notes are required

### 3.2.2 Output Efficiency

#### *3.2.2.1 Test Instructions*

Apply $2.5V$ at the solar cell outputs. Attach a battery charged to $3.3V$. Measure the efficiency of the Battery Chargers at battery voltage increments of $0.1V$ from $3.3V$ to $4.1V$.

Note: $Efficiency = \frac{P_{out}}{P_{in}}$, measure the power into the input shunt resistor and out the output current shunt resistor.

#### *3.2.2.2 Test Data*

| Measure the efficiency of Battery Charger A at outputs from $3.3V$ to $4.1V$. | | |
|---|---|---|
| Attach a graph of the data | Passing Criteria | Pass / Fail |
| | $Efficiency > 85\%$ | |

#### *3.2.2.3 Test Notes*

Delete me if no notes are required

## 3.3 ADC

**Result:**

**Test Configuration:**

### 3.3.1 Current Monitoring

#### *3.3.1.1 Test Instructions*

Connect the EPS to the Solar Panel with a cable connecting only I2C, GND, and 3.3V. Apply $2.5V$ to the solar panel outputs before executing this test. Attach a battery to the output and compare the measured voltages across the shunt resistor from the EPS and a DMM.

Note: $Error = \frac{|I_{EPS} - I_{DMM}|}{I_{DMM}}$

#### *3.3.1.2 Test Data*

| Apply $2.5V$ at the solar panel output and measure the voltage across the shunt resistor. | | | | | |
|---|---|---|---|---|---|
| Signal | EPS voltage | DMM voltage | Error | Passing Criteria | Pass / Fail |
| VOUT-A | | | | $Error < 1.0\%$ | |

#### *3.3.1.3 Test Notes*

Delete me if no notes are required

### 3.3.2 Voltage Monitoring

#### *3.3.2.1 Test Instructions*

Connect the EPS to the Solar Panel with a cable connecting only I2C, GND, and 3.3V. Charge or discharge the batteries to $3.7V$, and apply $2.5V$ to the solar panel outputs before executing this test. Apply a $40mA$ resistive load to the solar panel output and compare the output voltages measured by the EPS and a DMM.

Note: $Error = \frac{|V_{EPS} - V_{DMM}|}{V_{DMM}}$

#### *3.3.2.2 Test Data*

| Apply a $40mA$ resistive load to VOUT-A and measure the voltage at various signals. | | | | | |
|---|---|---|---|---|---|
| Signal | EPS Voltage | DMM Voltage | Error | Passing Criteria | Pass / Fail |
| VOUT-A | | | | $Error < 1.0\%$ | |
| VOUT-B | | | | $Error < 1.0\%$ | |

#### *3.3.2.3 Test Notes*

Delete me if no notes are required

### 3.3.3 Temperature Monitoring

#### *3.3.3.1 Test Instructions*

Connect the EPS to the Solar Panel and charge or discharge the batteries to $3.7V$ before executing this test. Compare the temperature measured by the EPS and a thermometer at the following thermistors:

- FRONT_TOP
- MPPT-A

Note: $Error = |T_{EPS} - T_{Thermometer}|$

#### *3.3.3.2 Test Data*

| Compare the temperature measured by the EPS and a thermometer | | | | | |
|---|---|---|---|---|---|
| Sensor | EPS Temperature | Thermometer Temperature | Error | Passing Criteria | Pass / Fail |
| TEMP_BACK | | | | $Error < 2°C$ | |
| MPPT-A | | | | $Error < 2°C$ | |

#### *3.3.3.3 Test Notes:*

Delete me if no notes are required

## 3.4 Photodiode

**Result:**
**Configuration:**

### 3.4.1 Output Voltage

#### *3.4.1.1 Test Instructions:*

Measure the photodiode amplifier output with the photodiode covered by an opaque material. Remove the cover, and slowly bring a bright light closer to the photodiode sensor. Verify that the output voltage increases smoothly.

#### *3.4.1.2 Test Data*

| Verify that the photodiode acts as expected | | | |
|---|---|---|---|
| Light Position | Output | Passing Criteria | Pass / Fail |
| No Light | | $V < 0.2V$ | |
| Moving Closer | | $Voltage\ Increases\ Smoothly$ | |
| As Close as Possible | | $V > 1.5V$ | |

#### *3.4.1.3 Test Notes*

Delete me if no notes are required

## 3.5 Solar Cell

**Result:**
**Test configuration:**

### 3.5.1 Output Voltage Under Solar Power

#### *3.5.1.1 Test Instructions*

Perform solar cell tests only after all other tests have been completed. Attach one solar cell to the solar panel. Measure the output voltage under no load using both the grow lamp and the sun on a clear day at or near, solar noon.

#### 3.5.1.2 Test Data

| Measure the output voltage under no load | | | |
|---|---|---|---|
| Test Condition | Output Voltage | Passing Criteria | Pass / Fail |
| Grow Lamp | | $4.0V < V < 4.2V$ | |
| Sun | | $4.0V < V < 4.2V$ | |

#### 3.5.1.3 Test Notes

Delete me if no notes are required

### 3.5.2 Output Power

#### 3.5.2.1 Test Instructions

Attach a battery to the power output. Measure the power input into the battery using the grow lamp and the sun on a clear day at, or near, solar noon.

#### 3.5.2.2 Test Data

| Measure the output power into a battery | | | |
|---|---|---|---|
| Test Condition | Output Power | Passing Criteria | Pass / Fail |
| Grow Lamp | | $P > 0mW$ | |
| Sun | | $P > 250mW$ | |

#### 3.5.2.3 Test Notes

Delete me if no notes are required