



This document explains the function of the Comms, its schematic level design, its board level design, and its functional testing

Comms

In-Orbit Communication

Subsystem Design

Revision: 1.1.1

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Table of Contents

| | | |
|--------|--|----|
| 1 | Introduction | 5 |
| 1.1 | Function | 5 |
| 1.2 | Requirements | 5 |
| 1.3 | Open Systems Interconnection (OSI) Model | 5 |
| 1.3.1 | Layers | 5 |
| 1.3.2 | CougSat Communication Subsystem | 6 |
| 1.4 | Link Budget | 6 |
| 2 | Detailed Description | 7 |
| 2.1 | Functional Block Diagram | 7 |
| 2.1.1 | Comms μ Controller | 7 |
| 2.1.2 | RF Clock Generators | 7 |
| 2.1.3 | 700mm Receiver Radio | 7 |
| 2.1.4 | 700mm Transmitter Radio | 7 |
| 2.1.5 | 230mm Transmitter Radio | 8 |
| 2.1.6 | 5V Boost Converter | 8 |
| 2.2 | Schematic | 8 |
| 2.2.1 | Isolated Grounds | 8 |
| 2.2.2 | Power Rails | 8 |
| 2.2.3 | Comms μ Controller | 8 |
| 2.2.4 | I ² C Bus | 9 |
| 2.2.5 | SPI Bus | 9 |
| 2.2.6 | Current Monitoring | 10 |
| 2.2.7 | Voltage Monitoring | 10 |
| 2.2.8 | Temperature Monitoring | 10 |
| 2.2.9 | Analog Voltage Supply | 10 |
| 2.2.10 | 5.0V Regulation | 10 |
| 2.2.11 | Low Drop-Out Regulators | 11 |
| 2.2.12 | RF Clock Generators | 11 |
| 2.2.13 | DACs | 11 |
| 2.2.14 | RF Modulators | 11 |

| | | |
|--------|---|----|
| 2.2.15 | RF Demodulator | 12 |
| 2.2.16 | Low Noise Amplifier / Pre-Amplifiers..... | 12 |
| 2.2.17 | 230mm Power Amplifier | 12 |
| 2.2.18 | 700mm Power Amplifier | 12 |
| 2.2.19 | Mechanical Features | 13 |
| 2.3 | Board | 13 |
| 2.3.1 | Layer Stack-Up | 13 |
| 2.3.2 | Layout Constraints | 13 |
| 3 | Testing..... | 16 |
| 3.1 | Before First Power-On Check..... | 16 |
| 3.1.1 | Test Instructions..... | 16 |
| 3.1.2 | Test Data | 16 |
| 3.2 | Power Rail Switching..... | 16 |
| 3.2.1 | Test Instructions..... | 17 |
| 3.2.2 | Test Data | 17 |
| 3.2.3 | Test Notes | 17 |
| 3.3 | I ² C Bus | 17 |
| 3.3.1 | Test Instructions..... | 17 |
| 3.3.2 | Test Data | 17 |
| 3.4 | SPI Flash | 17 |
| 3.4.1 | Test Instructions..... | 18 |
| 3.4.2 | Test Data | 18 |
| 3.4.3 | Test Notes | 18 |
| 3.5 | Current Monitoring..... | 18 |
| 3.5.1 | Test Instructions..... | 18 |
| 3.5.2 | Test Data | 18 |
| 3.5.3 | Test Notes | 18 |
| 3.6 | Voltage Monitoring..... | 18 |
| 3.6.1 | Test Instructions..... | 19 |
| 3.6.2 | Test Data | 19 |
| 3.6.3 | Test Notes | 19 |
| 3.7 | Temperature Monitoring | 19 |

| | | |
|--------|---------------------------------|----|
| 3.7.1 | Test Instructions..... | 19 |
| 3.7.2 | Test Data | 19 |
| 3.7.3 | Test Notes | 19 |
| 3.8 | Analog Voltage Reference..... | 19 |
| 3.8.1 | Voltage | 20 |
| 3.8.2 | Ripple and Noise | 20 |
| 3.9 | µController Programming | 21 |
| 3.9.1 | Test Instructions..... | 21 |
| 3.9.2 | Test Data | 21 |
| 3.9.3 | Test Notes | 21 |
| 3.10 | 5.0V and 9.0V Regulator | 21 |
| 3.10.1 | Output Voltage..... | 21 |
| 3.10.2 | Output Ripple and Noise..... | 22 |
| 3.10.3 | Output Efficiency..... | 22 |
| 3.10.4 | Current Limit | 23 |
| 3.10.5 | Load Response | 24 |
| 3.11 | Low Drop-Out Regulators | 25 |
| 3.11.1 | Output Voltage..... | 25 |
| 3.11.2 | Output Ripple and Noise..... | 26 |
| 3.12 | RF Clock Generators..... | 26 |
| 3.12.1 | Reference Clock Supply..... | 26 |
| 3.12.2 | Reference Clock Frequency..... | 27 |
| 3.12.3 | Output Frequency | 27 |
| 3.13 | Differential Drivers..... | 28 |
| 3.13.1 | Test Instructions..... | 28 |
| 3.13.2 | Test Data | 28 |
| 3.14 | RF Chain – 230mm Downlink | 28 |
| 3.14.1 | Test Instructions..... | 28 |
| 3.14.2 | Test Data | 29 |
| 3.14.3 | Test Notes | 29 |
| 3.15 | RF Chain – 700mm Downlink | 29 |
| 3.15.1 | Isolation Switch | 29 |

| | | |
|--------|-------------------------------|----|
| 3.15.2 | Digital Modulation | 30 |
| 3.15.3 | Analog Modulation | 30 |
| 3.16 | RF Chain – 700mm Uplink | 31 |
| 3.16.1 | Test Instructions..... | 31 |
| 3.16.2 | Test Data | 31 |
| 3.16.3 | Test Notes | 32 |

1 Introduction

This document explains how the Comms will fulfil the following Functions and conform to the following Requirements. This document refers to the Comms version 1.1, +X Panel version 1.0, and -Z Panel version 1.0.

1.1 Function

The In-Orbit Communication Subsystem (Comms) is responsible for the following:

- Transferring telemetry to the ground station
- Transferring payload data to the ground station
- Transferring commands from the ground station
- Transmitting a locating beacon

1.2 Requirements

The system requirements and Comms design requirements can be found [on GitHub](#).

1.3 Open Systems Interconnection (OSI) Model

The OSI model¹ is a conceptual model that can be applied to any communication system. It has eight layers; each layer serves the layer above it and is served by the layer below it.

1.3.1 Layers

| Layer | | | Protocol Data Unit | Function |
|--------------|---|--------------|--------------------|--|
| Host layers | 7 | Application | Data | High-level APIs |
| | 6 | Presentation | | Translation of data between a networking service and an application |
| | 5 | Session | | Managing communication sessions |
| | 4 | Transport | Segment | Reliable transmission of data segments between points on a network |
| Media layers | 3 | Network | Packet | Structuring and managing a multi-node network |
| | 2 | Data link | Frame | Reliable transmission of data frames between two nodes connected by a physical layer |
| | 1 | Physical | Symbol | Transmission and reception of raw bit streams over a physical medium |
| | 0 | Medium | Electrons, Photons | The physical medium: copper, fiber, wireless |

¹For more information, read [Wikipedia's article](#) on the OSI model

1.3.2 CougSat Communication Subsystem

The communication subsystem, formed from the in-orbit and ground subsystems, fulfills layers 0 through 4 of the OSI model. The Comms serves the Command and Data Handling (C&DH) subsystem which fulfills layers 5 and up. The Ground serves itself for layers 5 and up which results in a graphical representation of the exchanged information. The in-orbit and ground subsystems are very similar as they are required to be compatible. For details on the ground subsystem, see its [design document](#).

The hardware described here translates baseband signals generated by the Comms μ Controller into RF signals and vice versa. The translation of the baseband signals to digital data happens in the Comms μ Controller.

For more information on how each layer is structured see [CougSatNet](#) from a software perspective and details on the RF modulation techniques.

1.3.2.1 Layer 0

The communication subsystem is using wireless transmission, in the radio frequency band. There are two bands utilized: 700mm and 230mm. The 700mm radio is the primary radio used for telemetry and beacon. The 230mm radio is the secondary radio used for payload data transfers and only operates in downlink mode.

1.3.2.2 Layer 1

The modulation scheme used is Quadrature Phase Shift Keying (QPSK)². Each symbol is a change in the phase constant of the RF wave. The radios are software defined radios which allows reconfiguration of this layer if necessary. Other modulation schemes can be developed if the hardware supports it.

1.3.2.3 Layer 2 and Up

See [CougSatNet](#).

1.4 Link Budget

A [link budget](#) for downlink and uplink was tabulated indicating a transmit power of 1W is sufficient for up to 500kbps on the 230mm band. The 700mm band transmitter will incur less losses³ and send slower data⁴ but has a low gain antenna so 1W is also sufficient. Uplink has no problems thanks to access to high gain and high-power transmitters on the ground.

² For more information, read [Wikipedia's article](#) on Phase Shift Keying (PSK)

³ [Free-space path loss](#) is proportional to frequency squared

⁴ A slower data rate has looser requirements for signal-to-noise ratio because there is more time to decode the symbol

2 Detailed Description

This section references the Comms [schematic](#). Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Comms μ Controller

The Comms μ Controller is responsible for interfacing the radio signals and the Command and Data Handling subsystem⁵. This fulfills OSI model⁶ layers 1 through 4. It samples and synthesizes the baseband signals which are mixed with the carrier wave. This constitutes a software defined radio. The μ Controller has non-volatile storage in the form of SPI Flash to store configurations and reference waveforms.

2.1.2 RF Clock Generators

Each radio has a configurable clock generator used to synthesize the carrier waves. For the transmission of the beacon, the generator is the direct source without any modulation to the antenna⁷.

2.1.3 700mm Receiver Radio

Its RF diagram is the top row on page 2. The RF signal from the antenna is connected to the receiver radio via a high isolation RF switch. This switch prevents the transmitter from overdriving the sensitive receiver components and inducing damage. The signal is then amplified by low noise amplifiers which add very little noise to the signal to maintain the highest signal to noise ratio. The signal is then connected to the demodulator which removes the carrier frequency and splits that baseband signal into its in-phase and quadrature signals which are then sampled by the Comms μ Controller and demodulated into digital data. The receiver radio is designed for continuous operation and low power⁸.

2.1.4 700mm Transmitter Radio

Its RF diagram is the middle row on page 2. The Comms μ Controller generates in-phase and quadrature baseband signals using a digital to analog converter. This allows arbitrary waveform including voice signals⁹. These signals feed the modulator which puts the baseband signals on the carrier wave. This modulated RF gets amplified with a power amplifier to transmit the desired 1W, see the Link Budget.

⁵ Requirements COMMS-008, COMMS-009

⁶ Open Systems Interconnection (OSI) Model

⁷ Requirements COMMS-001

⁸ Requirement COMMS-005

⁹ Requirement COMMS-006

2.1.5 230mm Transmitter Radio

Its RF diagram is the bottom row on page 2. The Comms μ Controller generates in-phase and quadrature baseband signals a digital to analog converter. This allows arbitrary waveform required by multilevel modulation such as 16QAM. These signals feed the modulator which puts the baseband signals on the carrier wave. This modulated RF gets amplified with a power amplifier to transmit the desired 1W, see the Link Budget.

2.1.6 5V Boost Converter

The RF chains require a 5V supply which come from boost converters. The converters are sourced from the battery rail.

2.2 Schematic

2.2.1 Isolated Grounds

On page 3 of the schematic (D1 & D2), are the six isolated grounds found on the Comms. Power ground (*PGND*) is directly connected to the backplane and the boost converters. Most of the other grounds are shorted to *DGND* using a 0Ω resistor rated up to 2A, the expected current is less than 500mA each. Digital ground (*DGND*) connects to the digital circuitry including the Comms μ Controller and connects to *PGND*. Analog ground (*AGND*) connects to analog circuits including the ADCs, the voltage references, the thermistors, and the operational amplifiers. *AGND* connects to *DGND*. Chassis ground (*CHASSIS*) is connected to the Mechanical Features including bolt holes and the card rails. The 230mm RF chain and the 700 RF chains each have their own RF grounds (*RFGND-0* and *RFGND-1*, respectively). The layout preserves proper grounding techniques.

2.2.2 Power Rails

Page 3 of the schematic illustrates all the power rails on the Comms. Each RF chain can be turned off to save power and as a radio inhibit¹⁰.

2.2.3 Comms μ Controller

The Comms μ Controller (page 4) is a microcontroller from the STM32 low power family¹¹. It was chosen for its ease of programming, and low power consumption. It needed fast ADCs for sampling, large amounts of RAM for storing buffers, and a fast CPU for modulation/demodulation math.

2.2.3.1 Programming Connections

During testing, the Comms μ Controller is programmed via Serial Wire Debug¹² (SWD, page 4, A1). The process of programming is made simple with just a single six pin header and a robust software utility. In orbit, the μ Controller can be programmed via JTAG¹³. The [In-Flight JTAG Reprogrammer](#) (IFJR) connects via the

¹⁰ Requirement REQ-005

¹¹ CIS PN: [61-0003](#)

¹² For more information, see [ARM's article](#) on SWD

¹³ For more information, see [Wikipedia's article](#) on JTAG

backplane, through tri-state buffers/logic level converters¹⁴ (page 5, C3:D3). The IFJR can enable or disable the tri-state buffer which essentially disconnects the JTAG interface from the Comms μ Controller (it outputs high impedance), allowing the SWD to program. The logic level conversion feature is not used.

2.2.4 I²C Bus

The Comms μ Controller has one I²C bus (page 4, C4). It connects to the monitoring ADCs.

2.2.4.1 ADCs

There are 3 ADCs¹⁵ connected to the Comms μ Controller, each with 8 single-ended inputs. The ADC was chosen for its low power, SAR architecture, small package, and up to 27 addresses. The list of address (7b) follow:

- [0x2B] ADC-0 (page 6, A2), temperature
- [0x2F] ADC-1 (page 6, A5), temperature
- [0x2A] ADC-2 (page 6, C2), voltage and current

The two voltage sensing inputs have voltage dividers (page 6, C1) that reduces the voltage of every input to place their level within the sensing range of 0 to 2.5V. Using paired resistors helps match the gain across temperature.

2.2.5 SPI Bus

The Comms μ Controller has two SPI buses¹⁶. One connects to the C&DH to transfer packets and telemetry. One connects to the RF Clock Generators, and SPI Flash.

2.2.5.1 Backplane to the C&DH

The Comms μ Controller is a slave to the C&DH, see the [interface document](#) for details. Tri-state buffers isolate the bus when Comms is off as to not disturb the backplane side.

2.2.5.2 RF Clock Generators

The Comms μ Controller is a transmit only master to the RF Clock Generators. Each generator has tri-state buffers which only connects the bus if the generator's rail is on. Without this, when the generator is turned off, its ESD diodes would prevent the bus from moving above *GND* effectively disabling the bus.

The Comms μ Controller is a master to two SPI Flash chips¹⁷ (page 4, A5:B6) that provides 16Mb of mirrored storage or 32Mb of striped storage.

¹⁴ CIS PN: [09-0001](#)

¹⁵ CIS PN: [27-0003](#)

¹⁶ For more information, see [Wikipedia's article](#) on SPI

¹⁷ CIS PN: [29-0002](#)

2.2.6 Current Monitoring

At various locations, the power chain has shunt resistors connected to ADCs in through a differential amplifier¹⁸ monitor the current. Those locations are:

- 5V Regulator output (page 7, C2)
- Each RF chain input (page 8)

2.2.7 Voltage Monitoring

The regulator output and PA output are measured using the ADCs. Those locations are:

- 5V Regulator output (page 6, B6)
- 700mm PA power output Regulator output (page 13, C2)

2.2.8 Temperature Monitoring

At various locations, the temperature is monitored using thermistors and the ADCs. Those locations are:

- 5V Regulator (page 7, A3)
- Comms μ Controller (page 4, B3)
- RF clock generators (page 9, A4; page 10, A4; page 11, A4)
- DACs (page 9, D4; page 10, D4)
- 230mm downlink RF chain (page 12, B3, & C3)
- 700mm downlink RF chain (page 13, B3, & C3)
- 700mm uplink RF chain (page 14, D4; page 15, C4)

2.2.9 Analog Voltage Supply

The Comms has an analog voltage supply (page 6, C5) which is fed by the 3.3V rail filtered with a ferrite bead and capacitors. Precision is not required as all ADCs use the precision voltage reference for calibration. This is the source for the Temperature Monitoring thermistors and operational amplifiers.

2.2.10 5.0V Regulation

The 5.0V regulator (page 7) is switching mode, boost topology. The converter¹⁹ automatically senses the output voltage and adjusts the switching parameters to keep the output at 5.0V. The converter has an integrated switching MOSFET. The converter was chosen for its small size and high efficiency.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

¹⁸ CIS PN: [08-0004](#)

¹⁹ CIS PN: [65-0005](#)

The converter and inductor (page 7, B2:B3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

2.2.11 Low Drop-Out Regulators

The sensitive RF components are supplied through low drop-out (LDO) regulators²⁰ (page 8, A3, B3, & D3). These are linear regulators that require a small drop-out²¹ for proper regulation. They are used to reject the switching noise from the switching mode power supplies.

2.2.12 RF Clock Generators

The RF Clock Generators²² (page 9, A4; page 10, A4; page 11, A4) have a voltage-controlled oscillator and a phase-locked loop to take a reference clock and synthesize a RF wave. The reference clocks²³ (page 9, A3; page 10, A3; page 11, A3) have high frequency stability and are supplied with ferrite beads to further increase frequency stability. The supporting circuitry for the generators was created using Analog Device's [ADIsimPLL](#). The design files can be found under the [documentation folder](#). The output of the generators is designed to drive a 50 Ω load.

The 700mm Receiver Radio's demodulator divides its clock input by two, so the RF clock generator needs to output double the carrier frequency.

2.2.13 DACs

The Comms μ Controller outputs a parallel bus for the DACs²⁴ which feeds the RF Modulators. The DACs have a built-in interpolation filter to reduce high frequency spurs from the input signal.

The DACs output a current source of magnitude $2mA$, set by $FSADJ$ resistors to GND , differentially. Each modulator has a differential voltage and common mode voltage for these baseband signals which is set by the output resistors to GND and between the differential pair. This circuit was simulated in [LTSpice](#) and can be found under [electrical design](#). Precision resistors are used to reduce any common mode offset or gain imbalance. A capacitor in this output creates a low pass filter to help with bandwidth limiting.

2.2.14 RF Modulators

The 700mm Transmitter Radio's modulator²⁵ (page 13, A3) and the 230mm Transmitter Radio's modulator²⁶ (page 12, A3) have the RF Clock Generators AC coupled into their local oscillator input, and the DACs are directly connected to the baseband inputs. The RF output is AC coupled to the next element in the RF

²⁰ CIS PN: [60-0009](#)

²¹ Voltage difference between input and output

²² CIS PN: [65-0005](#)

²³ CIS PN: [42-206B](#)

²⁴ CIS PN: [27-0006](#)

²⁵ CIS PN: [65-0002](#)

²⁶ CIS PN: [65-0003](#)

chain. Output filters bandpass around the carrier to reduce unwanted spurs from being amplified.

2.2.15 RF Demodulator

The 700mm Receiver Radio's demodulator²⁷ (page 15, B3:B4) has the RF Clock Generators AC coupled into its local oscillator input. The 60.4Ω termination resistor is used to match a 50Ω input into the demodulator. The RF signal is connected to the modulator's input through a 1:4 balun (page 13, B2) to match a 50Ω input into the demodulator's 200Ω . The gain of the demodulator is set by a DAC output of the Comms μ Controller.

The demodulator outputs differential baseband signals $1.0V \pm 500mV$. this amplified and translated to $1.65V \pm 1V$ single ended for input to the Comms μ Controller's ADC by op-amps²⁸ (page 11, C1:D3). This circuit was simulated in LTSpice and can be found under [electrical design](#).

2.2.16 Low Noise Amplifier / Pre-Amplifiers

The low noise amplifiers (LNA)²⁹ (page 13, A5; page 14, B2, B5, & C3) amplify the RF signal for the next component in the RF chain. They were chosen for their low noise figure, broadband response, and high gain. For the 700mm Receiver Radio's LNAs, the bias voltage can be shorted to ground which disables the amplifier. This is required, along with toggling the RF switch, when transmitting on 700mm to not damage the demodulator. The output is biased via a ferrite bead to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the next component.

The 230mm pre-amplifier³⁰ (page 12, A5) has an internal two stage amplifier to achieve very gain with an output sufficient to drive the 230mm Power Amplifier.

2.2.17 230mm Power Amplifier

The 230mm power amplifier³¹ (page 12, C3) is the final amplifiers for the RF signal. It drives the antennas and output the desired $1W$, see the Link Budget. It was chosen for the output power, high efficiency, and appropriate frequency band. The output is biased via an inductor to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the antenna.

2.2.18 700mm Power Amplifier

The 700mm power amplifier³² (page 13, C3) is the final amplifiers for the RF signal. It drives the antennas and output the desired $1W$, see the Link Budget. It was chosen for the output power, high efficiency, and appropriate frequency

²⁷ CIS PN: [65-0004](#)

²⁸ CSI PN: [08-0002](#)

²⁹ CIS PN: [65-0008](#)

³⁰ CIS PN: [65-0013](#)

³¹ CIS PN: [65-0012](#)

³² CIS PN: [65-0011](#)

band. The output is biased via an inductor to provide power yet decouple the RF signal from the power supply. The output is AC coupled to feed into the antenna.

The amplifier has a power detector (page 13, C1) that is sampled by the Voltage Monitoring, to measure the power being sent to the antenna.

2.2.19 Mechanical Features

The 5V Boost Converter heatsink (page 6, D1) and RF chain heatsinks (page 12, D1; page 13, D1) mount directly to the Comms board using bolts. These holes are conductive and connected directly to *CHASSIS*, see Isolated Grounds. The Comms also slots into the structure using rails³³ which are also conductive and connected directly to *CHASSIS*. Each of the holes have a capacitor and resistor connecting to power ground which will absorb and dissipate transients.

2.3 Board

The board shall also conform to the dimensions specified by the [CougSat Module Standard](#).

2.3.1 Layer Stack-Up

The board shall be four layered with ENIG finish, see Figure 1. Only through vias shall be used. The external copper weight shall be $35\mu\text{m}$ and the internal copper weight shall be $18\mu\text{m}$.

| Layer | Thickness | Primary Function |
|------------|-------------------------|------------------------------------|
| 1 (top) | $35\mu\text{m}$ (1oz) | SMD components, RF & signal traces |
| Prepreg | $100\mu\text{m}$ | JLC2313: $\epsilon = 4.05$ |
| 2 | $18\mu\text{m}$ (0.5oz) | Ground planes |
| Core | $1265\mu\text{m}$ | |
| 3 | $18\mu\text{m}$ (0.5oz) | Power planes |
| Prepreg | $100\mu\text{m}$ | JLC2313: $\epsilon = 4.05$ |
| 4 (bottom) | $35\mu\text{m}$ (1oz) | Signal traces |

Figure 1: Stack-Up

2.3.2 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless otherwise specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

| | |
|--------------|--|
| Trace width: | 0.1mm |
| Vias: | $\varnothing 0.2\text{mm}$, unlimited count |
| Separation: | 0.1mm |
| Length: | unlimited |

Devices with specific placement and routing considerations are called out on the schematic, see "CAD Note:"

³³ See [backplane documentation](#) for details

2.3.2.1 All 50 Ω Impedance Traces

This applies to all RF traces except the demodulator's RF input. These traces shall be a coplanar waveguide with ground³⁴.

| | |
|--------------|----------|
| Trace width: | 0.22mm |
| Gap width: | 0.50mm |
| Vias: | none |
| Length: | minimize |

2.3.2.2 All 200 Ω Impedance Traces

This applies to the demodulator's RF input. These traces shall be an edge coupled microstrip³⁵ with differential impedance of 200 Ω . Ground located on second layer below (1.37mm substrate thickness).

| | |
|--------------|----------|
| Trace width: | 0.25mm |
| Gap width: | 0.60mm |
| Vias: | none |
| Length: | minimize |

2.3.2.3 All Differential Signals / Parallel Bus

This applies to the modulators' inputs. Single ended to/from differential shall occur as close to the single ended side as possible.

| | |
|--------------|--------------------------|
| Trace width: | 0.16mm |
| Gap width: | 0.16mm |
| Length: | Length match $\pm 1.0mm$ |
| Vias: | minimize |

2.3.2.4 Regulator Input - VBATT, PGND

This applies to *VBATT* and *PGND* between the backplane and the inputs to the regulators and their input capacitors.

| | |
|--------------|----------------------------------|
| Trace width: | 1.0mm (2.0mm on internal layers) |
|--------------|----------------------------------|

2.3.2.5 Regulator Output - 5.0V, PGND

PGND applies to between the regulator, its output capacitors, and the backplane.

| | |
|--------------|----------------------------------|
| Trace width: | 0.5mm (1.0mm on internal layers) |
|--------------|----------------------------------|

2.3.2.6 Regulator Channels - 3.1V_[0:2], 5.0V_[0:1], PGND

PGND applies to between the regulator, their loads, and the backplane.

| | |
|--------------|----------------------------------|
| Trace width: | 0.5mm (1.0mm on internal layers) |
|--------------|----------------------------------|

2.3.2.7 SPI Buses - SPI_[SCK, MOSI, MISO, CS], COM_SPI_[SCK, MOSI, MISO, CS]

| | |
|---------|---|
| Length: | Each node shall be length matched $\pm 1.0mm$ |
| Stubs: | < 10.0mm |

³⁴ For more information, read [Microwaves101's article](#) on CPW

³⁵ For more information, see [Microwaves101's article](#) on microstrips

- 2.3.2.8 JTAG - JTAG_[TCK, TDI, TDO, TMS], BUS_JTAG-[TCK, TDI, TDO, TMS]
Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$
- 2.3.2.9 I²C - I2C_[SCL, SDA]
Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

3 Testing

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test³⁶.

- Waveforms shall be captured whenever appropriate
- Have the event take fill the screen (for fast events, zoom in; for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: <https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-PowerBoard/Testing/Comms.1.1>

Common test instructions can be found on the [wiki](#).

3.1 Before First Power-On Check

Test Configuration:

This test is required to be executed before any external power is applied to the Comms.

3.1.1 Test Instructions

Measure the resistance of various points in reference to *PGND* located at the backplane. This is informational only.

3.1.2 Test Data

| Node | Resistance | | Node | Resistance |
|-------------------|------------|--|-------------------|------------|
| VBATT | | | 3.3V | |
| 3.1V-0 | | | 3.1V-1 | |
| 3.1V-2 | | | 5.0V | |
| 5.0V-0 | | | 5.0V-1 | |
| I2C_SCL | | | I2C_SDA | |
| ANTENNA_230_COAX | | | ANTENNA_700_COAX | |
| MOD_LNA_230_RFOUT | | | MOD_LNA_700_RFOUT | |

3.2 Power Rail Switching

Results: Pass / Fail

Test Configuration:

³⁶ For test 3.1, place files in the subfolder "3.1" and so on

This test evaluates the circuit described in Power Rails.

3.2.1 Test Instructions

Hold the μ Controller in reset or program a blank image, verify the power rails are powered off. Have the μ Controller enable the power rail, verify the power rails are powered on, ensuring the rail turns on only with its control signal.

3.2.2 Test Data

| Hold the μ Controller in reset, measure the voltage of each power rail | | | |
|--|---------|------------------|-------------|
| Rail | Voltage | Passing Criteria | Pass / Fail |
| 3.1V-0 | | Voltage < 50mV | |
| 3.1V-1 | | Voltage < 50mV | |
| 3.1V-2 | | Voltage < 50mV | |
| 5.0V-0 | | Voltage < 50mV | |
| 5.0V-1 | | Voltage < 50mV | |

| Have the μ Controller enable the power rail, measure the voltage of each power rail. Ensure the rail turns on only with its control signal | | | | |
|--|----------------|---------|------------------|-------------|
| Rail | Control Signal | Voltage | Passing Criteria | Pass / Fail |
| 3.1V-0 | PC_3.1V-0 | | Voltage > 3V | |
| 3.1V-1 | PC_3.1V-1 | | Voltage > 3V | |
| 3.1V-2 | PC_3.1V-2 | | Voltage > 3V | |
| 5.0V-0 | PC_5.0V-0 | | Voltage > 4V | |
| 5.0V-1 | PC_5.0V-1 | | Voltage > 4V | |

3.2.3 Test Notes

Delete me if not required

3.3 I²C Bus

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in I²C Bus.

3.3.1 Test Instructions

At the pull up resistors of the I²C bus, validate signal integrity. The μ Controller should generate random I²C traffic on the bus.

3.3.2 Test Data

| At the pull up resistors of the I ² C bus, validate the following timing parameters | | |
|--|------------------|-------------|
| Capture the SDA and SCL lines | Passing Criteria | Pass / Fail |
| | Signal Integrity | Pass |

3.4 SPI Flash

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in SPI Bus.

3.4.1 Test Instructions

Perform write and read operations to the SPI Flash chips. Verify functionality.

3.4.2 Test Data

| Perform write and read operations to the SPI Flash chips. Verify functionality. | | | |
|---|-----------|------------------|-------------|
| Chip | Direction | Passing Criteria | Pass / Fail |
| A | Read | Functionality | |
| A | Write | Functionality | |
| B | Read | Functionality | |
| B | Write | Functionality | |

3.4.3 Test Notes

Delete me if not required

3.5 Current Monitoring

Results: Pass / Fail

This test evaluates the circuit described in Current Monitoring.

3.5.1 Test Instructions

Apply a 10mA to 250mA resistive load to a 5.0V-0. Compare the current measured by the Comms and a DMM.

Note: $Error = \frac{|I_{Comms} - I_{DMM}|}{I_{DMM}}$

3.5.2 Test Data

| Apply a 10mA to 250mA resistive load to a single output channel. Compare the current measured by the Comms and a DMM | | | | | |
|--|-------------|-------------|-------|------------------|-------------|
| Load | EPS Current | DMM Current | Error | Passing Criteria | Pass / Fail |
| 10mA | | | | $Error < 1.0\%$ | |
| 25mA | | | | $Error < 1.0\%$ | |
| 50mA | | | | $Error < 1.0\%$ | |
| 100mA | | | | $Error < 1.0\%$ | |
| 250mA | | | | $Error < 1.0\%$ | |

3.5.3 Test Notes

Delete me if not required

3.6 Voltage Monitoring

Results: Pass / Fail

This test evaluates the circuit described in Voltage Monitoring.

3.6.1 Test Instructions

Compare the voltage measured by the Comms and a DMM on the following signals:

- $\underline{L}3.3V-0N$
- $\underline{L}3.3V-1P$
- $5.0V$

Note: $Error = \frac{|V_{Comms} - V_{DMM}|}{V_{DMM}}$

3.6.2 Test Data

| Compare the voltage measured by the Comms and a DMM | | | | | |
|---|---------------|-------------|-------|------------------|-------------|
| Signal | Comms Voltage | DMM Voltage | Error | Passing Criteria | Pass / Fail |
| PA_PDET_700 | | | | $Error < 1.0\%$ | |
| $5.0V$ | | | | $Error < 1.0\%$ | |

3.6.3 Test Notes

Delete me if not required

3.7 Temperature Monitoring

Results: Pass / Fail

This test evaluates the circuit described in Temperature Monitoring.

3.7.1 Test Instructions

Compare the temperature measured by the Comms and a thermometer on the following temperature sensors:

- 5.0V Regulator
- μ Controller
- $+X+Y$

Note: $Error = |T_{Comms} - T_{THERMOMETER}|$

3.7.2 Test Data

| Compare the temperature measured by the Comms and a thermometer | | | | | |
|---|-------------------|-------------------------|-------|----------------------|-------------|
| Sensor | Comms Temperature | Thermometer Temperature | Error | Passing Criteria | Pass / Fail |
| 5.0V Regulator | | | | $Error < 2^{\circ}C$ | |
| μ Controller | | | | $Error < 2^{\circ}C$ | |

3.7.3 Test Notes

Delete me if not required

3.8 Analog Voltage Reference

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in Analog Voltage Supply. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources.

3.8.1 Voltage

3.8.1.1 Test Instructions

Measure the voltage of each analog reference.

Note: Measure the DC component with $PLC^{37} > 100$

3.8.1.2 Test Data

| Measure the voltage of the following signals | | | |
|--|---------|---------------------|-------------|
| Signal | Voltage | Passing Criteria | Pass / Fail |
| ADC_VREF-0 | | $2.49V < V < 2.51V$ | |
| ADC_VREF-1 | | $2.49V < V < 2.51V$ | |
| ADC_VREF-2 | | $2.49V < V < 2.51V$ | |
| AVREF-0 | | $2.48V < V < 2.52V$ | |
| AVREF-1 | | $2.48V < V < 2.52V$ | |
| DAC_REFIO-230 | | $1.14V < V < 1.26V$ | |
| DAC_REFIO-700 | | $1.14V < V < 1.26V$ | |

3.8.1.3 Test Notes

Delete me if not required

3.8.2 Ripple and Noise

3.8.2.1 Test Instructions

Measure the ripple and noise of each analog reference.

Note: Measure the RMS AC component with $3Hz < f$

3.8.2.2 Test Data

| Measure the RMS voltage ripple and noise of the following signals | | | |
|---|---------|------------------------|-------------|
| Signal | Voltage | Passing Criteria | Pass / Fail |
| ADC_VREF-0 | | $ V_{rms} < 250\mu V$ | |
| ADC_VREF-1 | | $ V_{rms} < 250\mu V$ | |
| ADC_VREF-2 | | $ V_{rms} < 250\mu V$ | |
| AVREF-0 | | $ V_{rms} < 2.5mV$ | |
| AVREF-1 | | $ V_{rms} < 2.5mV$ | |
| DAC_REFIO-230 | | $ V_{rms} < 1mV$ | |
| DAC_REFIO-700 | | $ V_{rms} < 1mV$ | |

3.8.2.3 Test Notes

Delete me if not required.

³⁷ Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

3.9 μ Controller Programming

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in Programming Connections.

3.9.1 Test Instructions

Connect a SWD programmer to the SWD header and upload an image, validate the μ Controller is properly programmed. Connect a JTAG programmer to the backplane and upload an image, validate the μ Controller is properly programmed.

Note: Follow the programming instructions on the [wiki](#).

3.9.2 Test Data

| Program the μ Controller via SWD and JTAG, validate the μ Controller is properly programmed | | |
|---|--------------------------------------|-------------|
| Programmer | Passing Criteria | Pass / Fail |
| SWD | μ Controller properly programmed | |
| JTAG | μ Controller properly programmed | |

3.9.3 Test Notes

Delete me if not required

3.10 5.0V and 9.0V Regulator

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in 5.0V Regulation. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources

3.10.1 Output Voltage

3.10.1.1 Test Instructions

Apply 3.7V to VBATT. Measure the voltage of the 5.0V regulator under no load and under a 500mA resistive load.

Note: Measure the DC component with $PLC^{38} > 100$

³⁸ Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

3.10.1.2 Test Data

| Measure the voltage of the 5.0V regulator under no load and under a 500mA resistive load | | | | |
|--|-----------------|--------------------|-------------------|-------------|
| Regulator | No Load Voltage | 500mA Load Voltage | Passing Criteria | Pass / Fail |
| 5.0V | | | $4.9V < V < 5.1V$ | |

3.10.1.3 Test Notes

Delete me if not required

3.10.2 Output Ripple and Noise

3.10.2.1 Test Instructions

Apply 3.7V to VBATT. Measure the ripple and noise of the 5.0V regulator whilst under a 500mA resistive load.

Note: Measure the RMS AC component with $3Hz < f$

3.10.2.2 Test Data

| Measure the ripple and noise of the 5.0V regulator whilst under a 500mA resistive load. | | | |
|---|------------------------------|--------------------|-------------|
| Regulator | Capture the ripple and noise | Passing Criteria | Pass / Fail |
| 5.0V | | $ V_{rms} < 25mV$ | Pass |

3.10.3 Output Efficiency

3.10.3.1 Test Instructions

Measure the efficiency of the 5.0V regulator whilst under a 10mA to 500mA resistive loads and with 3.3V to 4.1V input voltage on VBATT.

Note: $Efficiency = \frac{P_{out}}{P_{in}}$, measure the power across the input and output current shunt resistors.

3.10.3.2 Test Data - 5.0V

| Measure the efficiency of the 5.0V regulator whilst under a 10mA resistive load and 3.3V to 4.1V input voltage. | | | | | |
|---|----------|-----------|------------|---------------------|-------------|
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
| 3.3V | | | | $Efficiency > 50\%$ | |
| 3.7V | | | | $Efficiency > 50\%$ | |
| 4.1V | | | | $Efficiency > 50\%$ | |

| Measure the efficiency of the 5.0V regulator whilst under a 20mA resistive load and 3.3V to 4.1V input voltage. | | | | | |
|---|----------|-----------|------------|---------------------|-------------|
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
| 3.3V | | | | $Efficiency > 50\%$ | |
| 3.7V | | | | $Efficiency > 50\%$ | |
| 4.1V | | | | $Efficiency > 50\%$ | |

| Measure the efficiency of the 5.0V regulator whilst under a 50mA resistive load and 3.3V to 4.1V input voltage. | | | | | |
|---|----------|-----------|------------|----------------------------|-------------|
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
| 3.3V | | | | <i>Efficiency > 50%</i> | |
| 3.7V | | | | <i>Efficiency > 50%</i> | |
| 4.1V | | | | <i>Efficiency > 50%</i> | |

| Measure the efficiency of the 5.0V regulator whilst under a 100mA resistive load and 3.3V to 4.1V input voltage. | | | | | |
|--|----------|-----------|------------|----------------------------|-------------|
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
| 3.3V | | | | <i>Efficiency > 70%</i> | |
| 3.7V | | | | <i>Efficiency > 70%</i> | |
| 4.1V | | | | <i>Efficiency > 70%</i> | |

| Measure the efficiency of the 5.0V regulator whilst under a 200mA resistive load and 3.3V to 4.1V input voltage. | | | | | |
|--|----------|-----------|------------|----------------------------|-------------|
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
| 3.3V | | | | <i>Efficiency > 90%</i> | |
| 3.7V | | | | <i>Efficiency > 90%</i> | |
| 4.1V | | | | <i>Efficiency > 90%</i> | |

| Measure the efficiency of the 5.0V regulator whilst under a 500mA resistive load and 3.3V to 4.1V input voltage. | | | | | |
|--|----------|-----------|------------|----------------------------|-------------|
| Input Voltage | Power In | Power Out | Efficiency | Passing Criteria | Pass / Fail |
| 3.3V | | | | <i>Efficiency > 90%</i> | |
| 3.7V | | | | <i>Efficiency > 90%</i> | |
| 4.1V | | | | <i>Efficiency > 90%</i> | |

3.10.3.3 Efficiency Plot

Create a plot of current versus efficiency with each input voltage.

3.10.3.4 Test Notes

Delete me if not required

3.10.4 Current Limit

3.10.4.1 Test Instructions

Apply 3.7V to VBATT. Apply an increasing load to the 5.0V output until the current no longer increases. Measure voltage and current of the rail.

Note: The load will likely be increased by adding more resistors in parallel or decrease the load resistance.

3.10.4.2 Test Data

| Apply an increasing load to 3.3V outputs until the current no longer increases | | | |
|--|-------------|--------------------|-------------|
| <i>Regulator</i> | Max Current | Passing Criteria | Pass / Fail |
| 5.0V | | $500mA < I < 1.5A$ | |

3.10.4.3 Test Notes

Delete me if not required

3.10.5 Load Response

3.10.5.1 Test Instructions

Apply 3.7V to VBATT. Apply the following loads to the regulator output:

- No load to 500mA resistive load
- 500mA resistive load to no load
- No load to 10 μ F MLCC
- 500mA resistive load adding 10 μ F MLCC
- No load to short circuit
- Short circuit to no load
- 500mA resistive load to short circuit
- Short circuit to 500mA resistive load
- Short circuit continuous

Capture the voltage, and current of the rail under test and the voltage of VBATT. Validate the Comms does not misoperate in any way.

3.10.5.2 Test Data

| To the regulator output, apply no load to 500mA resistive load | | | |
|--|--|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of VBATT | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

| To the regulator output, apply 500mA resistive load to no load | | | |
|--|--|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of VBATT | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

| To the regulator output, apply no load to 10 μ F MLCC | | | |
|---|--|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of VBATT | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

| To the regulator output, apply 500mA resistive load and add 10 μ F MLCC | | | |
|---|--|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of VBATT | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

| To the regulator output, apply no load to short circuit | | | |
|---|---|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of <i>VBATT</i> | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

| To the regulator output, apply short circuit to no load | | | |
|---|---|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of <i>VBATT</i> | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

| To the regulator output, apply 500mA resistive load to short circuit | | | |
|--|---|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of <i>VBATT</i> | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

| To the regulator output, apply short circuit to 500mA resistive load | | | |
|--|---|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of <i>VBATT</i> | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

| To the regulator output, apply short circuit continuous load | | | |
|--|---|------------------|-------------|
| Regulator | Capture voltage and current of the rail and the voltage of <i>VBATT</i> | Passing Criteria | Pass / Fail |
| 5.0V | | No misoperation | |

3.10.5.3 Test Notes

Delete me if not required

3.11 Low Drop-Out Regulators

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in Low Drop-Out Regulators. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Electrical Systems Team page of the Wiki under Tutorials and Resources

3.11.1 Output Voltage

3.11.1.1 Test Instructions

Apply 3.7V to *VBATT* and 3.3V to 3.3V. Measure the voltage of the 3.1V-0 regulator under no load and under an 50mA resistive load.

Note: Measure the DC component with $PLC^{39} > 100$

3.11.1.2 Test Data

| Measure the voltage of the 3.1V-0 LDO regulator under no load and under a 50mA resistive load | | | | |
|---|-----------------|-------------------|---------------------|-------------|
| Regulator | No Load Voltage | 50mA Load Voltage | Passing Criteria | Pass / Fail |
| 3.1V-0 | | | $3.05V < V < 3.15V$ | |

3.11.1.3 Test Notes

Delete me if not required

3.11.2 Output Ripple and Noise

3.11.2.1 Test Instructions

Apply 3.7V to VBATT and 3.3V to 3.3V. Measure the ripple and noise of the 3.1V-0 LDO regulators whilst under a 50mA resistive load.

Note: Measure the rms AC component with $3Hz < f$

3.11.2.2 Test Data

| Measure the ripple of the 3.1V-0 LDO regulator whilst under a 50mA resistive load. | | | |
|--|--------------------|--------------------|-------------|
| Regulator | Measure the ripple | Passing Criteria | Pass / Fail |
| 3.1V-0 | | $ V_{rms} < 25mV$ | |

3.11.2.3 Test Notes

Delete me if not required

3.12 RF Clock Generators

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in RF Clock Generators.

3.12.1 Reference Clock Supply

3.12.1.1 Test Instructions

Measure the voltage of each reference clock's supply. Ensure the voltage, including noise and ripple, is $3.3V \pm 0.5\%$.

3.12.1.2 Test Data

| Measure the voltage of each reference clock's supply. | | | |
|---|---------|---------------------|-------------|
| RF Chain | Voltage | Passing Criteria | Pass / Fail |
| 700mm Uplink | | $3.08V < V < 3.12V$ | |

³⁹ Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

| Measure the voltage of each reference clock's supply. | | | |
|---|---------|---------------------|-------------|
| RF Chain | Voltage | Passing Criteria | Pass / Fail |
| 700mm Downlink | | $3.08V < V < 3.12V$ | |
| 230mm Downlink | | $3.08V < V < 3.12V$ | |

3.12.1.3 Test Notes

Delete me if not required

3.12.2 Reference Clock Frequency

3.12.2.1 Test Instructions

Measure the frequency of each reference clock. Ensure the frequency is $19.68MHz \pm 5ppm$.

3.12.2.2 Test Data

| Measure the frequency of each reference clock output | | | |
|--|-------------------|-------------------------|-------------|
| RF Chain | Oscillator output | Passing Criteria | Pass / Fail |
| 700mm Uplink | | $f = 19.68MHz \pm 5ppm$ | |
| 700mm Downlink | | $f = 19.68MHz \pm 5ppm$ | |
| 230mm Downlink | | $f = 19.68MHz \pm 5ppm$ | |

3.12.2.3 Test Notes

Delete me if not required

3.12.3 Output Frequency

3.12.3.1 Test Instructions

Configure each generator to output its frequency as follows. Use a spectrum analyzer to measure the output. Ensure the frequency is within $10ppm$ and bandwidth is less than $200ppm$.

- 700mm Uplink: 880MHz
- 700mm Downlink: 440MHz
- 230mm Downlink: 1.27GHz

Note: Measure the bandwidth at the $-3dB$ point

3.12.3.2 Test Data

| Measure the frequency of each generator output with a spectrum analyzer | | | |
|---|------------------------------|---|-------------|
| RF Chain | Capture the generator output | Passing Criteria | Pass / Fail |
| 700mm Uplink | | $f = 880MHz \pm 10ppm$ $B < 176kHz$ | |
| 700mm Downlink | | $f = 440MHz \pm 10ppm$ $B < 87kHz$ | |
| 230mm Downlink | | $f = 1.27GHz \pm 10ppm$ $B < 250kHz$ | |

3.12.3.3 Test Notes

Delete me I not required

3.13 Differential Drivers

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in DACs.

3.13.1 Test Instructions

Have the μ Controller generate a square wave on each modulator input with a frequency of 25kHz. Validate the waveform and voltage levels at the gain resistors.

3.13.2 Test Data

| Have the μ Controller generate a square wave on each modulator input with a frequency of 25kHz. | | | |
|---|---|--|-------------|
| Signal | Capture the single ended and differential signals | Passing Criteria | Pass / Fail |
| 230 ID | | $V = 1.2V \pm 0.5V$ Within 3% Signal Integrity | |
| 230 QD | | $V = 1.2V \pm 0.5V$ Within 3% Signal Integrity | |
| 700 ID | | $V = 0.7V \pm 0.3V$ Within 3% Signal Integrity | |
| 700 QD | | $V = 0.7V \pm 0.3V$ Within 3% Signal Integrity | |

3.14 RF Chain - 230mm Downlink

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in RF Modulators, Low Noise Amplifier, and 230mm Power Amplifier.

3.14.1 Test Instructions

Have the μ Controller generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 120kbps. Validate the following parameters:

- Power output of 1W when power amplifier bias is set to maximum
- Spectral bandwidth of less than 120kHz
- Distinct separation of symbols

3.14.2 Test Data

| Have the μ Controller generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 120kbps on the 230mm radio. | | | |
|---|---|---------------------|----------------|
| Parameter | Value (Scope or Spectrum Analyzer Capture) | Passing Criteria | Pass / Fail |
| Output Power | | $P = 1W \pm 0.2W$ | |
| Spectral Bandwidth | | $B < 120kHz$ | |

| | | |
|---|---------------------|----------------|
| Have the μ Controller generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 120kbps on the 230mm radio. Use an SDR to demodulate into symbols | | |
| Capture the I/Q signals (waveforms and constellation) | Passing Criteria | Pass / Fail |
| | Distinct Symbols | |

3.14.3 Test Notes

Delete me if not required.

3.15 RF Chain - 700mm Downlink

Results: Pass / Fail

Test Configuration:

This test evaluates the circuit described in RF Modulators, Low Noise Amplifier, and 700mm Power Amplifier.

3.15.1 Isolation Switch

3.15.1.1 Test Instructions

Have the μ Controller gradually increase the power output of the 700mm downlink radio while the RF switch is set to downlink. Measure the power on the 700mm uplink radio input. Ensure this power does not exceed 0dBm.

3.15.1.2 Test Data

| Have the μ Controller gradually increase the power output of the 700mm downlink radio while the RF switch is set to downlink. Measure the power on the 700mm uplink radio input. Ensure this power does not exceed 0dBm. | | |
|--|------------------|-------------|
| Max power | Passing Criteria | Pass / Fail |
| | $P < 0dBm$ | |

3.15.1.3 Test Notes

Delete me if not required.

3.15.2 Digital Modulation

3.15.2.1 Test Instructions

Have the μ Controller generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 32kbps on the 700mm radio. Validate the following parameters:

- Power output of 1W when power amplifier bias is set to maximum
- Spectral bandwidth of less than 32kHz
- Distinct separation of symbols

3.15.2.2 Test Data

| Have the μ Controller generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 32kbps on the 700mm radio. | | | |
|--|---|---------------------|----------------|
| Parameter | Value (Scope or Spectrum Analyzer Capture) | Passing Criteria | Pass / Fail |
| Output Power | | $P = 1W \pm 0.2W$ | |
| Spectral Bandwidth | | $B < 32kHz$ | |

| Have the μ Controller generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 32kbps on the 700mm radio. Use an SDR to demodulate into symbols | | |
|--|---------------------|----------------|
| Capture the I/Q signals (waveforms and constellation) | Passing Criteria | Pass / Fail |
| | Distinct Symbols | |

3.15.2.3 Test Notes

Delete me if not required

3.15.3 Analog Modulation

3.15.3.1 Test Instructions

Have the μ Controller generate an amplitude modulated audio signal on the 700mm radio. Validate the following parameters:

- Power output of 1W when power amplifier bias is set to maximum
- Spectral bandwidth of less than 32kHz
- Recognizable demodulated audio

3.15.3.2 Test Data

| Have the μ Controller generate an amplitude modulated audio signal on the 700mm radio. | | | |
|--|---|---------------------|----------------|
| Parameter | Value (Scope or Spectrum Analyzer Capture) | Passing Criteria | Pass / Fail |
| Output Power | | $P = 1W \pm 0.2W$ | |

| Have the μ Controller generate an amplitude modulated audio signal on the 700mm radio. | | | |
|--|---|---------------------|----------------|
| Parameter | Value (Scope or Spectrum Analyzer Capture) | Passing Criteria | Pass / Fail |
| Spectral Bandwidth | | $B < 32kHz$ | |

| Have the μ Controller generate an amplitude modulated audio signal on the 700mm radio. Use an SDR to demodulate into audio. | | | |
|---|--|-----------------------|----------------|
| Capture the I/Q signals (waveforms) | | Passing Criteria | Pass / Fail |
| | | Recognizable audio | |

3.15.3.3 Test Notes

Delete me if not required

3.16 RF Chain - 700mm Uplink

Results: Pass / Fail

Test Configuration: Doug

This test evaluates the circuit described in RF Demodulator, and Low Noise Amplifier.

3.16.1 Test Instructions

Have a radio generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 20kbps to transmit to the 700mm radio with a received power of $-150dBm$. Validate the following parameters:

- Signal to noise ratio (SNR) $> 30dBm$
- Output voltage of $1.65V \pm 1V$
- Distinct separation of symbols

3.16.2 Test Data

| Have a radio generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 20kbps to transmit to the 700mm radio with a received power of $-150dBm$. | | | |
|---|---|---------------------|----------------|
| Parameter or Signal | Value (Scope or Spectrum Analyzer Capture) | Passing Criteria | Pass / Fail |
| SNR | | $SNR > 30dBm$ | |
| DEMOD_ID | | $V = 1.65V \pm 1V$ | |
| DEMOD_QD | | $V = 1.65V \pm 1V$ | |

| | | |
|---|------------------|-------------|
| Have a radio generate a QPSK modulated signal with pattern 00 01 11 10 with a data rate of 20kbps to transmit to the 700mm radio with a received power of $-150dBm$. | | |
| Capture the I/Q signals (waveforms and constellation) | Passing Criteria | Pass / Fail |
| | Distinct Symbols | |

3.16.3 Test Notes

Delete me if not required.