This document explains the function of the EPS, its schematic level design, its board level design, and its functional testing

EPS

Electrical Power Subsystem Design

Revision: 1.1.1

Bradley Davis

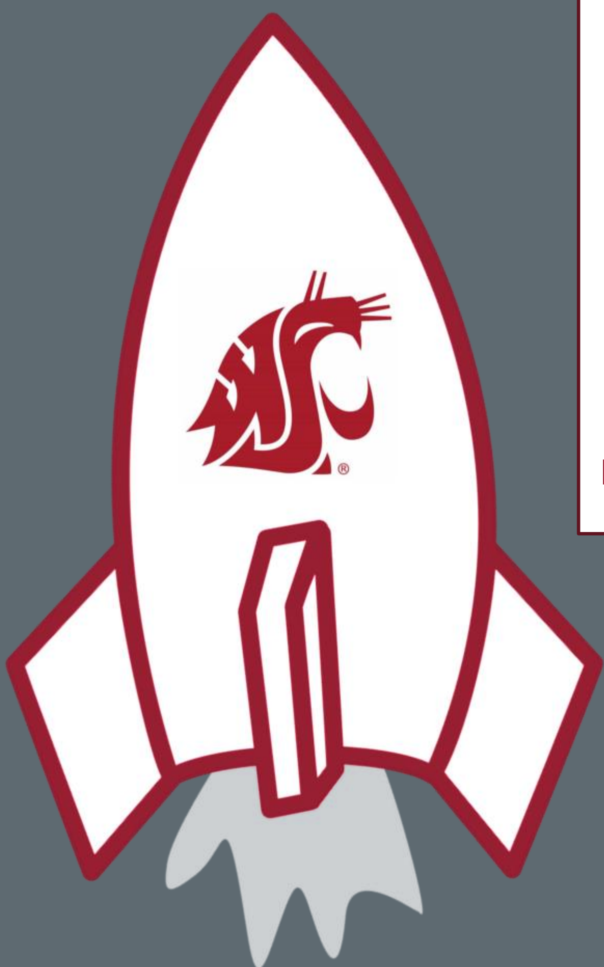

Table of Contents

1 Introduction

This document explains how the EPS will fulfil the following Functions and conform to the following Requirements. This document refers to the EPS version 2.1 and Solar Panel version 2.0.

1.1 Function

The Electrical Power Subsystem (EPS) is responsible for the following:

- Accumulating energy
- Regulating voltage
- Distributing power

1.2 Requirements

The system requirements and EPS design requirements can be found on GitHub.

2 Detailed Description

This section references the EPS schematic. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Power Input

Energy is captured from the Sun using an array of photovoltaic cells[1]. These cells are mounted onto solar panels that adjust the voltage and current to acceptable levels for direct charging of lithium-ion batteries[2]. These criteria are up to $4.1V$ and up to $0.5C$[3] per battery. Furthermore, power can be inputted from the umbilical[4] using the same criteria as the solar panels. The umbilical will only be used whilst on the ground. The PMIC will automatically monitor the charging and disable current paths to follow the prescribed charging, see Energy Storage for more details. Most lithium-ion charging curves indicate voltage up to $4.2V$ and current up to $1C$; however, the EPS will limit to $4.1V$ and $0.5C$ to preserve battery health[5]. Replacing the batteries on the EPS whilst in orbit is very difficult.

The solar panel and umbilical inputs are routed through a balance switching matrix before entering the batteries. This allows the PMIC to switch every cell going to either or both batteries[6].

2.1.2 Energy Storage

The EPS stores energy from the solar panels in batteries to fulfil high instantaneous power demands and any power demands during periods of eclipse[7]. Each battery has a protection IC that protects against the following faults:

- Overcharge
- Over-discharge
- Charge overcurrent
- Discharge overcurrent
- Load short-circuit detection

[1] Requirement EPS-010
[2] For details on charging lithium-ion batteries, http://batteryuniversity.com/learn/article/charging_lithium_ion_batteries
[3] 1C is equal to the charge of the battery divide by 1 hour (Take the Ah of the battery and drop the "h")
[4] Requirement EPS-021
[5] Requirement REQ-009
[6] Requirement EPS-008
[7] Requirements EPS-005, EPS-006, EPS-009

The PMIC will monitor and regulate the temperature of the batteries. The batteries (and power inputs) disconnect from the rest of the EPS via separation switches and the RBF switch[8].

2.1.3 Power Output

The EPS has two separate rails for distribution: unregulated from the batteries and $3.3V$[9]. There are two regulators[10], one per battery. Most loads are connected via the backplane and are individually switched between either source (power chain A or B) or turned off, and current monitored[11]. The PMIC controls these switches.

There is a single load that cannot be disconnected from the regulators: the PMIC[12]. This ensures there is at least one processor that can turn on the rest of the satellite. The outputs also have default states that allow the bus to be on if the PMIC fails to drive the switches.

2.1.4 PMIC

The Power Management IC (PMIC) is the microprocessor monitoring and operating the EPS[13]. Only one PMIC exist as adding redundant processors adds complexity that could reduce reliability. It communicates over I²C to Command and Data Handling subsystem (C&DH)[14] via the backplane and to its monitoring sensors directly. It collects sensor information and transfers this to the C&DH to be included in a telemetry packet to Ground[15]. The C&DH may also send commands. For example, enter safe mode by switching off these subsystems[16].

2.1.5 Monitoring

The PMIC, through ADCs, monitors current, and voltage at various locations and temperature of various components, indicated on the block diagram[17].

2.2 Schematic

2.2.1 Isolated Grounds

On page 2 of the schematic (D1), are the four isolated grounds found on the EPS. Power ground *(PGND)* is directly connected to the backplane and most of the power chain. The other grounds are shorted to *PGND* using a 0Ω resistor rated up to $2A$, the expected current is less than $50mA$ each. Digital ground *(DGND)* connects to the digital circuity including the PMIC and Monitoring circuits. Analog ground *(AGND)* connects to analog monitoring circuits including

[8] Requirements EPS-020
[9] Requirement EPS-001
[10] Requirement EPS-008
[11] Requirements EPS-008, EPS-011, EPS-012
[12] Requirements EPS-013
[13] Requirement EPS-022
[14] Requirement EPS-018
[15] Requirement EPS-019
[16] Requirement EPS-014
[17] Requirements EPS-011, EPS-015, EPS-016, EPS-017

the ADCs, their voltage reference, and the thermistors. Chassis ground *(CHASSIS)* is connected to the Mechanical Features including bolt holes and the card rails.

2.2.2 Power Rails

Page 2 of the schematic illustrates all the power rails on the EPS. Notice how most components of the power chain can be routed to the other chain to increase redundancy. The expected current consumptions are derived from the energy budget. The limit of $1A$ per rail is imposed by the backplane.

2.2.2.1 Always-On Rails

There are two rails that are always-on and cannot be switched off, except with the Separation Switching. These provide power for the PMIC as the PMIC cannot be allowed to turn off or other subsystems may not be able to be turned on. They are *VBATT* (page 4, C6), and *3.3V* (page 5, B6 & D6). They use "ideal diodes"[18] to OR the power together from both power chains.

2.2.3 Input Switching

A matrix of MOSFETs (page 3) switch the solar panel inputs and umbilical input to either or both batteries. The P-channel MOSFETs[19] have been chosen for their low Rds(on), sufficient power dissipation by the body, and dual package. The dual package allows for less space used on the PCB which is at a premium on a nanosatellite. They are logic level drive which allows the PMIC to directly control them.

As the GPIO of the PMIC defaults to high impedance input during boot up (every reset will enter this state). The input switches have $10k\Omega$ pull downs (page 8) to choose their default state: all inputs are connected to both batteries and power chains.

The power inputs are placed in parallel with the batteries such that the loads will draw from the power inputs before drawing from the batteries.

2.2.4 Battery & Battery Protection

The batteries (page 4, B2 & B5) are 18650 lithium-ion. The chemistry was chosen for its high volumetric and mass energy densities. A specific cell has not been chosen, a long-term study is required. The EPS will be compatible with most cells.

The batteries are protected by dedicated lithium-ion single-cell protection ICs[20] (page 4, B1 & B4). They measure the current passing through the battery by measuring the voltage between pins 4 & 6. With the Rds(on) of the MOSFET[21] and

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[18] LTC4411, a MOSFET with integrated control circuity to function like a diode
[19] NTLUD3A50PZ
[20] BQ29700
[21] DMN2008LFU

the shunt resistor, the IC prevents against $\frac{90\ to\ 110mV}{(6.4+6.4+10)m\Omega} = \ 4\ to\ 4.8A$ of overcurrent. The IC also prevents against $4.275V$ of over-voltage and $2.800V$ of under-voltage.

The batteries are thermally connected to a heater and Temperature Monitoring. The heater is a TO-220 10Ω resistor which generates up to $\frac{(3.7V)^2}{10\Omega} \approx 1.4W$ of heat. A lower resistance resistor may be exchanged for more heating capabilities, a thermal test will indicate this need. The heater can be driven at lower duty cycle, through PWM, to reduce the average output power.

2.2.5 Separation Switching

The separation switches (connected via the backplane) or the RBF pin switch (page 4, D2) disconnect the batteries and power input from the rest of the power chain. Either of the switches apply a pull down to the gate of a MOSFET that inverts the signal to another MOSFET that interrupts the power chain. When the umbilical is connected, and voltage is applied, it drives the MOSFETs the opposite way to connect the power chain. In the default state (no switches depressed or umbilical connected) a weak pull up to the batteries (through ORing diodes) keeps the MOSFETS driven to connect the power chain.

Connected to the separation switches and RBF pin switch is a capacitor and limiting resistor such that the time constant is $(1\mu F)(30M\Omega + 100k\Omega + 10k\Omega) \approx 30s$. The PMIC measures the voltage across the capacitor. When the PMIC boots up, it will check this voltage is decide if it is powering up after a reset (the capacitor will still be charged) or after a deployment (the capacitor will be discharged).

2.2.6 3.3V Regulation

The 3.3V regulators (page 5) are switching mode, buck topology. The controller[22] automatically senses the output voltage and adjusts the switching parameters to keep the output at $3.3V$. The controller was chosen for its small package and ability to output 100% duty cycle such that when the input drops below $3.3V$, the output will follow the voltage of the input.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

On the drain of the switching MOSFETs (page 5, A3 & C3) are snubber circuits that absorb and suppress transients thus reducing the output noise.

The switching MOSFETs and inductors (page 5, A3 & C3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

[22] TPS64200

2.2.7 Output Switching

The output switching (pages 6, 7) uses the same setup as the Input Switching. The default cases are as follow: rails connected to bus subsystems default on, rails connected to payloads default off.

Most outputs go into the backplane for distribution to their connected subsystem. The *PR_DEPLOY* output (for releasing deployable mechanisms) and *PV_3.3V* (for the solar panel monitoring circuits) connect to their load via wire harness (page 3, A2:C2).

2.2.8 Current Monitoring

At various locations, the power chain has shunt resistors connected to differential ADCs to monitor the current. Those locations are:

- Batteries: charging/discharging (page 4, B2 & B5)
- Power chain input (page 4, A2 & A5)
- 3.3V regulator input (page 5, A3 & C3)
- 3.3V regulator output (page 5, A5 & C5)
- Each output rail (pages 6, 7)

The solar panels monitor their own current and the PMIC communicates to them via the wire harness (page 3, A2:C2).

2.2.9 Voltage Monitoring

At various locations, the power chain is probed for the voltage using one of the ADCs in single ended mode. Those locations are:

- Batteries (page 4, B2 & B5)
- 3.3V regulator output (page 5, A6 & C6)
- Umbilical input (page 3, C2)

The solar panels monitor their own voltages and the PMIC communicates to them via the wire harness (page 3, A2:C2).

2.2.10 Temperature Monitoring

At various locations, the temperature is monitored using thermistors and one of the ADCs in single ended mode. Those locations are:

- Batteries (page 4, B2 & B5)
- 3.3V regulator switching components (page 5, A4 & C4)
- Each corner of the PCB (page 11, C5)

2.2.11 PMIC

The PMIC (page 9, B3, A1, A3, & A4) is a microcontroller from the STM32 low power family[23]. It was chosen for its ease of programming, and low power consumption. Since the PMIC is essentially just controlling GPIO and talking over two I²C Buses, the features of higher end processors are not needed. There is a total of 72 switch control signals and 10 other signals (programming, I²C,

[23] STM32L476RG

interrupts). Upgrading the processor to the 100 pin variant (from 64 pins) would eliminate the GPIO expanders but would also take up the same if not more PCB area, a premium on a nanosatellite. Furthermore, using I²C expanders reduces routing complexity as not every one of the 72 control signals need to connect all the way to the PMIC.

The PMIC's reset pin is connected to the backplane such that if it or any subsystem needs to reset itself, all the subsystems reset. This is to put all the subsystems in a known state which reduces cause for error.

2.2.11.1 Programming Connections

During testing, the PMIC is programmed via Serial Wire Debug[24] (SWD, page 9, B1). The process of programming is made simple with just a single 6 pin header and a robust software utility. In orbit, the PMIC can be programmed via JTAG[25]. The In-Flight JTAG Reprogrammer (IFJR) connects via the backplane, through a tri-state buffer/logic level converter[26] (page 9, B5:D5). The IFJR can enable or disable the tri-state buffer which essentially disconnects the JTAG interface from the PMIC (it outputs high impedance), allowing the SWD to program. The logic level conversion changes the *VBATT* voltages from the PMIC to $3.3V$ voltages found on the backplane.

2.2.12 I²C Bus

The PMIC has two I²C buses (page 9, A3 & A5). One is for the EPS monitoring and control devices. The other is to communicate with the C&DH. On the EPS bus, the PMIC is the master served by the attached devices.

2.2.12.1 GPIO Expanders

There are six GPIO expanders[27] connected to the PMIC, each with 16 IO. Two are on the EPS (page 9, C1 & C3). There is one on each solar panel. The expander was chosen for its low power and up to eight addresses. The list of address follow:

- [`0x40`] EPS-0 (page 9, C1)
- [`0x42`] EPS-1 (page 9, C5)
- [`0x44`] PV0 (+Z) (page 3, A2)
- [`0x46`] PV1 (-Y) (page 9, B2)
- [`0x48`] PV2 (-X) (page 9, B2)
- [`0x4A`] PV3 (+Y) (page 9, C2)

2.2.12.2 ADCs

There are 10 ADCs[28] connected to the PMIC, each with 16 single-ended inputs or eight differential inputs or a combination. Six are on the EPS (page 10, A2, A4, C2, & C4; page 11, A2 & C2). There is one on each solar panel. The ADC was

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[24] For more details on SWD, https://developer.arm.com/products/system-ip/coresight-debug-and-trace/coresight-architecture/serial-wire-debug
[25] For more details on JTAG, https://en.wikipedia.org/wiki/JTAG
[26] SN74LVC244AR
[27] TCA9535
[28] LTC2499

chosen for its low power, differential inputs, small package, and up to 27 addresses. The list of address follow:

- [`0xEE`] Global ADC address
- [`0x28`] EPS-0 (page 10, A2), current only
- [`0x2A`] EPS-1 (page 10, A4), current only
- [`0x2C`] EPS-2 (page 10, C2), current only
- [`0x2E`] EPS-3 (page 10, C4), current only
- [`0x6A`] EPS-4 (page 11, A2), current only
- [`0x6C`] EPS-5 (page 11, C2), voltage only
- [`0xC8`] PV0 (+Z) (page 3, A2), voltage and current
- [`0xCA`] PV1 (-Y) (page 3, B2), voltage and current
- [`0xCC`] PV2 (-X) (page 3, B2), voltage and current
- [`0xCE`] PV3 (+Y) (page 3, C2), voltage and current

2.2.12.3 Backplane to C&DH

The PMIC is a slave to the C&DH. See the interface document for details.

2.2.13 Analog Voltage Reference and Supply

The EPS has a precision voltage reference (page 11, A5)[29] for calibrating the ADCs. For the Current Monitoring ADCs, this is inputted into the reference input which results in a resolution at $16b$ of $\frac{900mV}{2^{16}} = 13.73\mu\frac{V}{LSB}$. For the Voltage Monitoring ADCs, this is inputted into one of the channels which provide calibration through linear math. These ADCs have the analog voltage supply inputted into the reference input. They also have a voltage divider between the channel inputs and the actual ADC input (page 11, C1) which allows 3.3 times the voltage for a total range of $(\pm 1.65V * 3.3) = \pm 5.4V$ and a resolution at $16b$ of $\frac{5.4V}{2^{16}} = 82\mu\frac{V}{LSB}$.

The EPS has an analog voltage supply (page 11, B5) which is fed by the always-on *3.3V* rail filtered with a ferrite bead and capacitors. Precision is not required as all ADCs use the precision voltage reference for calibration. This is the source for the Temperature Monitoring thermistors.

2.2.14 Mechanical Features

The RBF pin holder (page 4, D1) and 3.3V Regulation heatsink (page 5, B1 & D1) mount directly to the EPS board using bolts. These holes are conductive and connected directly to *CHASSIS*, see Isolated Grounds. The EPS also slots into the structure using rails[30] which are also conductive and connected directly to chassis ground. Each of the holes have a capacitor and resistor connecting to power ground which will absorb transients.

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[29] MCP1501

[30] See backplane documentation for details

2.3 Board

The board shall be double layered with $2\ oz$ copper and ENIG finish. The board shall also conform to the dimensions specified by the CougSat Module Standard.

2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless otherwise specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width:	$0.16mm$
Vias:	$\emptyset 0.3mm$, unlimited count
Separation:	$0.16mm$
Length:	unlimited

Devices with specific placement and routing considerations are called out on the schematic, see “CAD Note:”

2.3.1.1 Solar Panel Inputs - PV_IN[0:7], PGND

PGND applies to between the solar panel headers and the backplane

Trace width: $0.3mm$

2.3.1.2 Umbilical Input - UMB_IN, PGND

PGND applies to between the umbilical header and the backplane

Trace width: $0.6mm$

2.3.1.3 Battery Connections - VIN-[A:B], BP_VSS-[A:B], BP_VSS-I[A:B], VBATT-[A:B], PGND

PGND applies to between the low side battery protection MOSFETs and the backplane.

Trace width:	$3.0mm$
Vias:	$\emptyset 0.3mm$ five per layer change

2.3.1.4 SMPS Switching Node - 3.3V_ISENS-[A:B], 3.3V_REG_BUCK_NODE-[A:B]

Trace width:	$2.5mm$
Vias:	No vias

Minimize RF emission

2.3.1.5 SMPS Output - 3.3V_I-[A:B], 3.3V-[A:B]

The traces can taper down once loads branch off and less than three loads remain.

Trace width:	$2.5mm$
Vias:	$\emptyset 0.3mm$ three per layer change

2.3.1.6 SMPS Ground - PGND

PGND applies to between the filtering capacitors and the backplane.

Trace width: $1.0mm$

2.3.1.7 Rail Output Channels – PR_3.3V-[0:12], PR_BATT-[0:6], PR_BH-[0:1]

Trace width: $0.6mm$

2.3.1.8 Deployables Output – PR_DEPLOY

Trace width: $1.5mm$
Vias: $\emptyset 0.3mm$ two per layer change

2.3.1.9 JTAG – JTAG-[TCK, TDI, TDO, TMS], BUS_JTAG-[TCK, TDI, TDO, TMS]

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

2.3.1.10 I^2C – I2C_[SDA, SCL], BUS_I2C_[SDA, SCL, IRQ]

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

3 Testing

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test[31].

- Waveforms shall be captured whenever appropriate
- Have the event take fill the screen (for fast events, zoom in; for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-PowerBoard/Testing/EPS.2.1

Common test instructions can be found on the wiki.

Note: In the following sections, applying a $4.1V, 300mA$ source means to connect a power supply limited to $4.1V$ and $300mA$. The actual voltage and current may be less than this.

3.1 Before First Power-On Check

Configuration: Auden

This test is required to be executed before batteries are attached and before any external power is applied to the EPS.

3.1.1 Test Instructions

Measure the resistance of various points in reference to *PGND* located at the backplane. Measure the resistance across each current shunt resistor. This is informational only; the resistance of the current shunt resistor is used to calibrate the Current Monitoring. When measuring in circuit resistances, flip the probes and take the lower value.

3.1.2 Test Data

Node	Resistance		Node	Resistance
VIN-A	$42.4k\Omega$		VIN-B	$50.7k\Omega$
VBATT-A	$205k\Omega$		VBATT-B	$205k\Omega$
VBATT	$3.46k\Omega$		3.3V	$34.6k\Omega$
3.3V-A	$1.57k\Omega$		3.3V-B	$1.57k\Omega$
AVREF	$41.5k\Omega$		AVDD	$3.45k\Omega$

[31] For test 3.1, place files in the subfolder *"3.1"* and so on

Node	Resistance		Node	Resistance
I2C_SCL	$3.87k\Omega$		I2C_SDA	$3.85k\Omega$
BUS_I2C_SCL	$34.4k\Omega$		BUS_I2C_SDA	$34.5k\Omega$

Net	Resistor	Value		Net	Resistor	Value
Battery A	R36	$15.2m\Omega$		Battery B	R45	$12.0m\Omega$
VIN-A[32]	Q9			VIN-B	Q11	
3.3V Input A	R5 + R6	$21.5m\Omega$		3.3V Input A	R110 + R111	$20.5m\Omega$
3.3V Output A	R41	$14.5m\Omega$		3.3V Output B	R82	$17.1m\Omega$
PR_3.3V-0	R97	$53.3m\Omega$		PR_3.3V-1	R96	$54.2m\Omega$
PR_3.3V-2	R94	$51.8m\Omega$		PR_3.3V-3	R91	$54.4m\Omega$
PR_3.3V-4	R89	$49.3m\Omega$		PR_3.3V-5	R86	$52.1m\Omega$
PR_3.3V-6	R85	$51.8m\Omega$		PR_3.3V-7	R83	$55.8m\Omega$
PR_3.3V-8	R81	$49.7m\Omega$		PR_3.3V-9	R78	$53.8m\Omega$
PR_3.3V-10	R74	$53.4m\Omega$		PR_3.3V-11	R72	$51.8m\Omega$
PR_3.3V-12	R70	$52.8m\Omega$		PR_BATT-0	R69	$51.8m\Omega$
PR_BATT-1	R68	$52.4m\Omega$		PR_BATT-2	R65	$51.5m\Omega$
PR_BATT-3	R63	$51.7m\Omega$		PR_BATT-4	R60	$50.2m\Omega$
PR_BATT-5	R59	$49.7m\Omega$		PR_BATT-6	R58	$51.2m\Omega$
PV_3.3V-0	R11	$46.9m\Omega$		PV_3.3V-1	R13	$50.0m\Omega$
PV_3.3V-2	R113	$50.4m\Omega$		PV_3.3V-3	R112	$52.2m\Omega$
PR_BH-0	R43	$54.1m\Omega$		PR_BH-1	R67	$56.2m\Omega$
PR_DEPLOY	R109 ‖ R108	$27.1m\Omega$				

3.1.3 Test Notes

Measurement error of the $10m\Omega$ is significant, use the listed value for current sense.

Used four wire resistance measurement for the current shunt resistors.

Could not measure the resistance of the MOSFETs.

3.2 Separation Switching

Results: Fail
Configuration: Auden

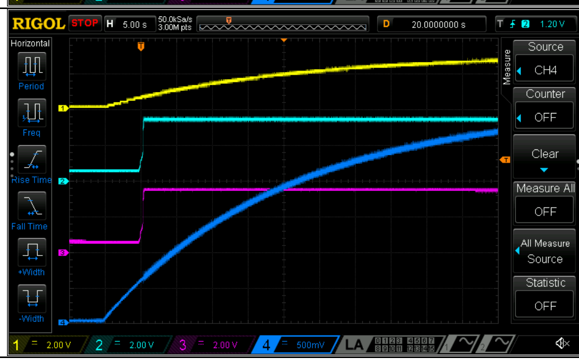
This test evaluates the circuit described in Separation Switching.

3.2.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Insert the RBF pin, wait at least $2min$, remove the RBF pin. Measure *PWR_CTRL_SW, VBATT-A, VBATT-B,* and *EJECT_TIMER.*

[32] The EPS uses the deployment switch as the current shunt. Drive the gate low and measure between drain and source

3.2.2 Test Data

Insert the RBF pin, wait at least $2min$, remove the RBF pin.			
Operation	Capture *PWR_CTRL_SW, VBATT-A, VBATT-B,* and *EJECT_TIMER*	Passing Criteria	Pass / Fail
Insertion		*VBATT-A* and *VBATT-B* fall < $10mV$ within $10ms$, EJECT_TIMER falls < $500mV$ within $2min$	**Fail**
Removal		*VBATT-A* and *VBATT-B* rise > $3V$ within $10ms$, *EJECT_TIMER* rises > $2V$ between $30s$ and $2min$	**Fail**

3.2.3 Test Notes

Ch 1: *PWR_CTRL_SW*
Ch 2: *VBATT-A*
Ch 3: *VBATT-B*
Ch 4: *EJECT_TIMER*

3.3 Power Rails

Results: Pass / Fail

This test evaluates the circuit described in Power Rails.

3.3.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the PMIC not running code, upload a blank image or assert its reset pin, and the RBF pin inserted, apply power to each input one at a time as follows:

- $4.1V, 300mA$ to the solar panel inputs
- $4.1V, 1.0A$ to the umbilical input

Ensure that both batteries are receiving the power.

3.3.2 Test Data

Apply $4.1V, 300mA$ to PV_IN-0					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-1					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-2					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-3					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-4					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-5					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-6					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 300mA$ to PV_IN-7					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $400mW$	
B				Power > $400mW$	

Apply $4.1V, 1.0A$ to UMB_IN					
Battery	Voltage	Current	Power	Passing Criteria	Pass / Fail
A				Power > $1.5W$	
B				Power > $1.5W$	

3.3.3 Test Notes

Not running until switching matrix is fixed, see 3.4 Test Notes.

3.4 Input Switching

Results: Fail
Configuration: Auden

This test evaluates the circuit described in Input Switching.

3.4.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Drive each input switch to the following states while applying a $4.1V, 300mA$ source:

- *Both Off*
- *A On*
- *B On*
- *Both Off*

Ensure each channel is properly routing the power.

3.4.2 Test Data

Configure each input channel to *Both Off*. Apply a $4.1V, 300mA$ source to the input under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_IN-0			$A < 10mW$ & $B < 10mW$	
PV_IN-1			$A < 10mW$ & $B < 10mW$	
PV_IN-2			$A < 10mW$ & $B < 10mW$	
PV_IN-3			$A < 10mW$ & $B < 10mW$	
PV_IN-4			$A < 10mW$ & $B < 10mW$	
PV_IN-5			$A < 10mW$ & $B < 10mW$	
PV_IN-6			$A < 10mW$ & $B < 10mW$	
PV_IN-7			$A < 10mW$ & $B < 10mW$	
UMB_IN			$A < 10mW$ & $B < 10mW$	

Configure each input channel to *A On*. Apply a $4.1V, 300mA$ source to the input under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_IN-0			$A > 800mW$ & $B < 10mW$	
PV_IN-1			$A > 800mW$ & $B < 10mW$	
PV_IN-2			$A > 800mW$ & $B < 10mW$	
PV_IN-3			$A > 800mW$ & $B < 10mW$	
PV_IN-4			$A > 800mW$ & $B < 10mW$	
PV_IN-5			$A > 800mW$ & $B < 10mW$	
PV_IN-6			$A > 800mW$ & $B < 10mW$	
PV_IN-7			$A > 800mW$ & $B < 10mW$	
UMB_IN			$A > 800mW$ & $B < 10mW$	

Configure each input channel to *B On*. Apply a $4.1V, 300mA$ source to the input under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_IN-0			$A < 10mW \ \& \ B > 800mW$	
PV_IN-1			$A < 10mW \ \& \ B > 800mW$	
PV_IN-2			$A < 10mW \ \& \ B > 800mW$	
PV_IN-3			$A < 10mW \ \& \ B > 800mW$	
PV_IN-4			$A < 10mW \ \& \ B > 800mW$	
PV_IN-5			$A < 10mW \ \& \ B > 800mW$	
PV_IN-6			$A < 10mW \ \& \ B > 800mW$	
PV_IN-7			$A < 10mW \ \& \ B > 800mW$	
UMB_IN			$A < 10mW \ \& \ B > 800mW$	

Configure each input channel to *Both On*. Apply a $4.1V, 300mA$ source to the input under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_IN-0			$A > 400mW \ \& \ B > 400mW$	
PV_IN-1			$A > 400mW \ \& \ B > 400mW$	
PV_IN-2			$A > 400mW \ \& \ B > 400mW$	
PV_IN-3			$A > 400mW \ \& \ B > 400mW$	
PV_IN-4			$A > 400mW \ \& \ B > 400mW$	
PV_IN-5			$A > 400mW \ \& \ B > 400mW$	
PV_IN-6			$A > 400mW \ \& \ B > 400mW$	
PV_IN-7			$A > 400mW \ \& \ B > 400mW$	
UMB_IN			$A > 400mW \ \& \ B > 400mW$	

3.4.3 Test Notes

When switches are configured to both on the batteries are shorted together and supply each other which trips the battery protection. A short to one battery shorts the other one.

3.5 Output Switching

Results: Fail
Configuration: Auden

This test evaluates the circuit described in Output Switching.

3.5.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. Drive each output switch to the following states while applying a 10Ω resistive load:

- *Both Off*
- *A On*
- *B On*
- *Both Off*

Ensure each channel is properly routing the power.

Note: PR_BH-[0,1] already have a 10Ω resistive load and do not need an external load applied.

3.5.2 Test Data

Configure each output channel to *Both Off*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_3.3V-0			$A < 10mW \,\&\, B < 10mW$	
PV_3.3V-1			$A < 10mW \,\&\, B < 10mW$	
PV_3.3V-2			$A < 10mW \,\&\, B < 10mW$	
PV_3.3V-3			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-0			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-1			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-2			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-3			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-4			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-5			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-6			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-7			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-8			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-9			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-10			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-11			$A < 10mW \,\&\, B < 10mW$	
PR_3.3V-12			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-0			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-1			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-2			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-3			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-4			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-5			$A < 10mW \,\&\, B < 10mW$	
PR_BATT-6			$A < 10mW \,\&\, B < 10mW$	
PR_DEPOLY			$A < 10mW \,\&\, B < 10mW$	
PR_BH-0			$A < 10mW \,\&\, B < 10mW$	
PR_BH-1			$A < 10mW \,\&\, B < 10mW$	

Configure each output channel to *A On*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_3.3V-0			$A > 750mW \,\&\, B < 10mW$	
PV_3.3V-1			$A > 750mW \,\&\, B < 10mW$	
PV_3.3V-2			$A > 750mW \,\&\, B < 10mW$	
PV_3.3V-3			$A > 750mW \,\&\, B < 10mW$	
PR_3.3V-0			$A > 750mW \,\&\, B < 10mW$	
PR_3.3V-1			$A > 750mW \,\&\, B < 10mW$	
PR_3.3V-2			$A > 750mW \,\&\, B < 10mW$	
PR_3.3V-3			$A > 750mW \,\&\, B < 10mW$	

Configure each output channel to *A On*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PR_3.3V-4			$A > 750mW \& B < 10mW$	
PR_3.3V-5			$A > 750mW \& B < 10mW$	
PR_3.3V-6			$A > 750mW \& B < 10mW$	
PR_3.3V-7			$A > 750mW \& B < 10mW$	
PR_3.3V-8			$A > 750mW \& B < 10mW$	
PR_3.3V-9			$A > 750mW \& B < 10mW$	
PR_3.3V-10			$A > 750mW \& B < 10mW$	
PR_3.3V-11			$A > 750mW \& B < 10mW$	
PR_3.3V-12			$A > 750mW \& B < 10mW$	
PR_BATT-0			$A > 750mW \& B < 10mW$	
PR_BATT-1			$A > 750mW \& B < 10mW$	
PR_BATT-2			$A > 750mW \& B < 10mW$	
PR_BATT-3			$A > 750mW \& B < 10mW$	
PR_BATT-4			$A > 750mW \& B < 10mW$	
PR_BATT-5			$A > 750mW \& B < 10mW$	
PR_BATT-6			$A > 750mW \& B < 10mW$	
PR_DEPOLY			$A > 750mW \& B < 10mW$	
PR_BH-0			$A > 750mW \& B < 10mW$	
PR_BH-1			$A > 750mW \& B < 10mW$	

Configure each output channel to B *On*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_3.3V-0			$A < 10mW \& B > 750mW$	
PV_3.3V-1			$A < 10mW \& B > 750mW$	
PV_3.3V-2			$A < 10mW \& B > 750mW$	
PV_3.3V-3			$A < 10mW \& B > 750mW$	
PR_3.3V-0			$A < 10mW \& B > 750mW$	
PR_3.3V-1			$A < 10mW \& B > 750mW$	
PR_3.3V-2			$A < 10mW \& B > 750mW$	
PR_3.3V-3			$A < 10mW \& B > 750mW$	
PR_3.3V-4			$A < 10mW \& B > 750mW$	
PR_3.3V-5			$A < 10mW \& B > 750mW$	
PR_3.3V-6			$A < 10mW \& B > 750mW$	
PR_3.3V-7			$A < 10mW \& B > 750mW$	
PR_3.3V-8			$A < 10mW \& B > 750mW$	
PR_3.3V-9			$A < 10mW \& B > 750mW$	
PR_3.3V-10			$A < 10mW \& B > 750mW$	
PR_3.3V-11			$A < 10mW \& B > 750mW$	
PR_3.3V-12			$A < 10mW \& B > 750mW$	
PR_BATT-0			$A < 10mW \& B > 750mW$	
PR_BATT-1			$A < 10mW \& B > 750mW$	
PR_BATT-2			$A < 10mW \& B > 750mW$	

Configure each output channel to B *On*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PR_BATT-3			$A < 10mW \ \& \ B > 750mW$	
PR_BATT-4			$A < 10mW \ \& \ B > 750mW$	
PR_BATT-5			$A < 10mW \ \& \ B > 750mW$	
PR_BATT-6			$A < 10mW \ \& \ B > 750mW$	
PR_DEPOLY			$A < 10mW \ \& \ B > 750mW$	
PR_BH-0			$A < 10mW \ \& \ B > 750mW$	
PR_BH-1			$A < 10mW \ \& \ B > 750mW$	

Configure each output channel to Both *On*. Apply a 10Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PV_3.3V-0			$A + B > 750mW$	
PV_3.3V-1			$A + B > 750mW$	
PV_3.3V-2			$A + B > 750mW$	
PV_3.3V-3			$A + B > 750mW$	
PR_3.3V-0			$A + B > 750mW$	
PR_3.3V-1			$A + B > 750mW$	
PR_3.3V-2			$A + B > 750mW$	
PR_3.3V-3			$A + B > 750mW$	
PR_3.3V-4			$A + B > 750mW$	
PR_3.3V-5			$A + B > 750mW$	
PR_3.3V-6			$A + B > 750mW$	
PR_3.3V-7			$A + B > 750mW$	
PR_3.3V-8			$A + B > 750mW$	
PR_3.3V-9			$A + B > 750mW$	
PR_3.3V-10			$A + B > 750mW$	
PR_3.3V-11			$A + B > 750mW$	
PR_3.3V-12			$A + B > 750mW$	
PR_BATT-0			$A + B > 750mW$	
PR_BATT-1			$A + B > 750mW$	
PR_BATT-2			$A + B > 750mW$	
PR_BATT-3			$A + B > 750mW$	
PR_BATT-4			$A + B > 750mW$	
PR_BATT-5			$A + B > 750mW$	
PR_BATT-6			$A + B > 750mW$	
PR_DEPOLY			$A + B > 750mW$	
PR_BH-0			$A + B > 750mW$	
PR_BH-1			$A + B > 750mW$	

3.5.3 Test Notes

When switches are configured to both on the regulators are shorted together. A shorted load to one regulator shuts down the other one as well.

3.6 Battery Charging

Results: Pass
Configuration: Auden

This test evaluates the circuit described in Battery & Battery Protection.

3.6.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the PMIC not running code, upload a blank image or assert its reset pin, and the RBF pin inserted, apply a $4.1V, 1.0A$ source to the umbilical input. Measure the change in voltage after $30\ minutes$ and validate the battery is charging.

Note: Measure the voltage without the external source applied

3.6.2 Test Data

Apply a $4.1V, 1.0A$ source to the umbilical input Measure the change in voltage after $30\ minutes$					
Battery	Initial Voltage	Final Voltage	ΔV	Passing Criteria	Pass / Fail
A	$3.198V$	$3.199V$	$1mV$	$\Delta V > 20mV$	Fail
B	$3.792V$	$3.929V$	$137mV$	$\Delta V > 20mV$	Pass

3.6.3 Test Notes

Battery A protection disabled charging because it had a short and is now fixed. The battery does charge.

3.7 Battery Protection

Results: Pass

This test evaluates the circuit described in Battery & Battery Protection.

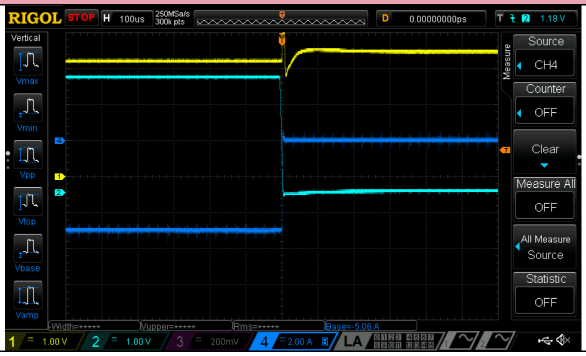
3.7.1 Discharge Overcurrent

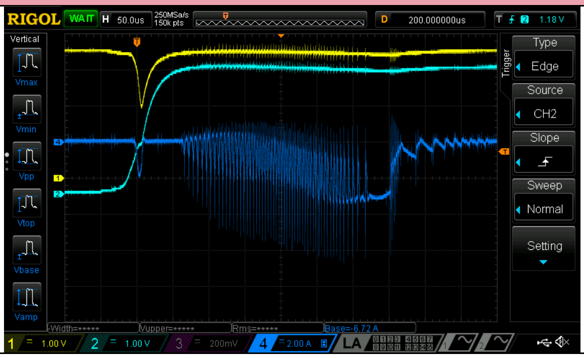
3.7.1.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply an increasing load to *VBATT* until *DOUT* transitions low. Decrease the load until the *DOUT* transitions high. Measure the battery current, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: Connect all the power outputs together to share the overcurrent.

3.7.1.2 Test Data

Apply an increasing load to *PR_BATT* outputs until *DOUT* transitions low				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A		$5.06A$	$3.5A < I < 5.4A$	Pass
B			$3.5A < I < 5.4A$	

Decrease a high load on *PR_BATT* outputs until *DOUT* transitions high				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A		$< 400mA$	$I < 3.5A$	Pass
B			$I < 4A$	

3.7.1.3 Test Notes

Recovered after last 10Ω resistor was removed. Testing battery B on next revision.

3.7.2 Load Short Circuit

3.7.2.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply a short between *VBATT* and *PGND*. Remove this short. Measure the battery current, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

3.7.2.2 Test Data

Apply a short between *VBATT* and *PGND*				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Delay	Passing Criteria	Pass / Fail
A		$288\mu s$	$125\mu s < t < 375\mu s$	Pass
B			$125\mu s < t < 375\mu s$	

Remove a short between *VBATT* and *PGND*				
Battery	Capture battery current, *COUT*, *DOUT*	Trigger Delay	Passing Criteria	Pass / Fail
A		$\sim 200ms$	$t < 1s$	Pass
B			$t < 1s$	

3.7.2.3 Test Notes

Recovering from a short requires the charger to be attached. Testing battery B on next revision.

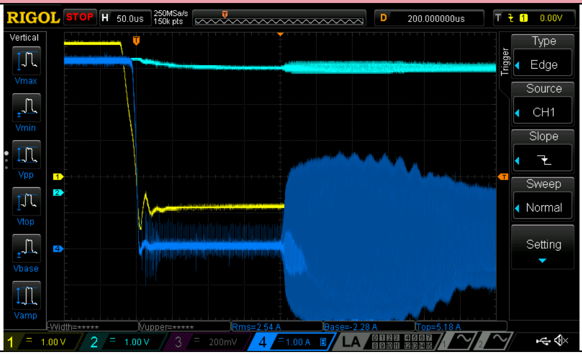
3.7.3 Charge Overcurrent

3.7.3.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply a $4.1V$ source to the power inputs with increasing current until *COUT* transitions low. Decrease the current until *COUT* transitions high. Measure the battery current, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: Connect all the power inputs together to share the overcurrent.

3.7.3.2 Test Data

Apply a $4.1V$ source to the power inputs with an increasing current until *COUT* transitions low				
Battery	Capture battery current, *COUT, DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A		$5.18A$	$3.5A < I < 5.4A$	Pass
B			$4A < I < 5A$	

Decrease the current from the previous source until *COUT* transitions low				
Battery	Capture battery current, *COUT, DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A	None, see notes	$0A$	$I < 4A$	Pass
B			$I < 4A$	

3.7.3.3 Test Notes

Recovers after charger is removed. Noise is due to floating node after FET is switched to high impedance. Testing battery B on next revision.

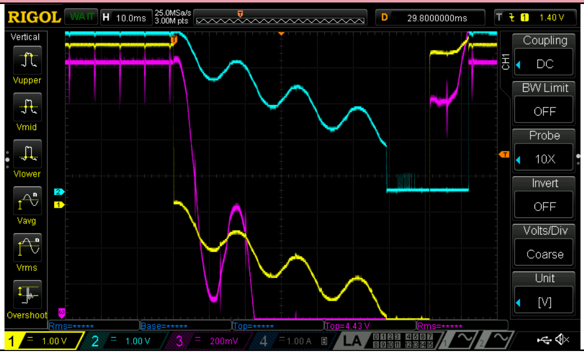
3.7.4 Charge Overvoltage

3.7.4.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. For each battery, apply a $4.1V, 100mA$ source to the umbilical with increasing voltage until *COUT* transitions low. Remove the source and apply a 20Ω resistive load until *COUT* transitions high. Measure the battery voltage, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: The overvoltage protection delay is typically 1.25s

3.7.4.2 Test Data

Apply a $4.1V, 100mA$ source to the umbilical input with an increasing voltage until *COUT* transitions low				
Battery	Capture battery voltage, *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A		$4.277V$	$4.265V < V < 4.285V$	Pass
B			$4.265V < V < 4.285V$	

During overvoltage protection, apply a 20Ω resistive load until *COUT* transitions high				
Battery	Capture battery voltage, *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A	None, see notes	-	$4.145V < V < 4.205V$	Pass
B			$4.145V < V < 4.205V$	

3.7.4.3 Test Notes

Disables charging for $70ms$ then triggers again after $1.22s$. Never remains low, likely due to the narrow hysteresis and use of power supply in place of a real battery. Ripple is due to floating net once FET is switched to high impedance. Testing battery B on next revision.

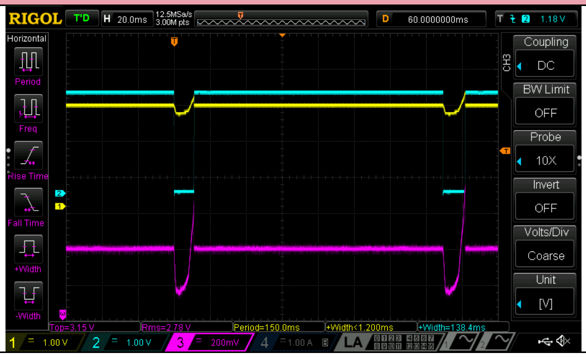
3.7.5 Discharge Undervoltage

3.7.5.1 Test Instructions

Discharge or charge the batteries to $3.0V$ before executing this test. For each battery, apply a 20Ω resistive load to *VBATT* until *DOUT* transitions low. Remove the load and apply a $4.1V, 100mA$ source to the umbilical input until *DOUT* transitions high. Measure the battery voltage, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: The undervoltage protection delay is typically 144ms

3.7.5.2 Test Data

Apply a 20Ω resistive load to *VBATT* until *DOUT* transitions low				
Battery	Capture battery voltage, *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A		$2.788V$	$2.75V < V < 2.85V$	Pass
B			$2.75V < V < 2.85V$	

During undervoltage protection, apply a $4.1V, 100mA$ source to the umbilical input until *DOUT* transitions high				
Battery	Capture battery voltage, *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A	None, see notes	-	$2.8V < V < 3.0V$	Pass
B			$2.8V < V < 3.0V$	

3.7.5.3 Test Notes

Disables discharging for $12ms$ then triggers again after $138ms$. Never remains low, likely due to the narrow hysteresis and use of power supply in place of a real battery. Testing battery B on next revision.

3.8 3.3V Regulator

Results: Pass
Configuration: Auden

This test evaluates the circuit described in 3.3V Regulation. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Power Team page of the Wiki under Tutorials and Resources

3.8.1 Output Voltage

3.8.1.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. With the RBF pin removed, measure the voltage of each 3.3V regulator under no load and under a $1.5A$ resistive load. Ensure the output switches are configured to the correct regulator.

Note: Measure the DC component with $f < 0.1Hz$

3.8.1.2 Test Data

Measure the voltage of each 3.3V regulator under no load and under a $1.5A$ resistive load				
Regulator	No Load Voltage	$1.5A$ Load Voltage	Passing Criteria	Pass / Fail
A	$3.335V$	$3.231V$	$3.135V < V < 3.465V$	Pass
B	$3.295V$	$3.202V$	$3.135V < V < 3.465V$	Pass

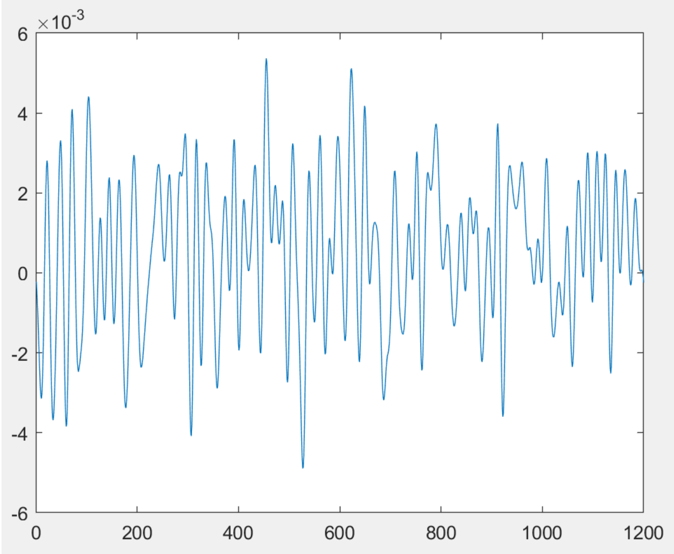
3.8.2 Output Ripple

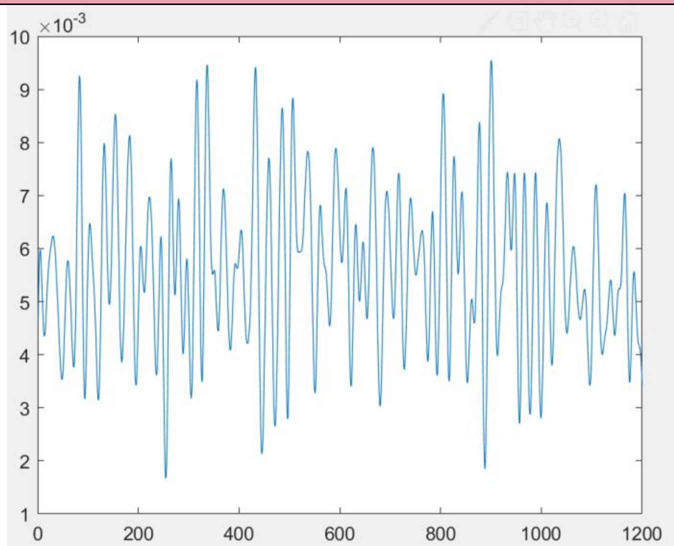
3.8.2.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. With the RBF pin removed, measure the ripple of each 3.3V regulator whilst under a $1.5A$ resistive load.

Note: Measure the RMS value of the AC component with $0.1Hz < f < 100Hz$

3.8.2.2 Test Data

Measure the ripple of each 3.3V regulator whilst under a $1.5A$ resistive load.			
Regulator	Capture the ripple	Passing Criteria	Pass / Fail
A		$\lvert V_{ripple} \rvert < 17mV$	Pass

Measure the ripple of each 3.3V regulator whilst under a $1.5A$ resistive load.			
Regulator	Capture the ripple	Passing Criteria	Pass / Fail
B		$\lvert V_{ripple} \rvert < 17mV$	Pass

3.8.2.3 Test Notes

Used MATLAB to filter the data, see results folder for script and data.

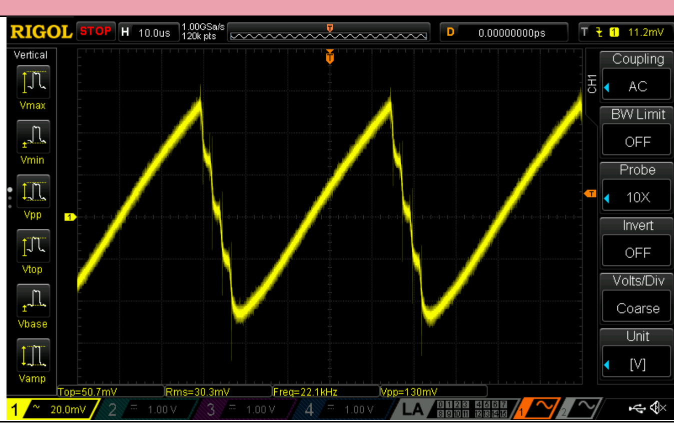
3.8.3 Output Noise

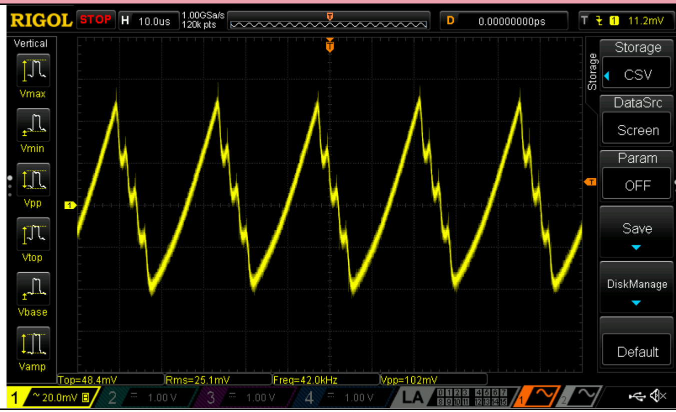
3.8.3.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. With the RBF pin removed, measure the noise of each 3.3V regulator whilst under a $1.5A$ resistive load. Measure at the test point; if the noise is too excessive, measure across the output capacitor.

Note: Measure the RMS value of the AC component with $100Hz < f$

3.8.3.2 Test Data

Measure the noise of each 3.3V regulator whilst under a $1.5A$ resistive load.			
Regulator	Capture the noise	Passing Criteria	Pass / Fail
A		$\lvert V_{noise} \rvert < 33mV$	Pass

Measure the noise of each 3.3V regulator whilst under a $1.5A$ resistive load.			
Regulator	Capture the noise	Passing Criteria	Pass / Fail
B		$\lvert V_{noise} \rvert < 33mV$	Pass

3.8.4 Output Efficiency

3.8.4.1 Test Instructions

Measure the efficiency of 3.3V regulator A whilst under a $10mA$ *to* $2.5A$ resistive loads and with $3.0V$ *to* $4.1V$ input voltage.

Note: $Efficiency = \frac{P_{out}}{P_{in}}$, measure the power across the input and output current shunt resistors.

3.8.4.2 Test Data

Measure the efficiency of 3.3V regulator A whilst under a $10mA$ resistive load and $3.0V$ *to* $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V	$32.1mW$	$31.9mW$	99.5%	$Efficiency > 50\%$	Pass
3.3V	$40.3mW$	$38.1mW$	94.6%	$Efficiency > 50\%$	Pass
3.7V	$41.7mW$	$36.7mW$	88.0%	$Efficiency > 50\%$	Pass
4.1V	$41.4mW$	$37.7mW$	91.1%	$Efficiency > 50\%$	Pass

Measure the efficiency of 3.3V regulator A whilst under a $100mA$ resistive load and $3.0V$ *to* $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V	$318mW$	$312mW$	98.1%	$Efficiency > 70\%$	Pass
3.3V	$381mW$	$368mW$	96.5%	$Efficiency > 70\%$	Pass
3.7V	$396mW$	$373mW$	94.3%	$Efficiency > 70\%$	Pass
4.1V	$399mW$	$372mW$	93.1%	$Efficiency > 70\%$	Pass

Measure the efficiency of 3.3V regulator A whilst under a $300mA$ resistive load and $3.0V$ *to* $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V	$927mW$	$898mW$	96.8%	$Efficiency > 90\%$	Pass
3.3V	$1.14W$	$1.10W$	96.2%	$Efficiency > 90\%$	Pass
3.7V	$1.17W$	$1.09W$	94.3%	$Efficiency > 90\%$	Pass

Measure the efficiency of 3.3V regulator A whilst under a $300mA$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
4.1V	$1.18W$	$1.10W$	93.4%	$Efficiency > 90\%$	Pass

Measure the efficiency of 3.3V regulator A whilst under a $600mA$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V	$1.89W$	$1.83W$	96.4%	$Efficiency > 85\%$	Pass
3.3V	$2.21W$	$2.12W$	96.1%	$Efficiency > 85\%$	Pass
3.7V	$2.31W$	$2.16W$	93.7%	$Efficiency > 85\%$	Pass
4.1V	$2.34W$	$2.18W$	92.9%	$Efficiency > 85\%$	Pass

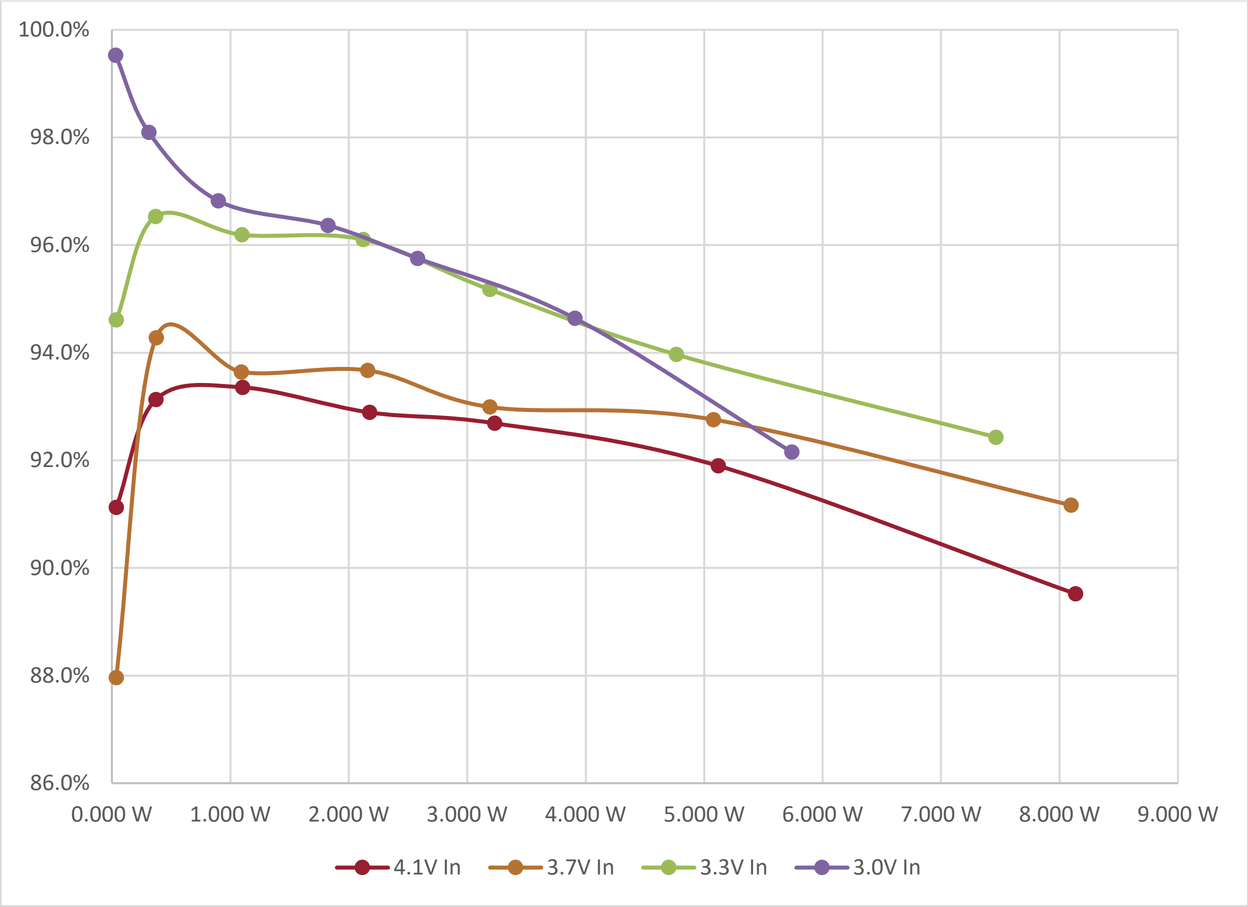
Measure the efficiency of 3.3V regulator A whilst under a $1.0A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V	$2.70W$	$2.58W$	95.8%	$Efficiency > 80\%$	Pass
3.3V	$3.35W$	$3.19W$	95.2%	$Efficiency > 80\%$	Pass
3.7V	$3.43W$	$3.19W$	93.0%	$Efficiency > 80\%$	Pass
4.1V	$3.49W$	$3.23W$	92.7%	$Efficiency > 80\%$	Pass

Measure the efficiency of 3.3V regulator A whilst under a $1.5A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V	$4.13W$	$3.91W$	94.6%	$Efficiency > 75\%$	Pass
3.3V	$5.07W$	$4.77W$	94.0%	$Efficiency > 75\%$	Pass
3.7V	$5.47W$	$5.08W$	92.8%	$Efficiency > 75\%$	Pass
4.1V	$5.57W$	$5.12W$	91.9%	$Efficiency > 75\%$	Pass

Measure the efficiency of 3.3V regulator A whilst under a $2.5A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V	$6.23W$	$5.74W$	92.2%	$Efficiency > 70\%$	Pass
3.3V	$8.08W$	$7.46W$	92.4%	$Efficiency > 70\%$	Pass
3.7V	$8.88W$	$8.10W$	91.2%	$Efficiency > 70\%$	Pass
4.1V	$9.09W$	$8.13W$	89.5%	$Efficiency > 70\%$	Pass

3.8.4.3 Efficiency Plot

Create a plot of current versus efficiency with each input voltage.



3.8.5 Current Limit

3.8.5.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. For each regulator, apply an increasing load to $3.3V$ until the current no longer increases. Measure voltage and current of the rail. Ensure the output switches are configured to the correct battery.

Note: Connect all the power outputs together to share the overcurrent. The load will likely be increased by adding more resistors in parallel or decrease the load resistance. Be sure to not exceed $1A$ per channel.

3.8.5.2 Test Data

Apply an increasing load to $3.3V$ outputs until the current no longer increases			
$3.3V$	Max Current	Passing Criteria	Pass / Fail
A	$4.56A$	$4.5A < I < 6A$	Pass
B	$4.51A$	$4.5A < I < 6A$	Pass

3.9 Load Response - Battery

Results: Pass

Configuration: Auden

This test evaluates the circuit described in Output Switching and Battery & Battery Protection.

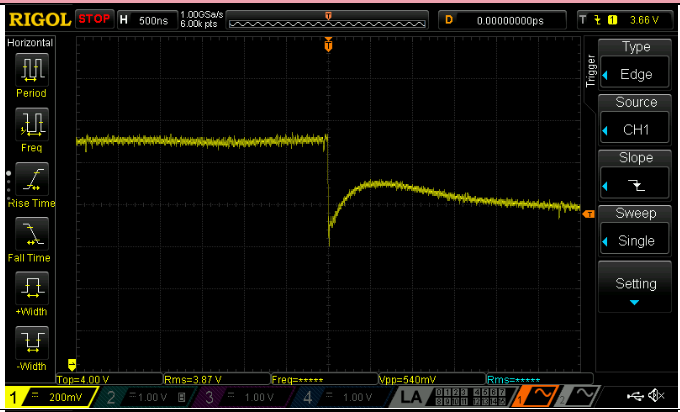
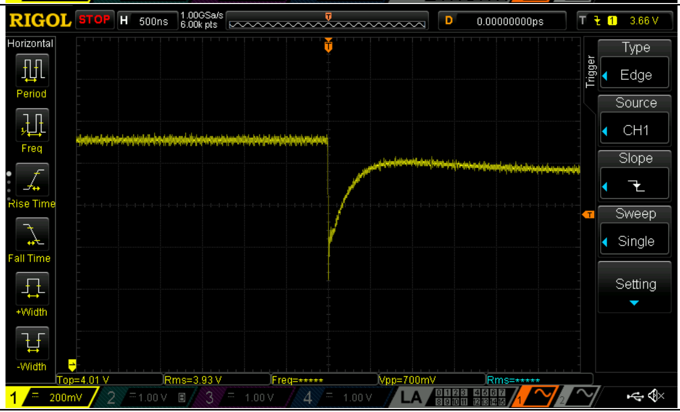
3.9.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Apply the following loads to both *VBATT* rails:

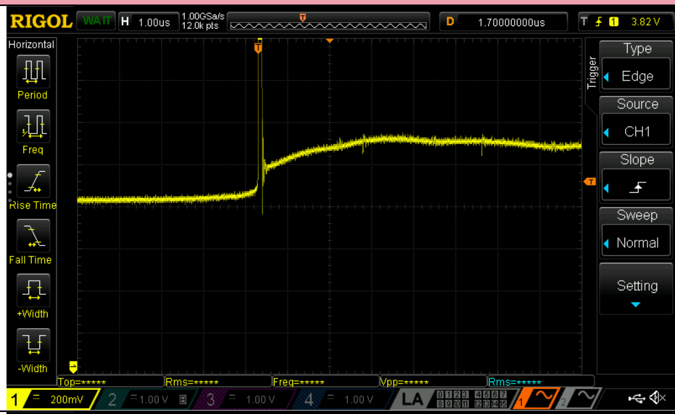
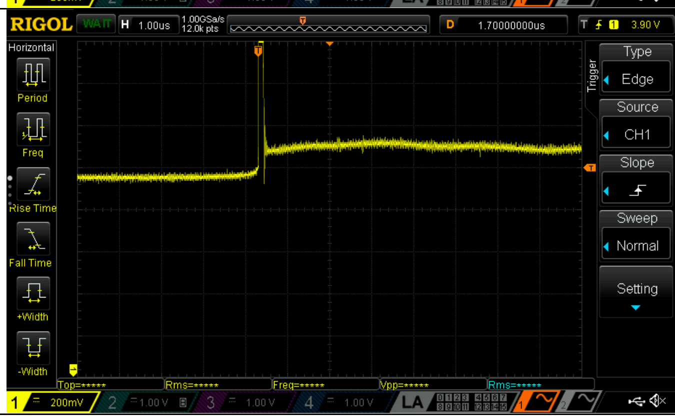
- No load to $1A$ resistive load
- $1A$ resistive load to no load
- No load to $10\mu F$ MLCC[33]
- $1A$ resistive load adding $10\mu F$ MLCC

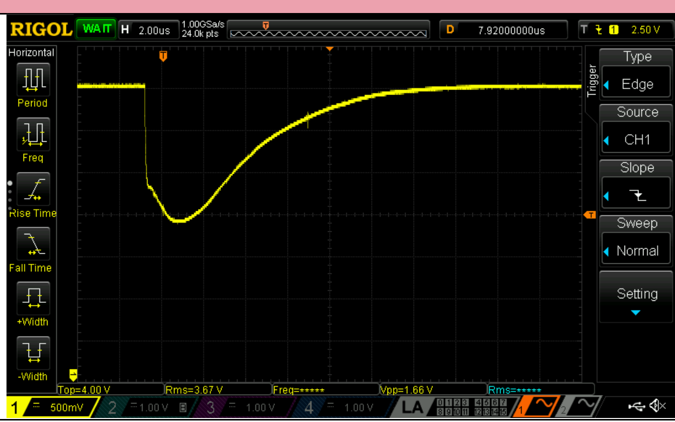
Capture the voltage of the rail under test. Validate the EPS does not misoperate in any way. Ensure the output switches are configured to the correct battery.

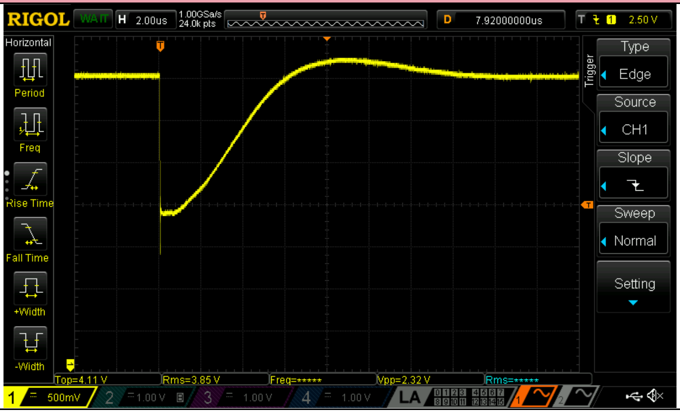
3.9.2 Test Data

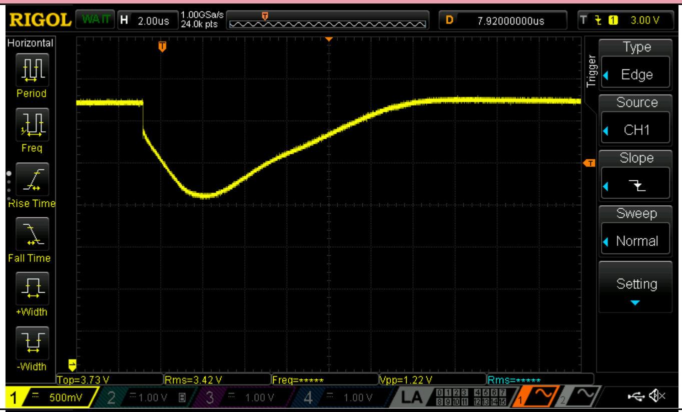
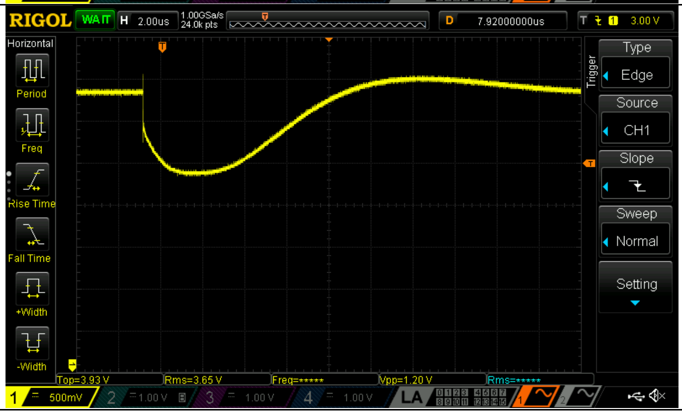
To each *VBATT* rail, apply no load to $1A$ resistive load			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
A		No misoperation	Pass
B		No misoperation	Pass

[33] Multilayer Ceramic Capacitor, CIS PN 13-106A

To each *VBATT* rail, apply $1A$ resistive load to no load			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
A		No misoperation	Pass
B		No misoperation	Pass

To each *VBATT* rail, apply no load to $10\mu F$ MLCC			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
A		No misoperation	Pass

To each *VBATT* rail, apply no load to $10\mu F$ MLCC			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
B		No misoperation	Pass

To each *VBATT* rail, apply $1A$ resistive load and add $10\mu F$ MLCC			
VBATT	Capture voltage of the rail	Passing Criteria	Pass / Fail
A		No misoperation	Pass
B		No misoperation	Pass

3.9.3 Test Notes

Load applied to the corresponding regulator's input capacitor. *VBATT* measured at the switching FET between the battery. This test is passed as there was no misoperation but investigation should be performed to reduce the effect of the $10\mu F$ MLCC load response.

3.10 Load Response – 3.3V Regulator

Results: Pass
Configuration: Auden

This test evaluates the circuit described in Output Switching and 3.3V Regulation.

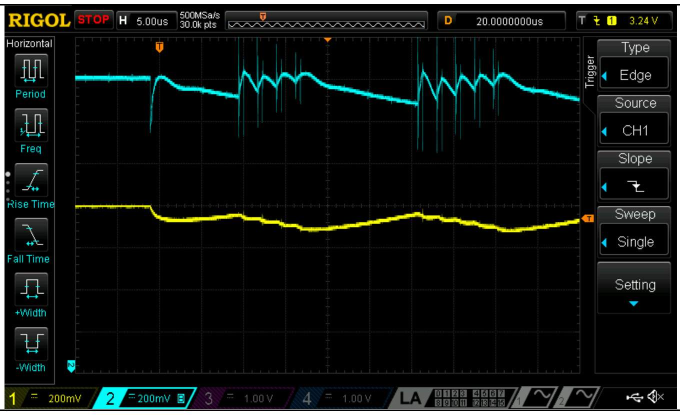
3.10.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Apply the following loads to both *3.3V* rails:

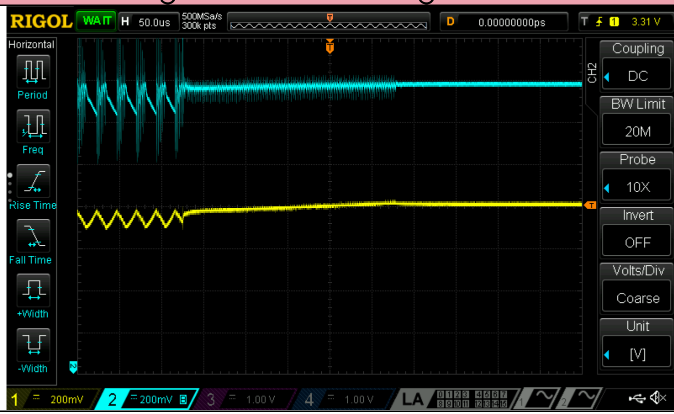
- No load to $1A$ resistive load
- $1A$ resistive load to no load
- No load to $10\mu F$ MLCC
- $1A$ resistive load adding $10\mu F$ MLCC
- No load to short circuit
- Short circuit to no load
- $1A$ resistive load to short circuit
- Short circuit to $1A$ resistive load
- Short circuit continuous

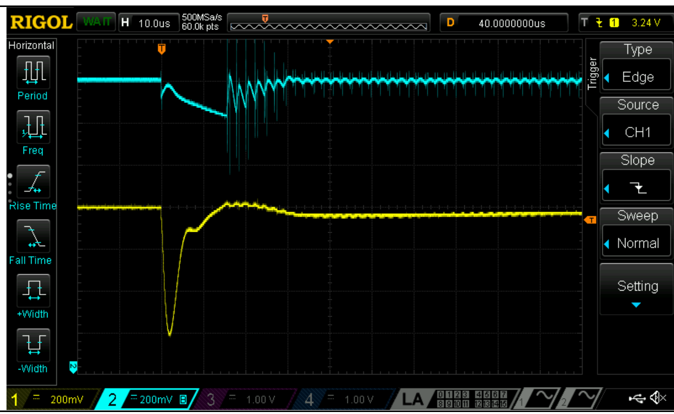
Capture the voltage, and current of the rail under test and the voltage of the sourcing *VBATT* rail. Validate the EPS does not misoperate in any way. Ensure the output switches are configured to the correct battery.

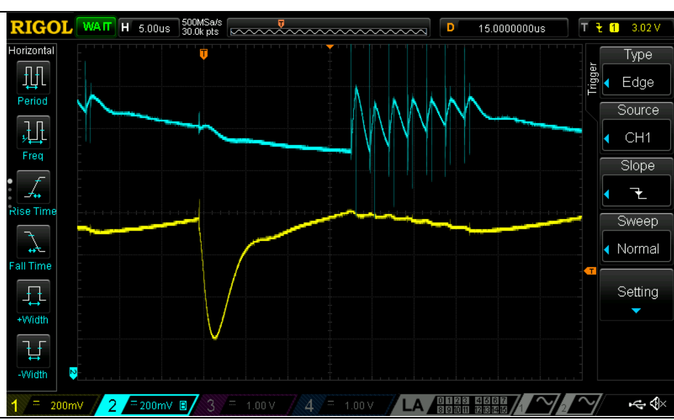
3.10.2 Test Data

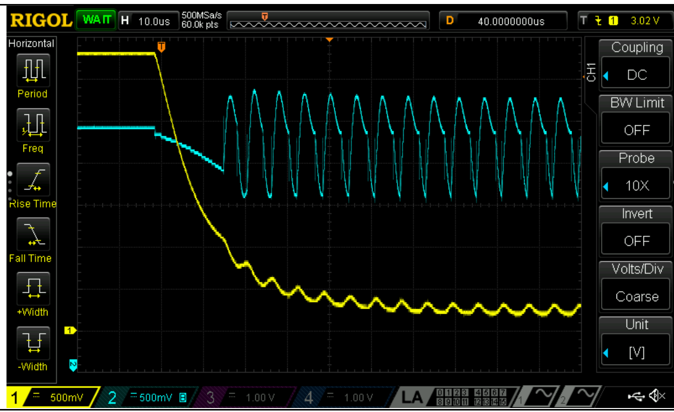
To each *3.3V* rail, apply no load to $1A$ resistive load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	Pass

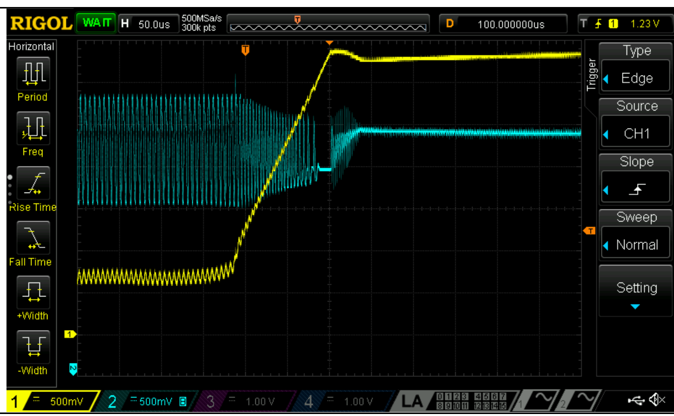
To each *3.3V* rail, apply $1A$ resistive load to no load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	

To each *3.3V* rail, apply $1A$ resistive load to no load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
B		No misoperation	Pass

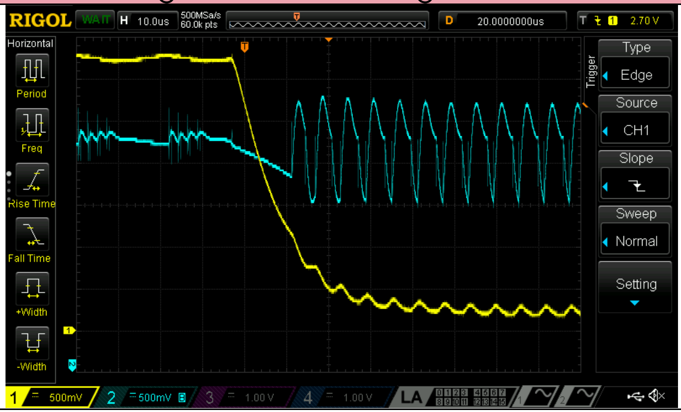
To each *3.3V* rail, apply no load to $10\mu F$ MLCC			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	Pass

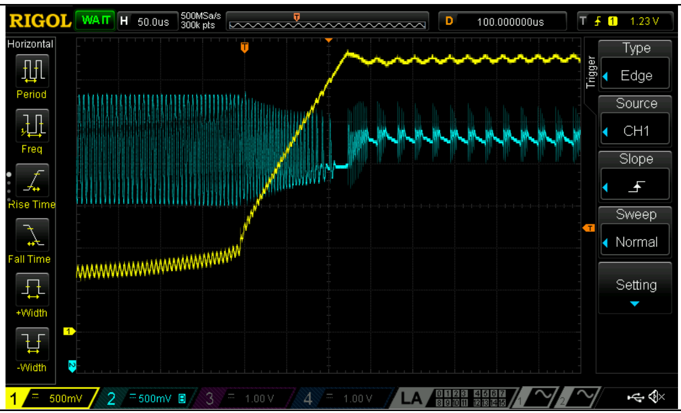
To each *3.3V* rail, apply $1A$ resistive load and add $10\mu F$ MLCC			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	Pass

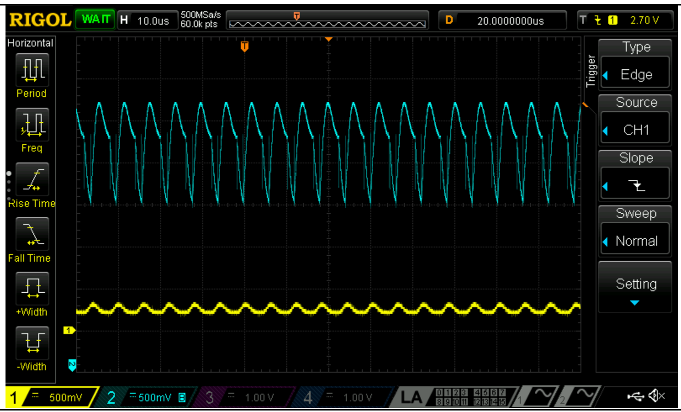
To each *3.3V* rail, apply no load to short circuit			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	Pass

To each *3.3V* rail, apply short circuit to no load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	Pass

To each *3.3V* rail, apply 1*A* resistive load to short circuit			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	

To each *3.3V* rail, apply *1A* resistive load to short circuit			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
B		No misoperation	Pass

To each *3.3V* rail, apply short circuit to *1A* resistive load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	Pass

To each *3.3V* rail, apply short circuit continuous load			
3.3V	Capture voltage and current of the rail and the voltage of the sourcing *VBATT* rail	Passing Criteria	Pass / Fail
A		No misoperation	
B		No misoperation	Pass

3.10.3 Test Notes

Battery A protection was not functioning properly due to a short so its regulator could not be tested. Testing on next revision.

3.11 I²C Bus

Results: Pass
Configuration: Auden

This test evaluates the circuit described in I²C Bus.

3.11.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. At the test points of the *I2C* bus and *BUS_I2C* bus, validate the following timing parameters, see Test Data table for the valid range for each parameter. Refer to Figure 1 for a definition of the timing parameters.

- V_H Logic high level
- V_L Logic low level
- f_{SDA} Clock frequency
- $t_{HD(SDA)}$ Hold time for (repeated) start condition
- t_{LOW} Low period of *SCL*
- t_{HIGH} High period of *SCL*
- $t_{SU(STA)}$ Setup time for a repeated start condition
- $t_{HD(SDA)}$ Data hold time
- $t_{SU(SDA)}$ Data setup time
- t_r Rise time for *SDA*
- t_f Fall time for *SDA*
- $t_{SU(STO)}$ Setup time for stop condition
- t_{BUF} Bus free time between a second start condition

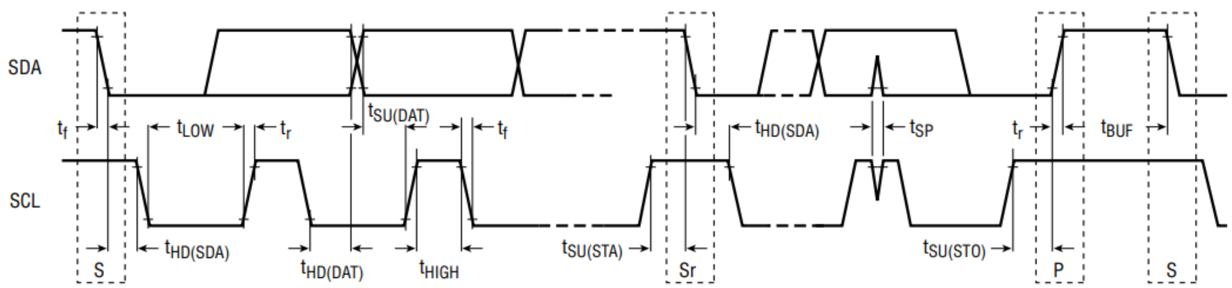


Figure 1: Definition of timing parameters for Fast mode on the I²C bus

Note: The PMIC should generate random I2C traffic on both buses. A slave device might need to be added to *BUS_I2C* to execute this test.

3.11.2 Test Data

At the test points of the *I2C* bus, validate the following timing parameters				
Symbol	Capture the *SDA* and *SCL* lines	Value	Passing Criteria	Pass / Fail
V_H			$V > 2.45V$	
V_L			$V < 990mV$	
f_{SDA}			$f < 400kHz$	
$t_{HD(SDA)}$			$t > 600ns$	
t_{LOW}			$t > 1.3\mu s$	
t_{HIGH}			$t > 600ns$	
$t_{SU(STA)}$			$t > 600ns$	
$t_{HD(SDA)}$			$0 < t < 900ns$	
$t_{SU(SDA)}$			$t > 600ns$	
t_r			$30ns < t < 300ns$	
t_f			$30ns < t < 300ns$	
$t_{SU(STO)}$			$t > 600ns$	
t_{BUF}			$t > 1.3\mu s$	

At the test points of the *BUS_I2C* bus, validate the following timing parameters				
Symbol	Capture the *SDA* and *SCL* lines	Value	Passing Criteria	Pass / Fail
V_H			$V > 2.45V$	
V_L			$V < 990mV$	
f_{SDA}			$f < 400kHz$	
$t_{HD(SDA)}$			$t > 600ns$	
t_{LOW}			$t > 1.3\mu s$	
t_{HIGH}			$t > 600ns$	
$t_{SU(STA)}$			$t > 600ns$	
$t_{HD(SDA)}$			$0 < t < 900ns$	
$t_{SU(SDA)}$			$t > 600ns$	
t_r			$30ns < t < 300ns$	
t_f			$30ns < t < 300ns$	
$t_{SU(STO)}$			$t > 600ns$	
t_{BUF}			$t > 1.3\mu s$	

3.11.3 Test Notes

This was tested but the data was lost. It does work and has successfully been used to communicate with the ADCs.

3.12 Current Monitoring

Results: Fail
Configuration: Auden

This test evaluates the circuit described in Current Monitoring.

3.12.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Apply a $10mA\ to\ 1.0A$ resistive load to a *PR_BATT-0*. Compare the current measured by the EPS and a DMM.

Note: $Error = \frac{|I_{EPS} - I_{DMM}|}{I_{DMM}}$

3.12.2 Test Data

Apply a $10mA\ to\ 1.0A$ resistive load to a single output channel. Compare the current measured by the EPS and a DMM					
Load	EPS Current	DMM Current	Error	Passing Criteria	Pass / Fail
$10mA$				$Error < 1.0\%$	
$25mA$				$Error < 1.0\%$	
$50mA$				$Error < 1.0\%$	
$100mA$				$Error < 1.0\%$	
$250mA$				$Error < 1.0\%$	
$500mA$				$Error < 1.0\%$	
$1.0A$				$Error < 1.0\%$	

3.12.3 Test Notes

Internal ESD diodes short the inputs and cause damage to the ADC. An implementation with series input resistors will be evaluated for the next revision.

3.13 Voltage Monitoring

Results: Pass / Fail
Configuration: Auden

This test evaluates the circuit described in Voltage Monitoring.

3.13.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Compare the voltage measured by the EPS and a DMM on the following signals:

- *UMB_IN*
- *VBATT-A*
- *3.3V-A*

Note: $Error = \frac{|V_{EPS} - V_{DMM}|}{V_{DMM}}$

3.13.2 Test Data

Compare the voltage measured by the EPS and a DMM					
Signal	EPS Voltage	DMM Voltage	Error	Passing Criteria	Pass / Fail
UMB_IN				$Error < 1.0\%$	
VBATT-A				$Error < 1.0\%$	
3.3V-A				$Error < 1.0\%$	

3.13.3 Test Notes
Did not run, see 3.12 Test Notes.

3.14 Temperature Monitoring
Results: Pass / Fail
Configuration: Auden

This test evaluates the circuit described in Temperature Monitoring.

3.14.1 Test Instructions
Discharge or charge the batteries to $3.7V$ before executing this test. Compare the temperature measured by the EPS and a thermometer on the following temperature sensors:

- Battery A
- PMIC
- +X+Y

Note: $Error = |T_{EPS} - T_{THERMOMETER}|$

3.14.2 Test Data

Compare the temperature measured by the EPS and a thermometer					
Sensor	EPS Temperature	Thermometer Temperature	Error	Passing Criteria	Pass / Fail
Battery A				$Error < 2°C$	
PMIC				$Error < 2°C$	
+X+Y				$Error < 2°C$	

3.14.3 Test Notes
Did not run, see 3.12 Test Notes.

3.15 Analog Voltage Reference
Results: Pass
Configuration: Auden

This test evaluates the circuit described in Analog Voltage Reference and Supply. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Power Team page of the Wiki under Tutorials and Resources

3.15.1 *VREF* Voltage

3.15.1.1 Test Instructions
Discharge or charge the batteries to $3.7V$ before executing this test. With the RBF pin removed, measure the voltage of *VREF*.

Note: Measure the DC component with $f < 0.1Hz$

3.15.1.2 Test Data

Measure the voltage of *VREF*		
Voltage	Passing Criteria	Pass / Fail
$1.7996V$	$1.7982V < V < 1.8018V$	Pass

3.15.2 *VREF* Ripple

3.15.2.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the RBF pin removed, measure the ripple of *VREF*.

Note: Measure the RMS value of the AC component with $0.1Hz < f < 100Hz$

3.15.2.2 Test Data

Measure the voltage ripple of *VREF*			
Capture the ripple	Voltage	Passing Criteria	Pass / Fail
Value is less than noise floor	$V < 100\mu V$	$\lvert V_{ripple} \rvert < 180\mu V$	Pass

3.15.2.3 Test Notes

DMM on AC voltage mode measured $0.0000mV$

3.15.3 *VREF* Noise

3.15.3.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the RBF pin removed, measure the noise of *VREF*.

Note: Measure the RMS value of the AC component with $100Hz < f$

3.15.3.2 Test Data

Measure the voltage noise of *VREF*			
Capture the noise	Voltage	Passing Criteria	Pass / Fail
Value is less than noise floor	$V < 100\mu V$	$\lvert V_{noise} \rvert < 90\mu V$	Pass

3.15.3.3 Test Notes

DMM on AC voltage mode measured $0.0000mV$

3.16 PMIC Programming

Results: Pass
Configuration: Auden

This test evaluates the circuit described in Programming Connections.

3.16.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Connect a SWD programmer to the SWD header and upload an image, validate the PMIC is properly programmed. Connect a JTAG programmer to the backplane and upload an image, validate the PMIC is properly programmed.

Note: Follow the programming instructions on the wiki.

3.16.2 Test Data

Program the PMIC via SWD and JTAG, validate the PMIC is properly programmed		
Programmer	Passing Criteria	Pass / Fail
SWD	PMIC properly programmed	Pass
JTAG	PMIC properly programmed	

3.16.3 Test Notes

Requires a $32kHz$ clock and a $8MHz$ clock to be connected for the program to boot. Did not have a JTAG programmer to test JTAG programming.