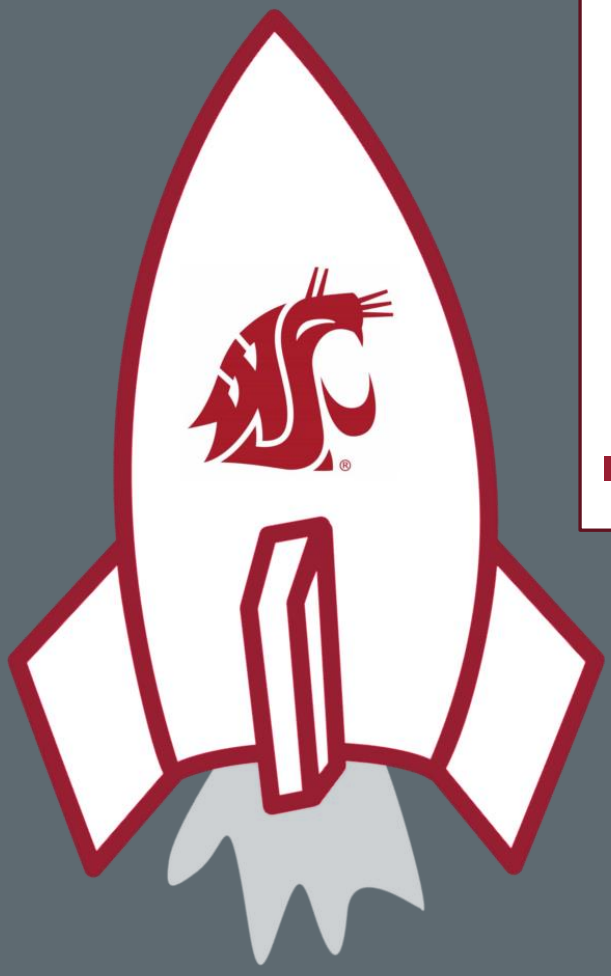
This document explains the function of the Backplane, its schematic level design, and its board level design

Backplane

Backplane Design

Revision: 1.0.1



Bradley Davis

Table of Contents

1 Introduction

This document explains how the Backplane will fulfil the following functions and conform to the following requirements. This document refers to the Backplane version 2.1.

1.1 Function

The Backplane connects all of the subsystems of the satellite together via a parallel bus and interchangeable cards.

1.2 Requirements

The system requirements can be found here[1]

[1] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1/CougSat1-Requirements.xlsx

2 Detailed Description

This section references the Backplane schematic[2]. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Card Slots

The Backplane has eight slots connected in parallel. Each slot is electrically identical. Any card is compatible with every slot.

2.1.2 Separation Switch

The separation switch connects via a connector to the Backplane.

2.2 Schematic

2.2.1 Isolated Grounds

On page 2 of the schematic (D1), are the two isolated grounds found on the Backplane. Power ground *(PGND)* is directly connected to the card. The other grounds are shorted to *PGND* using a 0Ω resistor rated up to $2A$, the expected current is less than $50mA$ each. Chassis ground *(CHASSIS)* is connected to the conductive mechanical features including bolt holes.

2.2.2 Separation Switching

There are two identical connectors to connect to the separation switches. The CubeSat requirements specify at least one separation switch, either or both connectors can be used. The switch is normal open and shorts to *PGND* when depressed.

2.2.3 Card Connectors

Each card connector is a SODIMM socket with 200 pins. See Table 1 for the pin allocation. Each power rail has four pins in parallel which allows loads rated up to $1A$. Each data signal has two pins in parallel which increases redundancy[3].

Table 1: Pin Allocation

Pins	Pin Name	Description
1: 4	PR_3.3V-0	Power Rail 3.3V - Channel 0
5: 8	PR_3.3V-1	Power Rail 3.3V - Channel 1
9: 12	PR_3.3V-2	Power Rail 3.3V - Channel 2
13: 16	PR_3.3V-3	Power Rail 3.3V - Channel 3
17: 20	PR_3.3V-4	Power Rail 3.3V - Channel 4
21: 24	PR_3.3V-5	Power Rail 3.3V - Channel 5

[2] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-Backplane/Documentation/Backplane.pdf
[3] REQ-009

Pins	Pin Name	Description
25: 28	PR_3.3V-6	Power Rail 3.3V - Channel 6
29: 32	PR_3.3V-7	Power Rail 3.3V - Channel 7
33: 36	PR_3.3V-8	Power Rail 3.3V - Channel 8
37: 40	PR_3.3V-9	Power Rail 3.3V - Channel 9
41: 44	PR_3.3V-10	Power Rail 3.3V - Channel 10
45: 48	PR_3.3V-11	Power Rail 3.3V - Channel 11
49: 52	PR_3.3V-12	Power Rail 3.3V - Channel 12
53: 56	PR_BATT-0	Power Rail Vbatt - Channel 0
57: 60	PR_BATT-1	Power Rail Vbatt - Channel 1
61: 64	PR_BATT-2	Power Rail Vbatt - Channel 2
65: 68	PR_BATT-3	Power Rail Vbatt - Channel 3
69: 72	PR_BATT-4	Power Rail Vbatt - Channel 4
73: 76	PR_BATT-5	Power Rail Vbatt - Channel 5
77: 80	PR_BATT-6	Power Rail Vbatt - Channel 6
82:184e	GND	Global ground potential. Includes only the even pins from 82 to 184
161, 163	PWR_CTRL_SW	Disconnects battery (active low), driven by deployment switch OR RBF pin
171, 175	BUS_I2C0_SDA	I2C interfaces for bidirectional data exchange among high priority devices
177, 179	BUS_I2C0_SCL	
181, 183	BUS_I2C0_IRQ	
121, 123	BUS_I2C1_SDA	I2C interfaces for bidirectional data exchange among low priority devices
125, 127	BUS_I2C1_SCL	
129, 131	BUS_I2C1_IRQ	
149, 151	BUS_SPI_SCK	SPI interface to subsystem or direct access to remote serial device
153, 155	BUS_SPI_MISO	
157, 159	BUS_SPI_MOSI	
165, 167	CTRL_RESET	Global reset (active low), *normal high*
169, 171	CTRL_SYNC	Global synchronization signal, driven by IHU
133, 135	COM_SPI_SCK	Serial interface for dedicated communication with the Comms
137, 139	COM_SPI_MISO	
141, 143	COM_SPI_MOSI	
145, 147	COM_SPI_CS	
185, 187	BUS_JTAG_TCK	Shared JTAG interface for subsystem software update via IFJR. Max 1 device at a time, normally high impedance
189, 191	BUS_JTAG_TDI	
193, 195	BUS_JTAG_TDO	
197, 199	BUS_JTAG_TMS	
186, 188	BUS_JTAG_EN-0	JTAG_SEL_COMMS
190, 192	BUS_JTAG_EN-1	JTAG_SEL_PMIC
194, 196	BUS_JTAG_EN-2	
198, 200	BUS_JTAG_EN-3	
81, 83	GPIO-0	SPI_EN_CAM0
85, 87	GPIO-1	SPI_EN_CAM1
89, 91	GPIO-2	
93, 95	GPIO-3	
97, 99	GPIO-4	
101, 103	GPIO-5	

Pins	Pin Name	Description
105, 107	GPIO-6	
109, 111	GPIO-7	
113, 115	GPIO-8	
117, 119	GPIO-9	

2.2.4 Mechanical Features

The Backplane mounts to the Structure using two bolts (page 5, D1) and the top and bottom edges. Each of the holes have a capacitor and resistor connecting to power ground which will absorb transients.

2.3 Board

The board shall be double layered with $1\ oz$ copper and ENIG finish.

2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width: $0.16mm$
Vias: $\emptyset 0.3mm$, unlimited count
Separation: $0.16mm$
Length: unlimited

Devices with specific placement and routing considerations are called out on the schematic, see "CAD Note:"

2.3.1.1 Power Channels - PR_3.3V-[0:12], PR_BATT-[0:6]

Trace width: $1.0mm$

2.3.1.2 Power Ground - PGND

Trace width: $6.0mm$

2.3.1.3 Data Lines

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

3 Testing

4 Discussion

5 Appendix