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This document explains the function of the Solar Panel, its schematic level design, and its board level design

Solar Panel

Solar Panel Design

Revision: 1.0.1



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# 1 Introduction

This document explains how the Solar Panel will fulfil the following [functions](#_1.1_Function) and conform to the following [requirements](#_1.2_Requirements). This document refers to the Solar Panel version 2.0.1.

## 1.1 Function

The Solar Panel is responsible for the following:

* Accumulating energy

## 1.2 Requirements

The system requirements and EPS design requirements can be found [here](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-Requirements.pdf)[[1]](#footnote-1)

# 2 Detailed Description – EPS Board

This section references the EPS [schematic](https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-PowerBoard/Documentation/EPS.pdf)[[2]](#footnote-2). Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

## 2.1 Functional Block Diagram

## 2.2 Schematic

## 2.3 Board

The board shall be double layered with copper and ENIG finish.

### 2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width:

Vias: , unlimited count

Separation:

Length: unlimited

Devices with specific placement and routing considerations are called out on the schematic, see “CAD Note:”

#### 2.3.1.1 Solar Panel Inputs – PV\_IN[0:7], PGND

PGND applies to between the solar panel headers and the backplane

Trace width:

#### 2.3.1.2 Umbilical Input – UMB\_IN, PGND

PGND applies to between the umbilical header and the backplane

Trace width:

#### 2.3.1.3 Battery Connections – VIN-[A:B], BP\_VSS-[A:B] , BP\_VSS-I[A:B], VBATT-[A:B], PGND

PGND applies to between the low side battery protection MOSFETs and the backplane.

Trace width:

Vias: five per layer change

#### 2.3.1.4 SMPS Switching Node – 3.3V\_ISENS-[A:B], 3.3V\_REG\_BUCK\_NODE-[A:B]

Trace width:

Vias: No vias

Minimize RF emission

#### 2.3.1.5 SMPS Output – 3.3V\_I-[A:B], 3.3V-[A:B]

The traces can taper down once loads branch off and less than three loads remain.

Trace width:

Vias: three per layer change

#### 2.3.1.6 SMPS Ground – PGND

PGND applies to between the filtering capacitors and the backplane.

Trace width:

#### 2.3.1.7 Rail Output Channels – PR\_3.3V-[0:12], PR\_BATT-[0:6], PR\_BH-[0:1]

Trace width:

#### 2.3.1.8 Deployables Output – PR\_DEPLOY

Trace width:

#### 2.3.1.9 JTAG – JTAG-[TCK, TDI, TDO, TMS], BUS\_JTAG-[TCK, TDI, TDO, TMS]

Length: Each node shall be length matched

Stubs:

#### 2.3.1.10 I2C – I2C\_[SDA, SCL], BUS\_I2C\_[SDA, SCL, IRQ]

Length: Each node shall be length matched

Stubs:

# 3 Testing

## 3.1 3.3V Regulator

# 4 Discussion

# 5 Appendix

1. <https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-Requirements.pdf> [↑](#footnote-ref-1)
2. <https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-PowerBoard/Documentation/EPS.pdf> [↑](#footnote-ref-2)