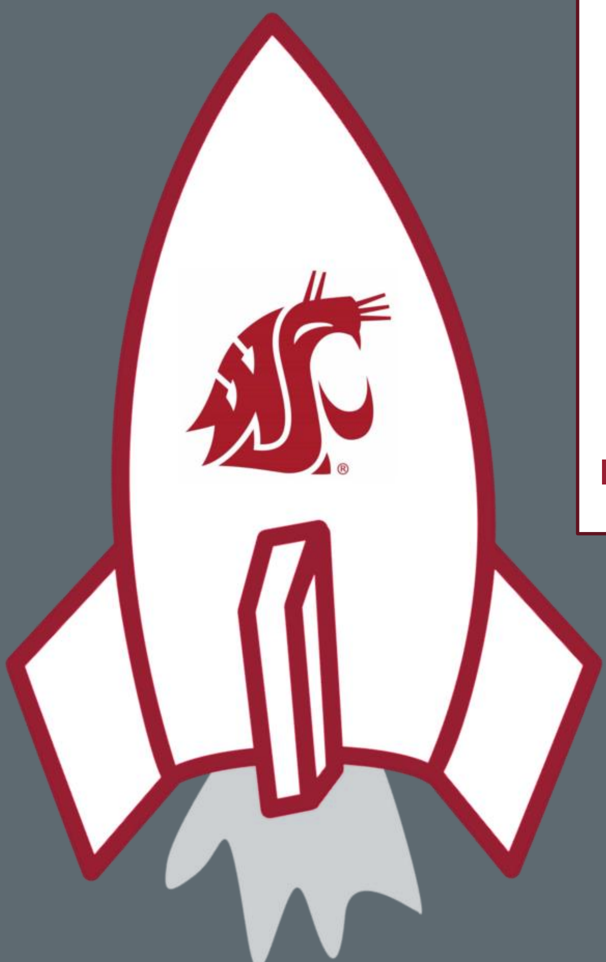
This document explains the function of the EPS, its schematic level design, its board level design, and its functional testing

EPS

Electrical Power Subsystem Design

Revision: 3.1.0



Bradley Davis

Table of Contents

1 Introduction

This document explains how the EPS will fulfil the following Functions and conform to the following Requirements. This document refers to the EPS version 3.1 and Solar Panel version 2.0.

1.1 Function

The Electrical Power Subsystem (EPS) is responsible for the following:

- Accumulating energy
- Regulating voltage
- Distributing power

1.2 Requirements

The system requirements and EPS design requirements can be found on GitHub.

2 Detailed Description

This section references the EPS schematic. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Power Input

Energy is captured from the Sun using an array of photovoltaic cells[1]. These cells are mounted onto solar panels that adjust the voltage and current to acceptable levels for direct charging of lithium-ion batteries[2]. These criteria are up to $4.1V$ and up to $0.5C$[3] per battery. Furthermore, power can be inputted from the umbilical[4] using the same criteria as the solar panels. The umbilical will only be used whilst on the ground. The PMIC will automatically monitor the charging and disable current paths to follow the prescribed charging, see Energy Storage for more details. Most lithium-ion charging curves indicate voltage up to $4.2V$ and current up to $1C$; however, the EPS will limit to $4.1V$ and $0.5C$ to preserve battery health[5]. Replacing the batteries on the EPS whilst in orbit is very difficult.

The solar panel and umbilical inputs are routed through a reverse blocking diode to prevent reverse current from flowing.

2.1.2 Energy Storage

The EPS stores energy from the solar panels in batteries to fulfil high instantaneous power demands and any power demands during periods of eclipse[6]. Each battery has a protection IC that protects against the following faults:

- Overcharge
- Over-discharge
- Charge overcurrent
- Discharge overcurrent
- Load short-circuit detection

The PMIC will monitor and regulate the temperature of the batteries. The batteries (and power inputs) disconnect from the rest of the EPS via separation switches and the RBF switch[7].

[1] Requirement EPS-010
[2] For details on charging lithium-ion batteries, http://batteryuniversity.com/learn/article/charging_lithium_ion_batteries
[3] 1C is equal to the charge of the battery divide by 1 hour (Take the Ah of the battery and drop the "h")
[4] Requirement EPS-021
[5] Requirement REQ-009
[6] Requirements EPS-005, EPS-006, EPS-009
[7] Requirements EPS-020

2.1.3 Power Output

The EPS has two separate rails for distribution: unregulated from the batteries and $3.3V$[8]. There is one regulator[9]. Most loads are connected via the backplane and are individually switched and current monitored[10]. The PMIC controls these turning on and off.

There is a single load that cannot be disconnected from the regulators: the PMIC[11]. This ensures there is at least one processor that can turn on the rest of the satellite. The outputs' default states are off such that the PMIC must turn the loads on, this prevents glitching as the PMIC boots up. The power rail going to the In-Flight JTAG Reprogrammer (IFJR) is logical ORed with *JTAG_EN_PMIC* such that if the IFJR is programming the PMIC, its GPIO goes high impedance but the IFJR remains powered on to avoid corruption.

2.1.4 PMIC

The Power Management IC (PMIC) is the microprocessor monitoring and operating the EPS[12]. Only one PMIC exist as adding redundant processors adds complexity that could reduce reliability. It communicates over I²C to Command and Data Handling subsystem (C&DH)[13] via the backplane and to its monitoring sensors directly. It collects sensor information and transfers this to the C&DH to be included in a telemetry packet to Ground[14]. The C&DH may also send commands. For example, enter safe mode by switching off specific subsystems[15].

2.1.5 Monitoring

The PMIC, through ADCs, monitors current, and voltage at various locations and temperature of various components, indicated on the block diagram[16].

2.2 Schematic

2.2.1 Isolated Grounds

On page 2 of the schematic (D1), are the four isolated grounds found on the EPS. Power ground *(PGND)* is directly connected to the backplane and most of the power chain. The other grounds are shorted to *PGND* using a 0Ω resistor rated up to $2A$, the expected current is less than $50mA$ each. Digital ground *(DGND)* connects to the digital circuity including the PMIC and Monitoring circuits. Analog ground *(AGND)* connects to analog monitoring circuits including the ADCs, their voltage reference, and the thermistors. Chassis ground *(CHASSIS)* is connected to the Mechanical Features including bolt holes and the card rails.

---

[8] Requirement EPS-001
[9] Requirement EPS-008
[10] Requirements EPS-008, EPS-011, EPS-012
[11] Requirements EPS-013
[12] Requirement EPS-022
[13] Requirement EPS-018
[14] Requirement EPS-019
[15] Requirement EPS-014
[16] Requirements EPS-011, EPS-015, EPS-016, EPS-017

2.2.2 Power Rails

Page 2 of the schematic illustrates all the power rails on the EPS. The expected current consumptions are derived from the energy budget. The limit of less than $1A$ per rail is imposed by the backplane via software.

2.2.2.1 Always-On Rail

There is one rail that is always-on and cannot be switched off, except with the Separation Switching. This provide power for the PMIC as the PMIC cannot be allowed to turn off or other subsystems may not be able to be turned on. It is *3.3V* (page 5, B5).

2.2.3 Input Reverse Blocking

A matrix of ideal diodes[17] (page 3) switch the solar panel inputs and umbilical input to the battery. They prevent reverse current from flowing discharging the batteries.

The power inputs are placed in parallel with the batteries such that the loads will draw from the power inputs before drawing from the batteries.

2.2.4 Battery & Battery Protection

The batteries[18] (page 4, B2 & B5) are 18650 lithium-ion. The chemistry was chosen for its high volumetric and mass energy densities. The chosen cells have flight heritage on other CubeSats.

The batteries are protected by dedicated lithium-ion single-cell protection ICs[19] (page 4, B2 & B5). They measure the current passing through the battery by measuring the voltage between pins 4 & 6. With the Rds(on) of the MOSFET[20] and the shunt resistor, the IC prevents against $\frac{90\ to\ 110mV}{(6.4+6.4+10)m\Omega} = \ 4\ to\ 4.8A$ of overcurrent. The IC also prevents against $4.275V$ of over-voltage and $2.800V$ of under-voltage.

The batteries are thermally connected to a heater and Temperature Monitoring thermistor. The heater is a TO-220 10Ω resistor which generates up to $\frac{(3.7V)^2}{10\Omega} \approx 1.4W$ of heat. A lower resistance resistor may be exchanged for more heating capabilities, a thermal test will indicate this need. The heater can be driven at lower duty cycle, through PWM, to reduce the average output power.

2.2.5 Separation Switching

The separation switches isolate the battery pack's positive and negative terminals. All three normal closed switches need to be released to close the circuit connecting the batteries to the EPS. The RBF pin drives a switch driving a FET (page 4, A4) which softly turns off the EPS while the RBF pin is inserted.

---

[17] CIS PN: 60-0015
[18] CIS PN: 01-0002
[19] CIS PN: 60-0006
[20] CIS PN: 56-0005

Connected to the separation switches and RBF pin switch is a capacitor and limiting resistor such that the time constant is $(220\mu F)(158k\Omega) \approx 35s$ buffered with a unity gain buffer[21]. The PMIC measures the voltage across the capacitor. When the PMIC boots up, it will check this voltage is decide if it is powering up after a reset (the capacitor will still be charged) or after a deployment (the capacitor will be discharged).

2.2.6 3.3V Regulation

The 3.3V regulator (page 5) is a switching mode, buck topology. The controller[22] automatically senses the output voltage and adjusts the switching parameters to keep the output at $3.3V$. The controller was chosen for its small package and ability to output 100% duty cycle such that when the input drops below $3.3V$, the output will follow the voltage of the input.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that one was to fail short, they would not compromise the power chain. The small package and tantalum capacitors are not likely to fail due to mechanical vibration.

On the drain of the switching MOSFET (page 5, B3) is a snubber circuit that absorbs and suppresses transients thus reducing the output noise.

The switching MOSFET and inductor (page 5, B3) are thermally connected to a thermistor for Temperature Monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

2.2.7 Output Switching

The output switching (pages 6, 7) uses FETs[23]. The PMIC controls each one individual. All rail's default state is off for when the PMIC is off and not driving the enable signals. Th IFJR's power rail is also (logical OR) enabled when the *JTAG_EN_PMIC* is on as described in Power Input.

Most outputs go into the backplane for distribution to their connected subsystem. The *PR_DP* output (for releasing deployable mechanisms) and *PV_3.3V* (for the solar panel monitoring circuits) connect to their load via wire harness (page 3).

2.2.8 Current Monitoring

At various locations, the power chain has shunt resistors with current shunt amplifiers[24] connected to ADCs to monitor the current. Those locations are:

- Batteries: charging/discharging (page 4, B2 & B5)
- Power chain input (page 4, B2 & B5)
- 3.3V regulator input (page 5, B3)

[21] CIS PN: 08-0002
[22] CIS PN: 06-0004
[23] CIS PN: 56-0002
[24] CIS PN: 08-0003 and 08-0004

- 3.3V regulator output (page 5, B5)
- Output power rails (pages 6, 7)

The solar panels monitor their own current and the PMIC communicates to them via the wire harness (page 3).

2.2.9 Voltage Monitoring

At various locations, the power chain is probed for the voltage using one of the ADCs. Those locations are:

- Batteries (page 4, B2 & B5)
- 3.3V regulator output (page 5, B6)
- Umbilical input (page 3, C2)

The solar panels monitor their own voltages and the PMIC communicates to them via the wire harness (page 3).

2.2.10 Temperature Monitoring

At various locations, the temperature is monitored using thermistors and one of the ADCs. Those locations are:

- Batteries (page 4, B3 & B4)
- 3.3V regulator switching components (page 5, B4)
- Input switching (page 3, D3)
- Output switching (page 6, D3; page 7, D3)
- PMIC (page 9, C4)
- Various locations of the PCB (page 11, A5:A6)
- Each ADC has an integrated temperature sensor

2.2.11 PMIC

The PMIC (page 9) is a microcontroller from the STM32 low power family[25]. It was chosen for its ease of programming, and low power consumption. Since the PMIC is essentially just controlling GPIO and talking over two I²C Buses and a SPI Bus, the features of higher end processors are not needed.

2.2.11.1 Programming Connections

During testing, the PMIC is programmed via Serial Wire Debug[26] (SWD, page 9, D5). The process of programming is made simple with just a single 6 pin header and a robust software utility. In orbit, the PMIC can be programmed via JTAG[27]. The In-Flight JTAG Reprogrammer (IFJR) connects via the backplane, through a tri-state buffer/logic level converter[28] (page 8, A1:B2). The IFJR can enable or disable the tri-state buffer which essentially disconnects the JTAG interface from

[25] CIS PN: 61-0002
[26] For more details on SWD, https://developer.arm.com/products/system-ip/coresight-debug-and-trace/coresight-architecture/serial-wire-debug
[27] For more details on JTAG, https://en.wikipedia.org/wiki/JTAG
[28] CIS PN: 09-0001

the PMIC (it outputs high impedance), allowing the SWD to program. The logic level conversion feature is not used.

2.2.12 I²C Bus

The PMIC has two I²C buses (page 9). One is for the EPS monitoring and control devices. The other is to communicate with the C&DH. On the EPS bus, the PMIC is the master served by the attached devices. Busses that communicate with devices on different power rails go through a tri-state buffer[29], such that when the device is powered off, its ESD diodes do not hold the bus low preventing communication with the other devices on the bus.

2.2.12.1 ADCs

There are nine ADCs[30] connected to the PMIC, each with eight single-ended inputs. Four are on the EPS (page 11). There is one on each solar panel. The ADC was chosen for its low power, small package, SAR architecture and up to nine addresses. The list of addresses (7b) follow:

- [`0x2C`] EPS-0 (page 11, A2)
- [`0x2E`] EPS-1 (page 11, B2)
- [`0x2F`] EPS-2 (page 11, C2)
- [`0x2B`] EPS-3 (page 11, B5)
- [`0x20`] EPS-4 (page 11, C5)
- [`0x2A`] PV0 (+Z) (page 3, A1)
- [`0x28`] PV1 (-Y) (page 3, A3)
- [`0x22`] PV2 (-X) (page 3, B1)
- [`0x23`] PV3 (+Y) (page 3, B3)

2.2.12.2 Backplane to C&DH

The PMIC is a slave to the C&DH. See the interface document for details.

2.2.13 SPI Bus

The PMIC has one SPI bus (page 9) to communicate with three ADCs[31]. These ADCs have a high bit count for resolution when measuring critical nodes including power chain currents and power chain voltages. Each ADC has its own select pin.

2.2.14 Analog Voltage Reference and Supply

Each ADC has its own analog reference of $2.5V$ with high temperature stability, not requiring a high precision external reference. For the thermistors, they are sourced from this analog reference with a unity gain buffer[32] to allow higher current draw (page 11, B4 & D4).

[29] CIS PN: `09-0001`
[30] CIS PN: `27-0003`
[31] CIS PN: `27-0004`
[32] CIS PN: `08-0002`

The EPS has an analog voltage supply (page 11, D2) which is fed by the always-on *3.3V* rail filtered with a ferrite bead and capacitors. Precision is not required as all ADCs use the precision voltage reference for calibration. This is the source for the analog unity gain buffers and ADCs.

2.2.15 Mechanical Features

The RBF pin holder (page 4, D1) and 3.3V Regulation heatsink (page 5, B1) mount directly to the EPS board using bolts. These holes are conductive and connected directly to *CHASSIS*, see Isolated Grounds. The EPS also slots into the structure using rails[33] which are also conductive and connected directly to chassis ground. Each of the holes have a capacitor and resistor connecting to power ground which will absorb transients.

2.3 Board

The board shall conform to the dimensions specified by the [CougSat Module Standard].

2.3.1 Layer Stack-Up

The board shall be four layered with ENIG finish, see Figure 1. Only through vias shall be used. The external copper weight shall be $35\mu m$ and the internal copper weight shall be $18\mu m$.

Layer	Thickness	Primary Function
1 (top)	$35\mu m$ $(1oz)$	SMD components, signal traces
Prepreg	$200\mu m$	
2	$18\mu m$ $(0.5oz)$	Ground planes
Core	$500\mu m$	
3	$18\mu m$ $(0.5oz)$	Power planes
Prepreg	$200\mu m$	
4 (bottom)	$35\mu m$ $(1oz)$	Signal traces

Figure 1: Stack-Up

2.3.2 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless otherwise specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width: $0.16mm$
Vias: $\emptyset 0.3mm$, unlimited count
Separation: $0.16mm$
Length: unlimited

Devices with specific placement and routing considerations are called out on the schematic, see "CAD Note:"

[33] See backplane documentation for details

2.3.2.1 Solar Panel Inputs – PV_IN[0:3][A:B], PGND

PGND applies to between the solar panel headers and the backplane

Trace width: $0.3mm$ ($0.6mm$ on internal layers)

2.3.2.2 Umbilical Input – UMB_IN, PGND

PGND applies to between the umbilical header and the backplane

Trace width: $0.8mm$ ($1.6mm$ on internal layers)

2.3.2.3 Battery Input – VIN, PGND

PGND applies to between the solar panel headers and the backplane

Trace width: $2.0mm$ ($4.0mm$ on internal layers)

2.3.2.4 Battery Connections – BP_VSS-[A:B], BP_VSS-I[A:B], VBATT-[A:B], PGND

PGND applies to between the low side battery protection MOSFETs and the backplane.

Trace width: $5.5mm$ ($11mm$ on internal layers)

Vias: $\emptyset 0.3mm$ five per layer change

2.3.2.5 SMPS Switching Node – 3.3V_ISENS, 3.3V_REG_BUCK_NODE

Trace width: $3.5mm$

Vias: No vias

Minimize RF emission

2.3.2.6 SMPS Output – 3.3V_I, 3.3V

The traces can taper down once loads branch off and less than three loads remain.

Trace width: $3.5mm$ ($7mm$ on internal layers)

Vias: $\emptyset 0.3mm$ three per layer change

2.3.2.7 SMPS Ground – PGND

PGND applies to between the filtering capacitors and the backplane.

Trace width: $0.8mm$ ($1.6mm$ on internal layers)

2.3.2.8 Rail Output Channels – PR_3.3V-[0:12], PR_BATT-[0:6], PR_BH-[0:1]

Trace width: $0.4mm$ ($0.8mm$ on internal layers)

2.3.2.9 Deployables Output – PR_DP-[0:1]

Trace width: $0.8mm$ ($1.6mm$ on internal layers)

2.3.2.10 JTAG – JTAG-[TCK, TDI, TDO, TMS], BUS_JTAG-[TCK, TDI, TDO, TMS]

Length: Each node shall be length matched $\pm 1.0mm$

Stubs: $< 10.0mm$

2.3.2.11 I^{2}C – I2C_[SDA, SCL], BUS_I2C_[SDA, SCL, IRQ]

Length: Each node shall be length matched $\pm 1.0mm$

Stubs: $< 10.0mm$

3 Testing

All tests shall be performed at room temperature and not under vacuum unless otherwise specified. If any modifications are performed, take note. Include enough information to understand circuit behavior and for others to replicate the results. Include any software written to execute the test and link it in the test notes section. Save all software, waveforms, etc. in a subfolder of the board's test folder for each test[34].

- Waveforms shall be captured whenever appropriate
- Have the event take fill the screen (for fast events, zoom in; for slow events, zoom out)
- Label each channel accurately
- Only have bandwidth limiting if necessary for the test (this applies to the oscilloscope and probe settings)
- If ringing or overshoot occurs, use a ground spring or differential probe

Results location: https://github.com/CougsInSpace/CougSat1-Hardware/tree/master/CougSat1-PowerBoard/Testing/EPS.3.1

Common test instructions can be found on the wiki.

Note: In the following sections, applying a $4.1V, 300mA$ source means to connect a power supply limited to $4.1V$ and $300mA$. The actual voltage and current may be less than this.

3.1 Before First Power-On Check

Configuration: Mr. Fitzgerald

This test is required to be executed before batteries are attached and before any external power is applied to the EPS.

3.1.1 Test Instructions

Measure the resistance of various points in reference to *PGND* located at the backplane. Measure the resistance across each current shunt resistor before installing. This is informational only; the resistance of the current shunt resistor is used to calibrate the Current Monitoring.

Measure low value resistors via a constant current source and voltmeter in a four-wire setup to minimize noise. Measure current limit set resistor via a constant current source through the limiter and a voltmeter on the resistor, this compensates the limiter's gain.

3.1.2 Test Data

Node	Resistance		Node	Resistance
VIN-A	$4.8k\Omega$		*VIN-B*	$4.8k\Omega$
VBATT-A	$3.3k\Omega$		*VBATT-B*	$3.3k\Omega$

[34] For test 3.1, place files in the subfolder *"3.1"* and so on

Node	Resistance		Node	Resistance
VIN	$46k\Omega$		*3.3V*	280Ω
I2C_SCL	$3.3k\Omega$		*I2C_SDA*	$3.3k\Omega$
BUS_I2C_SCL	$4.3k\Omega$		*BUS_I2C_SDA*	$4.3k\Omega$
PV_I2C_SCL	$3.2k\Omega$		*PV_I2C_SDA*	$3.2k\Omega$
BP_VSS-A	$100k\Omega$		*BP_VSS-B*	$100k\Omega$
AVDD	280Ω			

3.2 Separation Switching

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Separation Switching.

3.2.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Insert the RBF pin, wait at least $2min$, remove the RBF pin. Measure *PWR_CTRL_SW, VBATT,* and *EJECT_TIMER_BUF.*

3.2.2 Test Data

Insert the RBF pin, wait at least $2min$, remove the RBF pin.			
Operation	Capture *PWR_CTRL_SW, VBATT,* and *EJECT_TIMER*	Passing Criteria	Pass / Fail
Insertion		*VBATT* fall < $10mV$ within $4s$, *EJECT_TIMER* falls < $500mV$ within $2min$	Pass
Removal		*VBATT* rise > $3V$ within $10ms$, *EJECT_TIMER* rises > $2V$ between $30s$ and $2min$	Pass

3.2.3 Test Notes

Channel 1 is *EJECT_TIMER*, channel 3 is *VBATT-A.*

3.3 Power Rails

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Power Rails.

3.3.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the PMIC not running code, upload a blank image or assert its reset pin, and the RBF pin inserted, apply power to each input one at a time as follows:

- $4.1V, 300mA$ to the solar panel inputs
- $4.1V, 1.0A$ to the umbilical input

Ensure that both batteries are receiving the power.

3.3.2 Test Data

Apply $4.1V, 300mA$ to PV_IN-0A			
Battery	Power	Passing Criteria	Pass / Fail
A	$830mW$	Power > $100mW$	Pass
B	$140mW$	Power > $100mW$	Pass

Apply $4.1V, 300mA$ to PV_IN-0B			
Battery	Power	Passing Criteria	Pass / Fail
A	$830mW$	Power > $100mW$	Pass
B	$140mW$	Power > $100mW$	Pass

Apply $4.1V, 300mA$ to PV_IN-1A			
Battery	Power	Passing Criteria	Pass / Fail
A	$830mW$	Power > $100mW$	Pass
B	$140mW$	Power > $100mW$	Pass

Apply $4.1V, 300mA$ to PV_IN-1B			
Battery	Power	Passing Criteria	Pass / Fail
A	$830mW$	Power > $100mW$	Pass
B	$140mW$	Power > $100mW$	Pass

Apply $4.1V, 300mA$ to PV_IN-2A			
Battery	Power	Passing Criteria	Pass / Fail
A	$850mW$	Power > $100mW$	Pass
B	$120mW$	Power > $100mW$	Pass

Apply $4.1V, 300mA$ to PV_IN-2B			
Battery	Power	Passing Criteria	Pass / Fail
A	$850mW$	Power > $100mW$	Pass
B	$120mW$	Power > $100mW$	Pass

Apply $4.1V, 300mA$ to PV_IN-3A			
Battery	Power	Passing Criteria	Pass / Fail
A	$850mW$	Power > $100mW$	Pass
B	$120mW$	Power > $100mW$	Pass

Apply $4.1V, 300mA$ to PV_IN-3B			
Battery	Power	Passing Criteria	Pass / Fail
A	$850mW$	Power > $100mW$	Pass
B	$120mW$	Power > $100mW$	Pass

Apply $4.1V, 1A$ to UMB_IN			
Battery	Power	Passing Criteria	Pass / Fail
A	$1970mW$	Power > $400mW$	Pass
B	$1190mW$	Power > $400mW$	Pass

3.4 Output Switching

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Output Switching.

3.4.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. Drive each output switch to the following states while applying a 20Ω resistive load:

- *Off*
- *On*

Note: *PR_BH-[0,1]* already have a 10Ω resistive load and do not need an external load applied.

3.4.2 Test Data

Configure each output channel to *Both Off*. Apply a 20Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PR_3.3V-PV	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-0	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-1	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-2	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-3	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-4	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-5	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-6	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-7	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-8	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-9	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-10	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-11	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_3.3V-12	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_BATT-0	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_BATT-1	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_BATT-2	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_BATT-3	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_BATT-4	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_BATT-5	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_BATT-6	$120mW$	$0mW$	$A + B < 200mW$	Pass
PR_DEPOLY-0	$120mW$	$0mW$	$A + B < 200mW$	Pass

Configure each output channel to *Both Off*. Apply a 20Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PR_DEPOLY-1	$120mW$	$0mW$	$A+B<200mW$	Pass
PR_BH-0	$120mW$	$0mW$	$A+B<200mW$	Pass
PR_BH-1	$120mW$	$0mW$	$A+B<200mW$	Pass

Configure each output channel to *On*. Apply a 20Ω resistive load to the output under test				
Channel	Battery A Power	Battery B Power	Passing Criteria	Pass / Fail
PR_3.3V-PV	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-0	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-1	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-2	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-3	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-4	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-5	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-6	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-7	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-8	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-9	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-10	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-11	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_3.3V-12	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_BATT-0	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_BATT-1	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_BATT-2	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_BATT-3	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_BATT-4	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_BATT-5	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_BATT-6	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_DEPOLY-0	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_DEPOLY-1	$120mW$	$560mW$	$A+B>500mW$	Pass
PR_BH-0	$750mW$	$750mW$	$A+B>750mW$	Pass
PR_BH-1	$750mW$	$750mW$	$A+B>750mW$	Pass

3.4.3 Test Notes

Positive power indicated discharging, the EPS circuits (PMIC and such) were on and consuming power which is the $120mW$ quiessceint load.

3.5 Battery Charging

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Battery & Battery Protection.

3.5.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the PMIC not running code, upload a blank image or assert its reset pin, and the RBF pin inserted, apply a $4.1V, 1.0A$ source to the umbilical input. Measure the change in voltage after $30\ minutes$ and validate the battery is charging.

Note: Measure the voltage without the external source applied

3.5.2 Test Data

Apply a $4.1V, 1.0A$ source to the umbilical input Measure the change in voltage after $30\ minutes$					
Battery	Initial Voltage	Final Voltage	ΔV	Passing Criteria	Pass / Fail
A	$3.648V$	$3.735V$	$87mV$	$\Delta V > 20mV$	Pass
B	$3.724V$	$3.797V$	$73mV$	$\Delta V > 20mV$	Pass

3.6 Battery Protection

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Battery & Battery Protection.

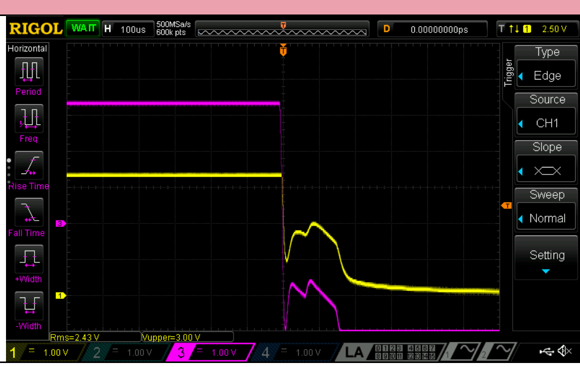
3.6.1 Discharge Overcurrent

3.6.1.1 Test Instructions

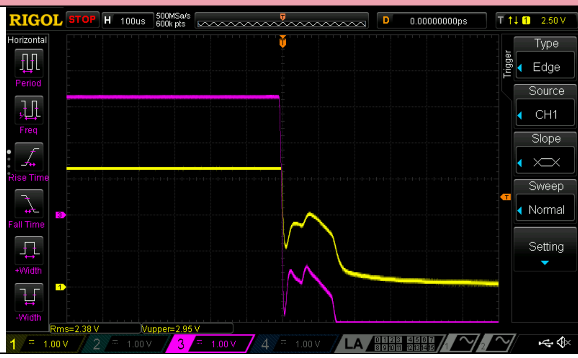
Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply an increasing load to *VBATT* until *DOUT* transitions low. Remove the load and attach the charger. Measure *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

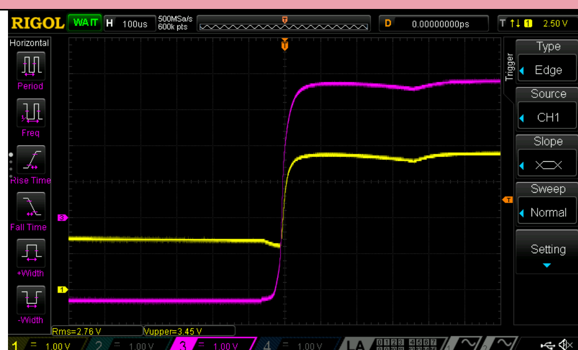
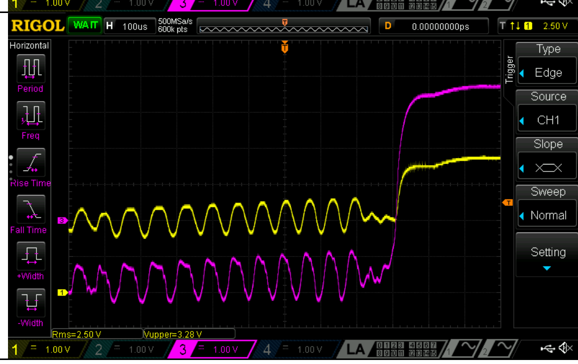
Note: Connect all the power outputs together to share the overcurrent.

3.6.1.2 Test Data

Apply an increasing load to *PR_BATT* outputs until *DOUT* transitions low				
Battery	Capture *COUT*, *DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A		$4.5A$	$3.5A < I < 5.4A$	Pass

WASHINGTON STATE UNIVERSITY
COUGS IN SPACE

Apply an increasing load to *PR_BATT* outputs until *DOUT* transitions low				
Battery	Capture *COUT, DOUT*	Trigger Current	Passing Criteria	Pass / Fail
B		$4.9A$	$3.5A < I < 5.4A$	Pass

Remove the load and attach the battery charger			
Battery	Capture *COUT, DOUT*	Passing Criteria	Pass / Fail
A		Operation Restored	Pass
B		Operation Restored	Pass

3.6.1.3 Test Notes

Yellow is COUT, purple is DOUT. Since COUT is referenced to PGND and the IC disconnected PGND and battery ground, COUT appears to fall but its ground is rising (note it does not fall a large voltage). This also explains the oscillations.

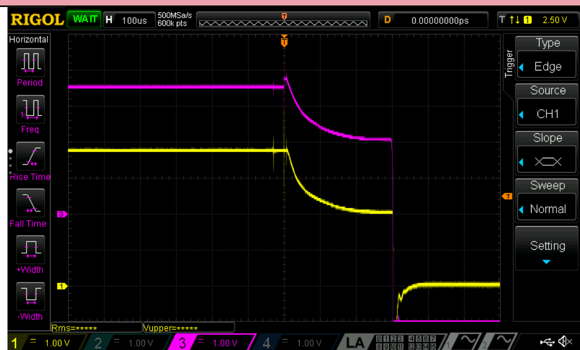
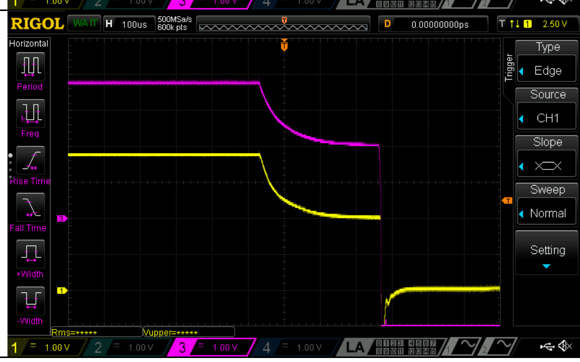
3.6.2 Load Short Circuit

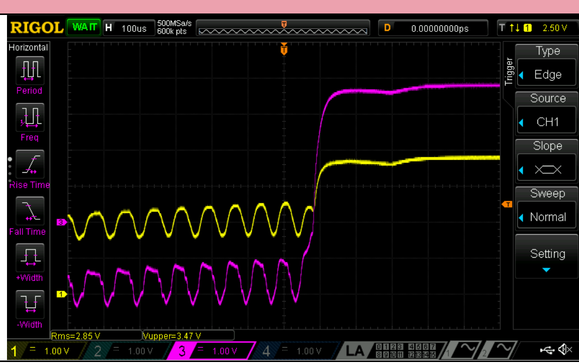
3.6.2.1 Test Instructions

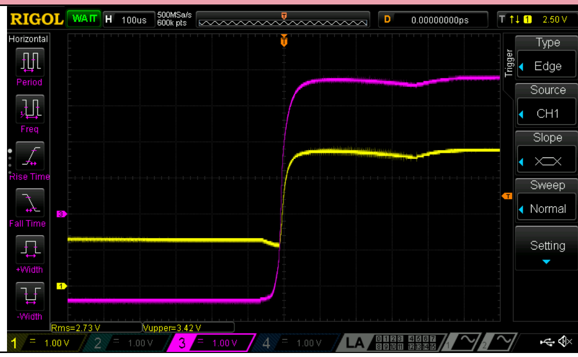
Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply a short between *VBATT* and *PGND*. Remove this short.

Measure *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

3.6.2.2 Test Data

Apply a short between *VBATT* and *PGND*				
Battery	Capture *COUT*, *DOUT*	Trigger Delay	Passing Criteria	Pass / Fail
A		$300\mu s$	$125\mu s < t < 375\mu s$	Pass
B		$350\mu s$	$125\mu s < t < 375\mu s$	Pass

Remove the load and attach the battery charger			
Battery	Capture *COUT*, *DOUT*	Passing Criteria	Pass / Fail
A		Operation Restored	Pass

Remove the load and attach the battery charger			
Battery	Capture *COUT, DOUT*	Passing Criteria	Pass / Fail
B		Operation Restored	Pass

3.6.2.3 Test Notes

Yellow is COUT, purple is DOUT. Since COUT is referenced to PGND and the IC disconnected PGND and battery ground, COUT appears to fall but its ground is rising (note it does not fall a large voltage). This also explains the oscillations.

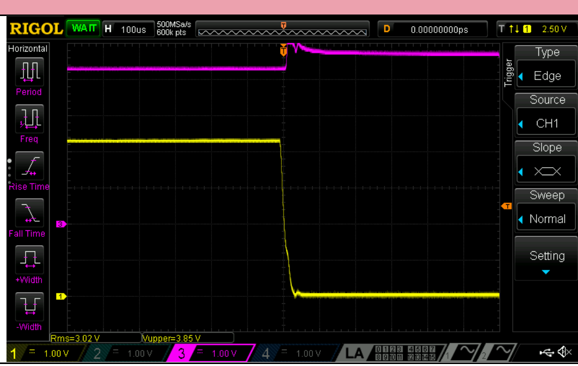
3.6.3 Charge Overcurrent

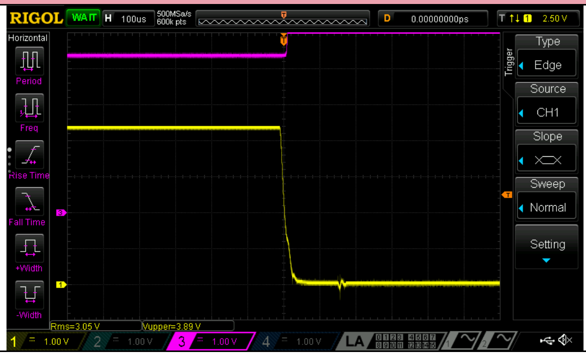
3.6.3.1 Test Instructions

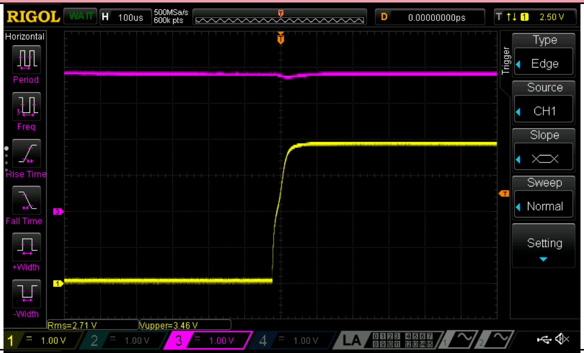
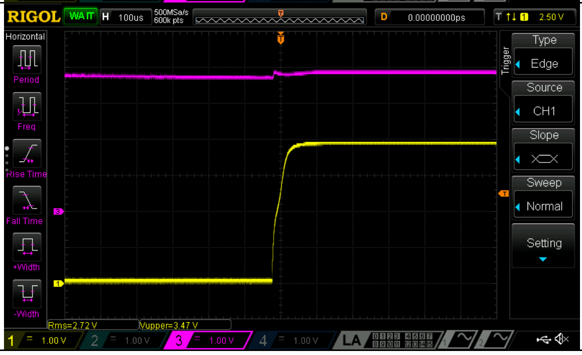
Discharge or charge the batteries to $3.7V$ before executing this test. For each battery, apply a $4.1V$ source to the power inputs with increasing current until *COUT* transitions low. Decrease the current until *COUT* transitions high. Measure the *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: Connect all the power inputs together to share the overcurrent.

3.6.3.2 Test Data

Apply a $4.1V$ source to the power inputs with an increasing current until *COUT* transitions low				
Battery	Capture *COUT, DOUT*	Trigger Current	Passing Criteria	Pass / Fail
A		$4.7A$	$3A < I < 5A$	Pass

Apply a $4.1V$ source to the power inputs with an increasing current until *COUT* transitions low				
Battery	Capture *COUT*, *DOUT*	Trigger Current	Passing Criteria	Pass / Fail
B		$4.9A$	$3A < I < 5A$	Pass

Remove the battery charger			
Battery	Capture *COUT*, *DOUT*	Passing Criteria	Pass / Fail
A		Operation Restored	Pass
B		Operation Restored	Pass

3.6.3.3 Test Notes

Yellow is COUT, purple is DOUT

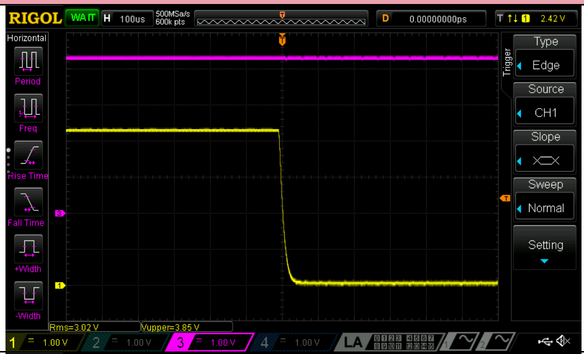
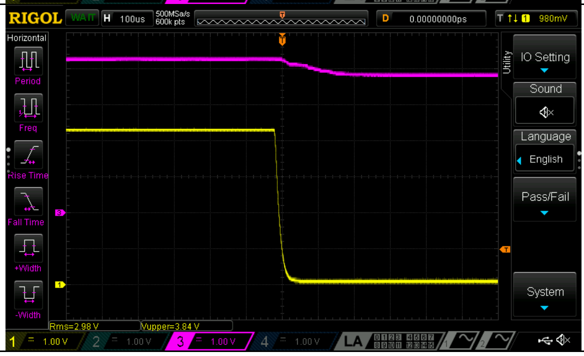
3.6.4 Charge Overvoltage

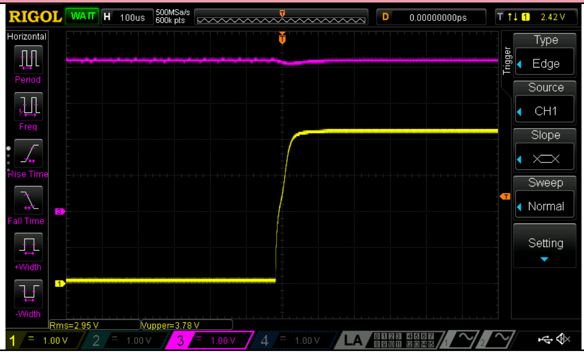
3.6.4.1 Test Instructions

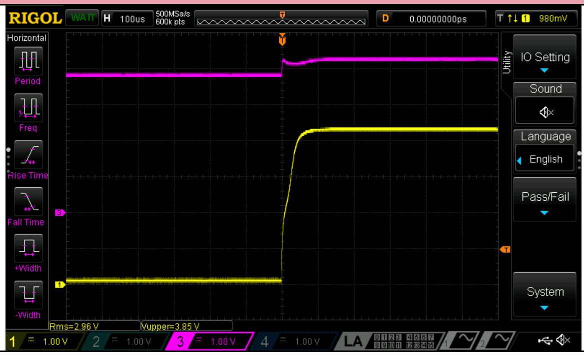
Discharge or charge the batteries to $4.1V$ before executing this test. For each battery, apply a $4.1V, 100mA$ source to the umbilical with increasing voltage until *COUT* transitions low. Remove the source and apply a 20Ω resistive load until *COUT* transitions high. Measure the battery voltage, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: The overvoltage protection delay is typically 1.25s

3.6.4.2 Test Data

Apply a $4.1V, 100mA$ source to the umbilical input with an increasing voltage until *COUT* transitions low				
Battery	Capture *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A		$4.281V$	$4.265V < V < 4.285V$	Pass
B		$4.275V$	$4.265V < V < 4.285V$	Pass

During overvoltage protection, apply a 20Ω resistive load until *COUT* transitions high				
Battery	Capture *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A		$4.189V$	$4.145V < V < 4.205V$	Pass

During overvoltage protection, apply a 20Ω resistive load until *COUT* transitions high				
Battery	Capture *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
B		$4.174V$	$4.145V < V < 4.205V$	Pass

3.6.4.3 Test Notes

Yellow is COUT, purple is DOUT

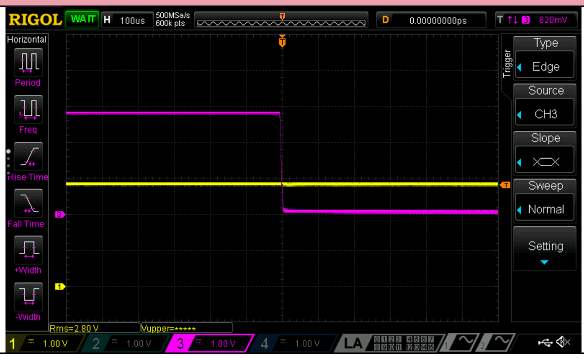
3.6.5 Discharge Undervoltage

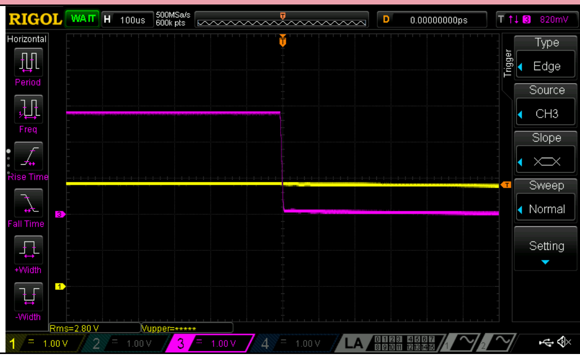
3.6.5.1 Test Instructions

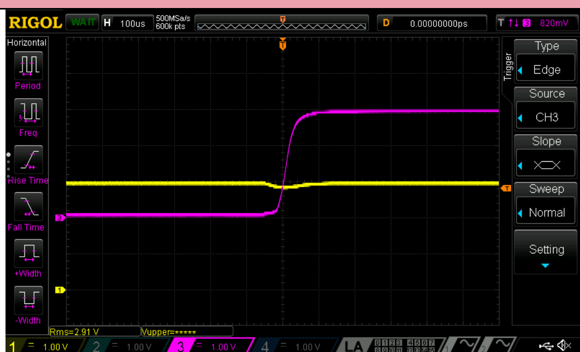
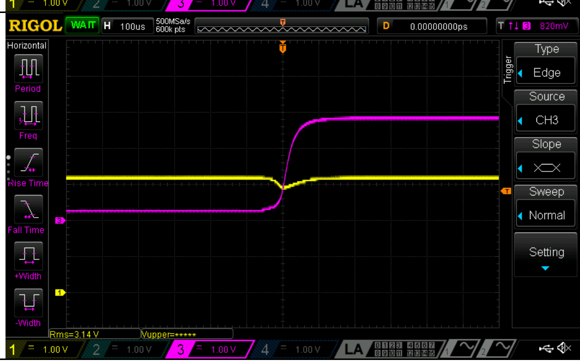
Discharge or charge the batteries to $3.0V$ before executing this test. For each battery, apply a 20Ω resistive load to *VBATT* until *DOUT* transitions low. Remove the load and apply a $4.1V, 100mA$ source to the umbilical input until *DOUT* transitions high. Measure the battery voltage, *COUT*, and *DOUT*. Ensure the output switches are configured to the correct battery.

Note: The undervoltage protection delay is typically 144ms

3.6.5.2 Test Data

Apply a 20Ω resistive load to *VBATT* until D*OUT* transitions low				
Battery	Capture *COUT*, *DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A		$2.79V$	$2.75V < V < 2.85V$	Pass

Apply a 20Ω resistive load to *VBATT* until D*OUT* transitions low				
Battery	Capture *COUT, DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
B		$2.79V$	$2.75V < V < 2.85V$	Pass

During undervoltage protection, apply a $4.1V$, $100mA$ source to the umbilical input until *DOUT* transitions high				
Battery	Capture *COUT, DOUT*	Trigger Voltage	Passing Criteria	Pass / Fail
A		$2.89V$	$2.8V < V < 3.0V$	Pass
B		$2.89V$	$2.8V < V < 3.0V$	Pass

3.6.5.3 Test Notes

Yellow is COUT, purple is DOUT

3.7 3.3V Regulator

Results: Fail
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in 3.3V Regulation. More information on measuring noise/ripple as well as using an oscilloscope can be found on the Power Team page of the Wiki under Tutorials and Resources

3.7.1 Voltage

3.7.1.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. With the RBF pin removed, measure the voltage of the 3.3V regulator under no load and under a $1.5A$ resistive load.

Note: Measure the DC component with PLC[35] > 100

3.7.1.2 Test Data

Measure the voltage of the 3.3V regulator under no load and under a $1.5A$ resistive load			
No Load Voltage	$1.5A$ Load Voltage	Passing Criteria	Pass / Fail
$3.286V$	$3.262V$	$3.135V < V < 3.465V$	Pass

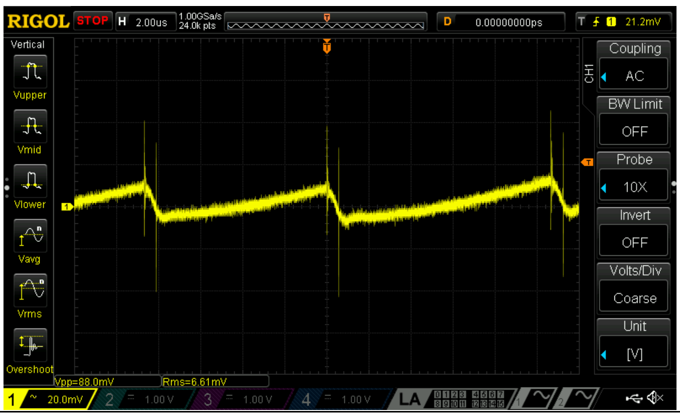
3.7.2 Ripple and Noise

3.7.2.1 Test Instructions

Discharge or charge the batteries to $4.1V$ before executing this test. With the RBF pin removed, measure the ripple of the 3.3V regulator whilst under a $1.5A$ resistive load.

Note: Measure the RMS value of the AC component with $3Hz < f$

3.7.2.2 Test Data

Measure the RMS voltage ripple and noise of the 3.3V regulator whilst under a $1.5A$ resistive load.		
Capture the ripple	Passing Criteria	Pass / Fail
DMM: $4.7mV$ 	$\lvert V_{ripple} \rvert < 17mV$	

[35] Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

3.7.3 Efficiency

3.7.3.1 Test Instructions

Measure the efficiency of 3.3V regulator whilst under a $10mA\ to\ 2.5A$ resistive loads and with $3.0V\ to\ 4.1V$ input voltage.

Note: $Efficiency = \frac{P_{out}}{P_{in}}$, measure the power across the input and output current shunt resistors.

3.7.3.2 Test Data

Measure the efficiency of 3.3V regulator whilst under a $10mA$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 50\%$	
3.3V				$Efficiency > 50\%$	
3.7V				$Efficiency > 50\%$	
4.1V				$Efficiency > 50\%$	

Measure the efficiency of 3.3V regulator whilst under a $100mA$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 70\%$	
3.3V				$Efficiency > 70\%$	
3.7V				$Efficiency > 70\%$	
4.1V				$Efficiency > 70\%$	

Measure the efficiency of 3.3V regulator whilst under a $300mA$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 90\%$	
3.3V				$Efficiency > 90\%$	
3.7V				$Efficiency > 90\%$	
4.1V				$Efficiency > 90\%$	

Measure the efficiency of 3.3V regulator whilst under a $600mA$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 85\%$	
3.3V				$Efficiency > 85\%$	
3.7V				$Efficiency > 85\%$	
4.1V				$Efficiency > 85\%$	

Measure the efficiency of 3.3V regulator whilst under a $1.0A$ resistive load and $3.0V\ to\ 4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 80\%$	
3.3V				$Efficiency > 80\%$	
3.7V				$Efficiency > 80\%$	

Measure the efficiency of 3.3V regulator whilst under a $1.0A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
4.1V				$Efficiency > 80\%$	

Measure the efficiency of 3.3V regulator whilst under a $1.5A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 75\%$	
3.3V				$Efficiency > 75\%$	
3.7V				$Efficiency > 75\%$	
4.1V				$Efficiency > 75\%$	

Measure the efficiency of 3.3V regulator whilst under a $2.5A$ resistive load and $3.0V$ to $4.1V$ input voltage.					
Input Voltage	Power In	Power Out	Efficiency	Passing Criteria	Pass / Fail
3.0V				$Efficiency > 70\%$	
3.3V				$Efficiency > 70\%$	
3.7V				$Efficiency > 70\%$	
4.1V				$Efficiency > 70\%$	

3.7.3.3 Efficiency Plot

Create a plot of current versus efficiency with each input voltage.

3.7.3.4 Test Notes

The electronic load to do efficiency testing easily is not available. The efficiency of EPS 2.1 (same circuit) passed. The efficiency will be tested on EPS 3.1.

3.7.4 Current Limit

3.7.4.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Apply an increasing load to $3.3V$ until the current no longer increases. Measure voltage and current of the rail.

Note: Connect all the power outputs together to share the overcurrent. The load will likely be increased by adding more resistors in parallel or decrease the load resistance. Be sure to not exceed $1A$ per channel.

3.7.4.2 Test Data

Apply an increasing load to $3.3V$ output until the current no longer increases		
Max Current	Passing Criteria	Pass / Fail
	$4.5A < I < 6A$	

3.7.4.3 Test Notes

The electronic load to do load testing easily is not available. The current limit of EPS 2.1 (same circuit) passed. The current limit will be tested on EPS 3.1.
Furthermore regulator B is breaking on EPS 3.0 which affects the current limit.

3.8 Load Response - Battery

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Output Switching and Battery & Battery Protection.

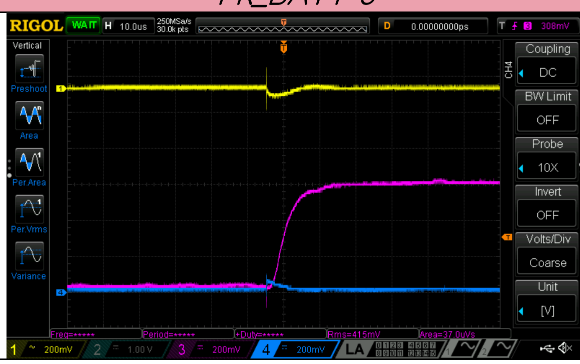
3.8.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Apply the following loads to the *VBATT* rail.

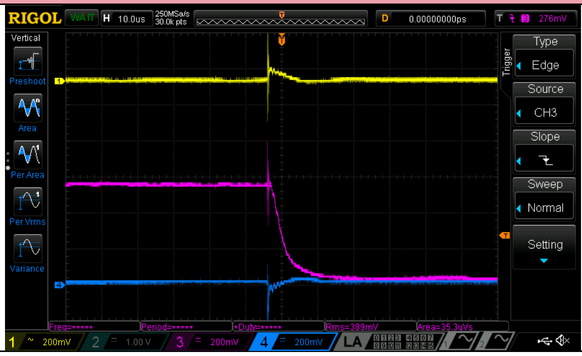
- No load to $1A$ resistive load
- $1A$ resistive load to no load
- No load to $10\mu F$ MLCC[36]
- $1A$ resistive load adding $10\mu F$ MLCC

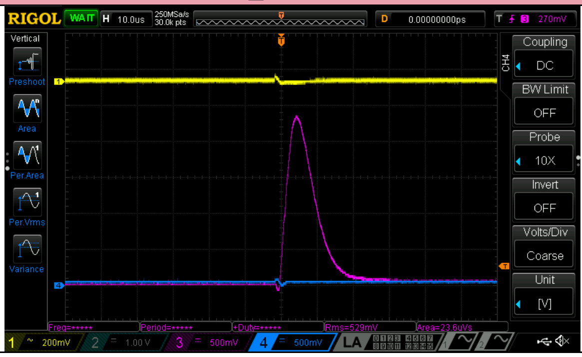
Capture the battery current and the voltage on *PR_BATT-6* with a $10\mu F$ MLCC to simulate a subsystem. Validate the EPS does not misoperate in any way. Ensure the output switches are configured to the correct battery.

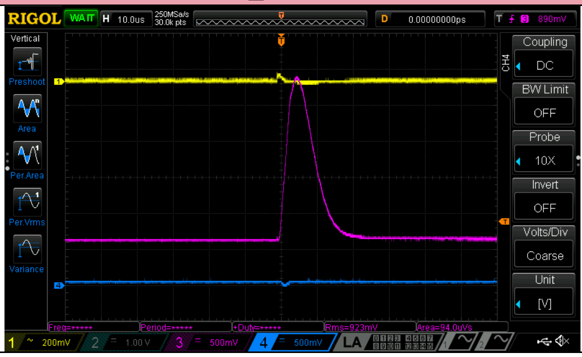
3.8.2 Test Data

To the *VBATT* rail, apply no load to $1A$ resistive load		
Capture current of the battery and the voltage of *PR_BATT-6*	Passing Criteria	Pass / Fail
	No misoperation	Pass

[36] Multilayer Ceramic Capacitor, CIS PN 13-106A

To the *VBATT* rail, apply $1A$ resistive load to no load		
Capture current of the battery and the voltage of *PR_BATT-6*	Passing Criteria	Pass / Fail
	No misoperation	Pass

To the *VBATT* rail, apply no load to $10\mu F$ MLCC		
Capture current of the battery and the voltage of *PR_BATT-6*	Passing Criteria	Pass / Fail
	No misoperation	Pass

To the *VBATT* rail, apply $1A$ resistive load and add $10\mu F$ MLCC		
Capture current of the battery and the voltage of *PR_BATT-6*	Passing Criteria	Pass / Fail
	No misoperation	Pass

3.8.3 Test Notes

Yellow is *PR_BATT-6*, purple is *VBATT-A* current, blue is *VBATT-B* current. $1A = 600mV$.

3.9 Load Response – 3.3V Regulator

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Output Switching and 3.3V Regulation.

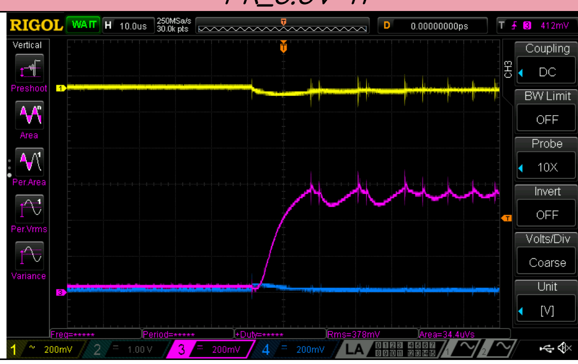
3.9.1 Test Instructions

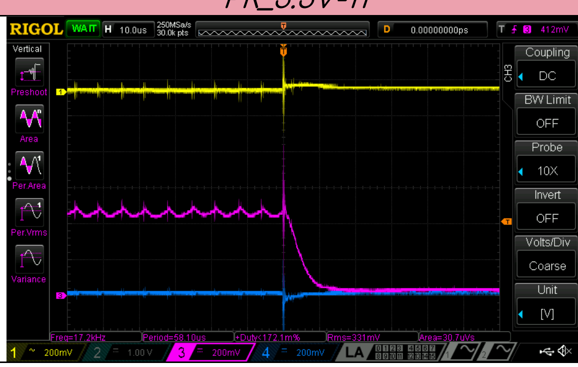
Discharge or charge the batteries to $3.7V$ before executing this test. Apply the following loads to the *3.3V* rail:

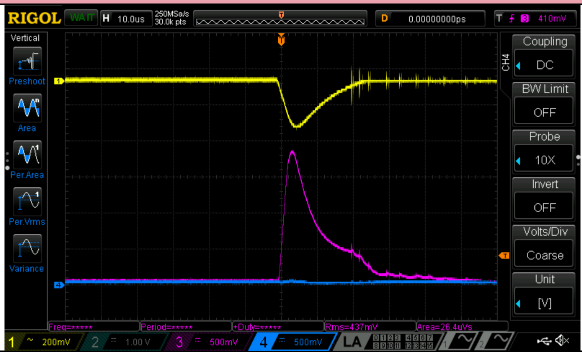
- No load to $1A$ resistive load
- $1A$ resistive load to no load
- No load to $10\mu F$ MLCC
- $1A$ resistive load adding $10\mu F$ MLCC
- No load to short circuit
- Short circuit to no load
- $1A$ resistive load to short circuit
- Short circuit to $1A$ resistive load
- Short circuit continuous

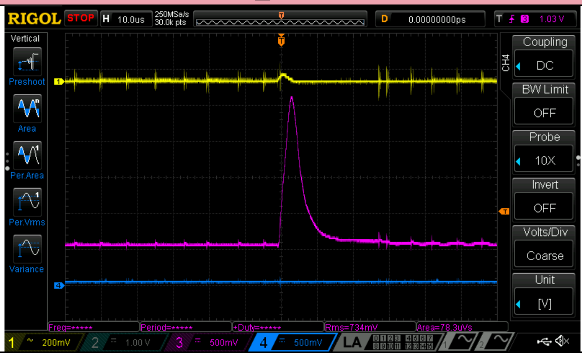
Capture the battery current and the voltage on *PR_3.3V-11* with a $10\mu F$ MLCC to simulate a subsystem. Validate the EPS does not misoperate in any way.

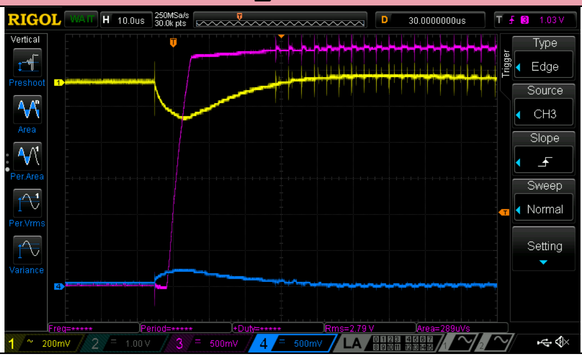
3.9.2 Test Data

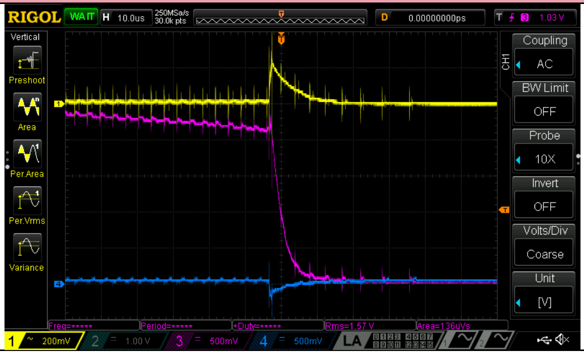
To the *3.3V* rail and *PR_3V3_0*, apply no load to $1A$ resistive load		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

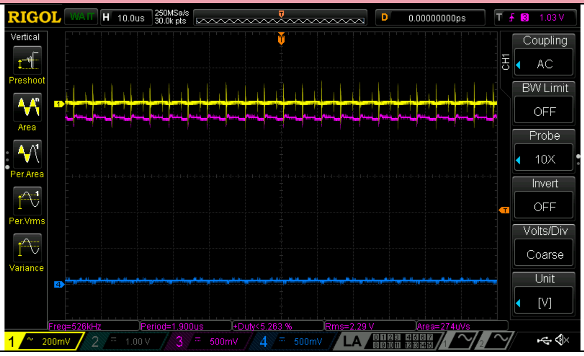
To the *3.3V* rail, apply $1A$ resistive load to no load		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

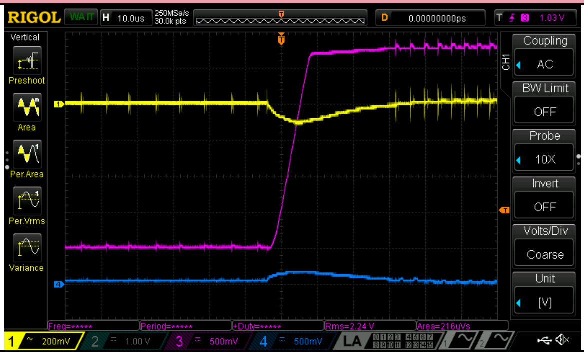
To the *3.3V* rail, apply no load to $10\mu F$ MLCC		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

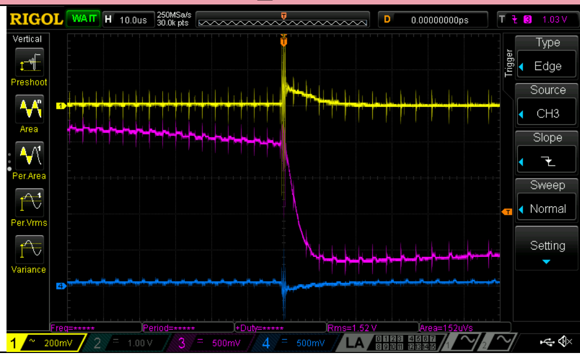
To the *3.3V* rail, apply $1A$ resistive load and add $10\mu F$ MLCC		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

To the *3.3V* rail, apply no load to short circuit		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

To the *3.3V* rail, apply short circuit to no load		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

To the *3.3V* rail, apply short circuit continuous load		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

To the *3.3V* rail, apply 1*A* resistive load to short circuit		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

To the *3.3V* rail, apply short circuit to $1A$ resistive load		
Capture current of the regulator and the voltage of *PR_3.3V-11*	Passing Criteria	Pass / Fail
	No misoperation	Pass

3.9.3 Test Notes

Yellow is *PR_3.3-11*, purple is *3.3V-A* current, blue is *3.3V-B* current. $1A = 600mV$.

3.10 I²C Bus

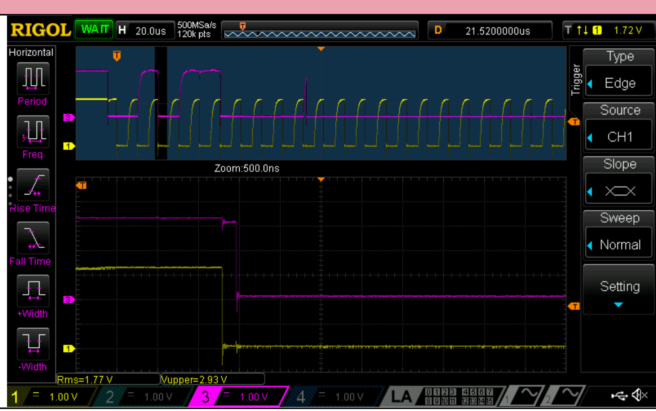
Results: Fail
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in I²C Bus.

3.10.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. At the test points of each I²C bus, validate signal integrity. The PMIC should generate random I²C traffic on each bus. A slave device might need to be added to execute this test.

3.10.2 Test Data

At the test points of the *I2C* bus, validate the following timing parameters			
Bus	Capture the *SDA* and *SCL* lines	Passing Criteria	Pass / Fail
I2C		Signal Integrity	Pass
PV_I2C		Signal Integrity	
BUS_I2C0		Signal Integrity	
BUS_I2C		Signal Integrity	

3.10.3 Test Notes

Other devices on the other busses is not available currently. It will be tested once they become available

3.11 Current Monitoring

Results: Fail
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Current Monitoring.

3.11.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Apply a $10mA\ to\ 1.0A$ resistive load to *PR_DEPLOY-0*. Compare the current measured by the EPS and a DMM.

Note: $Error = \frac{|I_{EPS} - I_{DMM}|}{I_{DMM}}$

3.11.2 Test Data

Apply a $10mA\ to\ 1.0A$ resistive load to *PR_DEPLOY-0*. Compare the current measured by the EPS and a DMM					
Load	EPS Current	DMM Current	Error	Passing Criteria	Pass / Fail
$10mA$				$Error < 1.0\%$	
$25mA$				$Error < 1.0\%$	
$50mA$				$Error < 1.0\%$	
$100mA$				$Error < 1.0\%$	
$250mA$				$Error < 1.0\%$	
$500mA$				$Error < 1.0\%$	
$1.0A$				$Error < 1.0\%$	

3.11.3 Test Notes

The current mirrors in `60-0014` output high impedance and the ADC's input impedance affects its ability to limit current. Every sample brings the node down to zero. This negates the current limiting feature. See the plot below (purple trace) which shows a jump in voltage due to a decrease in impedance.

3.12 Voltage Monitoring

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Voltage Monitoring.

3.12.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Compare the voltage measured by the EPS and a DMM on the following signals:

- *UMB_IN*

- *VBATT-A*
- *3.3V*

Note: $Error = \frac{|V_{EPS} - V_{DMM}|}{V_{DMM}}$

3.12.2 Test Data

Compare the voltage measured by the EPS and a DMM					
Signal	EPS Voltage	DMM Voltage	Error	Passing Criteria	Pass / Fail
UMB_IN	$3.687V$	$3.688V$	$1mV = 0.0\%$	$Error < 1.0\%$	Pass
VBATT-A	$3.667V$	$3.669V$	$2mV = 0.1\%$	$Error < 1.0\%$	Pass
3.3V	$3.281V$	$3.284V$	$3mV = 0.1\%$	$Error < 1.0\%$	Pass

3.13 Temperature Monitoring

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Temperature Monitoring.

3.13.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. Compare the temperature measured by the EPS and a thermometer on the following temperature sensors:

- Battery A
- PMIC
- Regulator

Note: $Error = |T_{EPS} - T_{THERMOMETER}|$

3.13.2 Test Data

Compare the temperature measured by the EPS and a thermometer					
Sensor	EPS Temperature	Thermometer Temperature	Error	Passing Criteria	Pass / Fail
Battery A	$296.7K$	$296.4K$	$0.3K$	$Error < 2°C$	Pass
PMIC	$297.8K$	$297.1K$	$0.7K$	$Error < 2°C$	Pass
Regulator	$297.4K$	$296.5K$	$0.9K$	$Error < 2°C$	Pass

3.14 Analog Voltage Reference

Results: Pass
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Analog Voltage Reference and Supply.

3.14.1 Voltage

3.14.1.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the RBF pin removed, measure the voltage of *VREF*.

Note: Measure the DC component with PLC[37] > 100

3.14.1.2 Test Data

Measure the voltage of each voltage reference				
Signal	Test Point	Voltage	Passing Criteria	Pass / Fail
ADC_REF-0	*TP41*	$2.4996V$	$2.49V < V < 2.51V$	Pass
ADC_REF-1	*TP14*	$2.5025V$	$2.49V < V < 2.51V$	Pass
ADC_REF-2	*TP30*	$2.4995V$	$2.49V < V < 2.51V$	Pass
ADC_REF-3	*TP5*	$2.4970V$	$2.49V < V < 2.51V$	Pass
ADC_REF-4	*TP9*	$2.4972V$	$2.49V < V < 2.51V$	Pass
ADC_REF-5	*TP24*	$2.4915V$	$2.49V < V < 2.51V$	Pass
ADC_REF-6	*TP10*	$2.4974V$	$2.49V < V < 2.51V$	Pass
ADC_REF-7	*TP39*	$2.4955V$	$2.49V < V < 2.51V$	Pass
AVREF-0	*TP13*	$2.4951V$	$2.48V < V < 2.52V$	Pass
AVREF-1	*TP38*	$2.4974V$	$2.48V < V < 2.52V$	Pass

3.14.2 Ripple and Noise

3.14.2.1 Test Instructions

Discharge or charge the batteries to $3.7V$ before executing this test. With the RBF pin removed, measure the ripple of *VREF*.

Note: Measure the RMS value of the AC component with $3Hz < f$

3.14.2.2 Test Data

Measure the RMS voltage ripple and noise of each voltage reference				
Signal	Test Point	Voltage	Passing Criteria	Pass / Fail
ADC_REF-0	*TP41*	$< 100nV$	$\lvert V_{ripple} \rvert < 250\mu V$	Pass
ADC_REF-1	*TP14*	$< 100nV$	$\lvert V_{ripple} \rvert < 250\mu V$	Pass
ADC_REF-2	*TP30*	$< 100nV$	$\lvert V_{ripple} \rvert < 250\mu V$	Pass
ADC_REF-3	*TP5*	$< 100nV$	$\lvert V_{ripple} \rvert < 250\mu V$	Pass
ADC_REF-4	*TP9*	$< 100nV$	$\lvert V_{ripple} \rvert < 250\mu V$	Pass
ADC_REF-5	*TP24*	$< 100nV$	$\lvert V_{ripple} \rvert < 250\mu V$	Pass
ADC_REF-6	*TP10*	$< 100nV$	$\lvert V_{ripple} \rvert < 250\mu V$	Pass
ADC_REF-7	*TP39*	$< 100nV$	$\lvert V_{ripple} \rvert < 250\mu V$	Pass
AVREF-0	*TP13*	$< 100nV$	$\lvert V_{ripple} \rvert < 2.5mV$	Pass
AVREF-1	*TP38*	$< 100nV$	$\lvert V_{ripple} \rvert < 2.5mV$	Pass

[37] Power Line Cycles: DMM setting to average during 100 cycles of the 60Hz wall outlet

3.14.2.3 Test Notes
6 ½ Digit DMM displayed $0.0000mV$ which is $< 100nV$.

3.15 PMIC Programming
Results: Fail
Configuration: Mr. Fitzgerald

This test evaluates the circuit described in Programming Connections.

3.15.1 Test Instructions
Discharge or charge the batteries to $3.7V$ before executing this test. Connect a SWD programmer to the SWD header and upload an image, validate the PMIC is properly programmed. Connect a JTAG programmer to the backplane and upload an image, validate the PMIC is properly programmed.

Note: Follow the programming instructions on the wiki.

3.15.2 Test Data
Program the PMIC via SWD and JTAG, validate the PMIC is properly programmed		
Programmer	Passing Criteria	Pass / Fail
SWD	PMIC properly programmed	Pass
JTAG	PMIC properly programmed	

3.15.3 Test Notes
JTAG programmer is not available right now. JTAG programming will be tested once we have one.