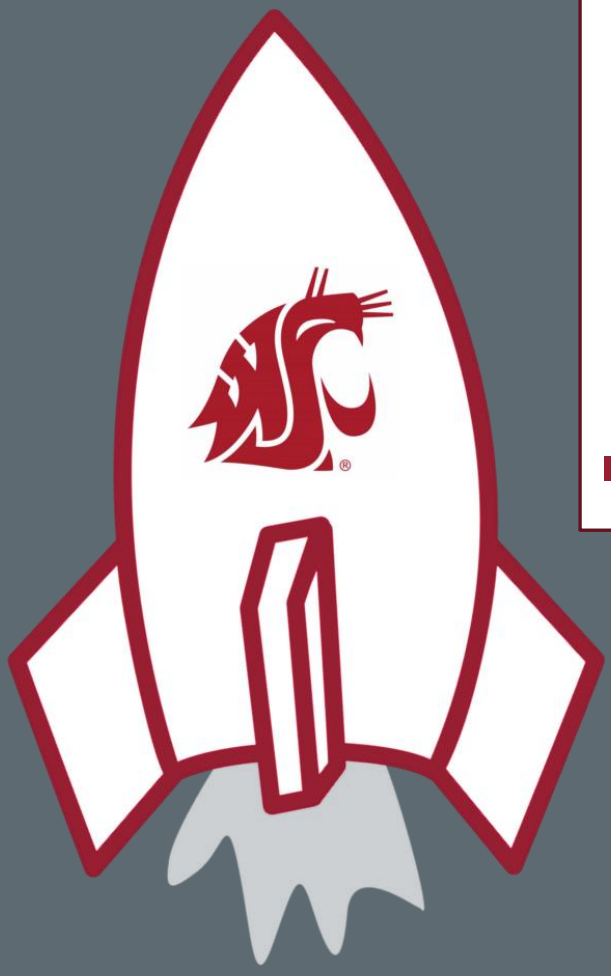
This document explains the function of the EPS, its schematic level design, and its board level design

EPS

Electrical Power Subsystem Design

Revision: 1.0.1



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1 Introduction

This document explains how the EPS will fulfil the following functions and conform to the following requirements. This document refers to the EPS version 2.1 and Solar Panel version 2.0.

1.1 Function

The Electrical Power Subsystem (EPS) is responsible for the following:

- Accumulating energy
- Regulating voltage
- Distributing power

1.2 Requirements

The system requirements and EPS design requirements can be found here[1]

[1] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-Requirements.pdf

2 Detailed Description – EPS Board

This section references the EPS schematic[2]. Page numbers will be listed and may have coordinates listed (number and letter combination found around the frame).

2.1 Functional Block Diagram

The block diagram can be found on the first page of the schematic.

2.1.1 Power Input

Energy is captured from the Sun using an array of photovoltaic cells[3]. These cells are mounted onto solar panels that adjust the voltage and current to acceptable levels for direct charging of lithium-ion batteries[4]. These criteria are up to 4.1V and up to 0.5C[5] per battery. Furthermore, power can be inputted from the umbilical[6] using the same criteria as the solar panels. The umbilical will only be used whilst on the ground. The PMIC will automatically monitor the charging and disable current paths to follow the prescribed charging, see Energy Storage for more details. Most lithium-ion charging curves indicate voltage up to 4.2V and current up to 1C; however, the EPS will limit to 4.1V and 0.5C to preserve battery health[7]. Replacing the batteries on the EPS whilst in orbit is very difficult.

The solar panel and umbilical inputs are routed through a balance switching matrix before entering the batteries. This allows the PMIC to switch every cell going to either or both batteries[8].

2.1.2 Energy Storage

The EPS stores energy from the solar panels in batteries to fulfil high instantaneous power demands and power demands during periods of eclipse[9]. Each battery has a protection IC that protects against the following faults:

- Overcharge
- Over-discharge
- Charge overcurrent
- Discharge overcurrent
- Load short-circuit detection

[2] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-PowerBoard/Documentation/EPS.pdf
[3] Requirement EPS-010
[4] For details on charging lithium-ion batteries, http://batteryuniversity.com/learn/article/charging_lithium_ion_batteries
[5] 1C is equal to the charge of the battery divide by 1 hour (Take the Ah of the battery and drop the "h")
[6] Requirement EPS-021
[7] Requirement REQ-009
[8] Requirement EPS-008
[9] Requirements EPS-005, EPS-006, EPS-009

The PMIC will monitor and regulate the temperature of the batteries. The batteries (and power inputs) disconnect from the rest of the EPS via separation switches and the RBF switch[10].

2.1.3 Power Output

The EPS has two separate rails for distribution: unregulated from the batteries and 3.3V[11]. There are two regulators[12], one per battery. Most loads are connected via the backplane[13] and are individually switched between either source (power chain A or B) or turned off, and current monitored[14]. The PMIC controls these switches.

There is a single load that cannot be disconnected from the regulators: the PMIC[15]. This ensures there is at least one processor that can turn on the rest of the satellite. The outputs also have default states that allow the bus to be on if the PMIC fails to drive the switches.

2.1.4 PMIC

The Power Management IC (PMIC) is the microprocessor monitoring and operating the EPS[16]. Only one PMIC exist as adding redundant processors adds complexity that could reduce reliability. It communicates over I^2C to the Internal Housekeeping Unit (IHU)[17] via the backplane and to its monitoring sensors directly. It collects sensor information and transfers this to the IHU to be included in a telemetry packet to Ground[18]. The IHU may also send commands. For example, enter safe mode by switching off these subsystems[19].

2.1.5 Monitoring

The PMIC, through ADCs, monitors current, and voltage at various locations and temperature of various components, indicated on the block diagram[20].

2.2 Schematic

2.2.1 Isolated Grounds

On page 2 of the schematic (D1), are the four isolated grounds found on the EPS. Power ground *(PGND)* is directly connected to the backplane and most of the power chain. The other grounds are shorted to *PGND* using a 0Ω resistor rated up to $2A$, the

[10] Requirements EPS-020
[11] Requirement EPS-001
[12] Requirement EPS-008
[13] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-Backplane/Documentation/Backplane-Design.pdf
[14] Requirements EPS-008, EPS-011, EPS-012
[15] Requirements EPS-013
[16] Requirement EPS-022
[17] Requirement EPS-018
[18] Requirement EPS-019
[19] Requirement EPS-014
[20] Requirements EPS-011, EPS-015, EPS-016, EPS-017

expected current is less than 50mA each. Digital ground *(DGND)* connects to the digital circuity including the PMIC and monitoring circuits. Analog ground *(AGND)* connects to analog monitoring circuits including the ADCs, their voltage reference, and the thermistors. Chassis ground *(CHASSIS)* is connected to the conductive mechanical features including bolt holes and the card rails.

2.2.2 Power Rails

Page 2 of the schematic illustrates all of the power rails on the EPS. Notice how most components of the power chain can be routed to the other chain to increase redundancy. The expected current consumptions are derived from the energy budget[21]. The limit of $1A$ per rail is imposed by the backplane.

2.2.2.1 Always-On Rails

There are two rails that are always-on and cannot be switched off, except with the separation switching. These provide power for the PMIC as the PMIC cannot be allowed to turn off or other subsystems may not be able to be turned on. They are *VBATT* (page 4, C6), and *3.3V* (page 5, B6 & D6). They use "ideal diodes"[22] to OR the power together from both power chains.

2.2.3 Input Switching

A matrix of MOSFETs (page 3) switch the solar panel inputs and umbilical input to either or both batteries. The P-channel MOSFETs[23] have been chosen for their low Rds(on), sufficient power dissipation by the body, and dual package. The dual package allows for less space used on the PCB which is at a premium on a nanosatellite. They are logic level drive which allows the PMIC to directly control them.

As the GPIO of the PMIC defaults to high impedance input during boot up (every reset will enter this state). The input switches have $10k\Omega$ pull downs (page 8) to choose their default state: all inputs are connected to both batteries and power chains.

The power inputs are placed in parallel with the batteries such that the loads will draw from the power inputs before drawing from the batteries.

2.2.4 Battery & Battery Protection

The batteries (page 4, B2 & B5) are 18650 lithium-ion. The chemistry was chosen for its high volumetric and mass energy densities. A specific cell has not been chosen, a long-term study is required. The EPS will be compatible with most cells.

[21] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-PowerBoard/Documentation/EnergyBudget.pdf
[22] LTC4411, a MOSFET with integrated control circuity to function like a diode
[23] NTLUD3A50PZ

The batteries are protected by dedicated lithium-ion single-cell protection ICs[24] (page 4, B1 & B4). They measure the current passing through the battery by measuring the voltage between pins 4 & 6. With the Rds(on) of the MOSFET[25] and the shunt resistor, the IC prevents against $\frac{90\ to\ 110mV}{(6.4+6.4+10)m\Omega} = \ 4\ to\ 4.8A$ of overcurrent. The IC also prevents against $4.275V$ of over-voltage and $2.800V$ of under-voltage.

The batteries are thermally connected to a heater and thermistor. The heater is a TO-220 10Ω resistor which generates up to $\frac{(3.7V)^2}{10\Omega} \approx 1.4W$ of heat. A lower resistance resistor may be exchanged for more heating capabilities, a thermal test will indicate this need. The heater can be driven at lower duty cycle, through PWM, to reduce the average output power.

2.2.5 Separation Switching

The separation switches (connected via the backplane) or the RBF pin switch (page 4, D2) disconnect the batteries and power input from the rest of the power chain. Either of the switches apply a pull down to the gate of a MOSFET that inverts the signal to another MOSFET that interrupts the power chain. When the umbilical is connected, and voltage is applied, it drives the MOSFETs the opposite way to connect the power chain. In the default state (no switches depressed or umbilical connected) a weak pull up to the batteries (through ORing diodes) keeps the MOSFETS driven to connect the power chain.

Connected to the separation switches and RBF pin switch is a capacitor and limiting resistor such that the time constant is $(1\mu F)(30M\Omega + 100k\Omega + 10k\Omega) \approx 30s$. The PMIC measures the voltage across the capacitor. When the PMIC boots up, it will check this voltage is decide if it is powering up after a reset (the capacitor will still be charged) or after a deployment (the capacitor will be discharged).

2.2.6 3.3V Regulation

The 3.3V regulators (page 5) are switching mode, buck topology. The controller[26] automatically senses the output voltage and adjusts the switching parameters to keep it at 3.3V. The controller was chosen for its small package and ability to output 100% duty cycle such that when the input drops below 3.3V, the output will follow the voltage of the input. The parts used in this circuit have been tested on EPS V2.0 and are working to satisfaction.

The large package Multi-Layer Ceramic Capacitors (MLCC, input and output filtering) are placed in series such that a single one were to fail short, they would not

[24] BQ29700
[25] DMN2008LFU
[26] TPS64200

compromise the power chain. The small package and tantalum capacitors are not likely to fail short.

On the drain of the switching MOSFETs (page 5, A3 & C3) are snubber circuits that absorb and suppress transients thus reducing the output noise.

The switching MOSFETs and inductors (page5, A3 & C3) are thermally connected to a thermistor for temperature monitoring and an optional heatsink if a thermal test indicates they need additional heat dissipation.

2.2.7 Output Switching

The output switching (pages 6, 7) uses the same setup as the input switching. The default cases are as follow: rails connected to bus subsystems default on, rails connected to payloads default off.

Most outputs go into the backplane for distribution to their connected subsystem. The *PR_DEPLOY* output (for releasing deployable mechanisms) and *PV_3.3V* (for the solar panel monitoring circuits) connect to their load via wire harness (page 3, A2:C2).

2.2.8 Current Monitoring

At various locations, the power chain has shunt resistors connected to differential ADCs to monitor the current. Those locations are:

- Batteries charging/discharging (page 4, B2 & B5)
- Power chain input (page 4, A2 & A5)
- 3.3V regulator input (page 5, A3 & C3)
- 3.3V regulator output (page 5, A5 & C5)
- Each output rail (pages 6, 7)

The solar panels monitor their own current and the PMIC communicates to them via the wire harness (page 3, A2: C2).

2.2.9 Voltage Monitoring

At various locations, the power chain is probed for the voltage using a single ended ADC. Those locations are:

- Batteries (page 4, B2 & B5)
- 3.3V regulator output (page 5, A6 & C6)
- Umbilical input (page 3, C2)

The solar panels monitor their own voltages and the PMIC communicates to them via the wire harness (page 3, A2: C2).

2.2.10 Temperature monitoring

At various locations, the temperature is monitored using thermistors and a single ended ADC. Those locations are:

- Batteries (page 4, B2 & B5)
- 3.3V regulator switching components (page 5, A4 & C4)
- Each corner of the PCB (page 11, C5)

2.2.11 PMIC

The PMIC (page 9, B3, A1, A3, & A4) is a microcontroller from the STM32 low power family[27]. It was chosen for its ease of programming, and low power consumption. Since the PMIC is essentially just controlling GPIO and talking over I²C, the features of higher end processors are not needed. There are a total of 72 switch control signals and 10 other signals (programming, I²C, interrupts). Upgrading the processor to the 100 pin variant (from 64 pins) would eliminate the GPIO expanders but would also take up the same if not more PCB area, a premium on a nanosatellite. Furthermore, using I²C expanders reduces routing complexity as not every one of the 72 control signals need to connect all the way to the PMIC.

The PMIC's reset pin is connected to the backplane such that if it or any subsystem needs to reset itself, all of the subsystems reset. This is to put all of the subsystems in a known state which reduces cause for error.

2.2.11.1 Programming Connections

During testing, the PMIC is programmed via Serial Wire Debug[28] (SWD, page 9, B1). The process of programming is made simple with just a single 6 pin header and a robust software utility. In orbit, the PMIC can be programmed vis JTAG[29]. The In-Flight JTAG Reprogrammer[30] connects via the backplane, through a tri-state buffer[31] (page 9, B5 & C5). The IFJR can enable or disable the tri-state buffer which essentially disconnects the JTAG interface from the PMIC (it outputs high impedance), allowing the SWD to program.

2.2.12 I²C Bus

The PMIC has two I²C buses (page 9, A3, & A5). One is for the EPS monitoring and control devices. The other is to communicate with the IHU. On the EPS bus, the PMIC is the master served by the attached devices.

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[27] STM32L476RG
[28] For more details on SWD, https://developer.arm.com/products/system-ip/coresight-debug-and-trace/coresight-architecture/serial-wire-debug
[29] For more details on JTAG, https://en.wikipedia.org/wiki/JTAG
[30] https://github.com/CougsInSpace/CougSat1-Hardware/blob/master/CougSat1-AvionicBoard/Documentation/IFJR-Design.pdf
[31] SN74LVC244AR

2.2.12.1 GPIO Expanders

There are six GPIO expanders[32] connected to the PMIC, each with 16 IO. Two are on the EPS (page 9, C1 & C3). There is one on each solar panel. The expander was chosen for its low power and up to eight addresses. The list of address follow:

- [0x40] EPS-0 (page 9, C1)
- [0x42] EPS-1 (page 9, C5)
- [0x44] PV0 (page 3, A2)
- [0x46] PV1 (page 9, B2)
- [0x48] PV2 (page 9, B2)
- [0x4A] PV3 (page 9, C2)

2.2.12.2 ADCs

There are 10 ADCs[33] connected to the PMIC, each with 16 single-ended inputs or eight differential inputs or a combination. Six are on the EPS (page 10, A2, A4, C2, & C4; page 11, A2 & C2). There is one on each solar panel. The ADC was chosen for its low power, differential inputs, small package, and up to 27 addresses. The list of address follow:

- [0xEE] Global ADC address
- [0x28] EPS-0 (page 10, A2), current only
- [0x2A] EPS-1 (page 10, A4), current only
- [0x2C] EPS-2 (page 10, C2), current only
- [0x2E] EPS-3 (page 10, C4), current only
- [0x6A] EPS-4 (page 11, A2), current only
- [0x6C] EPS-5 (page 11, C2), voltage only
- [0xC8] PV0 (+Z) (page 3, A2), voltage and current
- [0xCA] PV1 (-Y) (page 3, B2), voltage and current
- [0xCC] PV2 (-X) (page 3, B2), voltage and current
- [0xCE] PV3 (+Y) (page 3, C2), voltage and current

2.2.12.3 Backplane to IHU

The PMIC is a slave to the IHU. See the interface document[34] for details.

2.2.13 Analog Voltage Reference and Supply

The EPS has a precision voltage reference (page 11, A5)[35] for calibrating the ADCs. For the current sensing ADCs, this is inputted into the reference input which results in a resolution at 16b of $\frac{900mV}{2^{16}} = 13.73\mu\frac{V}{LSB}$. For the voltage sensing and both sensing ADCs, this is inputted into one of the channels which provide calibration through some linear math. These ADCs have the analog voltage supply inputted into

[32] TCA9535
[33] LTC2499
[34] https://github.com/CougsInSpace/CougSat1-Software/blob/master/CougSat1-PMIC/docs/PMICInterface.pdf
[35] MCP1501

the reference input. They also have a voltage divider between the channel inputs and the actual ADC input (page 11, C1) which allows 3.3 times the voltage for a total range of $(\pm 1.65V * 3.3) = \pm 5.4V$ and a resolution at 16b of $\frac{5.4V}{2^{16}} = 82\mu\frac{V}{LSB}$.

The EPS has an analog voltage supply (page 11, B5) which is the always-on *3.3V* rail filtered with a ferrite bead and capacitors. Precision is not required as all ADCs use the precision voltage reference for calibration. This is the source for the thermistors.

2.2.14 Mechanical Features

The RBF pin holder (page 4, D1) and 3.3V regulation heatsink (page 5, B1 & D1) mount directly to the EPS board using bolts. These holes are conductive and connected directly to chassis ground. The EPS also slots into the structure using rails[36] which are also conductive and connected directly to chassis ground. Each of the holes have a capacitor and resistor connecting to power ground which will absorb transients.

2.3 Board

The board shall be double layered with $2\ oz$ copper and ENIG finish.

2.3.1 Layout Constraints

Unless specified in the following subsections, all signals shall use the default parameters below. Signals in the following subsections do not include their sense signals unless specified. Trace width can be broken if a trace needs to bottleneck down to a pin, the bottleneck shall be minimized.

Trace width:	$0.16mm$
Vias:	$\emptyset 0.3mm$, unlimited count
Separation:	$0.16mm$
Length:	unlimited

Devices with specific placement and routing considerations are called out on the schematic, see "CAD Note:"

2.3.1.1 Solar Panel Inputs - PV_IN[0:7], PGND

PGND applies to between the solar panel headers and the backplane

Trace width: $0.3mm$

2.3.1.2 Umbilical Input - UMB_IN, PGND

PGND applies to between the umbilical header and the backplane

Trace width: $0.6mm$

[36] See backplane documentation for details

2.3.1.3 Battery Connections - VIN-[A:B], BP_VSS-[A:B] , BP_VSS-I[A:B], VBATT-[A:B], PGND

PGND applies to between the low side battery protection MOSFETs and the backplane.

Trace width: $3.0mm$
Vias: $\emptyset 0.3mm$ five per layer change

2.3.1.4 SMPS Switching Node - 3.3V_ISENS-[A:B], 3.3V_REG_BUCK_NODE-[A:B]

Trace width: $2.5mm$
Vias: No vias
Minimize RF emission

2.3.1.5 SMPS Output - 3.3V_I-[A:B], 3.3V-[A:B]

The traces can taper down once loads branch off and less than three loads remain.

Trace width: $2.5mm$
Vias: $\emptyset 0.3mm$ three per layer change

2.3.1.6 SMPS Ground - PGND

PGND applies to between the filtering capacitors and the backplane.

Trace width: $1.0mm$

2.3.1.7 Rail Output Channels - PR_3.3V-[0:12], PR_BATT-[0:6], PR_BH-[0:1]

Trace width: $0.6mm$

2.3.1.8 Deployables Output - PR_DEPLOY

Trace width: $1.5mm$
Vias: $\emptyset 0.3mm$ two per layer change

2.3.1.9 JTAG - JTAG-[TCK, TDI, TDO, TMS], BUS_JTAG-[TCK, TDI, TDO, TMS]

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

2.3.1.10 I^2C - I2C_[SDA, SCL], BUS_I2C_[SDA, SCL, IRQ]

Length: Each node shall be length matched $\pm 1.0mm$
Stubs: $< 10.0mm$

3 Testing

3.1 3.3V Regulator

4 Discussion

5 Appendix