Interleaving two Phase CRM/CCM Operation Power Factor Correction Controller

General Description

AT6201L is an advanced active power factor corrected controller that integrates two 180 out of phase PWM to drive PFC boost stages base on ATK patented Pseudo Digital Loop(PDL) control method.

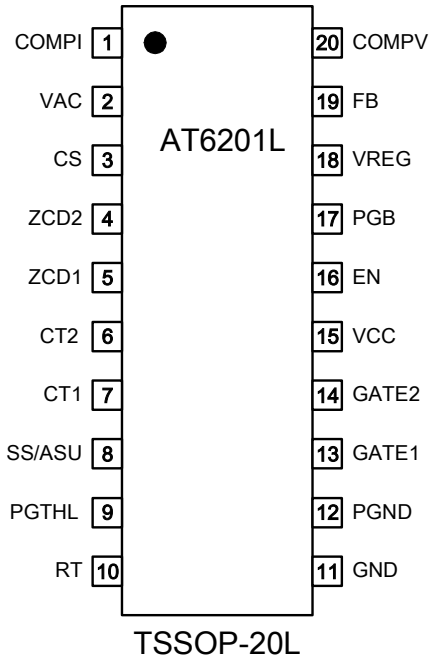
In PDL control ,AT6201L classically operates in Critical conduction Mode(CRM) when the inductor current below a programmable value.When the current is exceed this preset level ,the AT6201L natural change to Continuous conduction Mode(CCM).The loop stability and response is controlled by PDL. AT6201L features a robust suite of protection features to properly handle an array of power supply operating and fault condition.

The devices is available in TSSOP-20L package and require few external devices for operation.

Applications

- **High Efficiency Server and Desktop Power Supplies**
- **Telecom Rectifiers**
- **High Power Adaptor**
- **Off Line Appliances Requiring Power Factor Correction**

Pin Configuration



TSSOP-20L

Features

- **Pseudo Digital Control Loop without Analog multiplier**
- **Average Current Mode Interleaving PWM Control with Inherent Current Matching**
- **Quick Transient Response**
- **Intelligent AC Power Sag Protection**
- **Multi-Mode CRM/CCM operation**
- **Programmable Soft Start**
- **Programmable CCM Operation Frequency 18kHz~130kHz**
- **Sourcing 1A/Sinking 1A High Drive Cability Driver**
- **Brown In/Out protection**
- **Bias-Supply UVLO ,Over-Voltage Protection ,Open-Loop Detection ,**
- **TSSOP-20L Package**

Function Marking Information

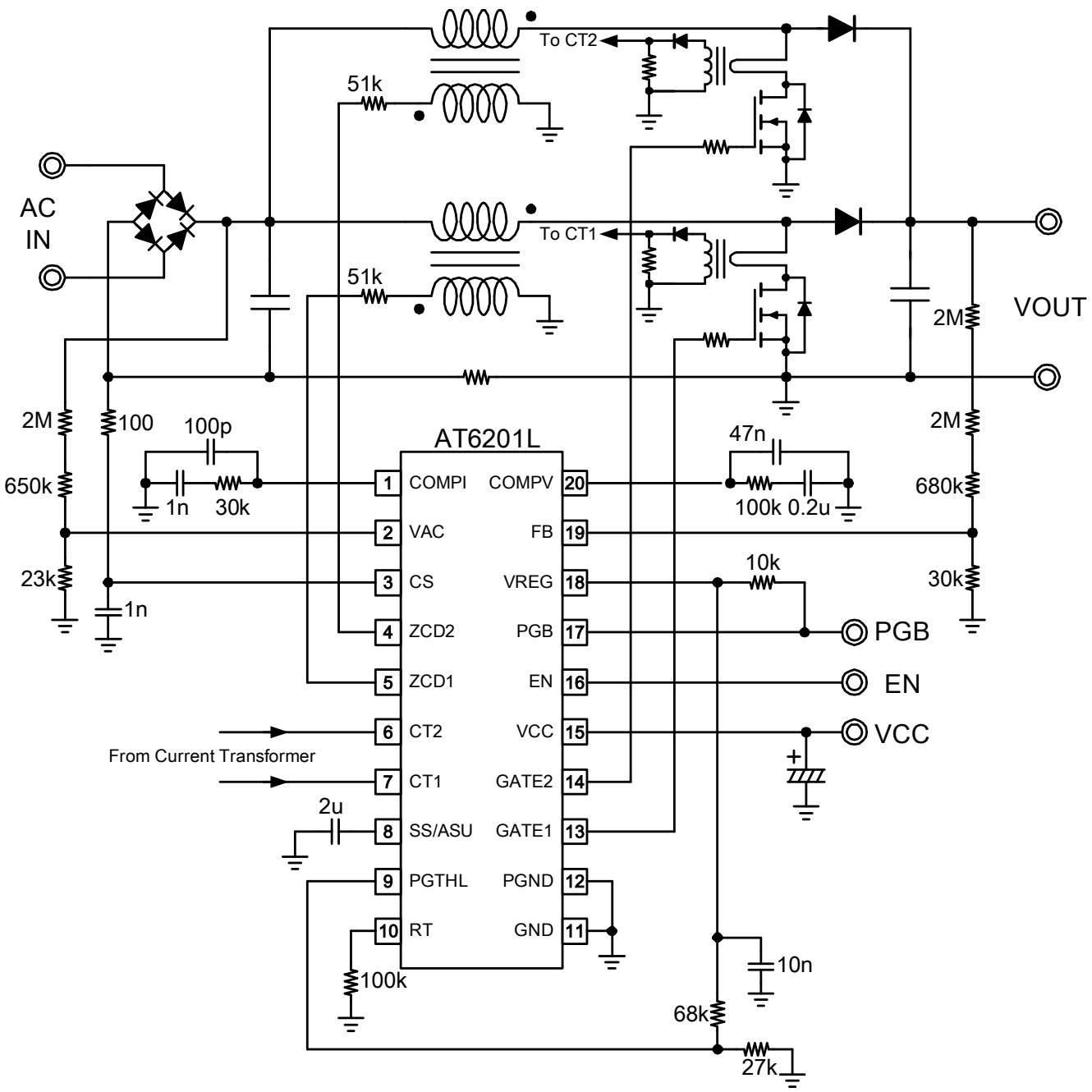
Top Marking	Switching Frequency	Vout Level Boost
AT6201L	ADJ	Enable

Ordering and Marking Information

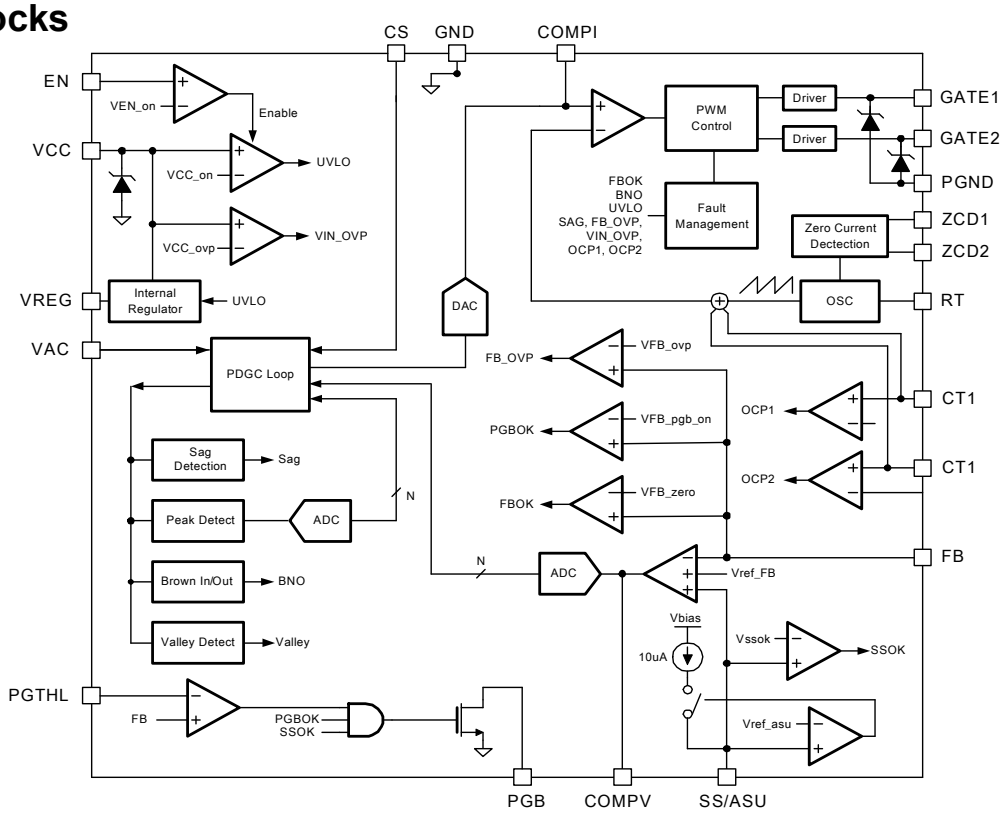
Order Number	Package	Top Marking
AT6201LSPF	TSSOP-20L	AT6201L

Note: Aplustek products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit



Function Blocks



Function Pin Description

No.	Pin Name	Pin Function
1	COMPI	**Current error amplifier output.**
2	VAC	**AC line sense input pin.**
3	CS	**PFC current sense**.
4	ZCD2	**Channel2 Zero current detect input Pin.** Pull low would operatein CCM,Pull high would Shutdown Channel2.
5	ZCD1	**Channel1 Zero current detect input Pin.** Pull low would operatein CCM,Pull high would Shutdown Channel1 adn 2..
6	CT2	**Channel2 current transformer detect input Pin.**
7	CT1	**Channel1 current transformer detect input Pin.**
8	SS/ASU	**Soft Start time setting input pin.**
9	PGTHL	**An I/O pin**.Setting for Power Good threshold to determine PGB to be pull high level.
10	RT	**CCM switching Frequency input pin.**
11	GND	**Ground.**
12	PGND	**Gate Driver1/2 GND.**
13	Gate1	**Channel1 Gate Driver output Pin.**
14	Gate2	**Channel2 Gate Driver output Pin.**
15	VCC	**Positive Supply for AT6201Z.**
16	EN	**IC Enable pin.**
17	PGB	**Power Good comparetor output pin.**
18	VREG	**Reference Voltage output pin.**
19	FB	**Voltage error amplifier input.**
20	COMPV	**Voltage error amplifier output.**

Absolute Maximum Ratings

(Note1)

Supply Input Voltage, V_{cc} ---------- -0.3V to +27V

PGB,EN to GND DC ---------- -0.3V to +27V

CS to GND DC ---------- -6V to +0.3V

Gate1/2 to GND DC ---------- -0.3V to 21V

COMPI,VAC,ZCD1/2,SS/ASU,PGTHL,RT,VREG,FB,COMPV,CT1/2 to GND DC ---------- -0.3V to +7V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- -40°C to +150°C

Lead Temperature Range(Soldering 10sec) ---------- 260°C

ESD Rating (Note2)

HBM(Human Body Mode)----------2KV

MM(Mechine Mode)----------200V

Thermal Characteristics

Package Thermal Resistance (Note3)

TSSOP-20L θ_{JA} ----------76°C/W

Power Dissipation, PD @ TA = 25°C

TSSOP-20L ----------1.3W

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Input Section						
VCC operation range			10	--	21	V
VCC UVLO threshold	$V_{CC,on}$	VCC Rising	--	10	--	V
	$V_{CC,off}$	VCC Falling	--	8	--	V
Over Voltage Protection Voltage	$V_{CC,ovp}$			24		V
Inter Zener Clamp	$V_{CC,clamp}$	IVCC=10mA ,CL=0		27		V
Startup current	$I_{CC,start}$			35	70	uA
Normal operation current	I_{CC_op}	CL=2nF	--	4.5	6.5	mA
VAC Section						
Brown In Threshold	VAC_brown_in		--	1	--	V
Brown In Debounce Time	Tdeb_brown_in			200		uS
Brown Out Threshold	VAC_brown_out		--	0.94	--	V
Brown Out Debounce Time	Tdeb_brown_out			440		mS
Pull low Impedance	ZVAC			500		kohm
High Line Threshold	VAC_hline	Sweep VAC from low to high		2.35		V
Low Line Threshold	VAC_lline	Sweep VAC from high to low		2.1		V
Low Threshold for Valley Detect	VAC_valley_l			0.35		V
High Threshold for Valley Detect	VAC_valley_h			0.72		V
SAG Debounce Time	Tdeb_sag			5		mS
Product of VAC Peak and Internal VAC Peak				5.4		V*V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
CS Section						
Delay to Output				250		nS
Threshold to off PWM at low Line	VCS_max_lline		--	-1.56	--	V
Threshold to off PWM at lhigh Line	VCS_max_hline		--	-0.94	--	V
Input Impedance	ZCS		20			kohm
Max Fain of CS over Internal VAC				0.2		V/V
ZCD 1/2 Section						
Negative Clamp Voltage	VZCD_clamp_l		--	-0.6	--	V
Positive Clamp Voltage	VZCD_clamp_h			6.1		V
Falling Threshold for Zero Current Detection	VZCD_zero_fall	Sweep ZCD from high to low		0.4		V
Rising Threshold for Zero Current Detection	VZCD_zero_rise	Sweep ZCD from low to high		0.5		V
Threshold to Keep low to off CRM mode	VZCD_crm_off			0.4		V
Threshold to Keep high to off PWM mode	VZCD_pwm_off			0.5		V
CT 1/2 Section						
Threshold to off PWM at Low Line	VCT_max_lline			3.5		V
Threshold to off PWM at High Line	VCT_max_hline			2.1		V
Leading Edge Blanking Time	t_leb			200		nS
SS/ASU Section						
Voltage lower than VCC in Power On for ASU mode					2	V
Charging Current in SS mode	ISS			10		uA
Soft Start Time in ASU mode	t_ss			175		mS
PGTHL Section						
FB voltage to pull PGB High at High FB mode	VFB_pgb_off_hfb	PGTHL=2V	1.98		2.02	V
FB voltage to pull PGB High at Low FB mode	VFB_pgb_off_lfb	PGTHL=2V	1.8		1.89	V
RT Section						
Nominal Frequency	fosc	connect 100kohm to GND		65		kHz
Resister Range			40		400	kohm
Frequency Variation vs.VCC					2	%
Frequency Variation vs. Temperature					2	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
COMPI Section						
Transconductance	gm_compi			72		uohm
Input Offset Voltage	vos_compi		-1		1	mV
Max Sink Current	Isink_max_compi		--	-36	--	uA
Max Source Current	Isource_max_compi			36		uA
Clamp High Voltage	VCOMPI_clamp_h			4.3		V
Clamp Low Voltage	VCOMPI_clamp_l			0.52		V
Threshold for Zero Duty	VCOMPI_zero			0.77		V
COMPV Section						
Transconductance	gm_compv			72		uohm
Input difference with GM Boost	Vdiff_gn_boost			-100		mV
Transconductance with GM Boost	gm_compvl_boost			163		uohm
Max Sink Current	Isink_max_compv			36		uA
Max Source Current	Isource_max_compv			36		uA
Clamp High Voltage	VCOMPV_clamp_h			4.3		V
Clamp Low Voltage	VCOMPV_clamp_l			0.72		V
Threshold for Zero Duty	VCOMPV_bs			0.8		V
Threshold for Low Feedback Mode	VCOMPV_lfb	Sweep COMPV from High to Low		2.54		V
Threshold for High Feedback Mode	VCOMPV_hfb	Sweep COMPV from Low to High		2.84		V
Threshold for Single Mode	VCMOP_single	Sweep COMPV from High to Low		1.585		V
Hysteresis of Single Mode Threshold				117		mV
FB Section						
Reference Voltage at High Feedback Mode	Vref_FB_hfb			2.515		V
Reference Voltage at Low Feedback Mode	Vref_FB_lfb			2.35		V
Debounce of Low Feedback Mode	Tdeb_lfb			1		S
Threshold for FB OVP	VFB_ovp	Sweep FB from Low to High		2.75		V
Hysteresis of FB OVP Threshold				200		mV
Threshold for PGB Pull Low	VFB_pgb_on			2.2		V
Threshold to off PWM	VFB_pwm_off			0.4		V
VREG Section						
Output Voltage	Vreg			6		V
Line Regulation		0mA<I<3mA			5	mV
Load Regulation					20	mV
PGB Section						
Output Voltage Low	Vpgb_ol	Io=10mA Sinking			0.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Gate 1/2 Section						
Maximum Duty Cycle	Dmax			98		%
Output Voltage Low	Vol	VCC=12V,Io=20mA Sinking			0.15	V
Output Voltage High	Voh	VCC=12V,Io=20mA Sinking	10			V
Rising Time	tr	CL=2nF,VGATE from 2V to 6V		30		nS
Falling Time	tf	CL=2nF,VGATE from 6V to 2V		10		nS
Gate Clamping Voltage	Vgate_clamp	VCC=21V	12	15	18	V
Output Phase Shift				180		Degr-ee
EN Section						
Threshold to Enable Controller	VEN_on			2.25		V
Hysteresis of EN Threshold				100		mV
TSD Section						
Internal Thermal Protection	TSD_int			150		Degr-ee
Hysteresis of Thermal Protection	TSD_int_hys			20		

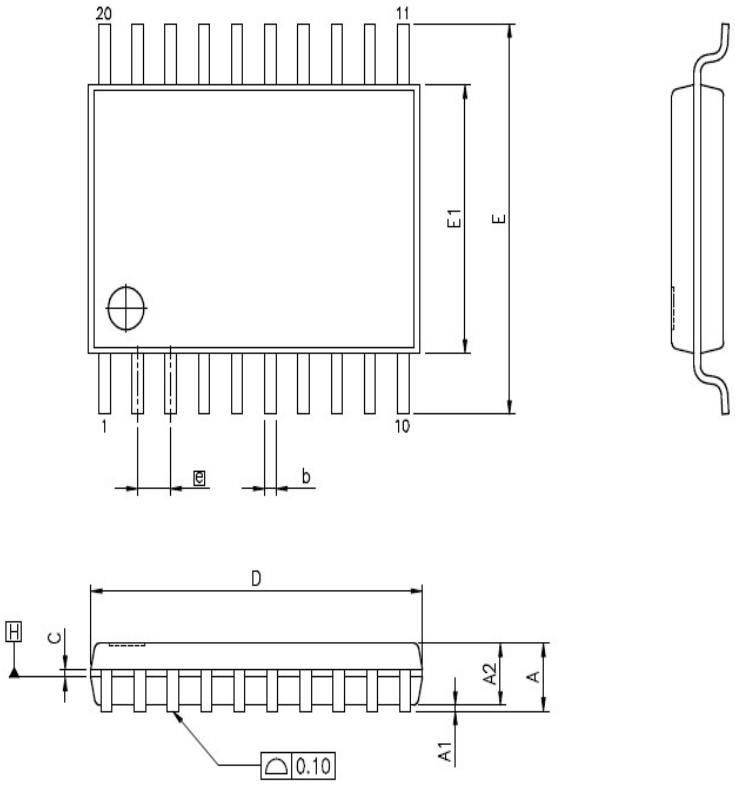
Note 1. Exceeding these limits may impaire the life of the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note 2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.The exposed pad of the package is soldered directly on the PCB.

Typical Operation Characteristics

Package Information

TSSOP-20L



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	0.90	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension .
   MAX: Maximum dimension specified.
   MIN: Minimum dimension specified.
   REF: Represents dimension for reference use only. The value is not the device specification.
   TYP: Represents as a typical value. The value is not the device specification.
2. All linear dimensions are in Millimeters.