Course Name: Digital System Design

Course Number and Section: **14:332:437:03**

Experiment: # 3 – Thunderbird Turn Signal

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----------For Lab Instructor Use ONLY----------

GRADE: _____

COMMENTS:

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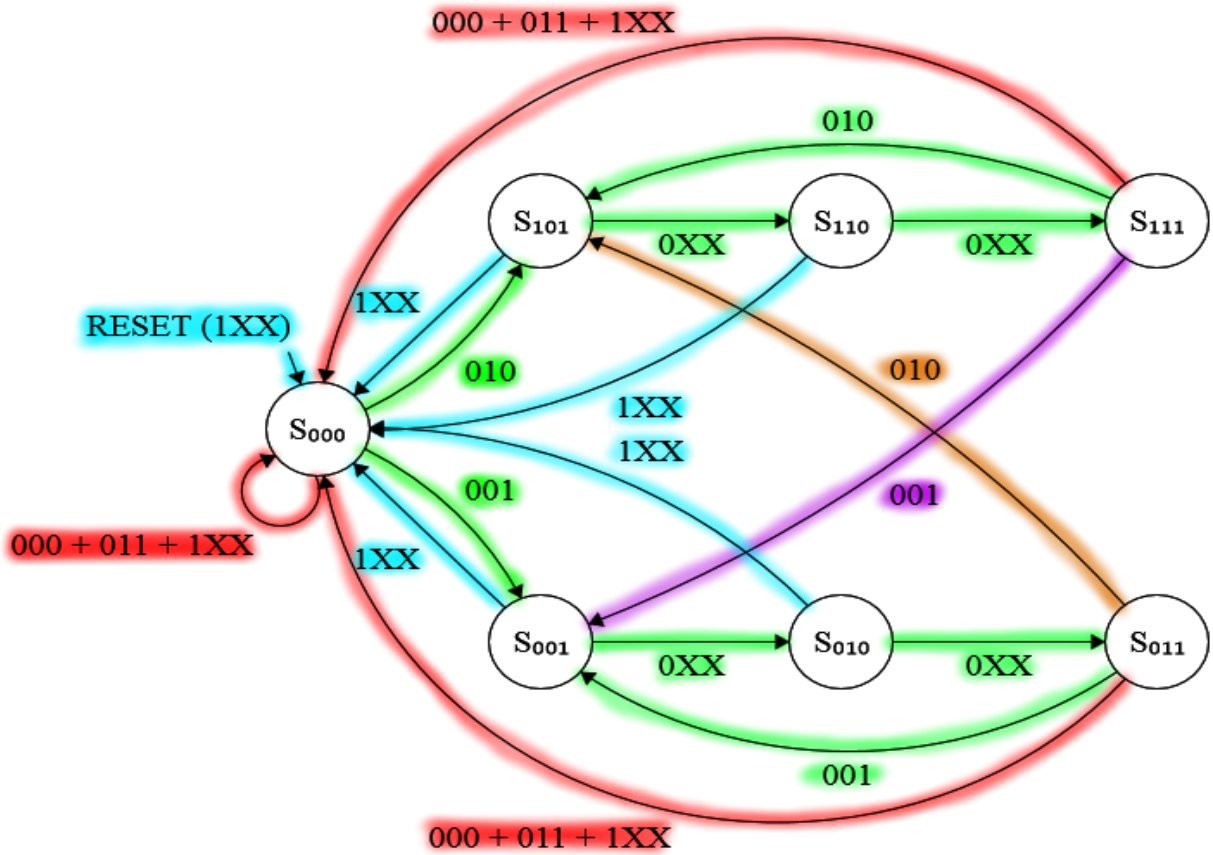
PURPOSE

To create a Thunderbird turn signal FSM by use of SystemVerilog and Quartus' compiler, in order to have the student obtain experience in coding such mechanics. Time spent: 7 hours total.

FSM Design



Where:

- S_{000} means all lights are off
- S_{001} means RA is on
- S_{010} means RA and RB are on
- S_{011} means RA, RB, and RC are on
- S_{101} means LA is on
- S_{110} means LA and LB are on
- S_{111} means LA, LB, and LC are on

FSM Transition Table

Inputs			Current State ($S_{2:0}$)			Next State ($S_{2:0}'$)		
RESET	**Left**	**Right**	**S2**	**S1**	**S0**	**S2'**	**S1'**	**S0'**
X	**X**	**X**	S2	S1	S0	S2	S1	S0
1	**X**	**X**	S2	S1	S0	0	0	0
0	**1**	**1**	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	**1**	0	0	0	0	**1**	0	**1**
0	0	**1**	0	0	0	0	0	**1**
0	**X**	**X**	0	0	**1**	0	**1**	0
0	**X**	**X**	0	**1**	0	0	**1**	**1**
0	0	**1**	0	**1**	**1**	0	0	**1**
0	**1**	**1**	0	**1**	**1**	0	0	0
0	0	0	0	**1**	**1**	0	0	0
0	**1**	0	0	**1**	**1**	**1**	0	**1**
0	**X**	**X**	**1**	0	**1**	**1**	**1**	0
0	**X**	**X**	**1**	**1**	0	**1**	**1**	**1**
0	**1**	0	**1**	**1**	**1**	**1**	0	**1**
0	**1**	**1**	**1**	**1**	**1**	0	0	0
0	0	0	**1**	**1**	**1**	0	0	0
0	0	**1**	**1**	**1**	**1**	0	0	**1**

SystemVerilog Code

Attached on end.

Waveforms

Also attached on end.

CONCLUSIONS

The compiler only seemed to use 1 register, instead of the expected 3 (S0, S1, and S2), which came as a complete shock. As for the I/O pins, the compiler assigned 10 pins - which is the exact amount of variables found in the code. So, I can fairly say that the compiler managed to perform some amount of ingenuity that exceeded my expectations.