To INT Cr To UINT



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To INT Or To UINT

"There are far too many integer types, there are far too lenient rules for mixing them together, and it's a major bug source, which is why I'm saying stay as simple as you can, use {signed} integers till you really need something else."

~Bjarne Stroustrup

https://graphitemaster.github.io/aau/

"The need for signed integer arithmetic is often misplaced as most integers never represent negative values within a program. The indexing of arrays and iteration count of a loop reflects this concept as well. There should be a propensity to use unsigned integers more often than signed, yet despite this, most coders incorrectly choses to use signed integers almost exclusively."

~ Dale Weiler

https://graphitemaster.github.io/aau/

Disclaimer: X86 machines only in this talk

SIMPLE EXAMPLE:

```
#include <stdint.h>
 2
     int64_t add_and_devide_s(int64_t a, int64_t b){
 3
         return (a+b)/2;
 5
 6
8
     uint64_t add_and_devide_u(uint64_t a, uint64_t b){
9
         return (a+b)/2;
10
11
```

SIMPLE EXAMPLE: UNSIGNED VERSION

SIMPLE EXAMPLE: UNSIGNED VERSION

```
add_and_devide_u(unsigned long, unsigned long):
lea rax, [rdi + rsi]
shr rax
ret
```

Register	Accumulator		Counter		Data		Base		Stack Pointer	Stack Base Pointer		Source	Destination	
64-bit	RAX		RCX		RDX		RBX		RSP	RBP		RSI	RDI	
32-bit	EAX		ECX		EDX		EBX		ESP	EBP		ESI	EDI	
16-bit		AX		CX	D)	X	В	X	SP		ВР	SI		DI
8-bit		AH AL	С	H CL	DH	DL	ВН	BL	SPL		BPL	SIL		DIL

```
add_and_devide_u(unsigned long, unsigned long):

lea rax, [rdi + rsi]

shr rax

ret
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```

SIMPLE EXAMPLE: SIGNED VERSION

SIMPLE EXAMPLE: SIGNED VERSION

```
add_and_devide_s(long, long):
             lea
                      rcx, [rdi + rsi]
3
                      rax, rcx
             mov
             shr
                      rax, 63
             add
                      rax, rcx
6
             sar
                      rax
             ret
```

Surprise



```
add_and_devide_s(long, long):
                     rcx, [rdi + rsi]
             lea
3
                     rax, rcx
             mov
             shr
                     rax, 63
             add
                      rax, rcx
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             sar
                      rax
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                      rax, rcx
             mov
             shr
                      rax, 63
             add
                      rax, rcx
6
             sar
                      rax
             ret
```

```
add_and_devide_s(long, long):
             lea
                      rcx, [rdi + rsi]
3
                      rax, rcx
             mov
             shr
4
                      rax, 63
             add
                      rax, rcx
6
             sar
                      rax
             ret
```

```
add_and_devide_s(long, long):
             lea
                      rcx, [rdi + rsi]
3
                      rax, rcx
             mov
             shr
                      rax, 63
             add
                      rax, rcx
6
                      rax
             sar
             ret
```

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                      rax, 63
             add
                      rax, rcx
6
             sar
                      rax
             ret
```

•In the current example we are dividing the number by two and so, division by two is just like shifting the number right, as all numbers are represented in the binary form. Therefor using n/2 is equal to n>>1.

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- •Each execution has its own unit and there is a limited number of execution units. (depends on the **CPU**)

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- •Each instruction that is fetched from the memory is pushed into a pipeline, one of the steps in the pipeline is execution, execution may be piped as well.
- Each execution has its own unit and there is a limited number of execution units. (depends on the CPU)
- Each instruction has its own latency

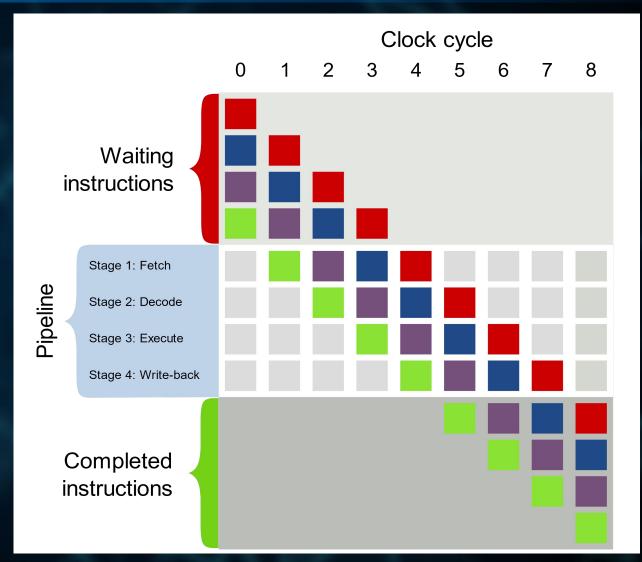
WHAT IS LATENCY?

- The number of cycles it takes to compute an instruction
 - Errors, misalignment, and cache misses might increase the cycles count
 - NAN's and INFS do not increase the cycles

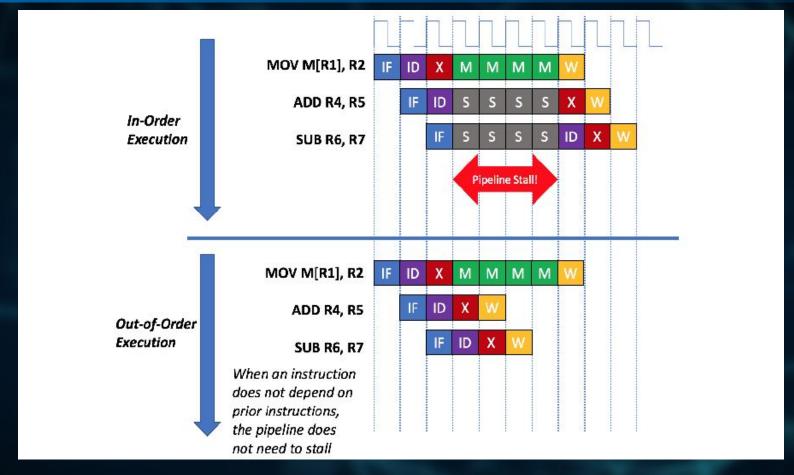
WHAT IS LATENCY: EXAMPLES

- ADD 1 cycle (not piped)
- •IMUL 3 cycles
- •DIV at least x20 time slower than imul (depending on the architecture)

WHAT IS LATENCY: PIPES

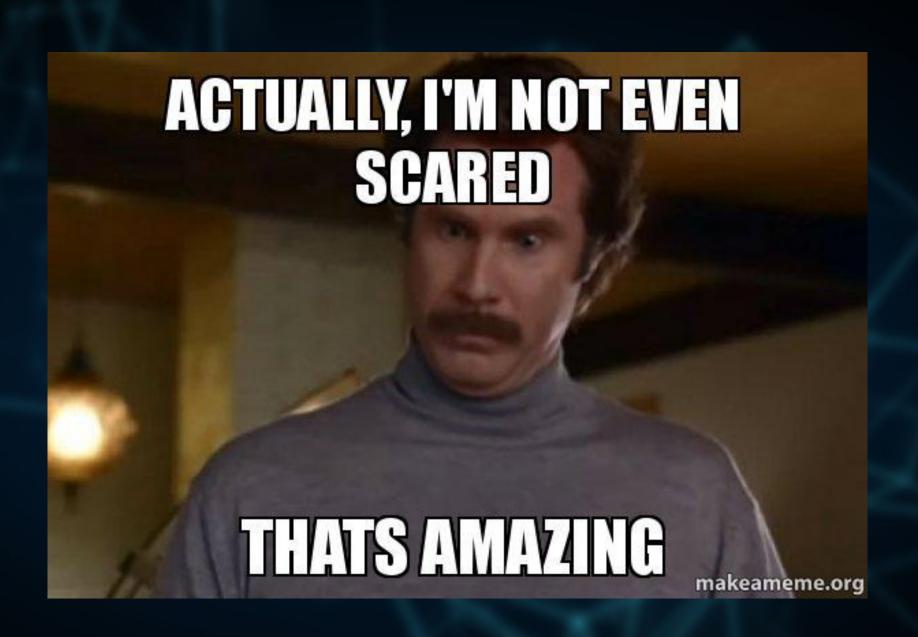


WHAT IS LATENCY: PIPES



Source:

 $\frac{https://www.semanticscholar.org/paper/RISC-V-Reward:-Building-Out-of-Order-Processors-in-Zekany-Tan/f7f6d27f334604c3c85f0b8d21d2a9b4df22a983}{\text{Any-Tan/f7f6d27f334604c3c85f0b8d21d2a9b4df22a983}}$



BACK TO OUR EXAMPLE: WHAT HAPPENED?

```
add_and_devide_s(long, long):
             lea
                      rcx, [rdi + rsi]
3
                      rax, rcx
             mov
             shr
                      rax, 63
             add
                      rax, rcx
6
             sar
                      rax
             ret
```

- Unsigned Integers:
 - Stored using Modulo 2 representation
 - Support only positive numbers
 - Overflow is well-defined
 - •The Range of a 64-bit unsigned integer is 0 to 18,446,744,073,709,551,615 (2^n)

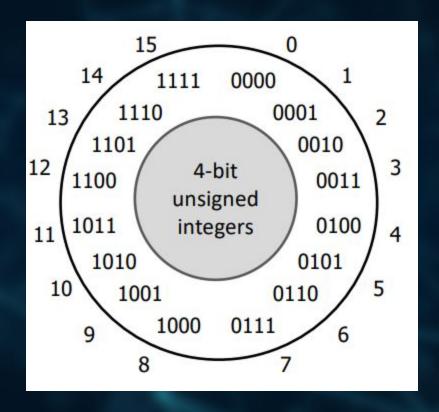
Unsigned Integers: representation

Bits:

Wight:

 $1^{2^{4}}+0^{2^{3}}+1^{2^{2}}+1^{2^{1}}+1^{2^{1}}+0^{2^{0}}=1^{2^{1}}+1^{2$ Actual:

Unsigned Integers: Overflow



$$15 + 2 = 1$$
 $1111 0010 = 0001$

- •Signed Integers:
 - support negative numbers
 - Stored using:
 - Sign and magnitude
 - One's complement
 - Two's complement
 - overflow is considered undefined behavior
 - •The range of a 64-bit signed integer is
 - -9,223,372,036,854,775,808 to 9,223,372,036,854,775,807

- One's Complement
 - Representing negative numbers by inverting all bits

Bits \$	Unsigned value ♦	Ones' complement value
000	0	0
001	1	1
010	2	2
011	3	3
100	4	-3
101	5	-2
110	6	-1
111	7	-0

Source: https://en.wikipedia.org/wiki/Ones%27 complement

- One's Complement
 - Example: 4 bit number

- Two's Complement
 - Start with a positive number
 - Invert all bits
 - Add 1 and ignore overflows

Bits +	Unsigned value ♦	Signed value (Two's complement) \$
000	0	0
001	1	1
010	2	2
011	3	3
100	4	-4
101	5	-3
110	6	-2
111	7	-1

Source: https://en.wikipedia.org/wiki/Two%27s complement

- Two's Complement
 - Example: 4 bit number

Source: https://en.wikipedia.org/wiki/Ones%27 complement

- Positive numbers are represented in the same way for signed and unsigned
- Since C++20 negative numbers are represented only with Two's complement

BACK TO OUR EXAMPLE: WHAT HAPPENED?

```
add_and_devide_s(long, long):
             lea
                      rcx, [rdi + rsi]
3
                      rax, rcx
             mov
             shr
                      rax, 63
             add
                      rax, rcx
6
             sar
                      rax
             ret
```

DIFFERENCE BETWEEN SHR AND SAR

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SHR: Logical right shift means shifting the bits to the right and MSB becomes 0.

Example: shr 1 0 1 1 0 1 1 1 = 0 1 0 1 1 0 1 1

DIFFERENCE BETWEEN SHR AND SAR

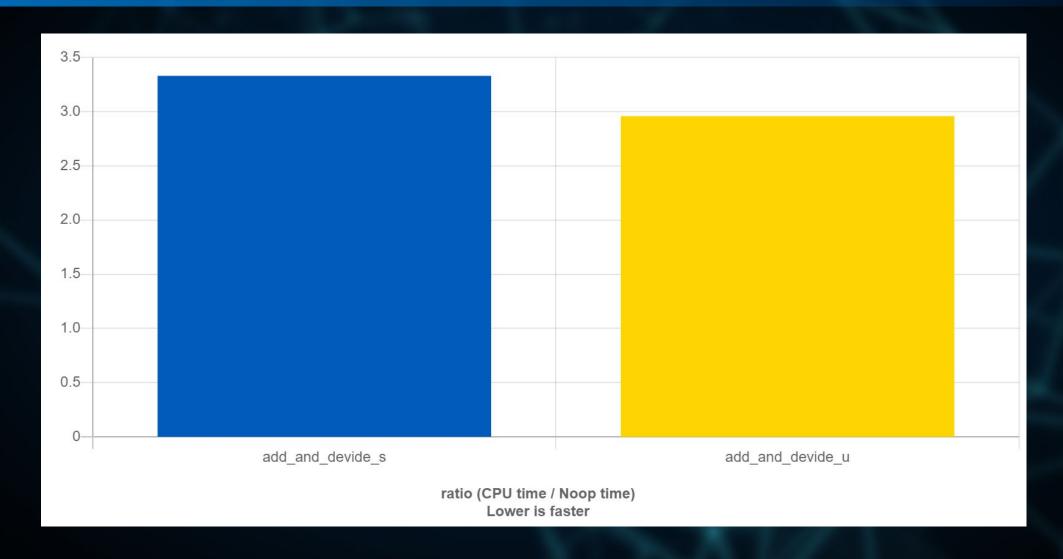
SAR: Arithmetic right shift means shifting the bits to the right and **MSB** bit is same as in the original number.

Example: sar $\mathbf{1}$ 0 1 1 0 1 0 1 = $\mathbf{1}$ 1 0 1 1 0 1 0.

BACK TO OUR EXAMPLE: WHAT HAPPENED?



BACK TO OUR EXAMPLE: PERFORMANCE



SIGNED AND UNSIGNED PITFALLS

SIGNED AND UNSIGNED PITFALLS:

```
14   auto add_uint8(uint8_t a, uint8_t b){
15    return a+b;
16 }
```

• what will the result be if we call add_uint8(255u, 1u)?

SURPRISE AGAIN: INTEGER PROMOTION

```
int add_uint8(uint8_t a, uint8_t b)
{
   return static_cast<int>(a) + static_cast<int>(b);
}
```

256

SIGNED AND UNSIGNED PITFALLS:

```
uint8_t add_uint8(uint8_t a, uint8_t b){
return a+b;
}
```

• what will be the result if we will call add_uint8(255u, 1u)?

INTEGER NARROWING

```
uint8_t add_uint8(uint8_t a, uint8_t b){
return static_cast<unsigned char>(static_cast<int>(a) + static_cast<int>(b));
}
```



SURPRISE AGAIN: WAIT THAT'S NOT ALL

```
19  auto my_add(auto x, auto y){
20   return x+y;
21 }
```

what will be the result if we will call

```
my_add(uint64_t(1), int64_t(-2))?
```

SURPRISE AGAIN: MORE INTEGER PROMOTION

```
unsigned long my_add(unsigned long x, long y)
{
   return x + static_cast<unsigned long>(y);
}
```

18446744073709551615

MIXING INTEGER TYPES MAY CAUSE HORRIBLE BUGS

```
uint64 t count(uint64 t size){
36
          uint64 t count;
37
          for (int i = 0; size-i >= 0; i++){
38
              count++;
39
40
41
          return count;
42
```

MIXING INTEGER TYPES MAY CAUSE HORRIBLE BUGS

```
void decode(std::byte* bytes, int size){

if (size == 0) return;

std::byte decoded[255];

for (uint64_t i = 0; i < size; i++){

    decoded[i] = static_cast<std::byte>(static_cast<uint8_t>(bytes[i])^0xc);
}
```

BEWARE OF THIS PATTERN

```
void do_somthing(std::byte* bytes, uint32_t size){
for (auto i=0; i < size; i++){
}
}</pre>
```

AUTO IS GREAT: USE IT DON'T ABUSE IT

29	auto	a1	=	0;
30	auto	a2	=	0u;
31	auto	a3	=	01;
32	auto	a4	=	0ul;
33	auto	a5	=	011;
34	auto	a6	=	0ull;

AUTO IS GREAT: USE IT DON'T ABUSE IT

```
int a1 = 0;
unsigned int a2 = 0U;

long a3 = 0L;

unsigned long a4 = 0UL;

long long a5 = 0LL;

unsigned long long a6 = 0ULL;
```

SIZE_T AND SSIZE_T

- •size_t:
 - Unsigned integer
 - Used for size operations
 - Defined in cstddef
 - •size_t limit is SIZE_MAX
 - Introduced in C89 to eliminate portability problems

SIZE_T AND SSIZE_T

- •ssize_t:
 - Signed version of size_t
 - Defined by POSIX.1-2017
 - Represent at least the range [-1,{SSIZE_MAX}].

```
for (int i = 0; i < container.ssize()-1; ++i)</pre>
```

AUTO IS GREAT: USE IT DON'T ABUSE IT (C++23 ADDITIONS)

```
auto a7 = 0z;
auto a8 = 0uz;
```

AUTO IS GREAT: USE IT DON'T ABUSE IT (C++23 ADDITIONS)

```
10 long a7 = 0L;
10 unsigned long a8 = 0UL;
10 long a7 = 0L;
11 long a7 = 0L;
12 long a7 = 0L;
13 long a7 = 0L;
14 long a8 = 0UL;
15 long a7 = 0L;
16 long a7 = 0L;
17 long a7 = 0L;
18 long a8 = 0UL;
18 long a8 long a8 = 0UL;
18 long a8 long
```

POP QUIZ ©

```
82     uint64_t do_it(uint64_t count){
83         return 1 << (count % 64);
84     }</pre>
```

 Series of numbers where the difference between any two sequential numbers is constant.

For example, 1,2,3,4,5,6,7,8,9,10,...,n is an **Arithmetic Series** where the difference between any two sequential numbers is 1.

$$\sum_{k=1}^{n} a_k = \frac{n(a_1 + a_n)}{2}$$

```
uint64_t arc_unsigned(uint64_t n){
59
         uint64 t sum = 0;
60
         for (uint64_t i = 1; i <= n; i++){
61
              sum += i;
62
63
64
65
         return sum;
66
67
     int64 t arc signed(int64 t n){
68
         int64_t sum = 0;
69
         for (int64_t i = 1; i <= n; i++){
70
              sum += i;
71
72
73
74
         return sum;
75
```

MORE COMPLEX EXAMPLE: UNSIGNED ASSEMBLY

MORE COMPLEX EXAMPLE: UNSIGNED ASSEMBLY

```
arc_unsigned(unsigned long):
                 rdi, rdi
        test
                 .LBB7 1
                 ecx, 1
        mov
        xor
                 eax, eax
.LBB7_4:
        add
                 rax, rcx
                 rcx, 1
        add
                 rcx, rdi
        cmp
        jbe
                 <u>.LBB7 4</u>
        ret
.LBB7_1:
        xor
                 eax, eax
        ret
```

MORE COMPLEX EXAMPLE: UNSIGNED ASSEMBLY

```
arc_unsigned(unsigned long):
                  rdi, rdi
         test
               <u>.LBB7_1</u>
                 ecx, 1
         mov
                  eax, eax
         xor
.LBB7_4:
         add
                  rax, rcx
                  rcx, 1
         add
                  rcx, rdi
         cmp
         jbe
                  <u>.LBB7 4</u>
         ret
.LBB7_1:
         xor
                  eax, eax
         ret
```

```
arc_unsigned(unsigned long):
                  rdi, rdi
         test
         jе
                  <u>.LBB7 1</u>
                  ecx, 1
         mov
         xor
                  eax, eax
.LBB7_4:
         add
                  rax, rcx
                  rcx, 1
         add
                  rcx, rdi
         cmp
         jbe
                  <u>.LBB7 4</u>
         ret
.LBB7 1:
         xor
                  eax, eax
         ret
```

```
arc_unsigned(unsigned long):
                rdi, rdi
        test
        jе
              <u>.LBB7_1</u>
              ecx, 1
        mov
                 eax, eax
        xor
.LBB7_4:
        add
                 rax, rcx
                 rcx, 1
        add
                 rcx, rdi
        cmp
        jbe
                 <u>.LBB7 4</u>
        ret
.LBB7_1:
        xor
                 eax, eax
        ret
```

```
arc_unsigned(unsigned long):
                  rdi, rdi
         test
         je
                  <u>.LBB7 1</u>
                  ecx, 1
         mov
                  eax, eax
         xor
.LBB7_4:
         add
                  rax, rcx
                  rcx, 1
         add
                  rcx, rdi
         cmp
         jbe
                  <u>.LBB7 4</u>
         ret
.LBB7_1:
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```

```
arc_unsigned(unsigned long):
                  rdi, rdi
         test
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                  <u>.LBB7 1</u>
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                  eax, eax
         xor
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                  rax, rcx
                  rcx, 1
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         xor
                  eax, eax
         ret
```

```
arc_unsigned(unsigned long):
                rdi, rdi
        test
        je
                .LBB7 1
                ecx, 1
        mov
        xor
                 eax, eax
.LBB7_4:
        add
                 rax, rcx
                 rcx, 1
        add
                 rcx, rdi
        cmp
        jbe
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        ret
.LBB7_1:
        xor
                 eax, eax
        ret
```

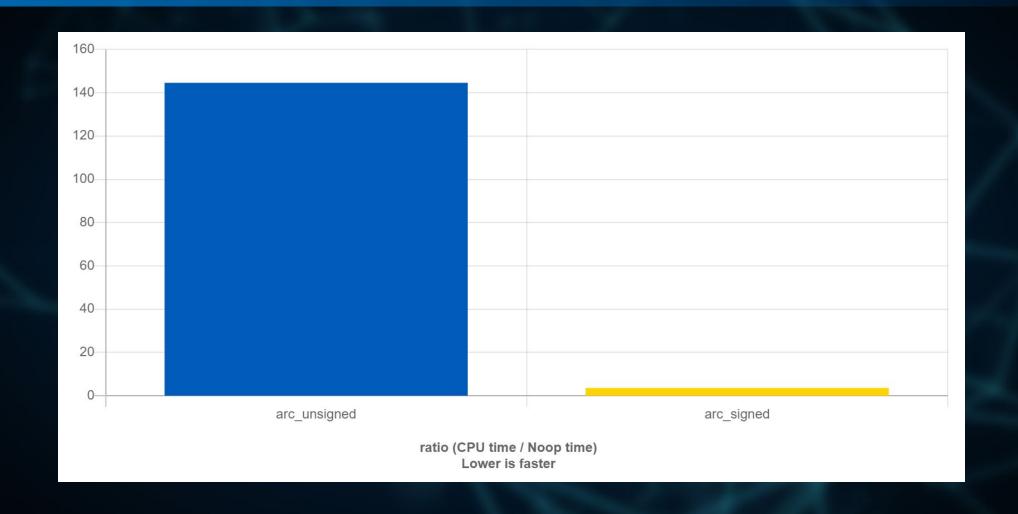
```
arc_unsigned(unsigned long):
                rdi, rdi
        test
        je
                .LBB7 1
                ecx, 1
        mov
        xor
                 eax, eax
.LBB7_4:
        add
                 rax, rcx
                 rcx, 1
        add
                 rcx, rdi
        cmp
        jbe
                 <u>.LBB7 4</u>
        ret
.LBB7_1:
        xor
                 eax, eax
        ret
```

```
arc_unsigned(unsigned long):
                rdi, rdi
        test
        je
                .LBB7_1
                ecx, 1
        mov
        xor
                 eax, eax
.LBB7_4:
        add
                 rax, rcx
                 rcx, 1
        add
                 rcx, rdi
        cmp
        jbe
                 <u>.LBB7 4</u>
        ret
.LBB7_1:
        xor
                 eax, eax
        ret
```

```
arc_signed(long):
               rdi, rdi
        test
        jle
              <u>.LBB8 1</u>
                 rax, [rdi - 1]
        lea
                 rcx, [rdi - 2]
        lea
        mul
                 rcx
        shld
                 rdx, rax, 63
                 rax, [rdx + 2*rdi]
        lea
        add
                 rax, -1
        ret
.LBB8_1:
                 eax, eax
        xor
        ret
```

```
arc_signed(long):
       test rdi, rdi
       jle <u>.LBB8_1</u>
               rax, [rdi - 1]
       lea
               n(a_1 + a_n)
 k=1
       ret
.LBB8_1:
       xor
              eax, eax
       ret
```

MORE COMPLEX EXAMPLE: PERFORMANCE

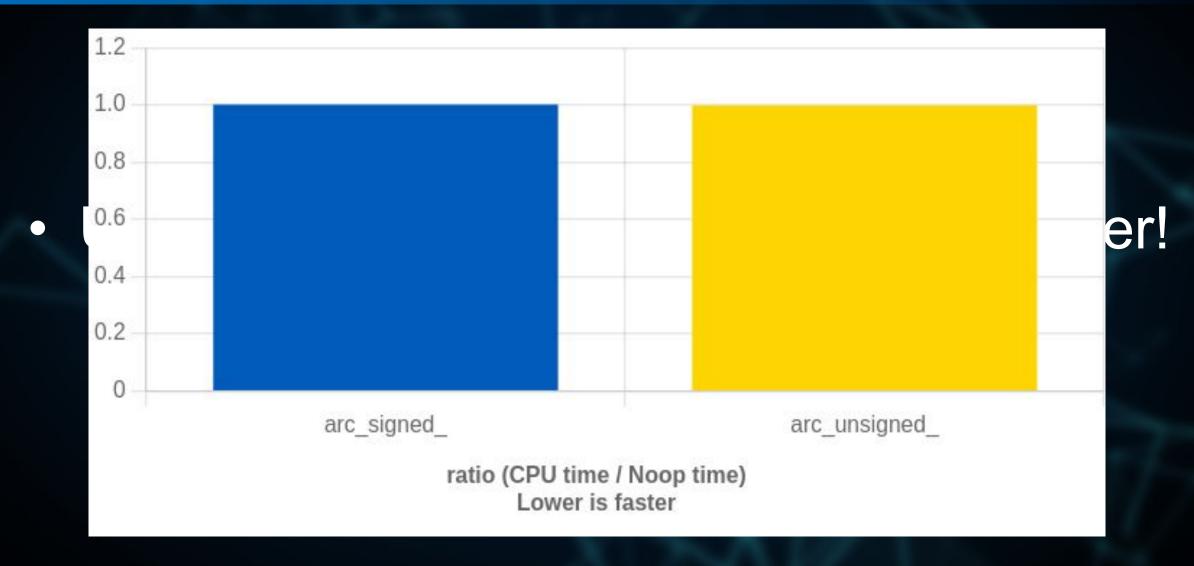


MORE COMPLEX EXAMPLE: WHY?









```
arc_unsigned(unsigned long):
                rdi, rdi
        test
        jе
           <u>.LBB1_1</u>
        inc
           rdi
            rdi, 3
        cmp
                ecx, 2
        mov
        cmovae rcx, rdi
        lea
                rax, [rcx - 2]
        lea
                rdx, [rcx - 3]
        mul
                rdx
        shld
                rdx, rax, 63
                rax, [rdx + 2*rcx]
        lea
        add
                rax, -3
        ret
.LBB1_1:
        xor
                eax, eax
        ret
```

```
arc_signed(long):
              rdi, rdi
       test
       jle
              .LBB0_1
       lea
              rax, [rdi - 1]
              rcx, [rdi - 2]
       lea
       mul
              rcx
       shld
              rdx, rax, 63
       lea
               rax, [rdx + 2*rdi]
       dec
              rax
       ret
.LBB0_1:
       xor
               eax, eax
       ret
```

- Use Sanitizers
 - -fsanitize=signed-integer-overflow
 - -fsanitize=unsigned-integer-overflow

- Use special types for better performance
 - int fastN t, uint fastN t

Know your CPU

- Use special helpers from the standard
 - MAKE SIGNED
 - MAKE UNSIGNED

```
78   auto make_signed_ver(auto val){
79    return std::make_signed_t<decltype(val)>(val);
80 }
```

```
constexpr auto val_signed = make_signed_ver(uint64_t(10));
static_assert(std::same_as<const int64_t, decltype(val_signed)>);
static_assert(val_signed == int64_t(10));
```

Use C++20 safe comparators

```
• std::cmp_equal: ==
• std::cmp_not_equal: !=
• std::cmp_less: <
• std::cmp_less_equal: <=
• std::cmp_greater: >
• std::cmp_greater equal: >=
```

```
int64_t func(auto x, auto y){
  if (x < y) return y;
  return x;
}</pre>
```

func(-10, 20ul) -> -10

```
4 \sint64_t func(auto x, auto y){
5     if (std::cmp_less(x, y)) return y;
6     return x;
7  }
```

func(-10, 20ul) —> 20

 Avoid using auto when not sure about the type

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- Use concrete types when possible!

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- Avoid using auto when not sure about the type
- Use concrete types when possible!
- Use modern loops as much as you can
- Use strong types.

Use strong types.



Use strong types.

```
struct strong_int{
    expline strong int i) : i_{i}
    private int i_,
}
```

QUESTIONS



THANK YOU FOR LISTENING

ALEX DATHSKOVSKY

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WWW.LINKEDIN.COM/IN/ALEXDATHSKOVSKY

Link to presented code: https://godbolt.org/z/W6zvzMzv7