Khulna University of Engineering and Technology

Course no. CSE 4224

Course title: Digital System Design Laboratory

Report on

Project making SAP-1 computer in Logisim

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Objectives:

The main objectives of this project are given below :-

⇒ To learn about SAP-1 computer.

⇒ To learn about different component of SAP-1 computer.

⇒ To design a SAP-1 computer using logisim.

⇒ To learn about instruction of SAP-1 computer.

Introduction:

The SAP-1 computer is a very basic model of a micro-processor. Its primary purpose is to develop basic understanding of how a microprocessor works, interacts with memory and other parts of the system like input and output.

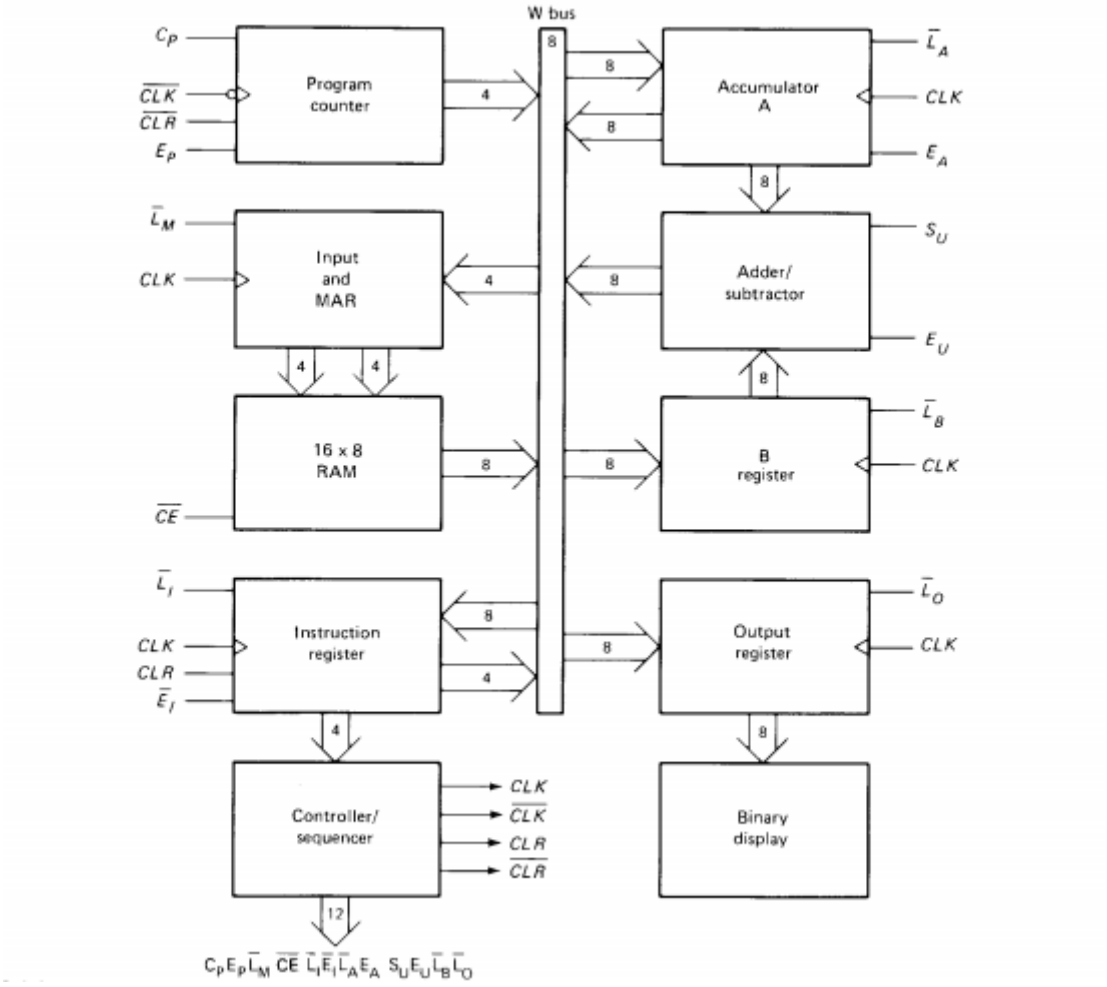

Fig1: SAP-1 Architecture

The SAP-1 computer is the first state towards modern computer and its instruction set is very simple and limited.

In Fig-1, we can see the architecture of SAP-1 computer. Actually, its a bus organized computer. It has a 8 bit bus and all the components are connected to the bus like, PC, Acc, B reg, Adder-subtractor. e.t.c. In this architecture the accumulator, B register and output register all are 8 bit register. But accumular can receive and send data on the other hand the rest only can receive data from the bus.

* Program Counter: Actually this is a 4 bit counter. So, it can count from 0000 to 1111. The PC is reset to 0000 before each program run. When, the computer run begins, the PC sends address 0000 to the memory and increamented. After each instruction fetched and executed the PC sends it data to the memory and get increamented.

* Input and MAR: It includes the address and data switch registers. It sends address bit and data bits to the RAM. As, instructions and data word are written into RAM before a computer run. During a computer run, the address in the PC is latched into MAR. Then the MAR applies the 4 bit address to RAM, where the read operation is performed.

* The RAM: The RAM is a 16x8 static TTL RAM. It stores the instruction and data in the memory befor the computer run. The RAM receives 4 bit address from the MAR and read the instructions or data from the location and place it in the bus.

* Instruction Register (IR): The RAM sends 8 bit instruction to the bus. Actually every instruction has 2 parts. They are: Opcode and oparand. Opcode is the upper 4 bit and oparand is the lower 4 bit. The IR receive the data from the bus sent by the RAM. Then, it split it into opcode and operand. Then, IR send opcode to Control sequence and operand to bus again.

* Control Sequence : This is a very vital part of SAP-1 computer. Actually it controls the SAP-1 computer. The SAP-1 computer has a control word contain 12 bits. The format is given below :→

$$CON = C_P E_P \overline{L_M} \overline{CE} \; \overline{L_I} \overline{E_I} \overline{L_A} E_A \; S_U E_U \overline{L_B} \overline{L_O}$$

This word determines how the registers will react to the next positive clock edge.

* Accumulator : Accumulator is a buffer register that stores intermediate answer during a computer run. It has two outputs. The two-state output goes directly to the ADDER-SUBTRACTOR and the three-state output goes to the bus. Besides it is the only register in SAP-1 computer which can send data to the bus and receive data from the bus.

*The Adder-Subtractor: The SAP-1 computer can perform only two mathematical operation. They are: Addition and Subtraction

When, $S_u = 0$, then $S = A + B$
When, $S_u = 1$, then $S = A + B'$

The Adder-Subtractor can send the result to the bus when E_u is high.

*B register: The B is another buffer register in SAP-1 computer. But it can only receive data from bus do not send to bus. It can send data to Adder-Subtractor for mathematical binary operation.

*Output register: At the end of the computer run, the accumulator contains the answer to the problem being solved. When $E_A = 1$ and $I_o = 0$, the next positive clock edge

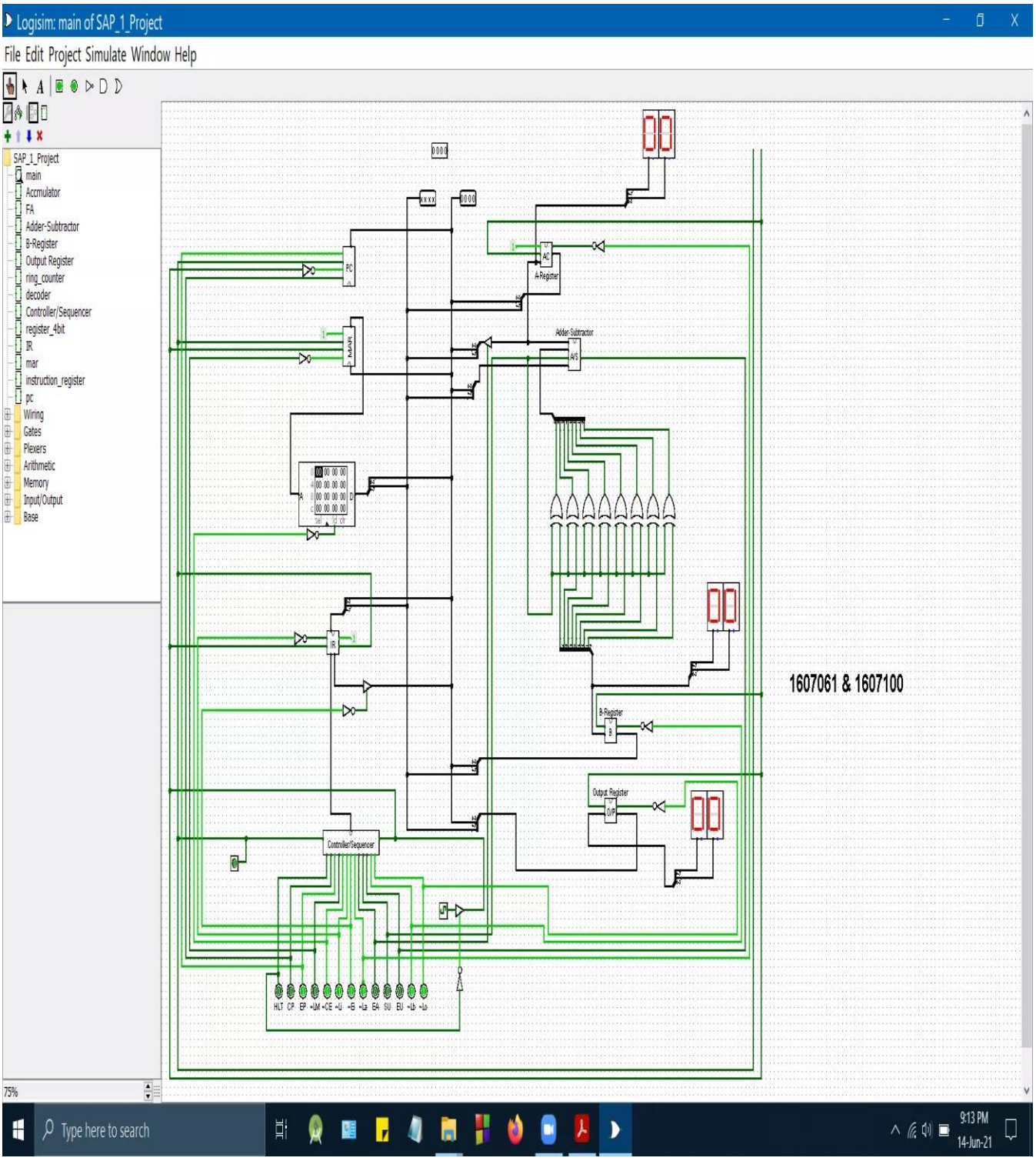

Fig2: Circuit Diagram

loads the accumulator word into the output register.

The output register is often called an output port because processed data can leave the computer through this register.

* Binary Display: The binary display is a row of 8 LEDs. Because, each LED connects to one flip-flop of the output port, the binary display can show the content of output register.

* Instruction set of SAP-1 computer:

There are only 5 instruction in SAP-1 computer. They are:-
LDA, ADD, SUB, OUT and HLT.

- LDA: LDA stands for "Load The Accumulator". A complete LDA instruction includes the hex address of data to be loaded.

- ADD : A complete add instruction includes the hex address of data to be added with the data of accumulator.

Ex : ADD 9H

This means Replace Acc with the Acc + data of 9H location.

- SUB : A complete SUB instruction includes the hex address of data to be subtracted with the data of accumulator.

Ex : SUB 7H

This means replace Acc with the Acc - data of 7H location.

- OUT : When the OUT instruction is executed, The SAP-1 computer transfer the accumulator content to output register.

- HLT: HLT instruction tells the SAP-1 computer to stop the program. It is must to use HLT at end of every SAP-1 program.

Discussion and Condusion:

In this project, the design of a SAP-1 computer is completed. Each and every component of SAP-1 computer is designed from scraeh in logisim. Finally by adding the component with the bus the SAP-1 computer is created. The successful run of a program in the SAP-1 computer has also done. By doing this project the important knowledge about SAP-1 computer is gathered. This knowledge will help us very much in future in designing complex computer So, the project is a successful one.