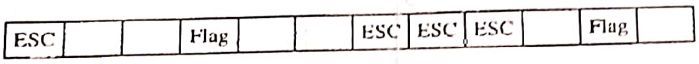
INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
UNA H.P.
An Institute of National Importance under MoE
Saloh, Una (HP) – 177 209
Website: www.iiitu.ac.in

School of Electronics
CURRICULUM: IIITUGECE22
Cycle Test - II
November 14, 2022
Time: 9:00 AM to 10:00 AM

Degree	B. Tech.	**Branch**	ECE
Semester	V		
Subject Code & Name	ECPE11: Data Communication and Networks		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	What is the definition of a linear block code? What is the definition of a cyclic code?	1
1.b	Find the minimum Hamming distance for the following cases: i. Detection of 3 errors or correction of 2 errors. ii. Detection of 6 errors or correction of 2 errors.	2 (1+1)
1.c	Using 5-bit sequence numbers, what is the maximum size of the send and receive windows for each of the following protocols? i. Selective Repeat ARQ ii. Go-Back-NARQ and Stop and wait ARQ	2
2.a	We need a data word of at least 11 bits. Find the values of *k* and *n* in the Hamming code *C(n, k)* with *dmin* ::: 3.	1
2.b	Illustrate direct and indirect packet delivery with examples.	2
2.c	i) Byte-stuff the data in Figure 1 and show the full frame format  Figure 1. ii) Bit-stuff the data given below and show the full frame format. 1000111111100111110100011111	2 (1+1)
3.a	Compare and contrast a circuit-switched network and a packet-switched network.	1
3.b	Explain an inter domain routing protocol with an example network.	2
3.c	Compare and contrast all forwarding techniques using network examples along with routing tables.	2
4.a	A sender sends a series of packets to the same destination using 5-bit sequence numbers. If the sequence number starts with 0, what is the sequence number after sending 100 packets?	1

4.b	Consider the network of Figure. Distance vector routing is used, and the following vectors have just come in to router C: from B: (5, 0, 8, 12, 6, 2); from D: (16, 12, 6, 0, 9, 10); and from E: (7, 6, 3, 9, 0, 4). What is C's new routing table? Give both the outgoing line to use and the cost.  	2
4.c	Figure 2 shows a state diagram to simulate the behavior of Stop-and-Wait ARQ at the sender site.  Figure 2 The states have a value of *Sn* (0 or 1). The arrows show the transitions. Explain the events that cause the two transitions labeled A and B.	2

**** GOOD LUCK ****

3(a) We need to make $k = n - m$ greater than or equal to 11, or $2^m - 1 - m \geq 11$

∴ for $m = 4$, $n = 2^4 - 1 = 15$ & $k = 15 - 4 = 11$ which satisfies condition $k \geq 11$

Code is C(15, 11)

3(b) $2^5 = 32$. So, starting sequence number will be '0' & ending sequence will be 31.

∴ 32nd packet's sequence number will be 31. Similarly 64th will also be 31. 96th packet will also be $31 \cdot 97^{th} = 0$, $98^{th} = 1$, $99^{th} = 2$, $100^{th} = 3$, 101^{th} =

3(c)(ii) Go-back N ARQ : Sender Window = Max size $= 2^m - 1 = 2^5 - 1 = 31$

Receiver window = Max size = always 1

Selective Repeat ARQ : Sender Window = Receiver Window = $\rightarrow$ at most one half of 2^m = one half of $2^5 = \frac{1}{2}$ of 32 =

Stop & Wait ARQ : Max size of sender & receiver window is 1.

3(a) Linear Block code is a code in which Exclusive OR (addition modulo-2) of two valid codewords creates another valid codeword. Cyclic code are special linear block code with one extra property. In cyclic code if codeword is cyclically shifted, the result is another codeword.

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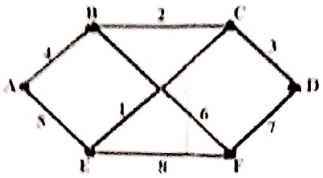
School of Electronics
CURRICULUM: IIITUGECE22
Cycle Test - II
October 09, 2023
Time: 09:00 AM to 10:00 AM

Degree	B. Tech.	Branch	ECE
Semester	V		
Subject Code & Name	ECPE11: Data Communication and Networks		
Time: 60 Minutes	Answer All Questions		Maximum: 20 Marks

Sl. No.	Question	Marks
1.a	What is the polynomial representation of result of 101110 after shifting two bits to the left?	1
1.b	Find the minimum Hamming distance for the following cases: i. Detection of 3 errors or correction of 2 errors. ii. Detection of 6 errors or correction of 2 errors.	2 (1+1)
1.c	Using 5-bit sequence numbers, what is the maximum size of the send and receive windows for each of the following protocols? i. Selective Repeat ARQ ii. Go-Back-NARQ and Stop and wait ARQ	2
2.a	Consider a data word of at least 11 bits. Find the values of k and n in the Hamming code $C(n, k)$ with $d_{min} = 3$.	1
2.b	Illustrate direct and indirect packet delivery with examples.	2
2.c	i) Byte-stuff the data in Figure 1 and show the full frame format ESC | | | Flag | | | ESC | ESC | ESC | | Flag | | Figure 1. ii) Bit-stuff the data given below and show the full frame format. 1000111111100111110100O111111	2 (1+1)
3.a	Compare and contrast a circuit-switched network and a packet-switched network.	1
3.b	Explain an inter domain routing protocol with an example network.	2
3.c	Compare and contrast all forwarding techniques using network examples along with routing tables.	2
4.a	A sender sends a series of packets to the same destination using 5-bit sequence numbers. If the sequence number starts with 0, what is the sequence number after sending 100 packets?	1
4.b	Consider the network of Figure 2. Distance vector routing is used, and the following vectors have just come in to router C: from B: (5, 0, 8, 12, 6, 2); from D: (16, 12, 6, 0, 9, 10); and from E: (7, 6, 3, 9, 0, 4). What is C's new routing table? Give both the outgoing line to use and the cost.	2

	 Figure 2.	
4.c	In Stop and wait protocol every 4th packet is lost and it is required to send total 10 packets. How many transmissions it will take to send all the packets?	2

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AY 2023-24
School of Electronics
CURRICULUM: IIITUGECE22
Cycle Test – II
09, Oct.'23

Degree	B. Tech.	**Branch**	ECE
Semester	V		
Subject Code & Name	ECPE21: DIGITAL SIGNAL PROCESSING		
Time: 60 Minutes	**Answer All Questions**	**Maximum: 20 Marks**	

Sl. No.	Question	Marks
1.a	Explain the concept of comb filter. How it can be used reject power supply pickup of 50Hz.	1
1.b	Derive the magnitude function $H(e^{jw})$ for symmetric linear phase FIR filter of length 7.	2
1.c	Briefly explain the different types of Complementary filters with their magnitude response characteristics.	2
2.a	Define an all pole low pass filter with its characteristics.	1
2.b	Obtain the transfer function of an analog Butterworth low pass filter with the specifications given as cut-off frequency $\Omega_c = 1$ and order of the filter $N = 7$.	2
2.c	Design an Chebyshev low pass filter with the specifications given below: $\delta_p = 0.8, \delta_s = 0.2, \Omega_p = 1Khz, \Omega_s = 4Khz$	2
3.a	Explain the difference between Analog and Digital filter design.	1
3.b	Obtain the direct form I, direct form II, and transposed realization for the following system: $y(n) = \frac{3}{4}y(n-1) - \frac{1}{8}y(n-2) + \frac{1}{3}x(n-1)$	2
3.c	Briefly explain the concept of transformation of normalized low pass filter in to de-normalized other kind of filters.	2
4.a	Consider an LTI system, initially at rest, described by the following difference equation: $y(n) = \frac{1}{4}y(n-2) + x(n)$ Determine the impulse response, $h(n)$, of the system.	1
4.b	Obtain the parallel structure for the following systems: $H(z) = \frac{2(1-z^{-1})(1+\sqrt{2}z^{-1}+z^{-2})}{(1+0.5z^{-1})(1-0.9z^{-1}+0.81z^{-2})}$	2
4.c	Compare FIR and IIR digital filter with the help of an example.	2

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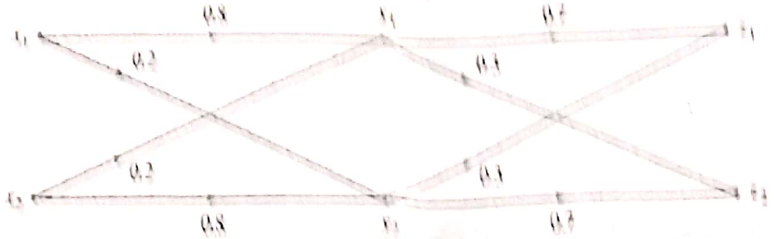
School of Electronics
CURRICULUM: IIITUGECE22
Cycle Test - II
09, Oct.' 23
09:00 AM-10:00 AM

Degree	B. Tech.	**Branch**	ECE
Semester	V		
Subject Code & Name	ECPE31: Communication Theory		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	State Shannon's information capacity theorem and derive the expression for limiting capacity of the channel.	1
1.b	Data is to be transmitted at the rate of 10000 bits/sec over a channel having bandwidth B = 3000 Hz. Determine the signal to noise ratio required if the bandwidth is increased to 10000 Hz.	2
1.c	For an AWGN channel with 4 kHz bandwidth and noise power spectral density $N_o/2 = 10^{-12}$ W/Hz, the signal power required at the receiver is 0.1mW. Calculate the capacity of this channel.	2
a	What is the channel Capacity of the binary Symmetric channel with an error probability of 0.2?	1
b	With the aid of the Shannon-Hartley theorem, explain why doubling the bandwidth of a channel while keeping a constant transmitting power will not automatically double the channel capacity.	2
	Consider a discrete memoryless source with alphabet {S0, S1, S2} and statistics (0.7, 0.15, 0.15) for its output. (i) Apply the Huffman algorithm to this source. Hence, show that the average code-word length of the Huffman code equals 1.3 bits/symbol. (ii) Let the source be extended to order two. Apply the Huffman algorithm to the resulting extended source and show that the average code-word length of the new code equals 1.1975 bits/symbol.	2
	Write the channel capacity of uniform dispersive channel and uniform focusing channel.	1

3.b	Two BSCs are connected in cascade, as shown in Fig. 1. (i) Find the channel matrix of the resultant channel. (ii) Find P(z1) and P(z2) if P(x1) = 0.6 and P(x2) = 0.4.  Fig. 1: Channel Diagram	2
3.c	Explain the source coding theorem with its definition indicators. Moreover, explain the different codes with examples.	2
4.a	Define Channel Coding Theorem. Write Kraft inequality.	1
4.b	Decode the message 0.572 given the coding model with Arithmetic Decoding Procedure.	2

Symbol	!	C	E
Probability	0.4	0.1	0.5

c	A DMS X has five symbols x_1, x_2, x_3, x_4, and x_5 with respective probabilities 0.2, 0.15, 0.05, 0.1, and 0.5. (i) Construct a Shannon-Fano code for X, and calculate the code efficiency. (ii) Repeat (i) for the Huffman code.	2

***** All The Best *****

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AY 2023-24
SCHOOL OF COMPUTING
CURRICULUM: HITUGCSE22
Cycle Test – II
10, Oct.'23

Degree	B. Tech.	**Branch**	CSE/IT/ECE
Semester	V		
Subject Code & Name	CSSE21 Relational Database Management Systems		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	Explain the problem of starvation. How can the problem of starvation be resolved?	(1)
1.b	Explain the difference between internal and external sorting. Which type of sorting is suitable for large databases?	(2)
1.c	Determine whether the given schedule S1 is strict, cascadeless, recoverable, or non-recoverable. Explain with appropriate reasons. S1: $r1(X)$; $r2(Z)$; $r1(Z)$; $r3(X)$; $r3(Y)$; $w1(X)$; $c1$; w3(Y); $c2$; $r2(Y)$; $w2(Z)$: $w2(Y)$; $c3$;	(2)
2.a	Why strict schedules are easy to recover as compared to cascadeless schedules?	(1)
2.b	Discuss briefly any four general transformation rules for query optimization. Explain with suitable examples.	(2)
2.c	How does query optimizer use left deep trees to optimize the query execution? Discuss using suitable example.	(2)
3.a	What are serial schedule and a serializable schedule? Why are a serial schedule and a serializable schedule considered correct?	(1)
3.b	What are the different cost components for query execution? Discuss each component using suitable examples.	(2)
3.c	Consider the following two transactions: T1: read(A); read(B); if A = 0 then B:= B + 1; write(B) T2: read(B); read(A); if B = 0 then A:= A + 1; write(A) Add lock and unlock instructions to transactions T1 and T2, so that they observe the two-phase locking protocol. Can the execution of these transactions result in a deadlock?	(2)
4.a	Why are locking techniques used for concurrency control in databases?	(1)
4.b	What is database catalog? How does database catalog help in selecting different algorithms for query execution?	(2
4.c	How is view serializability different from conflict serializability? If a schedule is view serializable, will it also be conflict serializable?	(

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AY 2022-23

School of Electronics

Cycle Test – II

14, November.'22

Degree	B. Tech.	**Branch**	ECE
Semester	V		
Subject Code & Name	ECPE22: Modelling and Testing of Digital Systems (VHDL)		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Q. No.		Questions	Marks
1.	a)	What is the basic unit of structural modeling?	[1]
	b)	Write down the VHDL Code for the 3 to 8 decoder using dataflow modeling.	[2]
	c)	Write down the VHDL Code for the D Flip-Flop using structural modeling.	[2]
2.	a)	What is inertial delay?	[1]
	b)	Write down the VHDL Code for the 1X8 multiplexer using dataflow modeling.	[2]
	c)	Write down the VHDL Code for the 2 to 4 decoder using structural modeling.	[2]
3.	a)	What is dataflow modeling?	[1]
	b)	Write down the VHDL Code for the full subtractor using dataflow modeling.	[2]
	c)	Write down the VHDL Code for the 1X4 multiplexer using structural modeling.	[2]
4.	a)	List the objects of VHDL.	[1]
	b)	Write down the VHDL Code for the binary to gray code converter using dataflow modeling.	[2]
	c)	Write down the VHDL Code for the 1-bit comparator using structural modeling.	[2]

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School of Electronics
CURRICULUM: IIITUGECE22
Cycle Test - II
November 15, 2022
Time: 9:00 AM to 10:00 AM

Degree	B. Tech.	**Branch**	ECE
Semester	V		
Subject Code & Name	ECPE32: Embedded Systems		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	What factors are considered in the selection of embedded memory selection?	1
1.b	How the data transfer is controlled in inter integrated circuit bus protocol? Explain with timing waveforms.	2
1.c	What is stepper motor? How is it different from ordinary dc motor?	2
2.a	What is Programmable Peripheral Interface (PPI)? Show the interfacing the 8255 PPI with an 8-bit controller.	1
2.b	Interpret the various states associated with a process and the state transitions with a neat diagram.	2
2.c	Compare Port I/O & Memory Mapped I/O.	2
3.a	Explain the various factors to be considered for the selection of a scheduling criteria	1
3.b	Which scheduling algorithm is best suited among FIFO, Round Robin, and Short Job First (SJF) in the following cases? Justify. i) The incoming processes are short and there is no need for the processes to execute in a specific order. ii) The processes are a mix of long and short processes and the task will only be completed if all the processes are executed successfully in a given time.	2
3.c	Three processes with process IDs P1, P2, P3 with estimated completion time 24, 3, 3 milliseconds respectively enter the ready queue together in order P2, P3, P1. Calculate the waiting time and Turn Around Time (TAT) for each process and the average waiting time and turnaround time.	2
4.a	Explain context switching. Why it is required?	1
4.b	Compare threads and processes in detail.	2
4.c	Explain the role of Watchdog Timer in Embedded System.	2

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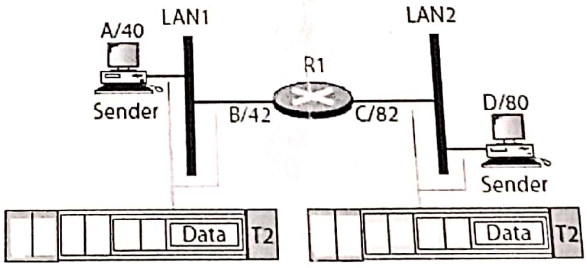
School of Electronics
CURRICULUM: IIITUGECE22
End Semester Examination
December 04, 2023
Time: 9:00 AM to 12:00 PM

Degree	B. Tech.	**Branch**	ECE
Semester	V		
Subject Code & Name	ECPE11: Data Communication and Networks		
Time: 180 Minutes	**Answer All Questions**	**Maximum: 100 Marks**	

Sl. No.	Question	Marks
1.a	In Fig. 1, assume that the communication is between a process running at computer A with port address ***i*** and a process running at computer D with port address ***j***. Create the packets and frames at the network, data link, and transport layer for each hop. At each transmission link address is mentioned as X/Y where X-Logical address and Y-Physical Address.  Fig. 1	5
1.b	How do the layers of the Internet model correlate to the layers of the OSI model? Mention the protocols with full names at each layer in TCP/IP model.	5 (2+3)
1.c	The loss in a cable is usually defined in decibels per kilometer (dB/km). If the signal at the beginning of a cable with -0.3 dB/km has a power of 2 mW, what is the power of the signal at 5 km?	5
1.d	Discuss the basic network topologies and cite an advantage of each topology.	5
2.a	Find the bandwidth for the following situations if a 5 KHz voice signal is to be modulated. i) AM ii) FM (Modulation index=5)	5 (2+3)
2.b	The telephone line has 4 KHz bandwidth. Calculate the maximum number of bits that can be sent using each of the following techniques. Let d =0. i) ASK ii) QPSK iii) 16-QAM iv) 64-QAM	5
2.c	Compare and contrast PCM and DM with respect to transmitter diagrams.	5