INDIAN INSTITUTE OF INFORMATION TECHNOLOGY UNA
HIMACHAL PRADESH
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Saloh, Una – 177 209
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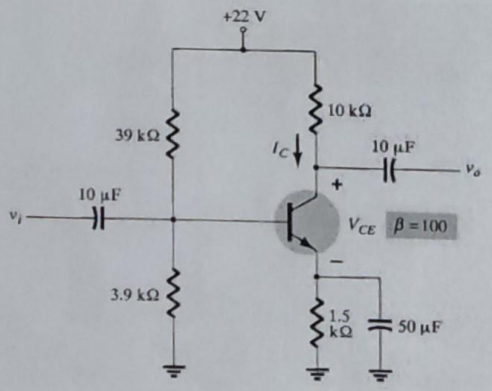
AY 2023-24
School of Electronics
CURRICULUM: IIITUGECE22
END SEMESTER EXAMINATION
26 Dec.' 2023 (9:00 – 12:00 hrs)

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC301: Electronic Devices and Circuits		
Time: 180 Minutes	**Answer All Questions**		**Maximum: 100 Marks**

S. No.	Question	Marks
1.a	State advantages and disadvantages of PN and Zener diode. Explain the working principle and construction of Zener diode in detail.	5
1.b	Explain the input and output characteristics of NPN transistor in CB configuration with transistor hybrid parameter models.	5
1.c	Draw the basic construction of a P-channel JFET. Apply the proper biasing between the drain and source and sketch the depletion region for $V_{GS} = 0V$.	5
1.d	Derive an expression of cut-in voltage and current of PN diode which are affected by temperature parameters. Also, show diagrammatically the variation in diode characteristics with temperature variation.	5
2.a	A transistor operating in CB configuration has I_C=2.98 mA, I_E=3.2 mA, and I_{CO}=0.02 mA. What current will flow in the collector circuit of this transistor when connected in CE configuration with I_B=30 μA?	5
2.b	Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration of Figure 1.  Figure 1	5

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AY 2022-23

School of Electronics

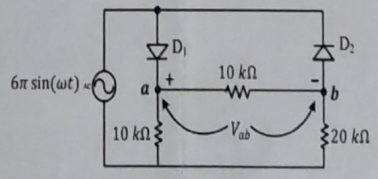
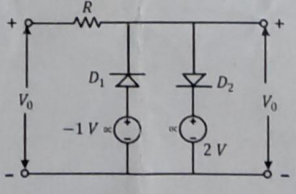
CURRICULUM: IIITUGECE22

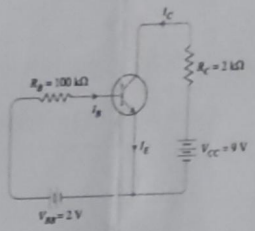
Cycle Test – II

28, Oct.'22

Time: 9:00AM-10:00AM

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC301: Electronic Devices and Circuits		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	State advantages and disadvantages of a photodiode and LED Diode.	(1)
1.b	Define Tunnel diode? Explain the operation of Tunnel diode with its equivalent circuit and mention its applications.	(2)
1.c	What is rectification? Explain the working of bridge full-wave rectifier with relevant circuit diagram and waveforms.	(2)
2.a	What is requirement of voltage multiplier? Also, draw the circuit diagram of voltage doubler.	(1)
2.b	In the Fig. 1, assume that the diodes D_1 and D_2 are ideal. Obtain the average value of voltage Vab (in volts) across terminals 'a' and 'b'.  Fig. 1	(2)
2.c	Two silicon diodes, with a forward voltage drop of 0.7 V, are used in the circuit shown in the Fig 2. Obtain the range of input voltage V_i for which the output voltage $V_0 = V_i$.  Fig. 2	(2)

3.a	What is Early effect? Explain how it affects the BJT characteristics in CB configuration.	(1)
3.b	A NPN BJT having reverse saturation current $I_S = 10^{-15}$ A is biased in the forward active region with V_{BE} = 700 mV and the current gain (β) may vary from 50 to 150 due to manufacturing variations. Determine the maximum emitter current (in μA) of BJT.	(2)
3.c	Explain input and output characteristics of NPN transistor in CB configuration with neat diagram.	(2)
4.a	For a BJT, the common – base current gain α is 0.98 and the collector base junction reverse bias saturation current I_{CO} is 0.6 μA. This BJT is connected in the common emitter mode and operated in the active region with a base drive current I_B = 20 μA. Calculate the collector current I_C for this mode of operation.	(1)
4.b	Draw the circuit diagram of a voltage divider bias and derive expression for Stability factor.	(2)
4.c	Fig. 3 shows biasing with base resistor method. (i) Determine the collector current I_C and collector-emitter voltage V_{CE} for β = 50. (ii) If R_B in this circuit is changed to 50 kΩ, find the new operating point. (Neglect small base-emitter voltage)  Fig. 3	(2)

**** GOOD LUCK *****

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School of Electronics

CURRICULUM: IIITUGECE22

Cycle Test - II

November 28, 2022, 02:00 PM-03:00 PM

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC302: Digital Circuits and Systems		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

S. No.	Question	Marks
1.a	Define the terms Combinational circuit and Sequential Circuit, and give suitable examples for each.	1
1.b	Minimize the following function (F_1) using suitable K-map and list out all the EPIs and NEPIs if any. $F_1(A,B,C,D) = \sum m\,(1,2,3,4,5,9,10,12,13,14) + \sum d\,(0,6,11)$	2
1.c	Design a circuit for the black box provided in Figure 1, that can accept two 2-bit numbers as inputs and provides 8-bit output as per the Table. In this Figure, Pin-7 is considered as the MSB and pin 0 is considered as LSB.	2
2.a	Implement Full adder circuit using Half adders and basic gates.	1
2.b	Implement the following functions of 'n' variables using the multiplexer of '(n-1)' selection lines using 'B' as input for F_2 and 'C' as input for F_3. $F_2(A,B,C,D) = \sum m\,(1,2,3,4,6,9,12,13,14)$ $F_3(A,B,C,D) = \sum m\,(0,2,5,9,11,14,15)$	2

S. No.	Condition	Output value in Hexadecimal
1.	A=B	$(02)_{16}$
2.	A<B	$(04)_{16}$
3.	A<B	$(10)_{16}$

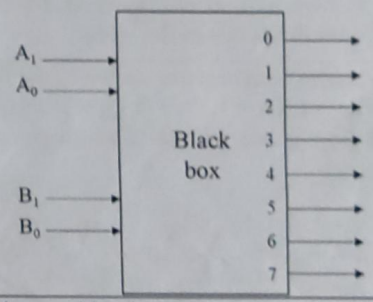
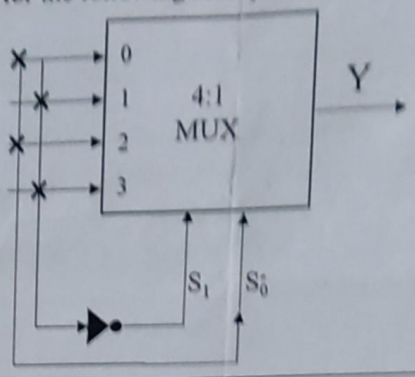
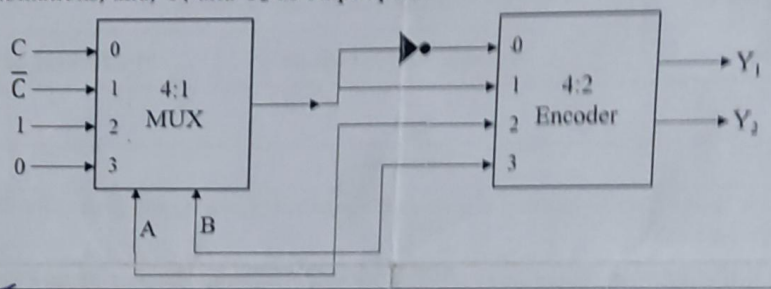
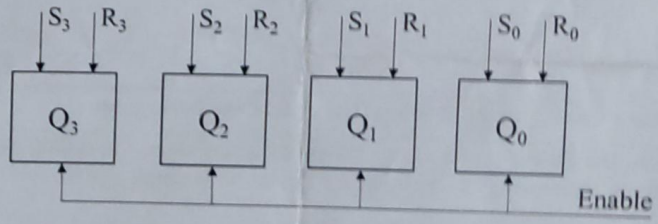


Figure 1:

2.c	Implement 32:1 MUX using only 4:1 MUX(s) and label the implementation clearly.	2
3.a	Write the truth table for the following multiplexer. 	1
3.b	Write the truth table for the following circuit by taking A, B and C as input combinations, and, Y_1 and Y_2 as output pins. 	2
3.c	Implement AND, OR, and XOR gates of 2 inputs (A and B), and, NOT gate of 1 input (A) using 2x1 multiplexer. Each gate needs to be implemented by one 2x1 multiplexer only by taking A as selection line. Assume all the literals (variables) and their complement are readily available.	2
4.a	Give the list of all flip-flops and explain the necessity of clock signal.	1
4.b	What is race around condition in JK-Flip-flop and explain how Master-Slave configuration addresses the issue.	2
4.c	Consider the 4-bit register shown in the Figure 2. If the initial value in the register is Enable = 1, $Q_3 = 1$, $Q_2 = 0$, $Q_1 = 1$, and, $Q_0 = 0$ (read as 1010). Mention the steps to replace the data with 0011 as the next state and write the excitation tables for the same.  **Figure 2:**	2

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CURRICULUM: IIITUGECE22

Cycle Test - II

November 28, 2022, 02:00 PM-03:00 PM

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC302: Digital Circuits and Systems		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

S. No.	Question	Marks
1.a	Define the terms Combinational circuit and Sequential Circuit, and give suitable examples for each.	1
1.b	Minimize the following function (F_1) using suitable K-map and list out all the EPIs and NEPIs if any. $F_1(A,B,C,D) = \sum m\,(1,2,3,4,5,9,10,12,13,14) + \sum d\,(0,6,11)$	2
1.c	Design a circuit for the black box provided in Figure 1, that can accept two 2-bit numbers as inputs and provides 8-bit output as per the Table. In this Figure, Pin-7 is considered as the MSB and pin 0 is considered as LSB.	2
2.a	Implement Full adder circuit using Half adders and basic gates.	1
2.b	Implement the following functions of 'n' variables using the multiplexer of '(n-1)' selection lines using 'B' as input for F_2 and 'C' as input for F_3. $F_2(A,B,C,D) = \sum m\,(1,2,3,4,6,9,12,13,14)$ $F_3(A,B,C,D) = \sum m\,(0,2,5,9,11,14,15)$	2

S. No.	Condition	Output value in Hexadecimal
1.	A=B	$(02)_{16}$
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3.	A<B	$(10)_{16}$

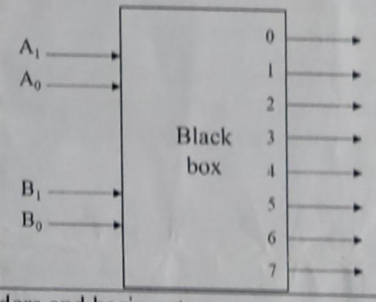
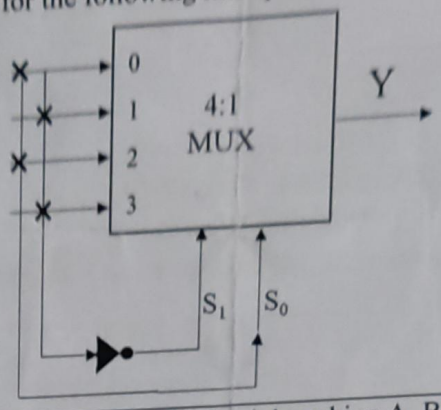
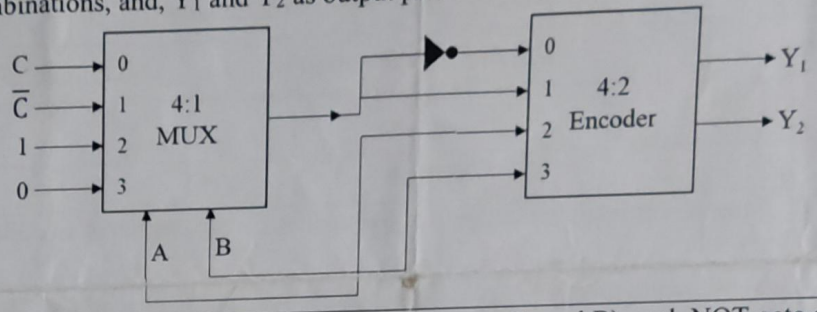
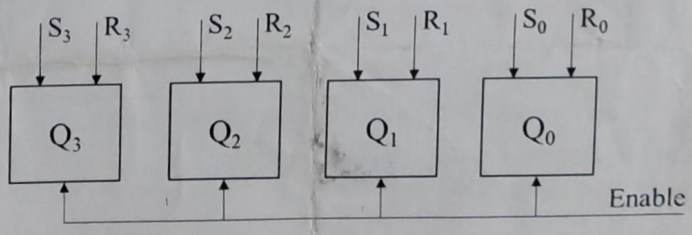


Figure 1:

2.c	Implement 32:1 MUX using only 4:1 MUX(s) and label the implementation clearly.	2
3.a	Write the truth table for the following multiplexer. 	1
3.b	Write the truth table for the following circuit by taking A, B and C as input combinations, and, Y_1 and Y_2 as output pins. 	2
3.c	Implement AND, OR, and XOR gates of 2 inputs (A and B), and, NOT gate of 1 input (A) using 2x1 multiplexer. Each gate needs to be implemented by one 2x1 multiplexer only by taking A as selection line. Assume all the literals (variables) and their complement are readily available.	2
4.a	Give the list of all flip-flops and explain the necessity of clock signal.	1
4.b	What is race around condition in JK-Flip-flop and explain how Master-Slave configuration addresses the issue.	2
4.c	Consider the 4-bit register shown in the Figure 2. If the initial value in the register is Enable = 1, $Q_3 = 1$, $Q_2 = 0$, $Q_1 = 1$, and, $Q_0 = 0$ (read as 1010). Mention the steps to replace the data with 0011 as the next state and write the excitation tables for the same.  **Figure 2:**	2

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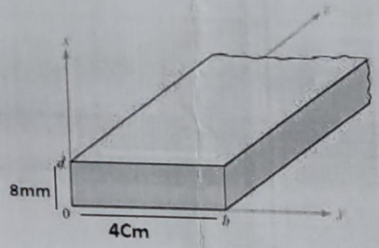
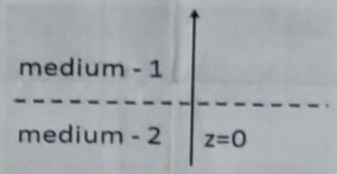
AY 2022-23
School of Electronics
Cycle Test – II
29, November '22

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC303: Electromagnetic Field Theory		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	Write True/False: i) Time-varying electric field produces magnetic field. ii) Time-varying magnetic field produces electric field.	(1)
1.b	The parallel-plate transmission line shown in the figure 1, with b=4cm and d=8mm, while the medium between the plates is characterized by $\mu_r = 1$, $\epsilon_r = 1$, and $\sigma = 0$. Neglect fields outside the dielectric. Given the field $H = 5Cos(10^9 t - \beta z)\vec{y}$ A/m. Use Maxwell's equation to help find $\beta, if\ \beta > 0$  Figure 1: Parallel-Plate Capacitors for Question 1b.	(2)
1.c	Considering the statement of Question 1(b); Find (i) displacement current density at z=0. (ii) total displacement crossing current the surface at $x = 0.5d;\ 0 < y < b;$ $0 < z < 0.1m$ in the $\vec{x}$ direction.	(2)
2.a	Write the four boundary conditions regrading electric and magnetic field at any surface of discontinuity.	(1)
2.b	The phasor electric field expression is given by: $\vec{E} = [a_x + \overrightarrow{E_y} a_y + (2 + 5j)a_z]e^{-j2.3(-0.6x+0.8y)}$. Find the following:	(2)

	a) $\widehat{E_y}$ b) Frequency and wavelength of wave	
2.c	Determine the current density function associated with the magnetic field given as: $\vec{H} = 2\rho\widehat{a_\rho} + 3\widehat{a_\theta} + Cos\theta\ \widehat{a_\phi}$	(2)
3.a	If electric field of plane wave is: $\vec{E}(z,t) = 3\cos(wt - kz + 30^0)\,\hat{x} - 3\sin(wt - kz + 45^0)\,\hat{y}$ (mV/m). The polarization state of plane wave is _____.	(1)
3.b	Derive the expression for parallel and perpendicular polarization of an electromagnetic wave reflected by a Perfect Dielectric for the case of normal incidence.	(2)
3.c	The space-time dependence of electric field of a linearly polarized light in free space is given as $\vec{E} = E_o Cos(\omega t - \beta z)\hat{x}$. Compute the value of the time average energy density associated with the electric field.	(2)
4.a	Explain depth of penetration. What will the expression be for a case of good conductor.	(1)
4.b	Two infinitely extended homogeneous isotopic dielectric media (medium-1and medium-2 with dielectric constant 2 and 5, respectively) meet at the $z = 0$ plane as shown in the figure 2. A uniform electric field exists everywhere. For $z \geq 0$, the electric field is given by $\vec{E} = 2\hat{\imath} - 3\hat{\jmath} + 5\hat{k}$. The interface separating the two media is charge free. Compute the value of electric displacement vector in the medium-2.  Figure 2: Parallel-Plate Capacitors for Question 4b.	(2)
4.c	Derive the expression for Brewster angle and Critical angle. What is the significance of both the angles.	(2)

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CURRICULUM: IIITUGECE22

Cycle Test – II

29, Nov.'22

Time: 02:00PM-03:00PM

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC304: COMMUNICATION SYSTEMS		
Time: 60 Minutes	**Answer All Questions**		**Maximum: 20 Marks**

Sl. No.	Question	Marks
1.a	Explain under sampling, over sampling and critical sampling process.	1
1.b	An angle modulated signal is given by $S(t) = 10\cos[2\pi 10^6 t + 20sin250t + 30\sin 250t]$. Find Maximum Frequency deviation and Maximum Phase deviation.	2
1.c	A receiver is tuned to 1MHz station. Intermediate frequency (I.F.) is 455KHz and Quality factor is 80. (i) Find Image Rejection Ratio. (ii) Find Image rejection ratio if receiver is tuned to 15 MHz.	2
2.a	Draw the block diagram of Super-heterodyne receiver for FM.	1
2.b	Find the Nyquist rate for the following signals: (i) $sinc\ 100t * sinc\ 200t$ (ii) $sinc\ 200t . sinc\ 300t$	2
2.c	Discuss the Direct method for generation of Frequency Modulation in detail.	2
3.a	Why amplitude limiter cannot be used in case of Amplitude modulation? Justify it.	1
3.b	Draw block diagram of Pulse Code Modulation scheme and explain each of the block.	2
3.c	A message signal $10\cos 2\pi 10^4 t$ is transmitted using PCM. Each sample is encoded with 8 bits. Find all possible parameters of PCM.	2
4.a	What is the need of Pre-emphasis and De-emphasis used in Analog Communication.	1
4.b	Explain the working of Tuned Radio Frequency receiver for AM.	2
4.c	A message signal is transmitted by using PCM such that maximum quantization error should be atmost of 1% of peak to peak amplitude of message signal. Find the minimum number of bits per sample required.	2

****** GOOD LUCK *******