INDIAN INSTITUTE OF INFORMATION TECHNOLOGY UNA
HIMACHAL PRADESH
An Institute of National Importance under MoE
Saloh, Una – 177 209
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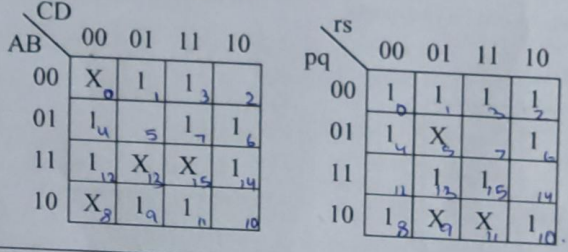
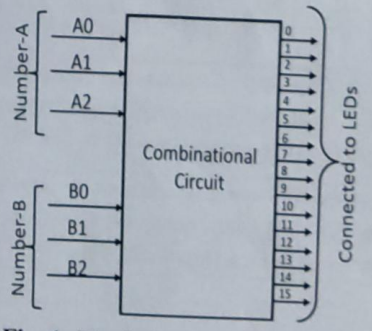
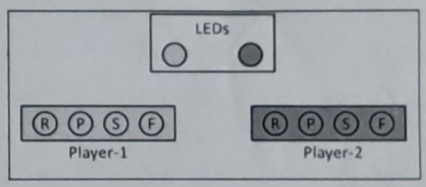
AY 2023-24
School of Electronics
CURRICULUM: IIITUGECE22
End Semester Examination
December 27, 2023, 09.00 am - 12.00 noon

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC302 – Digital Circuits and Systems		
Time: 180 Minutes	**Answer All Questions**		**Maximum: 100 Marks**

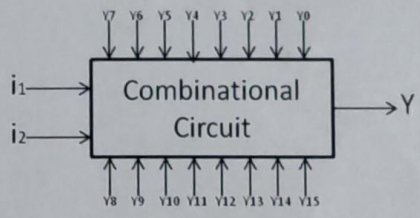
Sl. No.	Question	Marks
1.a	Perform the following conversions: i) Convert $(362.45)_{10}$ into Binary number system. ii) Convert $(643.25)_8$ into Decimal number system. iii) Convert the Decimal number obtained in (ii) to Hexadecimal number system. iv) Convert $(110011.1011)_2$ into Decimal number system. v) Convert $(6DB3)_{16}$ into Octal number system	5
1.b	Functions $F_1(A, B, C, D)$ and $F_2(p, q, r, s)$ are given as follows: Write the function in terms of minterms and reduce the function using suitable k-map. Implement the reduced function using only 2 input gates.  	5
1.c	Design a combinational circuit for the scenario shown in Fig. 1: Circuit has two 3-bit numbers A and B as inputs, the combinational circuit must perform the addition of 2 numbers and the LED corresponding to the result needs to be turned ON. For example, if A is 100, B is 101 then LED 9 must be turned ON. Draw the appropriate block schematic of the combinational circuit. Further give the complete internal circuit of the block at least once. (Circuit with minimum complexity will be much appreciated and attracts more marks.)  **Fig. 1:** Block diagram of the circuit	5

1.d	Design a 2-bit magnitude comparator using the multiplexers with n-1 selections lines, where 'n' represents number of input bits.	5
2.a	Let us consider a game named, "Rock (R)-Paper (P)-Scissor (S)-Fire (F)", which is being played between two players P1 and P2. In this game both the players have a choice to choose any word from R-P-S-F which are provided in the form of switches (as per Fig. 2). A player is said to be the winner based on the priorities assigned, as per the Table-1, to each word among R-P-S-F. Each player is assigned with an LED which glows when the player wins the round. Suppose P1 has chosen R button and P2 has chosen S button, then the LED corresponding to P1 will glow and if both the players press same button both the LEDs must turn ON. Design a combinational circuit which is connecting the switches of both the players to the respective LEDs. Draw the block diagram containing the inputs and outputs and mention any assumptions clearly before proceeding for the design. **Table-1:** Priority Table **Fig.2:** Scenario of the Game	5
2.b	Design the combinational circuit for the truth table, given in Table-2, by taking Fig. 3 as reference. In Fig. 3 first pin is Y0 and last pin is Y15 in order i.e., Y0, Y1, Y2 ... Y15. (**Design restrictions: Do not use basic or derived gates for the design; Pins alignment order should not be changed**). **Table-2**: Truth Table **Fig. 3:** Block Diagram of the Circuit	5
2.c	Define a Flip-flop. Explain the reason(s) in detail for occurrence of race-around condition in level-triggered JK Flip-flop and suggest the suitable measures to avoid it. Illustrate the race around condition and the measures to avoid it using the waveforms.	5
2.d	Perform the following operations by providing all the steps in details: (i) Convert a SR Flip-flop to JK Flip-flop. (ii) Convert a D Flip-flop to SR Flip-flop.	5

	R	P	S	F
R	-	P	R	R
P	P	-	S	F
S	R	S	-	F
F	R	F	F	-



Control lines		Output
i_1	i_2	Y
0	0	Y1
0	1	Y2
1	0	Y4
1	1	Y8



3.a	Design a 4-bit Universal Shift register using D-Flipflops and 4x1 Multiplexers for the conditions shown in Table-3. **Table-3:** Conditions for 4-bit Universal Shift register **Combination of selection lines** / **Condition** **S1** | **S0** 0 | 0 | Shift left 0 | 1 | Shift right 1 | 0 | Parallel-In Parallel-Out 1 | 1 | Buffer	5
3.b	Design a stopwatch that can count maximum time of 60 seconds and minimum time of 1 millisecond. This stop watch needs to have a button that activates the timer on pressing it and stops the timer on releasing it. Assume that clock of 15kHz, binary to BCD converters, BCD to 7-segment display converters, and negative edge triggered T Flip-flops are available for the design. Usage of any logic gate is permitted as a supporting gate with a valid requirement.	5
3.c	Design an arbitrary sequence counter using JK Flipflop, that would count the sequence 2, 3, 6, 4, 0, 2, 3, 6, 4, 0 and so on. To make sure that the arbitrary sequence counter is not struck at any unknown state, all the unknown states must be reset to zero. Draw the waveform for six clock pulses to represent the arbitrary sequence counter.	5
3.d	Explain the functionality of a 4-bit parallel-in and serial-out shift register with block diagram, clock pulse chart and waveform by taking an example of loading and unloading a 4-bit binary number.	5
4.a	Explain about the ring counter and the twisted ring counter with the help of block diagram, clock pulse chart and waveform.	5
4.b	Compare TTL and CMOS logic families based on the Voltage levels and Noise margin. Draw the diagrams or waveforms wherever necessary.	5
4.c	What are the devices used in the Unipolar logic family? Explain the working of the devices when the input is high and low. Draw the neat diagrams wherever necessary.	5
4.d	What is a DAC? Draw the block diagram of R-2R ladder type DAC and derive the expression for converting 3-bit data into analog voltage value.	5
5.a	Implement OR gate and XOR gate using CMOS Logic.	5
5.b	Implement the following functions using CMOS Logic: $F_3 = \overline{(AB + C).(D + EF)}$; $F_4 = AB + CD$	5
5.c	Write the design code and test bench for module definition in Verilog to implement a 2-bit comparator using behavioral model. Optimized logic has to be used for implementation.	5
5.d	Write the design code and test bench code for module definition in Verilog to implement 4-bit asynchronous counter.	5

*****GOOD LUCK*****

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AY 2023-24

School of Electronics

CURRICULUM: IIITUGECE22

End Semester Examination

28, Dec.'2023 (9:00 – 12:00 hrs)

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC303: Electromagnetic Field Theory		
Time: 180 Minutes	**Answer All Questions**		**Maximum: 100 Marks**

Q. No.		Question	Marks
1.	a.	Define wave polarization. Graphically illustrate linear, circular, and elliptical polarization. Discuss the conditions to achieve linear, circular, and elliptical polarization.	(5)
	b.	If a point $P(x,y,z)$ in Cartesian coordinate system is expressed by point $P(r,\theta,\phi)$ in spherical coordinate system, then show that: $r = \sqrt{x^2+y^2+z^2}$ $\theta = \tan^{-1}\left(\frac{\sqrt{x^2+y^2}}{z}\right)$ $\phi = \tan^{-1}\left(\frac{y}{x}\right)$ Also, verify the following equations: $x = r\sin(\theta)\cos(\phi)$ $y = r\sin(\theta)\sin(\phi)$ $z = r\cos(\theta)$	(5)
	c.	Define characteristic impedance of a transmission line. Draw L-type equivalent circuit model of two-conductor transmission line. Derive the transmission line equations (voltage and current wave equations).	(5)
	d.	Express the point $P(-2,6,3)$ in cylindrical and spherical coordinates.	(5)
2.	a.	Points P and Q are located at (0,2,4) and (-3,1,5). Find out a vector parallel to PQ with magnitude of 10.	(5)
	b.	Two point charges $1mC$ and $-2mC$ are located at (3,2,-1) and (-1,-1,4) respectively. Calculate the electric force on $10nC$ charge located at (0,3,1) and the electric field intensity at that point.	(5)

	c.	Derive the Poisson's and Laplace's equations. Write down at least one application of Laplace's equation.	(5)
	d.	Why a perfect conductor is termed as equipotential body?	(5)
3.	a.	Determine the divergence of the following vector field 'A' $A = yza_x + 4xya_y + ya_z$ and evaluate them at a point $P(1,-2,3)$.	(5)
	b.	Given that the electric field intensity $E = (3x^2 + y)a_x + xa_y$ kV/m Find the work done in moving a $-2\mu C$ charge from point (0,5,0) to point (2,-1,0) in a straight line path.	(5)
	c.	Two point charges Q_1 and Q_2 having magnitudes 4 nC and 6 nC respectively are placed at (1,1) and (5,7) respectively. Find the equation of the locus on which the electric field intensities due to Q_1 and Q_2 are equal.	(5)
	d.	An air line has a characteristic impedance of 70 Ω and a phase constant of 3 rad/m at 100 MHz. Calculate the inductance per meter and the capacitance per meter of the line.	(5)
4.	a.	Define Dispersion. Explain the cause of dispersion in lossy dielectric medium?	(5)
	b.	Determine the polarization of a plane wave with: $E(z,t) = 4e^{-0.25z}\cos(\omega t - 0.8z)a_x + 3e^{-0.25z}\sin(\omega t - 0.8z)a_y$ V/m	(5)
	c.	A lossy dielectric has an intrinsic impedance of $200\angle 30^\circ\ \Omega$ at a particular radian frequency ω. If, at that frequency, the plane wave propagating through the dielectric has the magnetic field component $H = 10e^{-\alpha x}\cos\left(\omega t - \frac{1}{2}x\right)a_y$ A/m Find E and α.	(5)
	d.	A lossless transmission line with $Z_o = 50\Omega$ is 30 m long and operates at 2 MHz. The line is terminated with a load $Z_L = 60 + j40\ \Omega$. If $u = 0.6c$ on the line, where c is the speed of light in vacuum, Determine the following: i. The reflection coefficient ii. The standing wave ratio iii. The input impedance	(5)
5.	a.	A distortionless line has $Z_o = 60\Omega$, $\alpha = 20$ mNp/m, $u = 0.6c$, where c is the speed of light in vacuum. Find R, L, G, C, and λ at 100 MHz.	(5)
	b.	Write down the generalized Maxwell's equations both in differential and integral form. Discuss the physical significance of each Maxwell equation.	(5)
	c.	"Maxwell's fourth equation (based on Ampere's circuit law) would be same under static fields as well as time-varying fields." Is the given statement true or false? Justify the answer.	(5)
	d.	State and verify Poynting theorem. Enlist the applications of Poynting theorem.	(5)

***** ALL THE BEST *****

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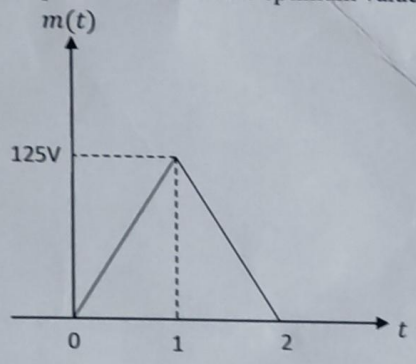
END SEMESTER EXAMINATION
29, December'23

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC304: Communication Systems		
Time: 180 Minutes	**Answer All Questions**		**Maximum: 100 Marks**

Sl. No.	Question	Marks
1.a	Draw the spectrum for multi-tone AM and explain the effect of total modulation index on total power, sideband power, and efficiency for multi-tone AM.	5
1.b	An AM signal $s(t)$ is given by the following equation: $s(t) = 4\cos 3200\pi t + 10\cos 4000\pi t + 4\cos 4800\pi t$ Find the value of Bandwidth, Total Power, Sideband Power, Efficiency, and $\frac{P_C}{P_t}$.	5
1.c	Discuss the concept of Quadrature null effect in DSB-SC using the mathematical equations.	5
1.d	A carrier signal of $10\cos(4\pi \times 10^5 t)$ is Amplitude modulated by a message signal of $4\cos(\pi \times 10^4 t)$ with $\mu = 0.5$. Find the value of carrier power, total power, sideband power, bandwidth, and efficiency.	5
2.a	Derive the mathematical expression for single-tone FM in terms of Bessel's Function.	5
2.b	Draw the circuit diagram for the envelope detector and explain the concept of choosing the optimum value of $R_L C$ for envelope detector.	5
2.c	Find the value of maximum frequency and deviation ratio for the signal $s(t)$ given below: $s(t) = 10\cos[\omega_c t + 5\sin 3000t + 10sin2000\pi t]$	5
2.d	Write down the difference between Frequency Multiplier and Mixer and justify the answer using the suitable examples.	5
3.a	Explain the Armstrong method for the generation of Frequency Modulation.	5
3.b	Thirty message signals each bandlimited to 20KHz are multiplexed using FDM with Guard band value equal to 2KHz. Find the multiplexed bandwidth scheme for the following type of modulation: (i) AM (ii) SSB	5

3.c	Draw the circuit diagrams used for improving the Fidelity of a receiver and justify the answer with mathematical analysis.	5
3.d	For the FM super-heterodyne receiver, find the required value of intermediate frequency to receive IRR=138, when the receiver is tuned to 25MHz station at Q=100.	5
4.a	A message signal of $4\cos(2\pi \times 10^3 t)$ is transmitted by using 3-bit PCM system. Find the value of the following parameters: i) Step size, bit rate, and bandwidth. ii) The quantizer and encoder output at the sampled values given as: [-3.5V, -2.6V, -1.1V, 0.5V, 2.2V, 3.8V]	5
4.b	Explain the relationship between inter-symbol interference and bandwidth of a raised cosine pulse.	5
4.c	Twenty message signals are multiplexed using TDM and the speed of commutator is 4000 rotations per second. Find the value of R_b in case of synchronization requires following number of extra bits: (i) 6 extra bits per each frame (ii) 2 extra bits per each sample (iii) 20% extra bits per each frame Assume each sample is encoded with 8 bits.	5
4.d	Explain the reason of preferring DPCM over PCM with suitable diagrams and mathematical expressions.	5
5.a	The message signal shown in Fig. 1, is transmitted using delta modulation with pulse rate of 1000 pulses per second. Find the optimum value of step size.  Fig. 1: Message signal for Problem 5.a	5
5.b	Explain the reason of choosing integer number of cycles of $c(t)$ in one T_b for ASK. Calculate the transmission bandwidth requirements for ASK using its spectrum.	5
5.c	A message signal of $10\cos 2\pi \times 10^4 t$ is given to 1024 level PCM system and the resulting binary sequence is transmitted through free space using binary signaling scheme. Find the transmission bandwidth, if the following type of modulation scheme is used: (i) ASK (ii) FSK.	5
5.d	Draw the block diagram and constellation diagram for QPSK modulation scheme with its mathematical expressions.	5

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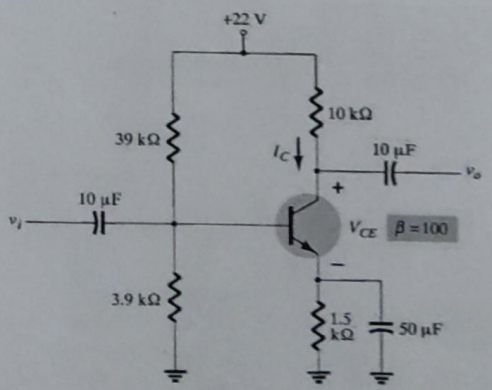
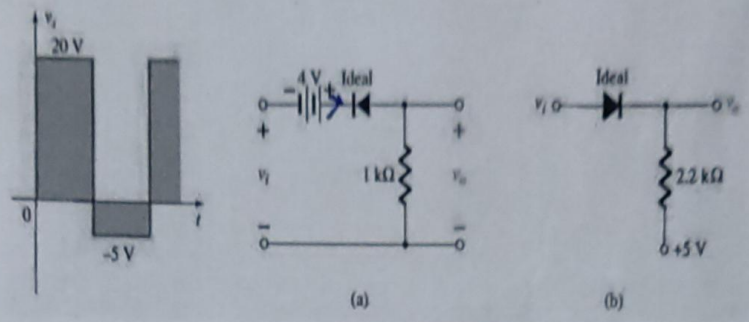
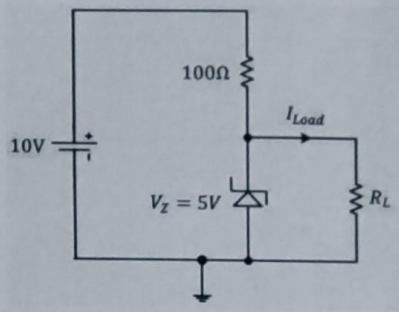
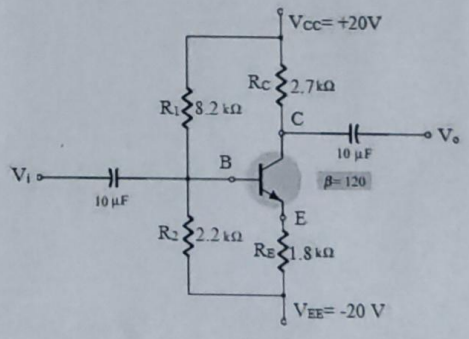
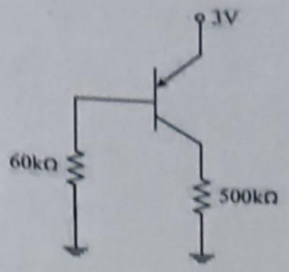
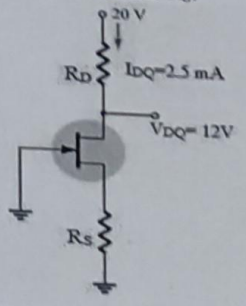
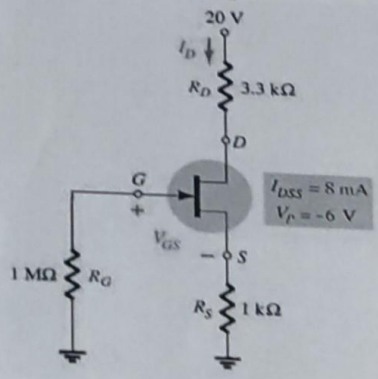
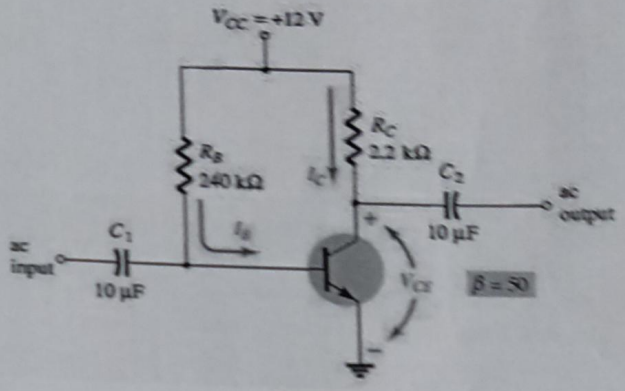
END SEMESTER EXAMINATION
26 Dec.' 2023 (9:00 – 12:00 hrs)

Degree	B. Tech.	**Branch**	ECE
Semester	III		
Subject Code & Name	ECC301: Electronic Devices and Circuits		
Time: 180 Minutes	**Answer All Questions**		**Maximum: 100 Marks**

S. No.	Question	Marks
1.a	State advantages and disadvantages of PN and Zener diode. Explain the working principle and construction of Zener diode in detail.	5
1.b	Explain the input and output characteristics of NPN transistor in CB configuration with transistor hybrid parameter models.	5
1.c	Draw the basic construction of a P-channel JFET. Apply the proper biasing between the drain and source and sketch the depletion region for $V_{GS} = 0V$.	5
1.d	Derive an expression of cut-in voltage and current of PN diode which are affected by temperature parameters. Also, show diagrammatically the variation in diode characteristics with temperature variation.	5
2.a	A transistor operating in CB configuration has I_C=2.98 mA, I_E=3.2 mA, and I_{CO}=0.02 mA. What current will flow in the collector circuit of this transistor when connected in CE configuration with I_B=30 μA?	5
2.b	Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration of Figure 1.  Figure 1	5

2.c	Determine V_0 for each network shown in Figure 2.  Figure 2	5
2.d	In Figure 3, the knee current of the ideal Zener diode is 10 mA. Find out the minimum value of R_L in Ω and the minimum power rating of the Zener diode in mW to maintain 5 V across R_L.  Figure 3	5
3.a	Can a transistor be constructed by simply connecting two separate diodes back to back? Why emitter region is heavily doped, base width is small and collector area is large in transistor?	5
3.b	Why is it preferred to locate the Q point at the center of the active region for amplification purposes? Obtain the stability factor of NPN transistor for the collector to base biasing.	5
3.c	Explain the base width modulation of BJT in detail. Determine V_C and V_B for the network shown in Figure 4.  Figure 4	5

3.d	Explain the thermal runway in BJT. In the circuit shown in Figure 5, the BJT has a current gain (β) of 50. Find V_{EC} for V_{EB} = 600 mV.  Figure 5	5
4.a	What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? Explain the operation and characteristics of P-channel JFET. Further, determine the trans-conductance, drain current, input and output resistance.	5
4.b	For the voltage-divider bias configuration given in Figure 6, the levels of V_{DQ} and I_{DQ} are specified. Determine the required values of R_D and R_S.  Figure 6	5
4.c	For the network given in Figure 7, determine the following: i) V_{GS} ii) I_D iii) V_{DS} iv) V_S v) V_D  Figure 7	5
4.d	Sketch the transfer and drain characteristics of an N-channel depletion-type MOSFET with I_{DSS} = 12 mA and V_P = -8 V for a range of V_{GS} = -V_P to V_{GS} = 1 V.	5
5.a	Discuss the difference between analog and power diodes. Explain the construction, equivalent circuit, operation, V-I characteristics, and salient features of TRIAC diode.	5

5.b	What is the difference between the construction of an enhancement type and a depletion type MOSFET? Explain the operation and characteristics of the N-channel MOSFET enhancement type. Also, obtain the equation of drain current after consideration of channel length modulation.	5
5.c	For the network given in Figure 8, determine the following: i) I_B ii) I_C iii) V_{CE} iv) V_{BC} v) V_B  Figure 8	5
5.d	Describe the working principle of SCR with V-I characteristics in detail.	5

Good Luck