FPGA Development for Radar, Radio-Astronomy and Communications

THE RADAR MASTERS COURSE

Dept. Electrical Engineering, University of Cape Town
Private Bag, Rondebosch, 7701, South Africa

http://www.rrsg.uct.ac.za

Presented by John-Philip Taylor

Convened by Dr Stephen Paine

Day 3 – 29 April 2022

Outline

Pipelines

Streaming Processors

Memory-Mapped Bus

Pulse-width Modulation

High Resolution PWM

Outline

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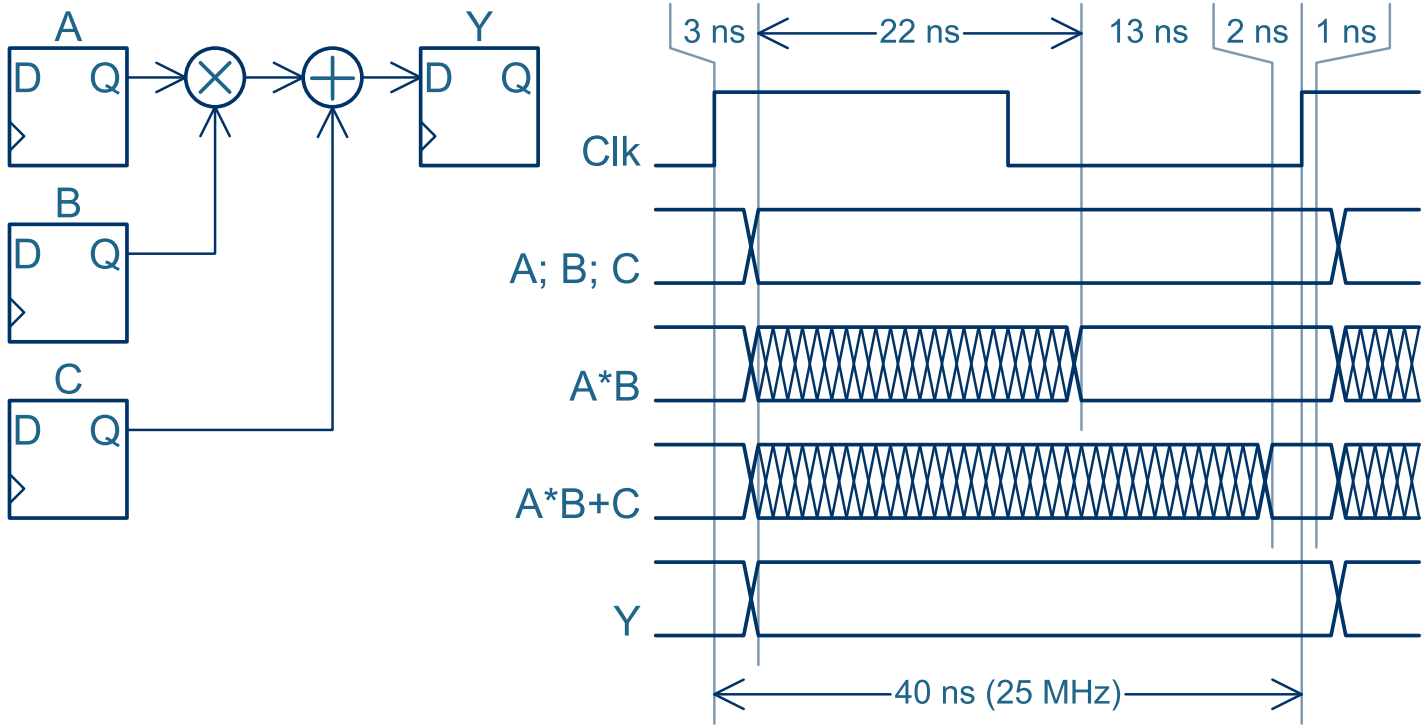
Simple Pipelines



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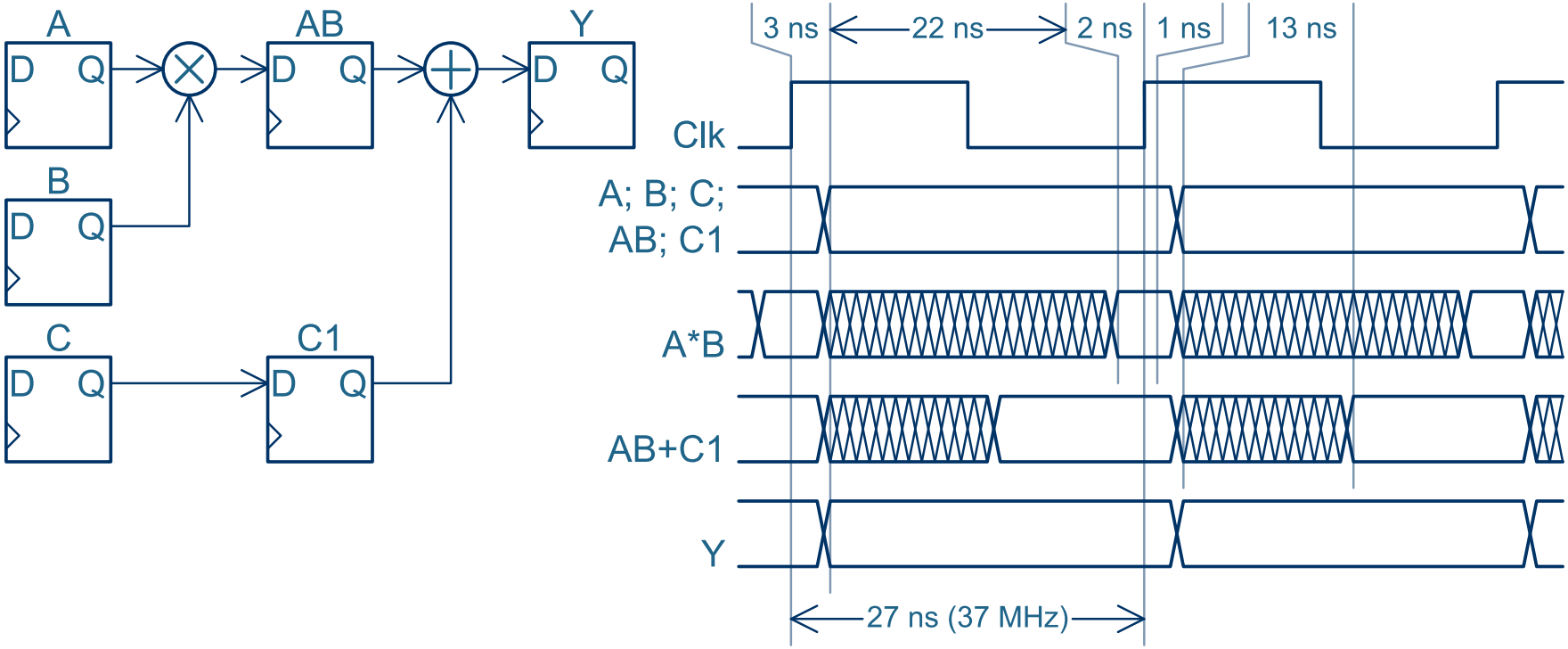

Simple Pipelines

- Gain throughput at the cost of latency and resources
- Often easier to use arrays, especially with long chains
- Keep the index equal to the stage which assigns the value

```
always @(posedge ipClk) begin
  // Stage 1
  AB <= A*B;
  C1 <= C;

  // Stage 2
  Y <= AB + C1;
end
```

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reg [7:0]C[1:0];

always @(posedge ipClk) begin
  // Stage 0
  C[0] <= C_Input;

  // Stage 1
  AB   <= A*B;
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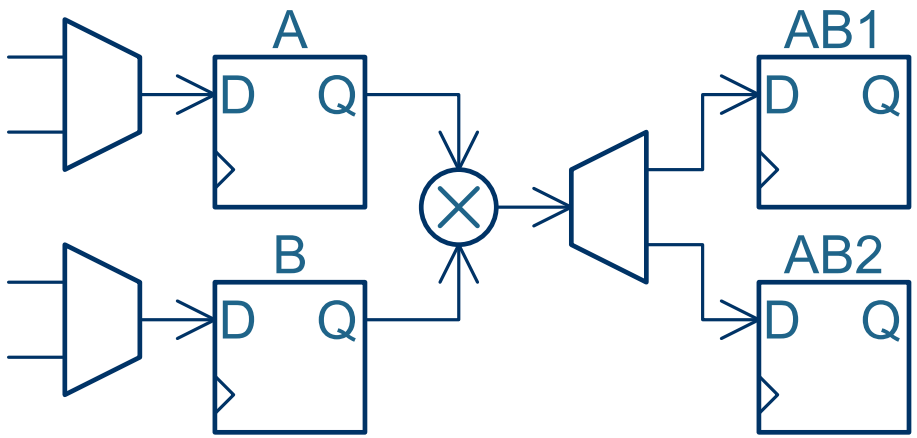
Sharing Resources


```
reg  [ 7:0]A, B;
wire [15:0]AB = A * B;

State1: begin
   AB2    <= AB;
   A      <= A1;
   B      <= B1;
   State  <= State2;
end

State2: begin
   AB1    <= AB;
   A      <= A2;
   B      <= B2;
   State  <= State1;
end
```



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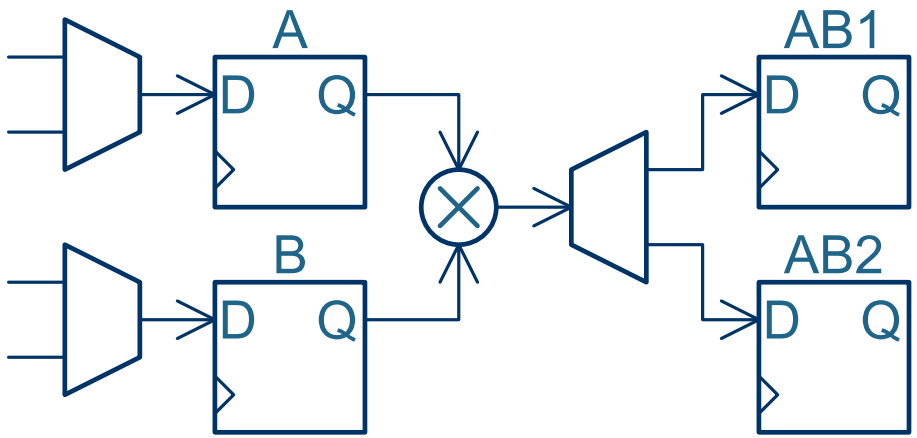

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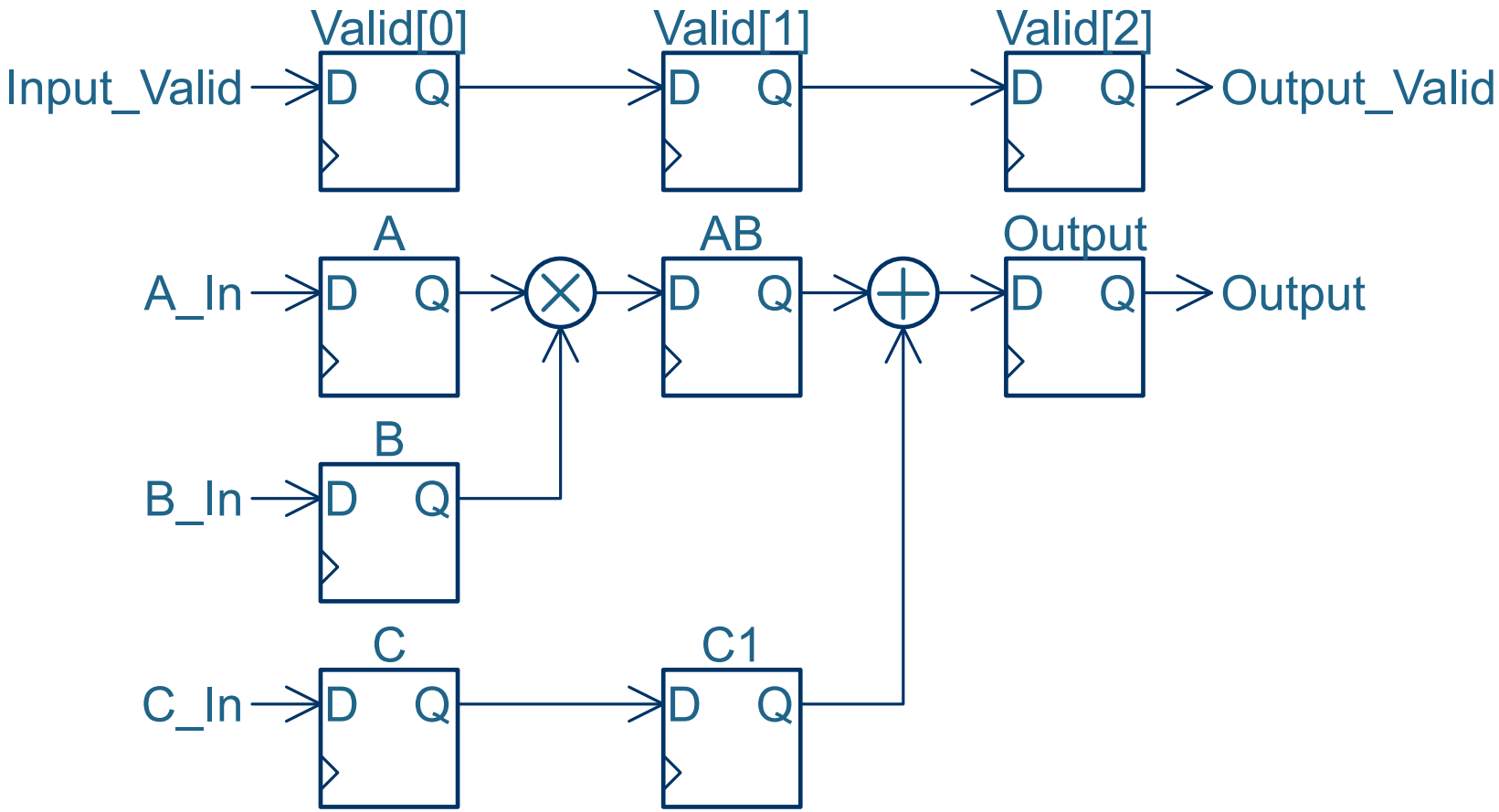
Stream Pipeline



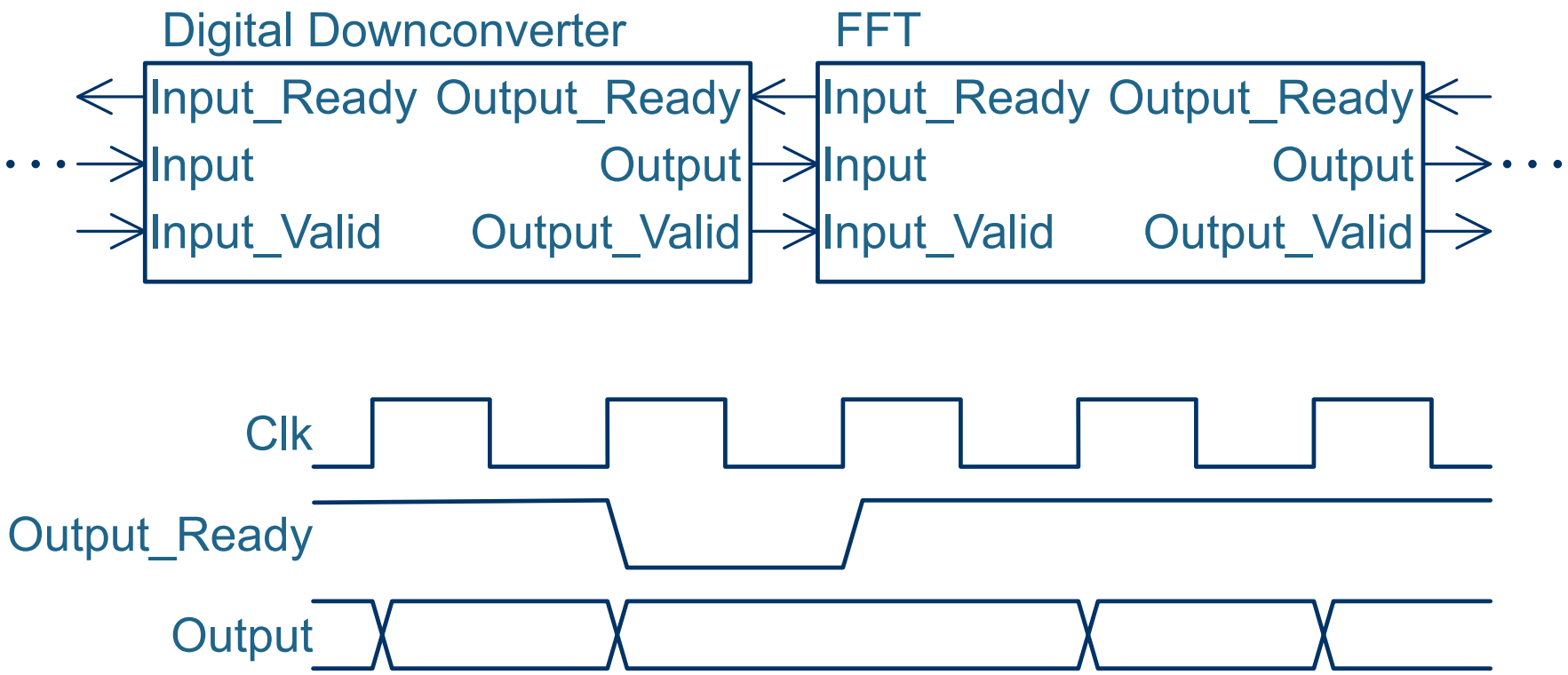
Stream Pipeline


```
reg [2:0]Valid;

always @(posedge ipClk) begin
  // Input
  A      <= A_In; B <= B_In; C <= C_In;
  Valid <= {Valid[1:0], Input_Valid};

  // Stage 1
  AB <= A*B;
  C1 <= C;

  // Stage 2
  Output <= AB + C1;
end

assign Output_Valid = Valid[2];
```

Back-pressure


```
reg [2:0]Valid;

always @(posedge ipClk) begin
  if(Output_Ready) begin
    // Input
    ...

    // Stage 1
    ...

    // Stage 2
    Output <= AB + C1;
  end
end

assign Input_Ready  = Output_Ready;
assign Output_Valid = Valid[2];
```

Streaming Processor



Handshaking Strategies

Different buses have different handshaking strategies:

- An Avalon source is allowed to wait for the sink to be ready before asserting the `Valid`.
- An AXI sink is allowed to wait for the source to be valid before asserting its `Ready`.
- A Wishbone slave must wait for valid data from the master before asserting its `Ack`.

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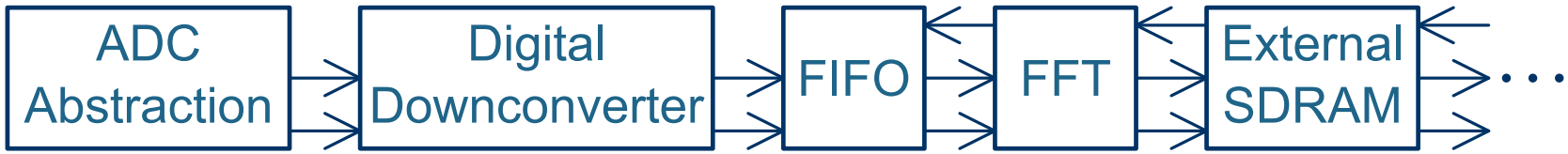
FIFO Queues



- Back-pressure makes it possible to move all the FIFO queues into a single queue
- Generally put the queue where the least amount of data is (saves resources)
- DSP chains have processing gain, so place the FIFO early in the chain

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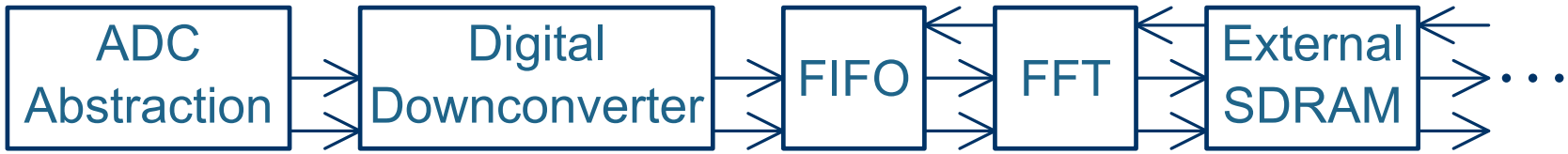

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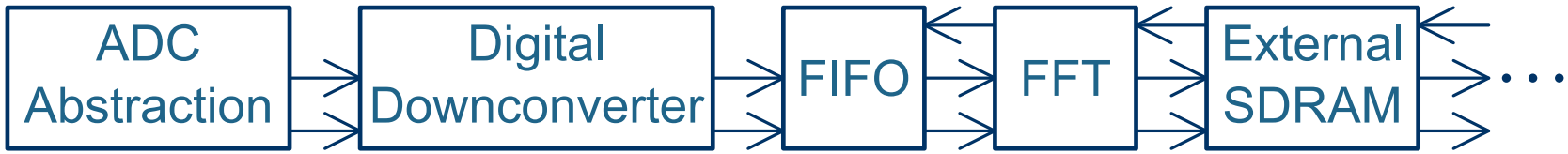

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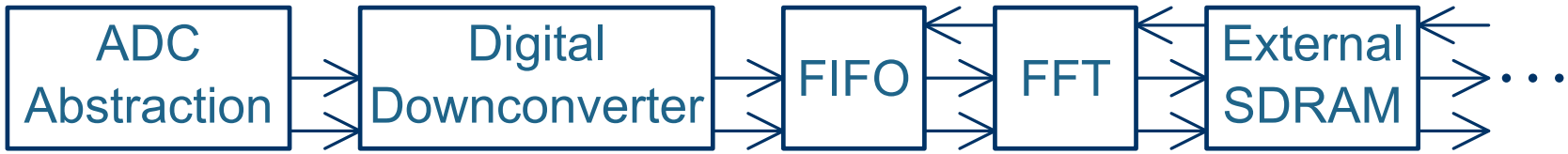

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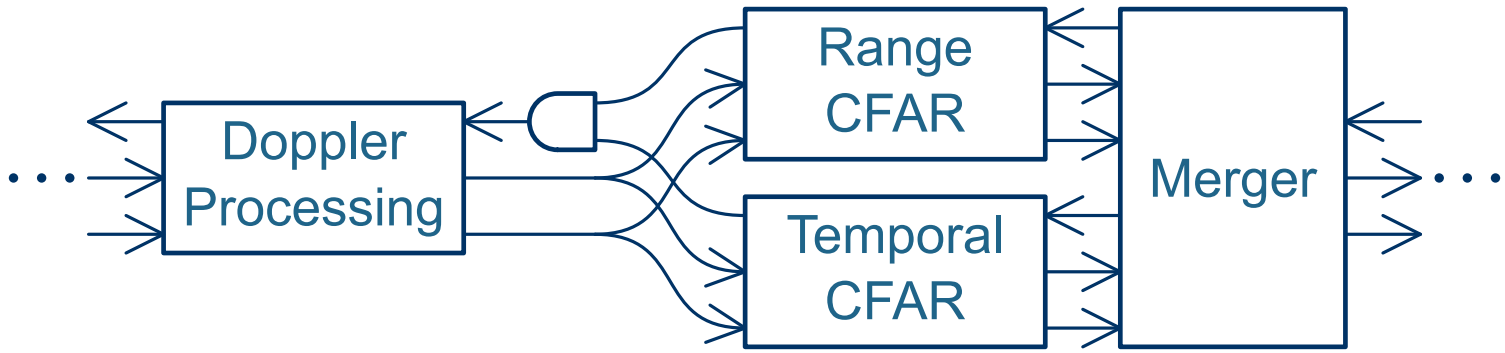

- Gate the “Valid” with the “Ready”
- The “Merger” can take various forms:

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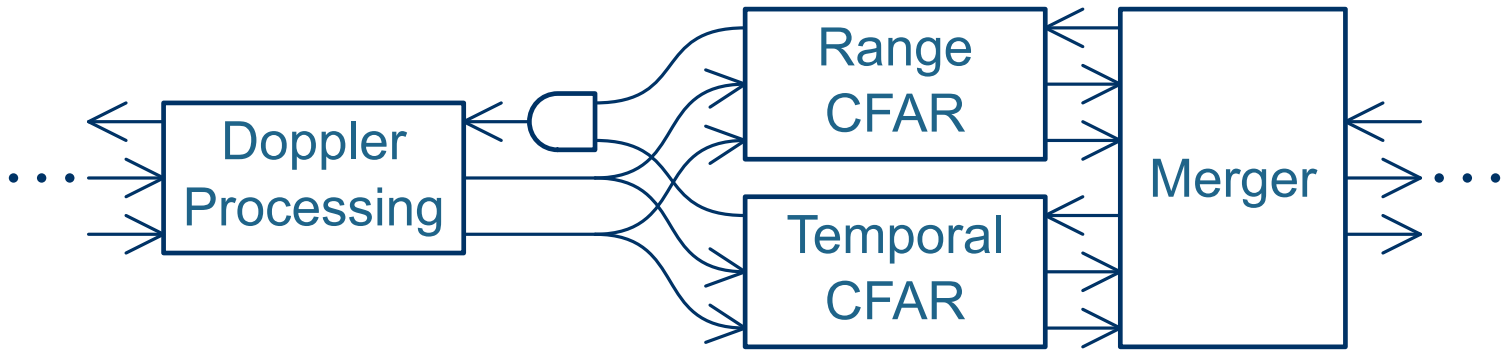

- Gate the “Valid” with the “Ready” (if either sink is not ready, both sinks must see a “not valid” input)
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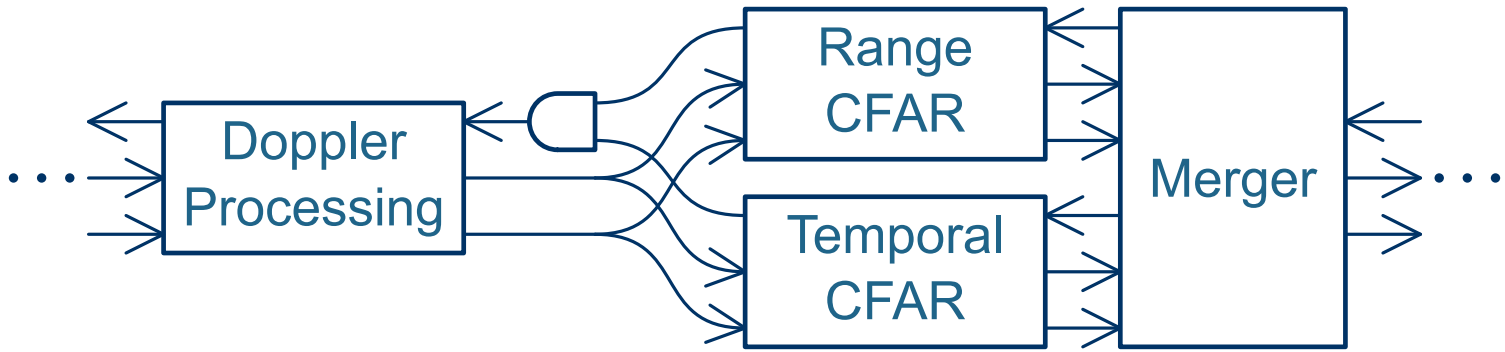

- Gate the “Valid” with the “Ready”
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  - Alternate (sent one logical unit from the one, then the other, then repeat)
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  - etc.

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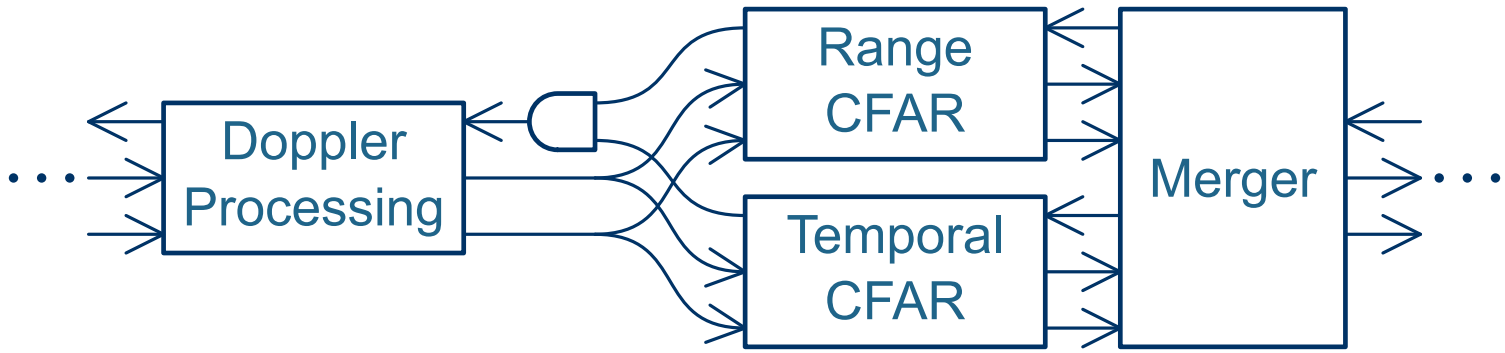

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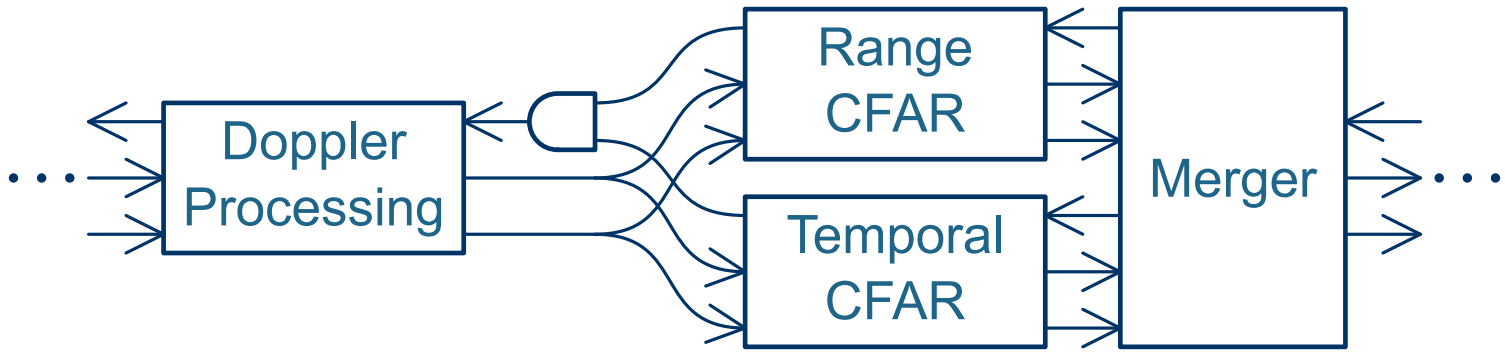

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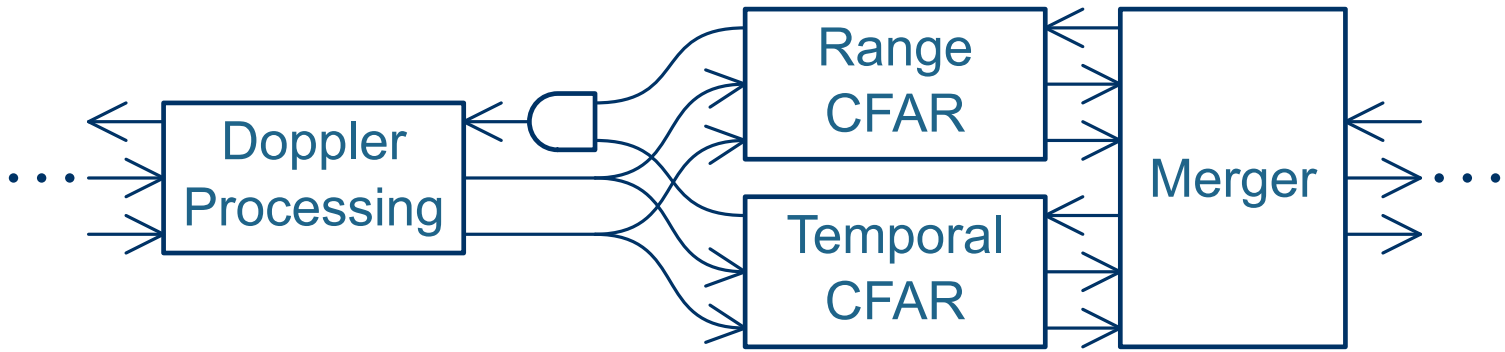

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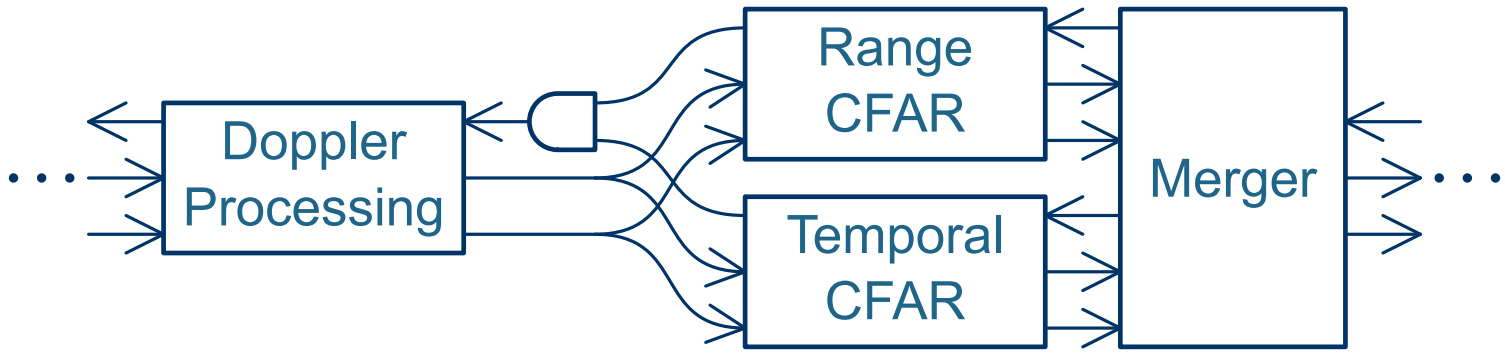

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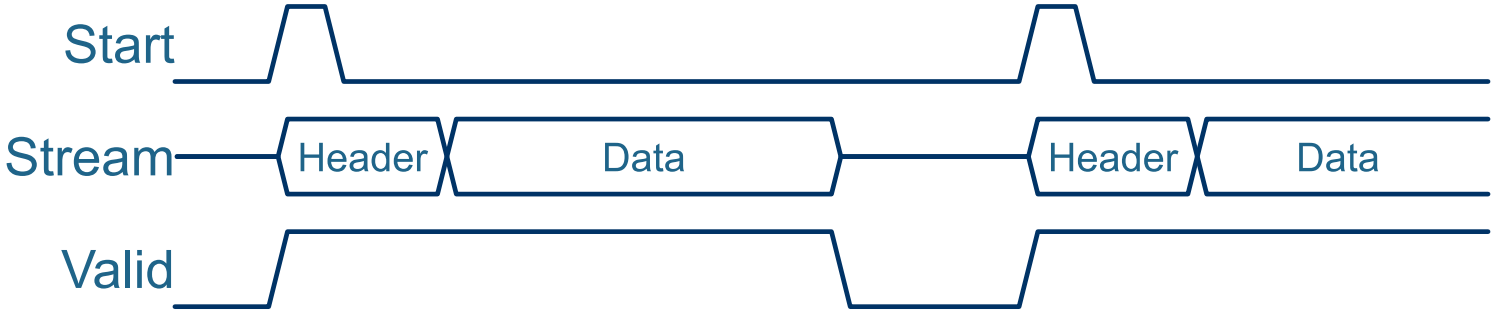
Packet-based Streams



- Add a start-of-packet strobe (valid for one clock-cycle only)
- Natural fit for RADAR: one packet per PRI
- Natural fit for packet-based communication (e.g. Ethernet or UDP – makes it easy to implement Ethernet-based FPGA-in-the-loop testing)
- The header can contain all sorts of metadata...

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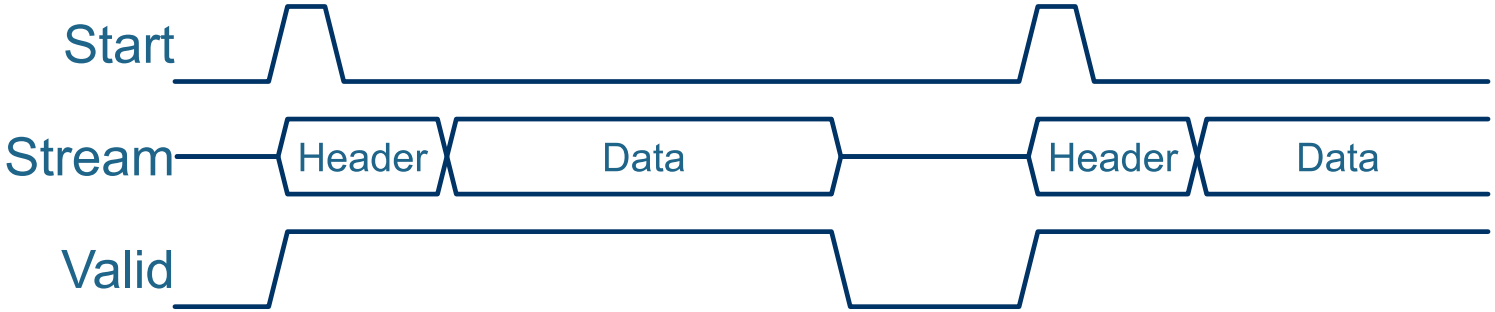

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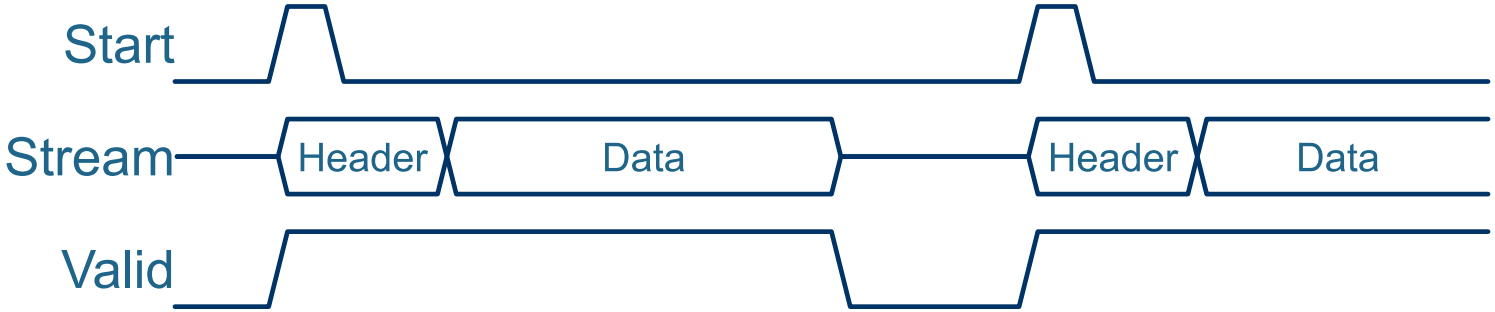

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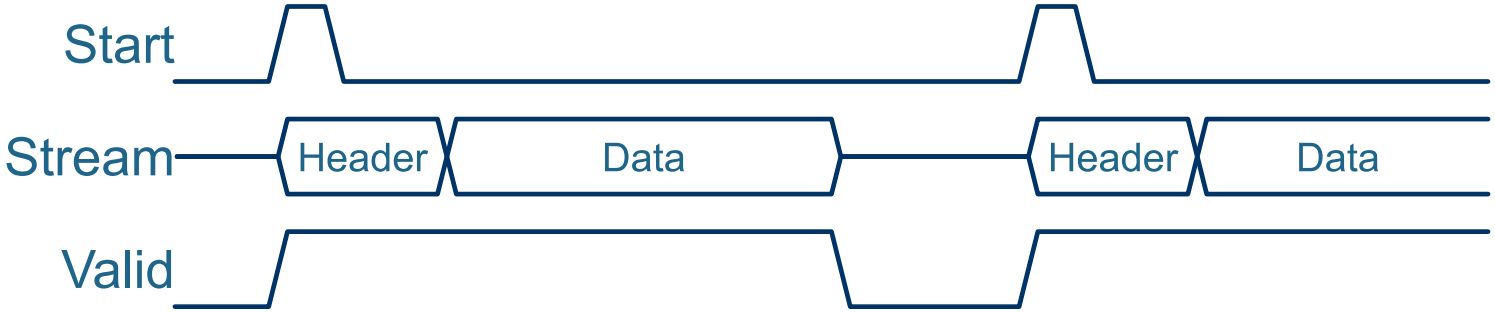

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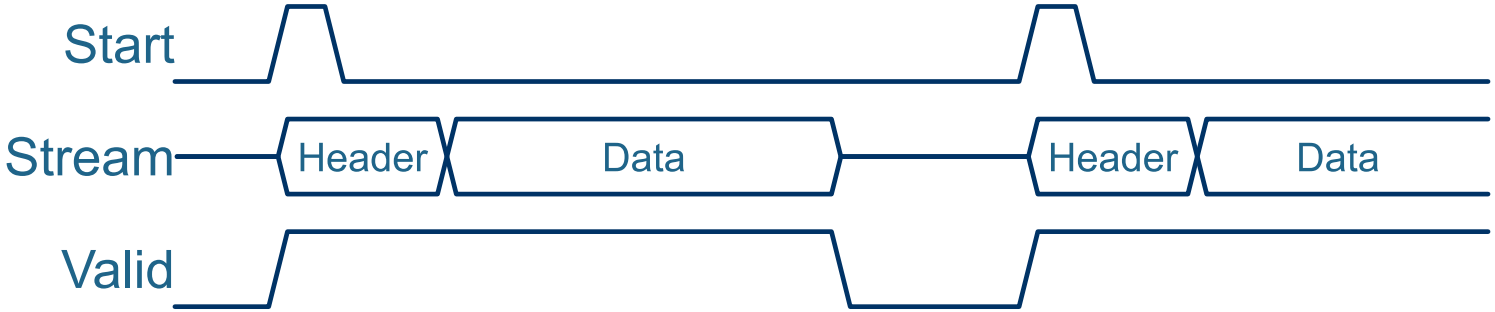

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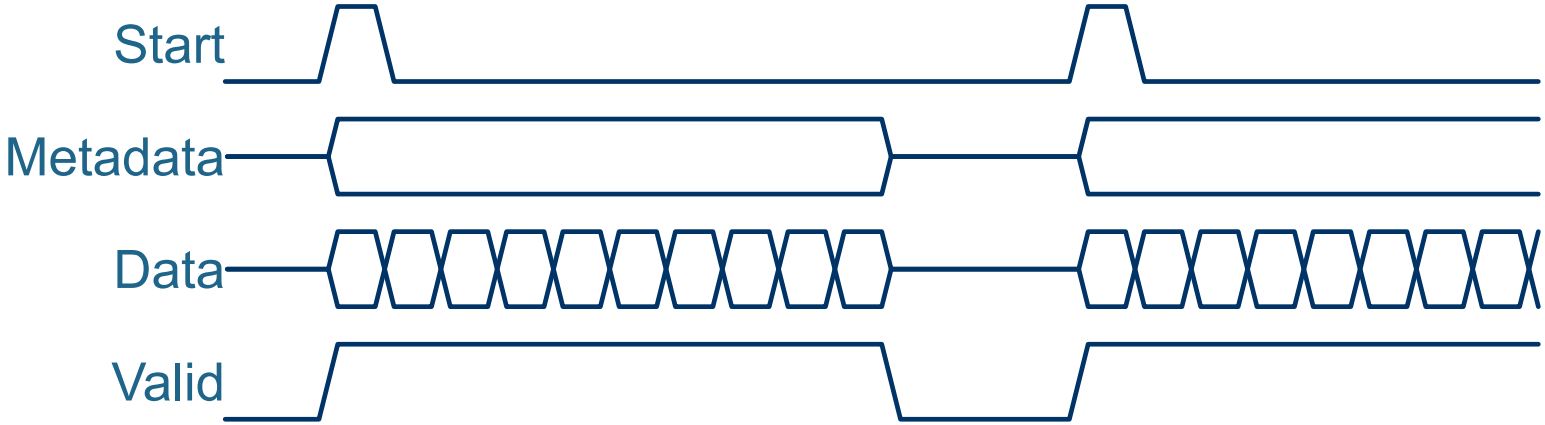

- Metadata can also be implemented as a side-channel
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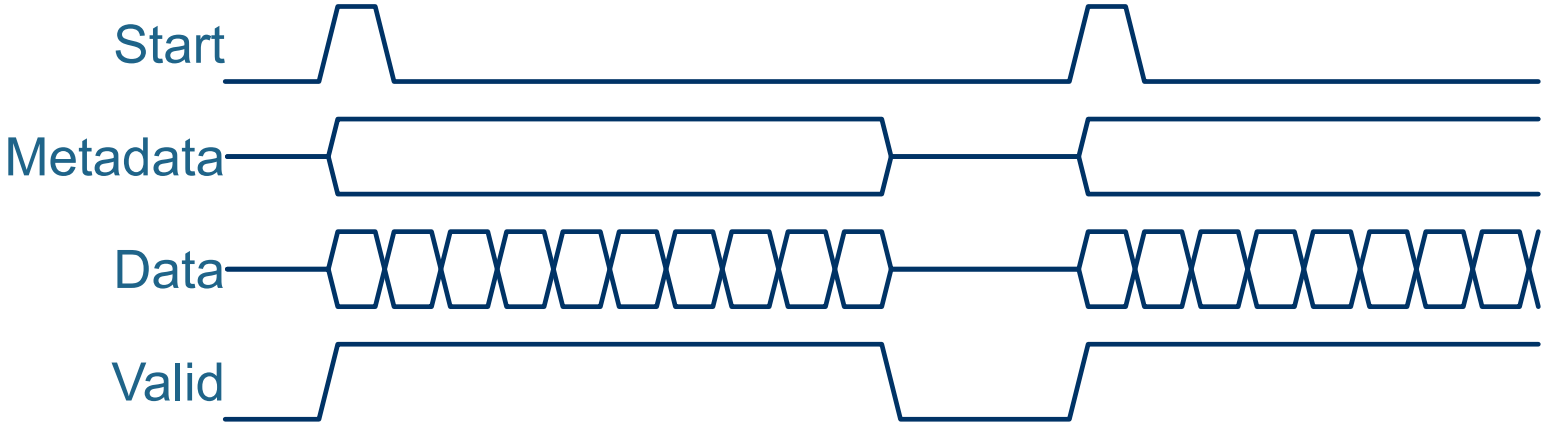

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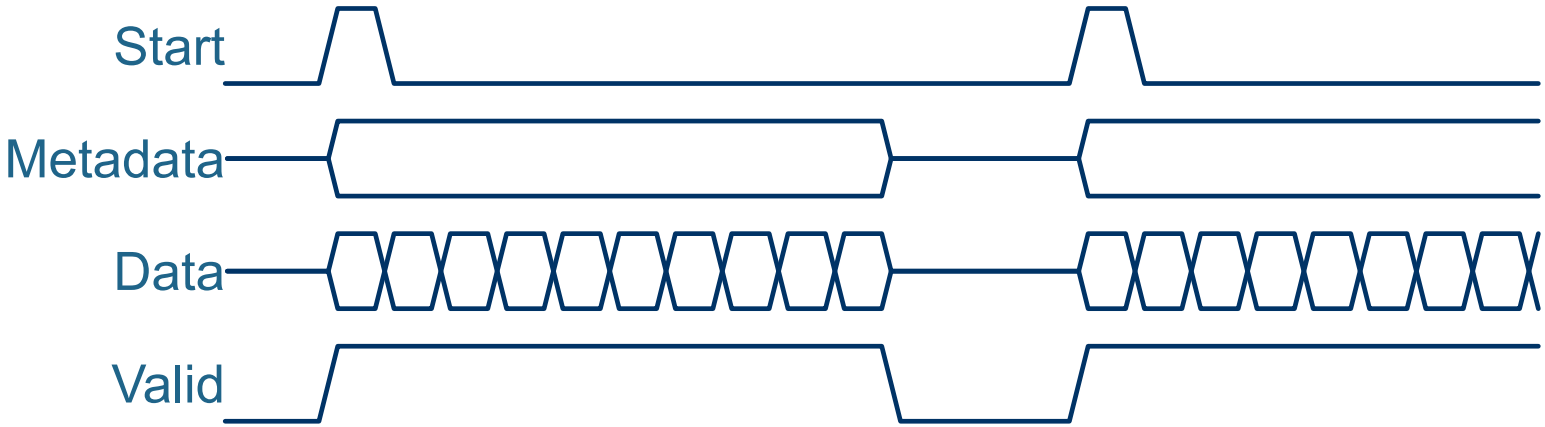

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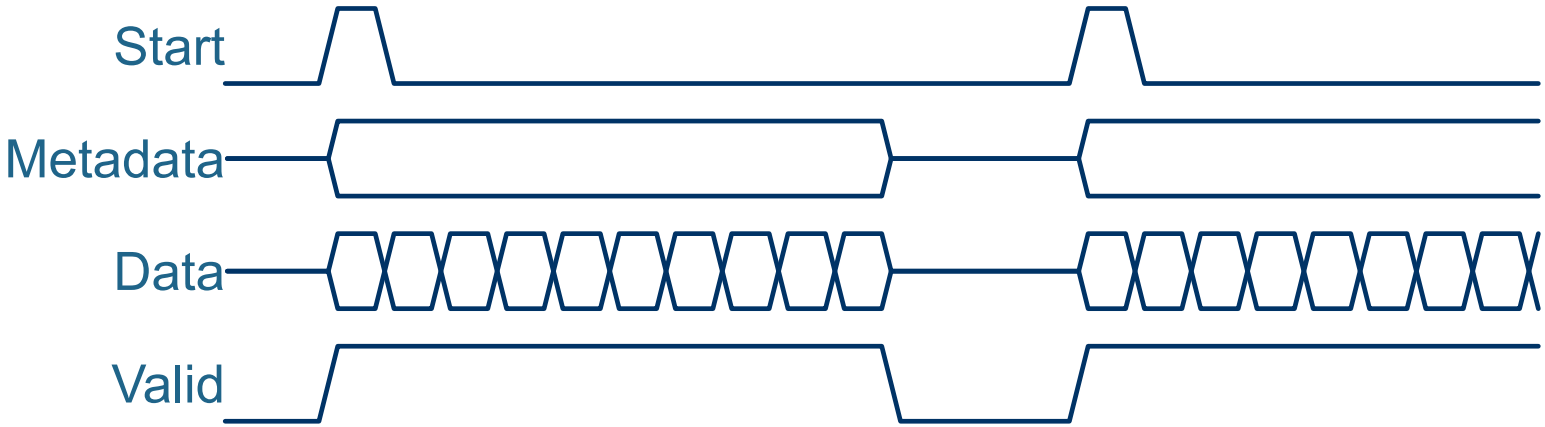

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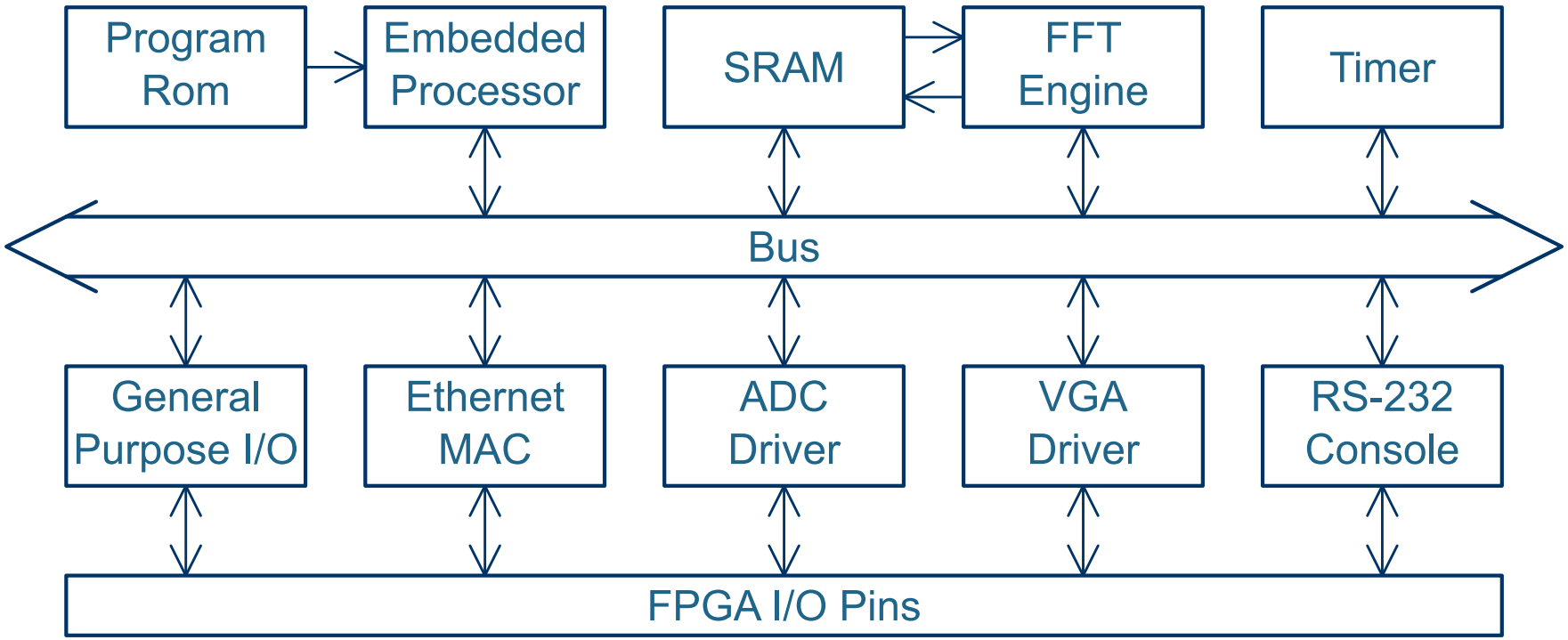

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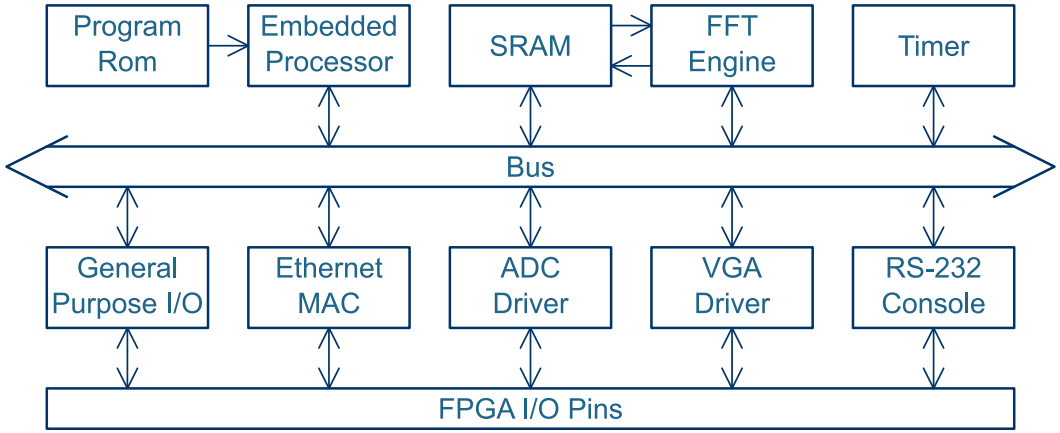

- Every node on the bus has an address range allocated
- Generally used for writing control registers, reading system status and accessing memory
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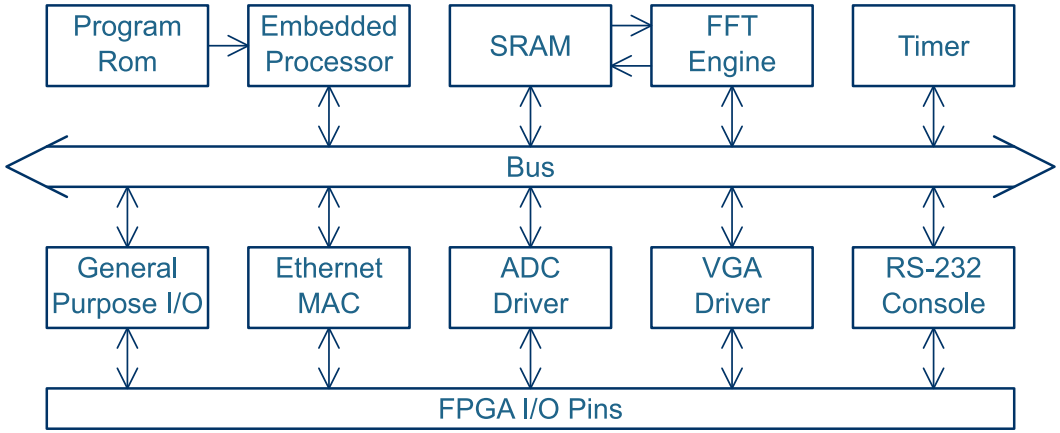

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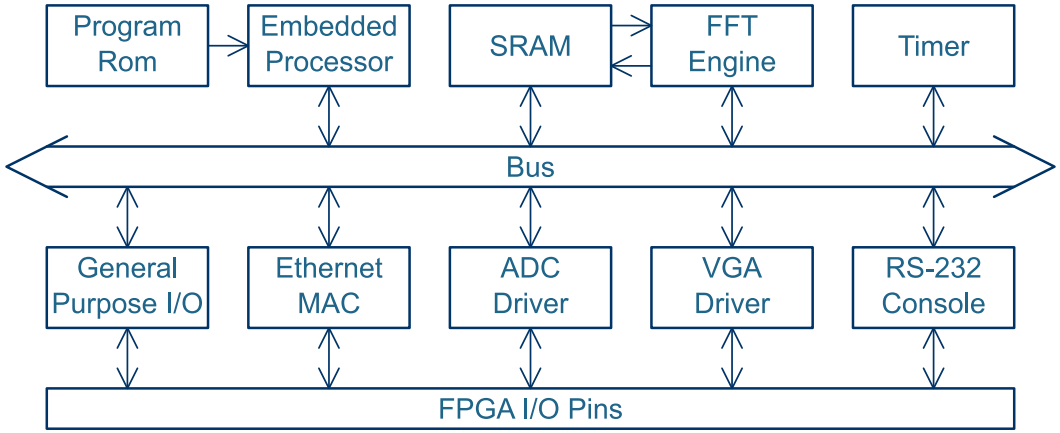

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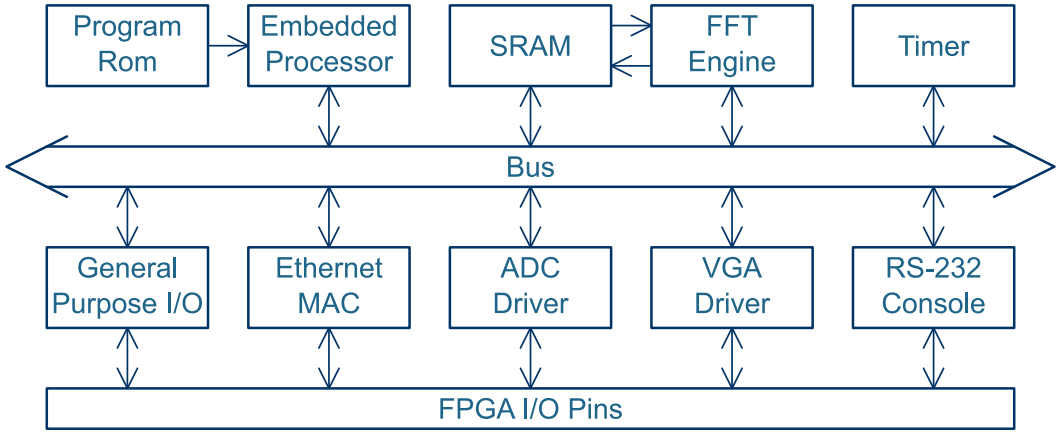

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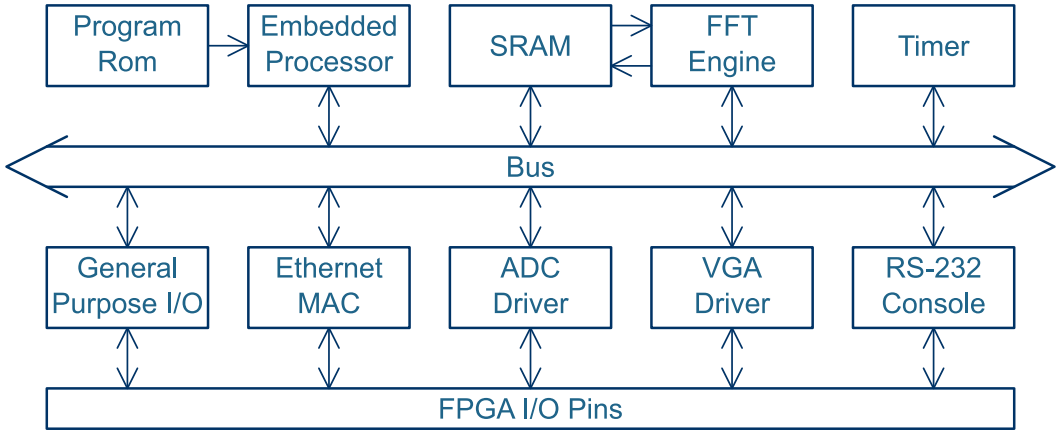

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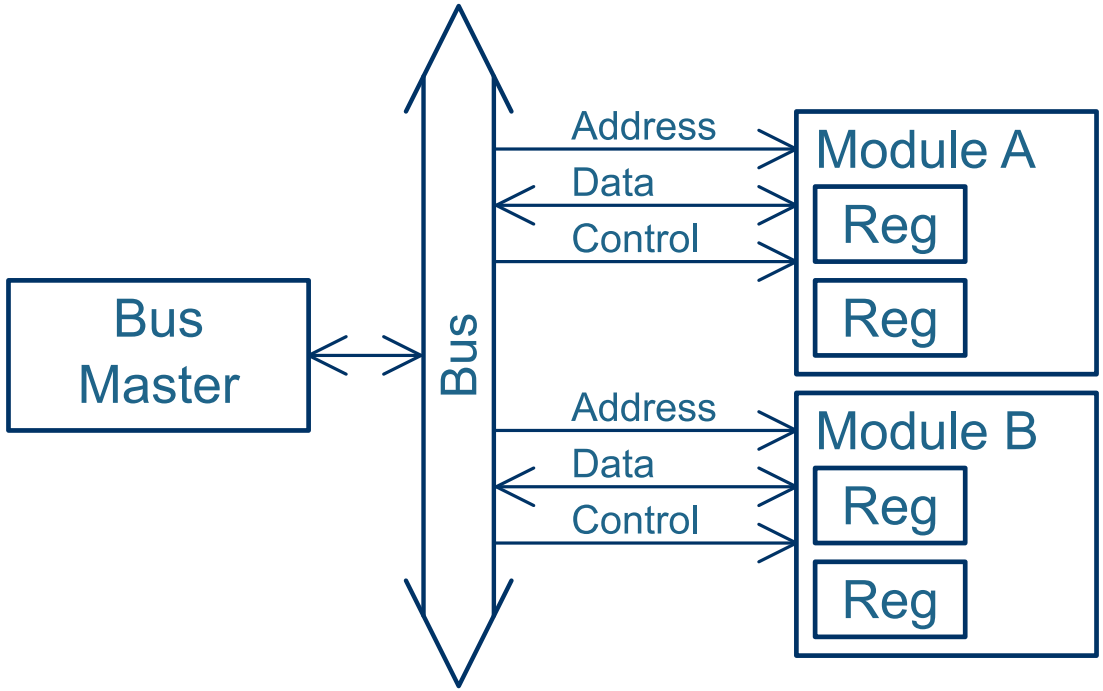
Memory-mapped Architectures



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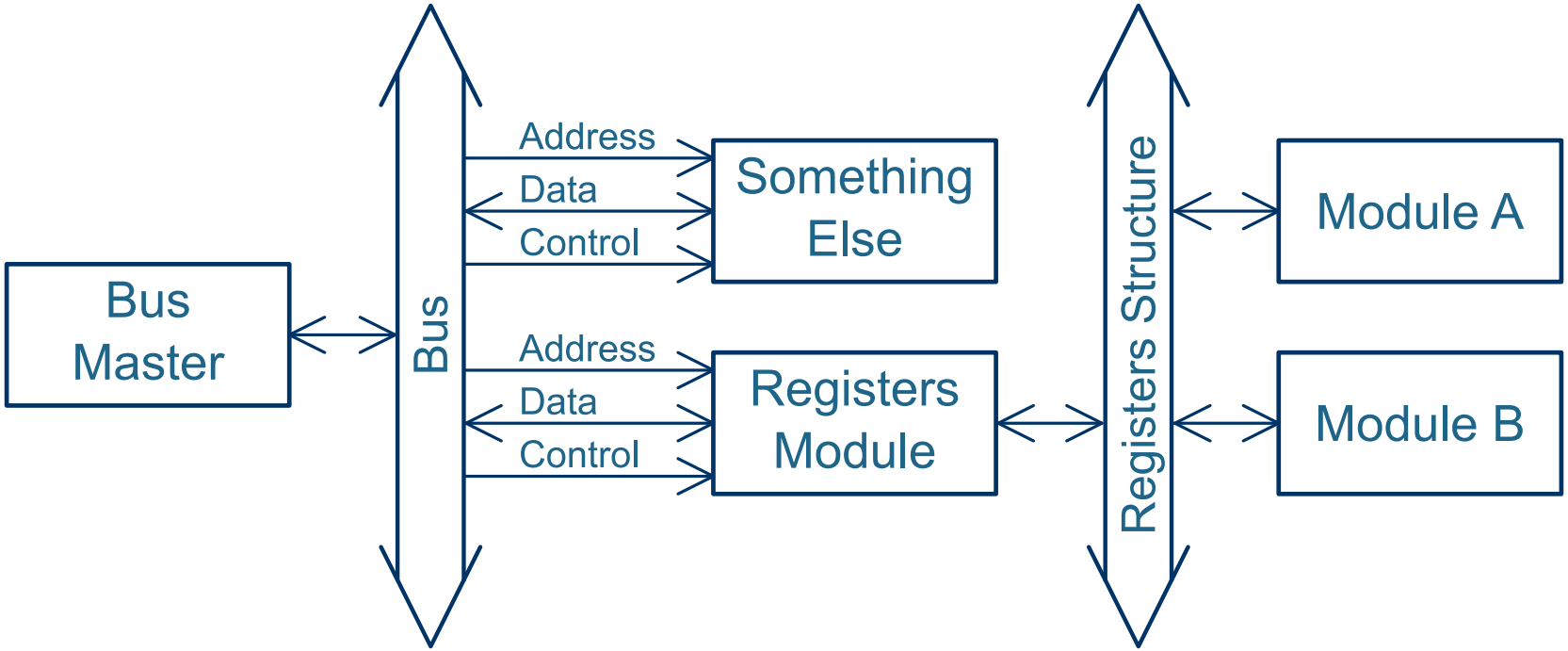
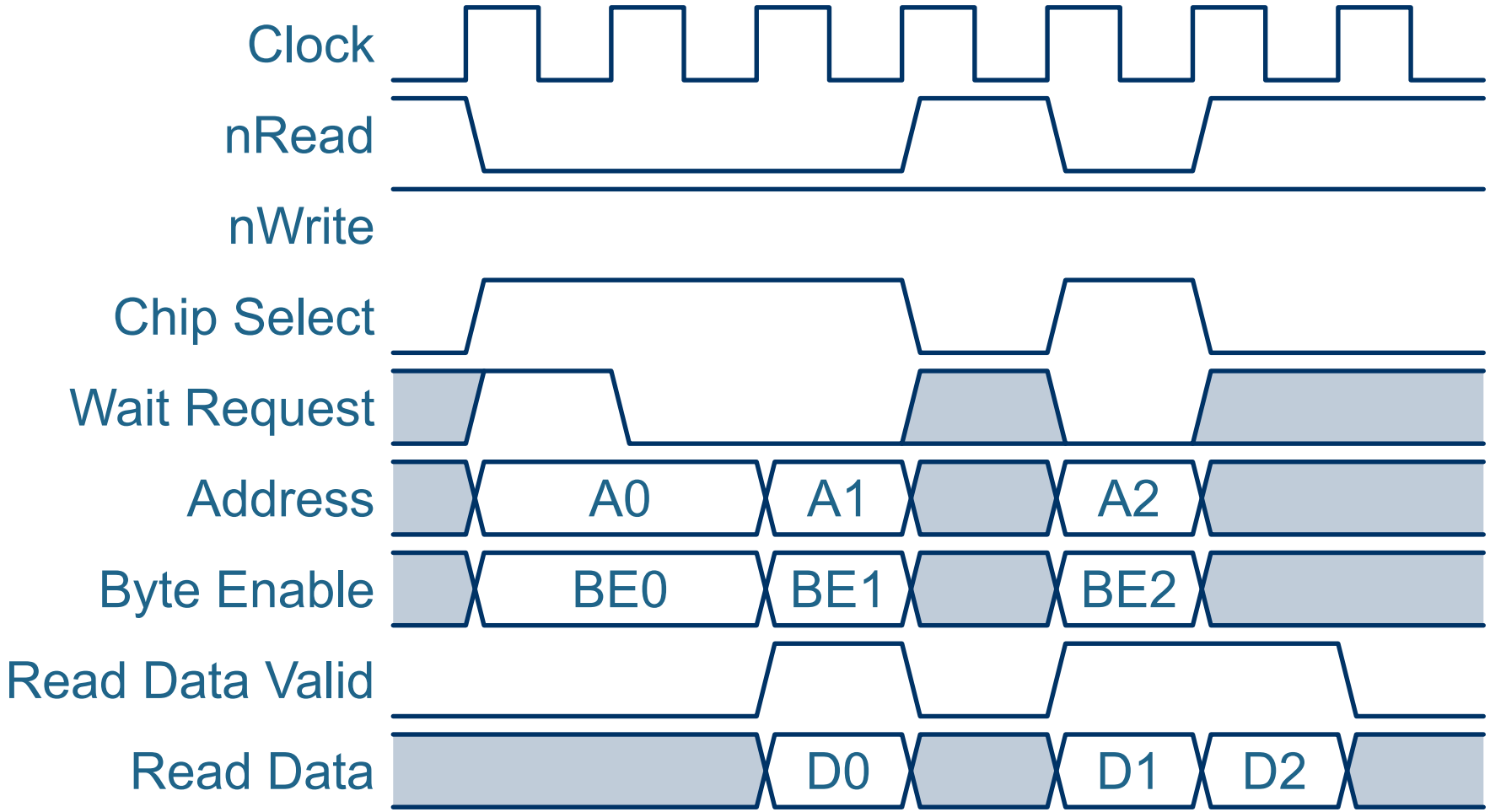
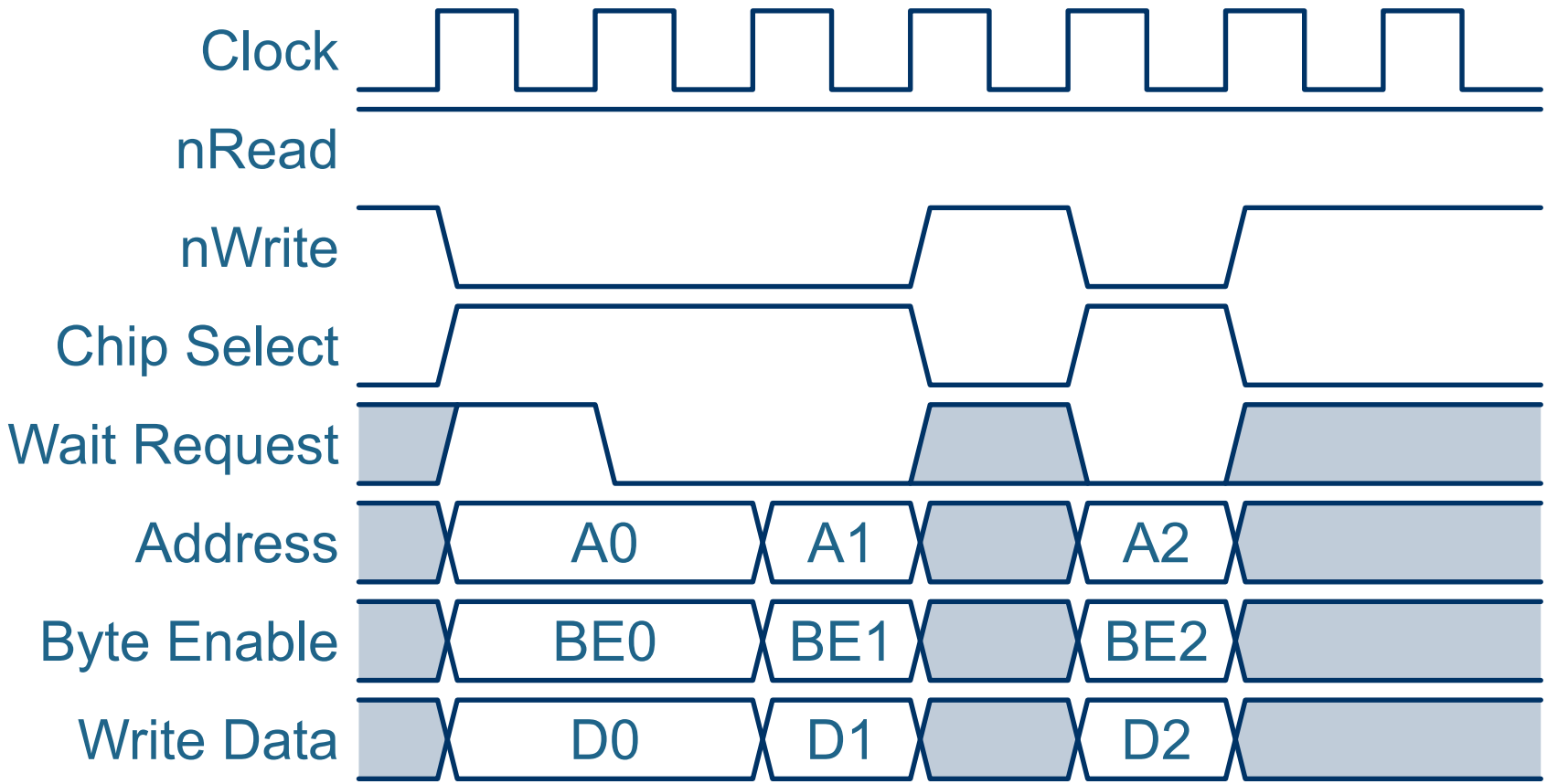


Interface Timing Diagrams



Interface Timing Diagrams



Structures

- SystemVerilog only
- Define these once in a separate file, typically as part of a package

```
package Structures;
  typedef struct{
    logic [ 1:0]Buttons;
    logic [ 9:0]Switches;
    logic [31:0]StatusBits;
  } RD_REGISTERS;

  typedef struct{
    logic [ 9:0]LEDs;
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    logic [ 2:0]Bandwidth;
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endpackage
```

Structures


```
import Structures::*;

module Registers(
   input ipClk, ipReset,

   input   [15:0]ipAddress,
   output  [31:0]opRdData,
   input   [31:0]ipWrData,
   input         ipWrEn,

   input   RD_REGISTERS ipRdRegisters,
   output  WR_REGISTERS opWrRegisters
);
...
```

Structures


```
// In the top-level module...

RD_REGISTERS RdRegisters;
WR_REGISTERS WrRegisters;

Registers Registers_Inst(
  Clk, Reset,
  Address, RdData, WrData, WrEn,
  RdRegisters, WrRegisters
);

NCO NCO_Inst(
  Clk, Reset,
  WrRegisters.NCO_Frequency,
  RdRegisters.StatusBits[15]
);
```

Structures

- You can map a structure to an input port and then use only what you need within the submodule
- You can not map the same structure to an output port of more than one module – you need to map the structure members individually
- Luckily, most registers are control registers, and therefore input ports of the target modules

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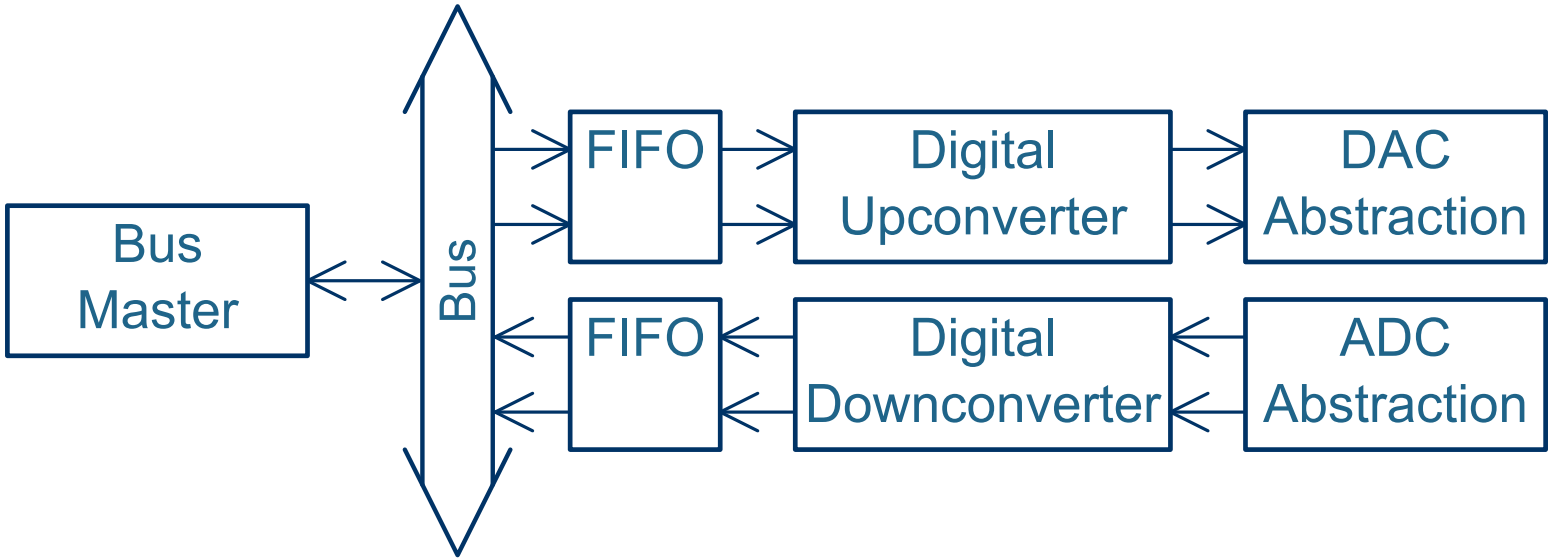
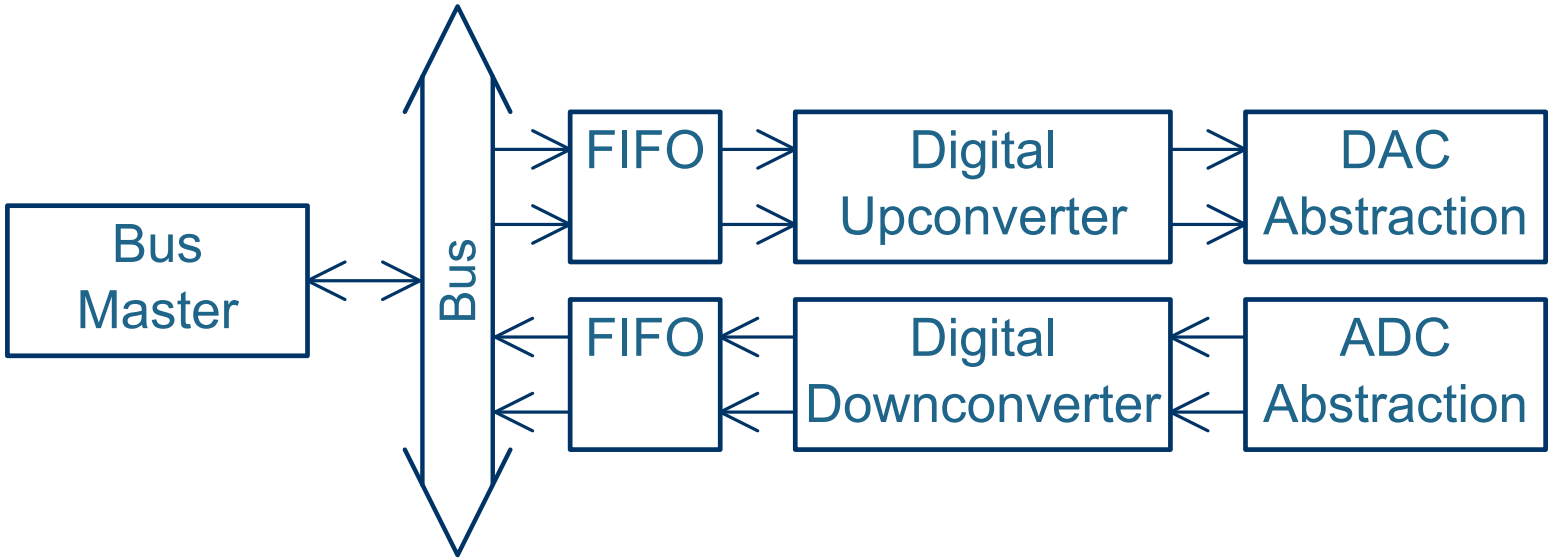
Memory-mapped Streams



- It is often convenient to allocate a bus address to a stream
- A write to that address injects one unit into the stream
- A read from that address reads one unit from the stream
- Most often unidirectional and FIFO-buffered with feed-back registers

Memory-mapped Streams



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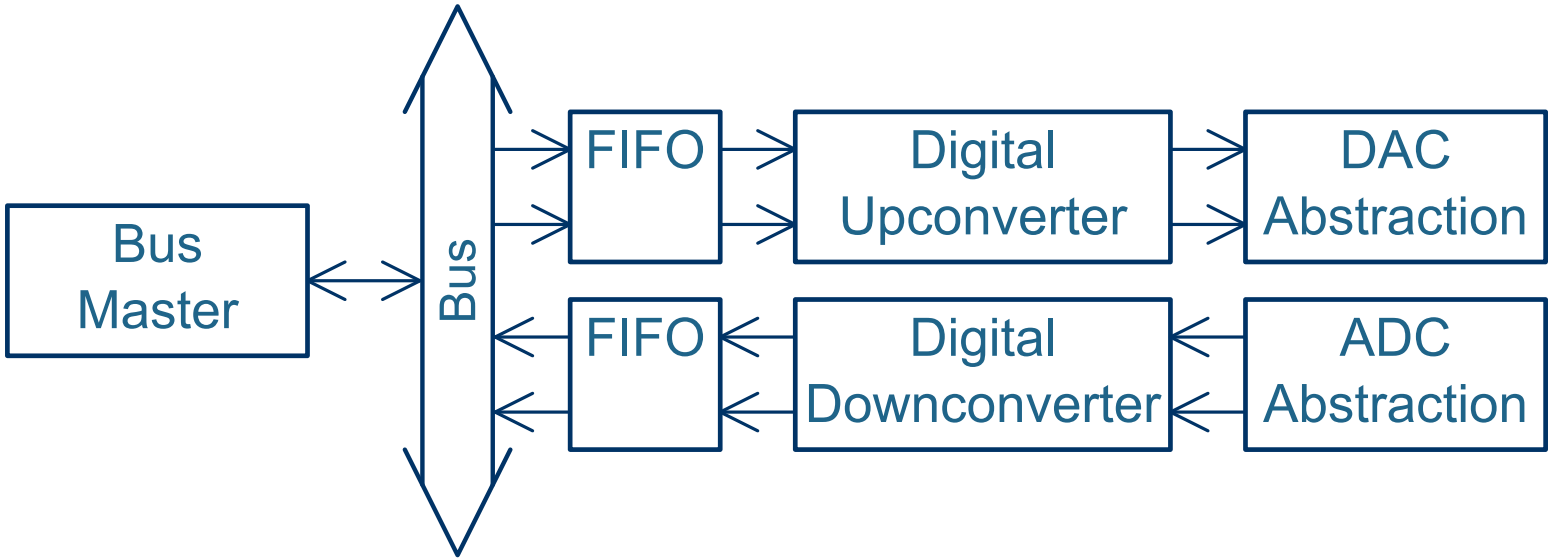

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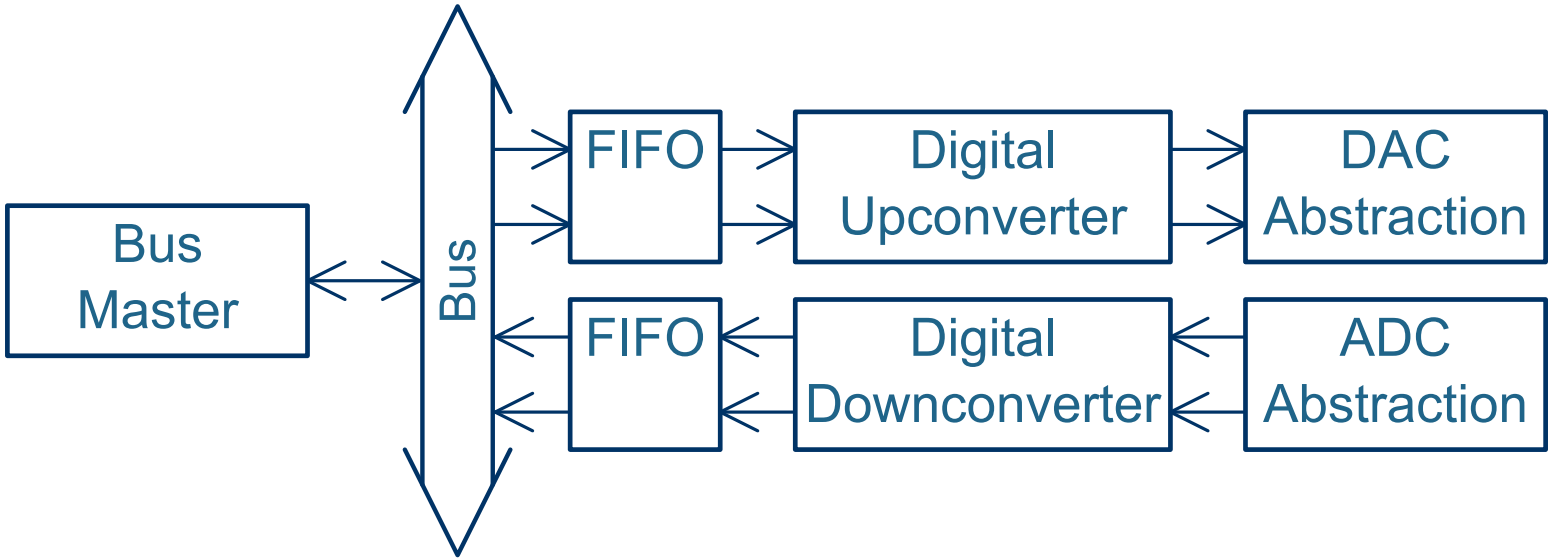

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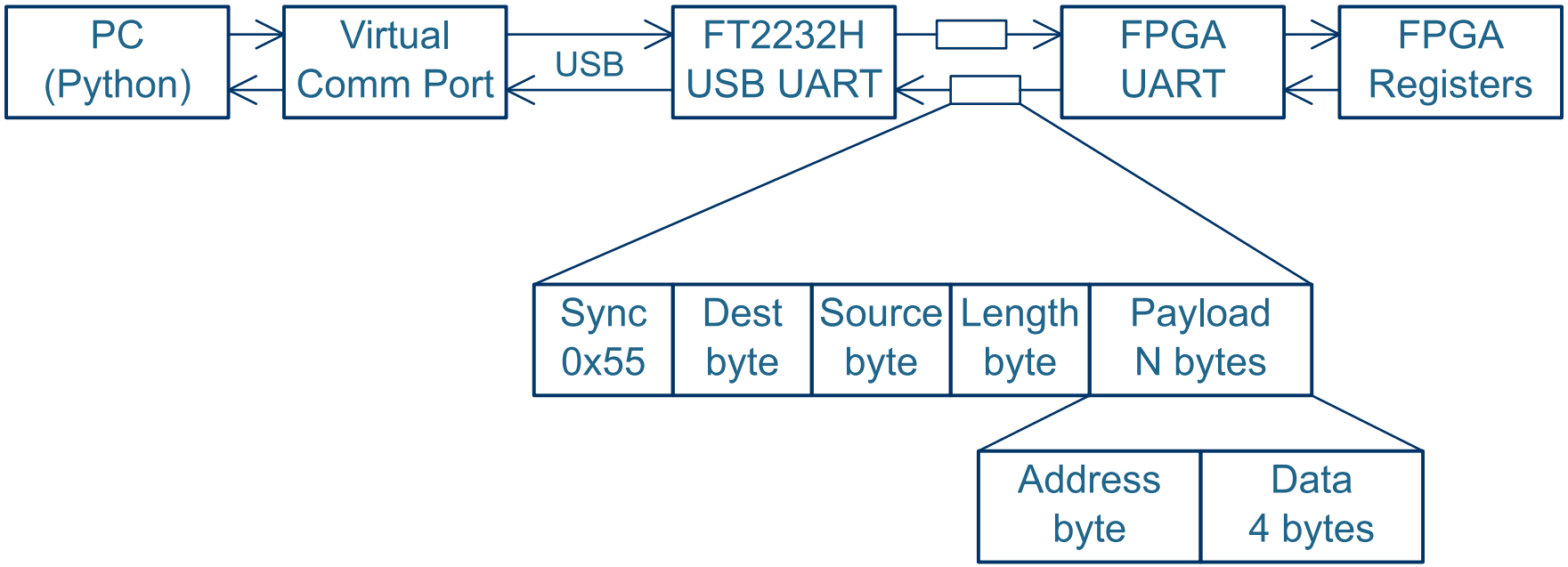
UART Controlled Bus

Practical `05 - Registers` makes use of a UART interface to control memory-mapped FPGA registers.



Outline

Pipelines

Streaming Processors

Memory-Mapped Bus

Pulse-width Modulation

High Resolution PWM

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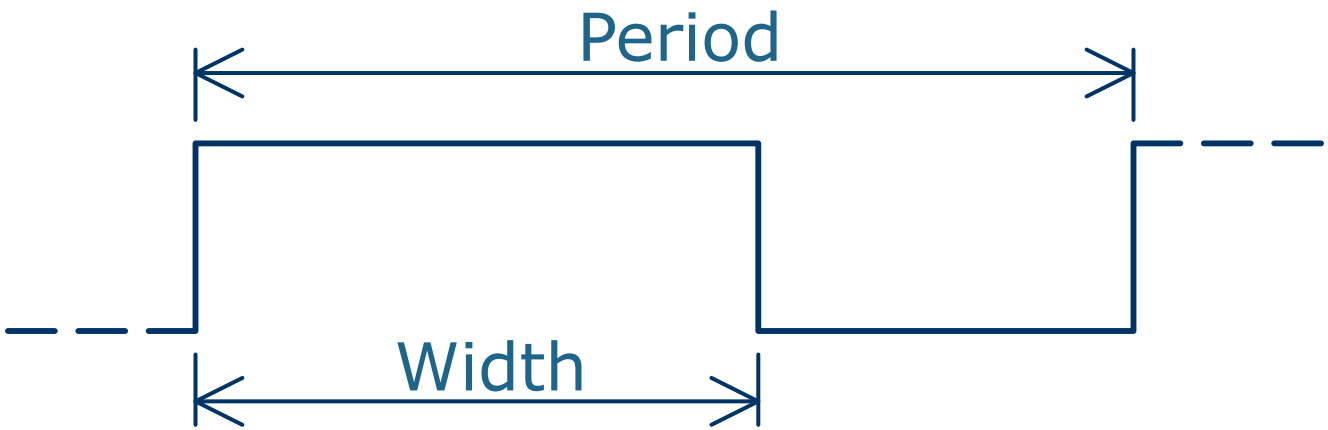
Pulse-width Modulation



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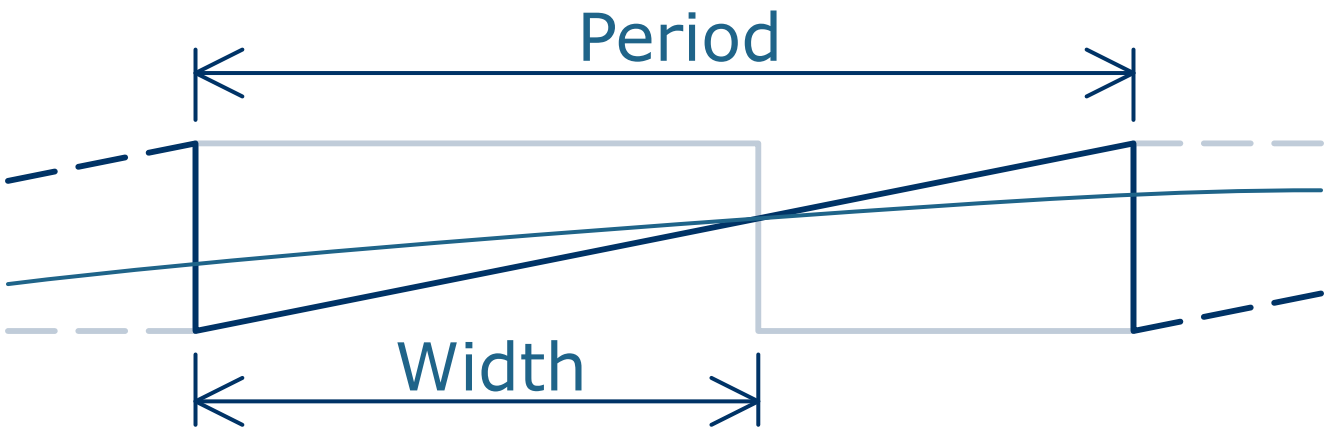

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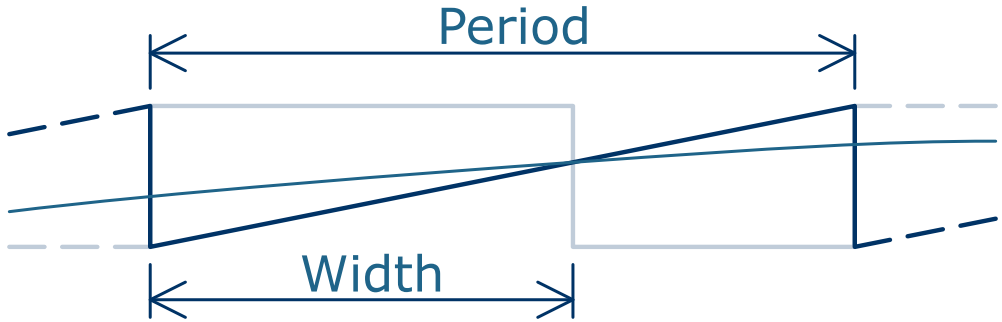

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- The PWM module requires an unsigned input from 0 to $(2^N - 1)$ – also known as offset-binary
- To convert from one to the other, invert the most-significant bit

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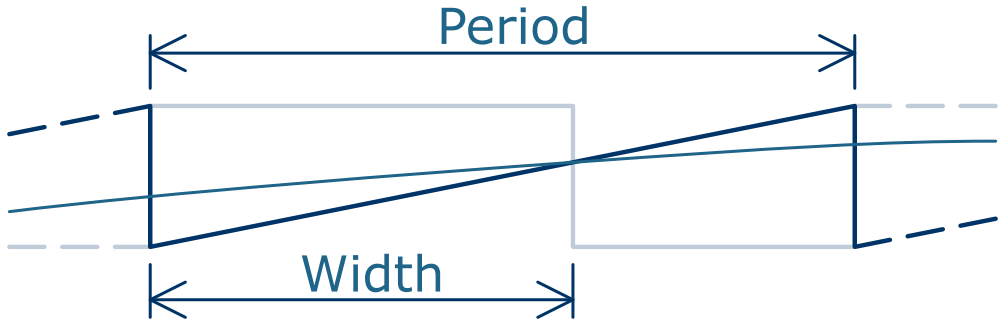

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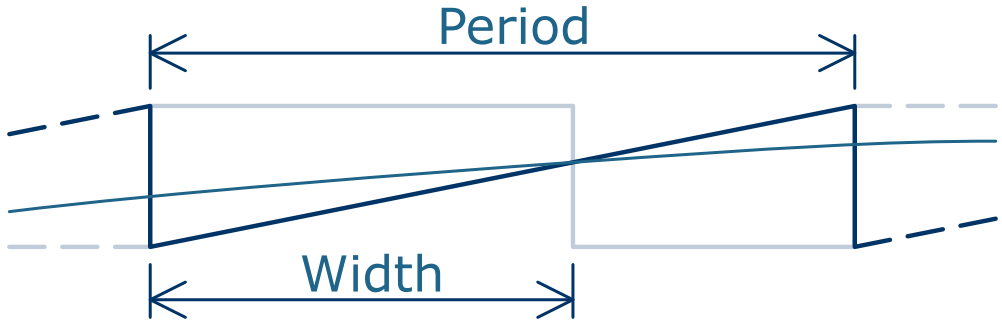

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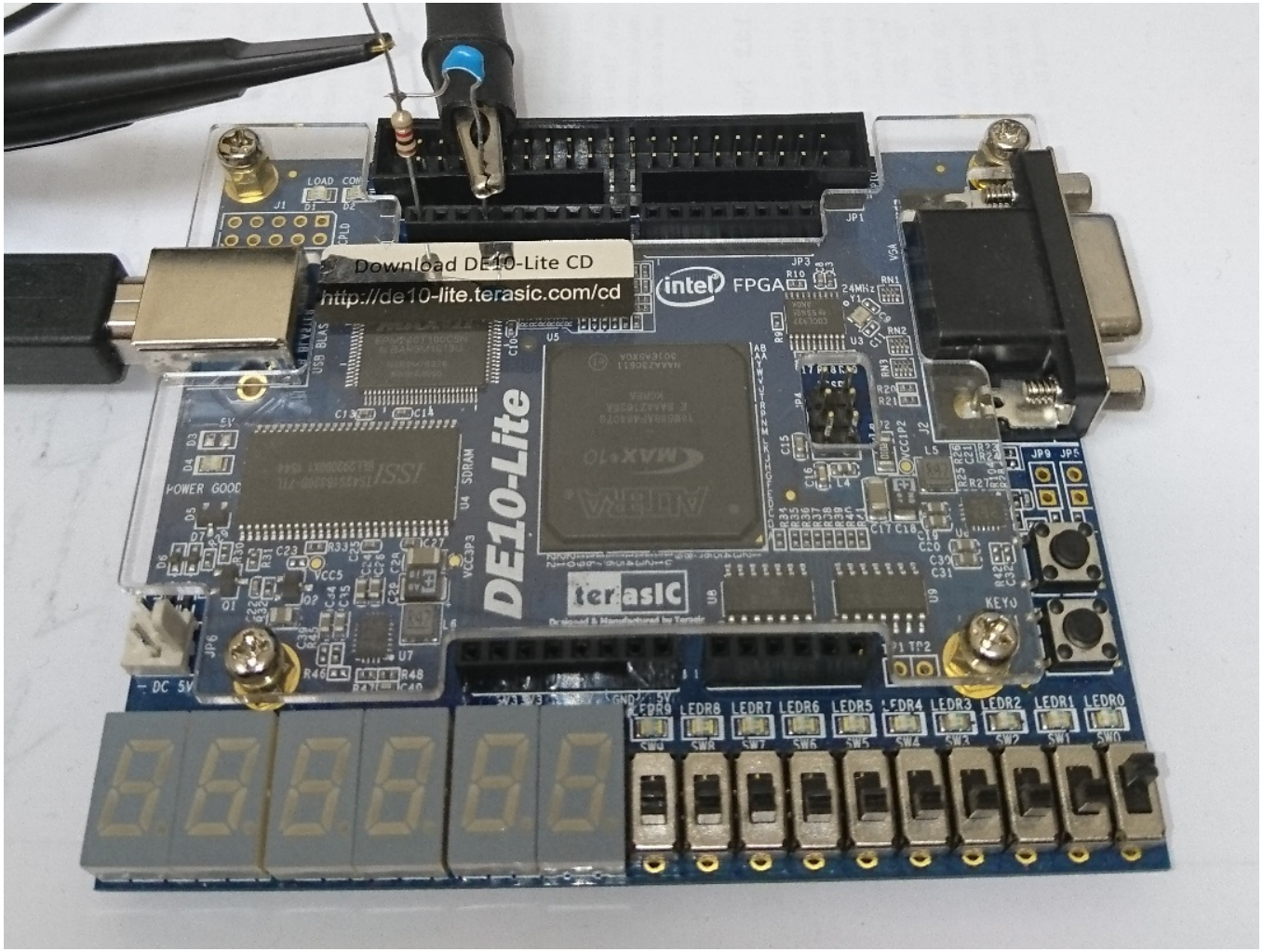

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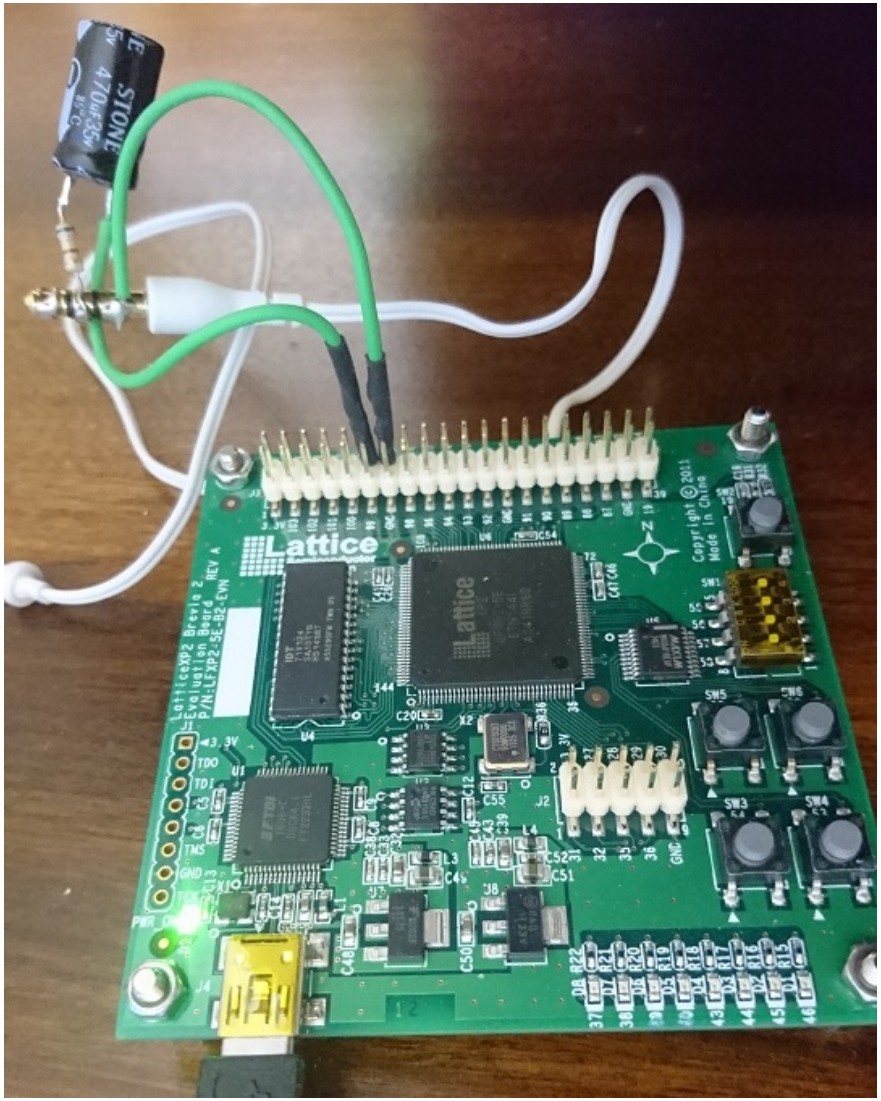
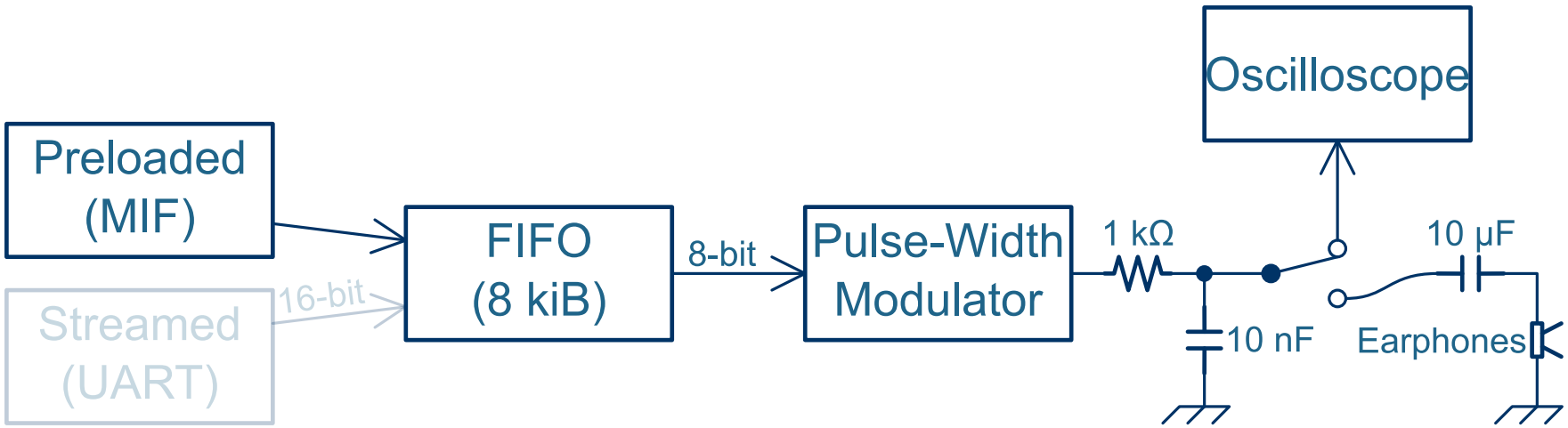


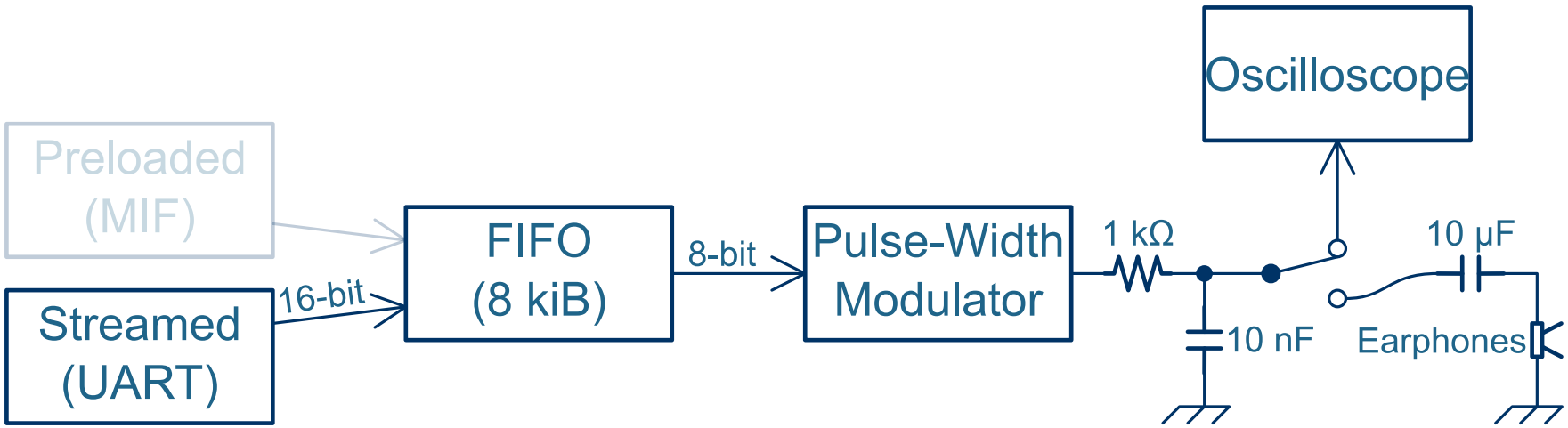
Simple Injection

Before continuing,
get the PWM and simple injection modules working...



UART Injection

Keep in mind that the same FIFO-based injection module must interface with the 16-bit UART or SRAM based injection...



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High Resolution PWM

- Assume that your signal is audio (20 kHz bandwidth)
- You want the PWM frequency at least 10 times the signal bandwidth $\Rightarrow$ 200 kHz
- Say you want 16-bit output resolution...
- You have to run the saw-tooth counter at 200 kHz $\times$ $2^{16} = 13.1072$ GHz
- That is a FAST clock!
- The solution...

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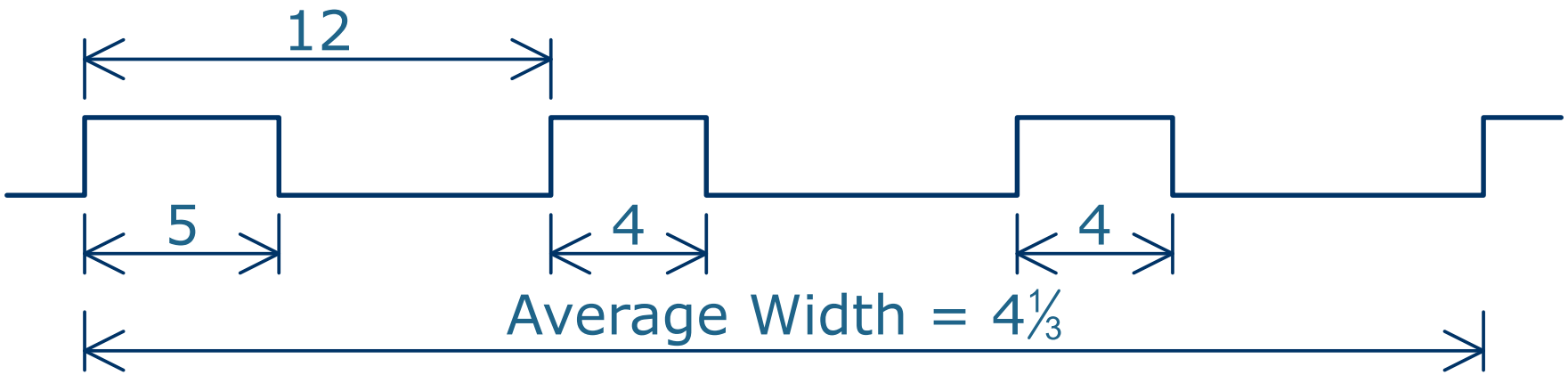
Noise Shaping



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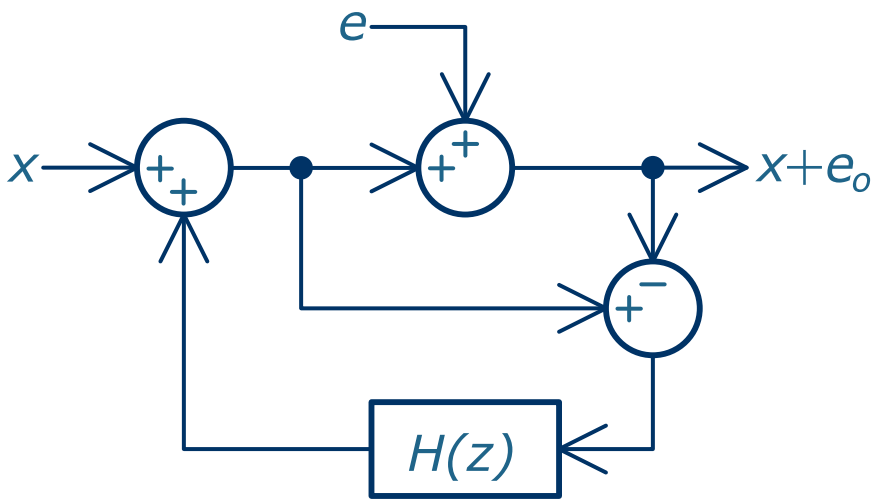

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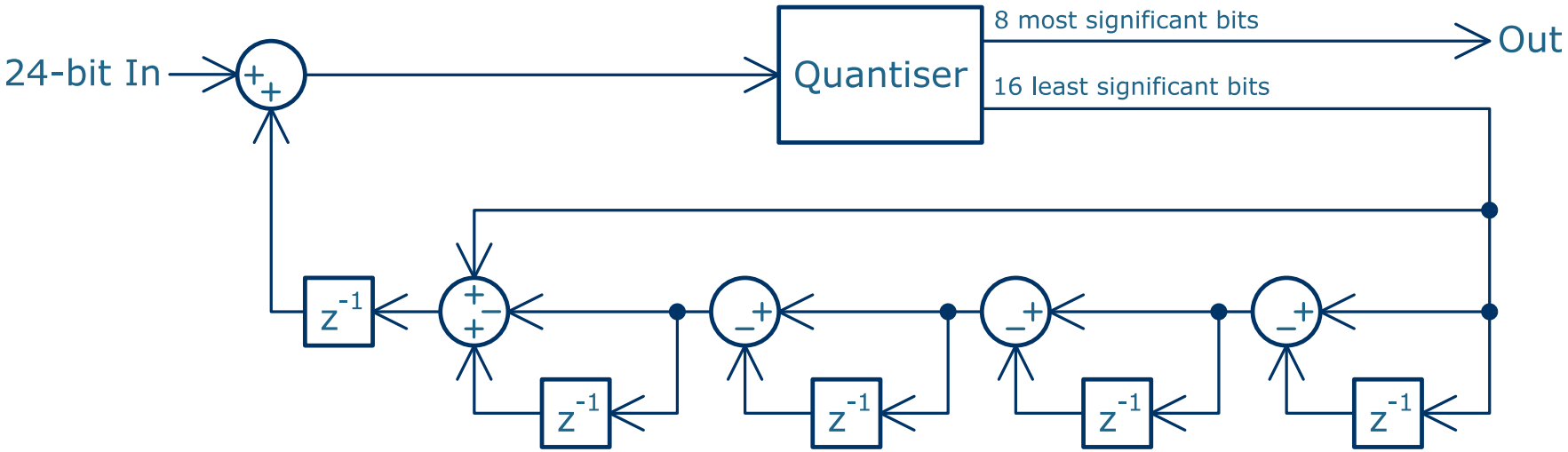

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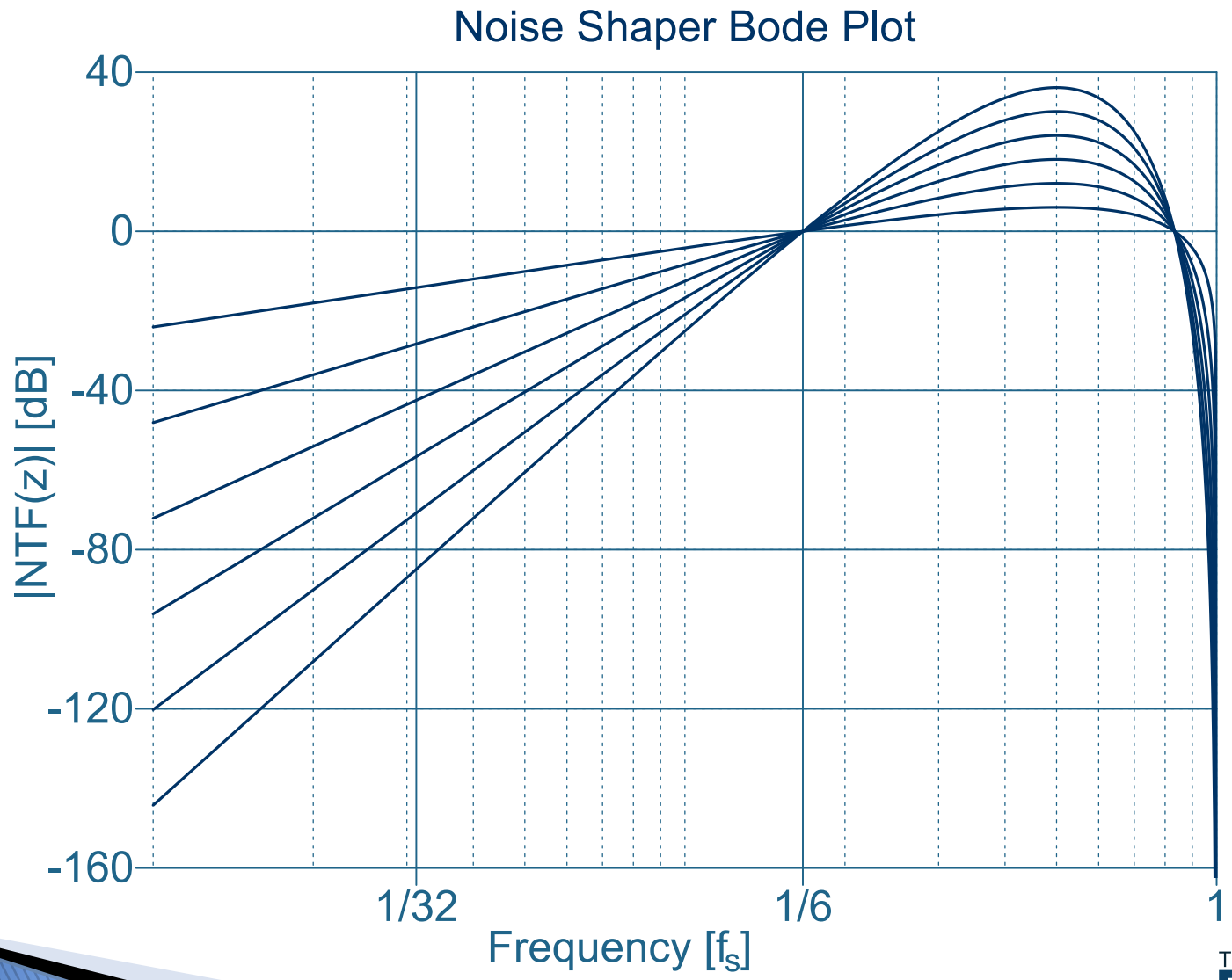

Select References

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Merrill L Skolnik
Introduction to RADAR Systems
ISBN 978-0-07-288138-7

Mark A. Richards and James A. Scheer
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Jean P. Nicolle
FPGA 4 Fun
http://www.fpga4fun.com/

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Presented by John-Philip Taylor

Convened by Dr Stephen Paine

Day 3 – 29 April 2022