FPGA Development for Radar, Radio-Astronomy and Communications

THE RADAR MASTERS COURSE

Dept. Electrical Engineering, University of Cape Town
Private Bag, Rondebosch, 7701, South Africa

http://www.rrsg.uct.ac.za

Presented by John-Philip Taylor

Convened by Dr Stephen Paine

Day 4 – 2 May 2022

Outline

Advanced Clocking

Clock Domains

Mutual Exclusion and Arbitration

Caching Systems

Flow Control

Practical – NCO and DDC

Numerically-controlled Oscillator

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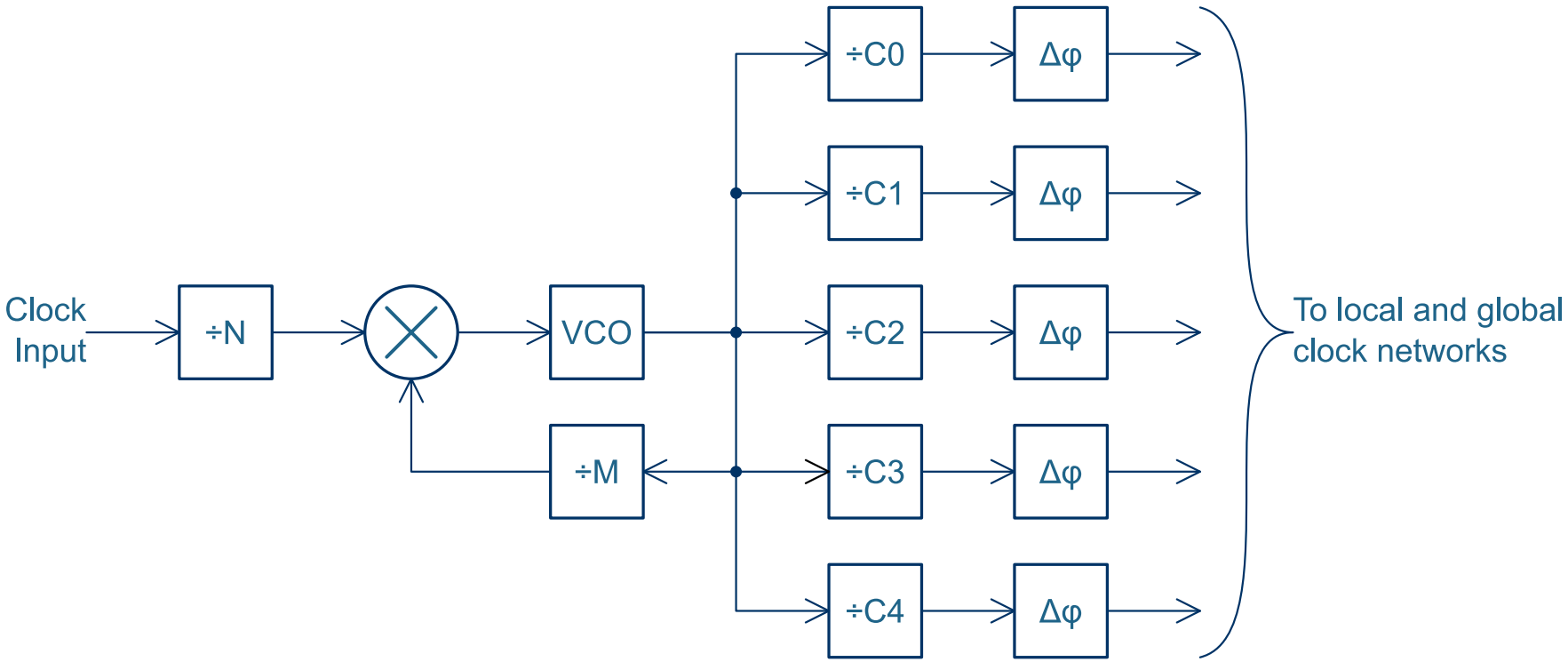
Phase-locked Loop



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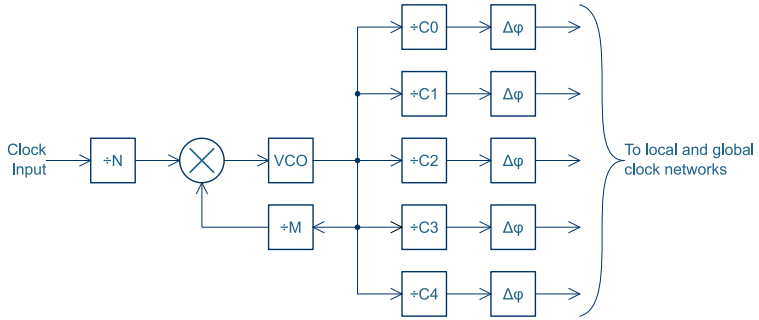

- Useful for generating a range of related clocks
- Output clock rising and falling edges can be set, independently, to a resolution equal to the VCO period, which is typically about 1 ns ± 500 ps
- All output clocks can be considered to be in the same clock domain
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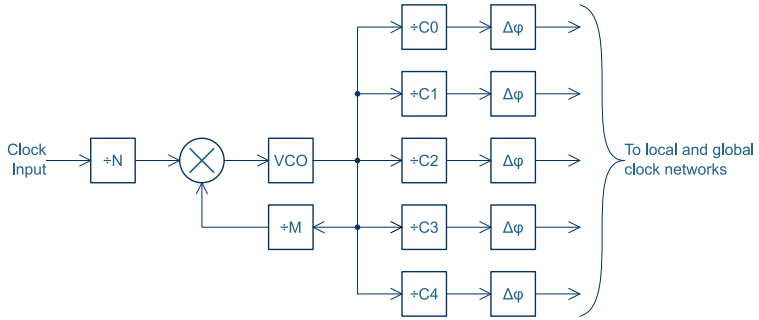

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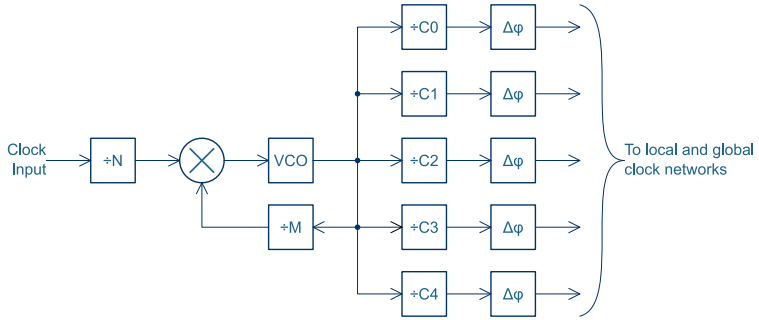

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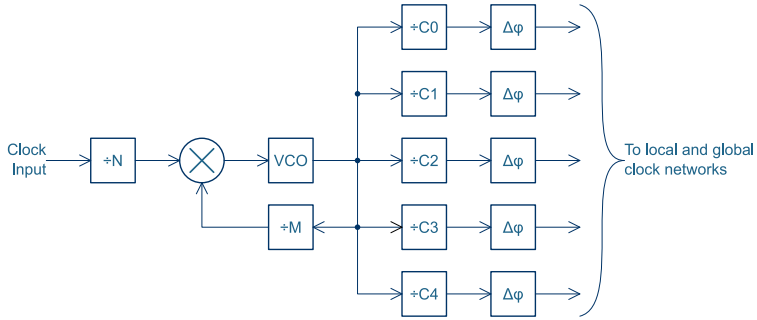

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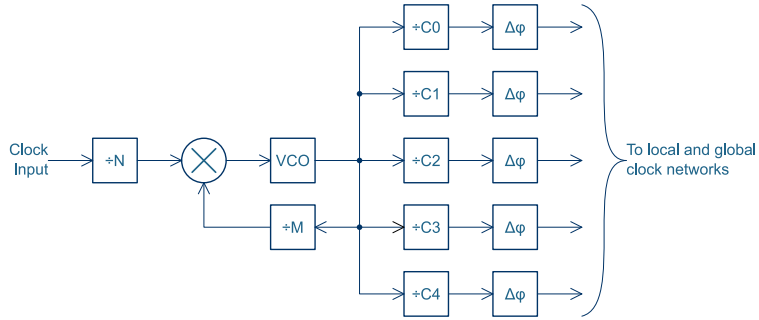

- **Direct**: No compensation, which results in better jitter performance
- **Normal**: The clock at the register is phase-aligned with the input clock pin
- **Source Synchronous**: The PLL ensures that the data delay from pin to register and the apparent clock delay from pin to register is the same
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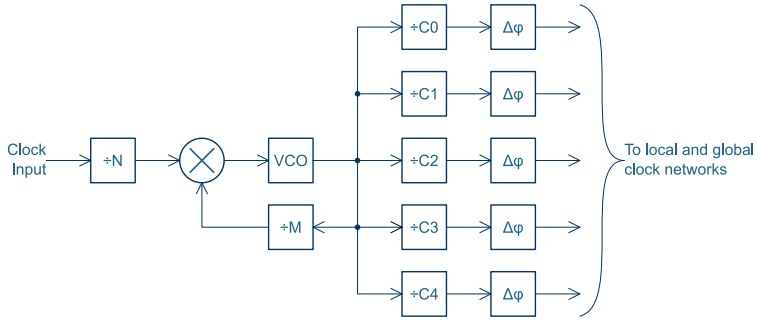

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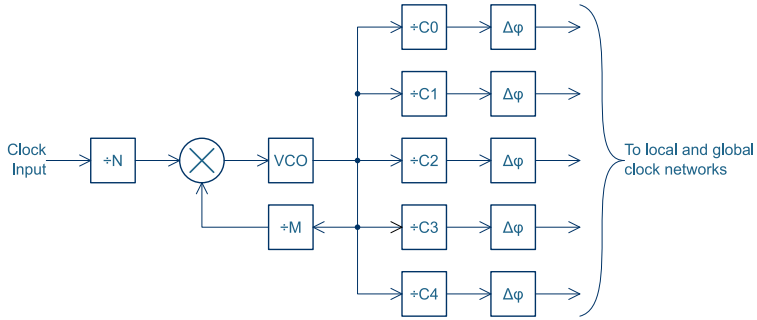

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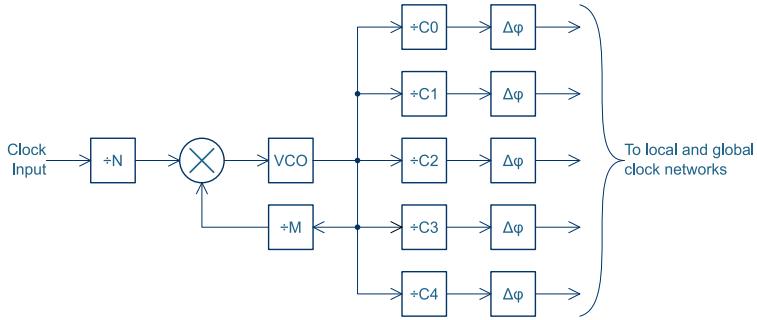

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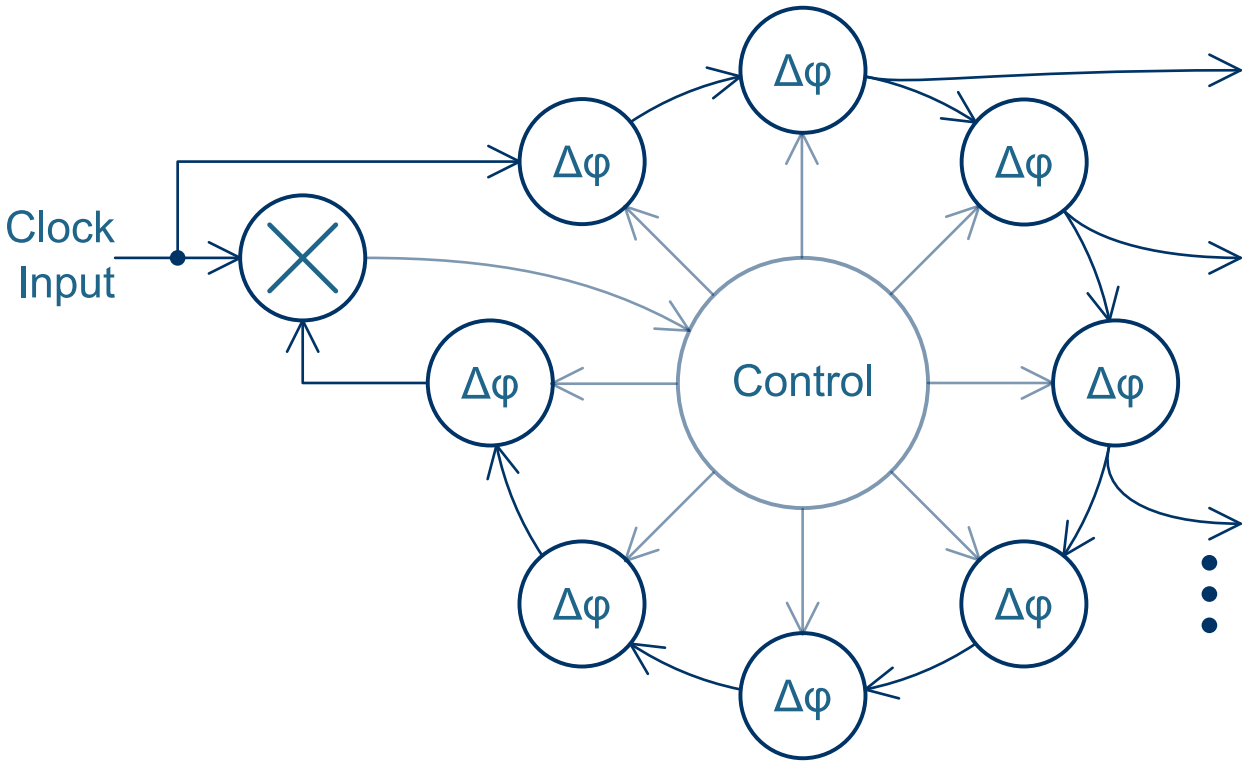

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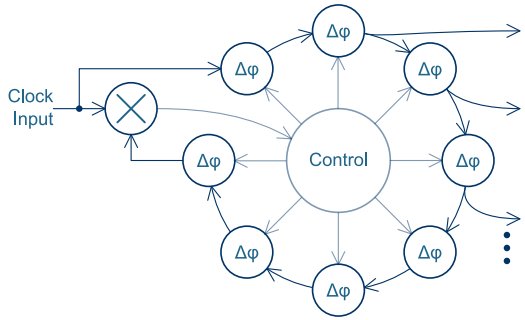

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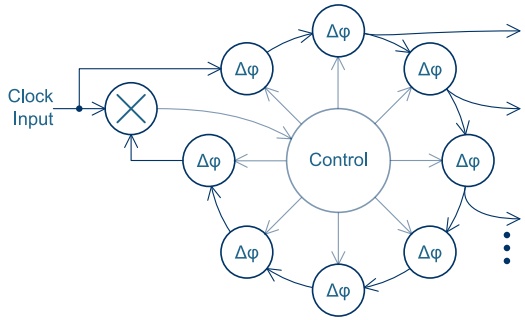

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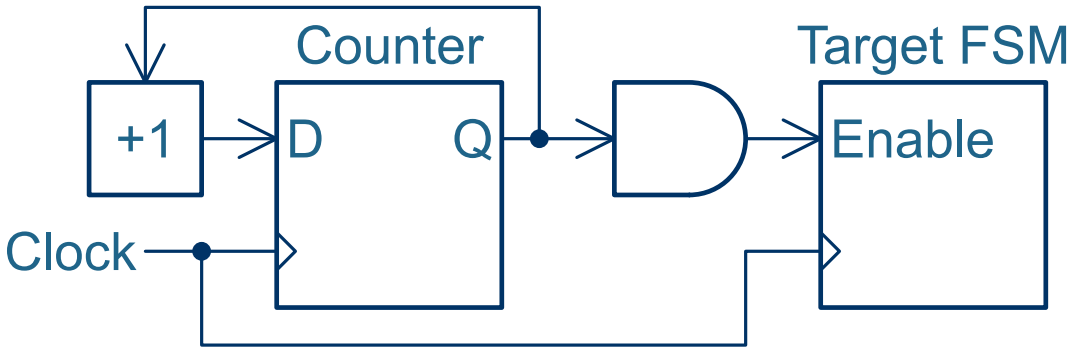

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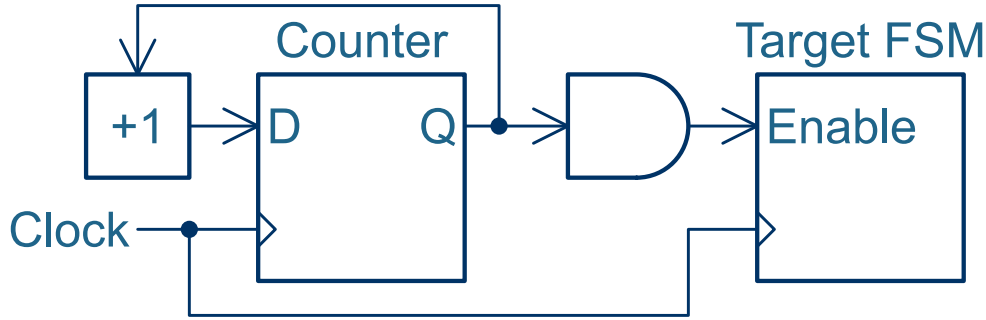

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- Potential to reduce overall device power usage
- Cannot be used for clocking external devices
- The multi-cycle timing requirements must be manually specified

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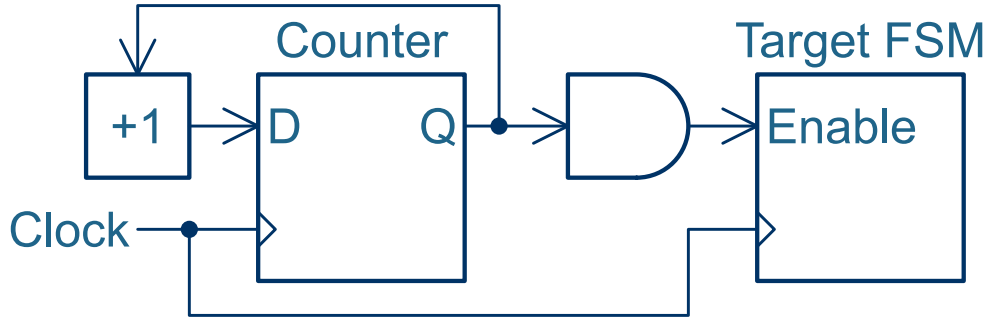

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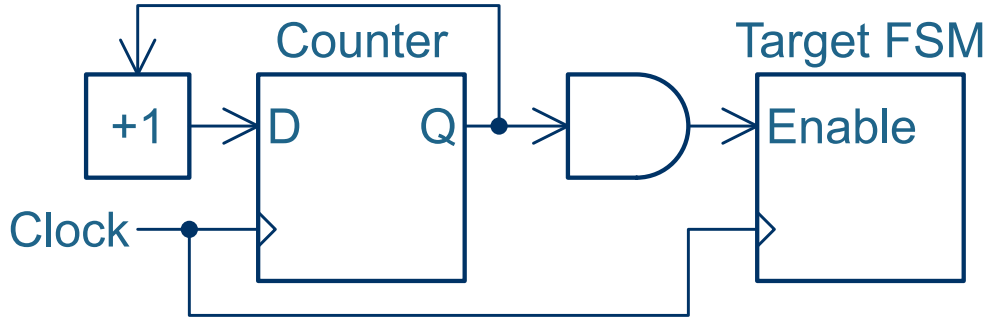

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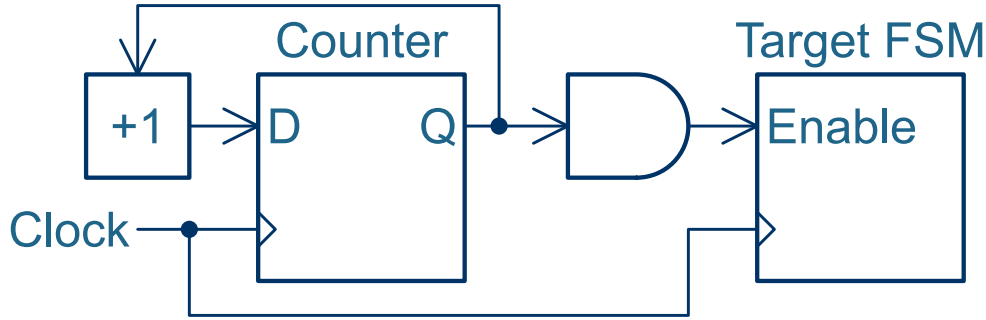

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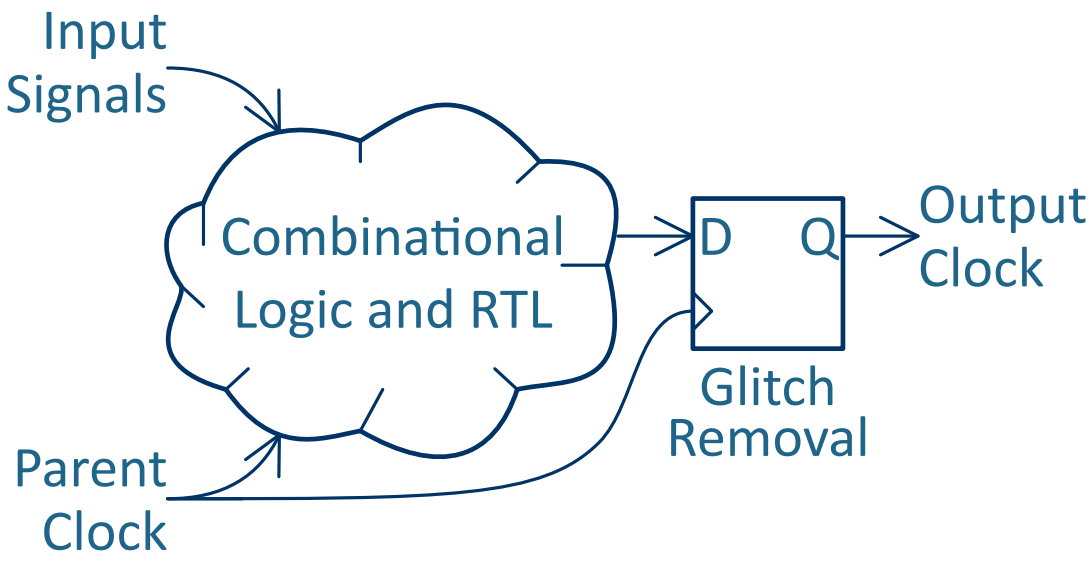

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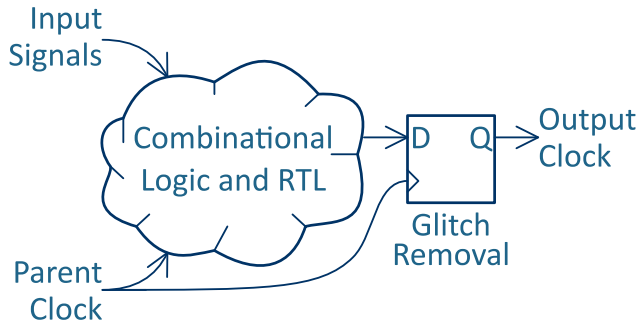

- Unrelated to all other clocks in the system, including the parent clock
- Often necessitates complex clock-domain crossing schemes to the general system clock
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  - The clock must drive an external device
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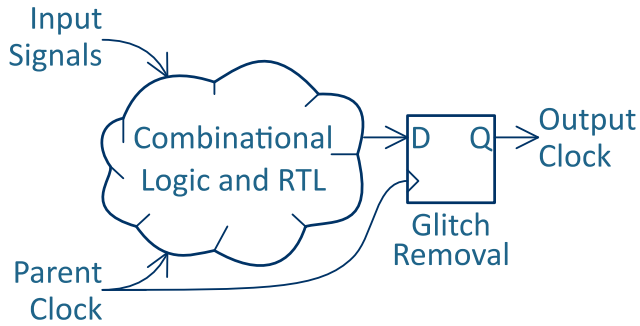

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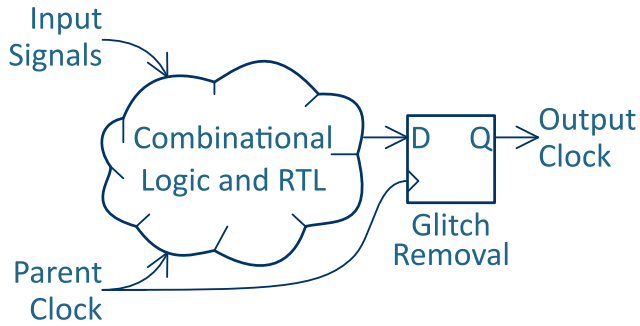

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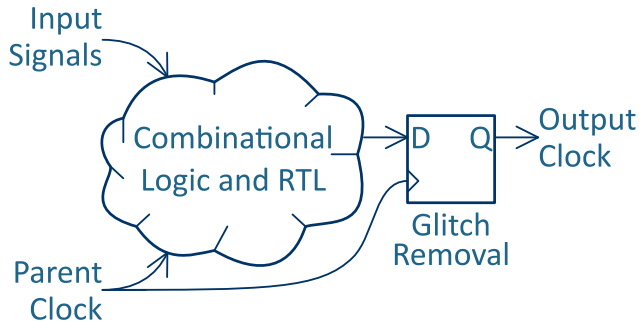

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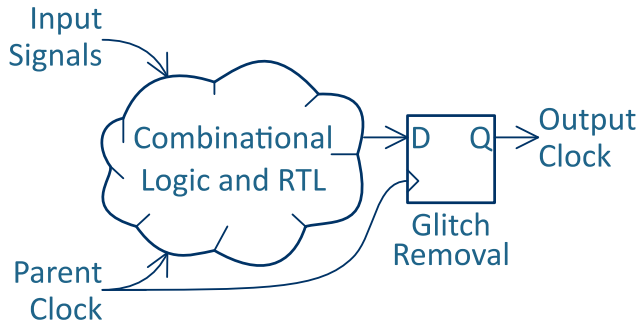

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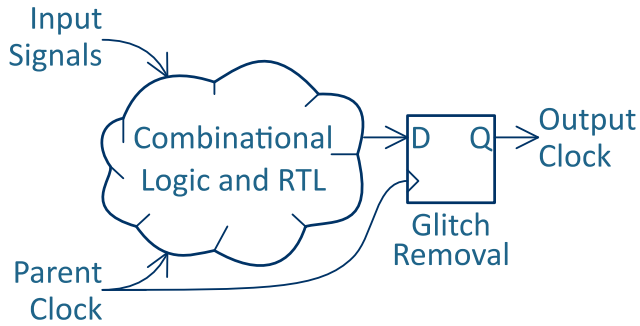

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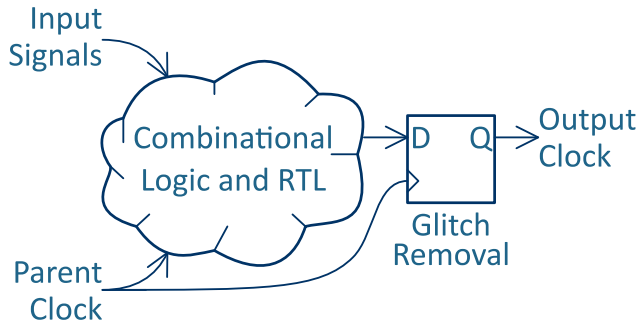

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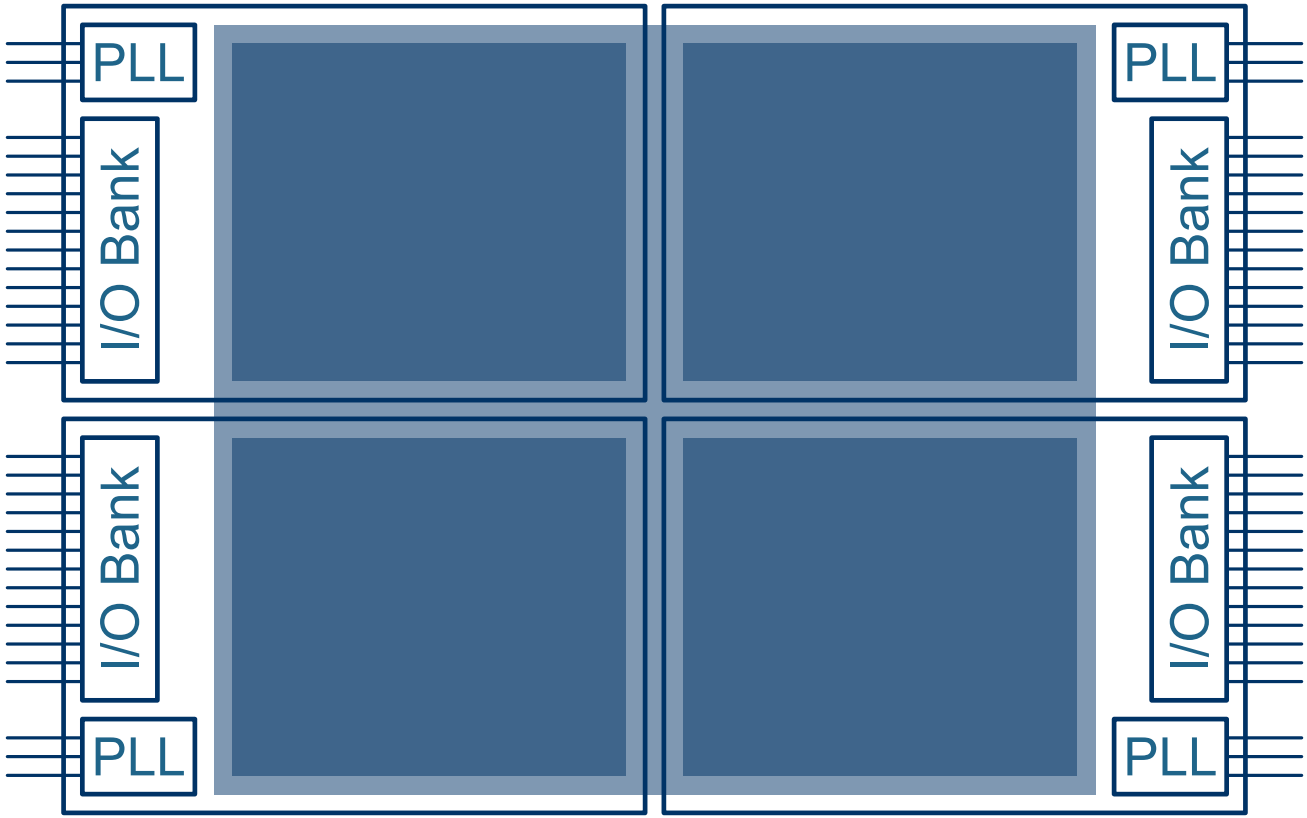

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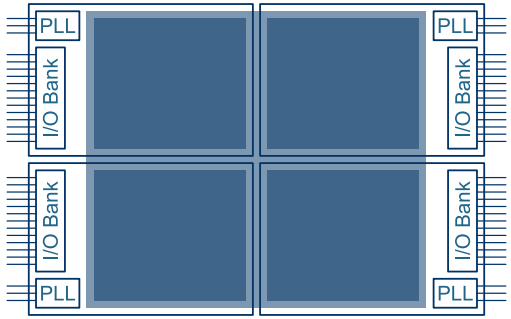

- FPGAs are generally organised into regions, each with its own PLL and I/O bank
- The local clock network is more efficient (and faster) than the global network
- When laying out the PCB, keep fast I/O in the same region as their clock

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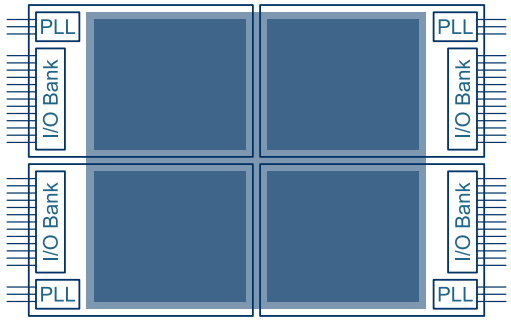

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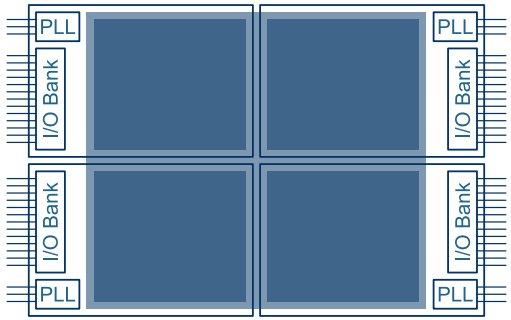

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Common Mistake

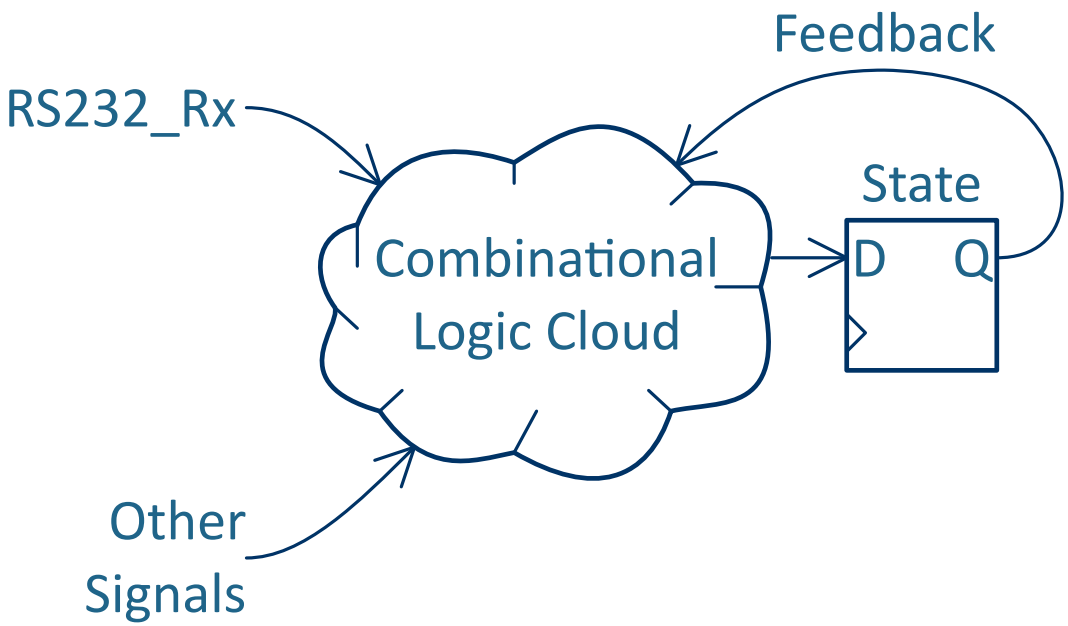

```
module RS232(
  input  ipClk, ipReset,
  input  ipRS232_Rx, // Asynchronous external signal
  output [7:0]opData
);

... // Definitions, state machine boilerplate, etc.

  Idle: begin
    if(!ipRS232_Rx) begin
      State <= Receiving;
    end
  end

  Receiving: begin
...
```

Common Mistake



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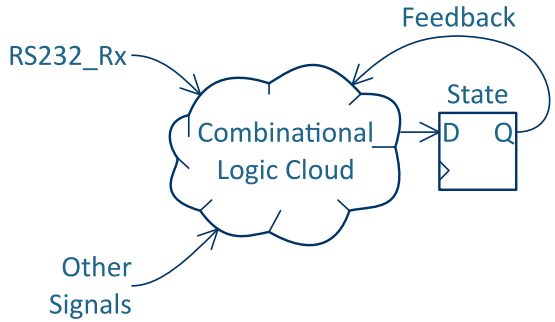
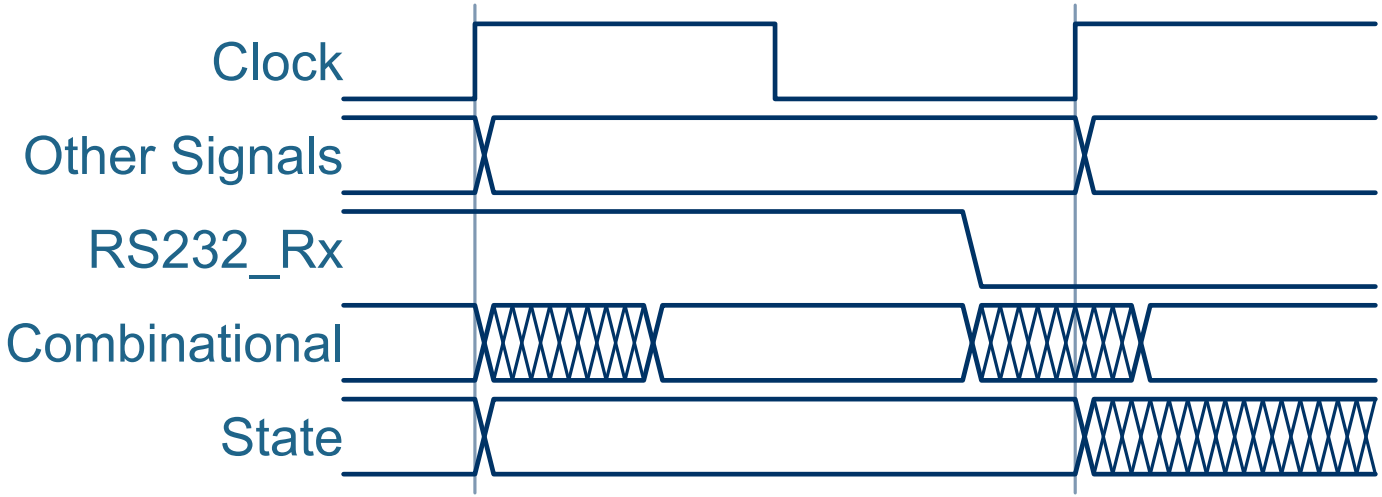
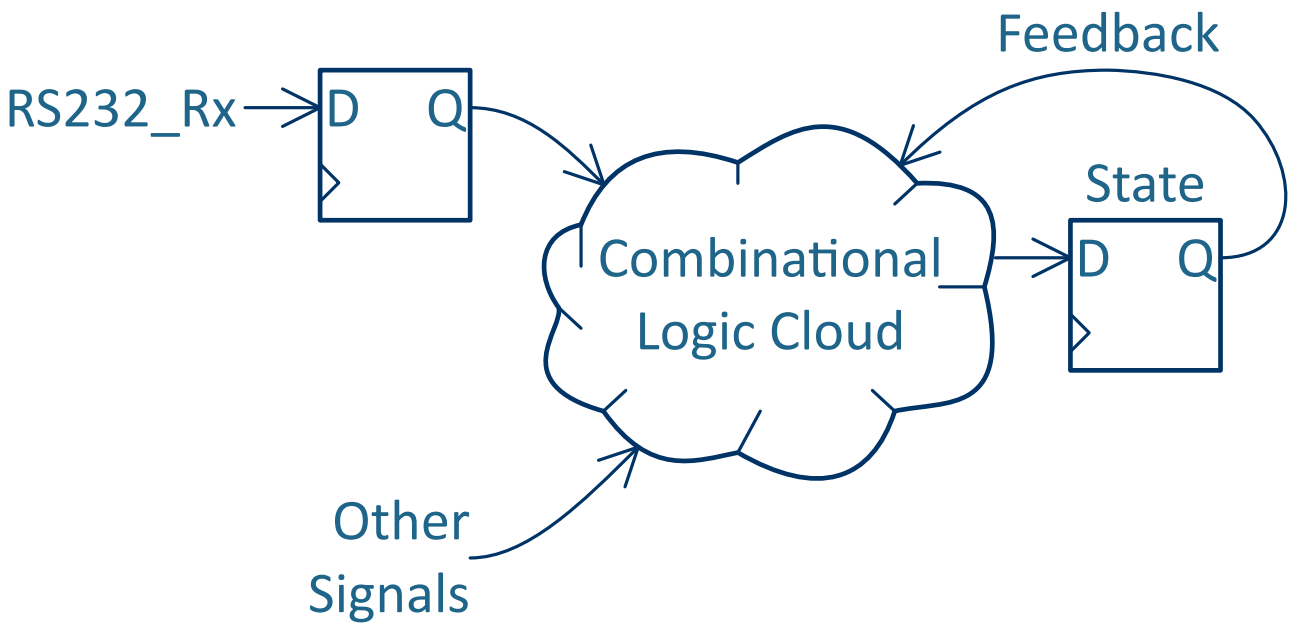




The Solution



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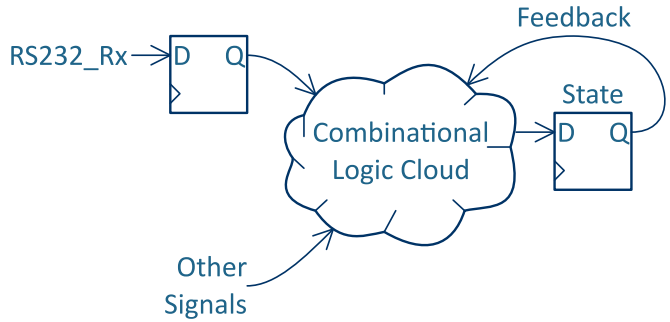
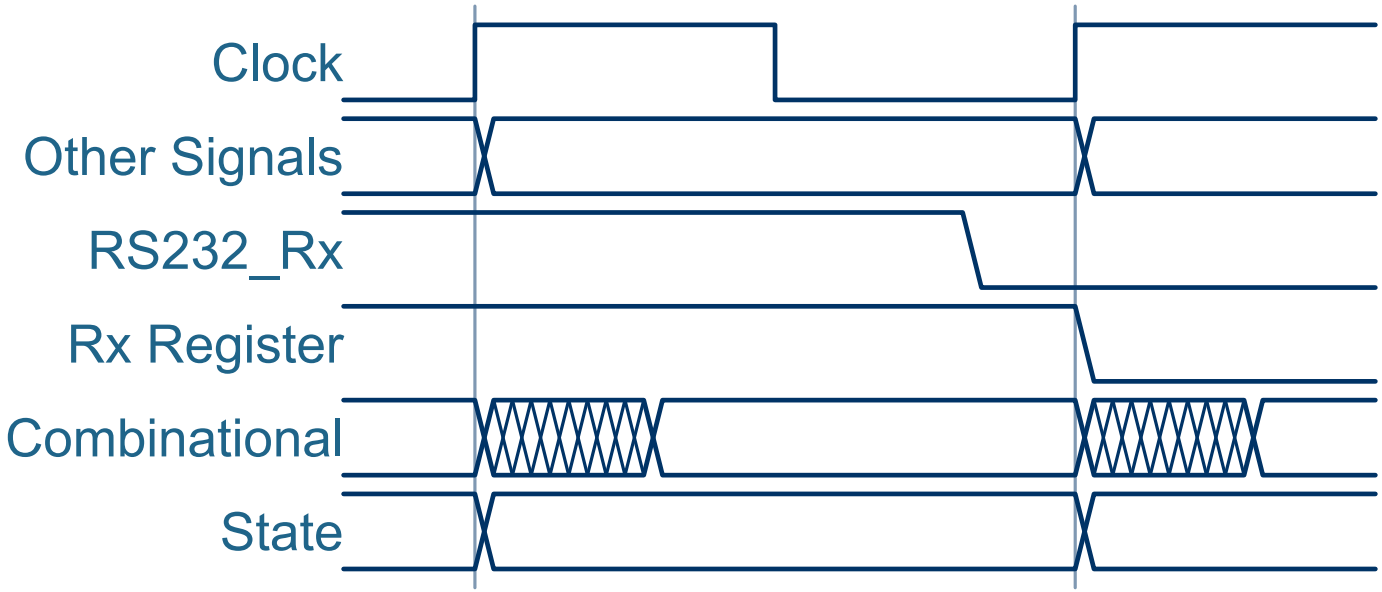
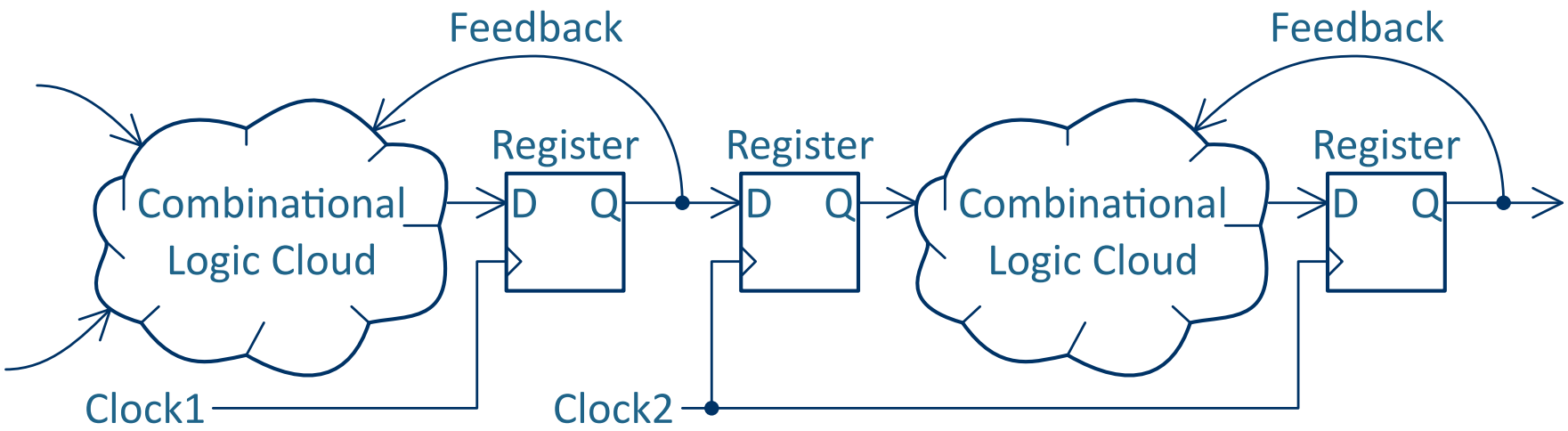




Register Chain



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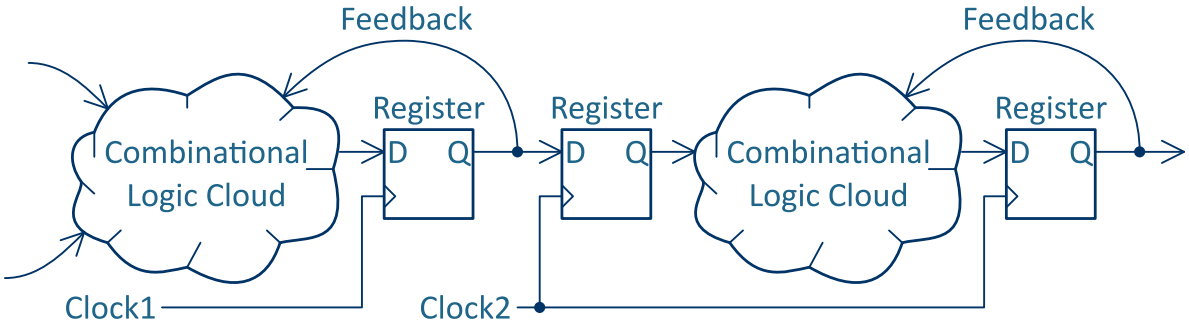

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- Only useful for crossing one bit at a time (unless the system is tolerant to temporary errors)
- Often used to cross hand-shaking signals
- Works in both directions (fast to slow / slow to fast)

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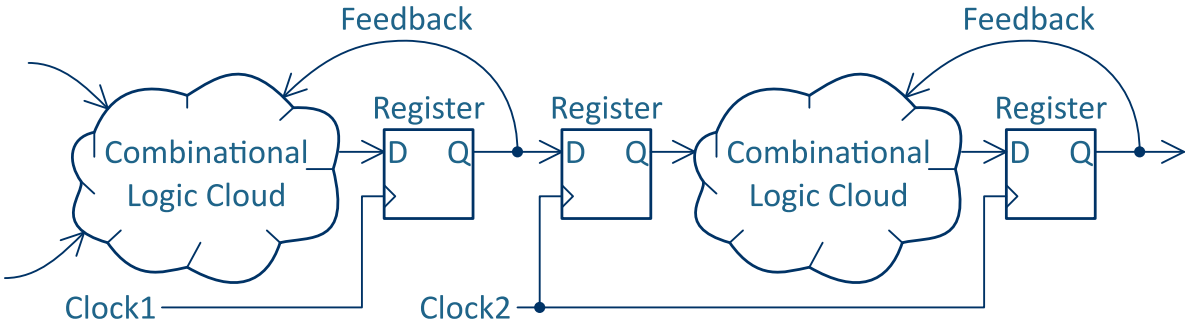

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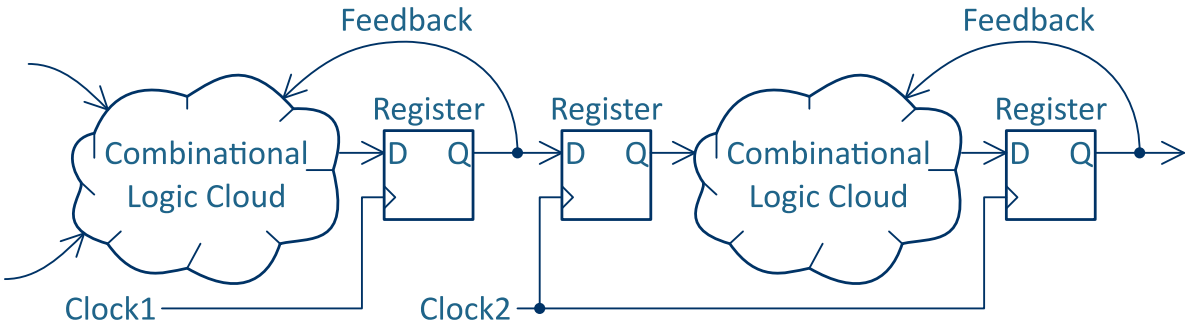

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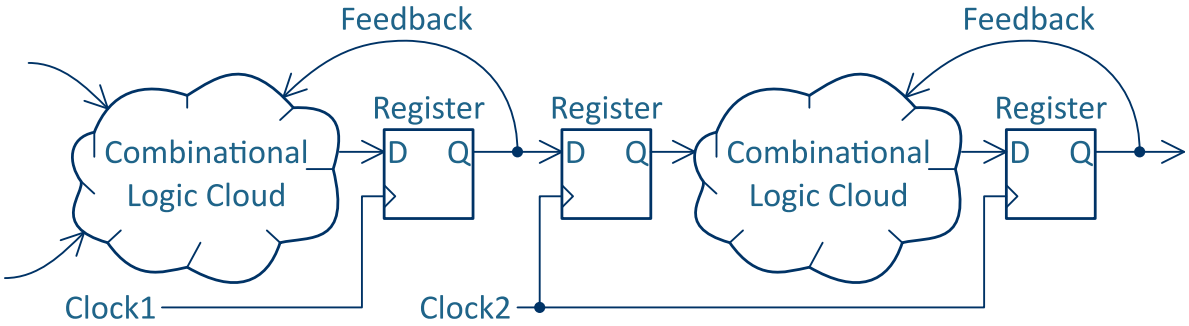

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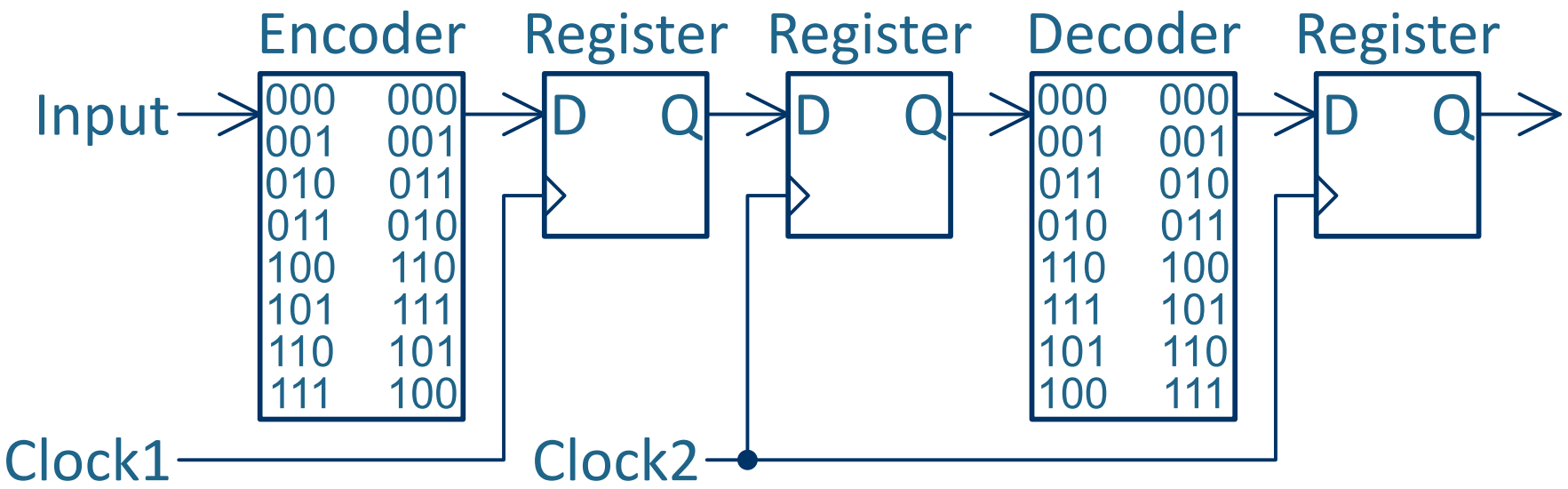
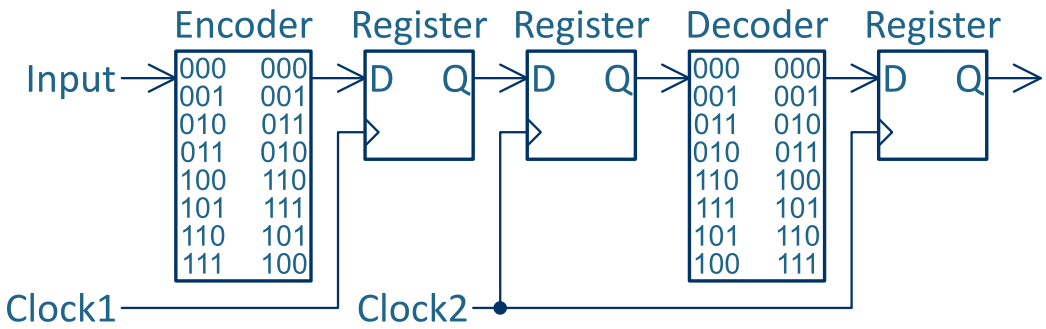
Gray Coding


Encoder
Register
Register
Decoder
Register
Input
000 000
001 001
010 011
011 010
100 110
101 111
110 101
111 100
D Q
D Q
000 000
001 001
011 010
010 011
110 100
111 101
101 110
100 111
D Q
Clock1
Clock2

Gray Coding



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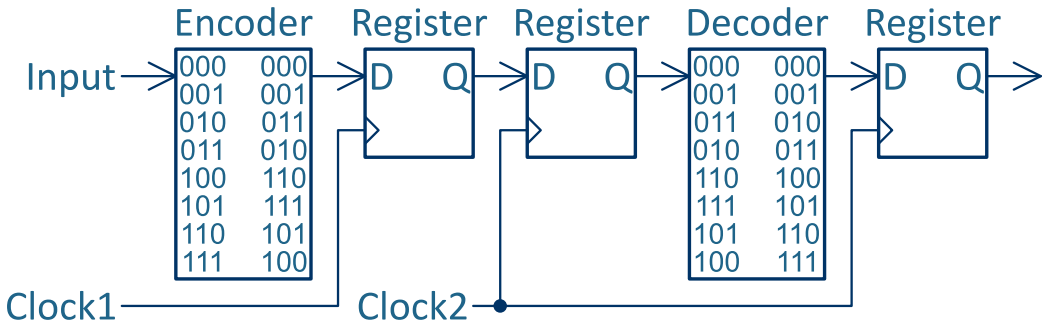

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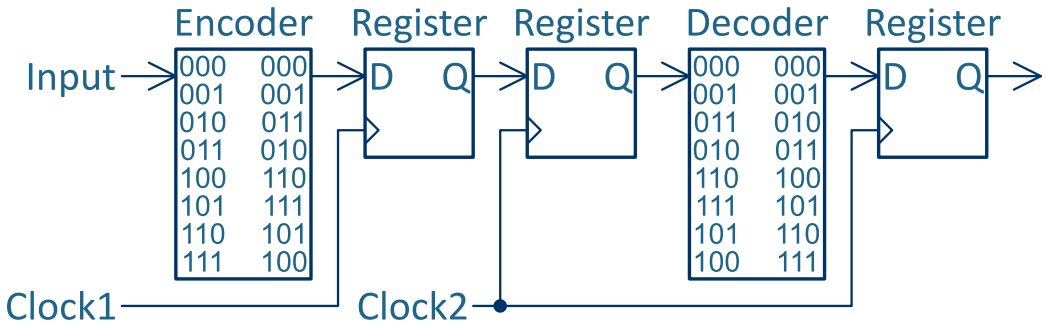

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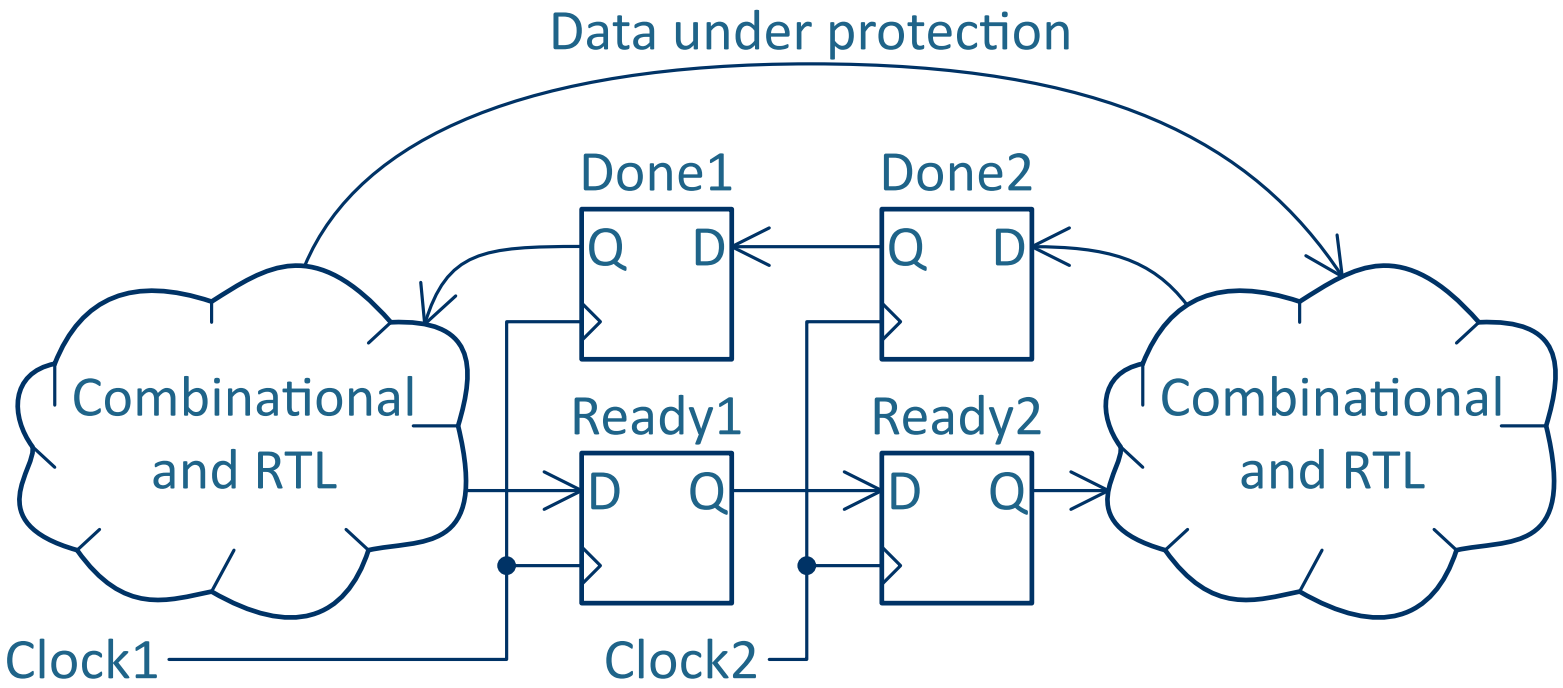
Hand-Shaking



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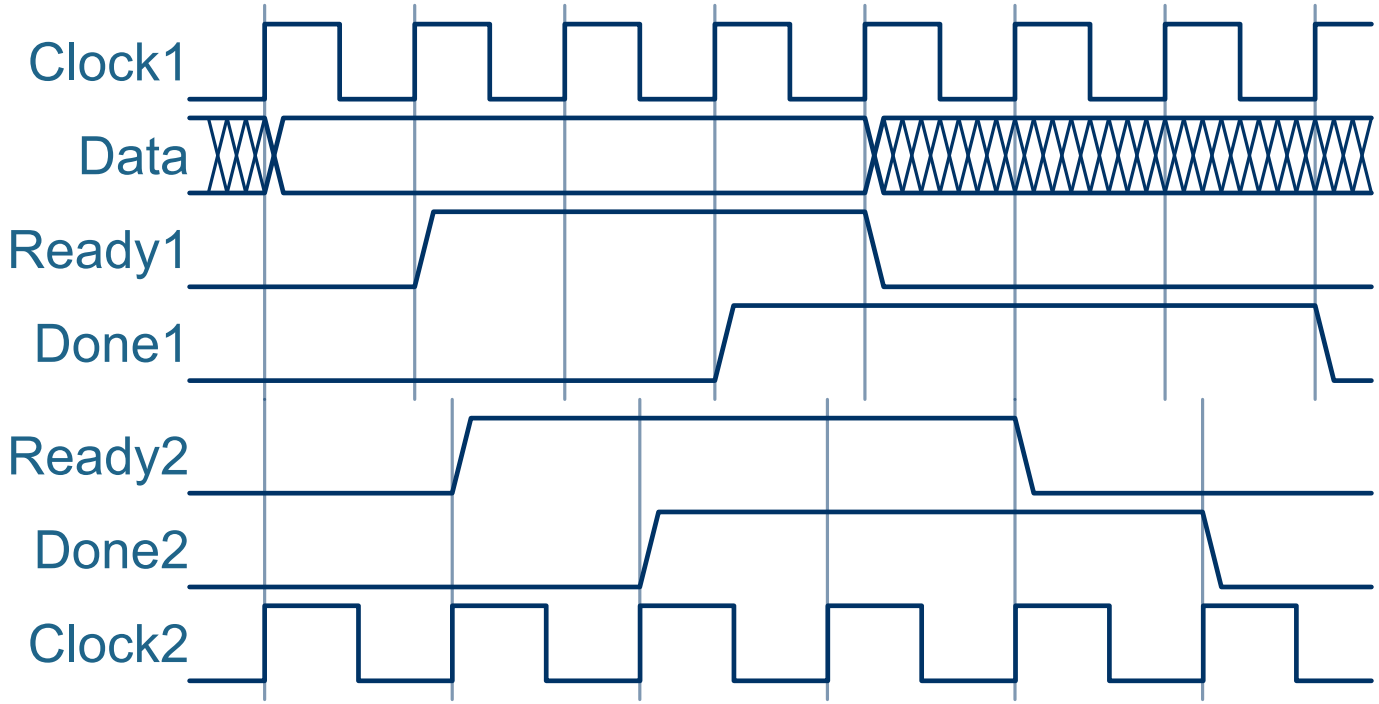

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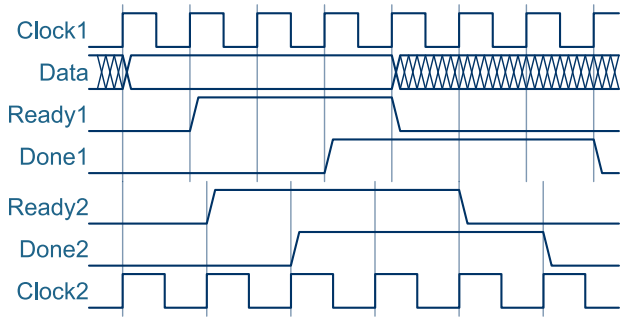

- Source must guarantee data stability while the handshaking is taking place
- Not time-efficient: need to wait for the entire transaction sequence to finish before starting the next one
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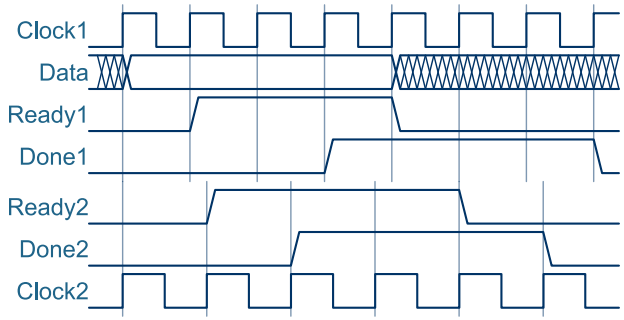

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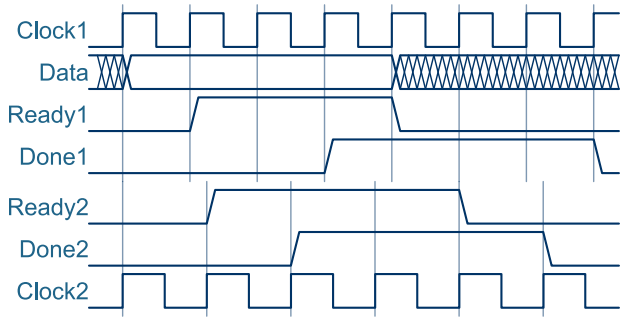

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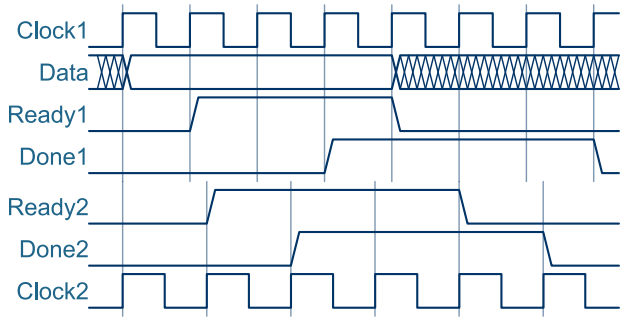

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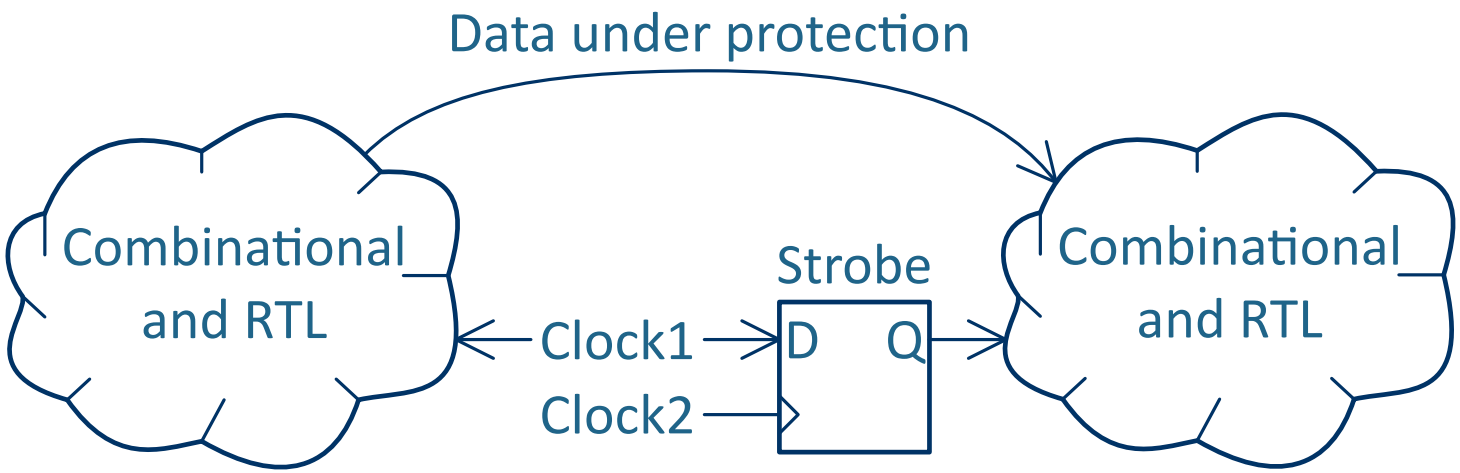

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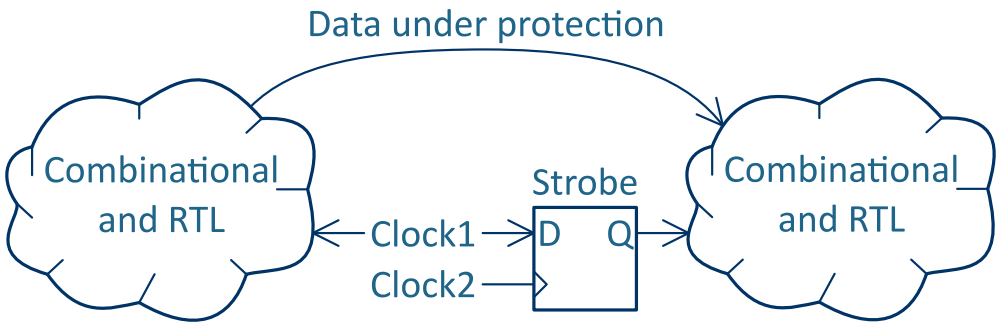

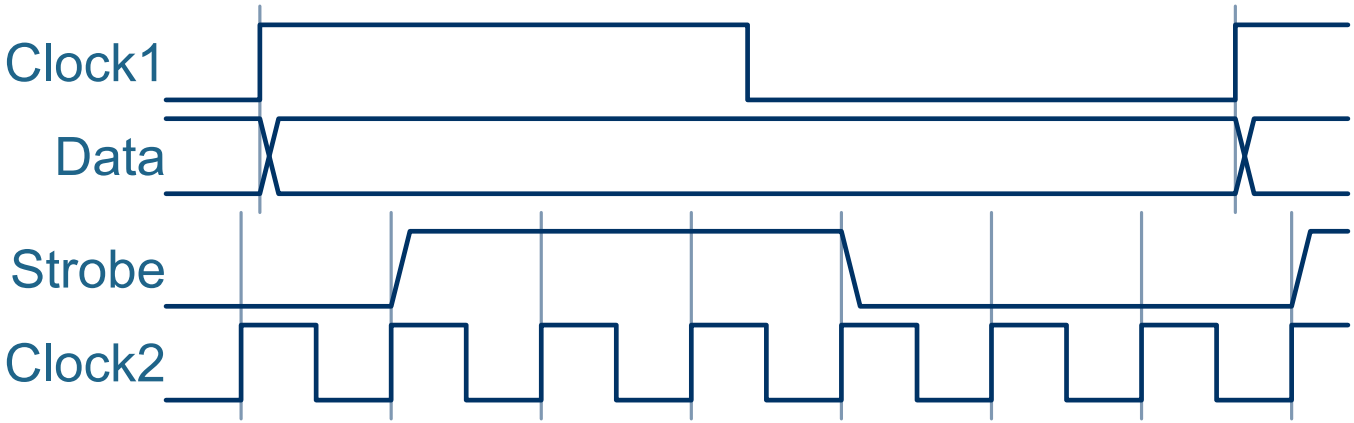

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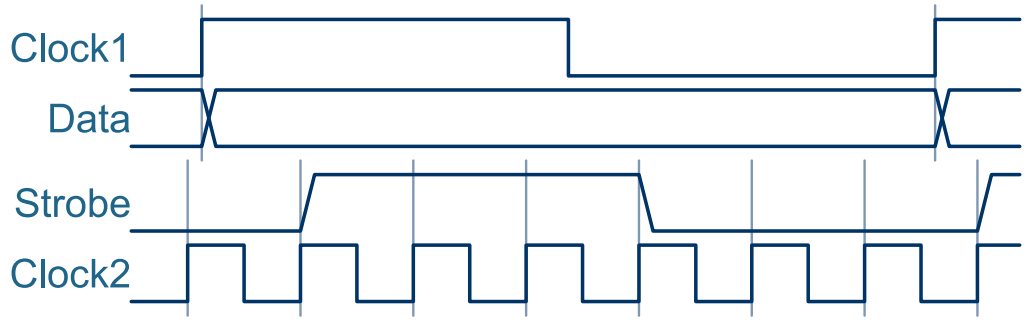

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- As fast as the source clock
- The strobe edges can be used to perform flow-control
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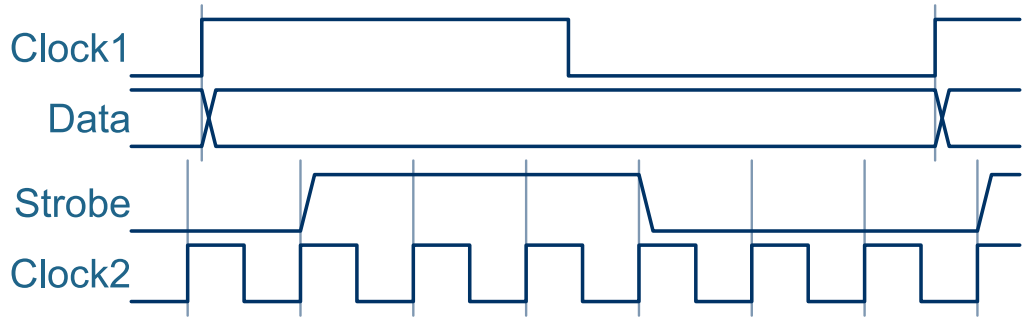

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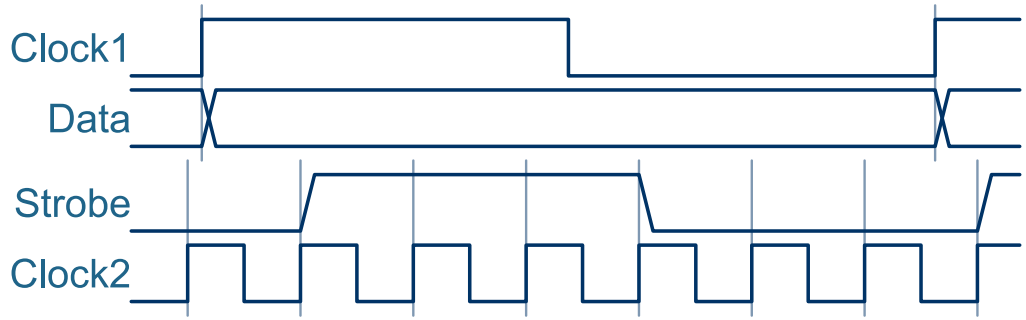

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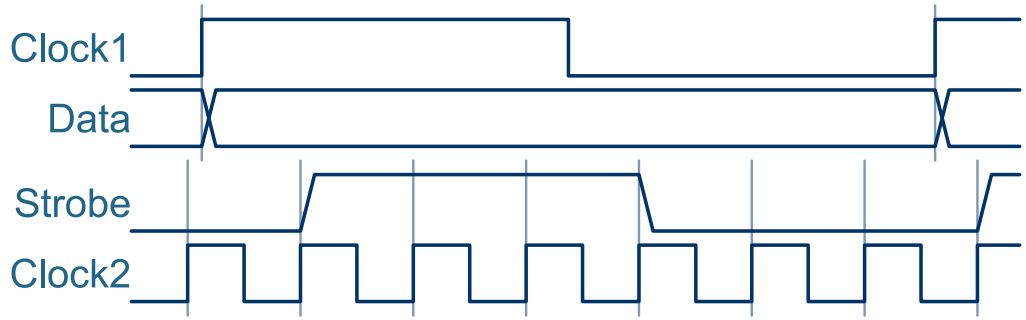

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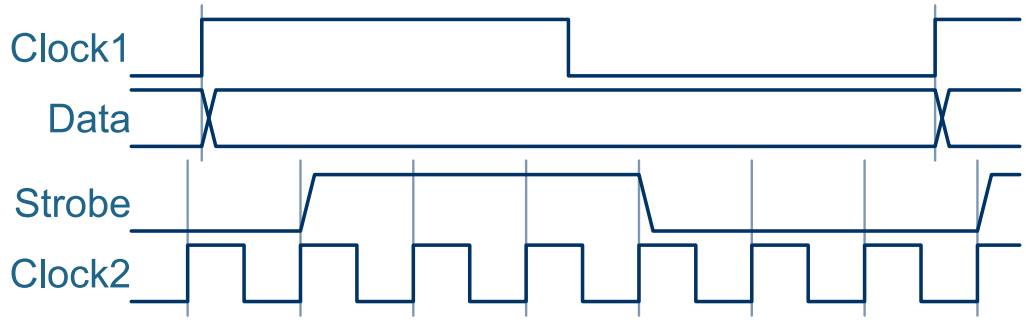

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```
set_clock_groups -logically_exclusive \
  -group [get_clocks ADC_Clk]          \
  -group [get_clocks Clk1]             \
  -group [get_clocks Clk2]             \
  -group [get_clocks {SRAM_CLK *altpll_0*}]
```

Coffee Break...

Outline

Advanced Clocking

Clock Domains

Mutual Exclusion and Arbitration

Caching Systems

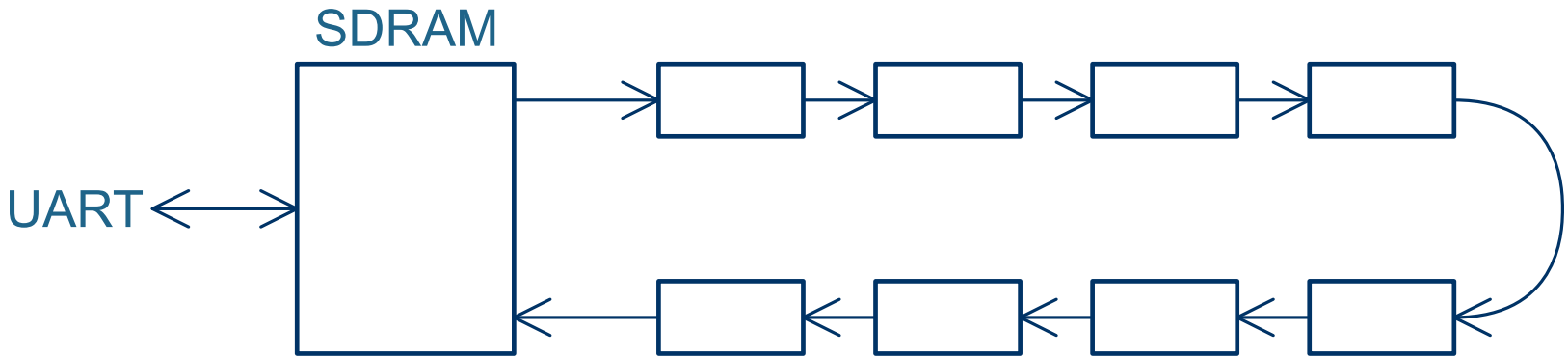
Flow Control

Practical – NCO and DDC

Numerically-controlled Oscillator

THE RADAR MASTERS COURSE

Sharing Resources



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- Examples include:
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  - I^2C bus
  - etc.

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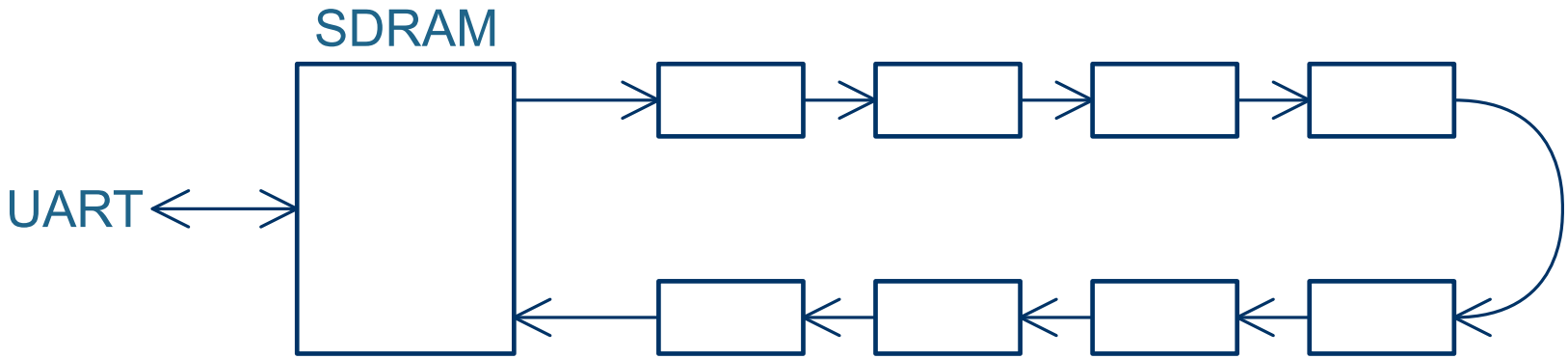

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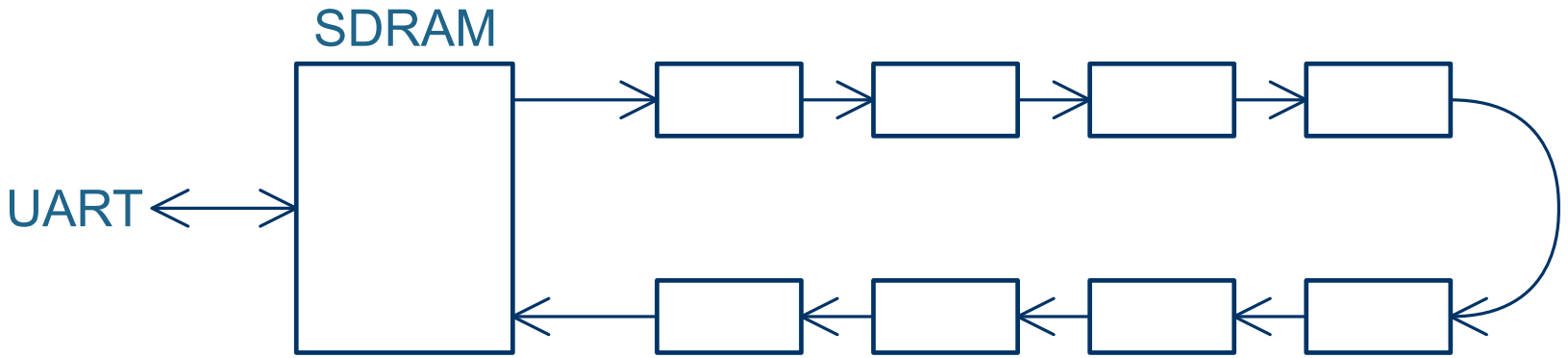

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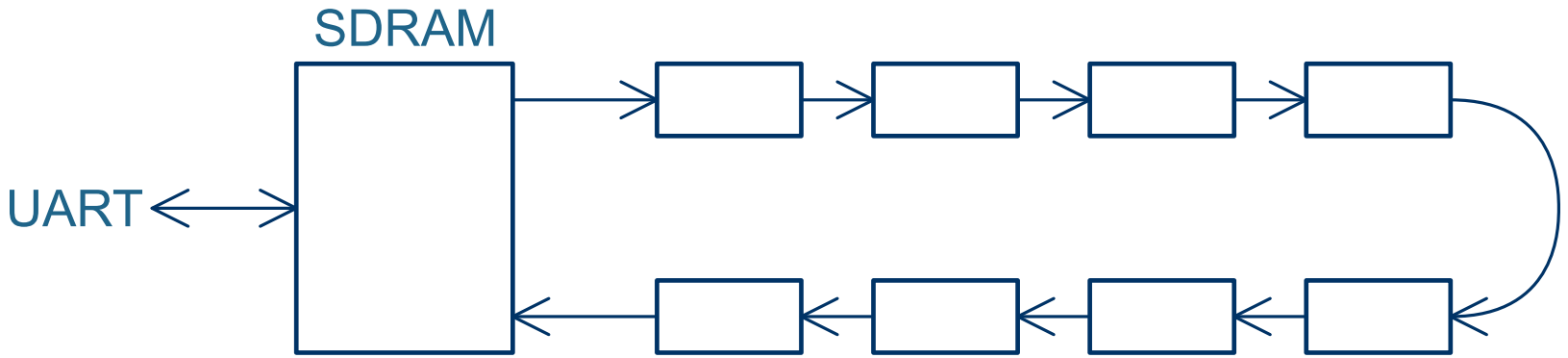

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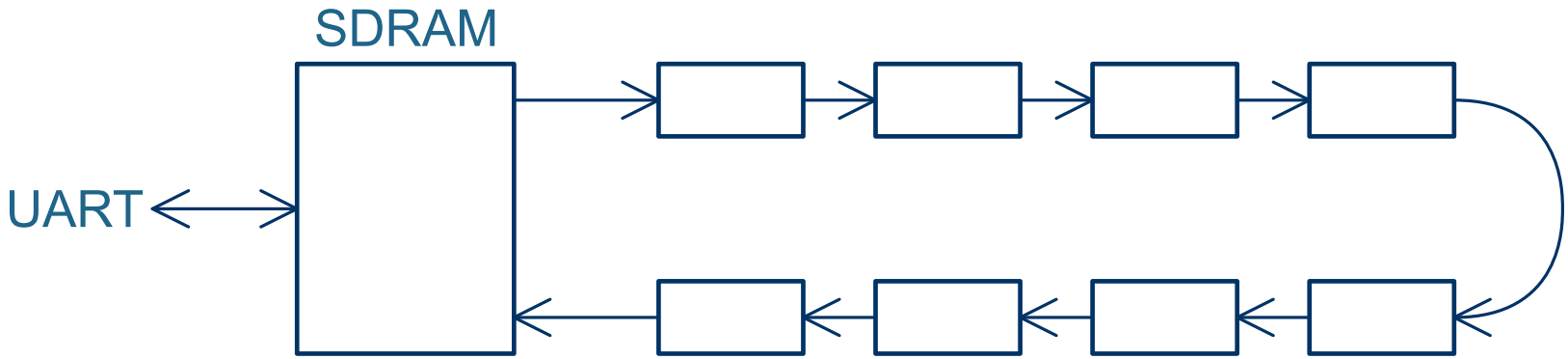

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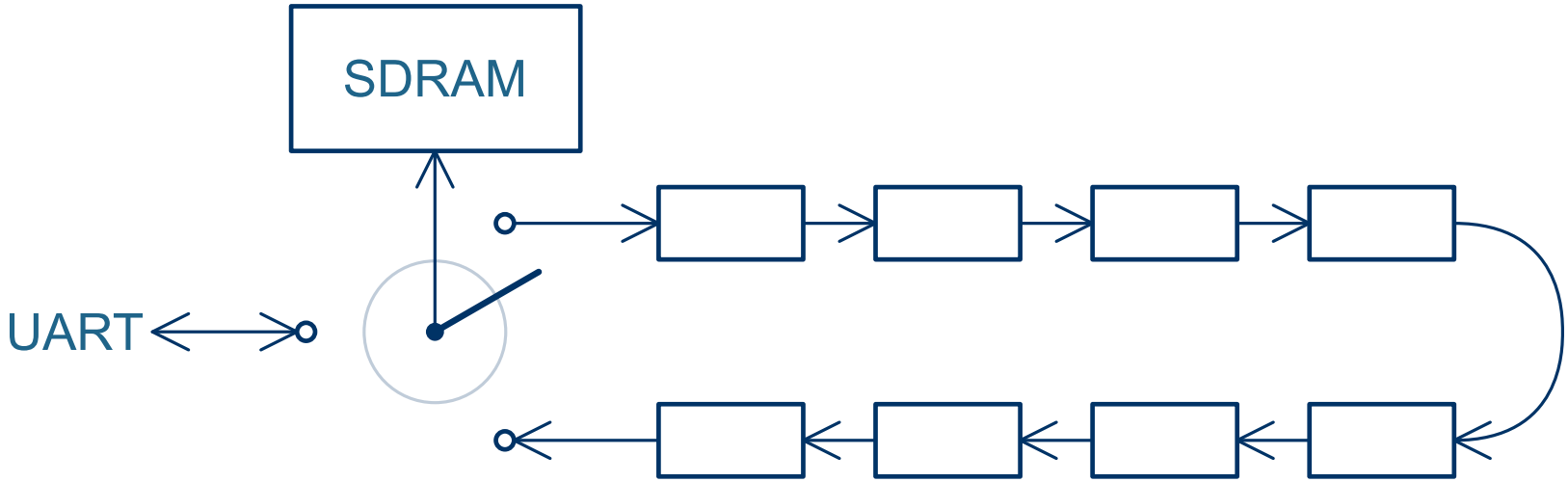

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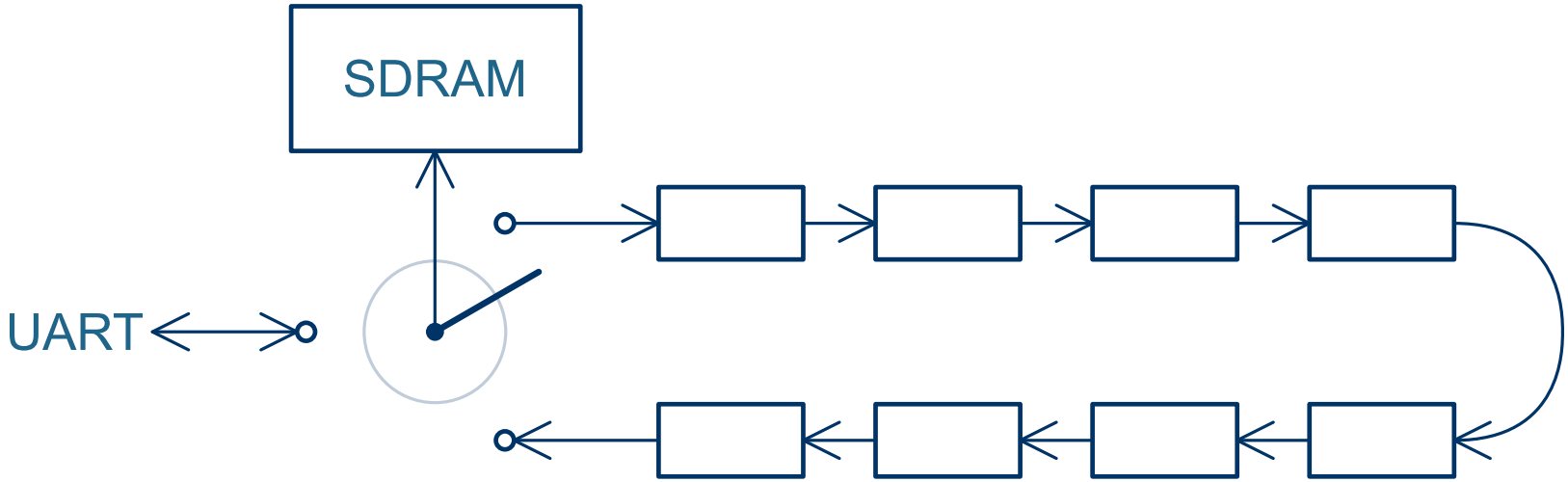

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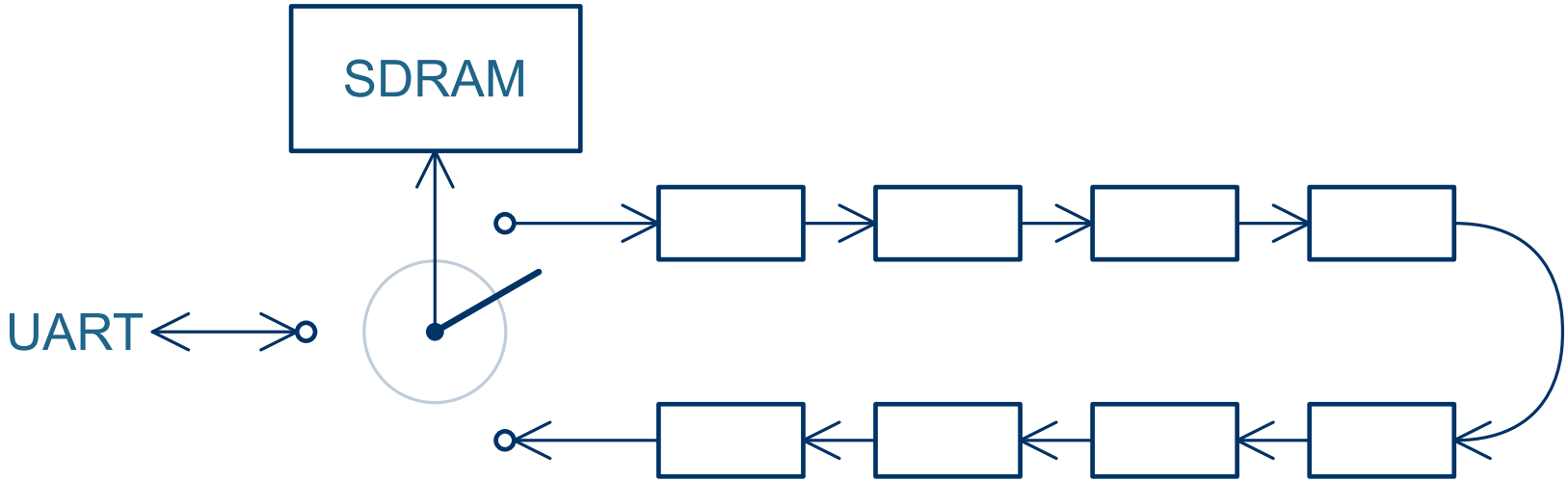

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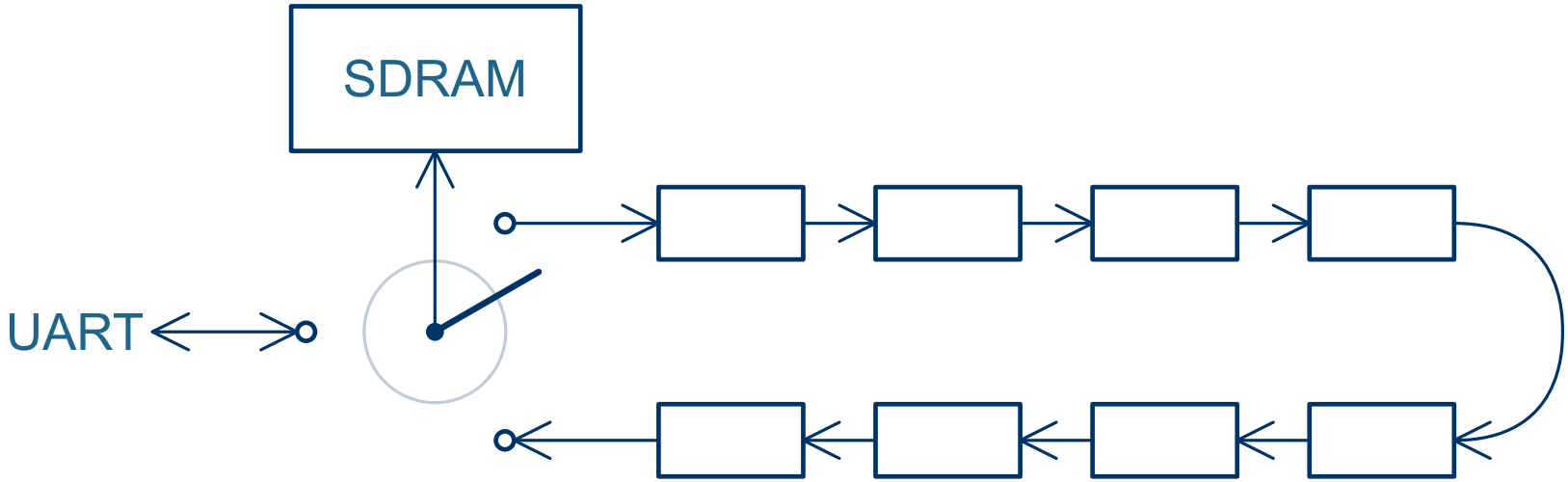

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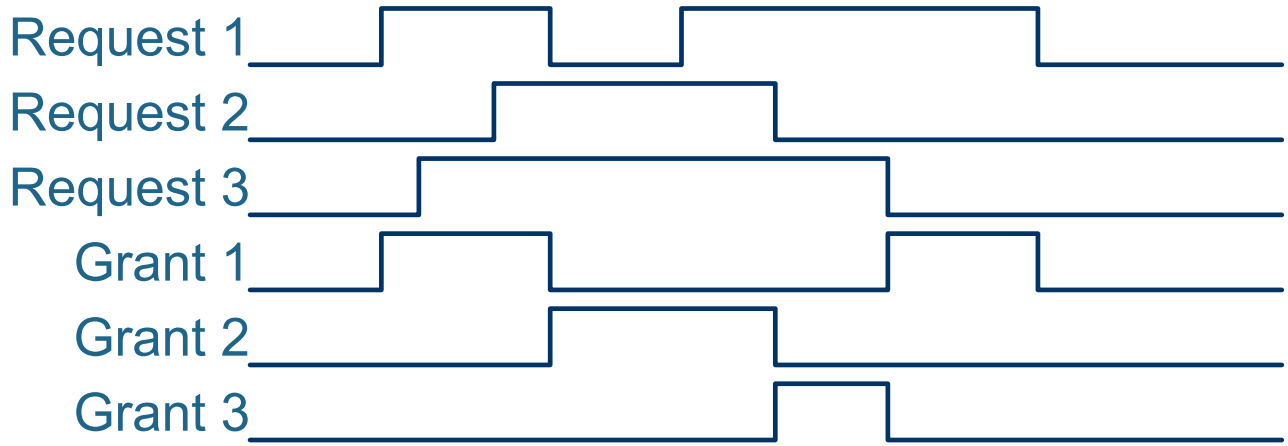

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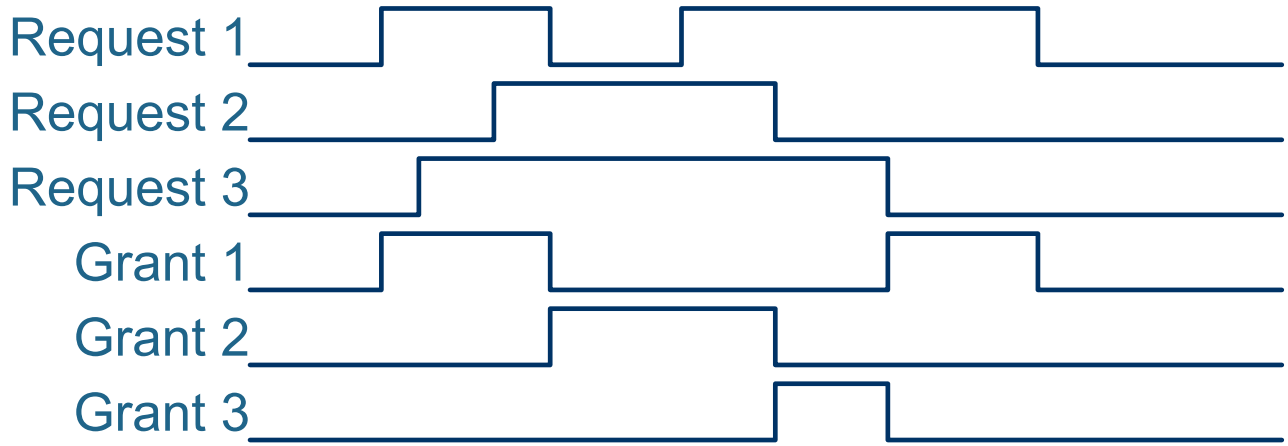

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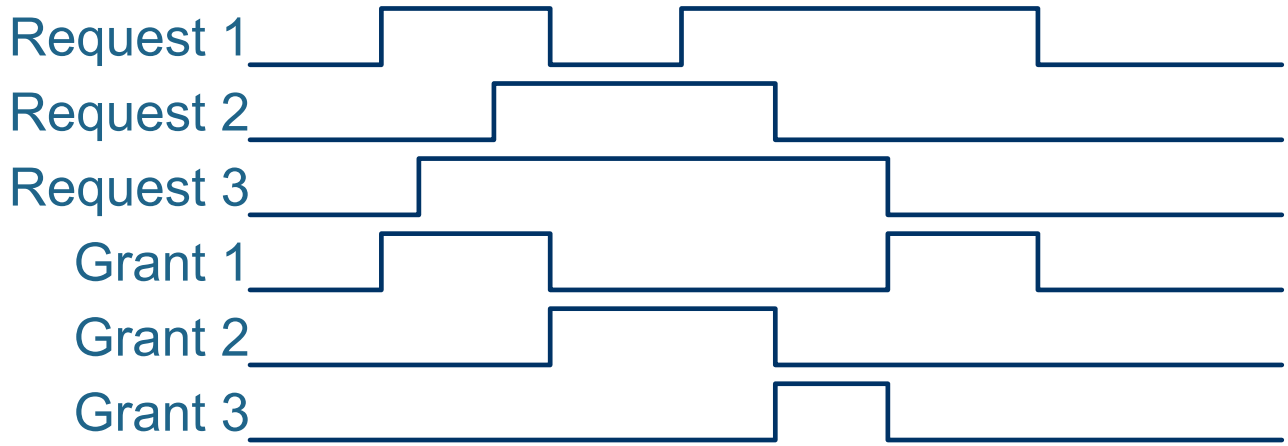

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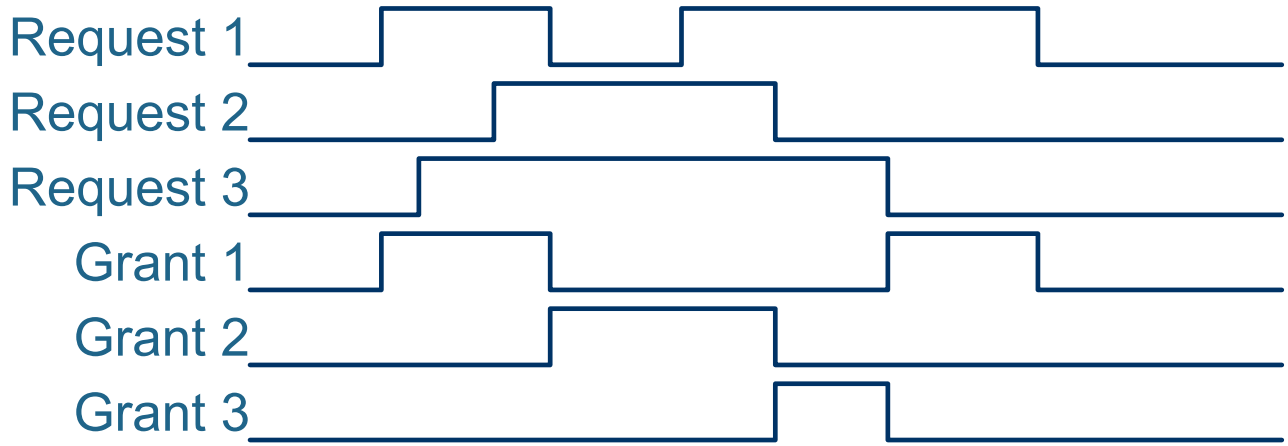

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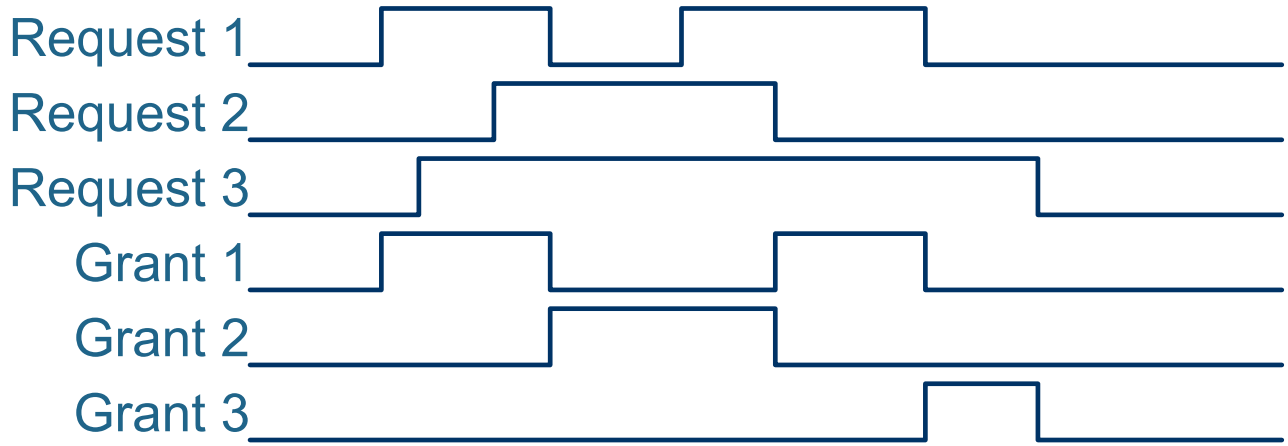

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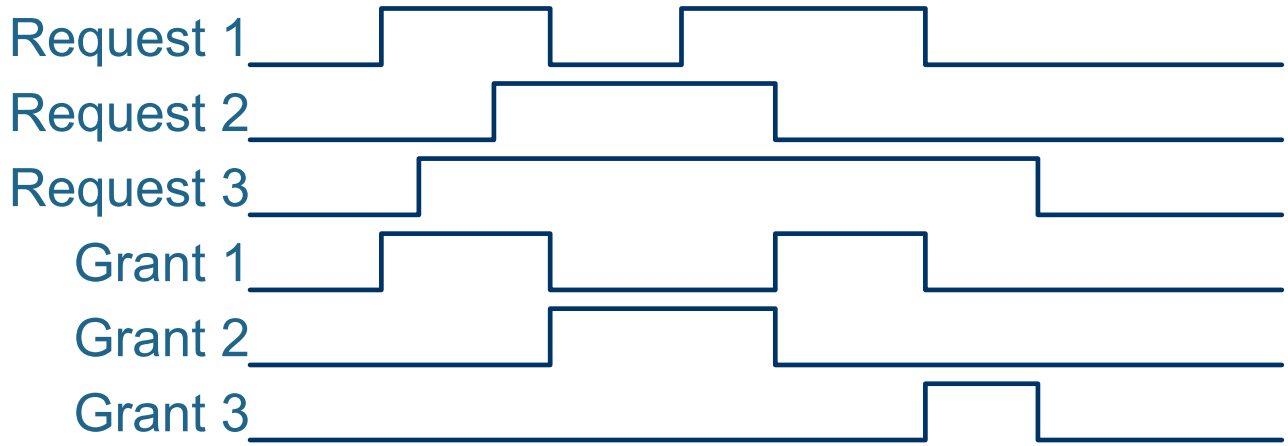

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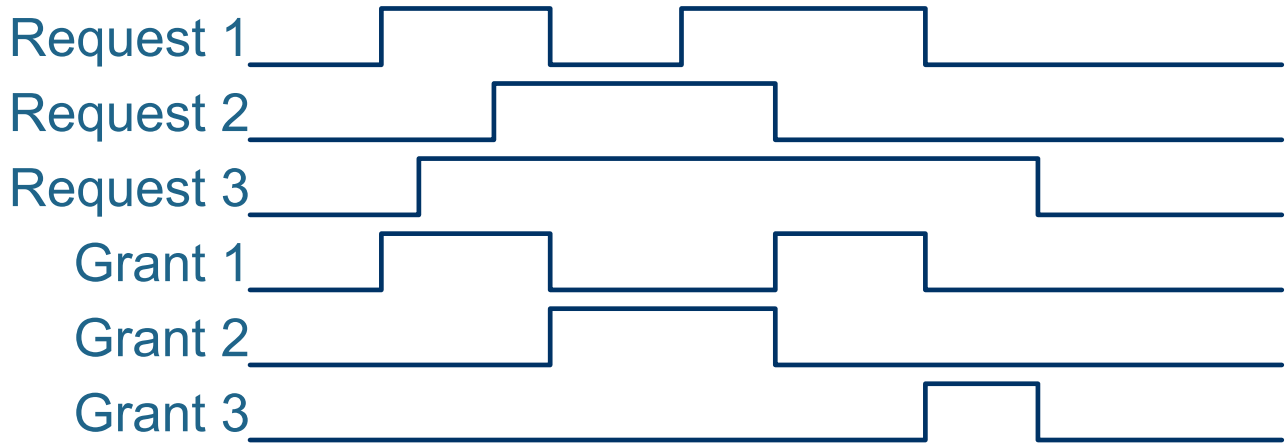

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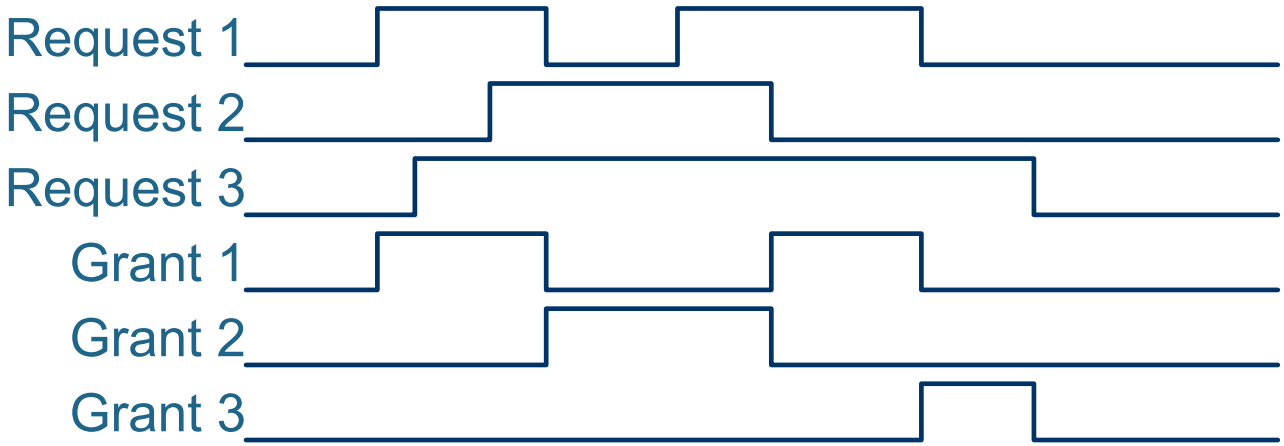

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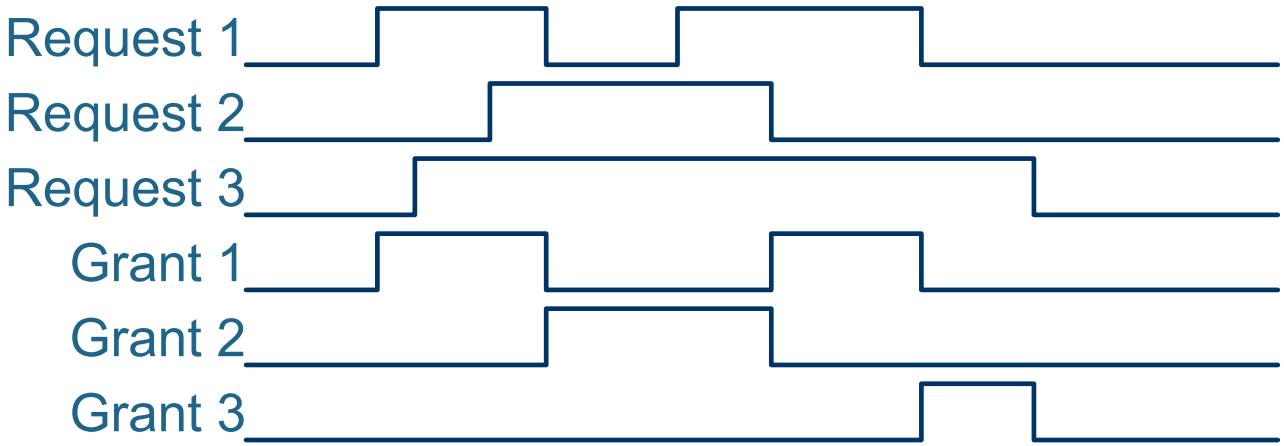

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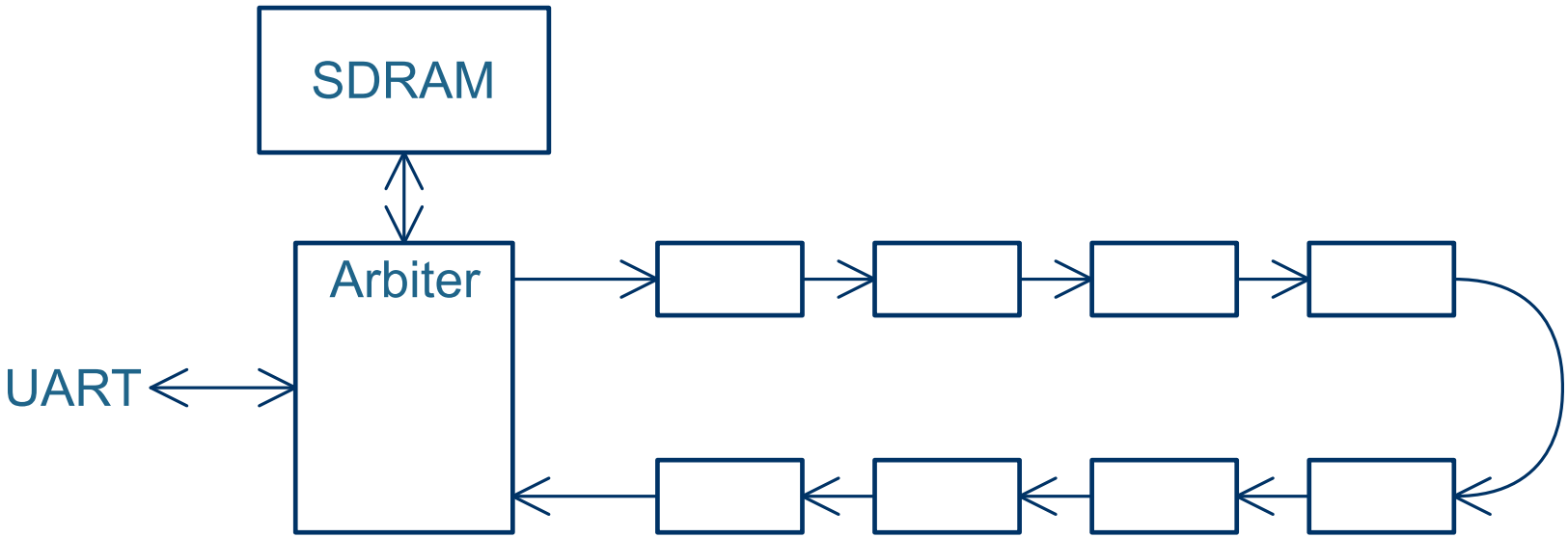

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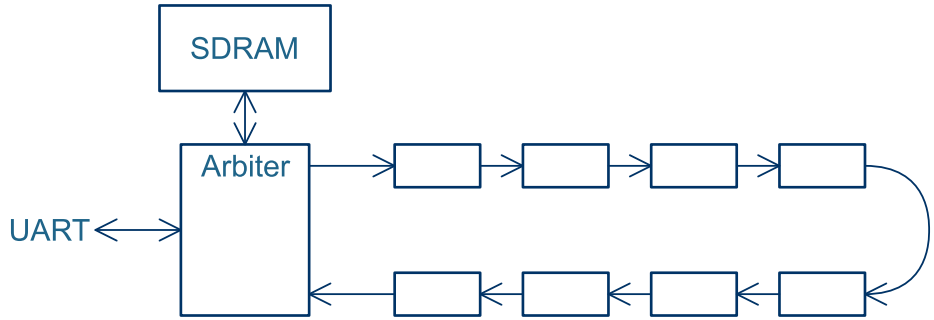

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- Often implemented by means of an embedded mutual exclusion unit (round-robin or priority based)
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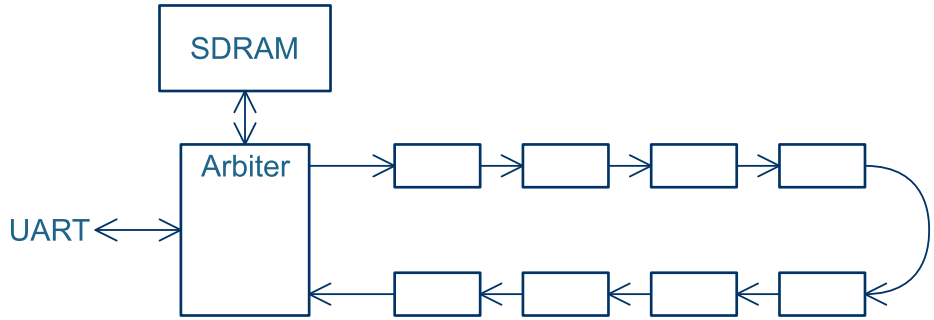

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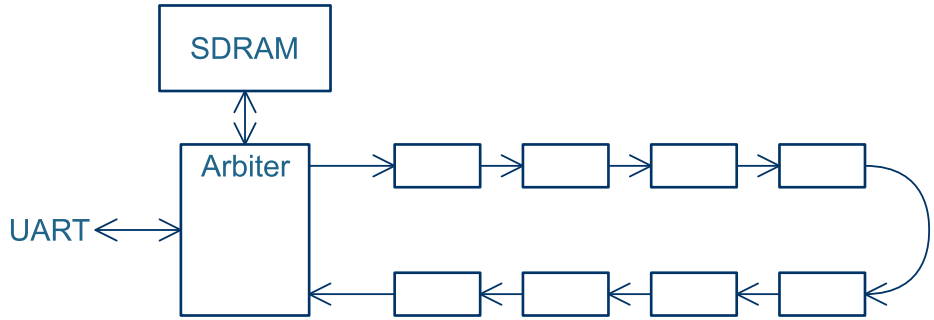

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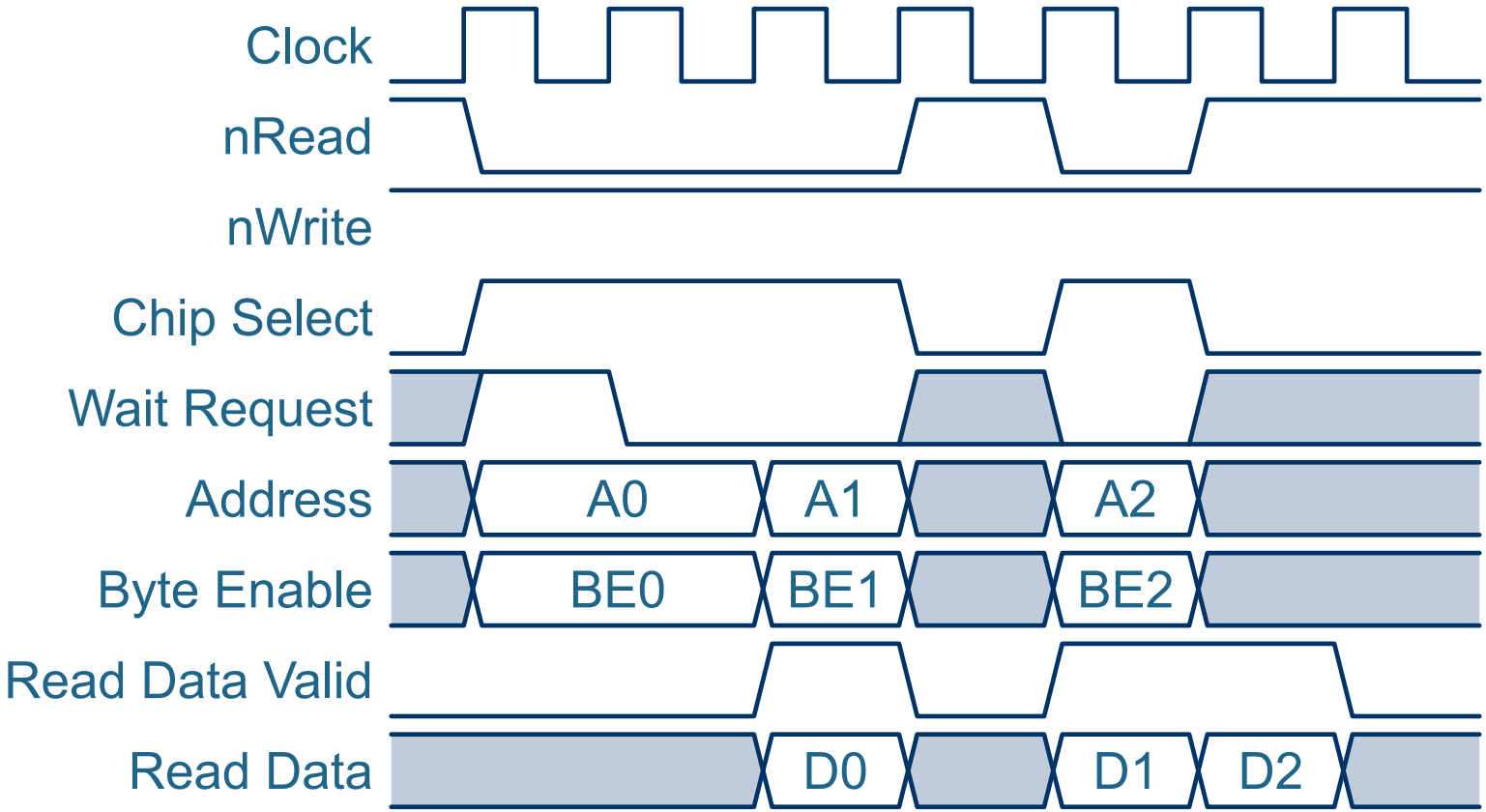
- The I^2C standard implements arbitration by collision-detection and random back-off: the modules monitor their own output, and when there is a mismatch, the module waits and tries again later.

Avalon Bus Arbitration



Outline

Advanced Clocking

Clock Domains

Mutual Exclusion and Arbitration

Caching Systems

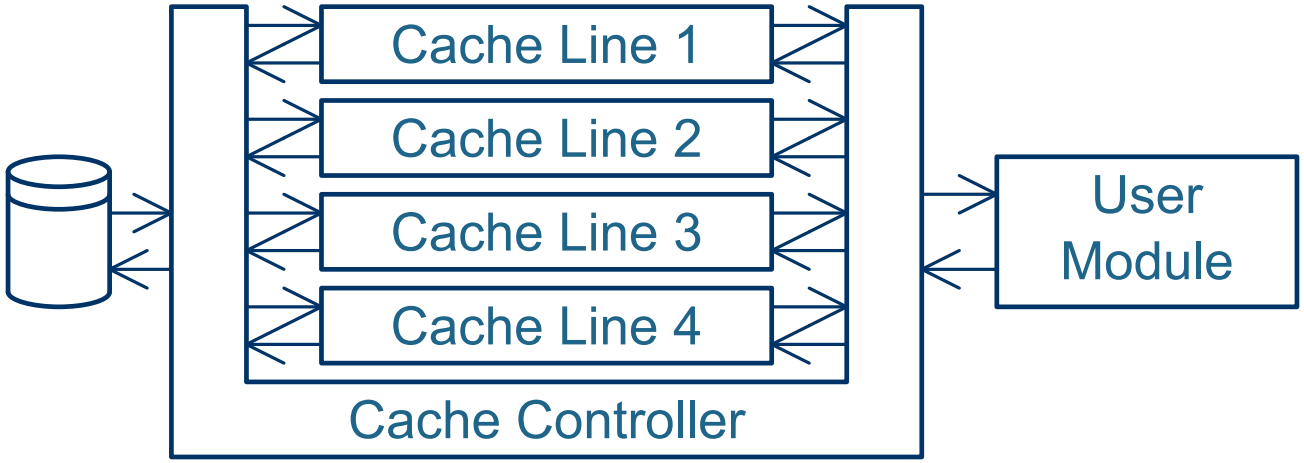
Flow Control

Practical – NCO and DDC

Numerically-controlled Oscillator

THE RADAR MASTERS COURSE

General Cache



- Lines are typically one page in size (4 kiB in modern PCs, typically smaller on embedded systems)
- The controller does address translation between the external and cache line addresses
- Read is on-demand, flushing the least recently used line and loading the content into it
- Controller blocks the user module when a cache miss occurs

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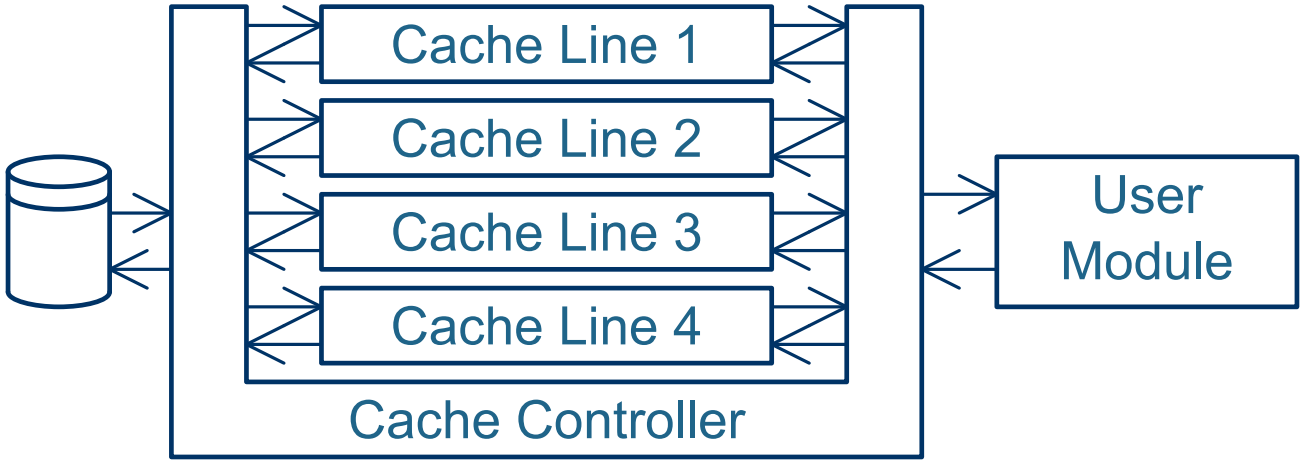

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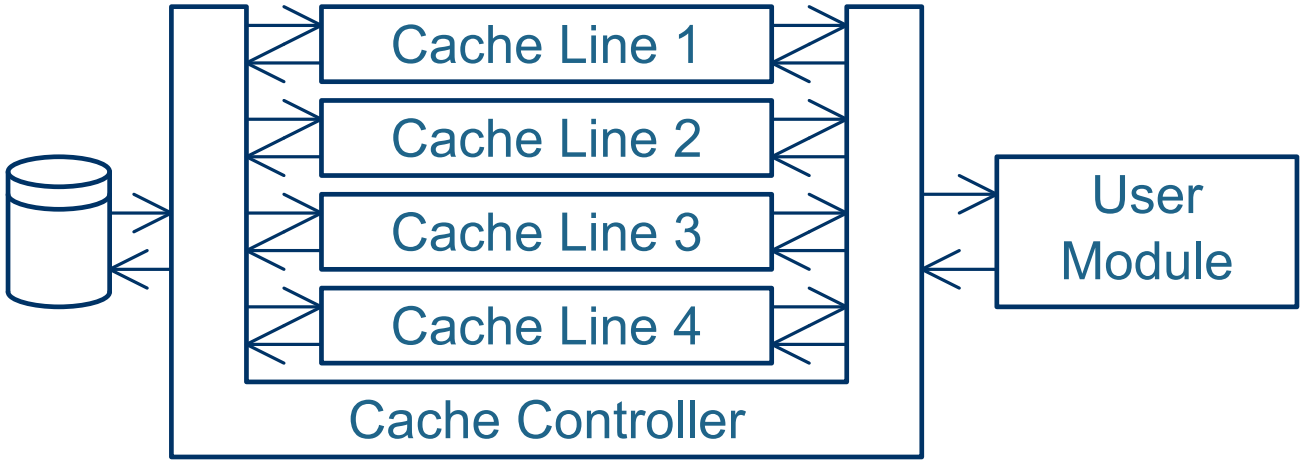

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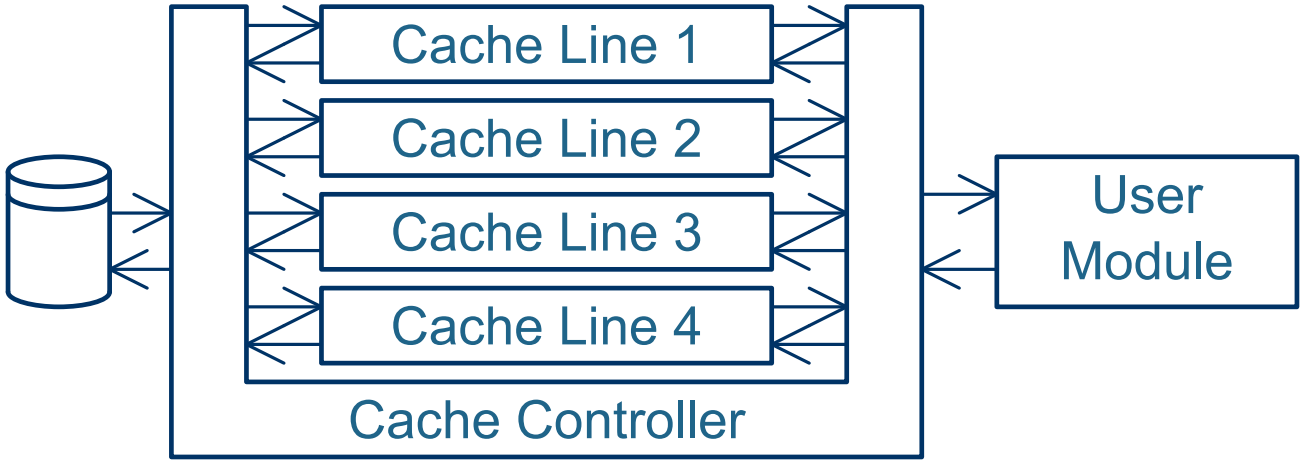

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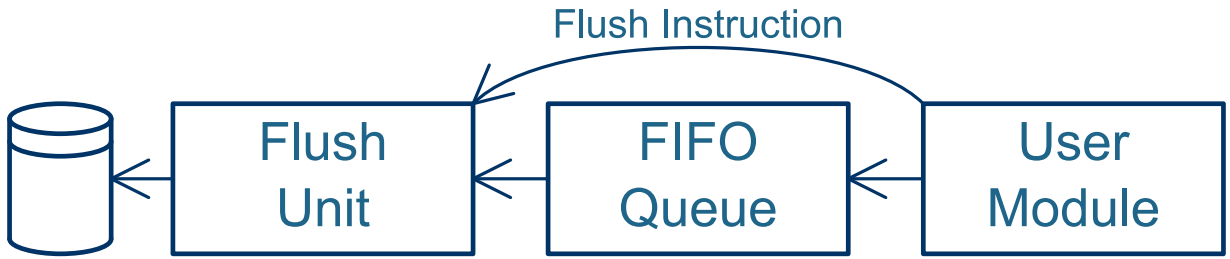

- Writing is continuous, and the user module is only blocked when the queue is full
- Alternatively, the user module is never blocked, and data is lost when the queue is full
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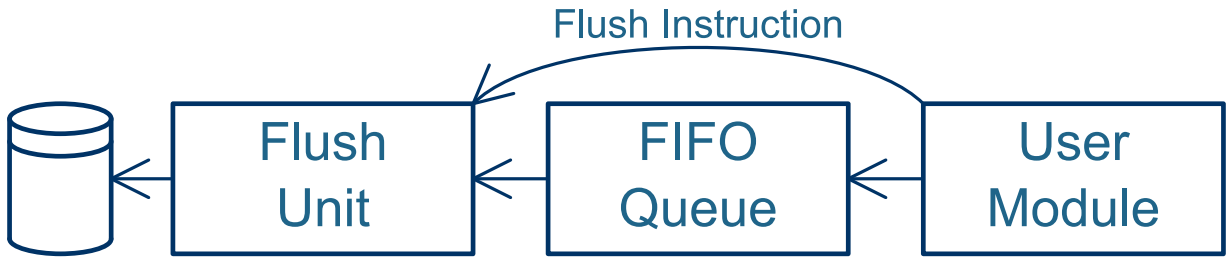

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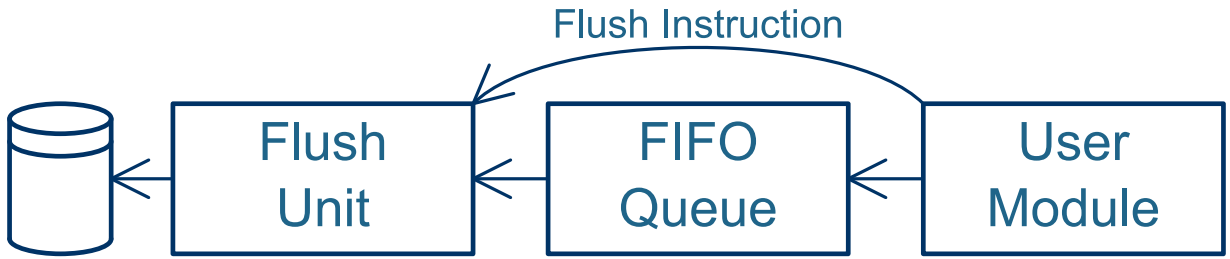

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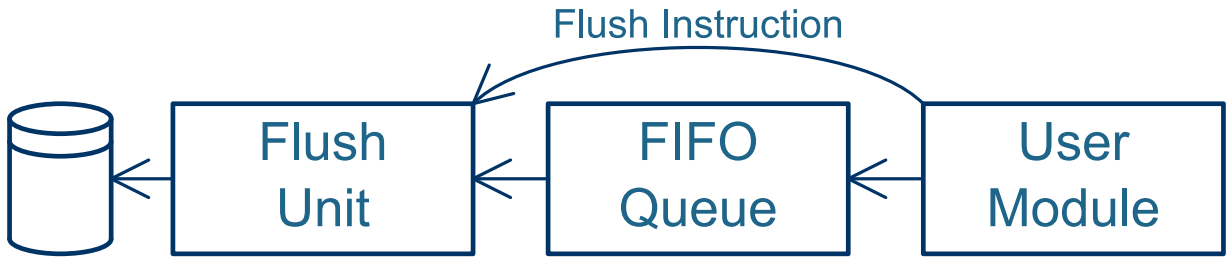

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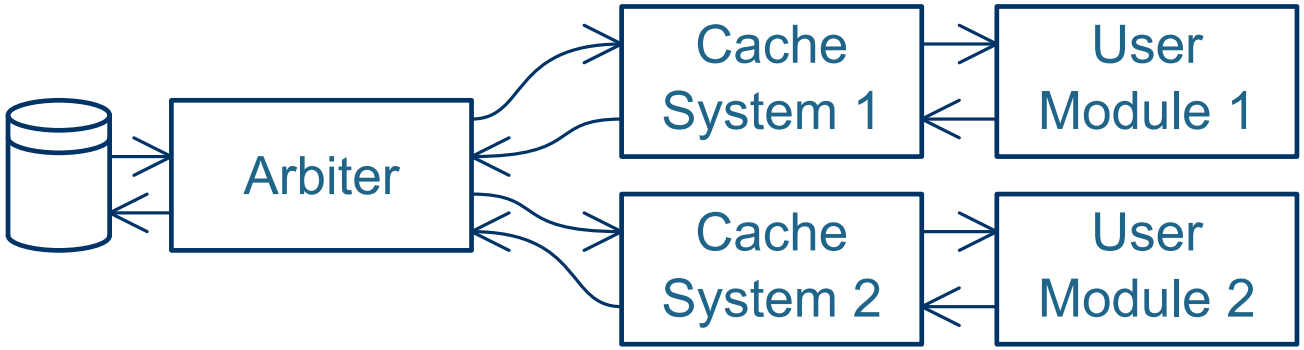

- Two independent cache system can potentially refer to the same place in external storage
- When the one user module reads what the other is writing, the two cache system must remain up to date with each other
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- Many schemes exist to mitigate these and other issues, which are outside the scope of this course

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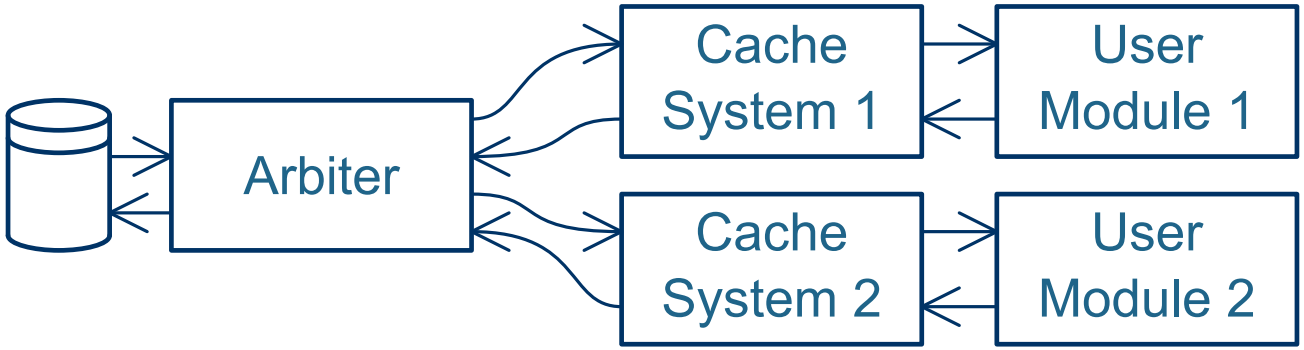

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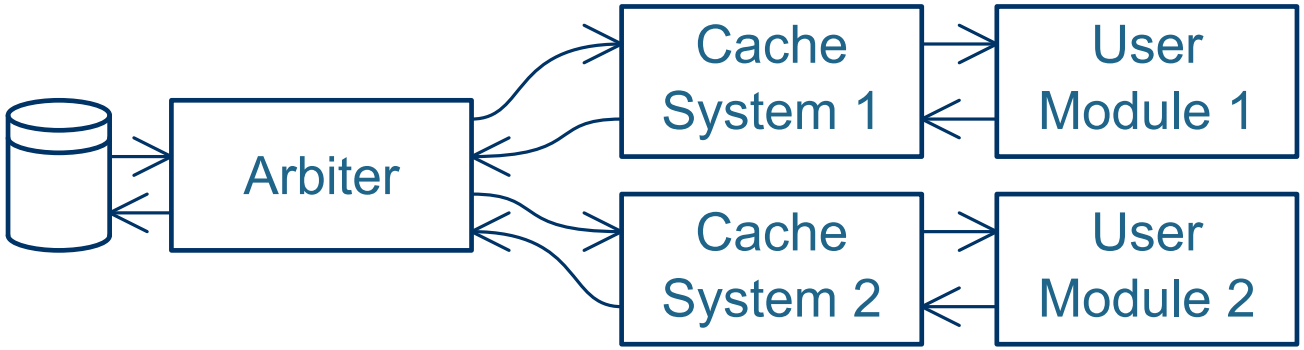

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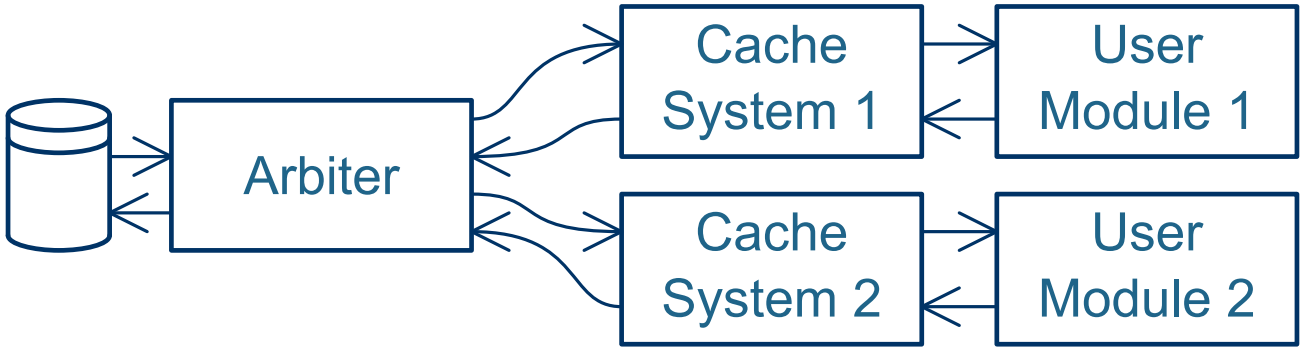

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- Assumes that the destination will handle the data, or
- The application can accept data loss

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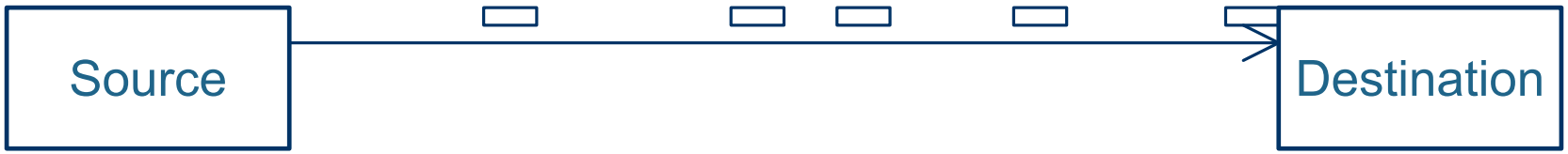

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- The source aims to fill the window with data
- This is used in TCP, among other protocols

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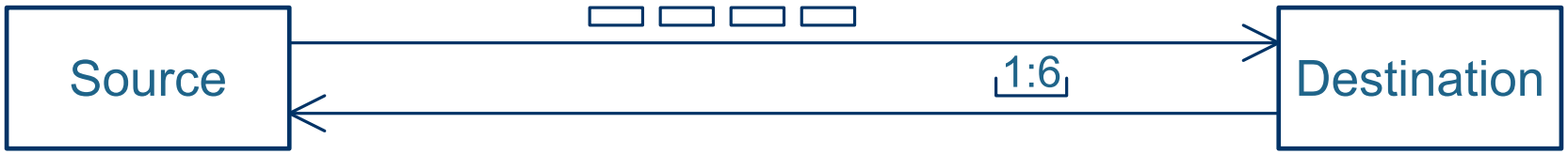

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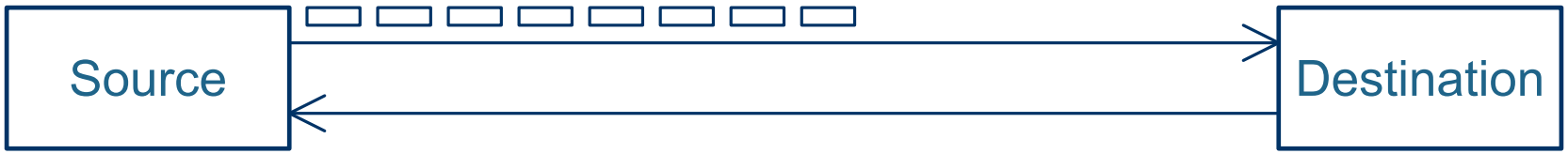

- The source assumes that the destination has a certain space
- The destination acknowledges all incoming packets
- The source sends packets aiming to keep the credit on zero
- Works best when the credit is large enough to keep both directions full at all times

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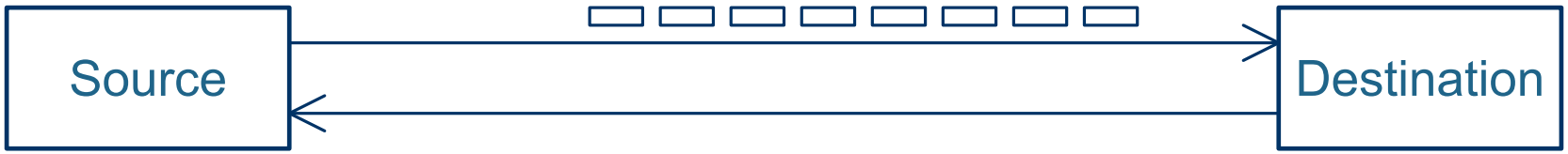

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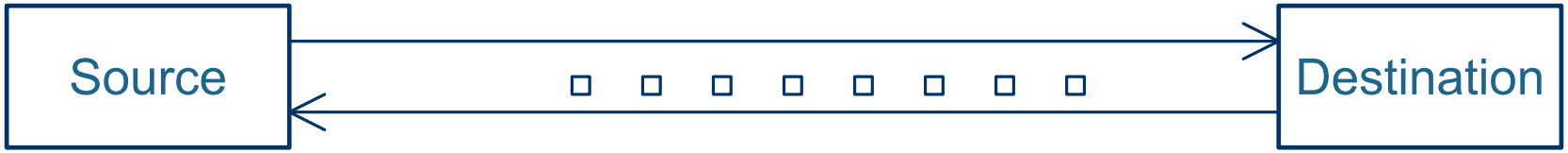

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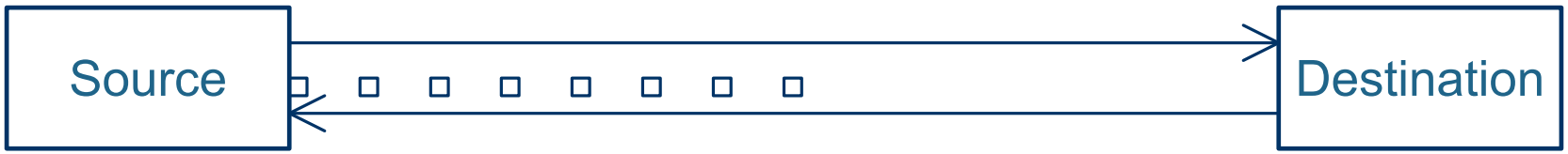

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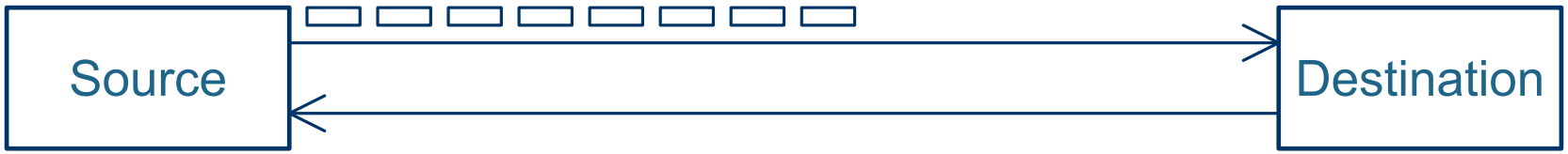

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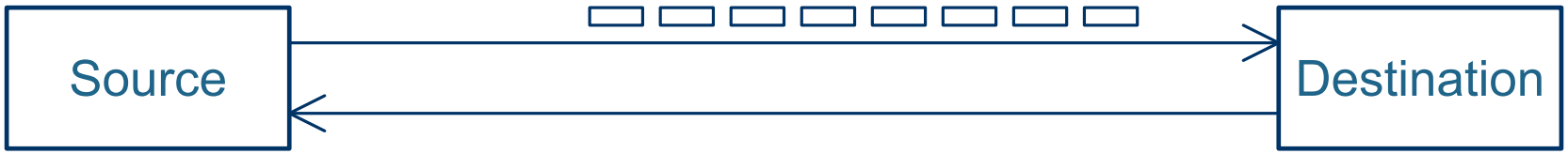

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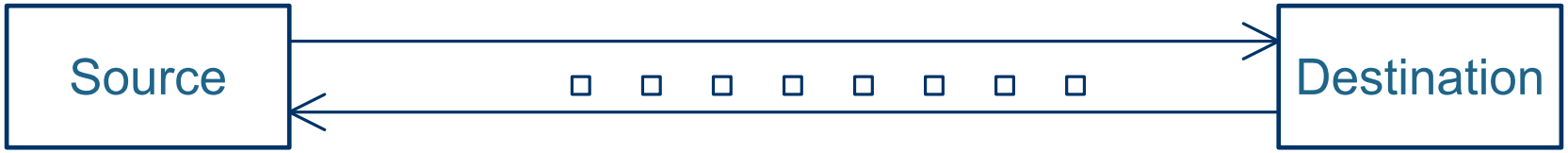

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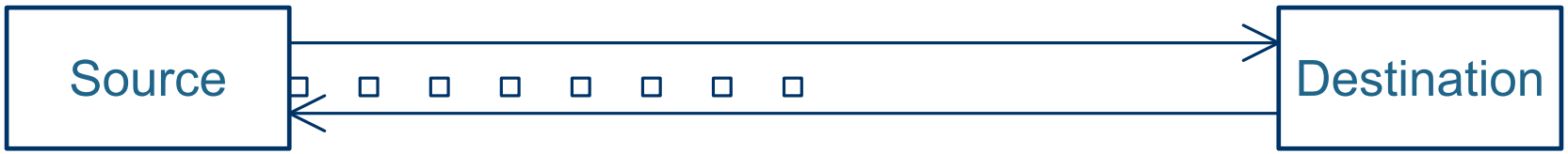

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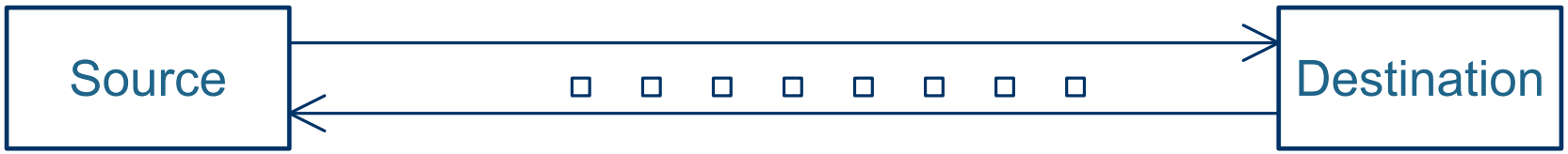

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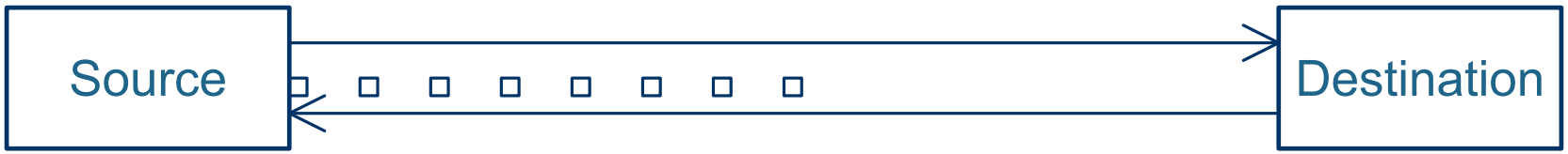

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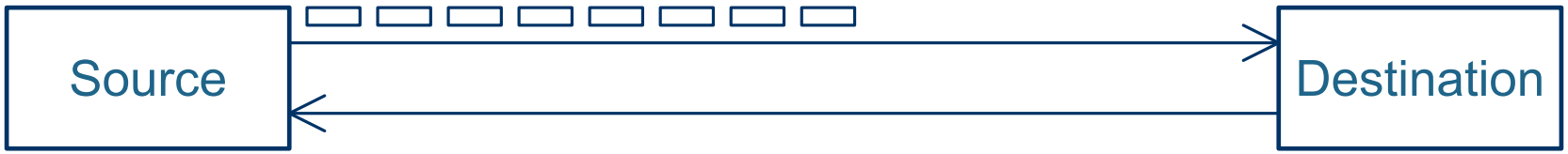

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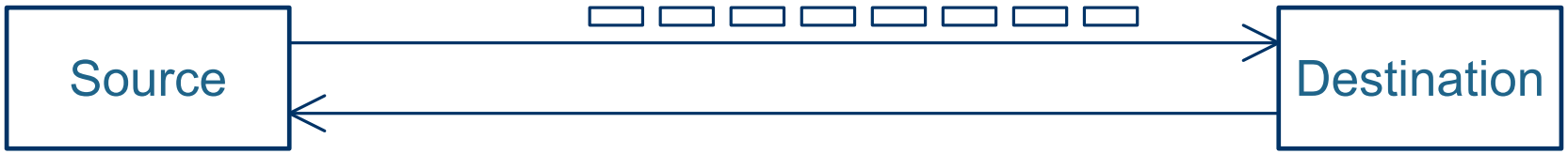

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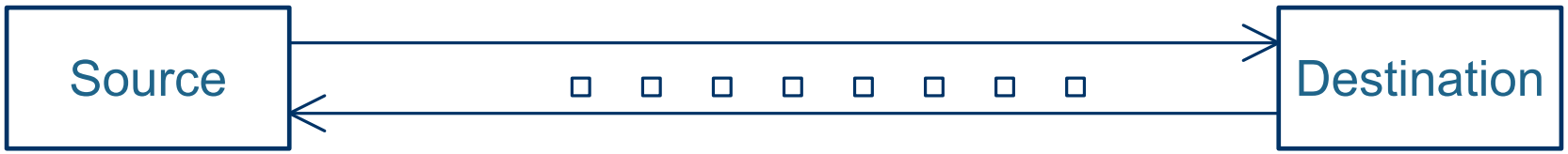

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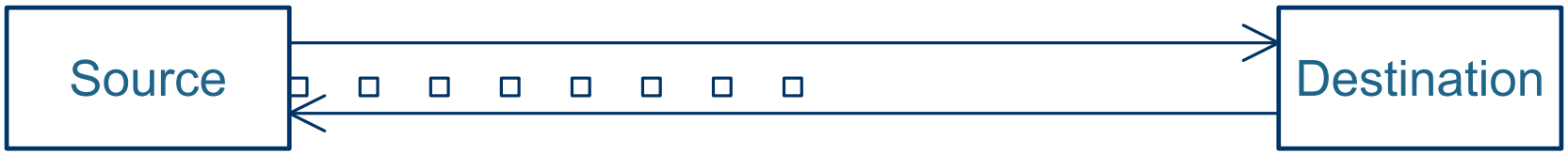

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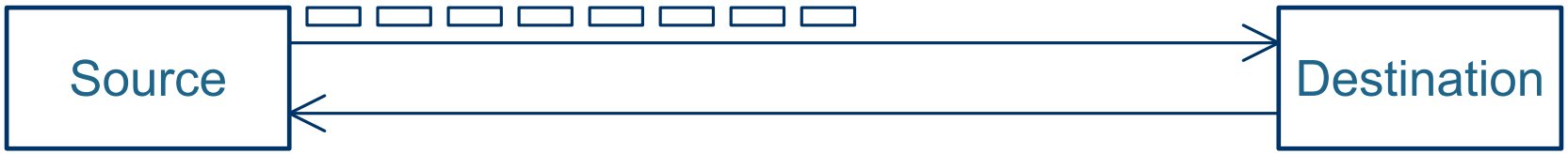

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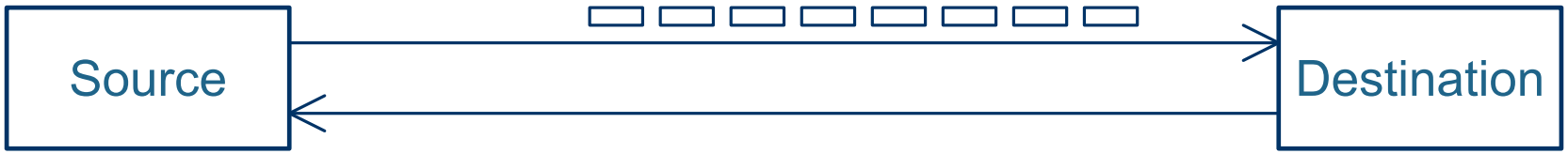

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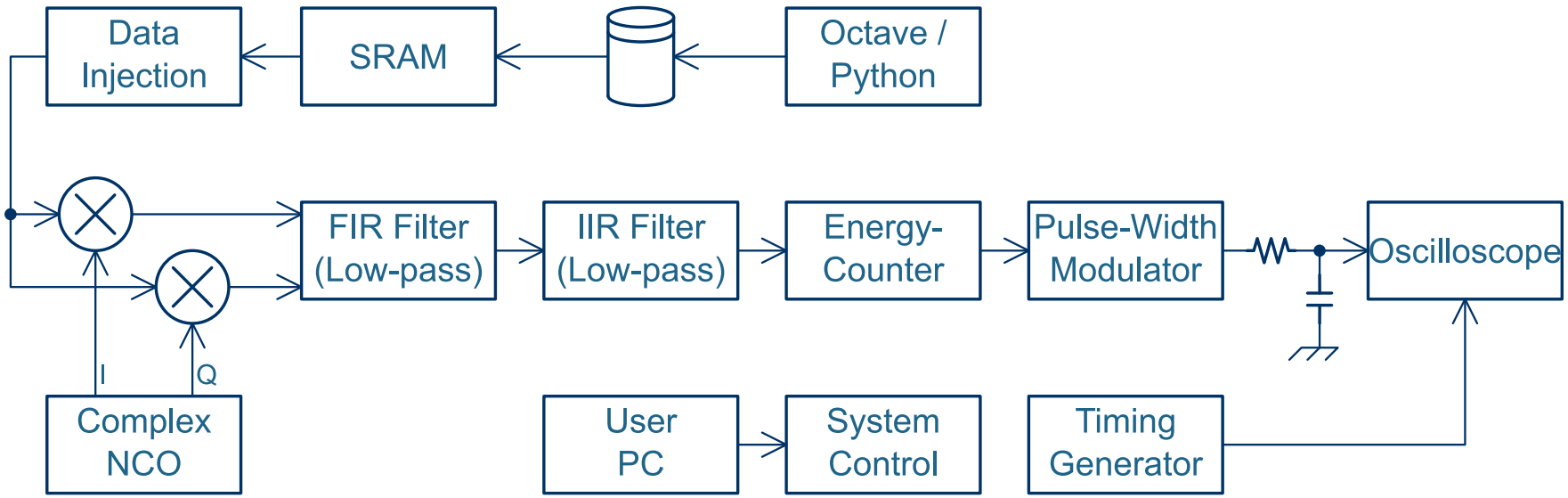
THE RADAR MASTERS COURSE

Practical – NCO and DDC



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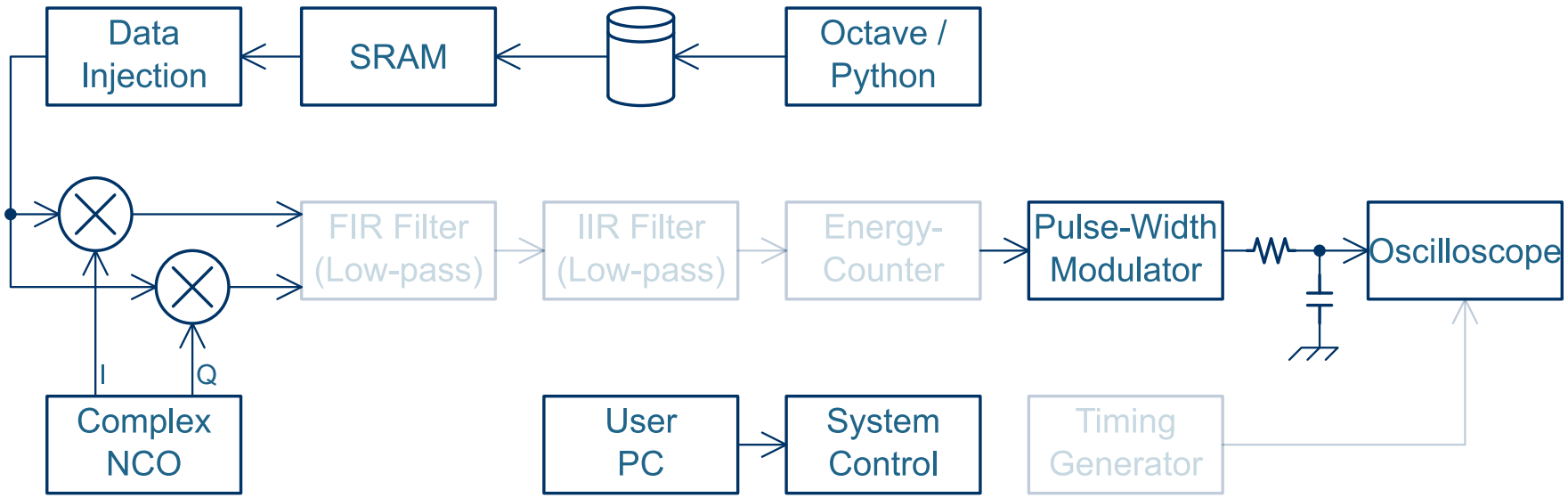

Outline

Advanced Clocking

Clock Domains

Mutual Exclusion and Arbitration

Caching Systems

Flow Control

Practical – NCO and DDC

Numerically-controlled Oscillator

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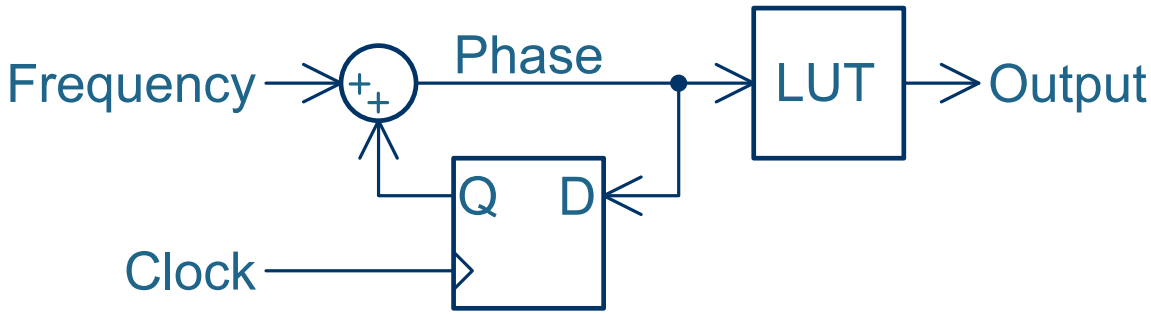
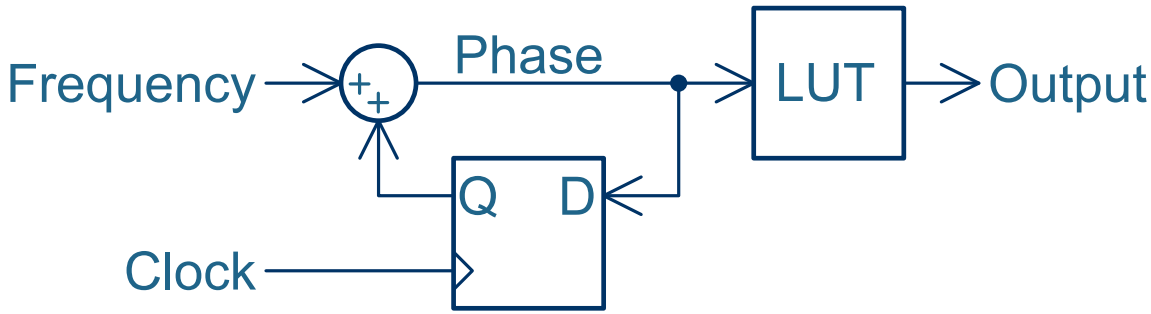
Numerically-controlled Oscillator



- Integrate frequency to obtain phase
- Use on-chip memory blocks as a look-up table to convert phase to the intended waveform
- Use dual-port ROM to obtain sine and cosine from the same LUT

Numerically-controlled Oscillator



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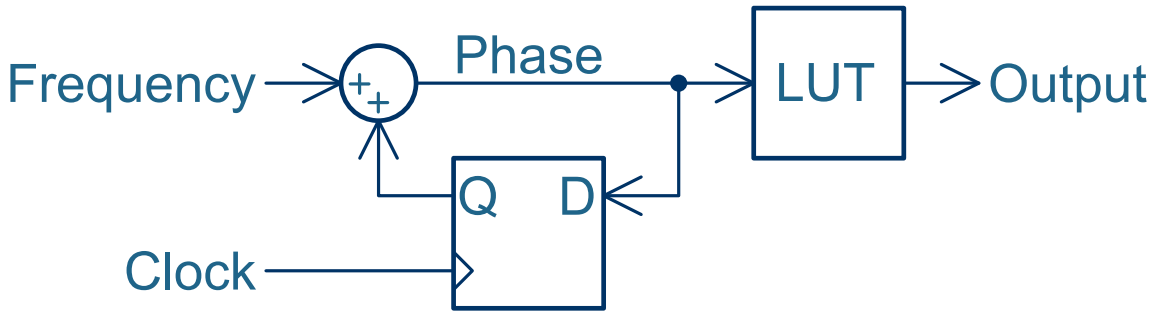

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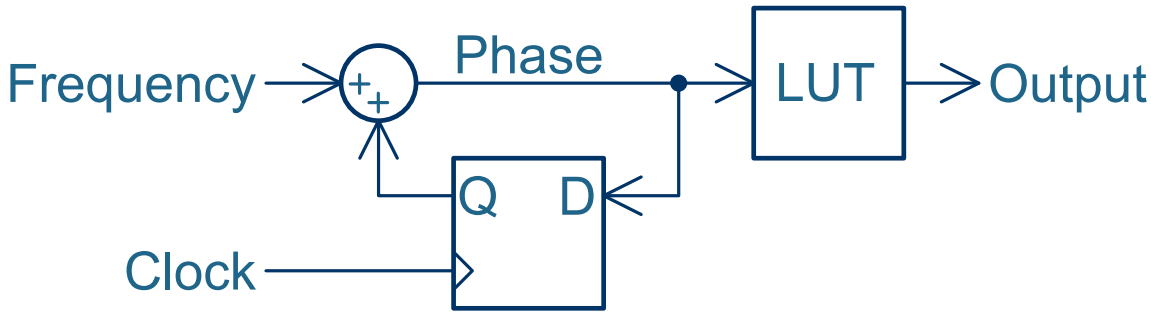

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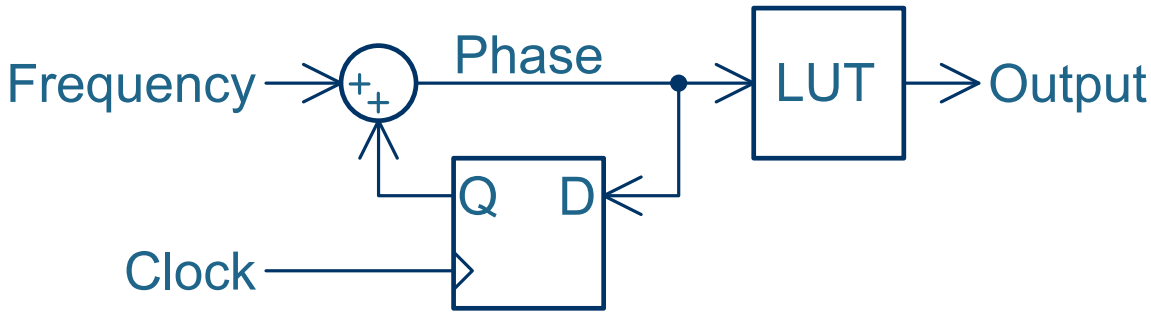

$$f_{out} = f_s \cdot \frac{f_{in}}{2^N}, \quad N = 32, \quad f_s = 100 \text{ MHz}$$

Select References

Stephen Brown and Zvonko Vranesic
Fundamentals of Digital Logic with Verilog Design, 2nd Edition
ISBN 978-0-07-721164-6

Merrill L Skolnik
Introduction to RADAR Systems
ISBN 978-0-07-288138-7

Mark A. Richards and James A. Scheer
Principles of Modern Radar: Basic Principles
ISBN 978-1-89-112152-4

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World of ASIC
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Presented by John-Philip Taylor

Convened by Dr Stephen Paine

Day 4 – 2 May 2022