FPGA Development for Radar, Radio-Astronomy and Communications

THE RADAR MASTERS COURSE

Dept. Electrical Engineering, University of Cape Town
Private Bag, Rondebosch, 7701, South Africa

http://www.rrsg.uct.ac.za

Presented by John-Philip Taylor

Convened by Dr Stephen Paine

Day 4 – 2 May 2022

Outline

Advanced Clocking

Clock Domains

Mutual Exclusion and Arbitration

Caching Systems

Flow Control

Practical – NCO and DDC

Numerically-controlled Oscillator

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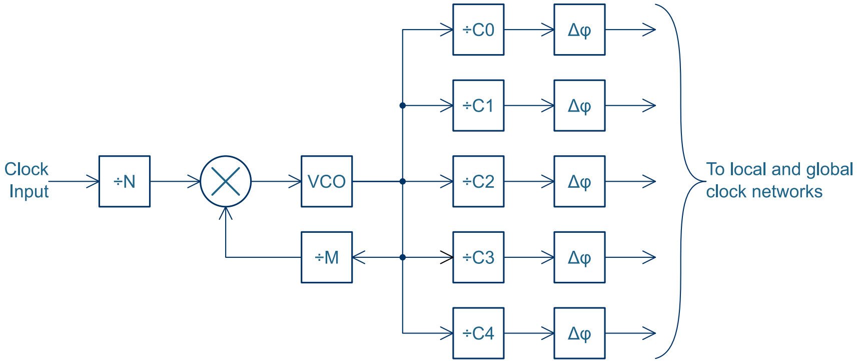
Numerically-controlled Oscillator

Phase-locked Loop



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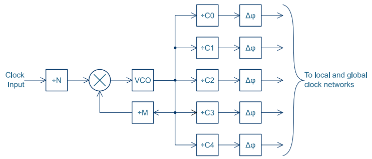

- Useful for generating a range of related clocks
- Output clock rising and falling edges can be set, independently, to a resolution equal to the VCO period, which is typically about 1 ns $\pm$ 500 ps
- All output clocks can be considered to be in the same clock domain
- Noise sensitive applications should avoid PLLs due to high phase noise

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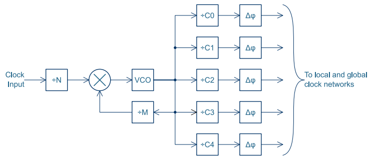

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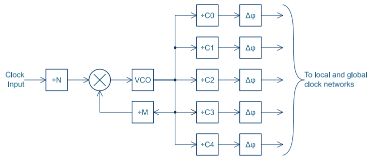

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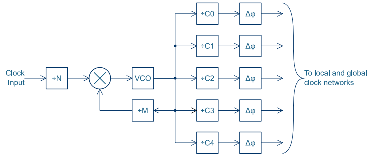

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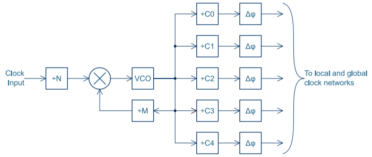

- **Direct**: No compensation, which results in better jitter performance
- **Normal**: The clock at the register is phase-aligned with the input clock pin
- **Source Synchronous**: The PLL ensures that the data delay from pin to register and the apparent clock delay from pin to register is the same
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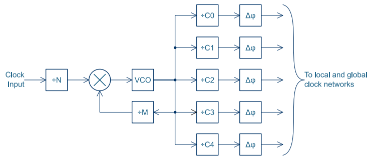

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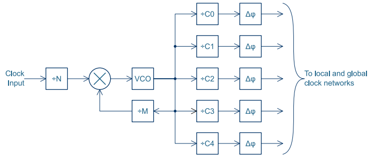

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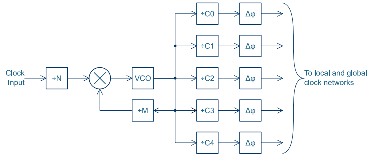

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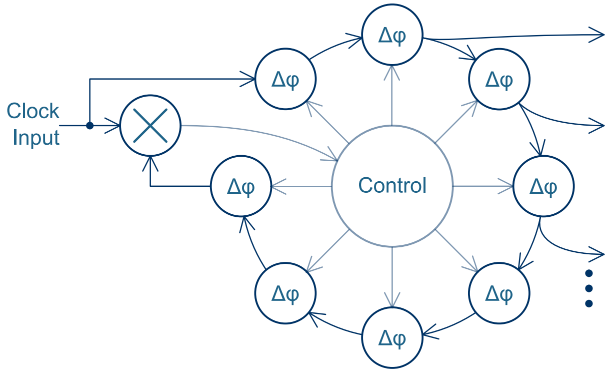

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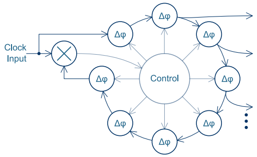

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- All output clocks can be considered to be in the same clock domain as the input clock

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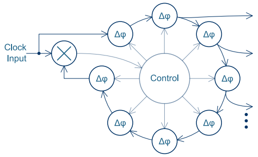

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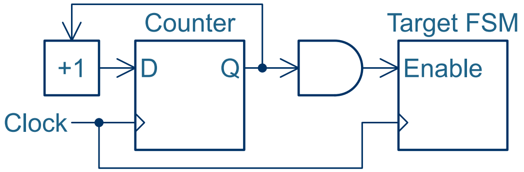

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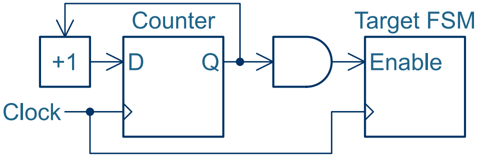

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- Cannot be used for clocking external devices
- The multi-cycle timing requirements must be manually specified

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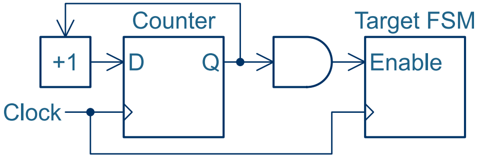

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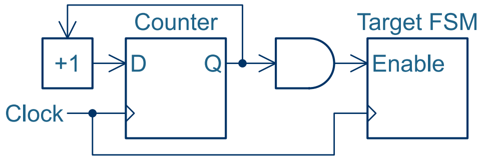

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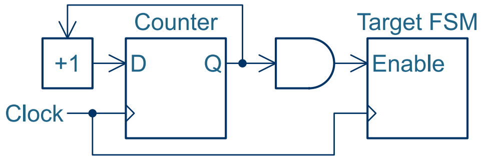

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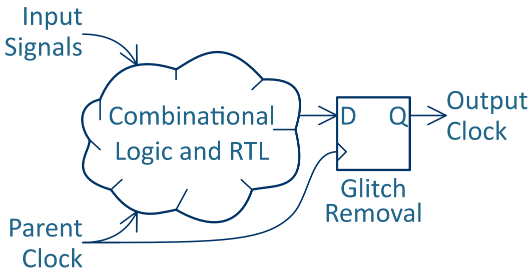

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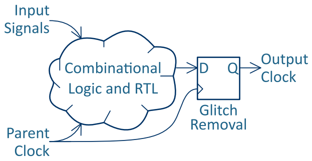

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- Often necessitates complex clock-domain crossing schemes to the general system clock
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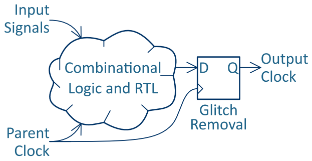

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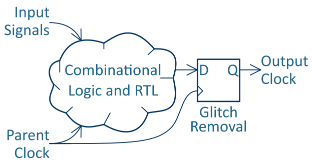

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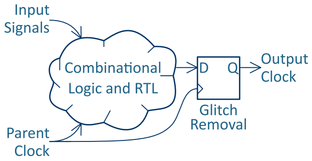

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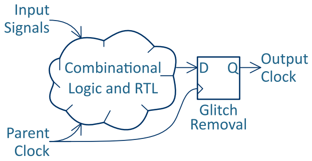

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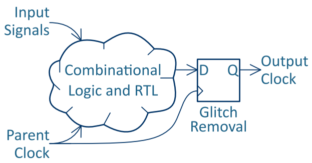

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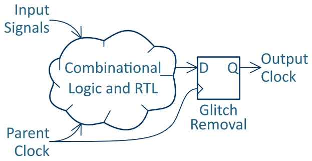

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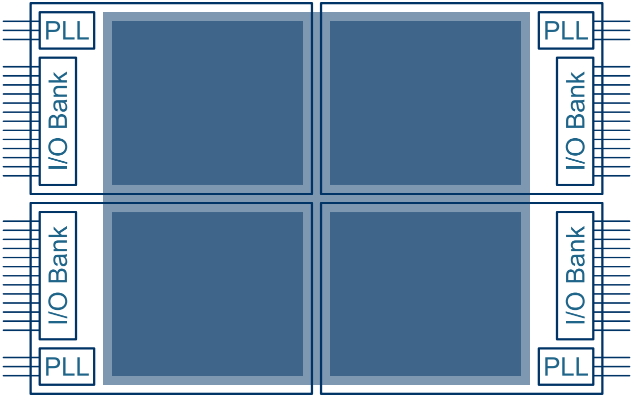

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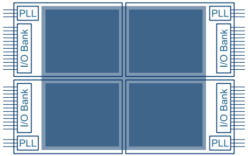

- FPGAs are generally organised into regions, each with its own PLL and I/O bank
- The local clock network is more efficient (and faster) than the global network
- When laying out the PCB, keep fast I/O in the same region as their clock

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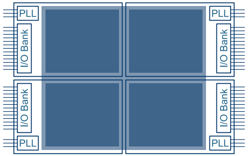

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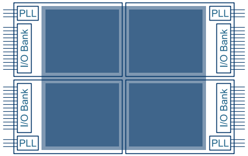

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Outline

Common Mistake

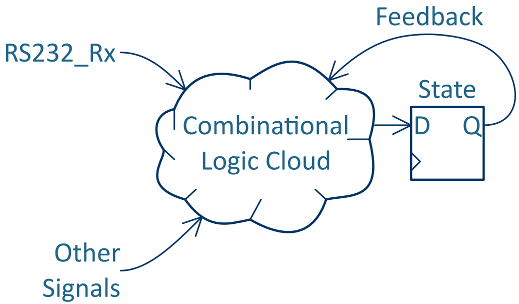
```
module RS232(
  input   ipClk, ipReset,
  input   ipRS232_Rx, // Asynchronous external signal
  output  [7:0]opData
);

... // Definitions, state machine boilerplate, etc.

  Idle: begin
    if(!ipRS232_Rx) begin
      State <= Receiving;
    end
  end

  Receiving: begin
...
```

Common Mistake



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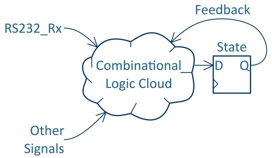
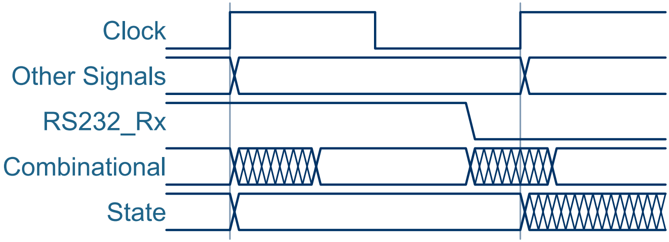
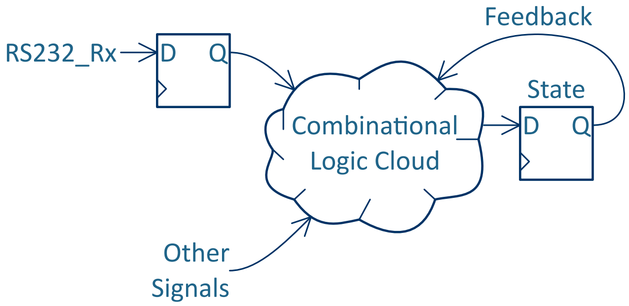




The Solution



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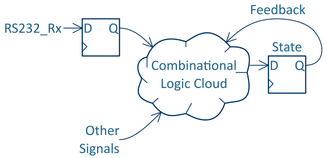
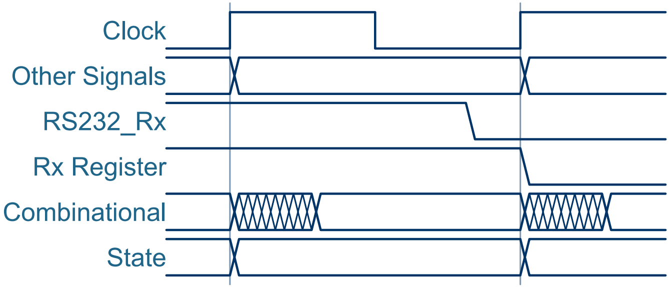
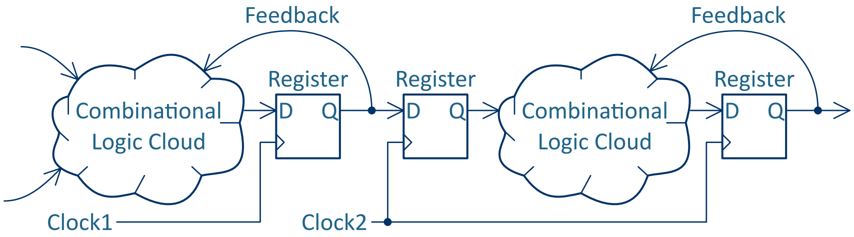




Register Chain



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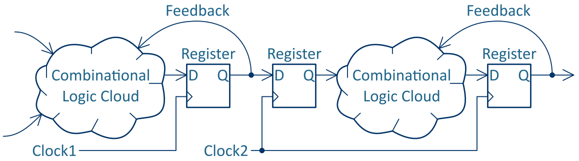

- Essential for crossing asynchronous external signals
- Only useful for crossing one bit at a time (unless the system is tolerant to temporary errors)
- Often used to cross hand-shaking signals
- Works in both directions (fast to slow / slow to fast)

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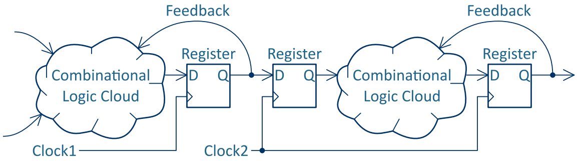

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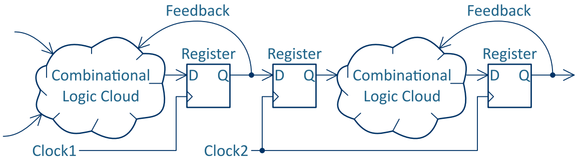

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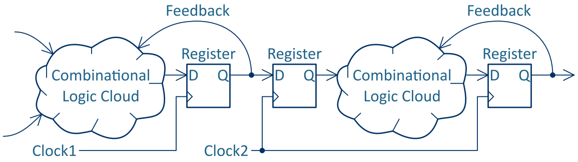

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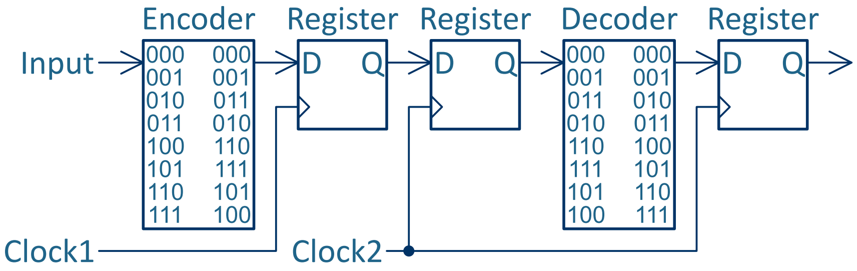
Encoder
Register
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Decoder
Register
Input
000 000
001 001
010 011
011 010
100 110
101 111
110 101
111 100
D Q
D Q
000 000
001 001
011 010
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110 100
111 101
101 110
100 111
D Q
Clock1
Clock2

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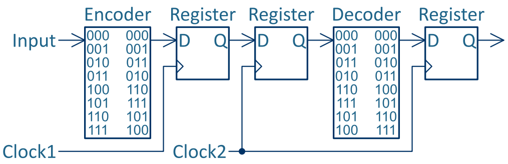

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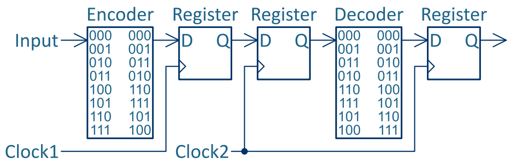

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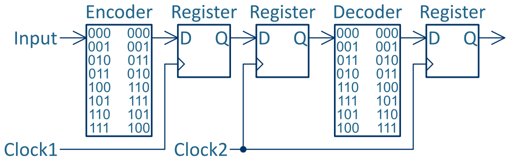

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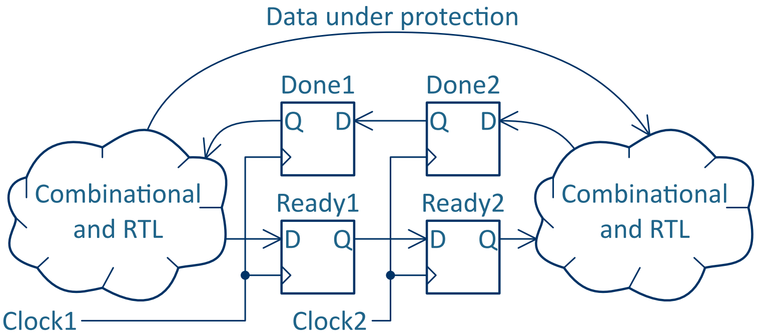

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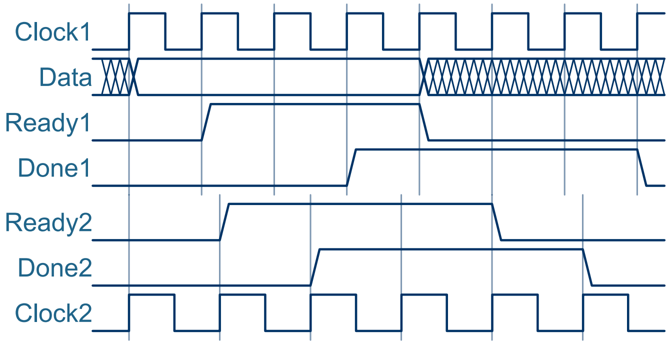

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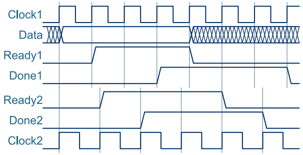

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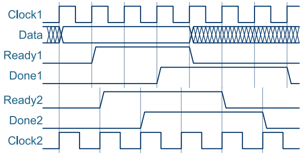

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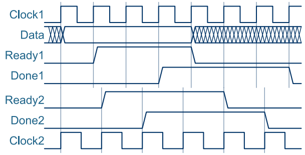

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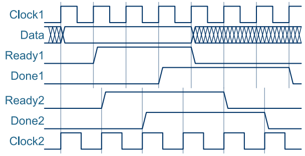

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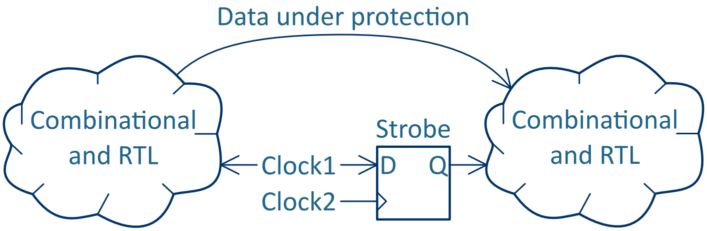
- Not time-efficient: need to wait for the entire transaction sequence to finish before starting the next one
- Use only for data that does not need to be crossed often
- Works in both directions (fast to slow / slow to fast)

Strobe-based



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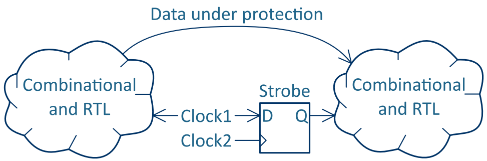

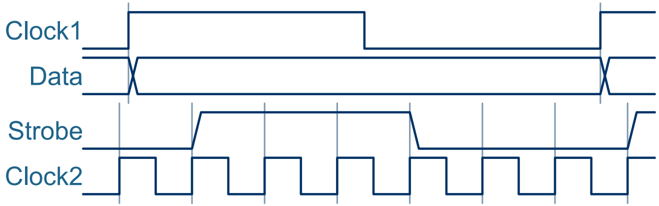

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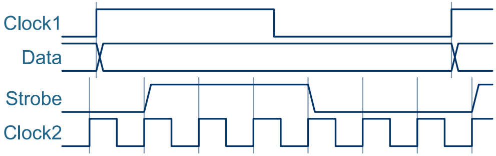

- The data is valid for as long as the strobe is high
- As fast as the source clock
- The strobe edges can be used to perform flow-control
- Only works when the destination clock is much faster than the source clock
- Note that the source “clock” can be a strobe signal generated by the source state machine...

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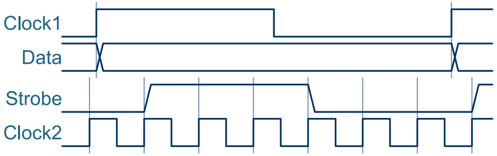

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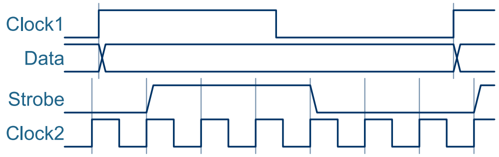

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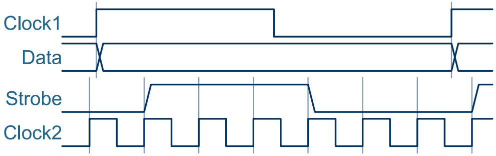

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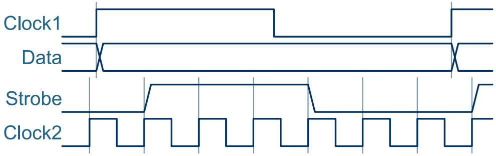

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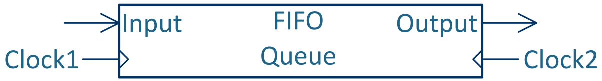

- Flow-control signals are crossed separately
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- Mixed-width RAM can be used to keep the data-rate constant across different frequencies (especially useful in DDR-based external memory)

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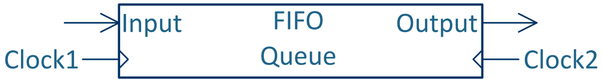

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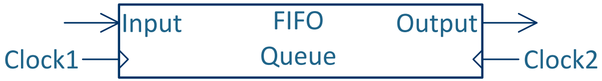

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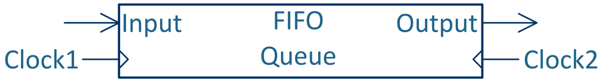

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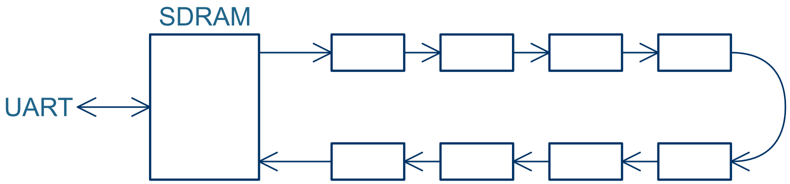
```
set_clock_groups -asynchronous \
  -group [get_clocks ADC_Clk]         \
  -group [get_clocks Clk1]            \
  -group [get_clocks Clk2]            \
  -group [get_clocks {SRAM_CLK *altpll_0*}]
```

Outline

Sharing Resources



- Often many modules need access to the same resource, but only one module can interface with it at a time
- Examples include:
  - External memory (SDRAM, SD-card, etc.)
  - I^2C bus
  - etc.

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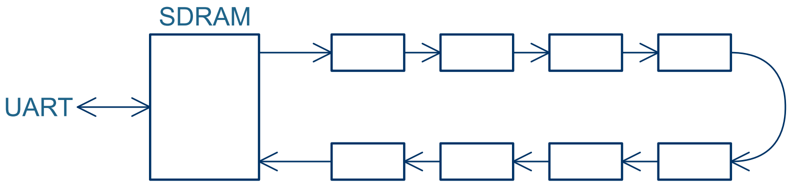

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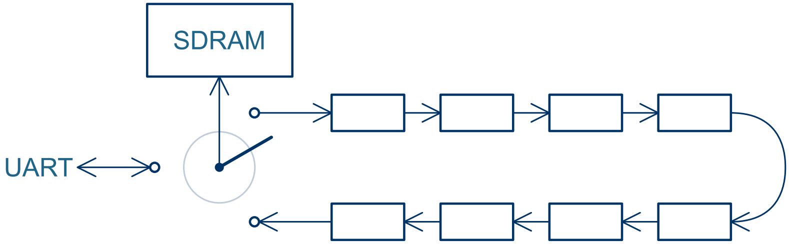

- Uses “Request” and “Grant” control lines
- The module would raise a request and then wait until it has been granted access before using the resource
- All the request lines go to a central control module that administers the granting of the resource

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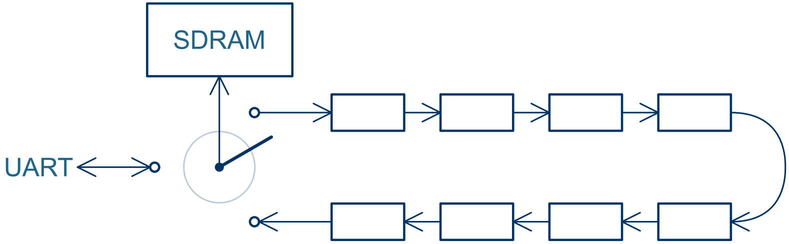

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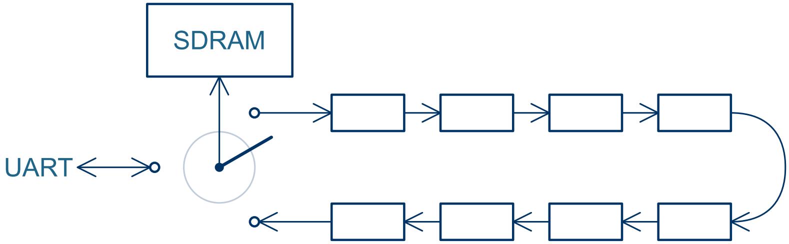

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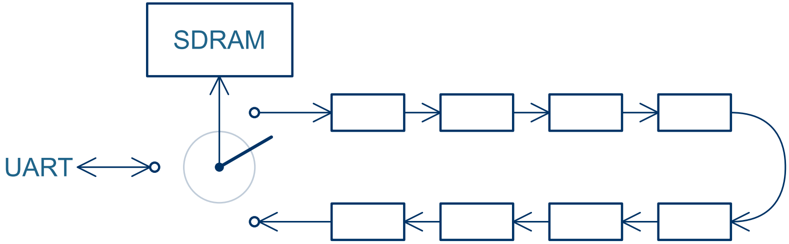

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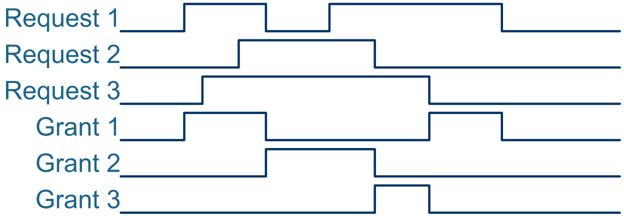

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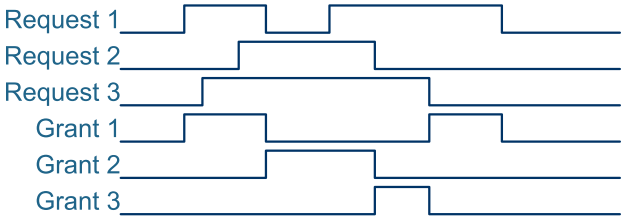

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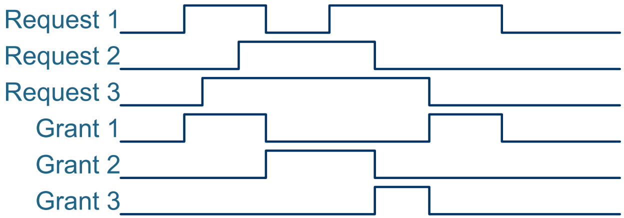

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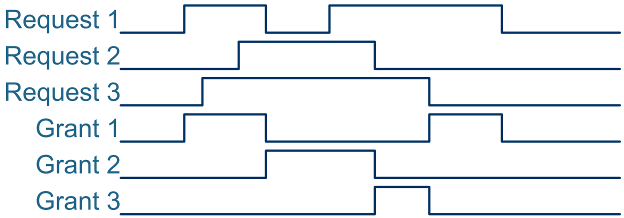

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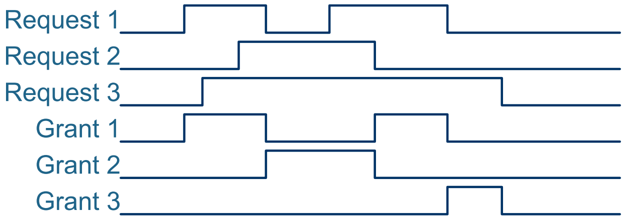

- When more that one module requests access, the one with higher priority always receives the grant
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THE RADAR MASTERS COURSE

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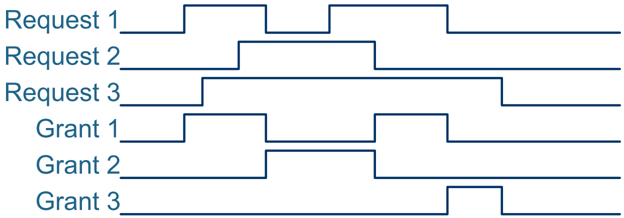

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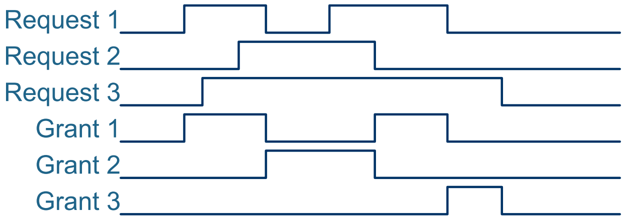

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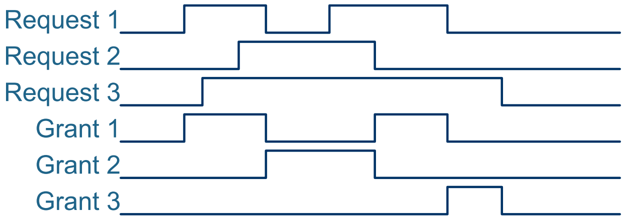

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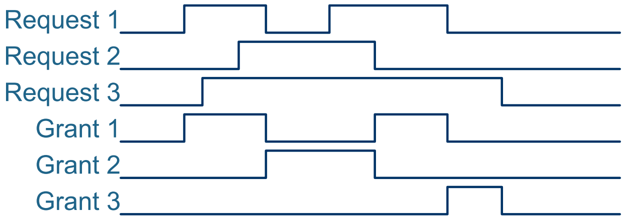

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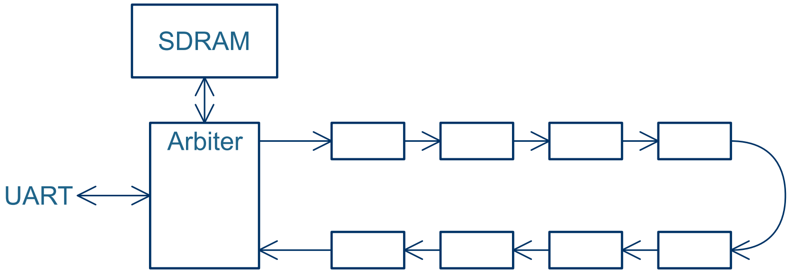

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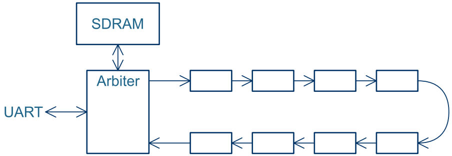

- The arbiter makes it look as if the resource has multiple independent interfaces. There are no control lines other than the interface itself.
- Often implemented by means of an embedded mutual exclusion unit (round-robin or priority based)
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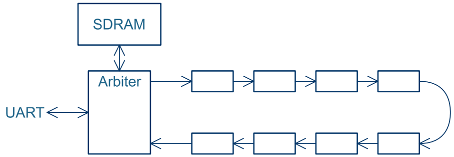

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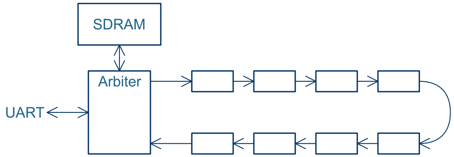

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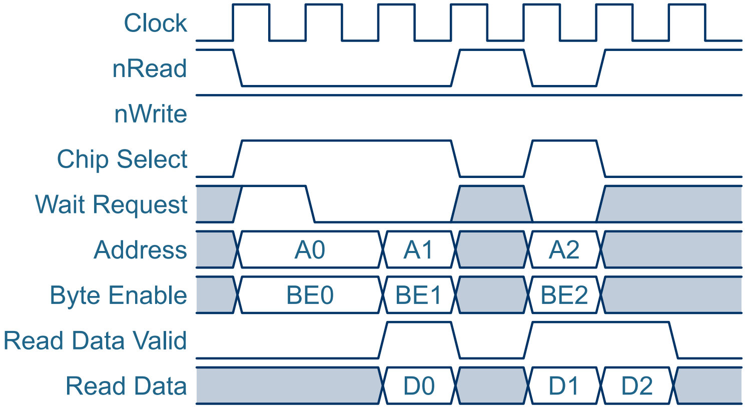


Coffee Break...

Outline

Advanced Clocking

Clock Domains

Mutual Exclusion and Arbitration

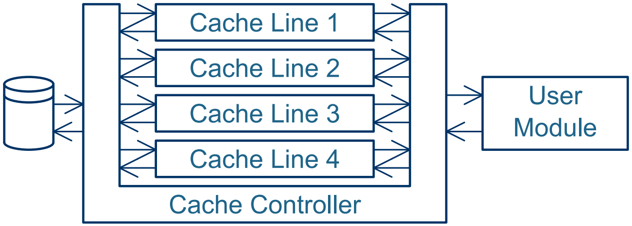
Caching Systems

Flow Control

Practical – NCO and DDC

Numerically-controlled Oscillator

General Cache



- Lines are typically one page in size (4 kiB in modern PCs, typically smaller on embedded systems)
- The controller does address translation between the external and cache line addresses
- Read is on-demand, flushing the least recently used line and loading the content into it
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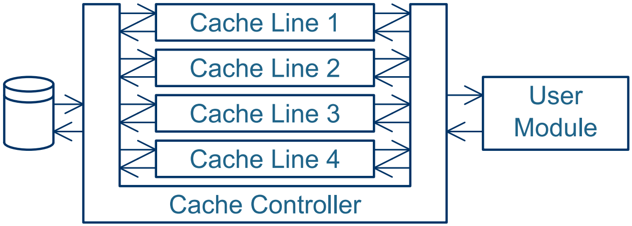

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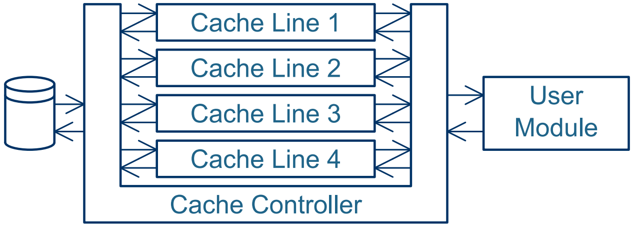

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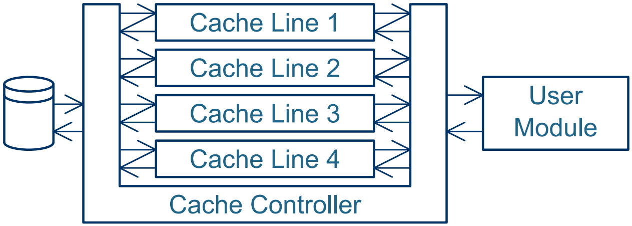

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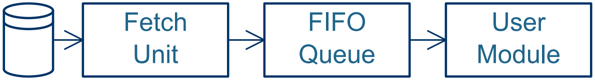

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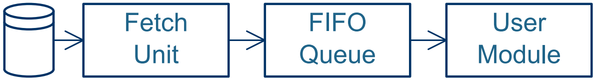

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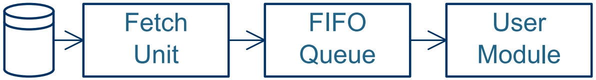

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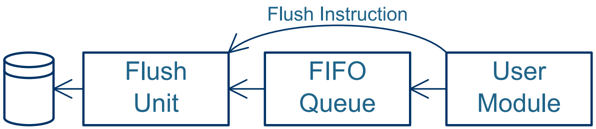

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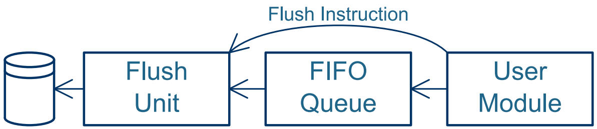

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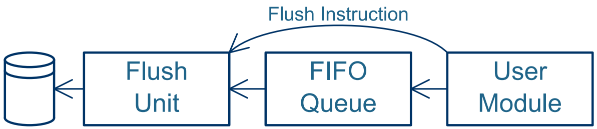

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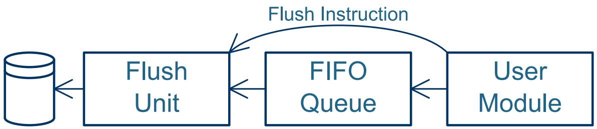

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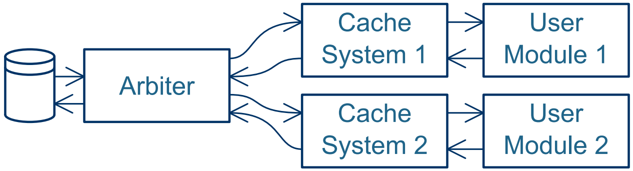

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- When the one user module reads what the other is writing, the two cache system must remain up to date with each other
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- Many schemes exist to mitigate these and other issues, which are outside the scope of this course

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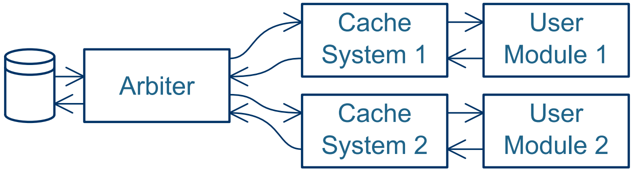

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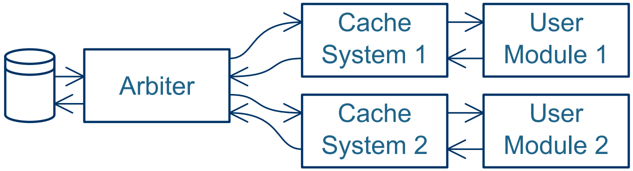

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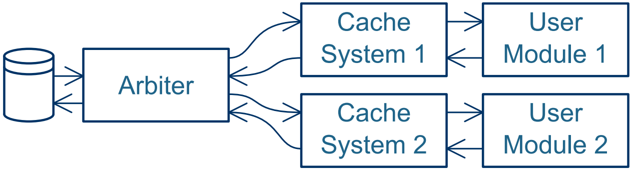
- When the two user modules write to different places in the same page, a flush must not overwrite the other's data
- Many schemes exist to mitigate these and other issues, which are outside the scope of this course

Cache Coherence



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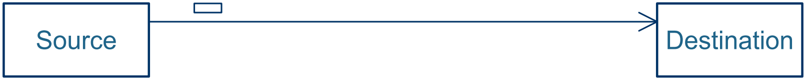
Outline

Fire and Forget



- No feedback from the destination to the source
- Assumes that the destination will handle the data, or
- The application can accept data loss

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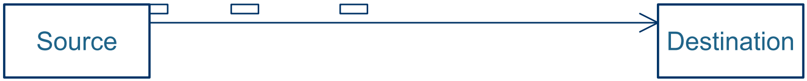

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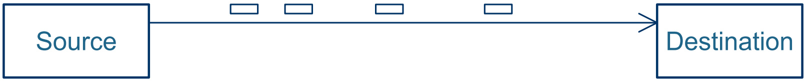

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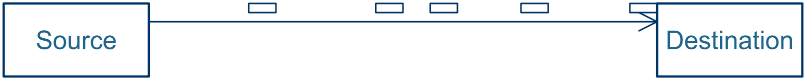

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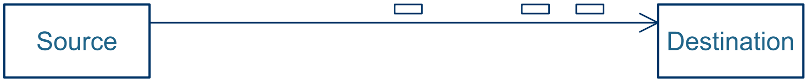

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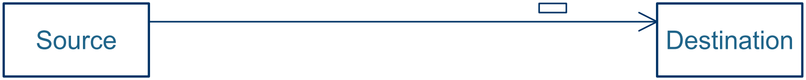

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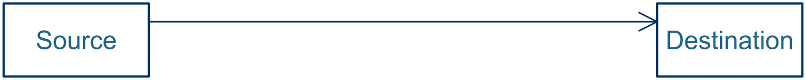

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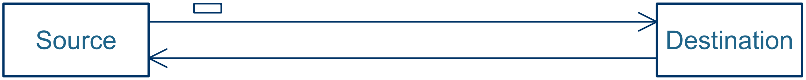
Command-Response



- The source sends one packet at a time
- And waits for the response from the destination

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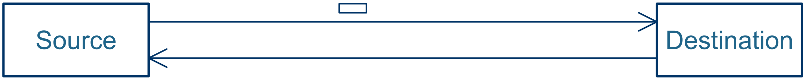

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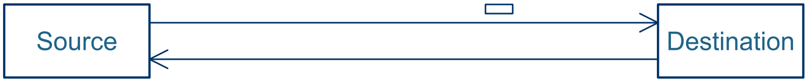

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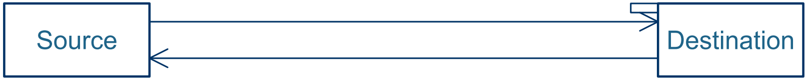

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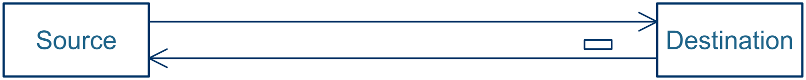

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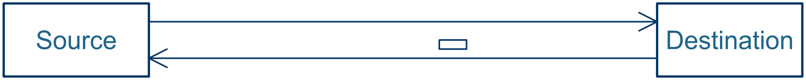

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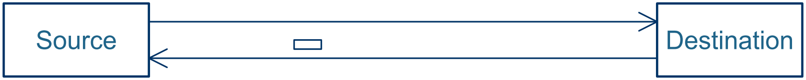

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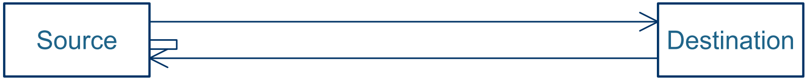

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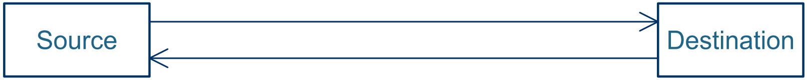

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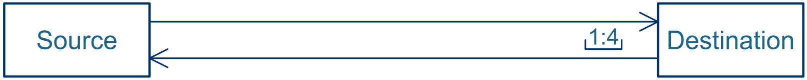

- The destination advertises a window
- The source aims to fill the window with data
- This is used in TCP, among other protocols

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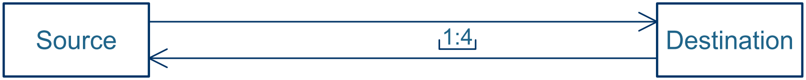

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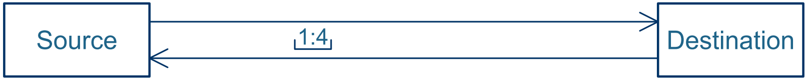

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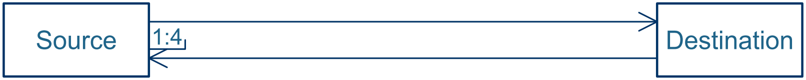

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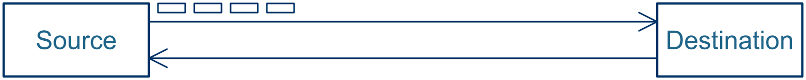

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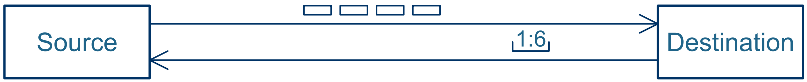

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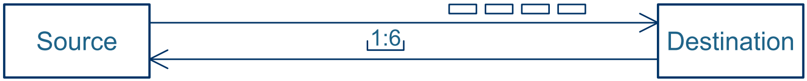

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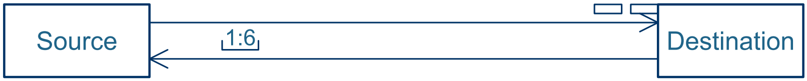

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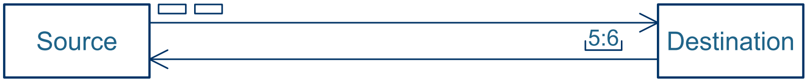

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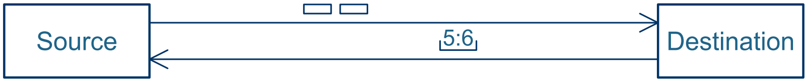

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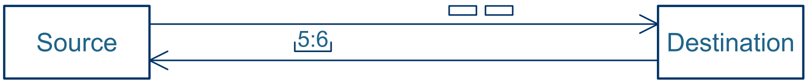

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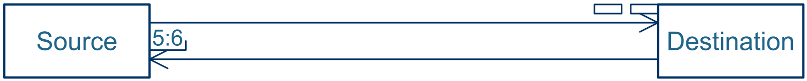

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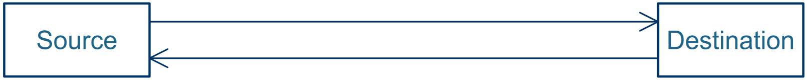

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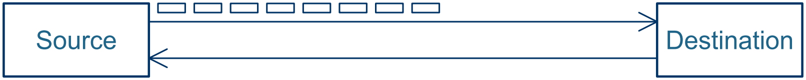

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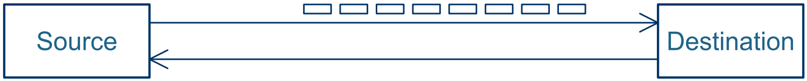

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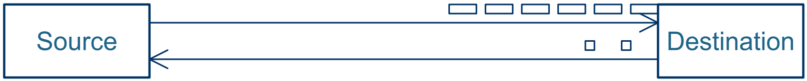

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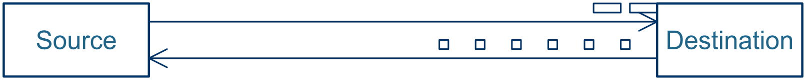

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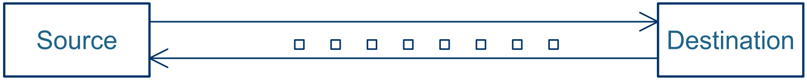

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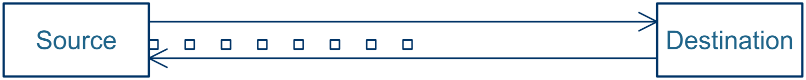

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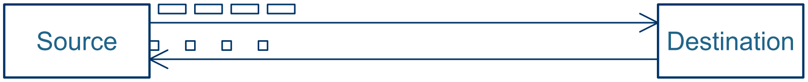

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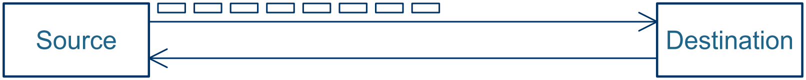

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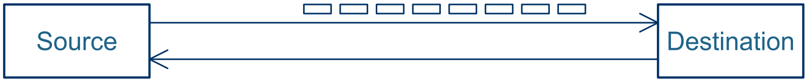

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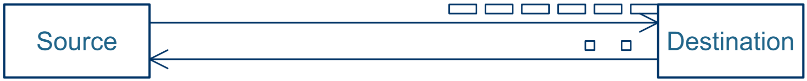

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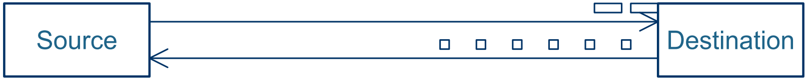

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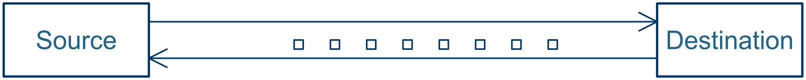

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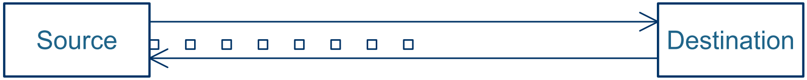

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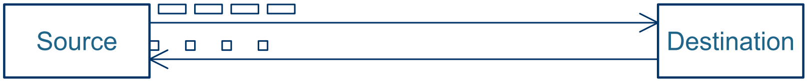

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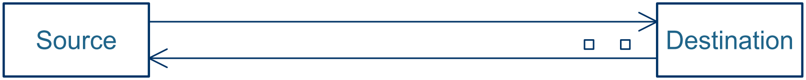

- Instead of the source starting with credit, an alternative algorithm lets the destination provide credit to the source
- This is used in PCIe, among other protocols

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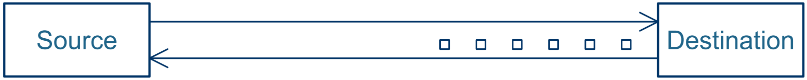

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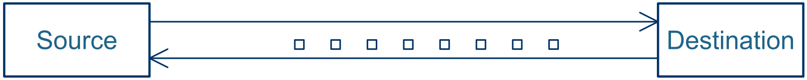

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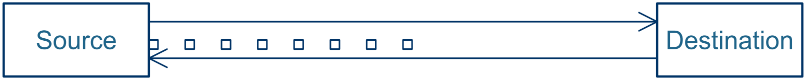

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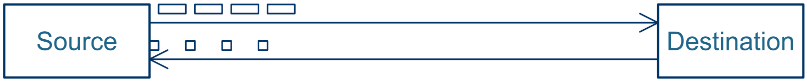

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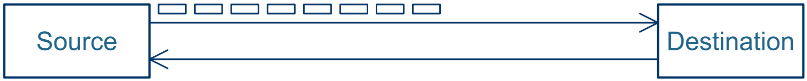

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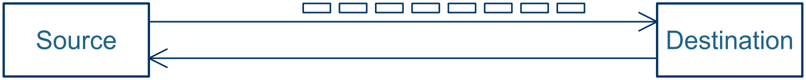

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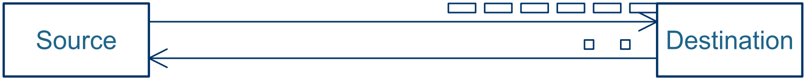

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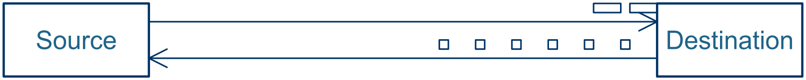

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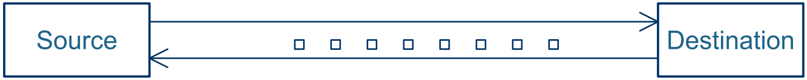

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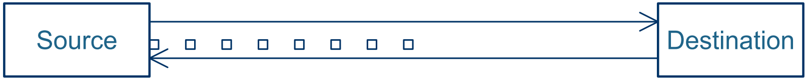

- Instead of the source starting with credit, an alternative algorithm lets the destination provide credit to the source
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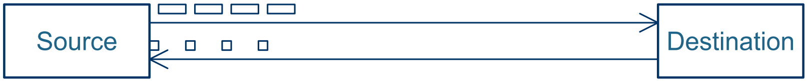

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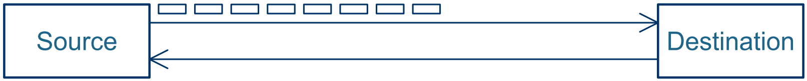

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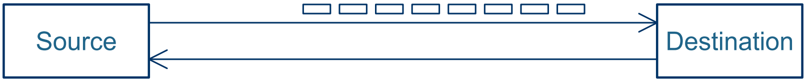

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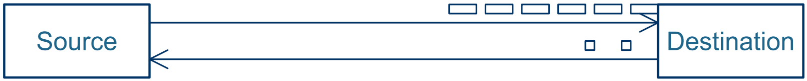

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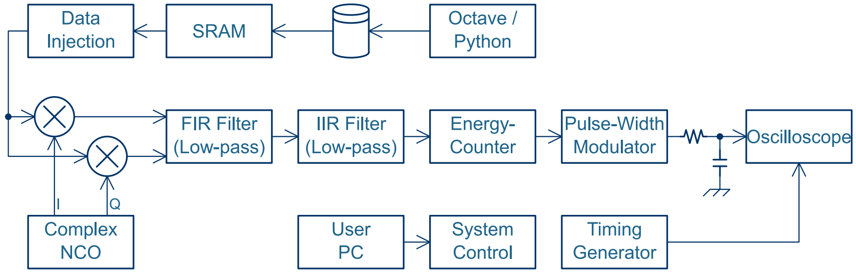
Outline

Practical – NCO and DDC



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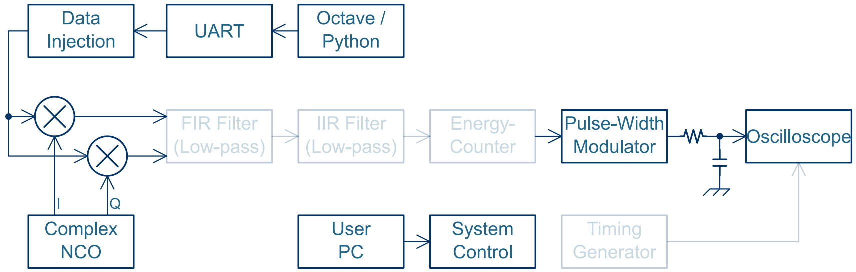

Outline

Advanced Clocking

Clock Domains

Mutual Exclusion and Arbitration

Caching Systems

Flow Control

Practical – NCO and DDC

Numerically-controlled Oscillator

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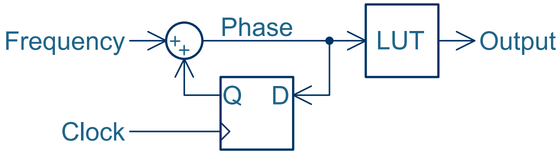
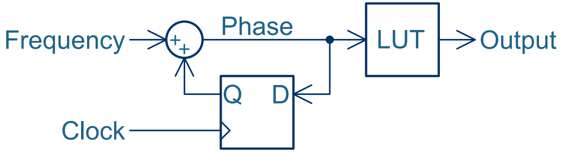


- Integrate frequency to obtain phase
- Use on-chip memory blocks as a look-up table to convert phase to the intended waveform
- Use dual-port ROM to obtain sine and cosine from the same LUT
- Higher resolution can be obtained with a CORDIC-based sine-cosine module

Numerically-controlled Oscillator



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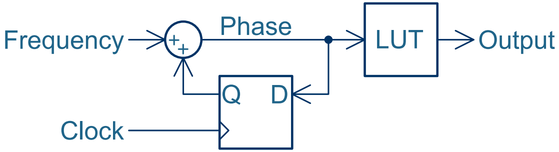

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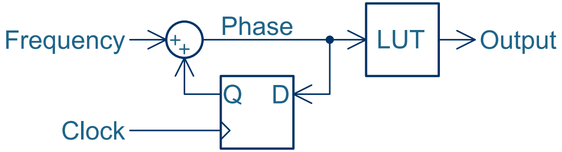

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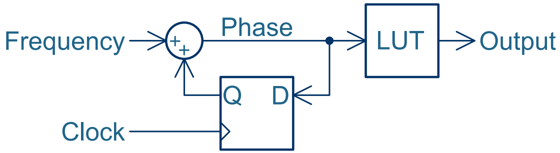

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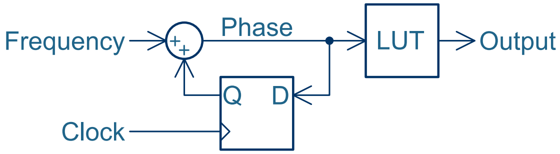

$$f_{out} = f_s \cdot \frac{f_{in}}{2^N}, \quad N = 32, \quad f_s = 50 \text{ MHz}$$

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Presented by John-Philip Taylor

Convened by Dr Stephen Paine

Day 4 – 2 May 2022