MAX2871

23.5MHz to 6000MHz Fractional/ Integer-N Synthesizer/VCO

General Description

The MAX2871 is an ultra-wideband phase-locked loop (PLL) with integrated voltage control oscillators (VCOs) capable of operating in both integer-N and fractional-N modes. When combined with an external reference oscillator and loop filter, the MAX2871 is a high-performance frequency synthesizer capable of synthesizing frequencies from 23.5MHz to 6.0GHz while maintaining superior phase noise and spurious performance.

The ultra-wide frequency range is achieved with the help of multiple integrated VCOs covering 3000MHz to 6000MHz, and output dividers ranging from 1 to 128. The device also provides dual differential output drivers, which can be independently programmed to deliver -1dBm to +8dBm output power. Both outputs can be muted by either software or hardware control.

The MAX2871 is controlled by a 3-wire serial interface and is compatible with 1.8V control logic. The device is available in a lead-free, RoHS-compliant, 5mm x 5mm, 32-pin TQFN package, and operates over an extended -40°C to +85°C temperature range.

The MAX2871 has an improved feature set and better overall phase noise and is fully pin- and software- compatible with the MAX2870.

Applications

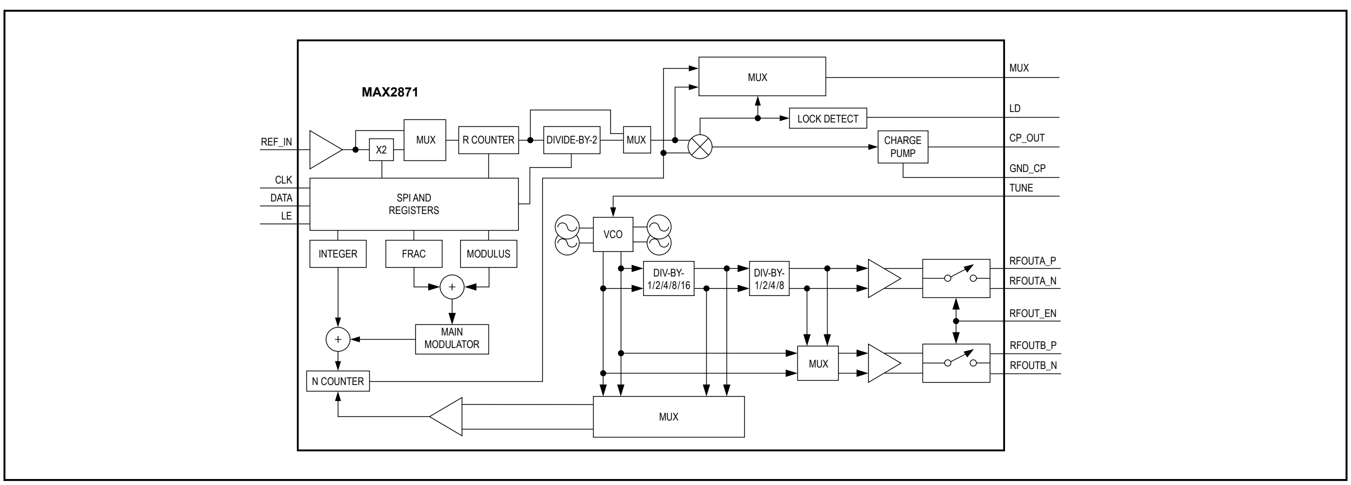
- Wireless Infrastructure
- Test and Measurement
- Clock Generation
- Microwave Radios

Benefits and Features

- Output Binary Buffers/Dividers Enable Extended Frequency Range
  - Divider Ratios of 1/2/4/8/16/32/64/128
  - 23.5MHz to 6000MHz
- High-Performance Phase Frequency Detector (PFD) and Reference Frequency Reduces Spectral Noise
  - PFD Up to 140MHz
  - Reference Frequency Up to 210MHz
- Low Normalized Inband Phase Noise of -230dBc/Hz Reduces System Noise Floor Contribution
- Manual or Automatic VCO Selection Permits Fast Switching
- Output Phase Reset and Adjustment Allow Synchronization of Multiple Synthesizers
- On-Chip Temperature Sensor with 7-Bit ADC Ensures Optimum VCO Selection
- Cycle Slip Reduction and Fast Lock Features Improve Accuracy and Acquisition Time
- VCO Lock Maintained Over Entire Temperature Range Provides Glitch-Free Operation
- Dual Differential Programmable Outputs Maximize Flexibility of Use

***Ordering Information* and *Typical Application Circuit* appears at end of data sheet.**

Functional Diagram



19-7106; Rev 0; 9/14

Absolute Maximum Ratings

$V_{CC\_}$ to GND_ ....-0.3V to +3.9V
All Other Pins to GND_ ....-0.3V to $V_{CC\_}$ + 0.3V
Continuous Power Dissipation (T_A = +70°C)
TQFN-EP Multilayer Board
(derate 34.5mW/°C above +70°C) 2758.6mW

Junction Temperature ....+150°C
Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(Measured using MAX2871 EV Kit. $V_{CC\_}$ = 3V to 3.6V, $V_{GND\_}$ = 0V, f_{REF_IN} = 50MHz, f_{PFD} = 50MHz, T_A = -40°C to +85°C. Typical values measured at $V_{CC\_}$ = 3.3V; T_A = +25°C; register settings 00780000, 20000141, 01005E42, 00000013, 610F423C, 01400005;. unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			3	3.3	3.6	V
RFOUT_ Current Consumption	$I_{RFOUT\_}$, minimum output power, single channel			9		mA
	$I_{RFOUT\_}$, maximum output power, single channel			25		
Supply Current	Both channels enabled, maximum output power	Total, including RFOUT, both channel (Note 3)		165	200	mA
		Each output divide-by-2		8		
		I_{CCVCO} + I_{CCRF} (Note 3)		122		
		Low-power sleep mode			1	

AC Electrical Characteristics

(Measured using MAX2871 EV Kit. $V_{CC\_}$ = 3V to 3.6V, $V_{GND\_}$ = 0V, f_{REF_IN} = 50MHz, f_{PFD} = 25MHz, $f_{RFOUT\_}$ = 6000MHz, T_A = -40°C to +85°C. Typical values measured at $V_{CC\_}$ = 3.3V, T_A = +25°C, register settings 00780000, 20000141, 01005E42, 00000013, 610F423C, 01400005; unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE OSCILLATOR INPUT (REF_IN)					
REF_IN Input Frequency Range		10		210	MHz
REF_IN Input Sensitivity		0.7		$V_{CC\_}$	V_{P-P}
REF_IN Input Capacitance			2		pF
REF_IN Input Current		-60		+60	µA
PHASE DETECTOR					
Phase Detector Frequency	Integer-N mode			140	MHz
	Fractional-N mode			125	

AC Electrical Characteristics (continued)

(Measured using MAX2871 EV Kit. $V_{CC\_}$ = 3V to 3.6V, $V_{GND\_}$ = 0V, f_{REF_IN} = 50MHz, f_{PFD} = 25MHz, $f_{RFOUT\_}$ = 6000MHz, T_A = -40°C to +85°C. Typical values measured at $V_{CC\_}$ = 3.3V, T_A = +25°C, register settings 00780000, 20000141, 01005E42, 00000013, 610F423C, 01400005; unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE PUMP						
Sink/Source Current	CP[3:0] = 1111, R_{SET} = 5.1kΩ			5.12		mA
	CP[3:0] = 0000, R_{SET} = 5.1kΩ			0.32		
R_{SET} Range			2.7		10	kΩ
RF OUTPUTS						
Fundamental Frequency Range			3000		6000	MHz
Divided Frequency Range	With output dividers (1/2/4/8/16/32/64/128)		23.4375		6000	MHz
VCO Sensitivity				100		MHz/V
Frequency Pushing	Open loop			0.8		MHz/V
Frequency Pulling	Open loop into 2:1 VSWR			70		kHz
2nd Harmonic	Fundamental VCO output			-40		dBc
3rd Harmonic	Fundamental VCO output			-34		dBc
2nd Harmonic	VCO output divided-by-2			-25		dBc
3rd Harmonic	VCO output divided-by-2			-20		dBc
Maximum Output Power	$f_{RFOUT\_}$ = 3000MHz (Note 4)			5		dBm
Minimum Output Power	$f_{RFOUT\_}$ = 3000MHz (Note 4)			-4		dBm
Output Power Variation (Note 4)	-40°C ≤ T_A ≤ +85°C			1		dB
	3V ≤ $V_{CC\_}$ ≤ 3.6V			0.2		
Muted Output Power	(Note 4)			-40		dBm
VCO AND FREQUENCY SYNTHESIZER NOISE						
VCO Phase Noise (Note 5)	VCO at 3000MHz	10kHz offset		-83		dBc/Hz
		100kHz offset		-111		
		1MHz offset		-136		
		5MHz offset		-149		
	VCO at 4500MHz	10kHz offset		-77		
		100kHz offset		-106		
		1MHz offset		-132		
		5MHz offset		-147		
	VCO at 6000MHz	10kHz offset		-71		
		100kHz offset		-101		
		1MHz offset		-128		
		5MHz offset		-144		
In-Band Noise Floor	Normalized (Note 6)			-229		dBc/Hz
1/f Noise	Normalized (Note 7)			-122		dBc/Hz
In-Band Phase Noise	(Note 8)			-102		dBc/Hz
Integrated RMS Jitter	(Note 9)			0.2		ps

AC Electrical Characteristics (continued)

(Measured using MAX2871 EV Kit. $V_{CC\_}$ = 3V to 3.6V, $V_{GND\_}$ = 0V, f_{REF_IN} = 50MHz, f_{PFD} = 25MHz, $f_{RFOUT\_}$ = 6000MHz, T_A = -40°C to +85°C. Typical values measured at $V_{CC\_}$ = 3.3V, T_A = +25°C, register settings 00780000, 20000141, 01005E42, 00000013, 610F423C, 01400005; unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Spurious Signals Due to PFD Frequency	50kHz loop bandwidth		-88		dBc
VCO Tune Voltage		0.5		$V_{CC\_}$ - 0.5	V
TEMPERATURE SENSOR AND ADC					
ADC Resolution			7		Bits
Temperature Sensor Accuracy			3		°C

DIGITAL I/O CHARACTERISTICS

($V_{CC\_}$ = +3V to +3.6V, $V_{GND\_}$ = 0V, T_A = -40°C to +85°C. Typical values at $V_{CC\_}$ = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE INPUTS (CLK, DATA, LE, CE, RFOUT_EN)					
Input Logic-Level Low	V_{IL}		0.4		V
Input Logic-Level High	V_{IH}		1.5		V
Input Current	I_{IH}/I_{IL}	-1		+1	µA
Input Capacitance			1		pF
SERIAL INTERFACE OUTPUTS (MUX, LD)					
Output Logic-Level Low	0.3mA sink current			0.4	V
Output Logic-Level High	0.3mA source current	V_{CC} - 0.4			V
Output Current Level High			0.5		mA

SPI TIMING CHARACTERISTICS

($V_{CC\_}$ = +3V to +3.6V, $V_{GND\_}$ = 0V, T_A = -40°C to +85°C. Typical values at $V_{CC\_}$ = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Clock Period	t_{CP}	Guaranteed by SCL pulse-width low and high	50			ns
CLK Pulse-Width Low	t_{CL}		25			ns
CLK Pulse-Width High	t_{CH}		25			ns
LE Setup Time	t_{LES}		20			ns
LE Hold Time	t_{LEH}		10			ns
LE Minimum Pulse-Width High	t_{LEW}		20			ns
Data Setup Time	t_{DS}		25			ns
Data Hold Time	t_{DH}		25			ns
MUX Valid	t_{DOT}	MUX transition valid after CLK fall			10	ns

Note 2: Production tested at T_A = +25°C. Cold and hot are guaranteed by design and characterization.

Note 3: f_{REFIN} = 100MHz, phase detector frequency = 25MHz, RF output = 6000MHz. Register setting: 00780000, 00400061, 34011242, F8010003, 638FF1FC, 80400005.

Note 4: Measured single ended with 27nH to V_{CC_RF} into 50Ω load. Power measured with single output enabled. Unused output has 27nH to V_{CC_RF} with 50Ω termination.

Note 5: VCO phase noise is measured open loop.

Note 6: Measured at 200kHz using a 50MHz Bliley NV108C19554 OCVCXO with 2MHz loop bandwidth. Register setting 801E0000, 8000FFF9, 80005FC2, 6C10000B, 638E80FC, 400005. EV kit loop filter: C2 = 1500pF, C1 = 33pF, R2A = 0Ω, R2B = 1100Ω, R3 = 0Ω, C3 = open.

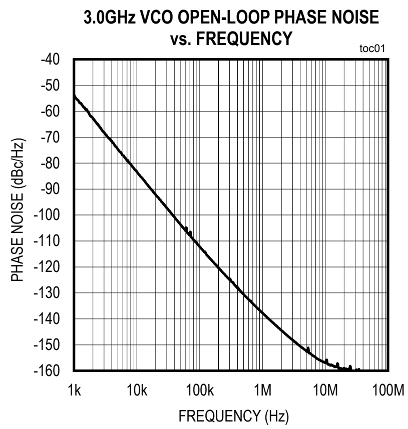
Note 7: 1/f noise contribution to the in-band phase noise is computed by using 1/fnoise + 10log(10kHz/f_{OFFSET}) + 20log(f_{RF}/1GHz). Register setting: 803A0000, 8000FFF9, 81005F42, F4000013, 6384803C, 001500005.

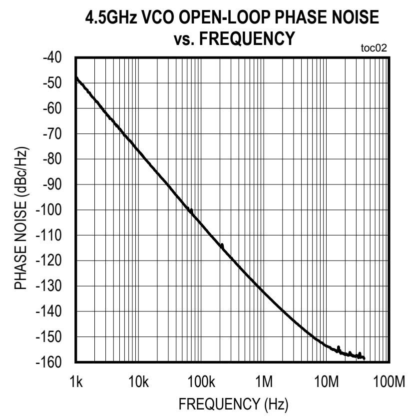
Note 8: f_{REFIN} = 50MHz; f_{PFD} = 25MHz; offset frequency = 10kHz; VCO frequency = 4227MHz, output divide-by-2 enabled. RFOUT = 2113.5MHz; N = 169; loop BW = 40kHz, CP[3:0] = 1111; integer mode.

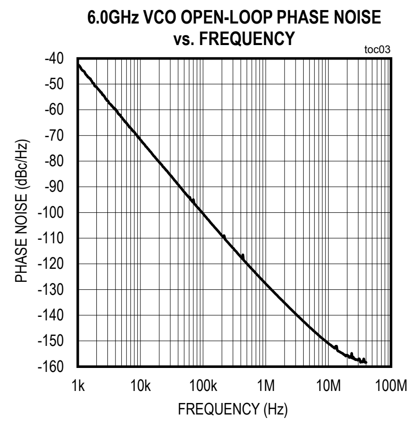
Note 9: f_{REFIN} = 50MHz; f_{PFD} = 50MHz; VCO frequency = 4400MHz, $f_{RFOUT\_}$ = 4400MHz; loop BW = 65kHz. Register setting: 002C0000, 200303E9, 80005642, 00000133, 638E82FC, 01400005. EV kit loop filter: C2 = 0.1µF, C1 = 0.012µF, R2A = 0Ω, R2B = 120Ω, R3 = 250Ω, C3 = 820pF.

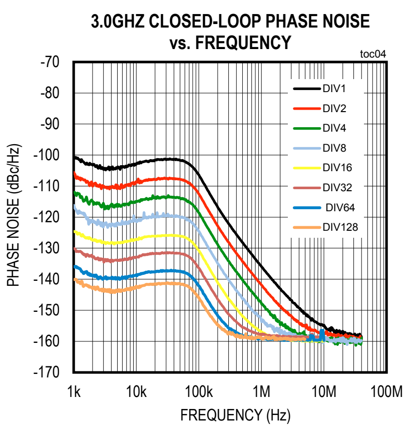
Typical Operating Characteristics

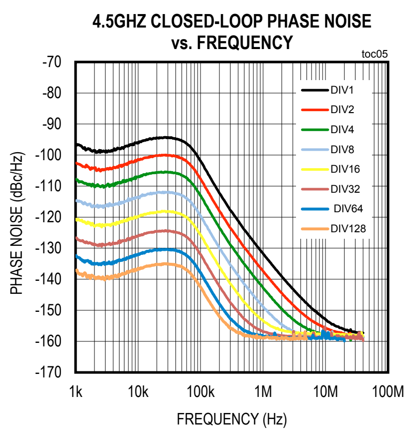
(Measured with MAX2871 EV Kit. $V_{CC\_}$ = 3.3V, $V_{GND\_}$ = 0V, f_{REF_IN} = 50MHz, T_A = +25°C, see the Testing Conditions Table.)

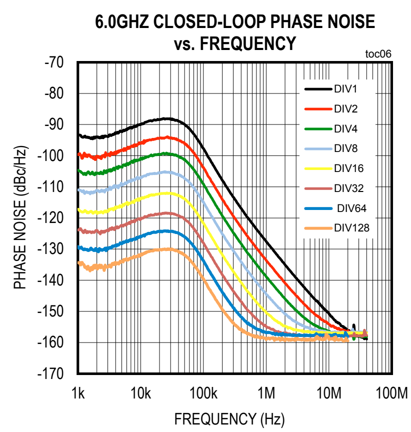


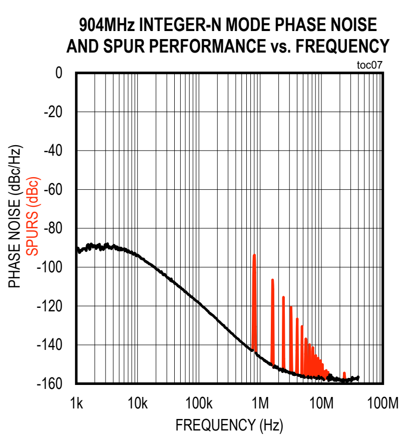


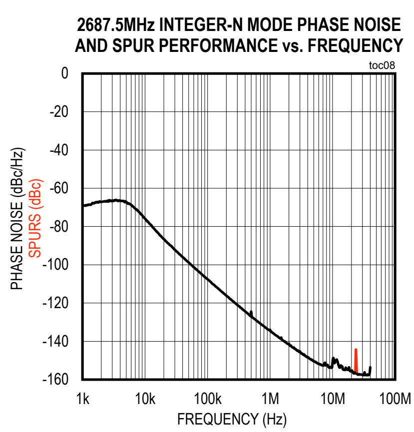


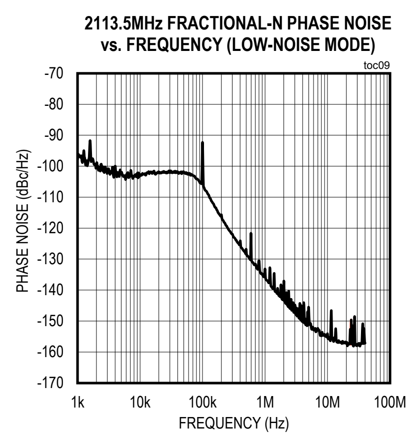








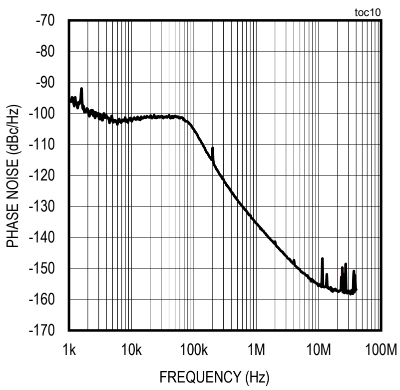




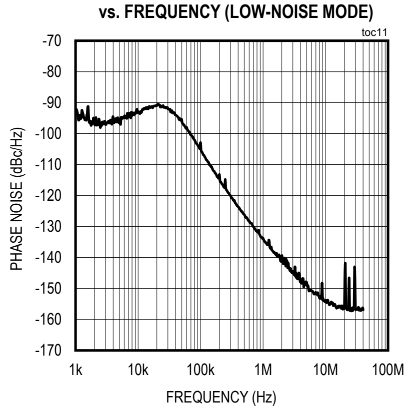
Typical Operating Characteristics (continued)

(Measured with MAX2871 EV Kit. $V_{CC\_}$ = 3.3V, $V_{GND\_}$ = 0V, f_{REF_IN} = 50MHz, T_A = +25°C, see the Testing Conditions Table.)

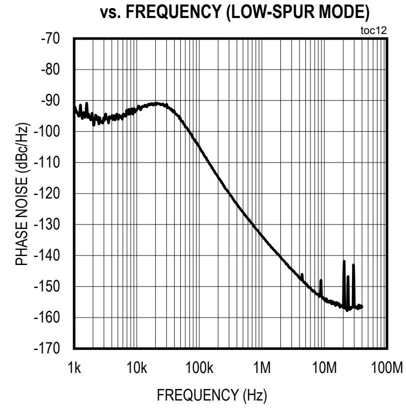
2113.5MHz FRACTIONAL-N PHASE NOISE vs. FREQUENCY (LOW-SPUR MODE)



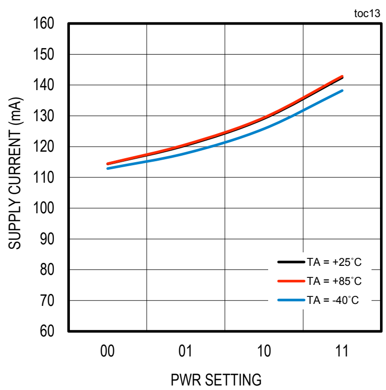
2679.4MHz FRACTIONAL-N PHASE NOISE vs. FREQUENCY (LOW-NOISE MODE)



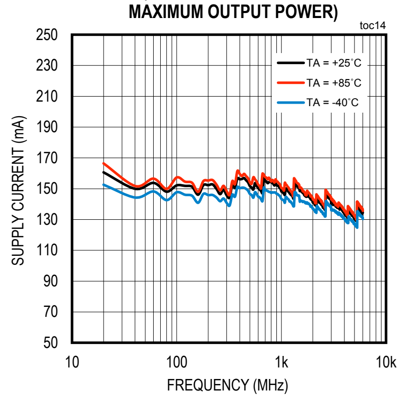
2679.4MHz FRACTIONAL-N PHASE NOISE vs. FREQUENCY (LOW-SPUR MODE)



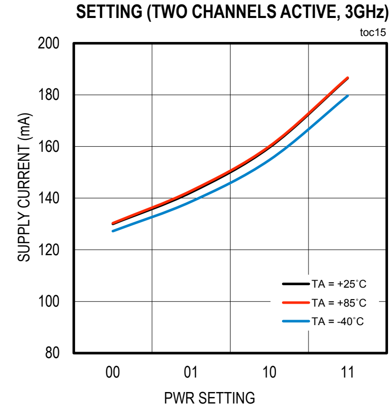
SUPPLY CURRENT vs. OUTPUT POWER SETTING (ONE CHANNEL ACTIVE, 3GHz)



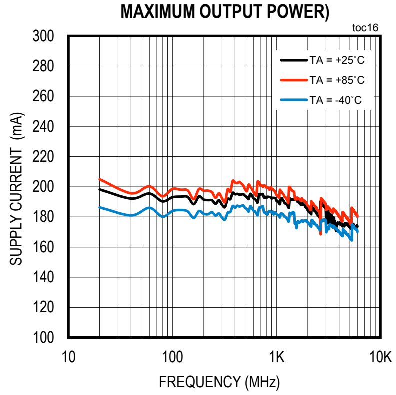
SUPPLY CURRENT vs. FREQUENCY (ONE CHANNEL ACTIVE, MAXIMUM OUTPUT POWER)



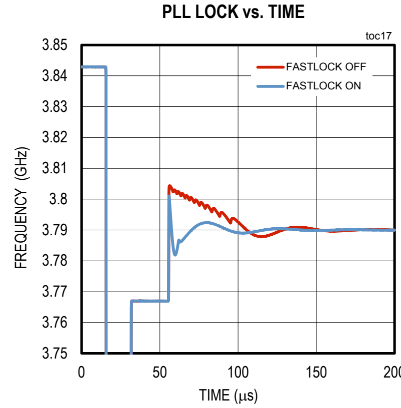
SUPPLY CURRENT vs. OUTPUT POWER SETTING (TWO CHANNELS ACTIVE, 3GHz)



SUPPLY CURRENT vs. FREQUENCY (TWO CHANNELS ACTIVE, MAXIMUM OUTPUT POWER)



PLL LOCK vs. TIME



Typical Operating Characteristics Testing Conditions Table

TOC TITLE	f_{REF} (MHz)	f_{PFD} (MHz)	REGISTER SETTINGS (hex)	LOOP FILTER BW (Hz)	MAX2871 EV KIT COMPONENT VALUES					COMMENTS
					C2 (F)	R2A + R2B (Ω)	C1 (F)	R3 (Ω)	C3 (F)	
3.0GHz VCO OPEN-LOOP PHASE NOISE vs. FREQUENCY	N/A	N/A	80B40000, 80000141, 0000405A, XX00013, 648020FC, 00000005	N/A	N/A	N/A	N/A	N/A	N/A	VCO bits set for 3GHz output, VAS_SHDN = 1
4.5GHz VCO OPEN-LOOP PHASE NOISE vs. FREQUENCY	N/A	N/A	80B40000, 80000141, 0000405A, XX00013 648020FC, 00000005	N/A	N/A	N/A	N/A	N/A	N/A	VCO bits set for 4.5GHz output, VAS_SHDN = 1
6.0GHz VCO OPEN-LOOP PHASE NOISE vs. FREQUENCY	N/A	N/A	80B40000, 80000141 0000405A XX00013, 648020FC 00000005	N/A	N/A	N/A	N/A	N/A	N/A	VCO bits set for 6.0GHz output, VAS_SHDN = 1
3.0GHz CLOSED-LOOP PHASE NOISE vs. FREQUENCY	50	25	803C0000 80000141 00009E42, E8000013, 618160FC, 00400005	40k	0.1µ	120	0.012µ	250	820p	
4.5GHz CLOSED-LOOP PHASE NOISE vs. FREQUENCY	50	25	805A0000, 80000141, 00009E42, E8000013, 618160FC, 00400005	40k	0.1µ	120	0.012µ	250	820p	
6.0GHz CLOSED-LOOP PHASE NOISE vs. FREQUENCY	50	25	80780000, 80000141, 00009E42, EA000013, 608C80FC, 00400005	40k	0.1µ	120	0.012µ	250	820p	

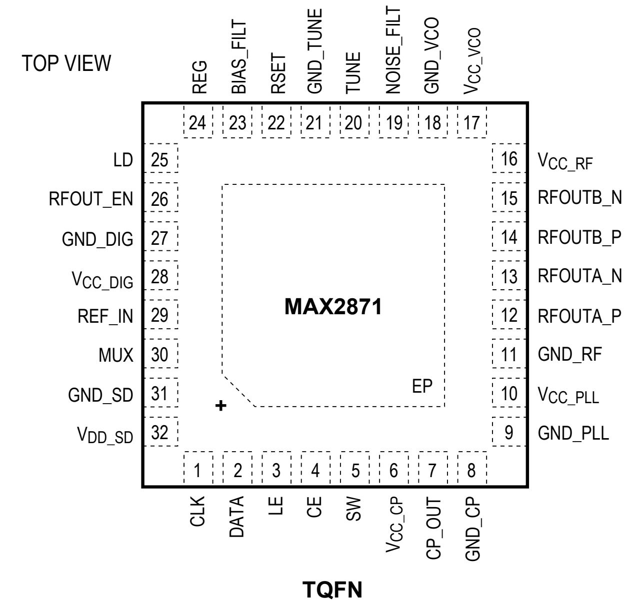
Typical Operating Characteristics Testing Conditions Table (continued)

TOC TITLE	f_{REF} (MHz)	f_{PFD} (MHz)	REGISTER SETTINGS (hex)	LOOP FILTER BW (Hz)	MAX2871 EV KIT COMPONENT VALUES					COMMENTS
					C2 (F)	R2A + R2B (Ω)	C1 (F)	R3 (Ω)	C3 (F)	
904MHz INTEGER-N MODE PHASE NOISE AND SPUR PERFOMANCE vs. FREQUENCY	40	0.8	82350000, 800007D1 E1065FC2, 2C000013 6020803C 00400005	16k	0.1µ	806	3300p	1201	470p	
2687.5MHz INTEGER-N PHASE NOISE AND SPUR PERFORMANCE vs. FREQUENCY	40	0.5	94FF0000, 803207D1, 010A1E42, B00000A3, 6090803C, 00400005	5k	0.1µ	1000	6800p	300	0.01µ	
2113.5MHz FRACTIONAL-N PHASE NOISE (LOW-NOISE MODE) vs. FREQUENCY	50	25	00548050, 400003E9, 81005FC2, E8000013, 609C80FC, 00400005	40k	0.1µ	120	0.012µ	250	820p	
2113.5MHz FRACTIONAL-N PHASE NOISE vs. FREQUENCY (LOW-SPUR MODE)	50	25	00548050, 400003E9, E1005FC2, E8000013, 609C80FC, 00400005	40k	0.1µ	120	0.012µ	250	820p	
2679.4MHz FRACTIONAL-N PHASE NOISE vs. FREQUENCY (LOW-NOISE MODE)	50	25	00358160, 203207D1, 01005E42, B20000A3, 6010003C, 00400005	40k	0.1µ	120	0.012µ	250	820p	
2679.4MHz FRACTIONAL-N PHASE NOISE vs. FREQUENCY (LOW-SPUR MODE)	50	25	00358160, 203207D1, 41005E42, B20000A3, 6010003C, 00400005	40k	0.1µ	120	0.012µ	250	820p	
SUPPLY CURRENT vs. OUTPUT POWER SETTING (ONE CHANNEL ACTIVE, 3GHz)	50	25	003C0000, 20000321, 01005E42, 00000013, 610F423C, 01400005,							APWR swept from 00 to 11

Typical Operating Characteristics Testing Conditions Table (continued)

TOC TITLE	f_{REF} (MHz)	f_{PFD} (MHz)	REGISTER SETTINGS (hex)	LOOP FILTER BW (Hz)	MAX2871 EV KIT COMPONENT VALUES					COMMENTS
					C2 (F)	R2A + R2B (Ω)	C1 (F)	R3 (Ω)	C3 (F)	
SUPPLY CURRENT vs. FREQUENCY (ONE CHANNEL ACTIVE, MAXIMUM OUTPUT POWER)	50	25	003C0000, 20000321, 01005E42, 00000013, 610F423C, 01400005							N and F values changed for each frequency
SUPPLY CURRENT vs. OUTPUT POWER SETTING (TWO CHANNELS ACTIVE)	50	25	003C0000, 20000321, 01005E42, 00000013, 610F43FC, 01400005							APWR and BPWR swept from 00 to 11
SUPPLY CURRENT vs. FREQUENCY (TWO CHANNELS ACTIVE MAXIMUM OUTPUT POWER)	50	25	003C0000, 20000321, 01005E42, 00000013, 610F43FC, 01400005							N and F values swept for each frequency
PLL LOCK vs. TIME	40	40	00250120, 20320141, 00004042, 000000A3, 0184023C, 01400005	40k	0.1µ	120	0.012µ	250	820p	CDM changed from 00 to 01

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	CLK	Serial Clock Input. The data is latched into the 32-bit shift register on the rising edge of the CLK line.
2	DATA	Serial Data Input. The serial data is loaded MSB first. The 3 LSBs identify the register address.
3	LE	Load Enable Input. When LE goes high the data stored in the shift register is loaded into the appropriate latches.
4	CE	Chip Enable. A logic-low powers the part down and the charge pump becomes high impedance.
5	SW	Fast-Lock Switch. Connect to the loop filter when using the fast-lock mode.
6	V_{CC_CP}	Power Supply for Charge Pump. Place decoupling capacitors as close as possible to the pin.
7	CP_OUT	Charge-Pump Output. Connect to external loop filter input.
8	GND_CP	Ground for Charge-Pump. Connect to board ground, not to the paddle.
9	GND_PLL	Ground for PLL. Connect to main board ground plane, not to the paddle.
10	V_{CC_PLL}	Power Supply for PLL. Place decoupling capacitors as close as possible to the pin.
11	GND_RF	Ground for RF Outputs. Connect to board ground plane, not to the paddle.
12	RFOUTA_P	Open Collector Positive RF Output A. See RFOUT± and RFOUTB± section in *Detailed Description*.
13	RFOUTA_N	Open Collector Negative RF Output A. See RFOUT± and RFOUTB± section in *Detailed Description*.

Pin Description (continued)

PIN	NAME	FUNCTION
14	RFOUTB_P	Open Collector Positive RF Output B. See RFOUT± and RFOUTB± section in *Detailed Description*.
15	RFOUTB_N	Open Collector Negative RF Output B. See RFOUT± and RFOUTB± section in *Detailed Description*.
16	V_{CC_RF}	Power Supply for RF Output and Dividers. Place decoupling capacitors as close as possible to the pin.
17	V_{CC_VCO}	VCO Power Supply. Place decoupling capacitors to the analog ground plane.
18	GND_VCO	Ground for VCO. Connect to main board ground plane, not directly to the paddle.
19	NOISE_FILT	VCO Noise Decoupling. Place a 1µF capacitor to ground.
20	TUNE	Control Input to the VCO. Connect to external loop filter.
21	GND_TUNE	Ground for Control Input to the VCO. Connect to main board ground plane, not directly to the paddle.
22	RSET	Charge-Pump Current Range Input. Connect an external resistor to ground to set the minimum CP current. $I_{CP} = 1.63/R_{SET} \times (1 + CP)$
23	BIAS_FILT	VCO Noise Decoupling. Place a 1µF capacitor to ground.
24	REG	Reference Voltage Compensation. Place a 1µF capacitor to ground.
25	LD	Lock Detect Output. Logic-high when locked, and logic-low when unlocked. See register description for more details (Table 9).
26	RFOUT_EN	RF Output Enable. A logic-low disables the RF outputs.
27	GND_DIG	Ground for Digital Circuitry. Connect to main board ground plane, not directly to the paddle.
28	V_{CC_DIG}	Power Supply for Digital Circuitry. Place decoupling capacitors as close as possible to pin.
29	REF_IN	Reference Frequency Input. This is a high-impedance input with a nominal bias voltage of $V_{CC\_DIG}/2$. AC-couple to reference signal.
30	MUX	Multiplexed I/Os. See Table 5.
31	GND_SD	Ground for Sigma-Delta Modulator. Connect to main board ground plane, not directly to the paddle.
32	V_{CC_SD}	Power Supply for Sigma-Delta Modulator. Place decoupling capacitors as close as possible to the pin.
—	EP	Exposed Pad. Connect to board ground.

Detailed Description

4-Wire Serial Interface

The MAX2871 serial interface contains six write-only and one read-only 32-bit registers. The 29 most-significant bits (MSBs) are data, and the three least-significant bits (LSBs) are the register address. Register data is loaded MSB first through the 4-wire serial interface (SPI). When LE is logic-low, the logic level at DATA is shifted at the rising edge of CLK. At the rising edge of LE, the 29 data bits are latched into the register selected by the address bits. The user must program all register values after power-up.

Register programming order should be address 0x05, 0x04, 0x03, 0x02, 0x01, and 0x00. Several bits are double buffered to update the settings at the same time. See the register descriptions for double buffered settings.

Register 0x06 can be read back through MUX. The user must set MUX = 1100. To begin the read sequence, set LE to logic-low, send 32 periods of CLK, and set LE to logic-high. While the CLK is running, the DATA pin can be held at logic-high or logic-low for 29 clocks, but the last 3 bits must be 110 to indicate register 6. Then finally, send 1 period of the clock. The MSB of register 0x06 appears on the falling edge of the next clock and continues to shift out for the next 29 clock cycles (Figure 2). After the LSB of register 0x06 has been read, the user can reset MUX = 0000.

Power Modes

The MAX2871 can be put into low-power mode by setting SHDN = 1 (register 2, bit 5) or by setting the CE pin to logic-low.

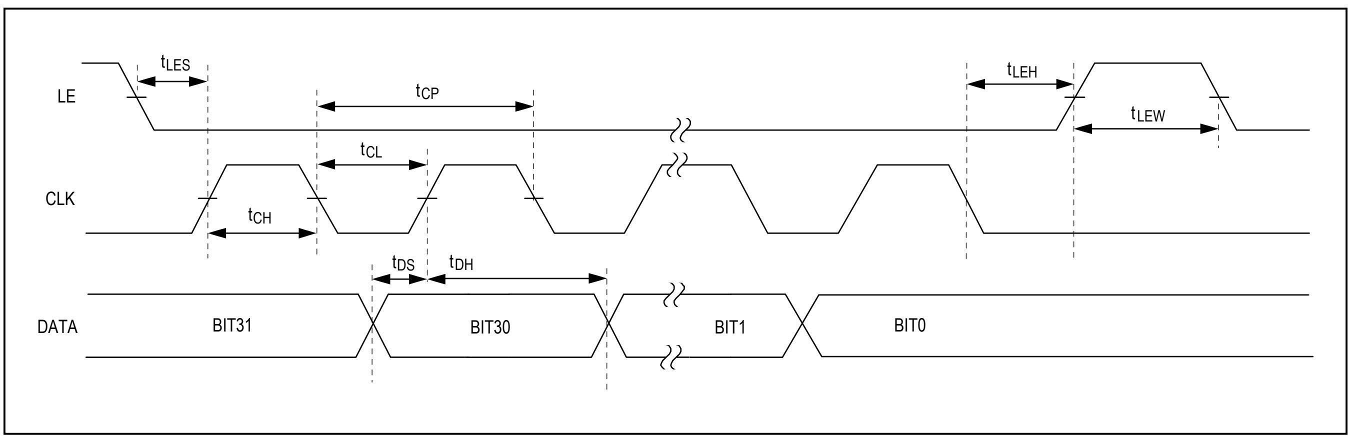


Figure 1. SPI Timing Diagram

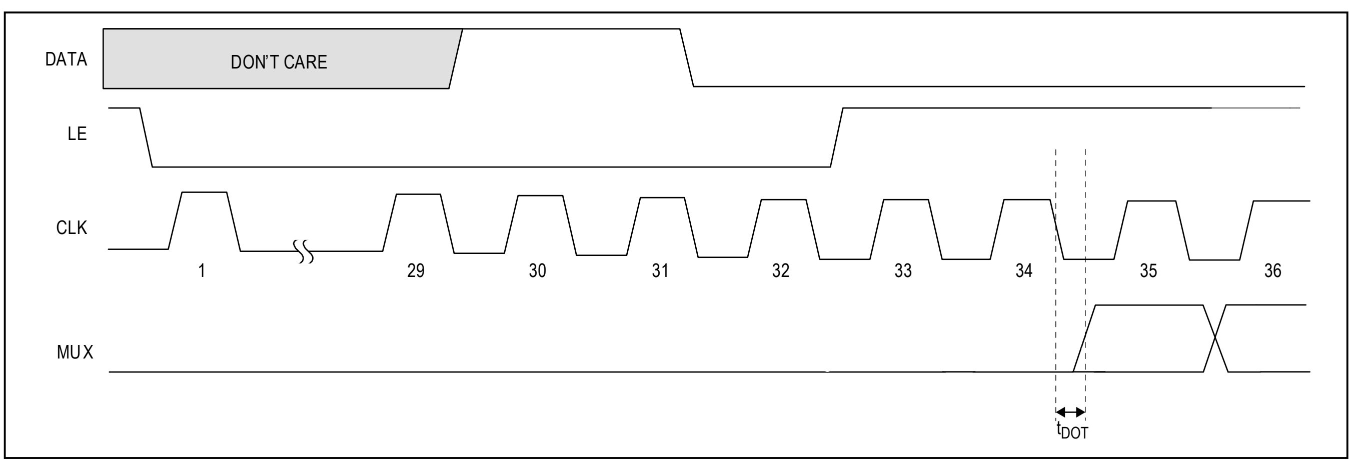


Figure 2. Initiating Readback

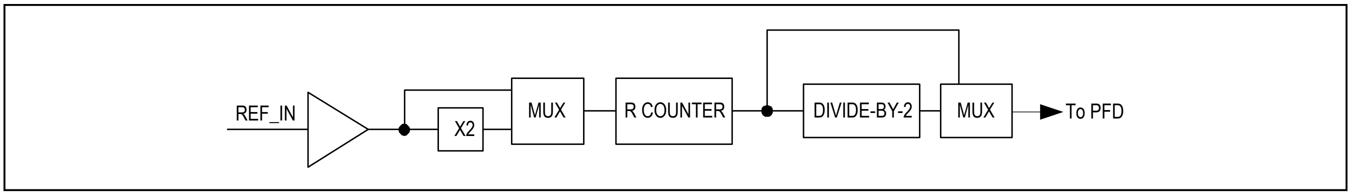


Figure 3. Reference Input

After exiting low-power mode, allow at least 20ms for external capacitors to charge to their final values before programming the final VCO frequency.

Reference Input

The reference input stage is configured as a CMOS inverter with shunt resistance from input to output. In shutdown mode this input is set to high impedance to prevent loading of the reference source.

The reference input signal path also includes optional x2 and ÷2 blocks. When the reference doubler is enabled (DBR = 1), the maximum reference input frequency is limited to 105MHz. When the doubler is disabled, the reference input frequency is limited to 210MHz. The minimum reference frequency is 10MHz. The minimum R counter divide ratio is 1, and the maximum divide ratio is 1023.

Int, Frac, Mod and R Counter Relationship

The phase-detector frequency is determined as follows:

$$f_{PFD} = f_{REF} \times [(1 + DBR)/(R \times (1 + RDIV2))]$$

f_{REF} represents the external reference input frequency. DBR (register 2, bit 25) sets the f_{REF} input frequency doubler mode (0 or 1). RDIV2 (register 2, bit 24) sets the f_{REF} divide-by-2 mode (0 or 1). R (register 2, bits 23:14) is the value of the 10-bit programmable reference counter (1 to 1023). The maximum f_{PFD} is 125MHz for frac-N mode and 140MHz for int-N mode. The R-divider can be held in reset when RST (register 2, bit 3) = 1.

The VCO frequency (f_{VCO}), N, F, and M can be determined based on desired RF output frequency (f_{RFOUTA}) as follows:

Set DIVA value property based on f_{RFOUTA} and Table 4 (register 4, bits 22:20)

$$f_{VCO} = f_{RFOUTA} \times DIVA$$

If bit FB = 1, (DIVA is not in PLL feedback loop):

$$N + (F/M) = f_{VCO}/f_{PFD}$$

If bit FB = 0, (DIVA is in PLL feedback loop) and DIVA ≤ 16:

$$N + (F/M) = (f_{VCO}/f_{PFD})/DIVA$$

If bit FB = 0, (DIVA is in PLL feedback loop) and DIVA > 16:

$$N + (F/M) = (f_{VCO} / f_{PFD})/16$$

N is the value of the 16-bit N counter (16 to 65535), programmable through bits 30:15 of register 0. M is the fractional modulus value (2 to 4095), programmable through bits 14:3 of register 1. F is the fractional division value (0 to MOD - 1), programmable through bits 14:3 of register 0. In frac-N mode, the minimum N value is 19 and maximum N value is 4091. The N counter is held in reset when RST = 1 (register 2, bit 3). DIVA is the RF output divider setting (0 to 7), programmable through bits 22:20 of register 4. The division ratio is set by 2^{DIVA}.

The RF B output frequency is determined as follows:

If BDIV = 0 (register 4, bit 9), $f_{RFOUTB} = f_{RFOUTA}$.

If BDIV = 1, $f_{RFOUTB} = f_{VCO}$.

Int-N/Frac-N Modes

Integer-N mode is selected by setting bit INT = 1 (register 0, bit 31). When operating in integer-N mode, it is also necessary to set bit LDF (register 2, bit 8) to set the lock detect to integer-N mode.

The device's frac-N mode is selected by setting bit INT = 0 (register 0, bit 31). Additionally, set bit LDF = 0 (register 2, bit 8) for frac-N lock-detect mode.

If the device is in frac-N mode, it will remain in frac-N mode when fractional division value F = 0, which can result in unwanted spurs. To avoid this condition, the device can automatically switch to integer-N mode when F = 0 if the bit F01 = 1 (register 5, bit 24).

Phase Detector and Charge Pump

The device's charge-pump current is determined by the value of the resistor from pin RSET to ground and the value of bits CP (register 2, bits 12:9) as follows:

$$I_{CP} = 1.63/R_{SET} \times (1 + CP\langle 3:0 \rangle)$$

To reduce spurious in frac-N mode, set charge-pump linearity bits CPL = 00/01/10/11 (register 1, bits 30:29). The user can determine which mode works best for their application. For int-N mode, set CPL = 00.

The charge-pump output can be put into high-impedance mode when TRI = 1 (register 2, bit 4). The output is in normal mode when TRI = 0.

The phase detector polarity can be changed if an active inverting loop filter topology is used. For noninverting loop filters, set PDP = 1 (register 2, bit 6). For inverting loop filters, set PDP = 0.

MUX

MUX is a multipurpose input/output for observing and controlling various internal functions of the MAX2871. MUX can also be configured as serial data output. Bits MUX (register 5, bit 18 and register 2, bit 28:26) are used to select the desired MUX function (see Table 5).

Lock Detect

Lock detect can be monitored through the LD output by setting the LD bits (register 5, bits 23:22). For digital lock detect, set LD = 01. The digital lock detect is dependent on the mode of the synthesizer. In frac-N mode set LDF = 0, and in int-N mode set LDF = 1. To set the accuracy of the digital lock detect, see Table 1 and Table 2.

Analog lock detect can be set with LD = 10. In this mode, LD is an open-drain output and requires an external pullup resistor.

The lock detect output validity is dependent on many factors. The lock detect output is not valid during VCO auto selection process. After the VCO auto selection process has completed, the lock detect output is not valid until the TUNE voltage has settled. TUNE voltage settling time is dependent on loop filter bandwidth, and can be calculated using EE-Sim Simulation tool found at **www.maximintegrated.com**.

Cycle Slip Reduction

Cycle slip reduction is one of the two methods available to improve lock time. It is enabled by setting CSM bit (register 3, bit 18) to 1. In this mode, the charge pump must be set to its minimum value.

Fast-Lock

Another method to decrease lock time is to use a fast-lock mode. This mode requires that CP = 0000 (register 2, bits 12:9) and that the shunt resistive portion of the loop filter be segmented into two parts, where one resistor is 1/4 of the total resistance, and the other resistor is 3/4 of the

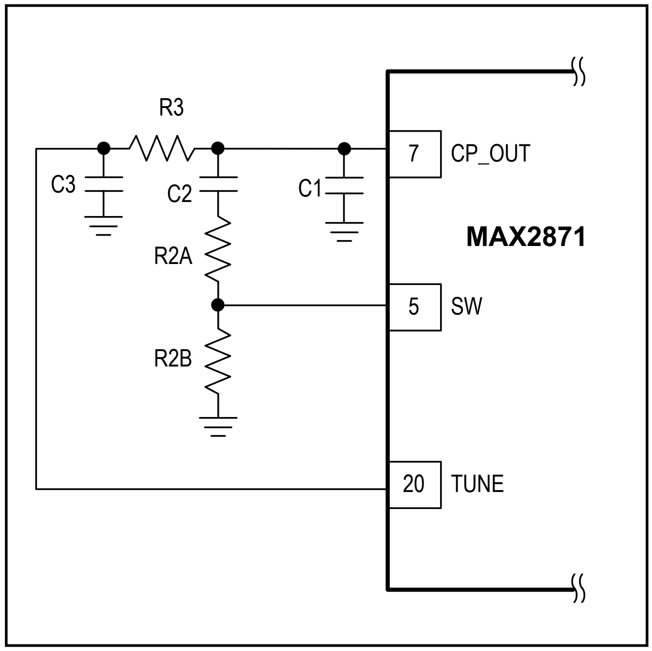


Figure 4. Fast Lock Filter Topology

Table 1. Frac-N Digital Lock-Detect Settings

PFD FREQUENCY	LDS	LDP	LOCKED UP/DOWN TIME SKEW (ns)	NUMBER OF LOCKED CYCLES TO SET LD	UP/DOWNTIME SKEW TO UNSET LD (ns)
≤ 32MHz	0	0	10	40	15
≤ 32MHz	0	1	6	40	15
> 32MHz	1	X	4	40	4

Table 2. Int-N Digital Lock-Detect Settings

PFD FREQUENCY	LDS	LDP	LOCKED UP/DOWN TIME SKEW (ns)	NUMBER OF LOCKED CYCLES TO SET LD	UP/DOWNTIME SKEW TO UNSET LD (ns)
≤ 32MHz	0	0	10	5	15
≤ 32MHz	0	1	6	5	15
> 32MHz	1	X	4	5	4

total resistance. The larger resistor should be connected from ground to SW, and the smaller resistor from SW to the loop filter capacitor (see Figure 4). When CDM = 01 (register 3, bits 16:15), fast-lock is active after the VAS has completed. During fast-lock, the charge pump is increased to CP = 1111 and the shunt loop filter resistance is set to 1/4 of the total resistance by changing pin SW from high impedance to ground. Fast-lock deactivates after a timeout set by the user. This timeout is loop filter dependent, and is set by:

$$t_{FAST\text{-}LOCK} = M \times CDIV/f_{PFD}$$

where M is the modulus setting and CDIV is the clock divider setting. The user must determine the CDIV setting based on their loop filter time constant.

RFOUTA± and RFOUTB±

The device has dual differential open-collector RF outputs that require an external RF choke or a 50Ω resistor to supply for each output. Each differential output can be independently enabled or disabled by setting bits RFA_EN (register 4, bit 5) and RFB_EN (register 4, bit 8). Both outputs are also controlled by applying a logic-high (enabled) or logic-low (disabled) to pin RFOUT_EN.

The output power of each output can be individually controlled with APWR (register 4, bits 4:3) for RFOUTA and BPWR (register 4, bits 7:6) for RFOUTB. The available differential output power settings are from -4dBm to +5dBm, in 3dB steps with 50Ω pullup to supply. The available single-ended output power ranges from -4dBm to +5dBm in 3dB steps with a RF choke to supply. Across the entire frequency range different pullup elements (L or R) are required for optimal output power. If single-ended output is used, the unused output should be supplied and terminated in the same manner as the corresponding load. If a differential output is unused then those RFOUT pins should be directly connected to VCC_RF (pin 16).

To prevent undesired frequencies from being output while acquiring lock, the output power can be disabled when the PLL is unlocked by using MTLD (register 4, bit 10). A logic 1 will disable the outputs when the digital lock detect is logic low. When acquiring lock the output can overshoot and pass through the desired frequency. In some circumstances, the digital lock detect will flicker high during these periods. To prevent this from happening, a timer can be used to delay the output from enabling after losing lock. Enable MUTEDEL (register 3, bit 17) with MTLD enabled to use this function. The delay for enabling the output is set by:

$$\text{Delay} = CDIV \times M/f_{PFD}$$

where CDIV (register 3, bits 14:3) is the clock divider, M (register 1, bits 14:3) is the variable modulus for the fractional N modulator, and f_{PFD} is the phase detector frequency.

Voltage-Controlled Oscillator

The fundamental VCO frequency of the device guarantees gap-free coverage from 3.0GHz to 6.0GHz using four individual VCO core blocks with 16 sub-bands within each block. Connect the output of the loop filter to the TUNE input. The TUNE input is used to control the VCO.

Tune ADC

A 7-bit ADC is used to read back the VCO tuning voltage. The ADC value can be read back through register 6, bits 22:16. To digitize the tuning voltage, do the following:

1) Set bits CDIV (register 3, bits 14:3) = f_{PFD}/100kHz to set the clock speed for the ADC.
2) Set bits ADCM (register 5, bits 5:3) = 100 to enable the ADC to read the TUNE pin voltage.
3) Set bit ADCS (register 5, bit 6) = 1 to start the ADC conversion process.
4) Wait 100µs for the conversion process to finalize.
5) Read back register 6. The ADC value is located in bits 22:16.
6) Reset bits ADCM = 0 and ADCS = 0.

The voltage on the TUNE pin can be calculated as:

$$V = 0.315 + ADC \times 0.0165$$

VCO Autoselect (VAS) State Machine

An internal VCO autoselect state machine is initiated when register 0 is programmed to automatically select the correct VCO if bit VAS_SHDN = 0 (register 3, bit 25). If VAS_SHDN = 1, then the VCO can be manually selected by bits VCO (register 3, bits 31:26).

The state machine clock, f_{BS}, must be set to 50kHz. This is set by the BS bits (register 4, bits 25:24, 19:12). The formula for setting BS is:

$$BS = f_{PFD}/50kHz$$

where f_{PFD} is the phase-detector frequency. The BS value should be rounded to the nearest integer. If the calculated BS is higher than 1023, then set BS = 1023. If f_{PFD} is lower than 50kHz, then set BS = 1. The time needed to select the correct VCO is $10/f_{BS}$.

The VAS_TEMP bit (register 3, bit 24) can be used to select the best VCO for the given ambient temperature to ensure that the VCO will not drift out of lock if the temperature changes within -40°C to +85°C. Bits RFA_EN (register 4, bit 5) and RFB_EN (register 4, bit 8) must be 0 during VCO acquisition. Setting VAS_TEMP = 1 will increase the time needed to achieve lock from $10/f_{BS}$ to approximately 100ms.

Phase Adjustment

After achieving lock, the phase of the RF output can be changed in increments of P (register 1, bits 26:15) /M (register 1, bits 14:3) x 360°.

When aligning the phase of multiple devices, connect their MUX pins together and do the following:

1) Force the voltage on the MUX pin to V_{IL}.
2) Set MUX = 0111.
3) Program the MAX2871s for the desired frequency and allow them to lock.
4) Force the voltage on the MUX pins to V_{IH}. This resets the MAX2871s so they are synchronous.
5) Set P for the desired amount of phase shift for each part.
6) Set CDM (register 3, bits 16:15) = 10.
7) Reset CDM = 00.

Low-Spur Mode

The device offers three modes for the sigma-delta modulator. Low-noise mode offers lower in-band noise at the expense of spurs. The spurs can be reduced by setting SDN = 10 (register 2, bits 30:29) or SDN = 11 for different modes of dithering. The user can determine which mode works best for their application.

Temperature Sensor

The device is equipped with an on-chip temperature sensor and 7-bit ADC.

To read the digitized output of the temperature sensor:

1) Set bits CDIV (register 3, bits 14:3) = f_{PFD}/100kHz to set the clock speed for the ADC.
2) Set bits ADCM (register 5, bits 5:3) = 001 to enable the ADC to read the temperature.
3) Set bit ADCS (register 5, bit 6) = 1 to start the ADC conversion process.
4) Wait 100µs for the conversion process to finalize.
5) Read back register 6. The ADC value is located in bits 22:16.
6) Reset bits ADCM=0 and ADCS=0.

The approximate ambient temperature can be converted as:

$$t = 95 - 1.14 \times ADC$$

This formula is most accurate when the VCO is enabled and RFOUTA is enabled at full output power. The temperature can vary based on output power and if one or both outputs are enabled.

Register and Bit Descriptions

The operating mode of the device is controlled by five on-chip registers.

Defaults are not guaranteed upon power-up and are provided for reference only. All reserved bits should only be written with default values. In low-power mode, the register values are retained. Upon power-up, the registers should be programmed twice with at least a 20ms pause between writes. The first write ensures that the device is enabled, and the second write starts the VCO selection process.

Table 3. Register 0 (Address: 000, Default: 007D0000$_{HEX}$)

BIT LOCATION	BIT ID	NAME	DEFINITION
31	INT	Int-N or Frac-N Mode Control	0 = Enables the fractional-N mode 1 = Enables the integer-N mode The LDF bit must also be set to the appropriate mode.
30:15	N[15:0]	Integer Division Value	Sets integer part (N-divider) of the feedback divider factor. All integer values from 16 to 65,535 are allowed for integer mode. Integer values from 0 to 15 are not allowed. Integer values from 19 to 4091 are allowed for fractional mode.
14:3	FRAC[11:0]	Fractional Division Value	Sets fractional value: 000000000000 = 0 (see F01 bit description) 000000000001 = 1 ---- 111111111110 = 4094 111111111111 = 4095
2:0	ADDR[2:0]	Address Bits	Control Register address bits

Table 4. Register 1 (Address: 001, Default: $2000FFF9_{HEX}$)

BIT LOCATION	BIT ID	NAME	DEFINITION
31	Reserved	Reserved	Reserved. Program to 0.
30:29	CPL[1:0]	CP Linearity	Sets CP linearity mode. 00 = Disables the CP linearity mode (integer-N mode) 01 = Enables the CP linearity mode (frac-N mode) 10 = Reserved 11 = Reserved
28:27	CPT[1:0]	Charge Pump Test	Sets charge-pump test modes. 00 = Normal mode 01 = Long Reset mode 10 = Force CP into source mode 11 = Force CP into sink mode
26:15	P[11:0]	Phase Value	Sets phase value. See the *Phase Adjustment* section. 000000000000 = 0 000000000001 = 1 (recommended) ----- 111111111111 = 4095
14:3	M[11:0]	Modulus Value (M)	Fractional modulus value used to program f_{VCO}. See the *Int, Frac, Mod and R Counter Relationship* section. Double buffered by register 0. 000000000000 = 0 000000000001 = 1 000000000010 = 2 ----- 111111111111 = 4095
2:0	ADDR[2:0]	Address Bits	Control Register address bits

Table 5. Register 2 (Address: 010, Default: 00004042_{HEX})

BIT LOCATION	BIT ID	NAME	DEFINITION
31	LDS	Lock-Detect Speed	Lock-detect speed adjustment. 0 = $f_{PFD} \leq$ 32MHz 1 = f_{PFD} > 32MHz
30:29	SDN[1:0]	Frac-N Sigma Delta Noise Mode	Sets noise mode (see the Low-Spur Mode section.) 00 = Low-noise mode 01 = Reserved 10 = Low-spur mode 1 11 = Low-spur mode 2
28:26	MUX[2:0]	MUX Configuration	Sets MUX pin configuration (MSB bit located register 05). 0000 = Three-state output 0001 = D_VDD 0010 = D_GND 0011 = R-divider output 0100 = N-divider output/2 0101 = Analog lock detect 0110 = Digital lock detect 0111 = Sync Input 1000 : 1011 = Reserved 1100 = Read SPI registers 06 1101 : 1111= Reserved
25	DBR	Reference Doubler Mode	Sets reference doubler mode. 0 = Disable reference doubler 1 = Enable reference doubler
24	RDIV2	Reference Div2 Mode	Sets reference divide-by-2 mode. 0 = Disable reference divide-by-2 1 = Enable reference divide-by-2
23:14	R[9:0]	Reference Divider Mode	Sets reference divide value (R). Double buffered by register 0. 0000000000 = 0 (unused) 0000000001 = 1 ----- 1111111111 = 1023

Table 5. Register 2 (Address: 010, Default: 00004042$_{HEX}$) (continued)

BIT LOCATION	BIT ID	NAME	DEFINITION
13	REG4DB	Double Buffer	Sets double buffer mode. 0 = Disabled 1 = Enabled
12:9	CP[3:0]	Charge-Pump Current	Sets charge-pump current in mA (R_{SET} = 5.1kΩ). Double buffered by register 0. ICP = 1.63/RSET × (1+CP<3:0>)
8	LDF	Lock-Detect Function	Sets lock-detect function. 0 = Frac-N lock detect 1 = Int-N lock detect
7	LDP	Lock-Detect Precision	Sets lock-detect precision. 0 = 10ns 1 = 6ns
6	PDP	Phase Detector Polarity	Sets phase detector polarity. 0 = Positive 1 = Negative
5	SHDN	Shutdown Mode	Sets power-down mode. 0 = Normal mode 1 = Device shutdown
4	TRI	Charge Pump Output High-Impedance Mode	Sets charge-pump output high-impedance mode. 0 = Disabled 1 = Enabled
3	RST	Counter Reset	Sets counter reset mode. 0 = Normal operation 1 = R and N counters reset
2:0	ADDR[2:0]	Address Bits	Control Register address bits

Table 6. Register 3 (Address: 011, Default: 0000000B$_{HEX}$)

BIT LOCATION	BIT ID	NAME	DEFINITION
31:26	VCO[5:0]	VCO	Manual selection of VCO and VCO sub-band when VAS is disabled. 000000 = VCO0 …. 111111 = VCO63
25	VAS_SHDN	VAS_SHDN	Sets VAS shutdown mode. 0 = VAS enabled 1 = VAS disabled
24	VAS_TEMP	VAS_TEMP	Sets VAS response to temperature drift. 0 = VAS temperature compensation disabled 1 = VAS temperature compensation enabled
23:19	Reserved	Reserved	Reserved.
18	CSM	CSM	Cycle Slip Mode 0 = Disable Cycle Slip Mode 1 = Enable Cycle Slip Mode
17	MUTEDEL	MUTEDEL	Mute Delay 0 = Do not delay LD to MTLD function to prevent flickering 1= Delay LD to MTLD function to prevent flickering
16:15	CDM[1:0]	Clock Divider Mode	Sets clock divider mode. 00 = Mute until Lock Delay 01 = Fast-lock enabled 10 = Phase Adjustment mode 11 = Reserved
14:3	CDIV[11:0]	Clock Divider Value	Sets 12-bit clock divider value. 000000000000 = Unused 000000000001 = 1 000000000010 = 2 ----- 111111111111 = 4095
2:0	ADDR[2:0]	Address Bits	Control Register address bits

Table 7. Register 4 (Address: 100, Default: 6180B23C$_{HEX}$)

BIT LOCATION	BIT ID	NAME	DEFINITION
31:29	Reserved	Reserved	Reserved. Program to 011.
28	SDLDO	Shutdown VCO LDO	Sets Shutdown VCO LDO mode. 0 = Enables LDO 1 = Disables LDO
27	SDDIV	Shutdown VCO Divider	Sets Shutdown VCO Divider mode. 0 = Enables VCO Divider 1 = Disables VCO Divider
26	SDREF	Shutdown Reference Input	Sets Shutdown Reference input mode. 0 = Enables Reference Input 1 = Disables Reference Input
25:24	BS[9:8]	Band-Select MSBs	Sets Band-Select clock divider MSBs. See bits[19:12].
23	FB	VCO Feedback Mode	Sets VCO to N counter feedback mode. 0 = Divided 1 = Fundamental
22:20	DIVA[2:0]	RFOUT_ Output Divider Mode	Sets RFOUT_ output divider mode. Double buffered by register 0 when REG4DB = 1. 000 = Divide by 1, if 3000MHz ≤ f_{RFOUTA} ≤ 6000MHz 001 = Divide by 2, if 1500MHz ≤ f_{RFOUTA} < 3000MHz 010 = Divide by 4, if 750MHz ≤ f_{RFOUTA} < 1500MHz 011 = Divide by 8, if 375MHz ≤ f_{RFOUTA} < 750MHz 100 = Divide by 16, if 187.5MHz ≤ f_{RFOUTA} < 375MHz 101 = Divide by 32, if 93.75MHz ≤ f_{RFOUTA} < 187.5MHz 110 = Divide by 64, if 46.875MHz ≤ f_{RFOUTA} < 93.75MHz 111 = Divide by 128, if 23.5MHz ≤ f_{RFOUTA} < 46.875MHz
19:12	BS[7:0]	Band Select	Sets band select clock divider value. MSB are located in bits [25:24]. 0000000000 = Reserved 0000000001 =1 0000000010 = 2 ---- 1111111111 = 1023
11	SDVCO	VCO Shutdown	Sets VCO Shutdown mode. 0 = Enables VCO 1 = Disables VCO
10	MTLD	RFOUT Mute until Lock Detect	Sets RFOUT Mute until Lock Detect Mode 0 = Disables RFOUT Mute until Lock Detect Mode 1 = Enables RFOUT Mute until Lock Detect Mode
9	BDIV	RFOUTB Output Path Select	Sets RFOUTB output path select. 0 = VCO divided output 1 = VCO fundamental frequency
8	RFB_EN	RFOUTB Output Mode	Sets RFOUTB output mode. 0 = Disabled 1 = Enabled
7:6	BPWR[1:0]	RFOUTB Output Power	Sets RFOUTB single-ended output power. See the *RFOUTA± and RFOUTB±* section. 00 = -4dBm 01 = -1dBm 10 = +2dBm 11 = +5dBm

Table 7. Register 4 (Address: 100, Default: 6180B23C$_{HEX}$) (continued)

BIT LOCATION	BIT ID	NAME	DEFINITION
5	RFA_EN	RFOUTA Output Mode	Sets RFOUTA output mode. 0 = Disabled 1 = Enabled
4:3	APWR[1:0]	RFOUTA Output Power	Sets RFOUTA single-ended output power. See the *RFOUTA± and RFOUTB±* section. 00 = -4dBm 01 = -1dBm 10 = +2dBm 11 = +5dBm
2:0	C[2:0]	Register Address	Control Register address bits

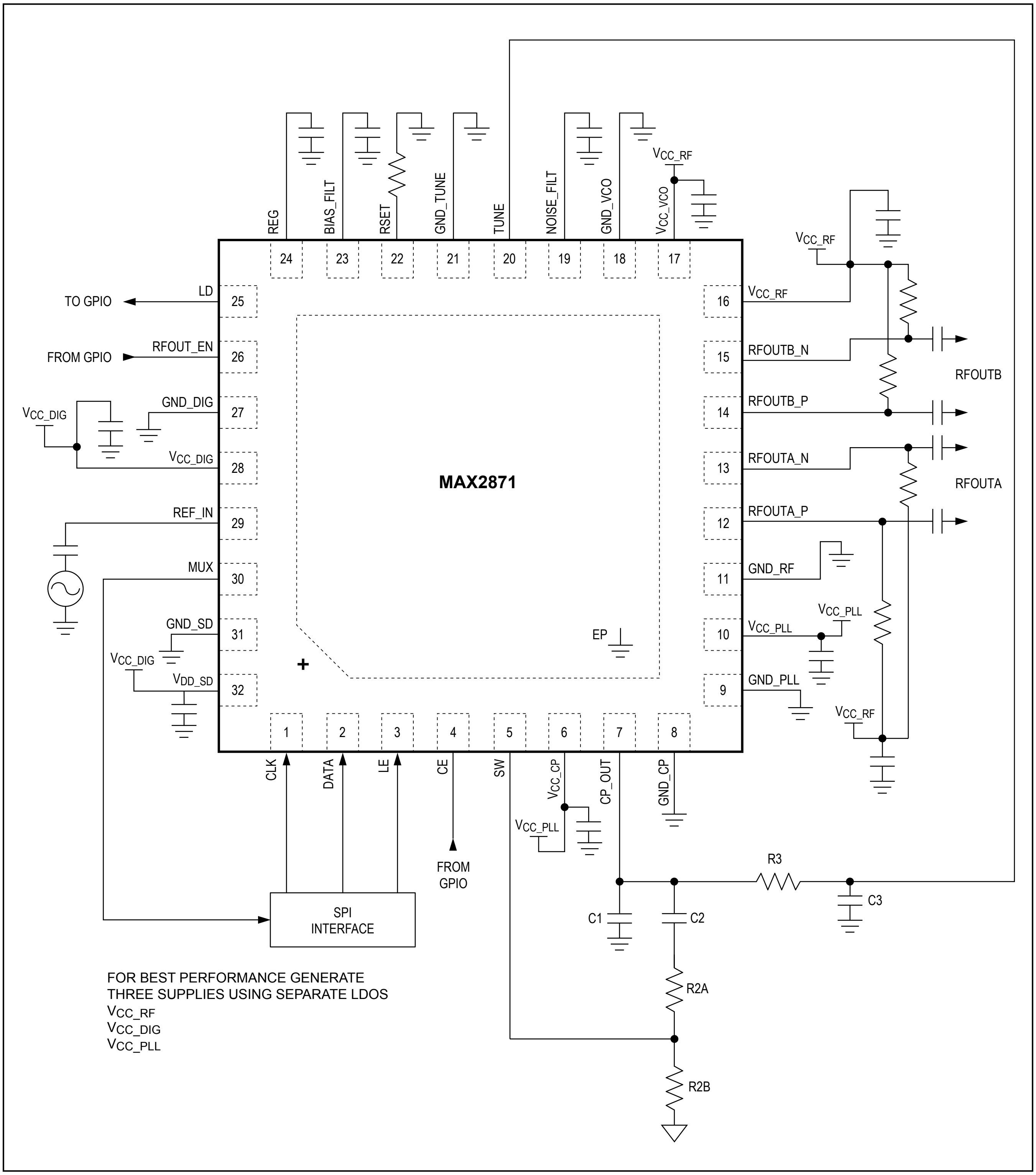
Table 8. Register 5 (Address: 101, Default: 00400005$_{HEX}$)

BIT LOCATION	BIT ID	NAME	DEFINITION
31:26	Reserved	Reserved	Reserved .Program to 011000.
25	SDPLL	Shutdown PLL	Sets Shutdown PLL mode. 0 = Enables PLL 1 = Disables PLL
24	F01	F01	Sets integer mode for F = 0. 0 = If F[11:0] = 0, then fractional-N mode is set 1 = If F[11:0] = 0, then integer-N mode is auto set
23:22	LD[1:0]	Lock-Detect Pin Function	Sets lock-detect pin function. 00 = Low 01 = Digital lock detect 10 = Analog lock detect 11 = High
21:19	Reserved	Reserved	Reserved. Program to 000.
18	MUX[3]	MUX MSB	Sets mode at MUX pin (see register 2 [28:26])
17:7	Reserved	Reserved	Reserved. Program to 00000000000.
6	ADCS	ADC Start	Sets ADC Start mode. 0 = ADC normal operation 1 = Start ADC conversion process
5:3	ADCM[2:0]	ADC Mode	Sets ADC mode. 000 = Disabled 001 = Temperature sensor 010 = Reserved 011 = Reserved 100 = Tune pin 101 = Reserved 110 = Reserved 111 = Reserved
2:0	ADDR[2:0]	Register Address	Control Register address bits

Table 9. Register 6 (Read-Only Register)

BIT LOCATION	BIT ID	NAME	DEFINITION
31:28	DIE[3:0]	Die ID	Die ID. 0110 = MAX2870 0111 = MAX2871
27:24	Reserved	Reserved	Reserved.
23	POR	Power On Reset	Power-On-Reset 0 = Power has not been cycled since last read 1 = Power has not been cycled since last read. All registers have been reset to default values.
22:16	ADC[6:0]	ADC Code	ADC Code.
15	ADCV	ADC Valid	Determines ADC code validity. 0 = Invalid ADC code 1 = Valid ADC code
14:10	Reserved	Reserved	Reserved.
9	VASA	VAS Active	Determines if VAS is Active. 0 = VCO Autoselect complete 1 = VCO Autoselect searching for correct VCO
8:3	V[5:0]	Current VCO	Current VCO.
2:0	ADDR[2:0]	Register Address	Control Register address bits.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2871ETJ+	-40°C to +85°C	32 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+5	21-0140	90-0013

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—