



# Microcontroller Overview

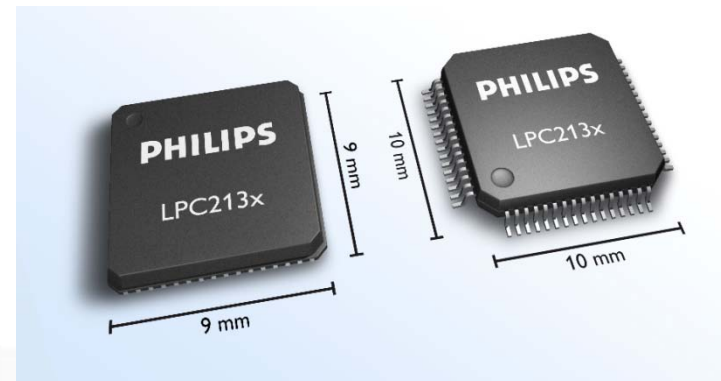


# LPC213x Series Overview

ARM

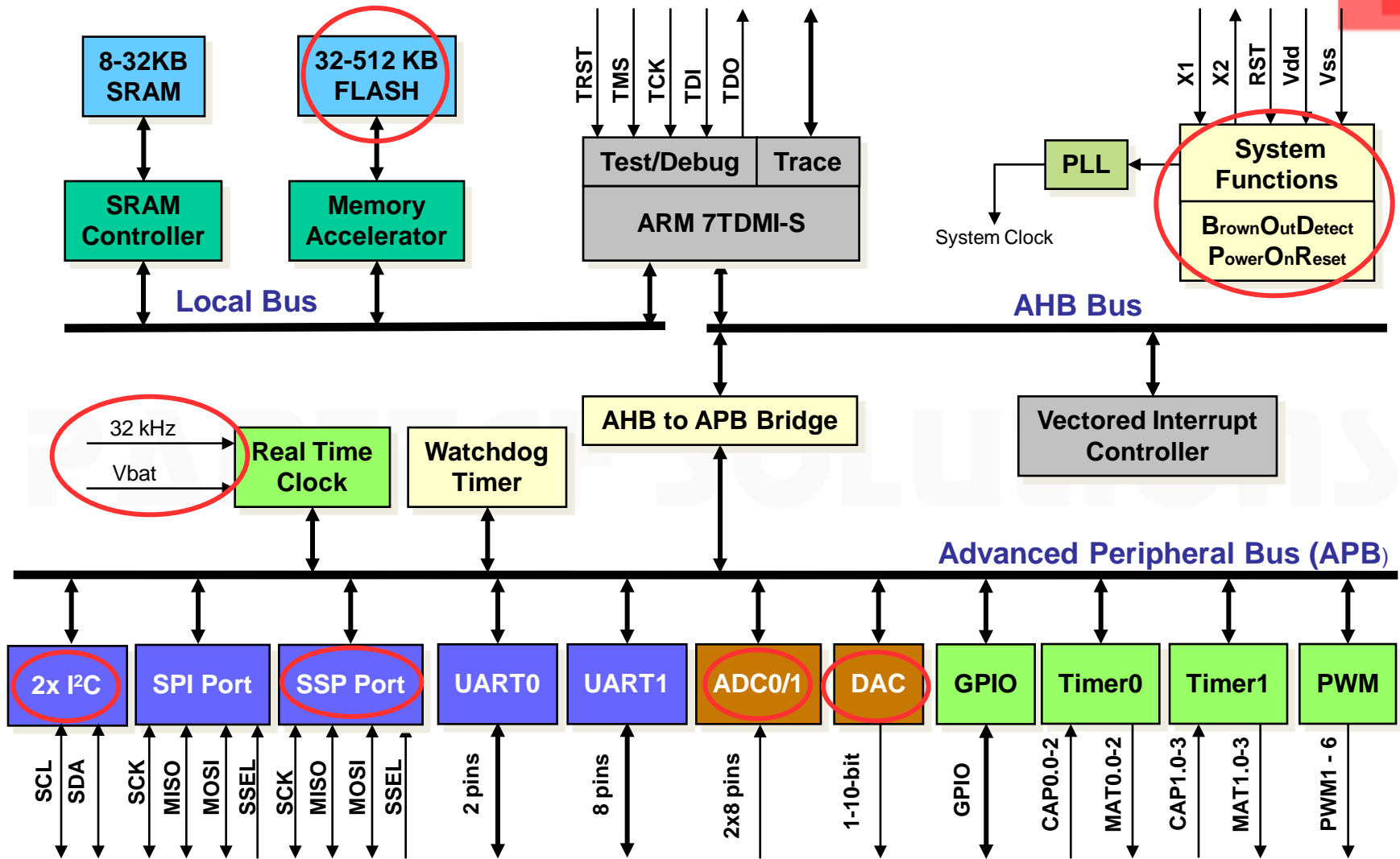


- ▶ 60 MHz Operation (54MIPS)  
from both on-chip Flash and SRAM
- ▶ 2 I2C, 2 UARTs, 1 SPI, 1 SPI/ SSP
- ▶ Two 8-ch 10-bit ADCs
- ▶ One 10-bit DAC
- ▶ 4 Timers (Capture/Match/PWM/WDT)
- ▶ 47 I/O pins (5V tolerant)
- ▶ 3.3V Single-Voltage Supply
- ▶ 32KHz RTC, BOD, POR
- ▶ User-code security
- ▶ Real-time Debugging & Trace
- ▶ ISP, IAP, Parallel Programmer Support
- ▶ Tiny Packages: QFP64 (10 x 10 x 1.4 mm), HVQFN64 (9 x 9 x 0.85 mm)



	Flash	SRAM	ADC	DAC	Pkg
<b>LPC2131</b>	32KB	8KB	1		QFP64
<b>LPC2132</b>	64KB	16KB	1	1	QFP64 QFN64
<b>LPC2134</b>	128KB	16KB	2	1	QFP64
<b>LPC2136</b>	256KB	32KB	2	1	QFP64
<b>LPC2138</b>	512KB	32KB	2	1	QFP64 QFN64

# LPC2131/32/34/36/38 Block Diagram



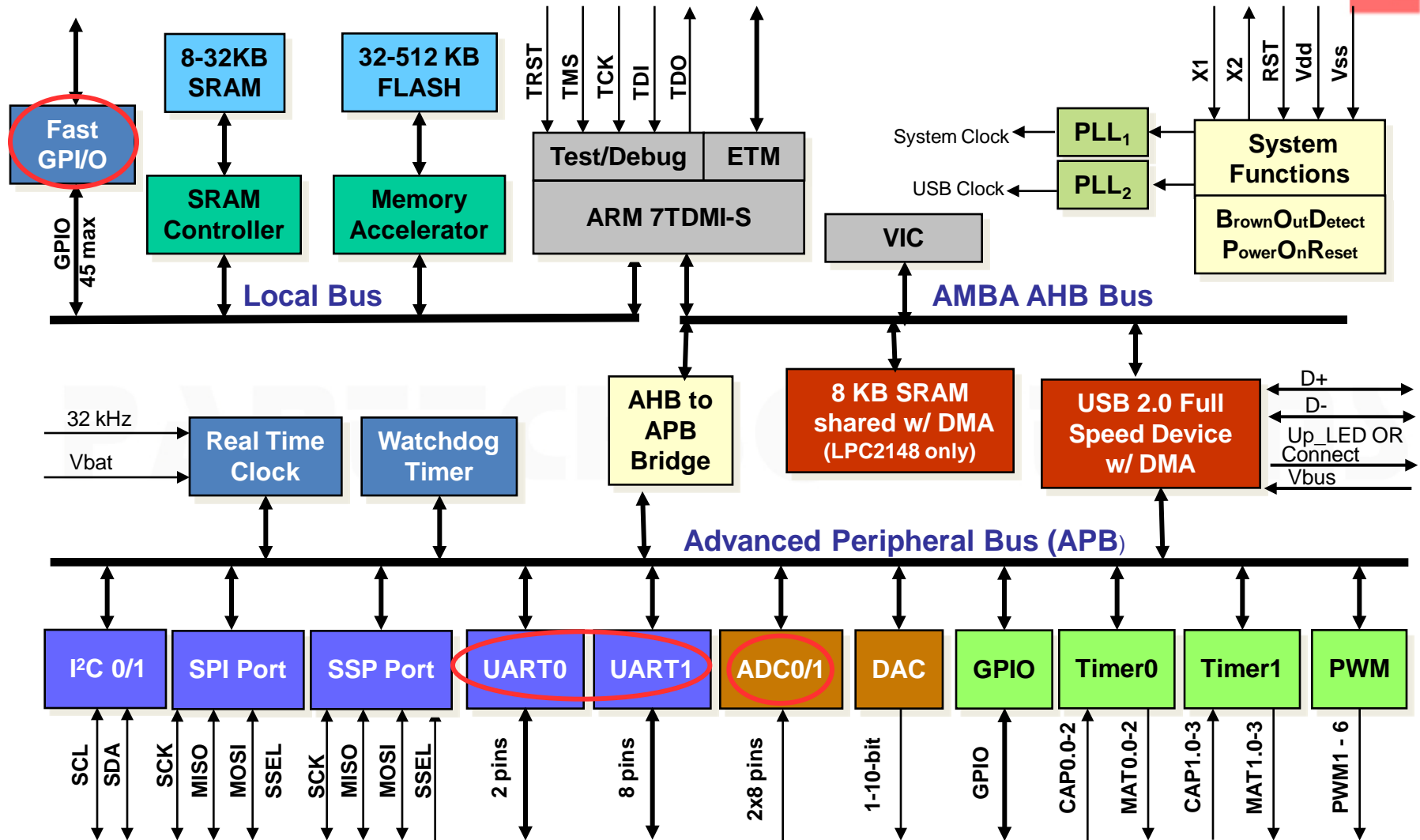


- ▶ Same device features as LPC213x
- ▶ USB 2.0 device
- ▶ Fast GPIO's
- ▶ ADC improvements
- ▶ Enhanced UART



# LPC2141/42/44/46/48 Block Diagram

64-pin LQFP





1. **Memory Addressing**
2. System Control Block
3. General Purpose I/O / Pin Connect Block
4. Vectored Interrupt Controller
5. Integrated Peripherals

Timer 0 / Timer 1, UART 0 / UART 1, I<sup>2</sup>C, SPI, PWM, RTC, Watchdog, ADC, USB, CAN, Ethernet, SD, IIS, GPDMA

# LPC2000 Memory Map



4.0 GB	AHB Peripherals	0xFFFF FFFF 0xF000 0000
3.75 GB	VPB Peripherals	0xEFFF FFFF 0xE000 0000
3.5 GB		
	Reserved for External Memory	
3.0 GB		0x8000 0000
2.0 GB	Boot Block (re-mapped from On-Chip Flash)	0x7FFF E000
	16 KB On-Chip Static RAM, USB	0x7FE0 0000
	16 KB On-Chip Static RAM, ETHERNET	0x7FD0 0000
	Reserved for On-Chip Memory	
	16 / 32 / 64 KB On-Chip Static RAM	0x4000 nnnn* 0x4000 0000
		0x3FFF FFFF
1.0 GB		
	Reserved for On-Chip Memory	
0.0 GB	8KB ... 1MB On-Chip Non-Volatile Memory	0x000m FFFF 0x0000 0000

Memory blocks not drawn to scale!

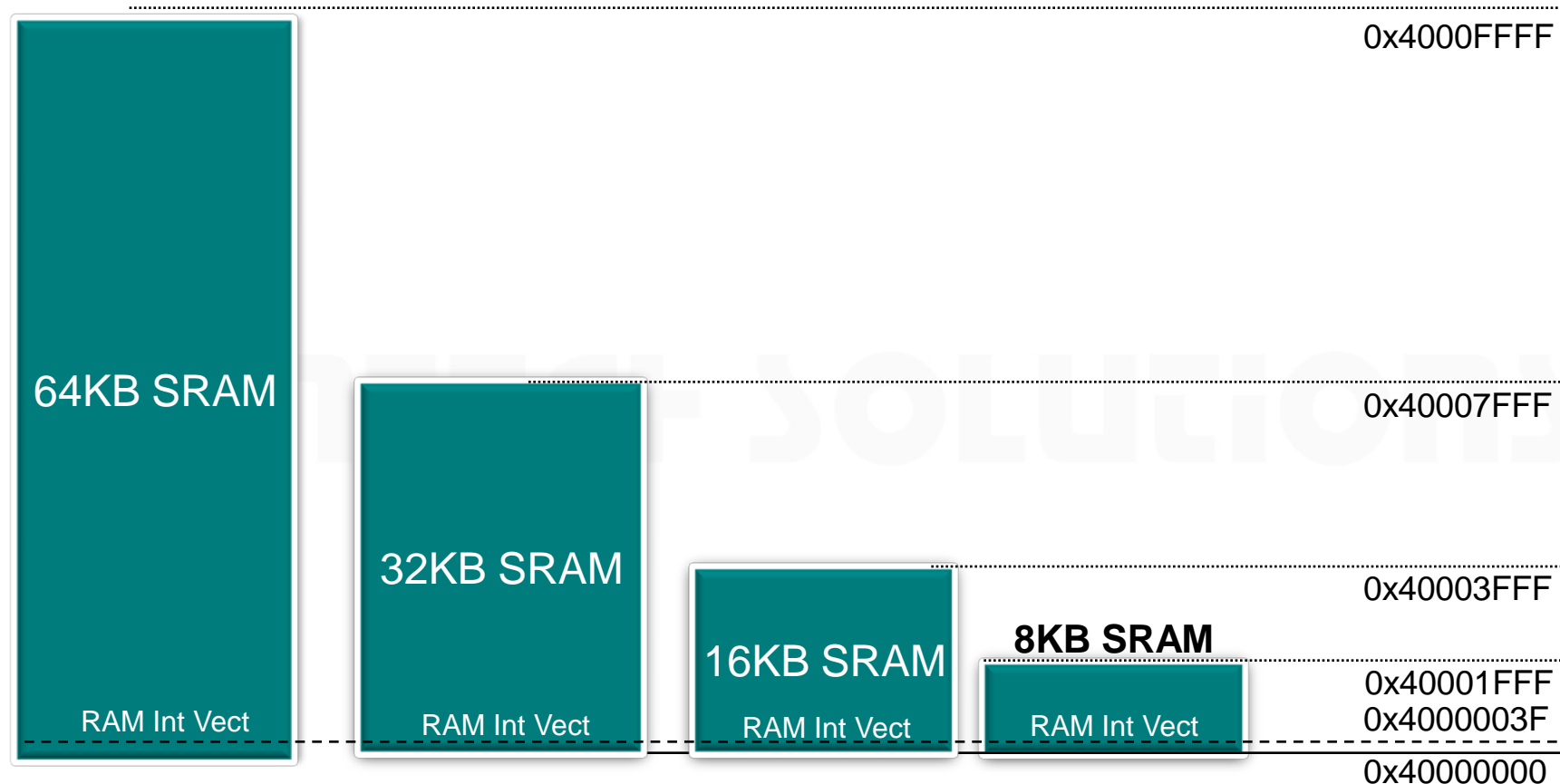
RAM on AHB

RAM on local bus  
-> fast access !

Not valid for LPC2888/0



# SRAM: 8, 16, 32 or 64 KB







## ▶ Vector Table

	⋮
0x1C	<b>FIQ</b>
0x18	<b>IRQ</b>
0x14	<b>(Reserved)</b>
0x10	<b>Data Abort</b>
0x0C	<b>Prefetch Abort</b>
0x08	<b>Software Interrupt</b>
0x04	<b>Undefined Instruction</b>
0x00	<b>Reset</b>

Valid user program key:  
Must contain a value that  
ensures that the checksum  
of all vectors is zero



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- ▶ Includes a number of important system features
  - Power Control
  - Memory mapping configuration
  - Oscillator
  - PLL
  - VPB (VLSI Peripheral Bus) divider
  - Reset (active low)
  - Wakeup Timer
  - External Interrupts



- Power Control Register [PCON – 0xE01FC0C0] R/W

PCON[0]	IDL	Idle mode - processor clock stopped, on-chip peripherals remain active, interrupts cause wakeup
PCON[1]	PD	Power Down mode - oscillator and on-chip clocks stopped, wakeup by external interrupt

20 uA at room temperature,  
50 uA with single voltage supply

For example 5 mA with most peripherals powered down

**Biggest factors:**  
temperature, clock rates  
Peripheral Clock Divider: 20%

- When disabled, peripherals are switched off to conserve power

- Power Control for  
Peripherals Register

[PCONP – 0xE01FC0C4]

R/W

PCONP 1	PCTIM0	Enable Timer0
PCONP 2	PCTIM1	Enable Timer1
PCONP 3	PCURT0	Enable UART0
PCONP 4	PCURT1	Enable UART1
PCONP 5	PCPWM0	Enable PWM0
PCONP 7	PCI2C	Enable I2C
PCONP 8	PCSPI	Enable SPI
PCONP 9	PCRTC	Enable RTC
.....		

Each peripheral  
typically below 1mA



- Power Control for Peripherals Register cont'd

...		
PCONP 8	PCSP0	Enable SPI0
PCONP 9	PCRTC	Enable RTC
PCONP 10	PCSPI1	Enable SPI1
PCONP 11	PCEMC	Enable External Memory Controller
PCONP 12	PCAD	Enable A/D-Converter
PCONP 13	PCCAN1	Enable CAN Controller 1
PCONP 14	PCCAN2	Enable CAN Controller 2
PCONP 15	PCCAN3	Enable CAN Controller 3
PCONP 16	PCCAN4	Enable CAN Controller 4

Acceptance Filter  
enabled with any  
CAN Controller

CAN peripheral  
typically below 2mA



## ► Re-mapping of **Exception Vectors**

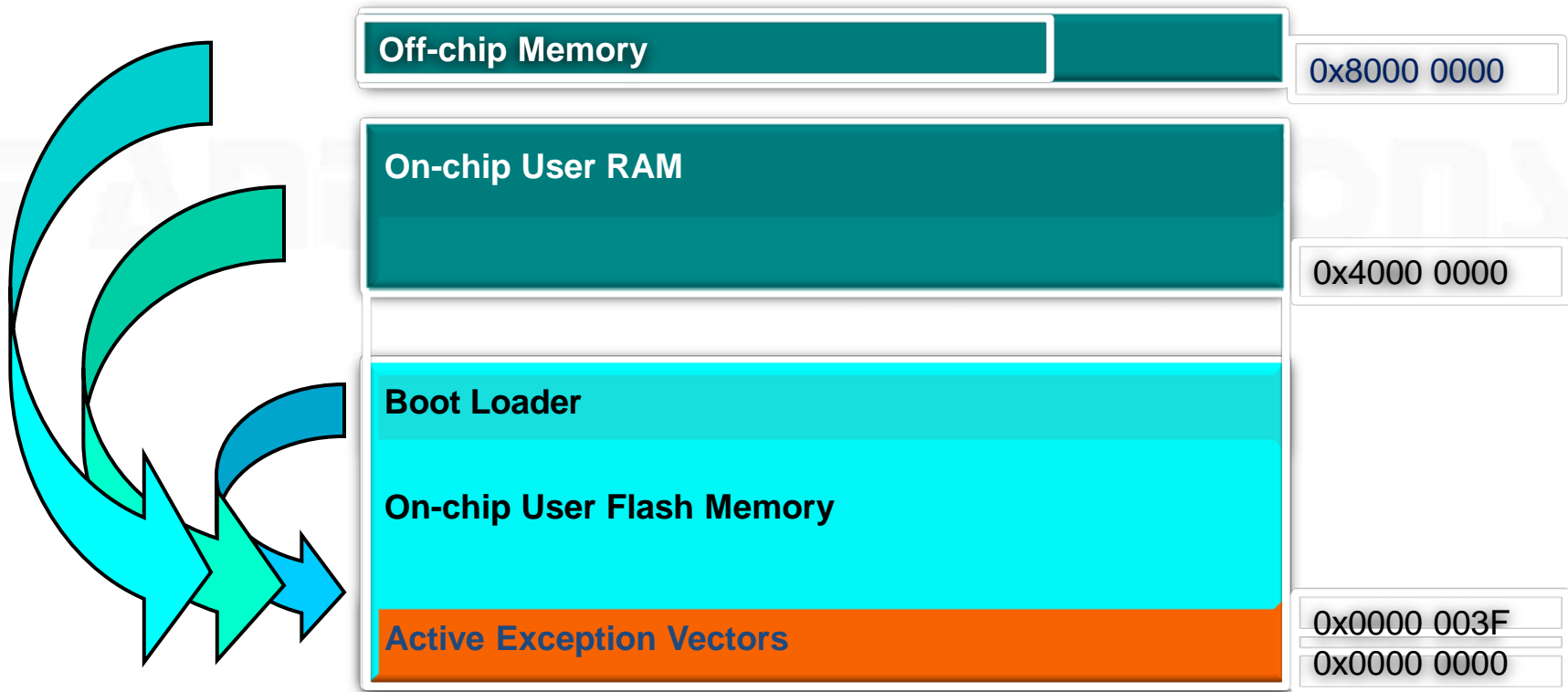
- always appear to begin at 0x0000 0000
- but can be mapped from different sources:
  - User Flash
    - **Exception Vectors** are **not** re-mapped and reside in Flash



# Memory Mapping Control (2)

ARM

- Boot Loader
  - Always executed after reset. **Exception Vectors** re-mapped from Boot Block
- User RAM
  - **Exception Vectors** are re-mapped from RAM

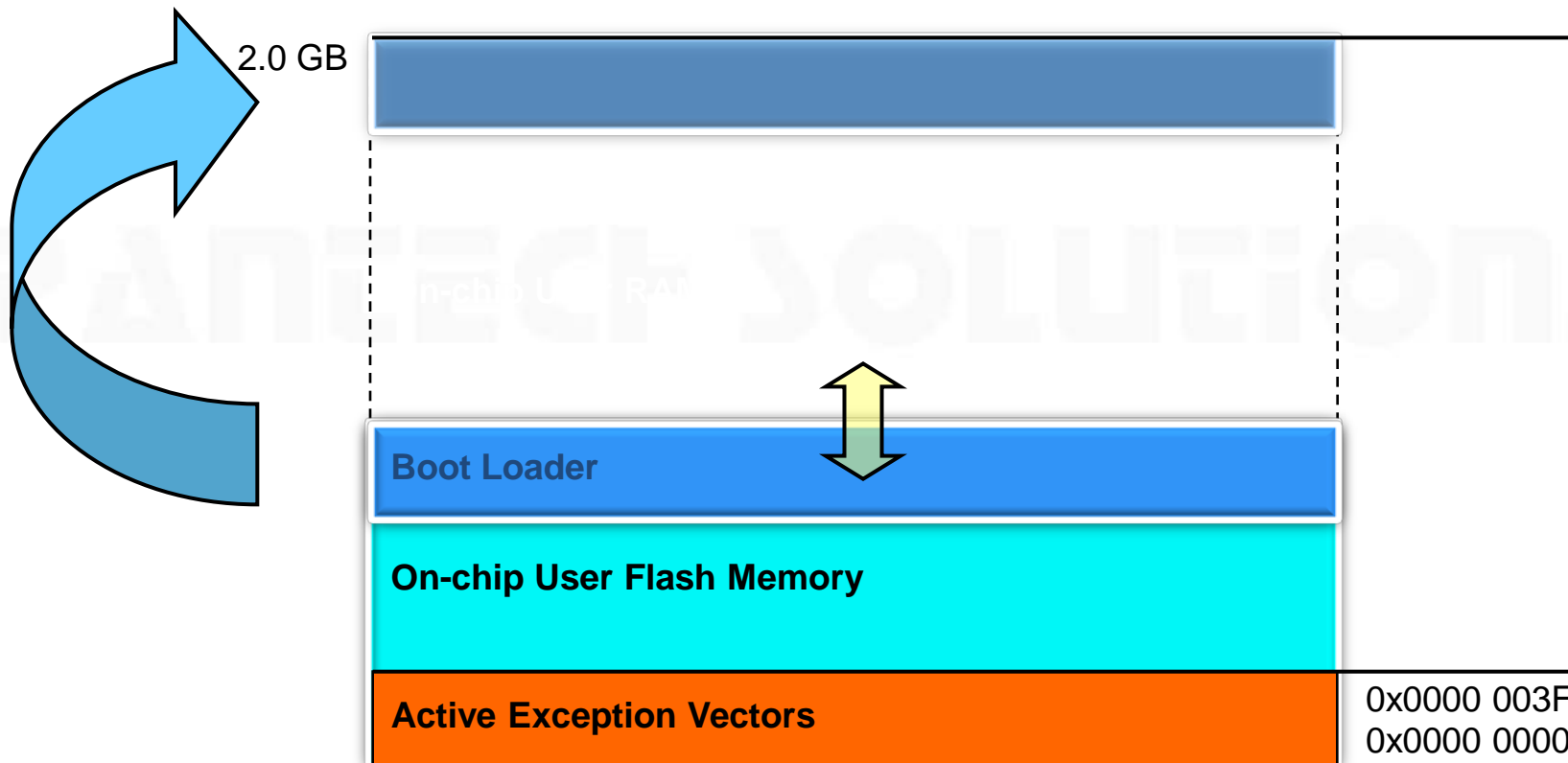






## ► Re-mapping of **Boot Block**

- mapped from top of Flash to top of on-chip memory space





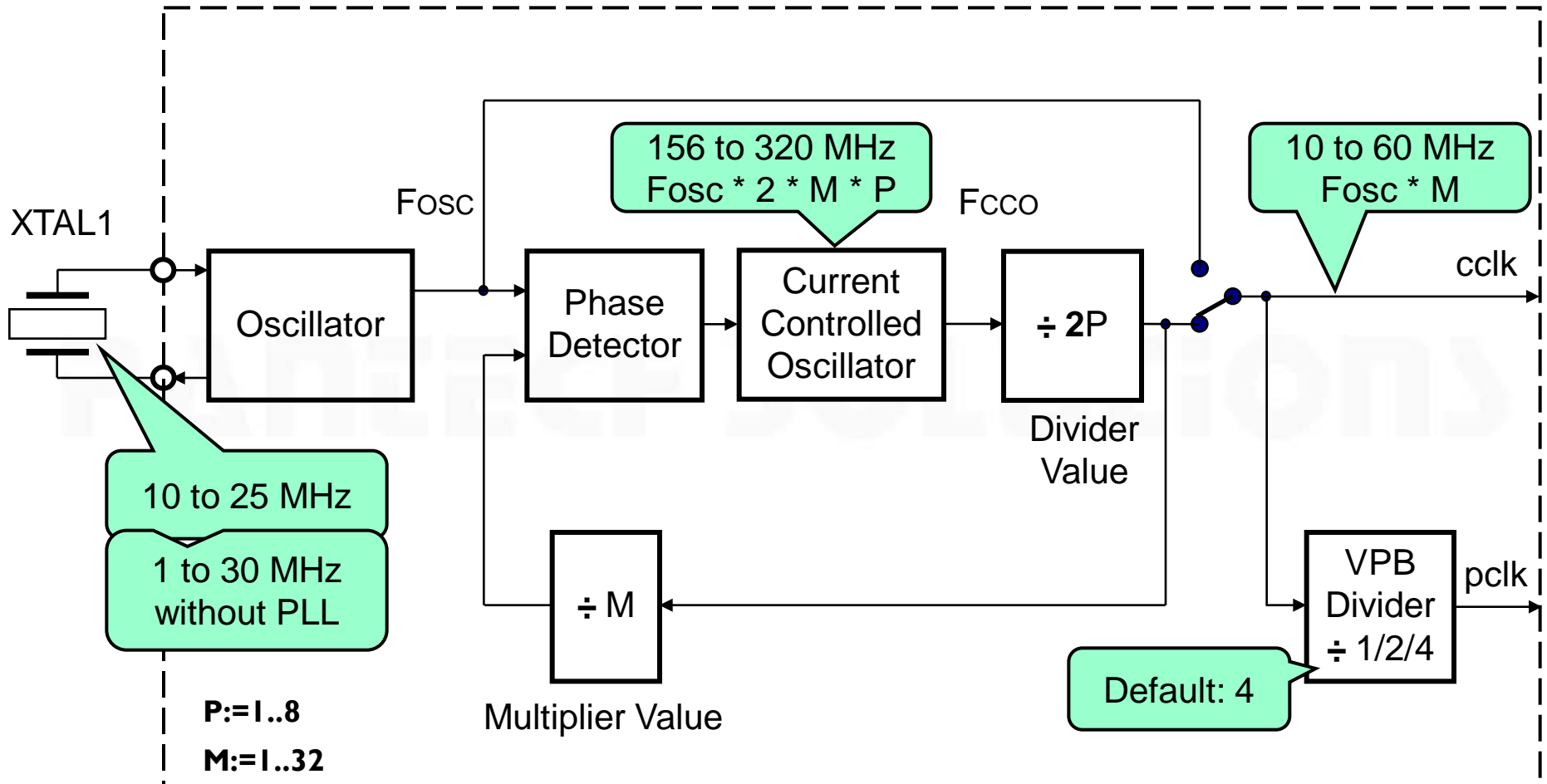
- Memory Mapping Control [MEMMAP – 0xE01FC040] R/W

MEMMAP 1:0	MAP 1:0	
		00: Boot Loader Mode
		01: User Flash Mode (no re-mapping)
		10: User RAM Mode
		11: External Memory

Selects the memory being mapped to address zero



- ▶ 10 to 25 MHz input clock frequency
- ▶ Output frequency from 10 MHz up to the max.
- ▶ PLL bypassed on reset
- ▶ PLL lock indicator can be used as an interrupt to connect the PLL once it is locked
- ▶ PLL programming requires a special feed sequence (like the watchdog) for safety





- ▶ Pins available for GPIO:

- ▶ LPC21xx/22xx

- 48-pin devices: 32
- 64-pin devices: 46
- 144 pin devices: 76 (max.) (with external memory)  
112 (w/o external memory)

- ▶ LPC23xx/24xx

- Up to 160 GPIO pins, all implemented as fast GPIOs, with 64 GPIO interrupts (plus 4 other external interrupts).

- ▶ Shared with

- Alternate functions of all peripherals
- Data/address bus and strobe signals for external memories



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Timer 0 / Timer 1, UART 0 / UART 1, I<sup>2</sup>C, SPI, PWM, RTC, Watchdog, Ethernet, SD, IIS, GPDMA



- ▶ Direction control of individual bits
- ▶ Separate set and clear registers
- ▶ Pin value and output register can be read separately
- ▶ Slew rate controlled outputs (10 ns)
- ▶ 5 registers used to control I/Os



## Register

**IOPIN**

The current state of the port pins is read from this register

**IOSET**

Writing "1" sets pins **high**, writing "0" has no effect

**IOCLR**

Writing "1" sets pins **low** and clears corresponding bits in IOSET

Port pin direction: 0 = INPUT 1 = OUTPUT

**IODIR**

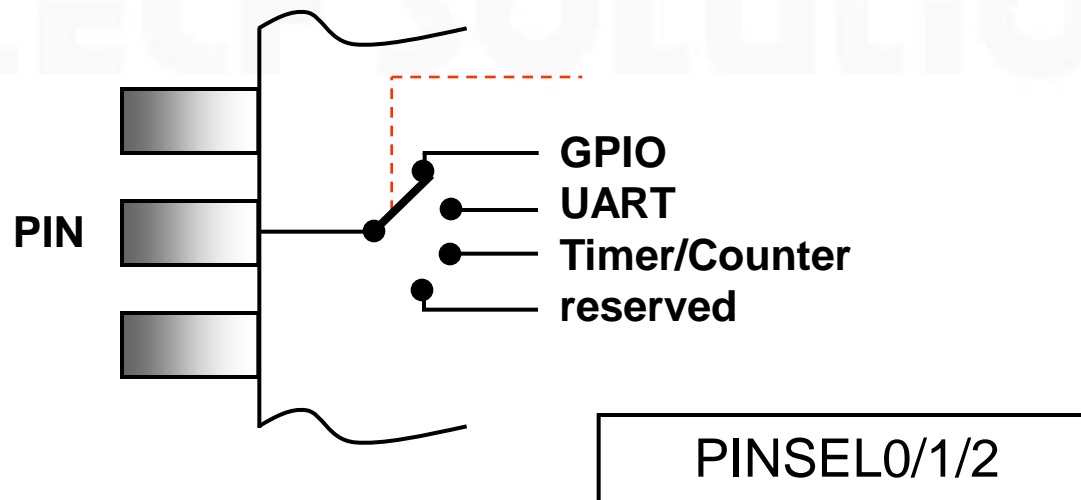
Selects function of pins (Pin Connect Block)

**PINSEL0/1**





- ▶ Many on-chip functions can use I/O pins
- ▶ Number of I/O-pins is limited
  - ⇒ I/Os can be configured to adapt various functions
- ▶ Configuration done by **Pin Connect Block**





## ► Pin Function Select Registers

### – PINSEL0 and PINSEL1

- Configuration of **P0**
- Assign P0.0 ... P0.31 to GPIO or an alternate function (1 of max. 3)

### – PINSEL2 **(not available in 48-pin devices)**

- Configuration of **P1** (64/144-pin devices) and **P2, P3** (144-pin devices)
- Select availability of debug and trace ports on Port1 pins
- Controls use of address/data bus and strobe pins (144-pin devices)
- Selection of additional ADC-inputs (144-pin devices)



## Example:

- Pin Function Select Register 0 [PINSEL0 - 0xE002C000] R/W

...	...	...
PINSEL0 21:20	P0.10	00: GPIO Port 0.10 01: RTS (UART1) 10: Capture 1.0 (Timer 1) 11: reserved
...	...	...



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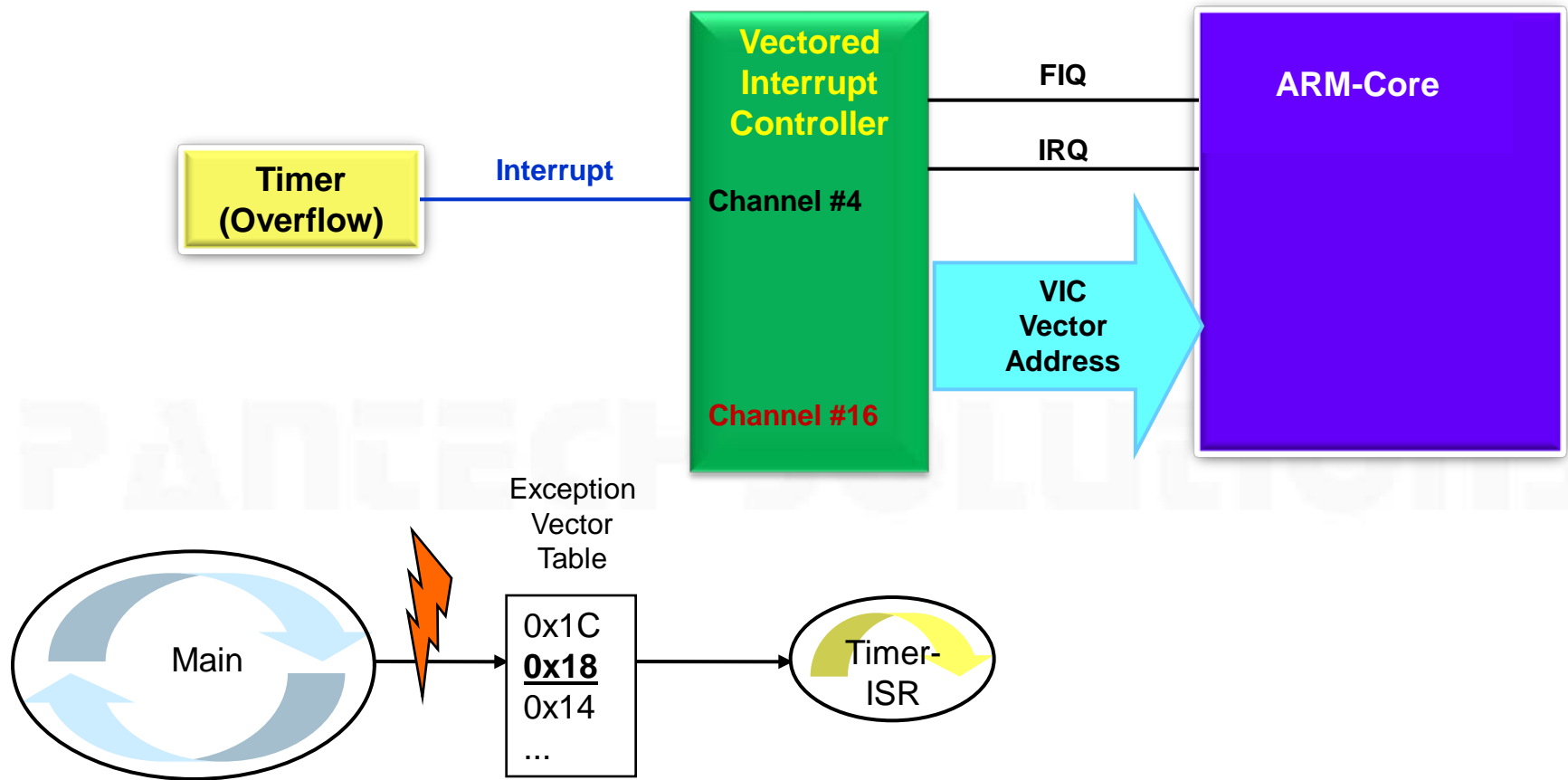
Timer 0 / Timer 1, UART 0 / UART 1, I<sup>2</sup>C, SPI, PWM, RTC, Watchdog, Ethernet, SD, IIS, GPDMA



- ▶ ARM PrimeCell™
- ▶ 32 interrupt request inputs
- ▶ 16 IRQ interrupts can be auto-vectored
  - single instruction vectoring to ISR
  - dynamic software priority assignment
- ▶ 16 FIQ non-vectored interrupts
- ▶ Software interrupts

# IRQ Interrupts

ARM



**CONST** = 0x0FF for LPC21xx, and LPC22xx  
0x120 for LPC23xx, and LPC24xx



- ▶ FIQs have higher priority than IRQs
  - Serviced first
  - FIQs disable IRQs
  
- ▶ FIQ Vector is last in vector table (allows handler to be run sequentially from that address)
  
- ▶ FIQ mode has 5 extra banked registers, r8-12 (interrupt handlers must always preserve non-banked registers)



1. Memory Addressing
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5. **Integrated Peripherals**

Timer 0 / Timer 1, UART 0 / UART 1, I<sup>2</sup>C, SPI, PWM, RTC, Watchdog, Ethernet, SD, IIS, GPDMA



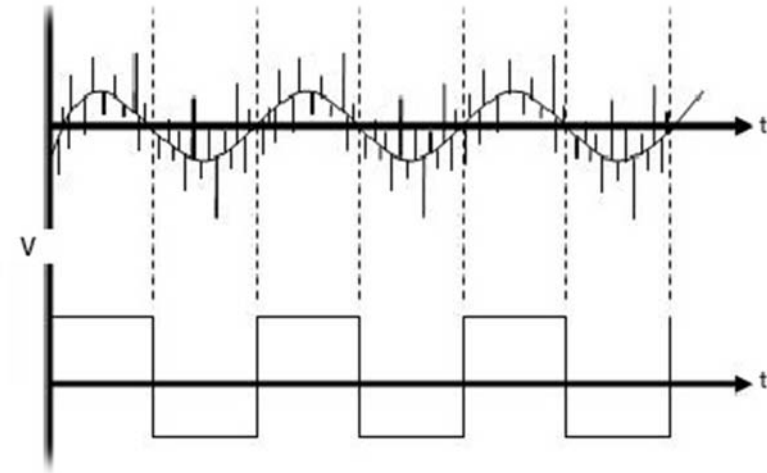


**ADC**



## Features

- 10 bit successive approximation analog to digital converter
- Multiplexed inputs
  - 4 pins (64-pin devices)
  - 8 pins (144-pin devices)
- Power down mode
- Measurement range 0V ... 3V
- Minimum 10 bit conversion time: 2.44  $\mu$ s
- Burst conversion mode for single or multiple inputs
- Optional conversion on transition on input pin or Timer Match signal
- Programmable divider to generate required 4.5MHz from VPB clock





- ▶ CLKS: bit 17, 18, 19 of ADCR select the number of clocks used per conversion and the accuracy
  - 000b: 11 clocks, 10 bits
  - 001b: 10 clocks, 9 bits
  - 010b: 9 clocks, 8 bits
  - 011b: 8 clocks, 7 bits
  - ...
  - 111b: 4 clocks, 3 bits

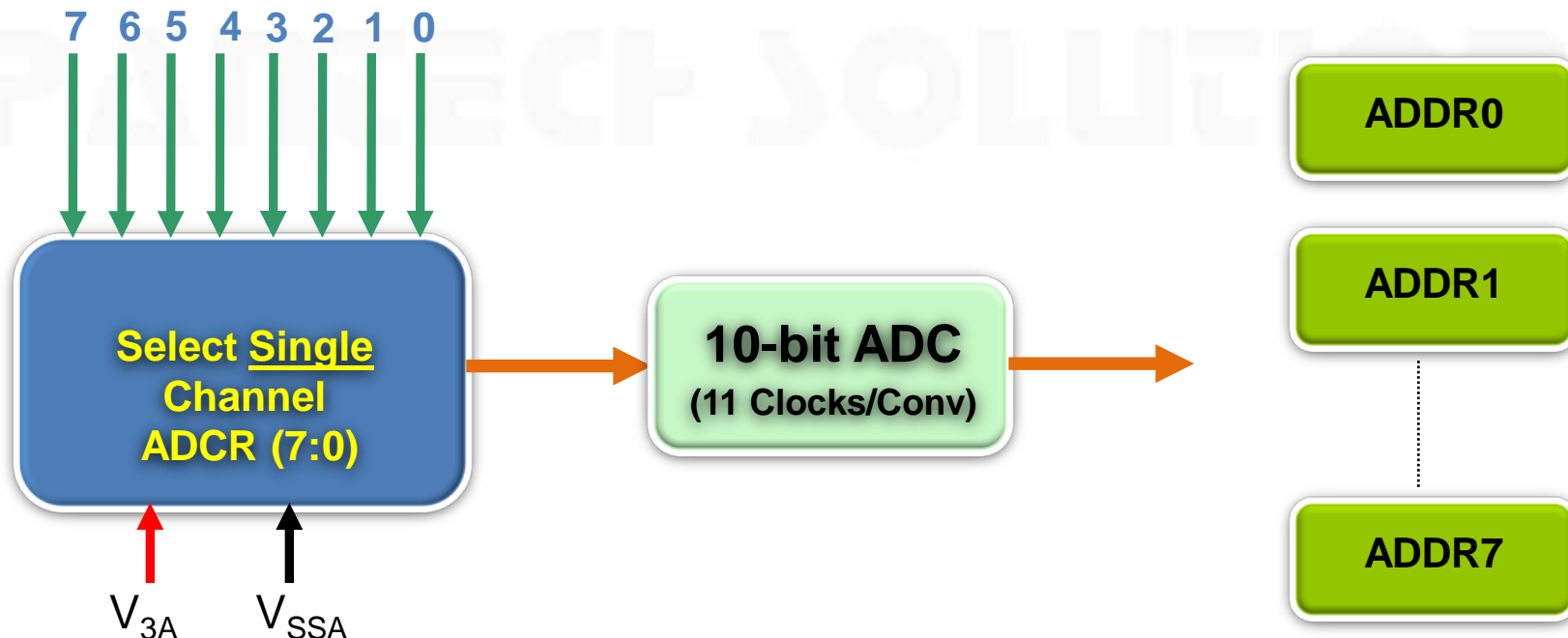


- ▶ Separate result register for each channel
  - Reduces the interrupt overhead by a factor of 8
- ▶ Measurement range of 0 V to 3 V
  - Separate voltage pins for analogue 3V supply (V3A) and analogue ground (VSSA)



- ▶ All conversions are 10-bit and take 11 clocks
- ▶ 4.5MHz Maximum Clock
- ▶ Allows conversion to start on an external edge

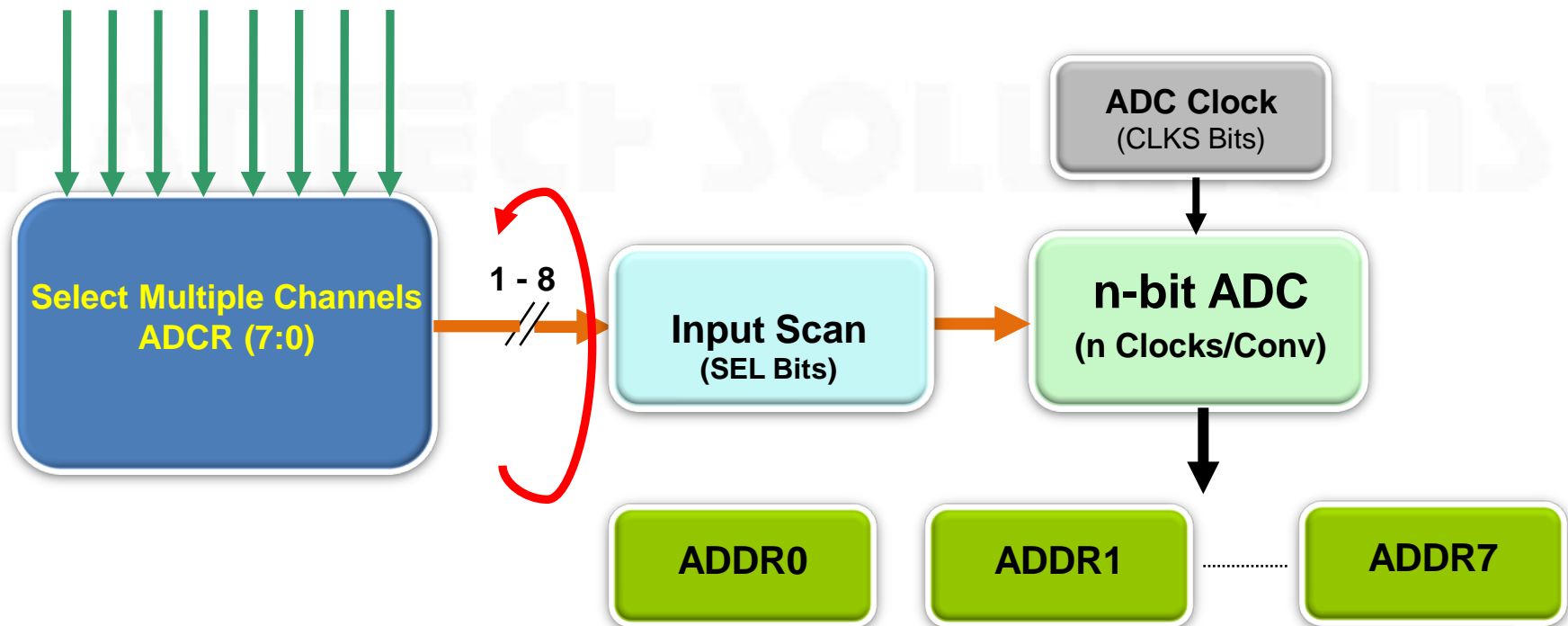
## ADC Inputs





- ▶ Result accuracy and speed are programmable
- ▶ Input selected by the SEL bits are scanned

## ADC Inputs

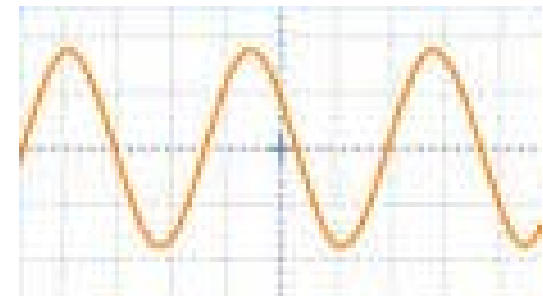




**DAC**



- Enables the device to generate a variable analog output
- 10-bit resolution DAC with a buffered output
  - Last output value is held as long as DAC is on
- Register string architecture
- Output from Zero Volt to Reference Voltage in 1024 steps
- Selectable Conversion speed vs. power
  - Settling time 1us, up to 350uA
  - Settling time 2.5us, up to 700uA
- Selective power down



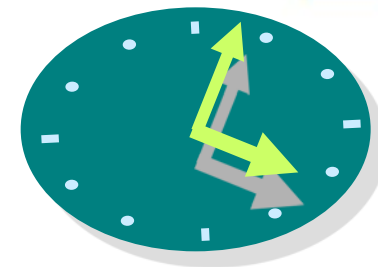


- 
- TIMERS
  - PWMs
  - RTC
  - WATCHDOG



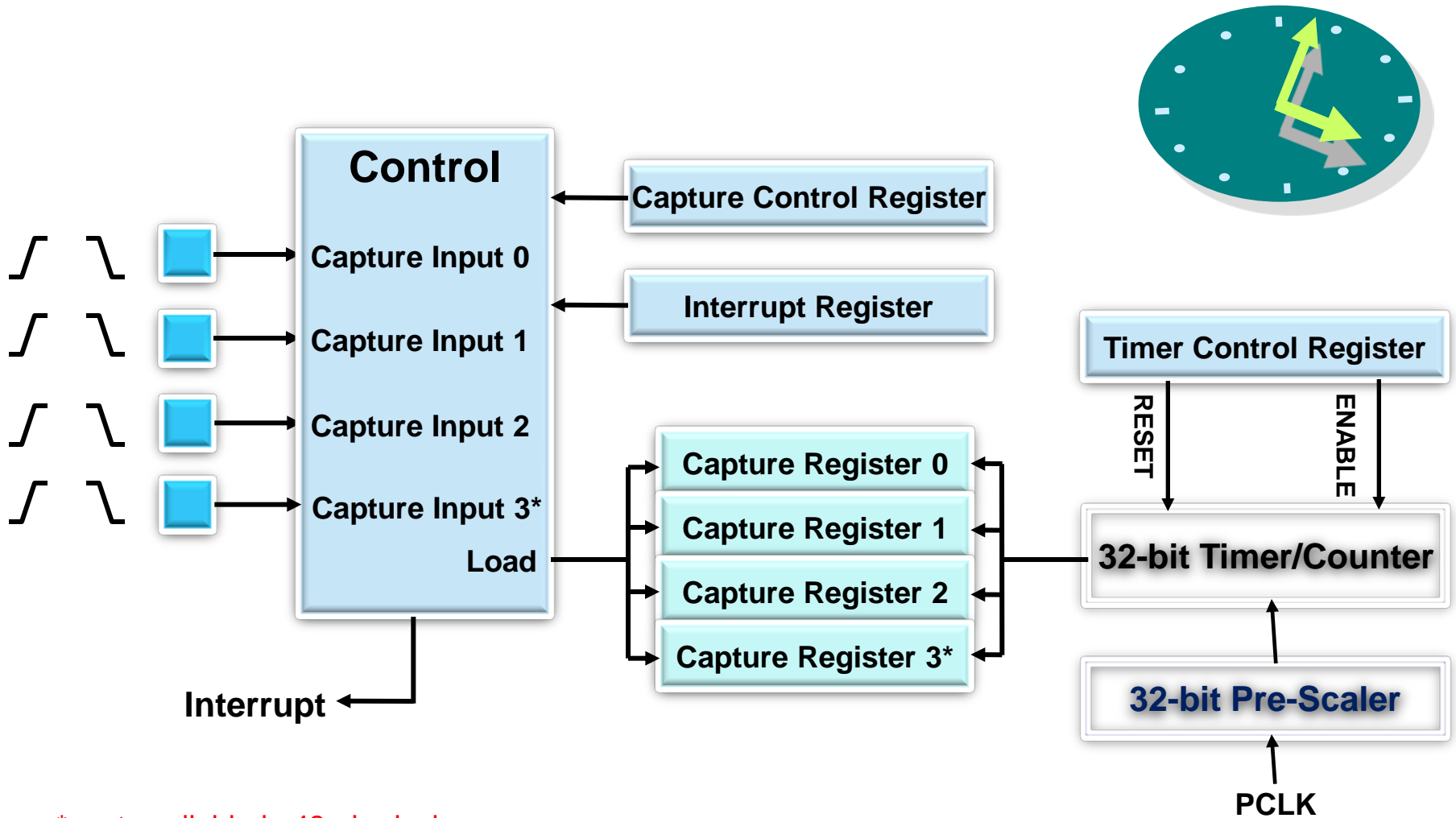
- ▶ Timer can be used to control the sequence of an event or process





- ▶ 32-bit Timer
- ▶ 32-bit Capture Registers and Capture Pins
  - Four on each timer (48-pin devices three on Timer 0 and four on Timer 1)
  - Capture event can optionally trigger an interrupt
- ▶ 32-bit Match Registers and Match Pins
  - Four on each timer (48-pin devices three on Timer 0 and four on Timer 1)
  - Interrupt, timer reset or timer halt on match
  - Match output can toggle, go high, go low or do nothing

# Timer Capture



\*: not available in 48-pin devices



- ▶ Dedicated 32-bit PWM timer
  - similar functionality to Timer0 / Timer1
- ▶ Three additional match registers for a total of 7
  - all PWM outputs have the same rate, which is programmable
  - allows up to 6 single edge controlled or 3 double edge controlled PWM outputs in any combination



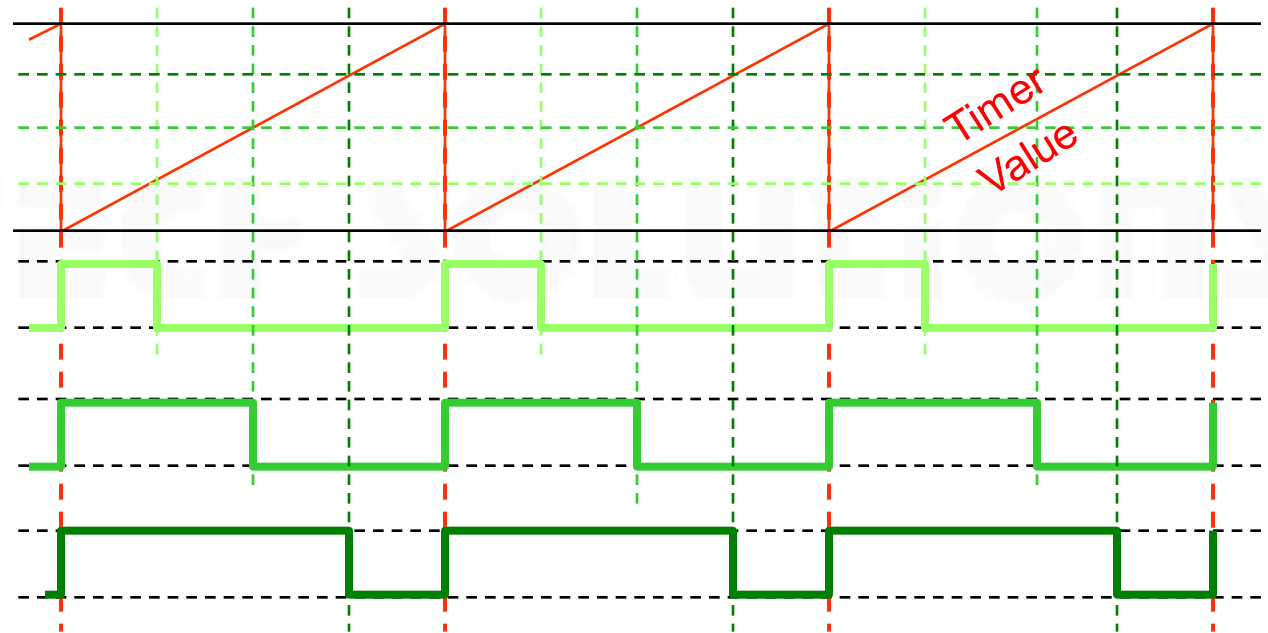
- ▶ PWM outputs all go high at the beginning of each cycle and go low on a Match

Match Register 0 Value  
Compare (Match) Value z  
Compare (Match) Value y  
Compare (Match) Value x  
0000 0000h

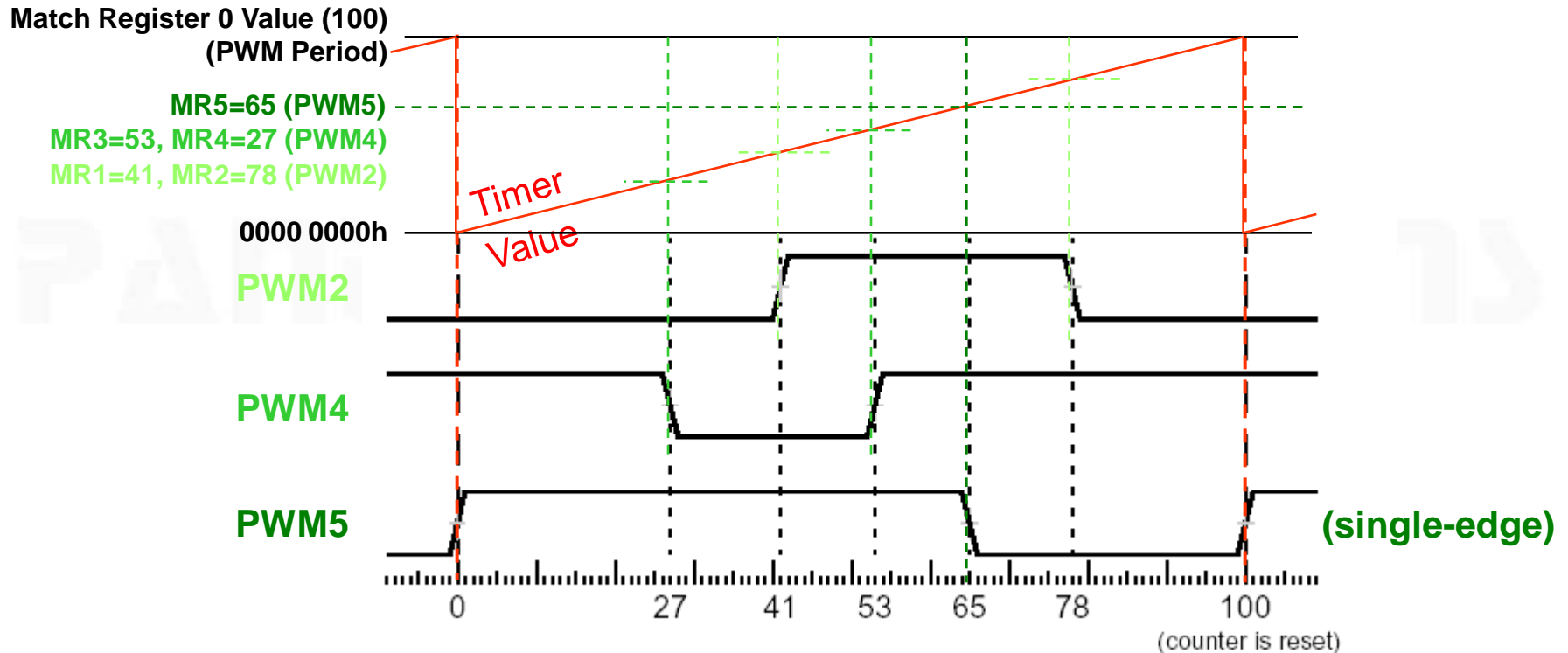
PWMx

PWMy

PWMz



- ▶ Double edge controlled PWM outputs can have either edge occur at any position within a cycle





## ► Full Clock/Calendar function with alarms

- Dedicated 32-bit timer with 32-bit pre-scaler
- Generates its own 32.768 kHz reference clock from any crystal frequency (Prescaler values need to be calculated)
- Counts seconds, minutes, hours, day of month, month, year, day of week and day of year
- Can generate an interrupt or set an alarm flag for any combination of the counters



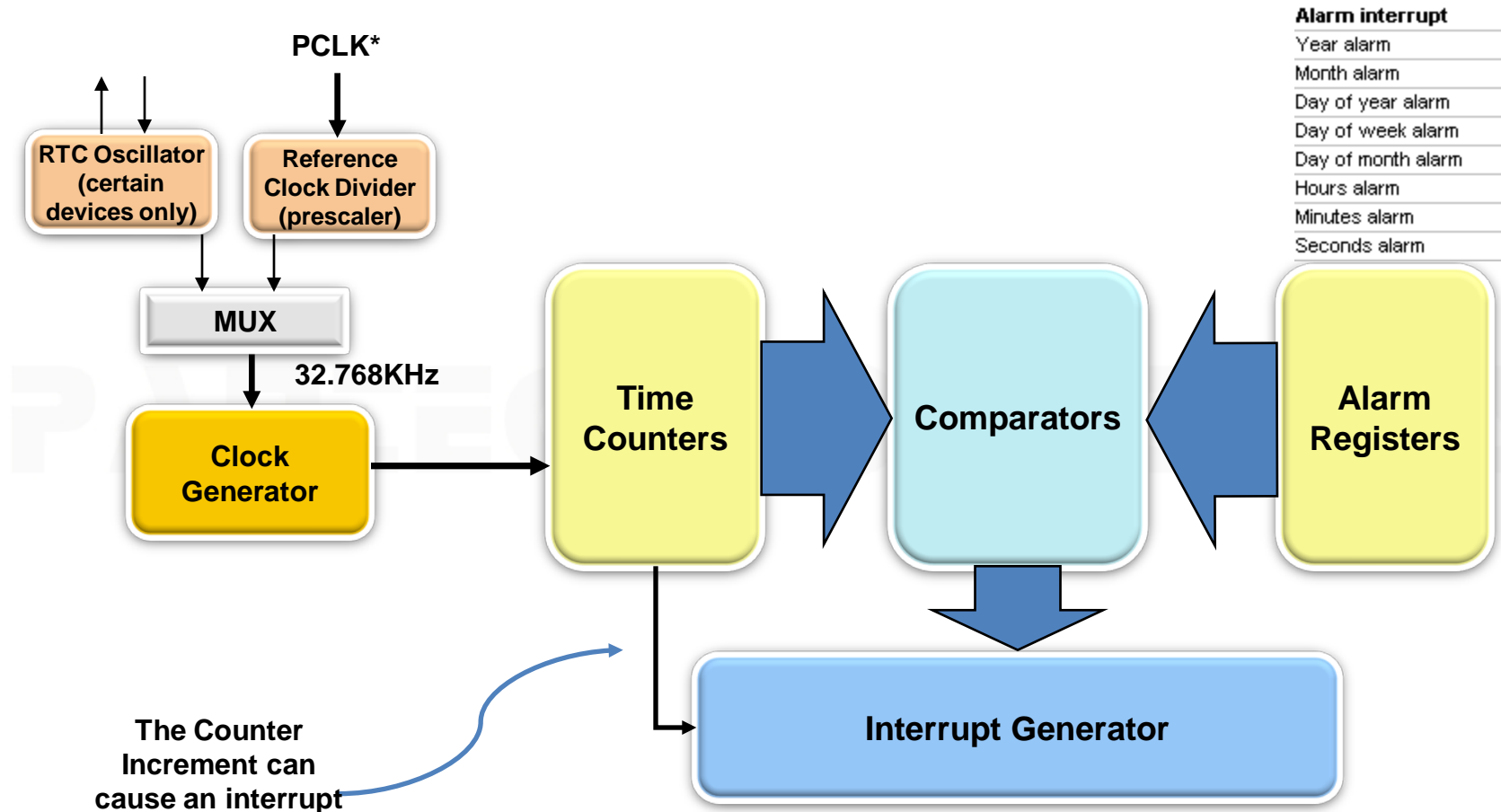


- ▶ Can be clocked by a separate 32.768KHz or by prescaler divider based on VPB clock
- => RTC can run in Power Down mode

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- ▶ Separate supply pin Vbat which can be connected to battery or to the 3.3V supply

# RTC Block Diagram



\* keep in mind what the settings are for PLL and the VPB Divider





- ▶ Once activated, the Watchdog will reset the entire chip if it is not fed regularly
- ▶ Feed is accomplished by a specific sequence of data writes
- ▶ Watchdog flag allows software to tell that a watchdog reset has occurred
- ▶ Selectable overflow time ( $\mu\text{s}$  ... minutes)
- ▶ Debug Mode generates an interrupt instead of a reset
- ▶ Secure: watchdog cannot be turned off once it is enabled
- ▶ Watchdog Timer value can be read in one cycle



## **Helpful hints and links**

# Microcontroller Web Site

www.nxp.com/microcontrollers

The screenshot shows the NXP Semiconductors Microcontrollers website as it appeared in the early 2000s, viewed through Microsoft Internet Explorer. The browser's address bar shows the URL <http://www.standardics.nxp.com/microcontrollers/>. The website features the NXP logo (founded by Philips) and a navigation menu with links to Home, About NXP, News, In Focus, Careers, Investors, Contact, and my.NXP. A breadcrumb trail indicates the path: Products > Microcontrollers. The main content area is titled 'Microcontrollers' and includes a 'Standard ICs' sidebar with links to Logic, PC, Interface, Microcontrollers (selected), Analog, and RF. The 'Microcontrollers' section has sub-links for Introduction, Highlights, Products, and Support. An image of a person working on a circuit board is displayed. Below the image, text describes the range of microcontrollers from 8-bit to 32-bit ARM, highlighting the LPC3000, LPC2000, LH7A, and LH7 families. The right sidebar contains search tools, a 'Standard ICs quick find' section, and a list of 'Standard ICs sections' including Product families & functions, Literature, Packaging, Support, Quality, and Contact. An 'Updates' section lists recent releases like the LPC954 MCU and updated sample code bundles.

NXP Semiconductors - Microcontrollers [Home] - Microsoft Internet Explorer

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**Microcontrollers**

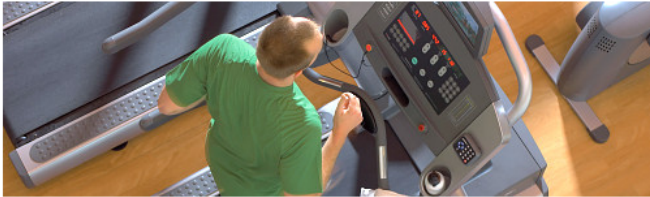
**Standard ICs:**

- Logic
- PC
- Interface
- Microcontrollers**
- Analog
- RF

**Microcontrollers**

- Introduction
- Highlights
- Products
- Support

**Introduction**



From the smallest 8-bit to the highest performing 32-bit ARM microcontrollers, we drive the industry as an innovation leader with our highly-integrated and cost-effective products. Our leading **LPC3000** and **LPC2000** ARM-based families have numerous, sophisticated integrated peripherals available. Our newest ARM-based **LH7A** and **LH7** families feature high-resolution integrated LCD controllers and

Select site: English

Type search here Search

Type # Cross-ref Site

Advanced search

Applications Looking for

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**Standard ICs sections**

- Product families & functions
- Literature brochures, leaflets, presentations
- Packaging specs & SOT #s
- Support manuals, models, FAQ, software, demoboard
- Quality handbook, markings
- Contact sales, distributors

**Updates**

- LPC954 MCU with 16KB flash
- Updated LPC23xx/LPC24xx sample code bundle 1.50
- LPC288x peripherals sample code V1.30
- Latest LH7(A) BlueStreak support documents



# Product Link



Products - Pantech Solution Pvt Ltd - Microsoft Internet Explorer

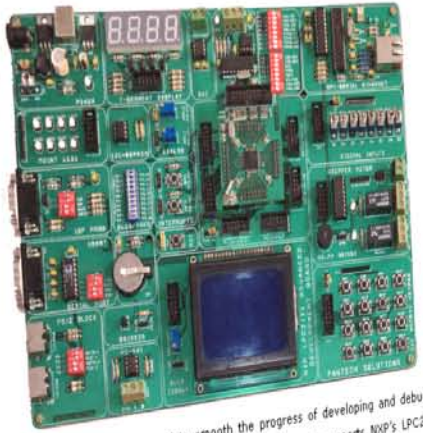
Address: <http://www.pantechsolutions.net/Arm%20Adv%20Development%20Board.html>

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## ARM Advanced Development Board



ARM Advanced Development Board is proposed to smooth the progress of developing and debugging of various designs encompassing of High speed 32-bit Microcontrollers from NXP. The board supports NXP's LPC211x family devices with various memory and peripheral options. The board is comprised of a application board and a mother board. The mother board holds the NXP's LPC211x series microcontroller. It integrates on board two UARTs, LEDs, keypads, an ADC input and LCD Display to create a stand-alone versatile test platform. A 20-pin JTAG interface is also provided on this board to support high-speed download, in-circuit debugging and flash programming. User can easily engage in development in this platform.

8051 Evaluation Board  
8051 Development Board  
8051 Adv Development Board  
PIC Evaluation Board  
PIC Development Board  
PIC Adv Development Board  
dsPIC Development Board  
AVR Evaluation Board  
AVR Development Board  
AVR Adv Development Board  
R8C Tiny Evaluation Board  
R8C Tiny Development Board  
PIC Web Server Board  
ARM Evaluation Board

This ARMEVB evaluation board is a cost prototype real world interface.

Block Diagram:

Windows Embedded Partner  
SPARTAN-3  
ARM  
ANALOG DEVICES  
MICROCHIP  
Linux

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# LPC2000 User's Group – The #1 active microcontroller group on Yahoo



## Home

Activity within 7 days: **54** New Members - **309** New Messages

### Description

The NXP (formerly Philips) LPC2000 family of ARM MCUs is sufficiently different from other ARM variants that I decided that a forum dedicated to it would be useful.

### Info

### Settings

#### Group Information

Members: 5745

Category:  
[Microcontrollers](#)

Founded: Nov 17, 2003

Language: English

### Message History

	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
2007	776	631	807	733	578	551	613	719	850	309		
2006	1039	930	1041	903	730	701	911	814	702	640	764	575
2005	592	577	551	550	385	436	418	377	471	754	1072	896
2004	328	545	344	286	364	335	322	178	299	427	393	571
2003											113	308

<http://groups.yahoo.com/group/lpc2000/>



- ▶ ARM7 is an open architecture
- ▶ On-Board Peripherals features, Advantages  
ARM7TDMI-S.
- ▶ Protocols Features.



