SA1000
Fixed Disk Drive

OEM Manual

Shugart

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1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The Shugart Model 1000 series disk drive is a random access storage device with one or two non-removable 8'' disks as storage media. Each disk surface employs one movable head to service 256 data tracks. The two models of the SA1000 series are the 1002 and the 1004 with single and double platters respectively. The SA1002 provides 5 megabytes accessed by 2 movable heads and the SA1004 provides 10 megabytes accessed by 4 movable heads.

Low cost and unit reliability are achieved through the use of a unique band actuator design. The inherent simplicity of mechanical construction and electronic controls allows maintenance free operation throughout the life of the drive.

Mechanical and contamination protection for the head, actuator and disks are provided by an impact resistant plastic and aluminum enclosure. A self contained recirculating system supplies clean air through a 0.3 micron filter. Another absolute filter allows pressure equalization with ambient air.

The optional SA1200 Data Separator PCB or equivalent circuitry is necessary to provide MFM encoding/decoding, write precompensation, a crystal write oscillator and address mark writing and detection. These functions are also provided by the optional SA1400 controller.

The SA1000 fixed disk drive's interface is similar* to the Shugart 8'' family of floppy disk drives. The SA1000 is designed to fit into the same physical space as the 8'' floppies.

Key Features:

- Storage Capacity of 5.33 or 10.67megabytes.
- Winchester design reliability.
- Same physical size and identical mounting configuration as the SA800/850 floppies.
- Uses the same D.C. voltages as the SA800/850 floppies.
- Proprietary Fas Flex III band actuator.
- 4.34 Mbits/second transfer rate.
- Simple floppy like interface.

*Existing floppy controllers are not compatible with the SA1000 due to differences in the data transfer rates.

1.2 Specification Summary

1.2.1 Physical Specifications

Environmental Limits

Ambient Temperature =	50° to 115°F (10° to 46°C)
Relative Humidity =	8% to 80%
Maximum Wet Bulb =	78° non-condensing

AC Power Requirements

50/60 Hz ± 0.5Hz

100/115 VAC Installations	= 90-127V at 1.1A typical
200/230 VAC Installations	= 180-253V at 0.6A typical

DC Voltage Requirements

+ 24VDC ± 10% 2.8A typical during stepping (0.2A typical steady state, non stepping)

+ 5VDC ± 5% 2.0A typical during stepping (3.6A typical non-stepping)

-5VDC ± 5% (-7 to -16VDC optional) 0.2A typical

Mechanical Dimensions

	Rack Mount	Standard Mount
Height =	4.62 in. (117.3mm)	4.62 in. (117.3mm)
Width =	8.55 in. (217.2mm)	9.50 in. (241.3mm)
Depth =	14.25 in. (362.0mm)	14.25 in. (362.0mm)
Weight =	17 lbs. (7.7Kg)	17 lbs. (7.7Kg)

Heat Dissipation = 150 Watts (511 BTU/Hr) Max.

1.2.2 Reliability Specifications

MTBF: 8,000 POH typical usage
PM: None Required
MTTR: 30 minutes
Component Life: 5 years

Error Rates:

Soft Read Errors:	1 per 10^{10} bits read
Hard Read Errors:	1 per 10^{12} bits read
Seek Errors:	1 per 10^{6} seeks

1.2.3 Performance Specifications

Capacity	SA1002	SA1004
Unformatted		
Per Drive	5.33 Mbytes	10.67 Mbytes
Per Surface	2.67 Mbytes	2.67 Mbytes
Per Track	10.4 Kbytes	10.4 Kbytes
Formatted		
Per Drive	4.2 Mbytes	8.4 Mbytes
Per Surface	2.1 Mbytes	2.1 Mbytes
Per Track	8.2 Kbytes	8.2 Kbytes
Per Sector	256 bytes	256 bytes
Sectors/Track	32	32
Transfer Rate	4.34 Mbits/sec	4.34 Mbits/sec
Access Time		
Track to Track	19 msec	19 msec
Average	70 msec	70 msec
Maximum	150 msec	150 msec
Average Latency	9.6 msec	9.6 msec

1.2.4 Functional Specifications

Rotational Speed	3125 rpm	3125 rpm
Recording Density	6270 bpi	6270 bpi
Flux Density	6270 fci	6270 fci
Track Density	172 tpi	172 tpi
Cylinders	256	256
Tracks	512	1024
R/W Heads	2	4
Disks	1	2

2.0 FUNCTIONAL CHARACTERISTICS

2.1 GENERAL OPERATION

The SA1000 fixed disk drive consists of read/write and control electronics, read/write heads, track positioning mechanism, media, and air filtration system. These components perform the following functions:

1. Interpret and generate control signals.
2. Position the heads over the selected track.
3. Read and Write data.
4. Provide a contamination free environment (Class 100 or better).

2.2 READ/WRITE AND CONTROL ELECTRONICS

The standard electronics are packaged on a single printed circuit board containing the following circuits:*

1. Index Detector Circuit
2. Head Position Actuator Drivers
3. Read/Write Amplifiers
4. Drive (Ready) up to Speed Circuit
5. Drive Select Circuit
6. Write Fault Detection Circuit
7. Read/Write Head Select Circuit
8. Step Buffers with Ramped Stepper Circuit
9. Track 000 indicator

*Early units may have two printed circuit boards.

2.3 Drive Mechanism

The AC drive motor rotates the spindle at 3125 RPM through a belt-drive system. Either 50 or 60 Hz power is accommodated by changing the drive pulley and belt.

2.4 Air Filtration System (Figure 1)

The disk(s) and read/write heads are fully enclosed in a module using an integral recirculating air system with an absolute filter which maintains a clean environment. A separate absolute breather filter permits pressure equalization with the ambient air without contamination.

2.5 Positioning Mechanism (Figure 2)

The read/write heads are mounted on a ball bearing supported carriage which is positioned by the Fasflex III™ actuator. A stepper motor is used to precisely position the carriage assembly utilizing a unique metal band/capstan concept.

2.6 Read/Write Heads and Disk(s)

The recording media consists of a lubricated thin magnetic oxide coating on a 200mm diameter aluminum substrate. This coating formulation, together with the low load force/low mass Winchester type flying heads, permit reliable contact start/stop operation.

Data on each disk surface is read by one read/write head, each of which accesses 256 tracks. The drive is available in two basic configurations: one disk with two read/write heads, or two disks with four read/write heads.

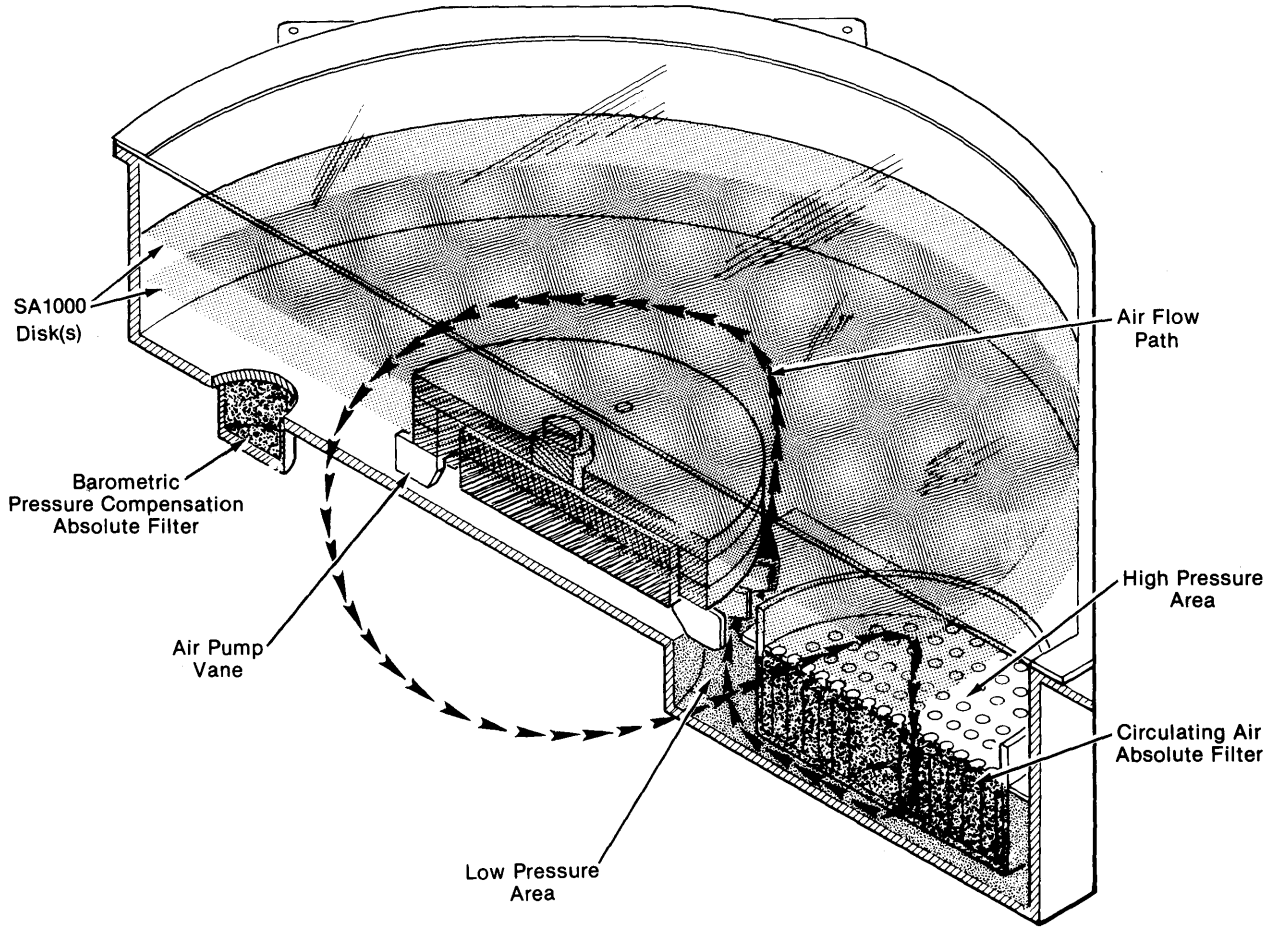


Figure 1 Air Filtration System

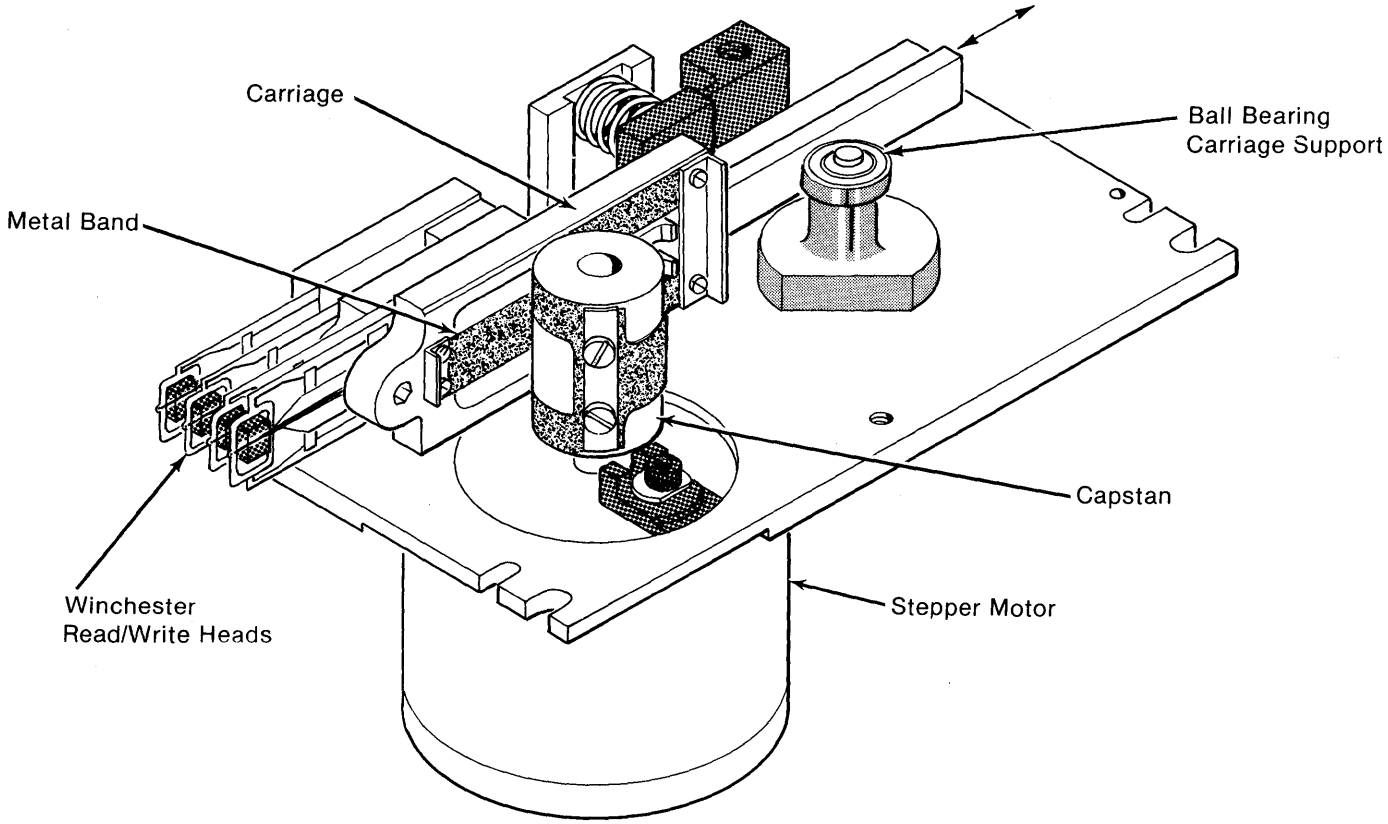


Figure 2 Positioning Mechanism

3.0 FUNCTIONAL OPERATIONS

3.1 POWER SEQUENCING

Since the SA1000 has a speed sense circuit that prevents stepping until the disk is rotating at the proper speed, no power on sequence is required. A READY signal will be presented to the controller interface once the disk is up to 95% of its normal rotational speed. At READY time, after an initial power up, the drive will recalibrate itself to TK000. After a 18 msec head settle time, SEEK COMPLETE will go true. Normal seek and read/write functions can now begin. Refer to Figure 3.

3.2 DRIVE SELECTION

Drive selection occurs when one of the Drive Select lines is activated. Only the disk appropriately jumpered will respond to the activated Drive Select line.

3.3 TRACK ACCESSING

Read/Write Head positioning is accomplished by:

a. Deactivating Write Gate.

b. Activating the appropriate Drive Select Line.

c. Being in the READY condition with SEEK COMPLETE true.

d. Selecting the appropriate Direction.

e. Pulsing the Step Line.

Stepping can occur at either the Normal or Buffered rate. During Normal Stepping, the heads are repositioned at the rate of incoming step pulses. In the case of Buffered Stepping, incoming step pulses are received at a high rate and are buffered into counters. When all of the steps have been received, they are issued at a ramped stepping rate, to the stepper drivers.

Each pulse will cause the heads to move either 1 track in or 1 track out, depending on the level of the Direction In line. A true on the Direction In Line will cause an inward seek; a false on the Direction In Line will result in an outward seek toward TK000.

3.4 HEAD SELECTION

Any of the 4 possible heads can be selected by placing that head's binary address on the two Head Select lines.

3.5 READ OPERATION

Reading data from the disk is accomplished by:

a. Deactivating the Write Gate Line.

b. Activating the appropriate Drive Select Line.

c. Assuring that the drive is Ready.

d. Selecting the appropriate head.

3.6 WRITE OPERATION

Writing data onto the disk is accomplished by:

a. Activating the appropriate Drive Select Line.

b. Assuring that the Drive is Ready.

c. Clearing any write fault conditions if they exist, by reselecting the drive.

d. Selecting the proper head.

e. Activating Write Gate and placing data on the Write Data line.

4.0 ELECTRICAL INTERFACE

The interface of the SA1000 can be divided into three categories:

1. Signal Interface
2. DC Power
3. AC Power

The following sections provide the electrical definition for each line.

4.1 SIGNAL INTERFACE

The signal interface consists of three categories:

1. Control Input lines
2. Control Output lines
3. Data Transfer lines

All control lines are digital in nature and either provide signals to the drive (input) or provide signals to the disk controller (output) via the interface connector J1/P1. The data transfer signals are differential in nature, they provide data and clocking, either to or from the drive, via J2/P2.

NOTE: Refer to Figure 3.*Those signal lines marked SPARE are uncommitted. They may be used as alternate lines to carry SA1000 signals if the user prefers to do his own modification.* **Those signal lines marked NA are uncommitted for the SA1000, but are assigned for the SA800/850.** Therefore, these signals should not be used as alternate signals if a controller having an SA800/850 interface is used.

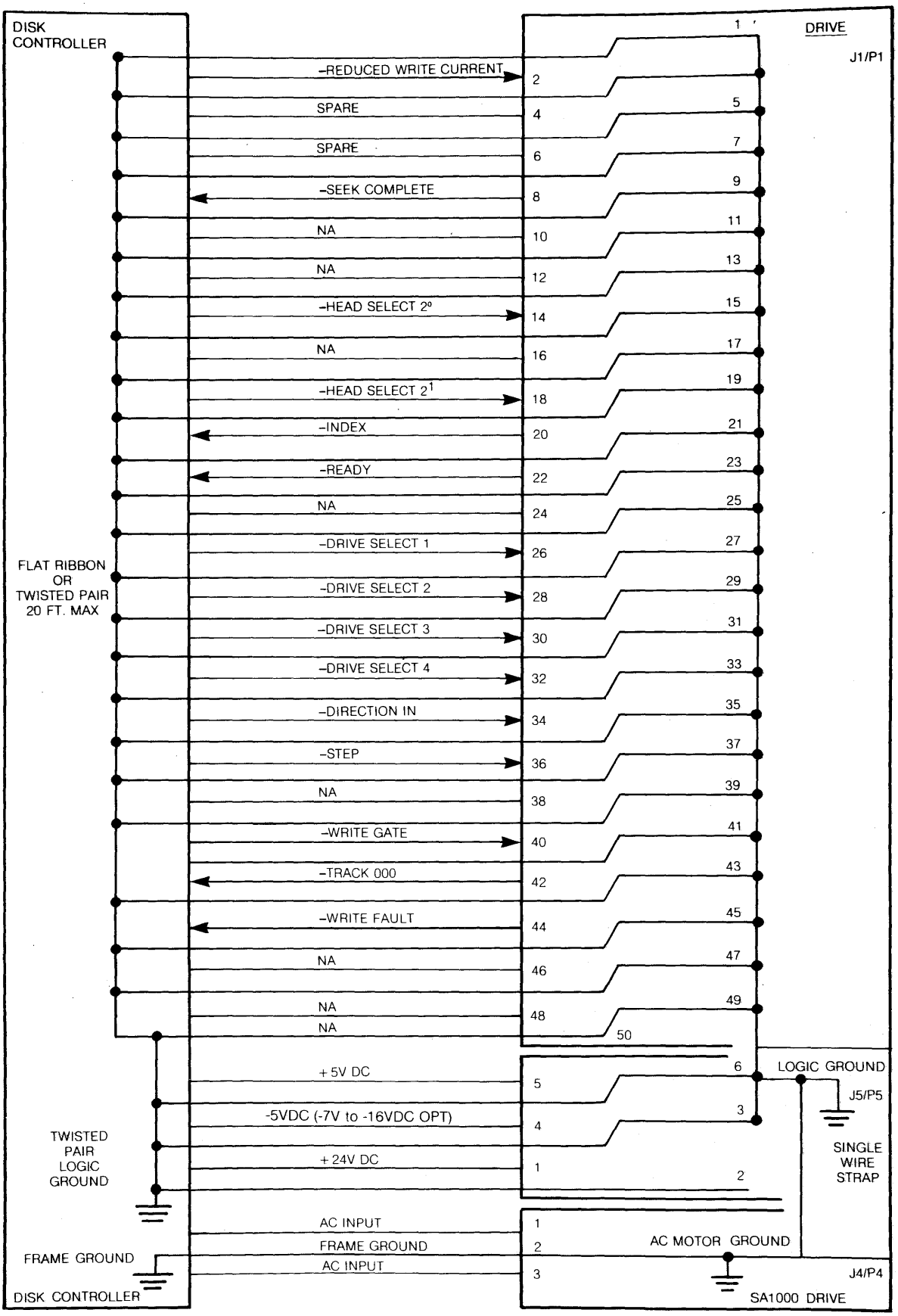


Figure 3 J1 Interface and Power Connection

4.1.1 CONTROL INPUT LINES

The control input signals are of two types: those intended to be mutliplexed in a multiple drive system and those intended to control the multiplexing. The control input signals to be mutliplexed are STEP, DIRECTION IN, HEAD SELECT 2^0 and 2^1, WRITE GATE and REDUCED WRITE CURRENT. The signal which is intended to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to Figure 4 for the recommended circuit.

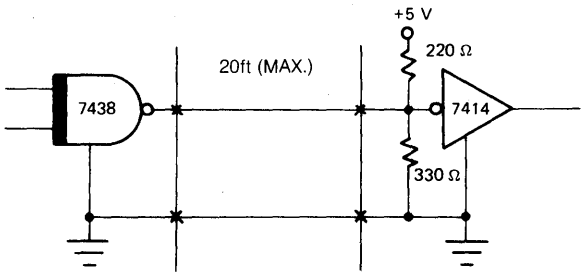


Figure 4 Control Input Driver/Receiver Combination

The 7438 has the following characteristics:

True = 0.0VDC to 0.4VDC @ Iin = 40 ma(max)
False = 2.5VDC to 5.25 VDC @ Iin = 250 μa (open)

Only 1 drive in the system should be terminated, if floppy disks are daisy chained together with SA1000 drives. A SA1000 should be physically located at the end of the cable and terminated at IC location 8C.

A 220/330Ω resistor pack, located at IC location 8C, provides input line termination.

4.1.1.1 DRIVE SELECT 1-4

DRIVE SELECT, when logically true, connects the drive to the control lines. Only one DRIVE SELECT line may be active at a time.

Jumper options DS1, DS2, DS3, and DS4 are used to select which drive select line will activate the interface for that unique drive.

4.1.1.2 DIRECTION IN

This signal defines the direction of motion of the read/write heads when the STEP line is pulsed. An open circuit or logical false, defines the direction as "out " and if a pulse is applied to the STEP line, the read/write head will move away from the center of the disk. If the input is shorted to ground, or logical true, the direction of motion is defined as "in" and if a pulse is applied to the STEP line, the read/write heads will move towards the center of the disk.

4.1.1.3 STEP

This line causes the read/write heads to move in the direction as defined by the DIRECTION IN line. The motion is initiated at each logical true to false transition. Any change in the DIRECTION IN line must be made at least 200 ns before the trailing edge of the step pulse. Stepping can be performed in either the Normal or Buffered mode:

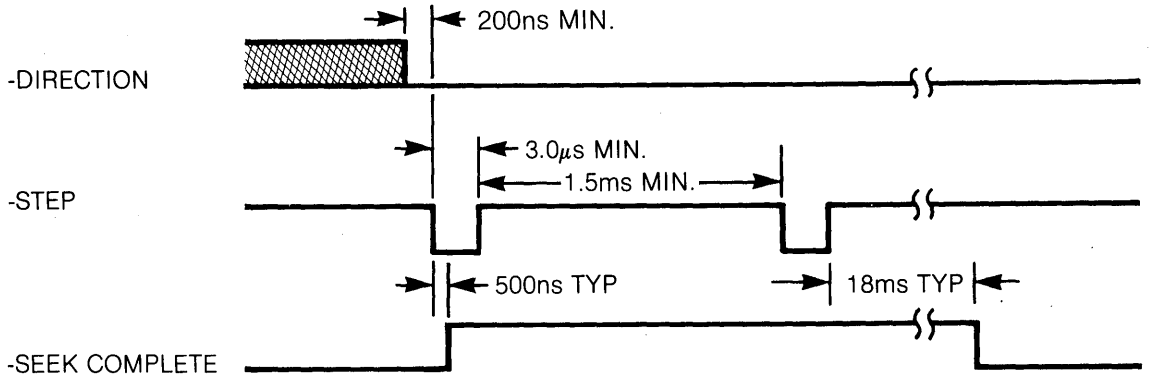


Figure 5 Normal Step Mode

- Normal Step Mode- In this mode, the read/write heads will move at the rate of the incoming step pulses. The minimum time between successive steps is 1.5ms, with a minimum pulse width of 3.0μs. Refer to Figure 5.

- Buffered Step Mode- In this mode, the step pulses are received at a high rate and buffered into a counter. After the last step pulse, the read/write heads will begin stepping the desired number of cylinders and SEEK COMPLETE (Refer to Section 4.1.2.5) will go true after the read/write heads settle on the cylinder. *This mode of operation is automatically selected when the time between step pulses is the less than 200μsec.*

  100 ns after the last step pulse has been sent to the drive, the DRIVE SELECT line may be dropped and a different drive selected.

  The maximum time between steps is 200μs with a minimum pulse width of 3.0μs. (Refer to Figure 6).

NOTE : A high pitched noise may be present if AC and DC power are applied to an SA1000 with the data cable disconnected (no timing clock signal). It's the stepper motor trying to return to track zero with no step pulses present. While this will not damage the drive, this condition should be avoided.

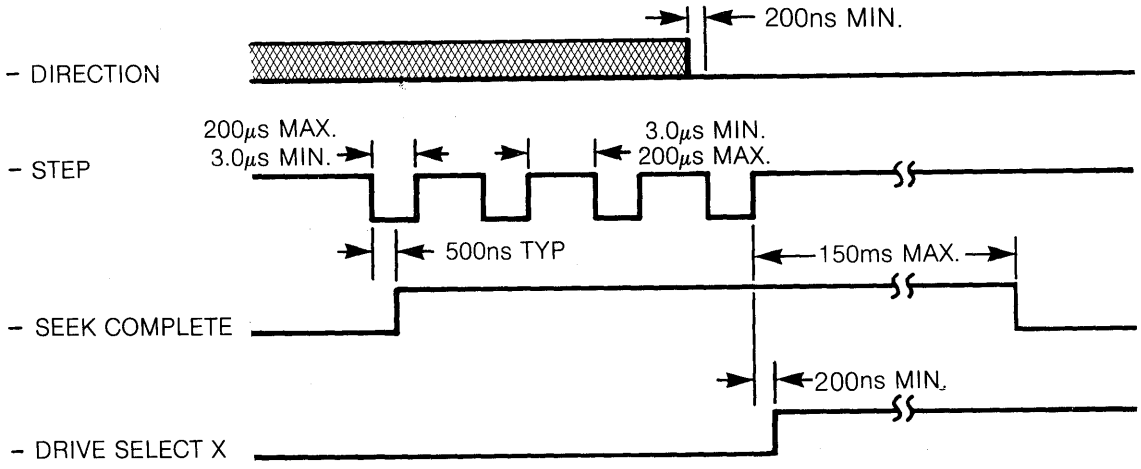


Figure 6 Buffered Step Mode

NOTES: 1. Step pulses with periods between 200μs and 1.5ms are not permitted. Seek accuracy is not guaranteed if this timing requirement is violated.

2. A 220/330Ω resistor pack,located at IC location 8C, allows for Step line termination.

4.1.1.4 HEAD SELECT 2^0 and 2^1

These two lines provide for the selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. When all HEAD SELECT lines are false, head 0 will be selected. Table 1 shows the HEAD SELECT SEQUENCE and model variations for the HEAD SELECT lines. (Refer to Figure 7 for the timing sequences).

A 220/330Ω resistor pack, located at IC location 8C, allows for input line termination.

HEAD SELECT LINE 2^0	HEAD SELECT LINE 2^1	HEAD# SELECTED SA1002	HEAD# SELECTED SA1004
1	1	0	0
1	0	1	1
0	1	-	2
0	0	-	3

Table 1 Head Select (1 = False, 0 = True)

4.1.1.5 WRITE GATE

The active state of this signal (logical zero level) enables WRITE DATA to be written onto the disk. The inactive state of this signal (logical one level) enables data to be transferred from the drive and enables STEP pulses to reposition the head arm.

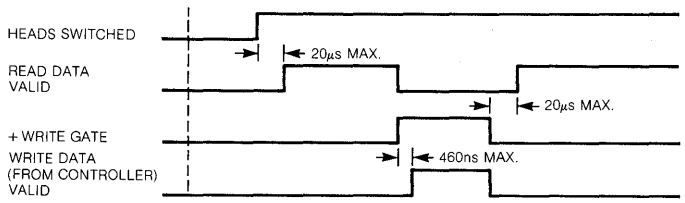


Figure 7 Head Selection Timing

A 220/330Ω resistor pack, located at IC location 8C, allows for termination of this line.

4.1.1.6 REDUCED WRITE CURRENT

When this interface signal is low (true) the lower value of Write Current is selected (for writing on cylinders 128 through 255). When this signal is high (false), the higher value of Write Current is selected (for writing on cylinders 0 through 127). A 220/330Ω resistor pack, located at IC location 8C, allows for line termination.

4.1.2 CONTROL OUTPUT LINES

The control output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at logical zero (true), with a maximum voltage of 0.4V measured at the driver. When the line driver is at logical one (false) the driver transistor is off and the collector cut off current is a maximum of 250 microamperes.

All J1 output lines are enabled by their respective DRIVE SELECT line.

Figure 8 shows the recommended control signal driver/receiver combination.

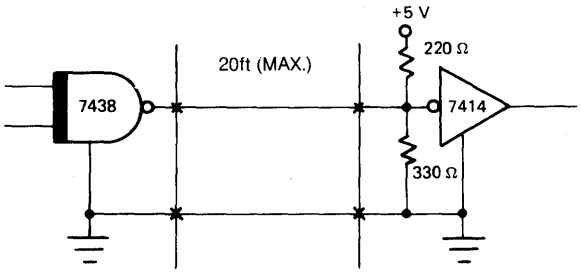


Figure 8 Control Output Driver/Receiver Combination

4.1.2.1 TRACK 000

This interface signal indicates a true state (logical zero) only when the selected drive's read/write heads are at track zero (the outermost data track) and the access circuitry is driving current through phase one of the stepper motor. This signal is false (logical one) when the selected drive's read/write head is not at track zero.

4.1.2.2 INDEX

The drive provides this interface signal once each revolution (19.2ms) to indicate the beginning of the track. Normally, this signal is a logical one and makes the transition to logical zero for a period of approximately 10μs once each revolution. Refer to Figure 9.

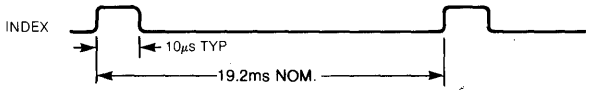


Figure 9 Index Timing

4.1.2.3 READY

This interface signal when true (logical zero), together with SEEK COMPLETE, indicates that the drive is ready to read, write, or seek and that the signals are valid. When this line is false (logical one), all writing to the disk and seeking is inhibited at the drive.

Ready will be true after the drive is 95 ± 2% up to speed. The typical time for READY to become true after power on is 5 seconds.

4.1.2.4 WRITE FAULT

This signal when active (logical zero) is used to indicate that a condition exists at the drive that could cause improper writing on the disk. A WRITE FAULT occurs whenever one of two conditions occur:

- WRITE CURRENT in the head without WRITE GATE active.
- Multiple heads selected.

To reset the WRITE FAULT line, deselect the drive for at least 500 ns.

4.1.2.5 SEEK COMPLETE

SEEK COMPLETE will go true (logical zero) when the read/write heads have settled on the final track at the completion of a seek. Reading or writing should not be attempted until SEEK COMPLETE is true.

SEEK COMPLETE will go false in two cases:

- A recalibration sequence is initiated (by the drive logic) at power on if the read/write heads are not over track zero.
- 500 NS typical, after the leading edge of a STEP pulse (or the first of a series of step pulses).

4.1.3 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host are differential in nature and may not be multiplexed. These three pairs of balanced signals are: MFM WRITE DATA, MFM READ DATA, and TIMING CLOCK and are provided at the J2/P2 connectors on all drives. Figure 10 illustrates the driver/receiver combination.

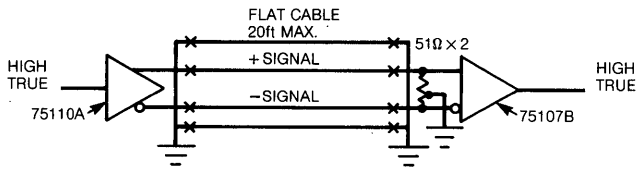


Figure 10 Data Transfer Line Driver/Receiver Combination

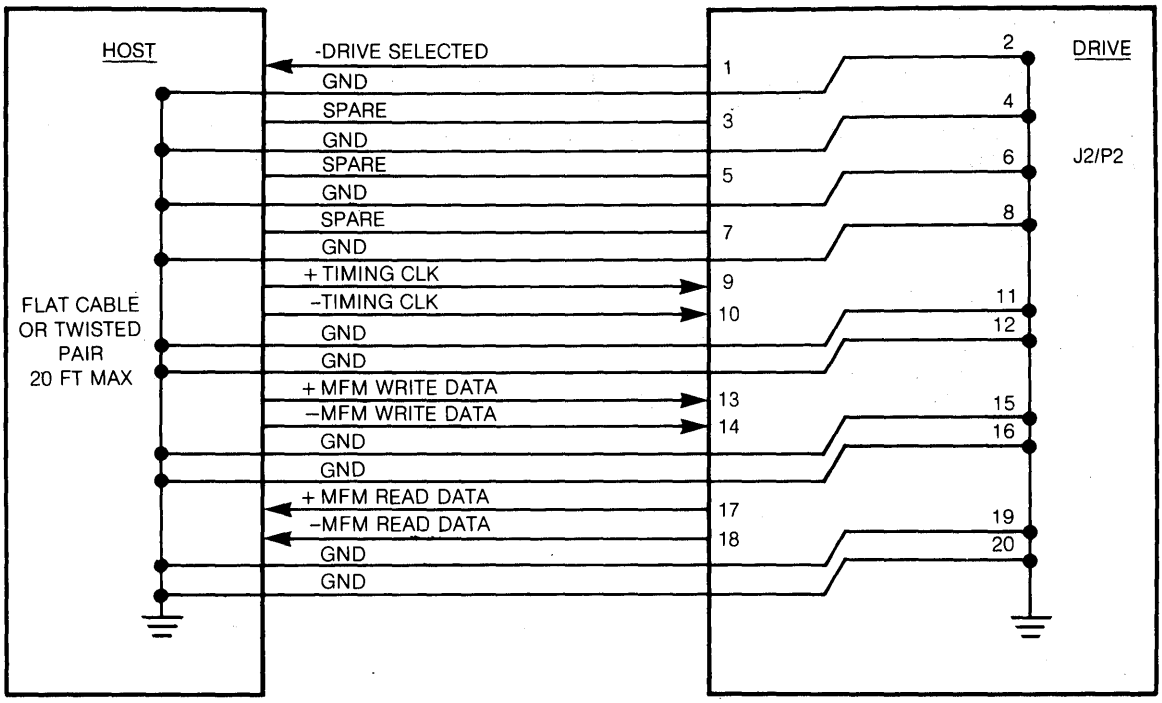


Figure 11 J2 Interface Connection

4.1.3.1 MFM WRITE DATA

This pair of signals defines the transitions (bits) to be written on the disk. + MFM WRITE DATA going more positive than -MFM WRITE DATA will cause a flux reversal on the track under the selected head providing WRITE GATE is active. This signal must be driven to an inactive state (+ MFM WRITE DATA more negative than -MFM WRITE DATA) by the host system when in the read mode. Figure 12 shows the timing for MFM WRITE DATA.

4.1.3.2 MFM READ DATA

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM READ DATA lines. This transition of the + MFM READ DATA line going more positive than -MFM READ DATA line represents a flux reversal on the track of the selected head while WRITE GATE is inactive. Refer to Figure 12.

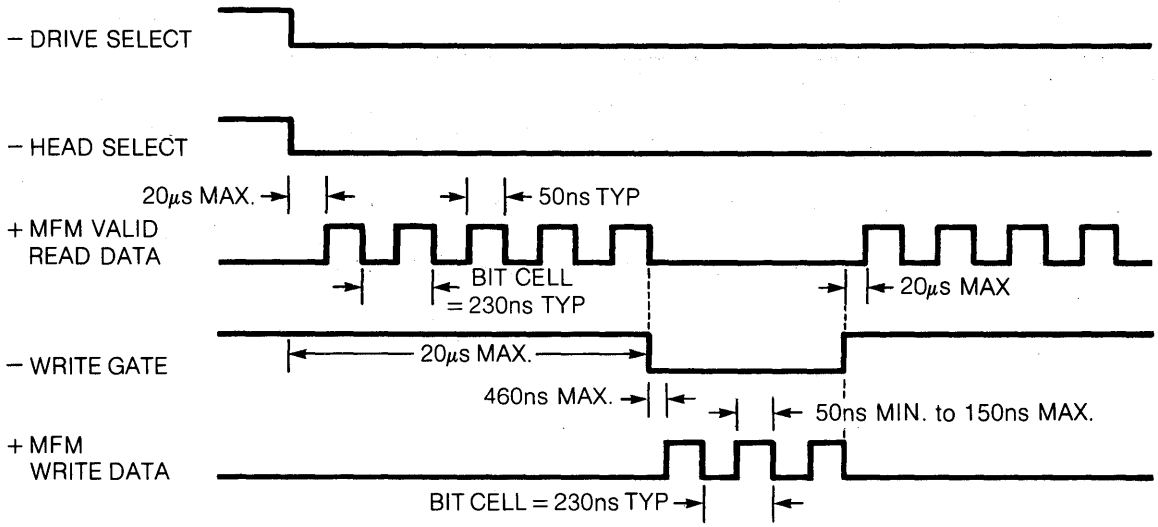


Figure 12 MFM Read/Write Data Timing

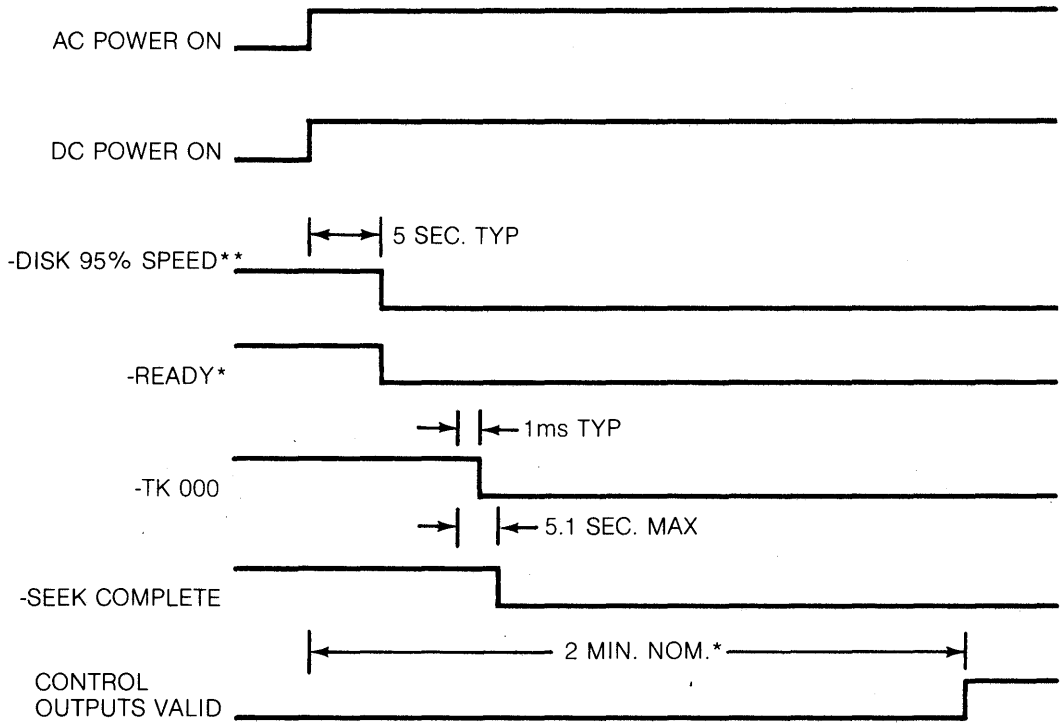
4.1.3.3 TIMING CLOCK

This is a differential pair of clock signals (provided by the host) having a 50% (nominal) duty cycle and a 3.6866 μs ± .1% period. The frequency of this clock is exactly 1/16 the bit frequency for the standarized write data. Phase relationship between TIMING CLOCK and MFM WRITE DATA need not be maintained by the host for the SA1000 interface. The TIMING CLOCK is used by the drive logic for clocking and timing purposes.

4.1.4 SELECT STATUS

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driven as shown in Figure 8. This signal will go active only when the drive is programmed as drive X (X = 1, 2, 3 and 4) by proper placement of the shorting plug in the vicintiy of J1, and that DRIVE SELECT X line at J1/P1 is activated by the host system.



*The drive will bring Ready active as soon as the disk is rotating at 95% of normal speed. It is now safe to seek the drive but an additional 2 minutes should be allowed for thermal expansion to stabilize.

**Disk up to speed signal does not connect to the drive interface cable.

Figure 13 General Control Timing Requirement

4.1.5 GENERAL TIMING REQUIREMENTS

The timing diagram as shown in Figure 13 shows the necessary sequence of events (with associated timing restrictions) for proper operation of the drive.

Note that a recalibrate to track zero sequence is initiated automatically at every DC power on. For this auto-recal sequence to function, the following conditions must be met:

- TIMING CLOCK is supplied to the drive (via J2/P2).
- STEP Input at J1/P1 is held inactive.
- Spindle is spinning at regular speed (if AC and DC are switched on at the same time, stepping action will not occur until disk is up to speed).

4.2 POWER INTERFACE

The SA1000 requires both AC and DC power for operation. The AC power is used for the drive motor and the DC power is used for the electronics and the stepper motor.

4.2.1 AC POWER

The AC power is via the connector J4 mounted at the center rear of the drive. Table 2 shows a listing of the AC power requirements.

4.2.2 DC POWER

DC power to the drive is via connector J5/P5 located on the solder side of the PCB. The three DC voltages and their specifications along with their J5/P5 pin designations, are outlined in Table 3.

NOTE: The SA1000 is shipped with DC (base casting) and AC ground (drive motor) connected together with a ground strap located on the drive motor. If the system configuration requires the separation of these grounds, remove the strap.

CONN P4	60HZ		50HZ	
	110V (STANDARD)	203/230V	110V	220V
1 2 3	90-127V FRAME GND 90-127V RTN	180-253V FRAME GND 180-253V	90-127V FRAME GND 90-127V RETURN	180-253V FRAME GND 180-253V
MAX INRUSH CURRENT (3 SEC)	2.6A	1.1/1.25A	2.6A	1.2A
MAX RUN CURRENT	1.0A	0.5A	1.1A	0.6A
FREQ TOL	±0.5 HZ		±0.5 HZ	

Table 2 AC Power Requirements

P5 CONNECTOR	CURRENT			
	STEADY STATE		STEPPING	
	MAX.	TYP	MAX.	TYP
+24 ± 2.4V 1V. P-P MAX. Ripple	0.25A	0.20A	3.3A	2.8A
+5 ± 0.25V 50mV P-P MAX. Ripple	4.1A	3.6A	2.5A	2.0A
(-7 TO -16V OPT) -5 ± 0.25V 50mV P-P MAX. Ripple	0.25A	0.20A	0.25A	0.20A

Table 3 DC Requirements

5.0 PHYSICAL INTERFACE

The electrical interface between the SA1000 and the host system is via four connectors. The first connector, J1, provides control signals for the drive; the second connector, J2, provides for the radial connection of the read/write signals; the third connector, J5, provides DC power; and the fourth connector, J4, provides AC power and frame ground. Refer to Figure 14 for the connector locations.

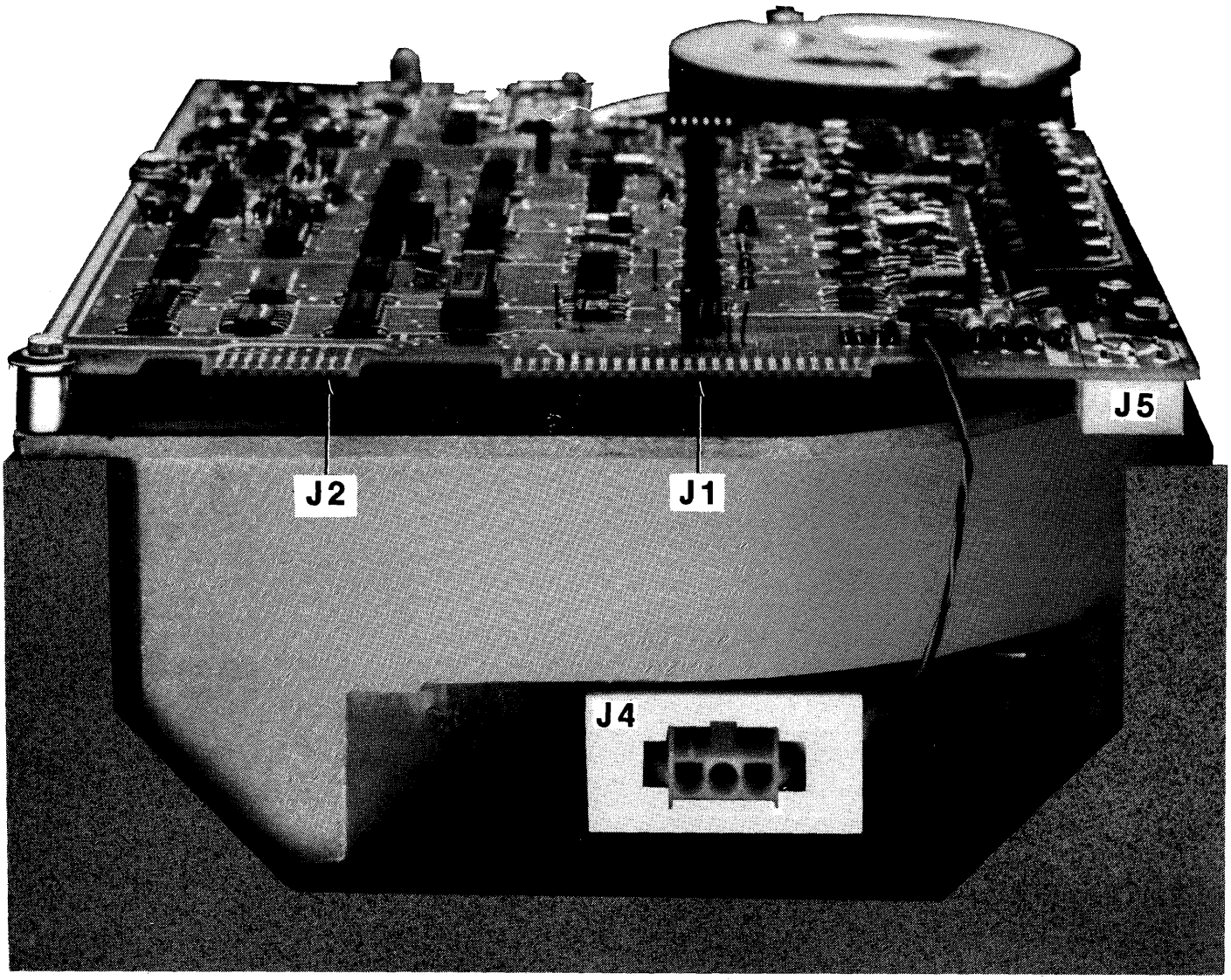


Figure 14 Connector Locations

5.1 J1/P1 CONNECTOR

Connection to J1 is through a 50 pin PCB edge connector. The dimensions for this connector are shown in Figure 15. The pins are numbered 1 through 50 with the even numbered pins located on the component side of the PCB and odd pins located on the non-component side of the PCB. Pin 2 is located on the end of the PCB connector closest to the J2 connector and is labeled. A Key Slot is provided between pins 4 and 6. The *recommended mating connector* for P1 is Scotchflex ribbon connector P/N 3415-0001.

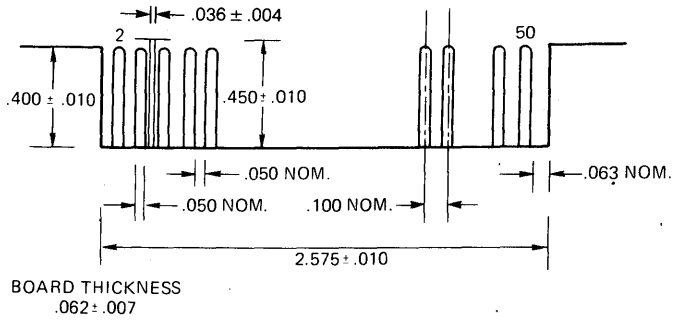


Figure 15 J1 Connector Dimensions

5.2 J2/P2 CONNECTOR

Connection to J2 is through a 20 pin PCB edge connector. The pins are numbered 1 through 20 with the even numbered pins located on the component side of the PCB. The *recommended mating connector* for P2 is a Scotchflex ribbon connector P/N 3461-0001. A key slot is provided between pins 4 and 6. Figure 16 shows the dimensions for the connector.

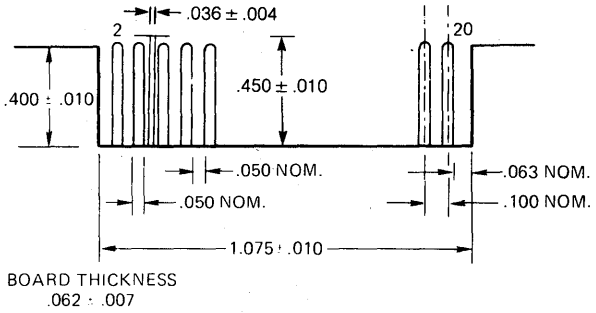


Figure 16 J2 Connector Dimensions

5.3 J4/P4 CONNECTOR

AC power and frame ground are interfaced through a 3 pin connector, J4, located on the end of the drive. The AMP part number for J4 is 1-480701-0 with pins AMP P/N 350687-1 and 350654-1 (ground pin), refer to Figure 17. The *recommended mating connector,* P4, is AMP socket P/N 1-480700-0 with AMP pins P/N 350536-1.

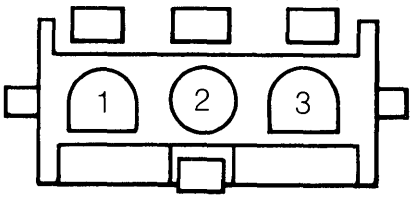


Figure 17 J4 Connector

5.4 J5/P5 CONNECTOR

The DC power connector, J5, is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0, mounted on the non-component side of the Control PCB. The *recommended mating connector,* P5, is an AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. The J5 pins are labeled on the connector. Refer to Figure 18.

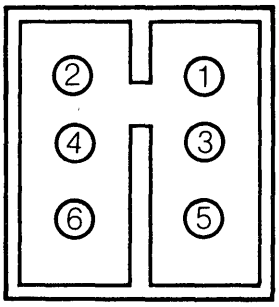


Figure 18 J5 Connector

6.0 PHYSICAL SPECIFICATIONS

This section describes the mechanical dimensions and mounting recommendations for the SA1000. Refer to Figures 19 and 20 for the dimensions.

The SA1000 is capable of being mounted in either one of the following positions:

- Vertical - on either side
- Horizontal - PCB Up.

IMPORTANT NOTE: Spindle lock shown in figures 19 & 20 must be installed whenever drive is being transported. Damage to the magnetic heads, disks, or both may occur if spindle is not locked during shipment.

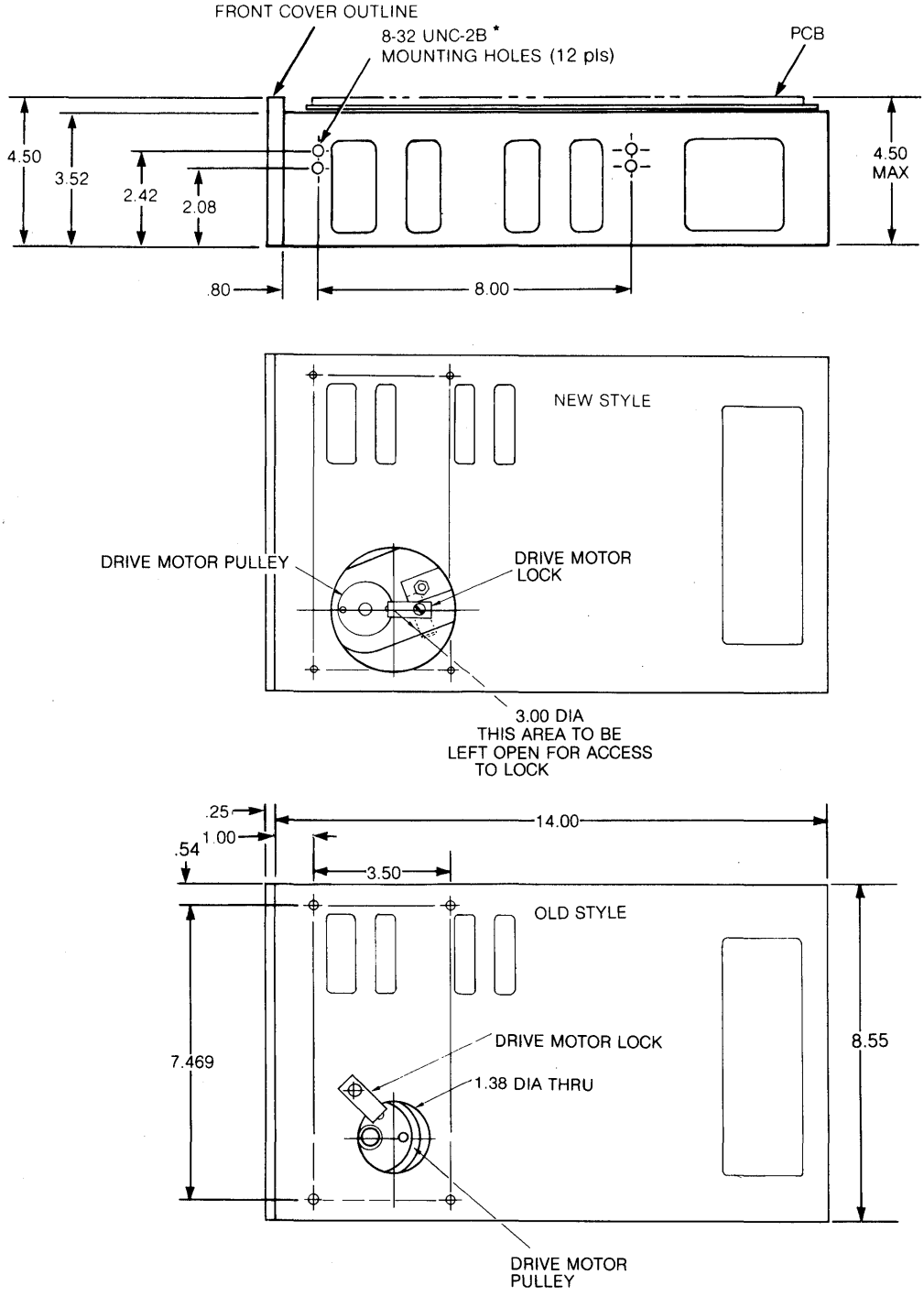


Figure 19 Rack Mount Physical Dimensions

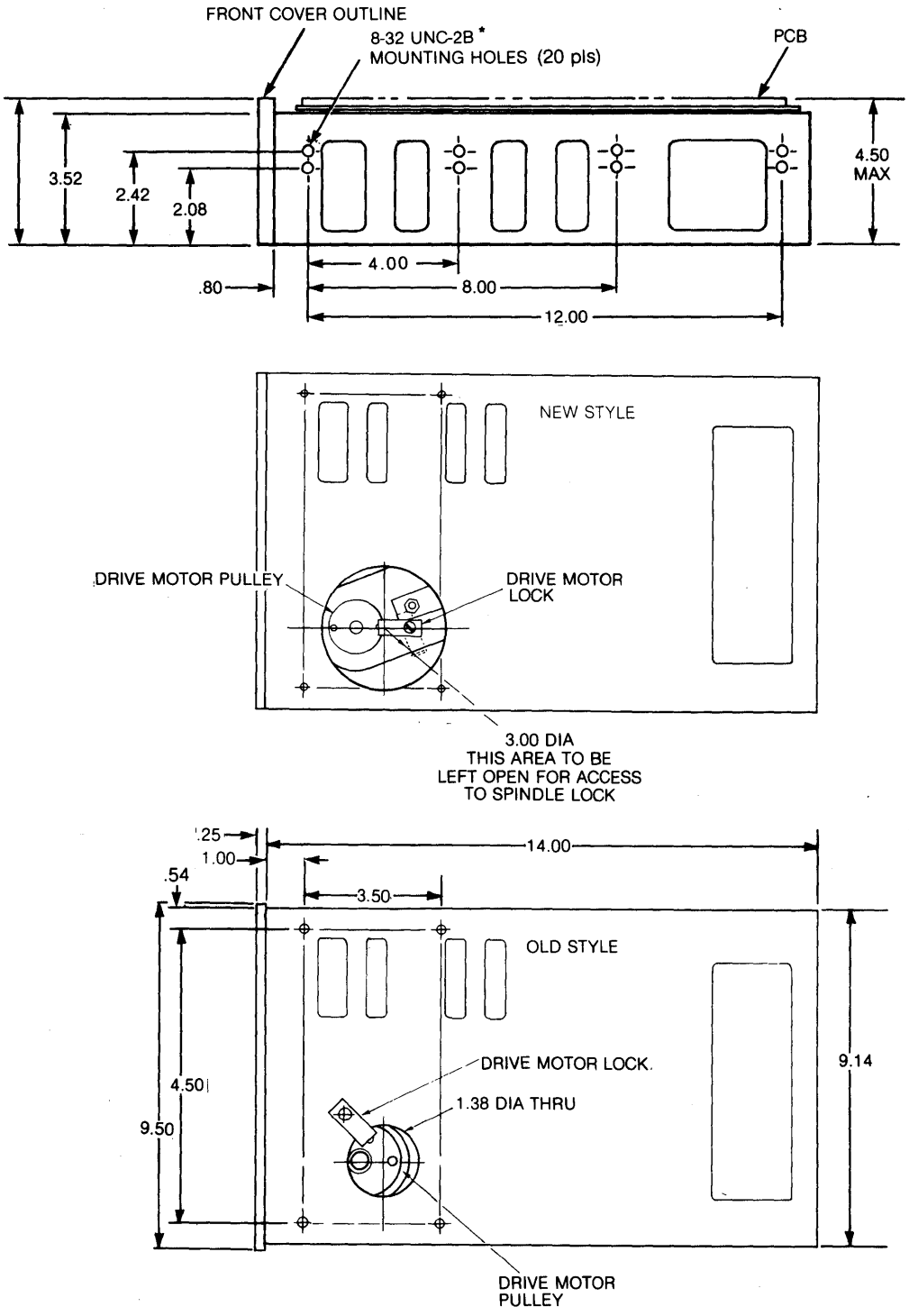


Figure 20 Standard Mount Physical Dimensions

7.0 MEDIA DEFECT & ERRORS

Introduction

In high density digital recording storage systems it is necessary to increase the reliability or improve the operational performance by providing an error detection and correction scheme. For disk storage systems, the predominant error pattern is a burst of errors occurring in one or more tracks which are drop outs (absent bits) or shifted bits from their nominal position more than the data separator can tolerate them to shift. These errors are due to defects in the media as well as signal to noise ratio contributing to probability of error occurrence. The error rate is dependent upon noise and phase characterisitics of media, Read/Write circuits, head and positioning of actuator.

What Is The Definition Of An Error?

An error is any discrepancy between recovered data and true correct recorded data. There can be an extra bit or a missing bit, i.e., a "zero" can be transformed into "one" or a "one"can be changed to"zero".Errors can be classified into soft or hard errors. Soft errors are generally related to signal to noise ratio of the system.

If an error is repeatable with a high probability, it is due to media defect and is termed a hard error.

How Will Shugart Find the Errors?

The errors will be identified prior to shipment and information incorporated in a usable format to enable the user to skip those defective locations per his system capability. Shugart has a unique media test system which exercises the drive in extreme marginal conditions and measures the amplitude and phase distortion of each bit recorded on the disk storage.

Error Reporting

A map will be provided with each drive showing defective bytes as a location from index identified by cylinder and head address. Additionally, cylinder 000 is guaranteed to be error free.

Error Acceptance Criteria

There will be no more than 12 tracks with defects per head of which no more than 4 tracks will contain multiple defects.

A single defect is defined as an error less than 2 bytes long. A multiple defect is defined as an error greater than 2 bytes long, or a single error in several sectors.

8.0 SA1000 TRACK FORMAT

The purpose of a format is to organize a data track into smaller, sequentially numbered, blocks of data called sectors. The SA1000 format is a soft sectored type which means that the beginning of each sector is defined by a prewritten identification (I.D.) field which contains the physical sector address, plus cylinder and head information. The I.D. field is then followed by a user data field.

The soft sectored format is a slightly modified version of the I.B.M. system 34 double density, which is commonly used on 8 inch floppy disk drives. The encoding method used here is modified frequency modulation (MFM).

In the example shown (Figure 21), each track is divided into 32 sectors. Each sector has a data field of 256 bytes in length.

The beginnings of both the I.D. field and the data field are flagged by unique characters called address marks.

An address mark is 2 bytes in length. The first byte is always an "A1" data pattern. This is followed by either an "FE" pattern which is the pattern used to define an I.D. address mark, or an "F8" which is a data address mark pattern.

The "A1" pattern is made unique by violating the encode rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination.

Each I.D. and data field are followed by a 16 bit cyclic redundancy check (CRC) character used for data verification. Each CRC polynomial is unique for a particular data pattern.

Surrounding The I.D. and data field are gaps called Interrecord gaps.

8.1 GAP LENGTH CALCULATIONS

8.1.1 GAP 1

Gap 1's purpose is to provide a head switching recovery period so that when switching from one track to another, sequential sectors may be read without waiting the rotational latency time. Gap 1 should be at least 11 bytes long which corresponds to the head switching time of 20 microseconds. Gap 1 is immediately followed by a sync field for the I.D. field of the first sector.

8.1.2 GAP 2

Following the I.D. field, and separating the I.D. field from the data field, is gap 2. Gap 2 provides a known area for the data field write update splice to occur. The remainder of this gap also serves as the sync up area for the data field address mark. The length of gap 2 is determined by the data separator lock up performance.

8.1.3 GAP 3

Gap 3, following the data field, is a speed variation tolerance area. This allows for a situation where a track has been formatted while the disk is running 3% slower than nominal, then write updated with the disk running 3% faster than nominal (power line variations).
Gap 3 should be at least 15 bytes in length.

8.1.4 GAP 4

Gap 4 is a speed tolerance buffer for the entire track. This allows the disk to rotate at least 3% faster than normal without overflowing the track during the format operation. The format operation which writes the I.D. fields, begins with the first encountered index and continues to the next index.

8.2 WRITE PRECOMPENSATION

Whenever two bits are written in close proximity to each other, a phenomenon called pulse superposition occurs, which tends to cause the two bits to move away from each other. This is a large factor of bit shift.

Other phenomenon such as random noise, speed variation, etc., will also cause bit shift, but to a lesser degree.

The effect of bit shift can be reduced by a technique called precompensation which, by detecting which bits will occur early and which bits will occur late, can be done by writing these bits in the opposite direction of the expected shift.

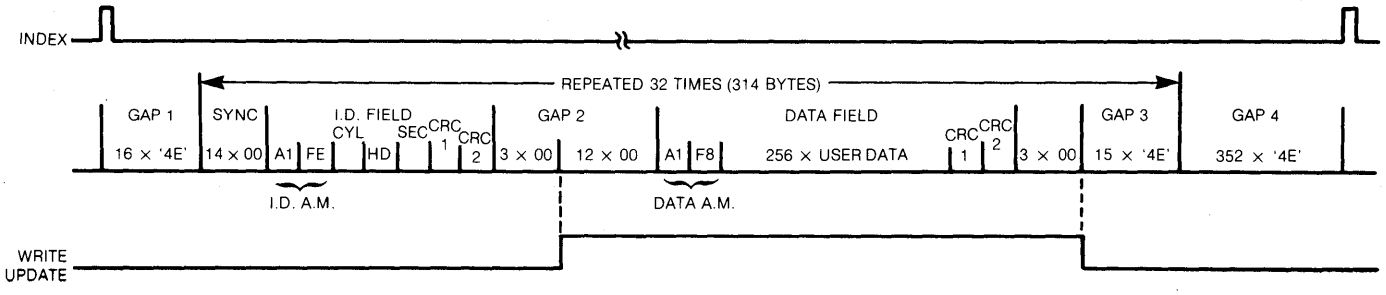
Bit shift is more apparent on the innermost data tracks due to pulse crowding. Therefore, precompensation should only be at track number greater than 128.

The optimum amount of pre-compensation for the SA1000 is 12 nanoseconds for both early and late written bits.
TABLE 4 shows various bit patterns for pre-compensation.

WRITE POSITION	DIRECTION OF SHIFT
0 0 0 0	= On Time Clock
0 0 0 1	= Late Clock
0 0 1 0	= On Time Data
0 0 1 1	= Early Data
0 1 0 0	-----
0 1 0 1	-----
0 1 1 0	= Late Data
0 1 1 1	= On Time Data
1 0 0 0	= Early Clock
1 0 0 1	= On Time Clock
1 0 1 0	= On Time Data
1 0 1 1	= Early Data
1 1 0 0	-----
1 1 0 1	-----
1 1 1 0	= Late Data
1 1 1 1	= On Time Data

Table 4. Write Precompensation

Precompensation Pattern Detection bits are shifted through a 4 bit shift register. Bit is written out of the third position.



NOTES:
1. NOMINAL TRACK CAPACITY - 10416 BYTES.
2. MINIMUM TRACK CAPACITY - (NOMINAL - 3% SPEED VARIANCE) 10102 BYTES.
3. WRITE TO READ RECOVERY TIME = 20 MICROSECONDS.
4. HEAD SWITCHING TIME = 20 MICROSECONDS.

Figure 21 Track Format

9.0 SA1000 JUMPER OPTIONS

The following jumper options are located on the control PCB, P/N 26050. Reference Figure 15 for the locations.

JUMPER	FUNCTION
Fault	When jumpered, this option disables the fault detection circuitry.
Ready	When jumpered, this option enables an active ready signal at the interface.
Drive Select (DS1 - 4)	When jumpered, this option selects the designated drive.
-5, -15 Volts	When jumpered in the -5 volt configuration, this option bypasses the regulator chip - to be used when the input voltage is rated at -5 volts. When jumpered in the -15 volt configuration, this option allows a -15 volt input to be regulated to -5 volts.

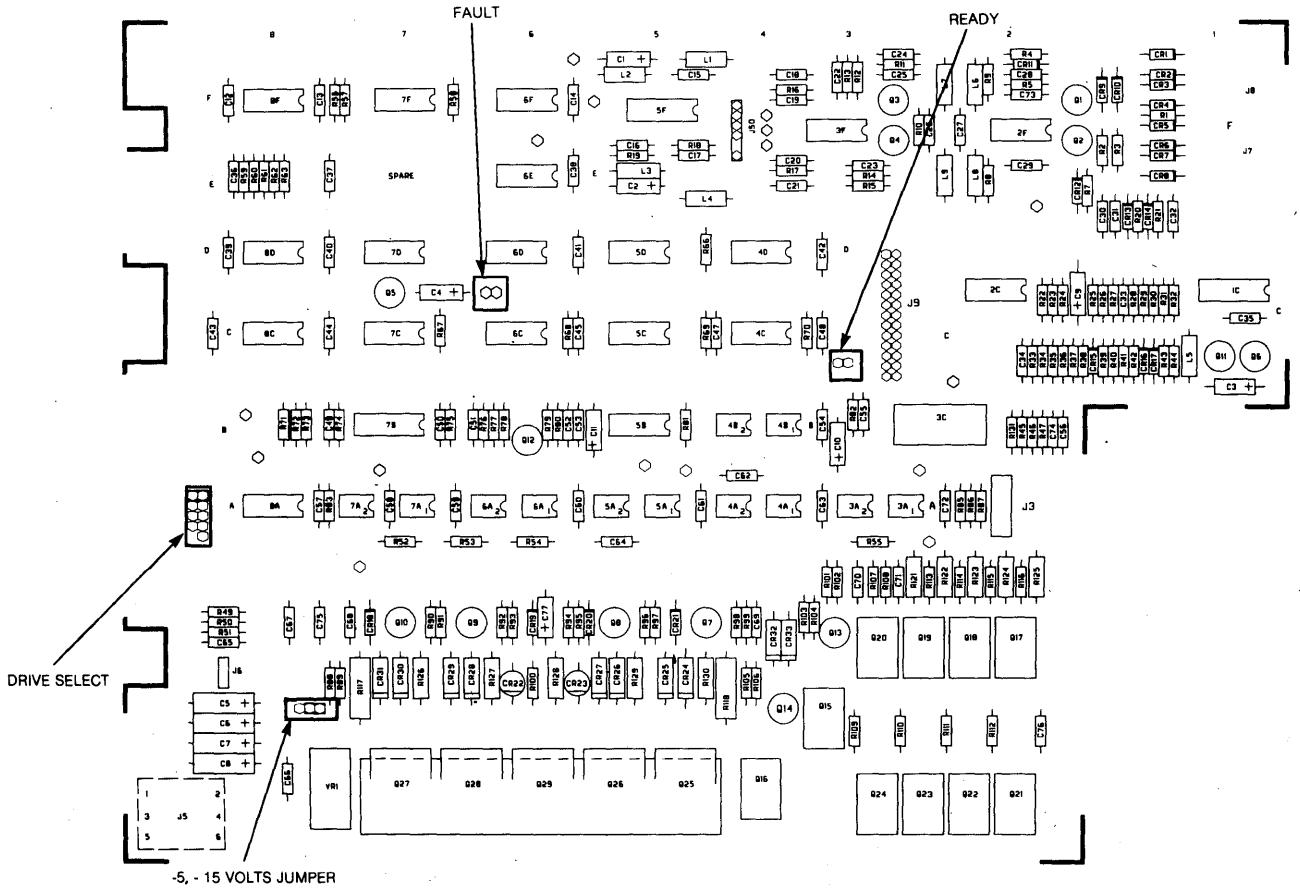


Figure 22 SA1000 Control PCB

10.0 SA1000 UNPACKAGING INSTRUCTIONS

Attention: These instructions must be carefully followed to insure the proper operation of the drive.

1. The spindle lock (P/N 60464) must be removed before applying AC power to the drive (reference the figure below). Retain the lock for reinstallation prior to transporting the drive.

2. To prevent possible damage to the heads and media, rotate the spindle in a clockwise direction only.

3. To isolate the AC ground from logic ground, remove the motor ground strap (P/N 60060).

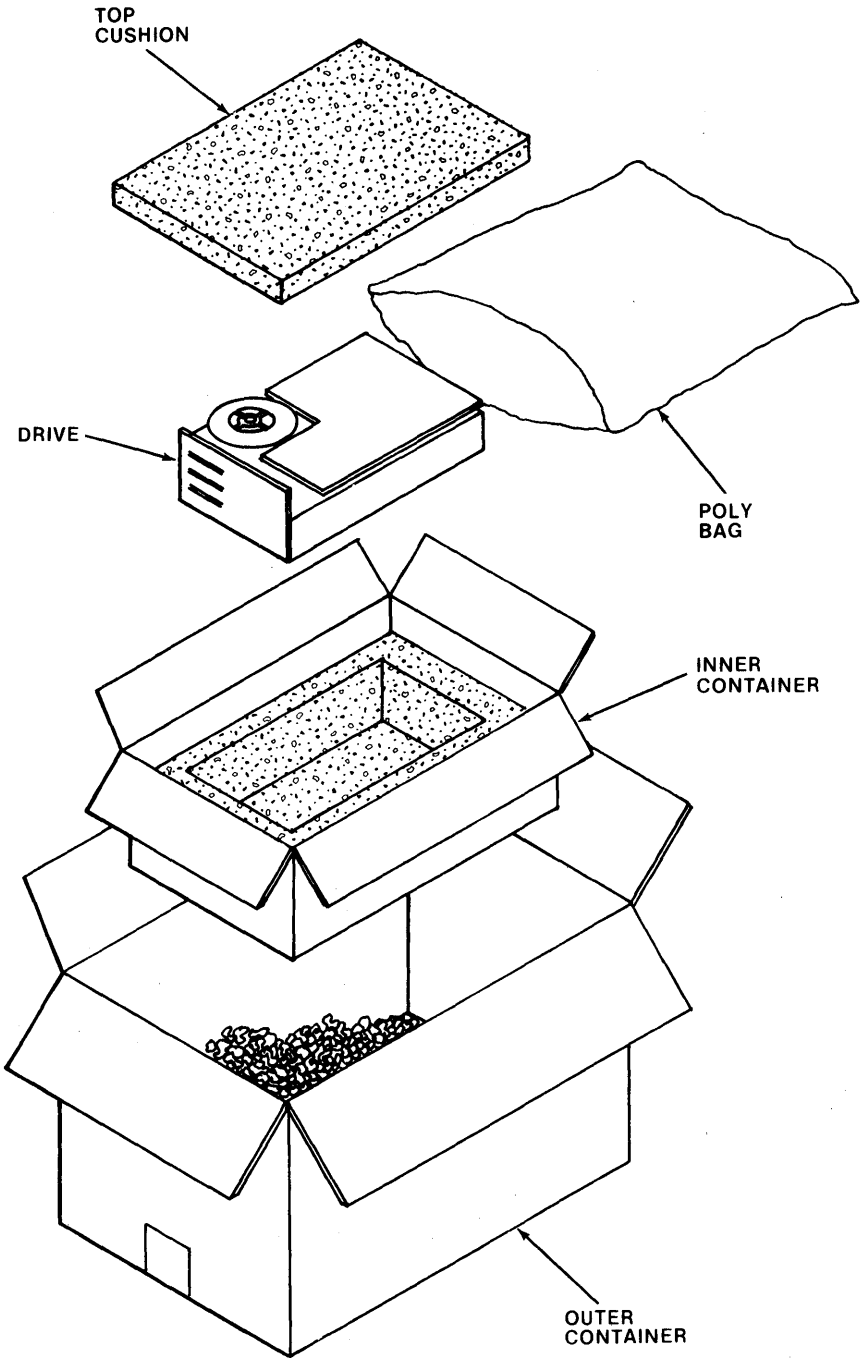


Figure 23 SA1000 Packaging

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