RALINK TECHNOLOGY, CORP.

RT5350

Contents

List of Figures

1 GENERAL DESCRIPTION

This document provides the detailed RT5350 AP mechanical & interface specifications for application. The subsequent photos are of the RT5350 AP.

Figure 1: RT5350 AP Top Side

Figure 2: RT5350 AP Bottom Side

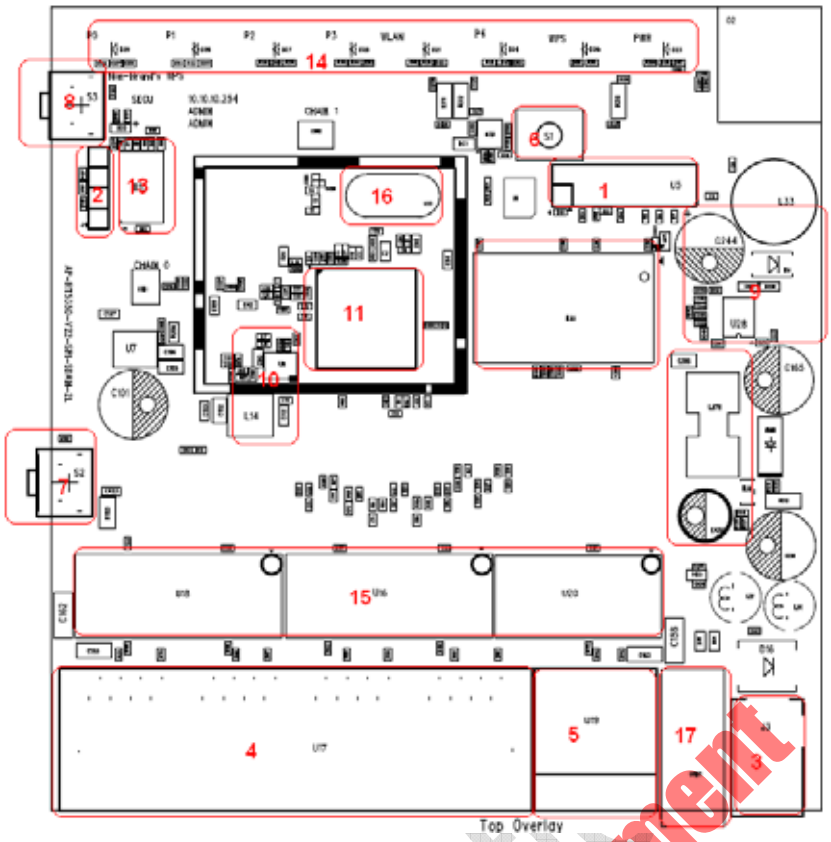


Figure 3: RT5350 AP Placement Top Side

Figure 4: RT5350 AP Placement Bottom Side

Item	Description	Note
Connector		
1	RT5350 JTAG Port	Header pin 2X7
2	RT5350 Console Port	Header pin 1X4
3	Power Jack	5V Input
4	4 Port RJ-45	LAN Ports
5	1 Port RJ-45	WAN Port
Push Button		
6	Reset Push Button	
7	Factory Default Push Button	
8	WPS Push Button	Temporary useless
DC-DC PWM Switching Power		
9	Step-Down regulator, 2A, 380KHz	5V to 3.3V
MOSFET		
10	MOSFET, N and P-ch, N-Id=3A	1.85V for RT5350
IC		
11	11n SoC, 1T1R, RT5350	
12	SDRAM , 16M*16 120MHz, 3.3V	
13	SPI Flash, 4Mbytes	
LED		
14	LED, green	
Transformer		
15	X'MER, 1:1, 5 port+	4 LAN + 1WAN
X'tal		
16	XTAL, 20MHz, CL=15pF, 15ppm	For RT5350
USB		
17	USB 2.0 port 0	Host

These abbreviations are used in this document:

Type	Description
I	indicates signal is input
O	indicates signal is output
I/O	indicates signal is bidirectional
OD	indicates signal is open drain
P	indicates signal is power
#	All pin names with the _# suffix are asserted low
D+	Differential pair positive
D-	Differential pair negative
NC	No Connect

1.1 RT5350 Information

Chip	RT5350
Front-end	1-TX/1-RX
Band	2.4 GHz
Package	TFBGA-196 ball
Dimension	12mmx12mm
CPU	360/350/320/300 MHz
SDRAM	16-bit SDRAM (up to 64 Mbytes)
SPI Flash	Yes
NOR Flash	No
Ethernet	Embedded a 5-port 10/100Mbps Ethernet switch and a 5-port UTP PHY
USB 2.0	YES, USB 2.0 host/Device x1

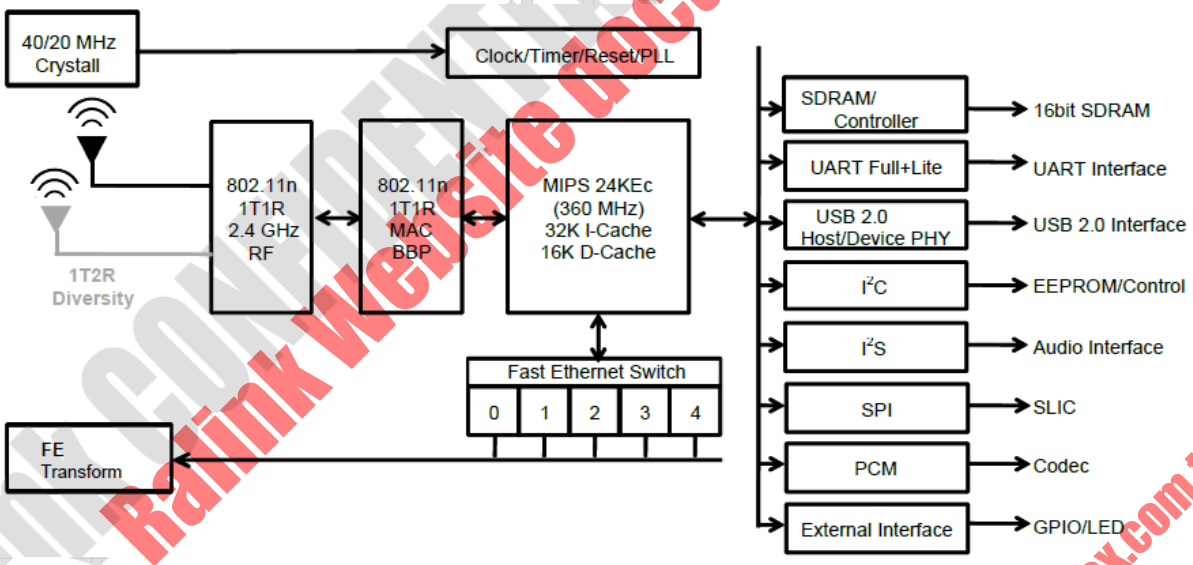


Figure 5: RT5350 Function Block Diagram

2 SYSTEM CONNECTOR

This section provides information about the RT5350 AP system connector pin-out definitions for different applications.

2.1 Pin-Out Definition for USB Port (5V)

The subsequent table provides the system connector pin definitions for USB AP interface with 5V supply.

Pin #	Name	Type
USB Port 0		
1	5V	P
2	USBPHY0_PADM	D-
3	USBPHY0_PADP	D+
4	GND	P

USB UPHY_VBUS/UPHY_ID in each project

Project	RT3052/ RT3050/RT3350	RT3883/ RT3662	RT3352	RT5350
Type (OTG / non-OTG)	OTG	non-OTG	non-OTG	non-OTG
Need 5V power for UPHY_VBUS	Yes	No	No	No
USB0 Host/Device	by resistors for UPHY_ID pull Low : Host pull High : Device	by software	by software	by software
USB1 Host/Device	No USB1	Host only	Host only	No USB1
VBUS voltage input spec	5.5V – 4.5 V (5V +/-10%)	N/A	N/A	N/A

Figure 6: USB UPHY_VBUS/UPHY_ID in each project Table

2.2 Signals Functional Description

The subsequent table provides the system pin definitions for **USB Port interface** with 3.3V/1.2V supply.

IC Ball Name	Ball Number	Description
UPHY0_VDDA_V33A	N11	3.3v USB PHY analog power supply
UPHY0_VDDL_V12D	P13	1.2v USB PHY digital power supply
UPHY0_VRES	P11	Connect to an external 8.2K Ohm resistor for band-gap reference circuit
UPHY0_PADM	N12	USB data pin Data-
UPHY0_PADP	P12	USB data pin Data+

The subsequent table provides the system pin definitions for **5-Port PHY interface**.

Ball Name	Ball Number	Description
EPHY_RXN_P0	L5	10/100 PHY Port #0 RXN
EPHY_RXP_P0	M5	10/100 PHY Port #0 RXP
EPHY_TXN_P0	N5	10/100 PHY Port #0 TXN
EPHY_TXP_P0	P5	10/100 PHY Port #0 TXP
EPHY_RXN_P1	L6	10/100 PHY Port #1 RXN
EPHY_RXP_P1	M6	10/100 PHY Port #1 RXP
EPHY_TXN_P1	N6	10/100 PHY Port #1 TXN
EPHY_TXP_P1	P6	10/100 PHY Port #1 TXP
EPHY_RXN_P2	N7	10/100 PHY Port #2 RXN
EPHY_RXP_P2	P7	10/100 PHY Port #2 RXP
EPHY_TXN_P2	M7	10/100 PHY Port #2 TXN

Ball Name	Ball Number	Description
EPHY_TXP_P2	L7	10/100 PHY Port #2 TXP
EPHY_RXN_P3	M8	10/100 PHY Port #3 RXN
EPHY_RXP_P3	L8	10/100 PHY Port #3 RXP
EPHY_TXN_P3	N8	10/100 PHY Port #3 TXN
EPHY_TXP_P3	P8	10/100 PHY Port #3 TXP
EPHY_RXN_P4	N9	10/100 PHY Port #4 RXN
EPHY_RXP_P4	P9	10/100 PHY Port #4 RXP
EPHY_TXN_P4	M9	10/100 PHY Port #4 TXN
EPHY_TXP_P4	L9	10/100 PHY Port #4 TXP
EPHY_REF_RES	P4	Connects to an external resistor to provide accurate bias current.

3 AP CONNECTION

3.1 Critical Signal Connections

Following are suggestions for critical signal connections.

RT5350 Pin #	RT5350 Pin Name	Description
L1	EPHY_LED1_N	If these pins are also for EPHY LED(low active) controls, power on boot strapping must with 100-ohm resistor for pull-low setting
L4	EPHY_LED2_N	
M1	EPHY_LED3_N	
M4	EPHY_LED4_N	
K1	WLAN_LED_N	If this pin is also for activity LED(low active) indication, power on boot strapping must with 100-ohm resistor for pull-low setting
N2	TXD2	The TXD2 is also for power on boot strapping setting, improper connection will result system cannot boot issue. Follow below procedure in either can avoid the system cannot boot issue. 1. Remove the Ralink console port adapter LED (D1) when the adapter is plugged into the system before system boot. Figure 13 is console adapter circuit. 2. After system is boot up, then plug the console adapter.

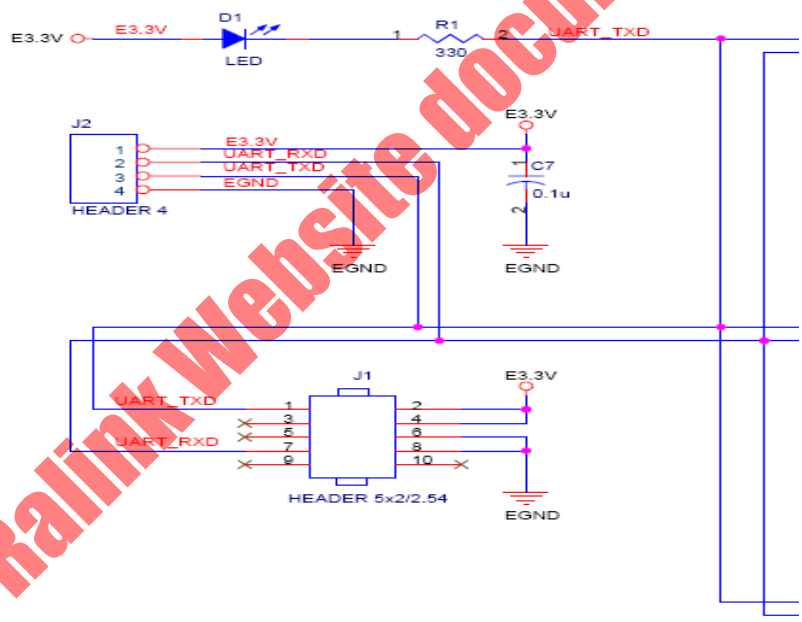


Figure 7: Console port adapter circuit

3.2 RT5350 PLL Loop Filter Connection

RT5350 Pin #	RT5350 Pin Name	Boot Strapping
A6	PLL_VC_CAP	This is PLL external loop filter capacitor. Improper capacitor will result EVM degrade problem. Suggest referring the suggested vendor parts in the reference design.

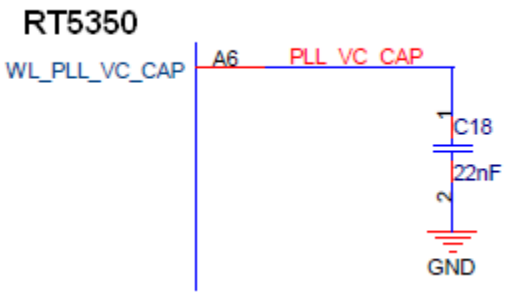


Figure 8: PLL external loop filter

3.3 RT5350 EPHY_REF_RES Connection

RT5350 Pin #	RT5350 Pin Name	Boot Strapping
P4	EPHY_REF_RES	Connects to an external resistor to provide accurate bias current.

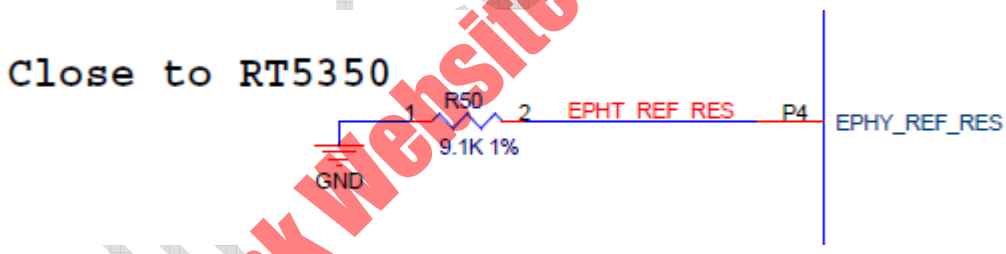


Figure 9: EPHY_REF_RES

4 CONSOLE PORT

This section includes the subsequent information about the RT5350 AP console port:

- Pin-out definition
- Console port connection
- PC COM Port Setting

4.1 Pin-Out Definition

Pin #	Pin Name	Type	Description
1	3.3V	P	3.3-V supply input.
2	RXD2	O	UART2 Receive Data.
3	TXD2	I	UART2 Transmit Data.
4	GND	I	Ground pin.

4.2 Console Port Connection

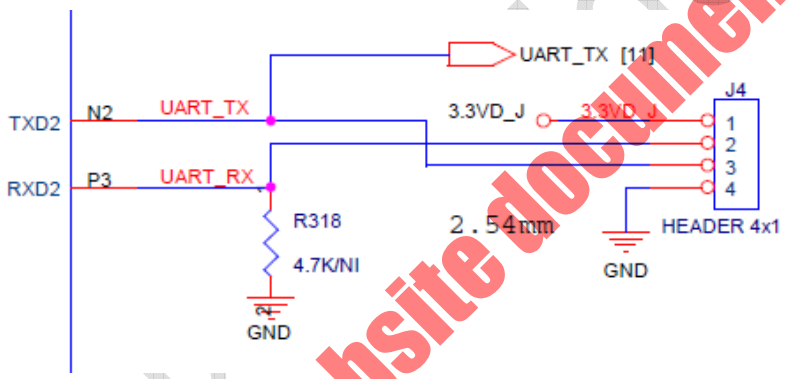


Figure 10: Console Port Connection

4.3 PC COM Port Setting

Figure 11: PC COM port setting

5 JTAG PORT

This section includes the subsequent information about the RT5350 AP JTAG port:

• Pin-out definition

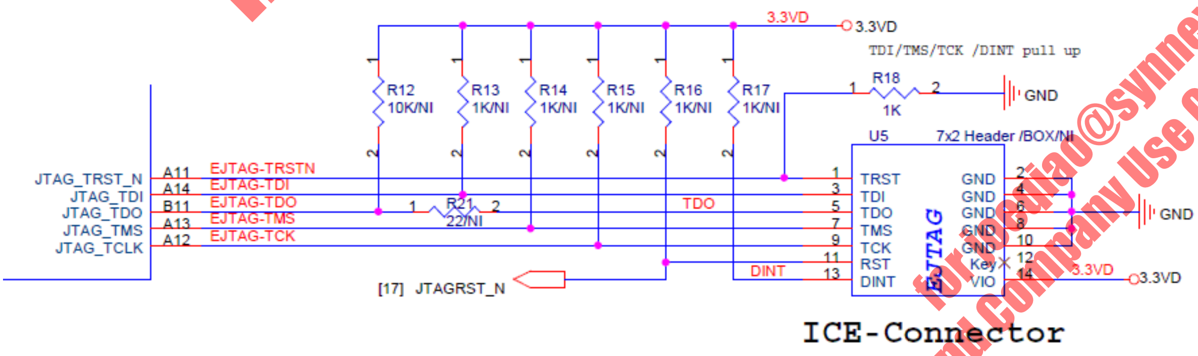
• JTAG Port Connection

5.1 Pin-Out Definition

Pin #	Name	Pin #	Name
1	EJTAG-TRSTN	2	GND
3	EJTAG-TDI	4	GND
5	EJTAG-TDO	6	GND
7	EJTAG-TMS	8	GND
9	EJTAG-TCK	10	GND
11	RST	12	Key
13	DINT	14	3.3V

Pin #	Pin Name	Type	Description
1	EJTAG-TRSTN	I	EJTAG Test Reset.
2,4,6,8,10	GND	P	Ground pin.
3	EJTAG-TDI	I	EJTAG Test Data In.
5	EJTAG-TDO	O	EJTAG Test Data Out.
7	EJTAG-TMS	I	EJTAG Test Mode Select.
9	EJTAG-TCK	I	EJTAG Test Clock
11	RST	I	System reset signal.
13	DINT	I	EJTAG Debug Interrupt.
14	VIO	P	3.3-V supply to ICE.

5.2 JTAG Port Connection



6 GPIO USAGE

RT5350 Ball #	Ball name	Function	TYPE	Description
M3	GPIO14/RIN	WPS_LED/UARTF	O	Use for WPS LED on Reference board.
K2	GPIO8/TXD	Boot Strapping/UARTF	I	Boot Strapping
L3	GPIO13/DSR_N	SECU_LED/UARTF	O	Use for security LED on Reference board.
B12	GPIO0	WPS_PB	I	WPS Push Button.
N3	GPIO10/RXD	RST_PBC/UARTF	I	Factory Default Push Button.
K4	GPIO9/CTS_N	PWR_LED/UARTF	O	Use for power LED on Reference board.
P2	GPIO7/RTS_N	GPIO7/UARTF	I/O	NC
N4	GPIO11/DTR_N	GPIO11/UARTF	I/O	NC
J4	GPIO12/DCD_N	GPIO12/UARTF	I/O	NC

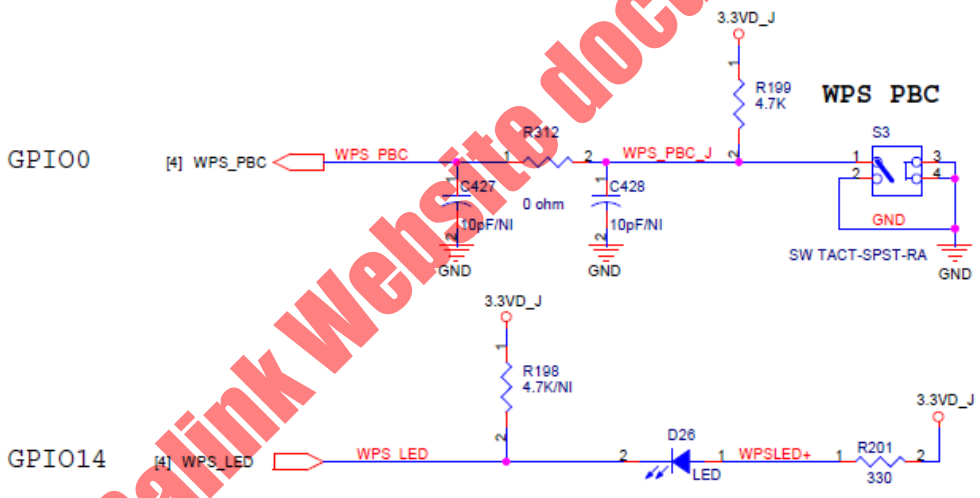


Figure 12: WPS switch connection

7 BOOT STRAPPING

This section provides information on the RT5350 boot strapping requirements for an AP application.

7.1 Boot Strapping Definition for AP

The subsequent table shows boot strapping information for RT5350 AP applications.

The settings are based on following configuration:

- RT5350 5-PORT 10/100 SWITCH
- SDRAM is 256Mbit (16M*16bit) and configuration is from the boot strapping signals
- With SPI flash 4Mbytes.

RT5350 Pin Name	Boot Strapping Signal Name	Description	RT5350 Setting
SPI_CLK	XTAL_FREQ_HI	0: 20 MHz (default) 1: 40 MHz	0
WLAN_LED_N	BIGENDIAN	0: Little-endian(default) 1: Big-endian	0
EPHY_LED4_N	DRAM_FROM_EE	0: DRAM configuration from boot strapping. 1: DRAM configuration(size/width) from EEPROM	0
{ EPHY_LED3_N , EPHY_LDE2_N}	DRAM_SIZE	INIC/AP(SDR) 0: 2 MB/8 MB 1: 8 MB/16 MB 2: 16 MB/32 MB, 32 MB*2 3: 32 MB	10
{EPHY_LED1_N , EPHY_LED0_N}	CPU_CLK_SEL	CPU Clock Select 0: 360 MHz (default) 1: Reserved 2: 320 MHz 3: 300 MHz	00
{ SPI_MOSI , TXD2, TXD}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. In non-test/debug operation, 0: Normal mode (boot from SPI serial flash) (default) 1: i-NIC USB mode 2: Reserved 3: Reserved 4: Reserved 5: i-NIC PHY mode 6: Scan mode 7: Debug/test mode	000

8 LAYOUT GUIDELINE DETAILS

This application note shows a detailed design guide for the RT5350 chipset. The best location for specific components of the chipset (i.e. decoupling capacitors, power traces, RF section, SDRAM, Ethernet, etc.) are shown here. Obeying the guidelines makes performance better and prevents the negative effect of noise.

8.1 RT5350 Power Section

This table provides RT5350 AP Important Power Pins.

RT5350 Ball #	Ball name	I/O	Description
LDO Balls of Digital partial			
G2	LDO_V18A	P	1.8 V power input for internal MOS
G1	VOUT_1P2	P	1.2 V regulation output
G3	LDOSEL	I	Internal/External LDO select Default: floating, use internal Tied to 3.3: use externally.
H3	EXT_LDO_1P2	P	Gate drive for external BJT
H2	DCDC_V33A	P	3.3 V analog power
G4	COMP	A	This pin is the error amplifier output and combines with the FB pin to compensate the voltage control.
H4	FB	A	Programmable feedback reference voltage for SW regulator and compensation network of the error amplifier
H1	UGATE	A	Gate drive for external upper MOSFET
J1	LGATE	A	Gate drive for external lower MOSFET
J2	DCDC_V33D	P	3.3 V power supply only for gate driver of SW (Ipeak<200 mA; Iavg<20 mA)
G2	LDO_V18A	P	1.8 V power input for internal MOS
G1	VOUT_1P2	P	1.2 V regulation output
G3	LDOSEL	I	Internal/External LDO select Default: floating, use internal Tied to 3.3: use externally.
PLL Power Balls			
B10	PLL_DVDD_V12D	P	1.2 V digital power supply to PLL
A10	PLL_AVDD_V12A	P	1.2 V analog power supply to PLL

RT5350 Ball #	Ball name	I/O	Description
RF Power Balls			
A2	WL_RF0_2G_INP	I	2.4 GHz RX0 input (positive)
A3	WL_RF0_2G_INN	I	2.4 GHz RX0 input (negative)
B1	WL_RF0_PA_V33P	P	3.3 V supply for RF channel 0
C1	WL_RF0_PA_OUTP	O	2.4 GHz TX PA output (negative)
D1	WL_RF0_PA_OUTN	O	2.4 GHz TX0 output (negative)
E1	WL_RF0_PA_V33N	P	3.3 V supply for RF channel 0
E3	WL_RF0_PA1_V33A	P	3.3 V supply for RF0 PA1
B5	WL_RF0_IF_V12A	P	1.2 V supply for IF0
B3	WL_RF0_RF_V12A	P	1.2 V supply for RF0
B9	WL_ADC_V12	P	1.2 V supply for ADC analog blocks
A5	WL_RF_BB1_V12A	P	1.2 V supply for analog baseband
C9	WL_RF_BB2_V12A	P	1.2 V supply for analog baseband
B8	WL_BG_RES_12K	I/O	External reference resistor (12K ohm)
A9	WL_BG_V33A	P	3.3 V supply for band gap reference
C8	WL_LDORF_OUT_V12	O	LDO 1.2V 200 mA output for RF core
C7	WL_LDOPLL_OUT_V12	O	LDO 1.2V 200 mA output for PLL core
A8	WL_LDORF_IN_VX	I	LDO 1.5~2 V 300 mA input for RF core and PLL
A7	WL_PLL_X1	I	Crystal oscillator input
B7	WL_PLL_X2	O	Crystal oscillator output
B6	WL_PLL_V12A	P	1.2V Supply for PL
A6	WL_PLL_VC_CAP	I/O	PLL external loop filter
C6	WL_VCO_VCO_V12A	P	1.2 V Supply for VCO output buffer
Power Balls			
F5,G5,D10	SOC_IO_V33D	P	3.3 V digital I/O power supply
F10,G10,H10	SDRAM_IO_V33D	P	3.3 V/1.8 V SDRAM I/O power supply
H5,J5,F9,G9,H9	SOC_CO_V12D	P	1.2 V digital core power supply

RT5350 Ball #	Ball name	I/O	Description
K5,K6,K7	EPHY_V33A	P	3.3 V I/O power supply for

8.1.1 RT5350 power topology

Following is RT5350 Power topology.

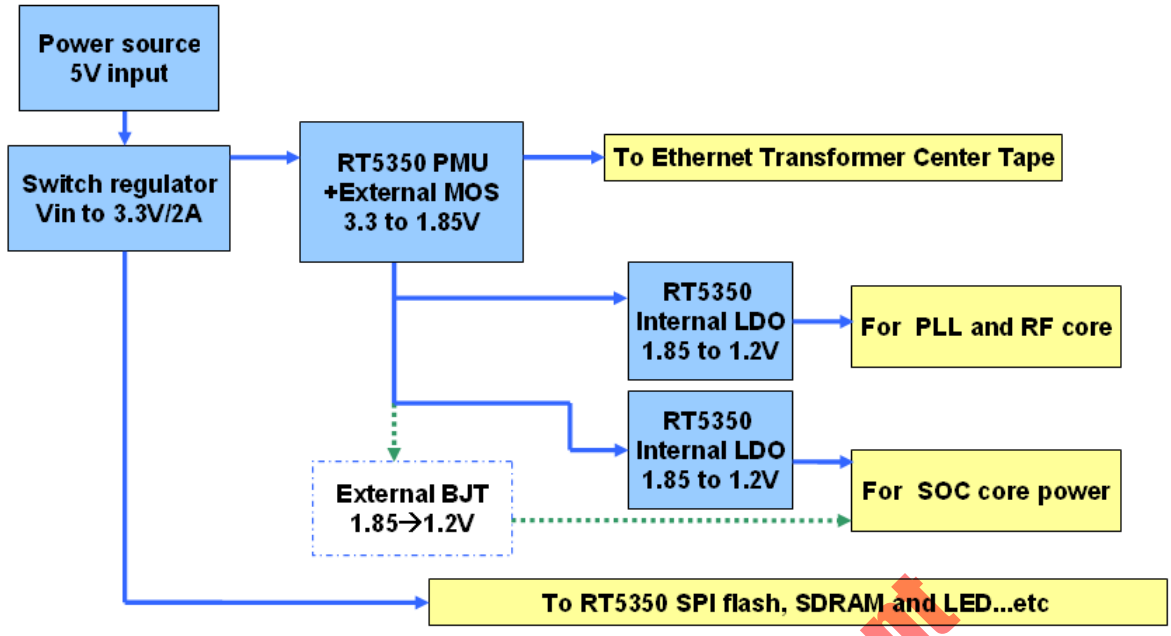
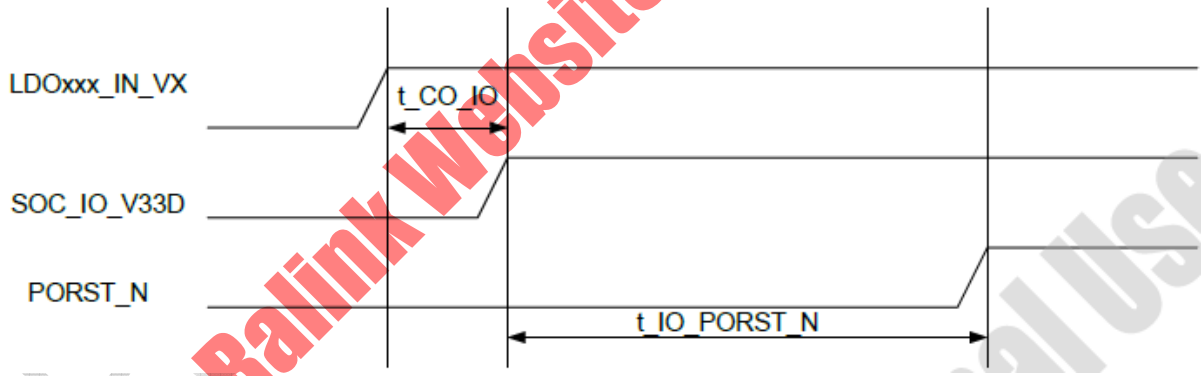


Figure 13: RT5350 Power block

8.1.2 PMU Power Sequence

Following is RT5350 PMU power sequence.



Symbol	Description	Min	Max	Unit	Remark
t_CO_IO	Time between core power on to I/O power on	0	-	ms	
t_IO_PORST_N	Time between I/O power on to PORST_N de-assertion	10	-	ms	

Figure 14: PMU Power Sequence

8.1.3 Rt5350 PMU system SOC_1.8VD DC electrical characteristics

Parameters	Sym	Conditions	Min	Typ	Max	Unit
PMU DC/DC Controller Design Spec	Vcc15		1.45		3.6	V
PMU DC/DC Controller shares with Low Power SDRAM	Vcc15		1.7	1.8	1.95	V
PMU DC/DC Controller shares with Ethernet	Vcc15		1.8	1.85	2.0	V

Figure 15: RT5350 system SOC_1.8VD DC electrical characteristics

8.1.4 Rt5350 PMU system Layout Consideration

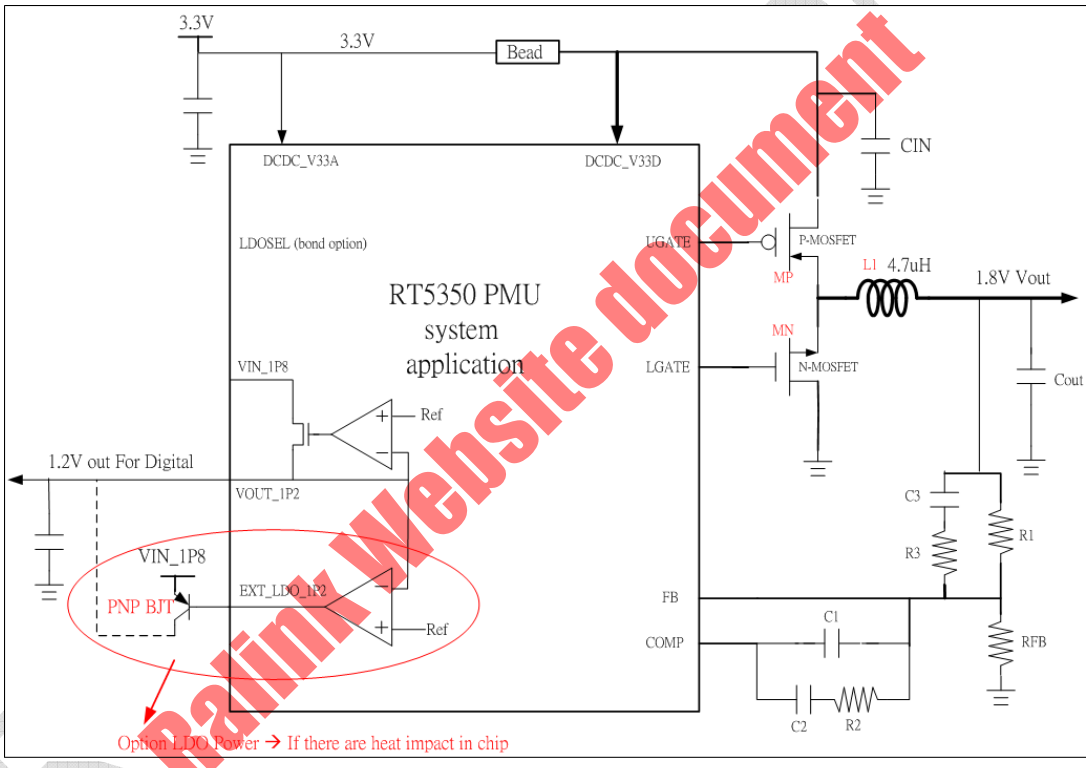


Figure 16: RT5350 PMU Block Diagram

Following is RT5350 PMU system circuit.

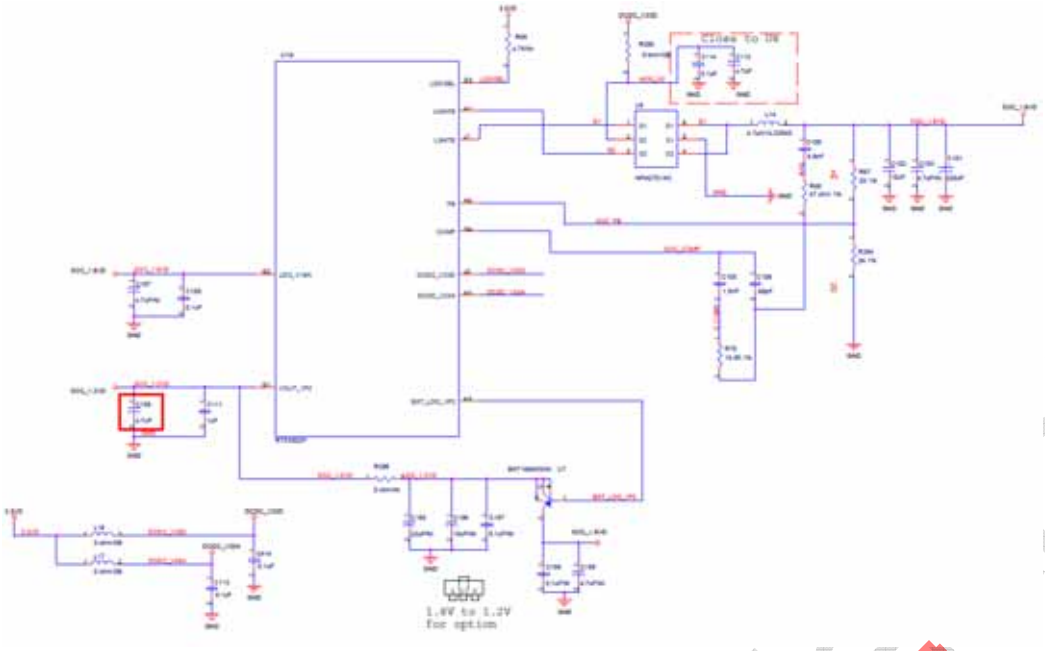


Figure 17: RT5350 PMU system circuit Connection

Following are RT5350 layout suggestions.

a) The wiring traces from the IC UGATE and LGATE pins to the MOSFET gate should be kept short and wide enough to handle the 0.5A of drive current.

b) Minimize the length of the connections between the CIN C112 and the power MOSFET (U8) by placing them nearby.

c) The external power MOSFET should be placed close to the UGATE/LGATE.

d) Tight layout of the external components and short, wide traces minimizes the magnitude of voltage spikes.

e) Place the external compensation components close to the FB and COMP pins.

f) The output path should be kept wide enough to handle the 1.5A of drive current and minimizes the parasitic resistance.

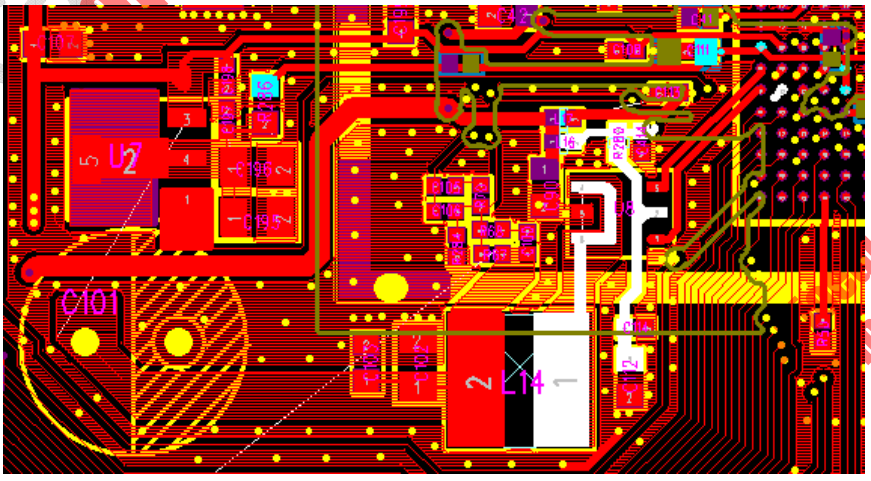


Figure 18: RT5350 PMU Layout

8.1.5 3.3V Connection

The 3.3V power trace will influence the RF performance, so the power trace routing is very important; on the other word 3.3V power trace will influence the EMI, sensitivity, EVM and so on.

a. The 3.3V power trace routing of connect to internal PA pleases fellow RFB design.
b. The capacitor position please fellow please fellow RFB design.
c. The capacitor value pleases fellow RFB design.
d. The detail capacitor values, please sees the RFB schematic.
e. Please put the ground VIA around the power trace path.
f. When the power trace change layer such us layer1 to layer tw2, the reference ground VIA near the power trace.
g. The 3.3V power trace doesn't close to single trace or other power trace, if the layout limited please put some ground VIA between us.
h. The SDRAM 3.3V power trace pleases fellow RFB design and to avoid the SDRAM CLK couple to power trace.

8.1.6 1.2V LDO Regulator Connection

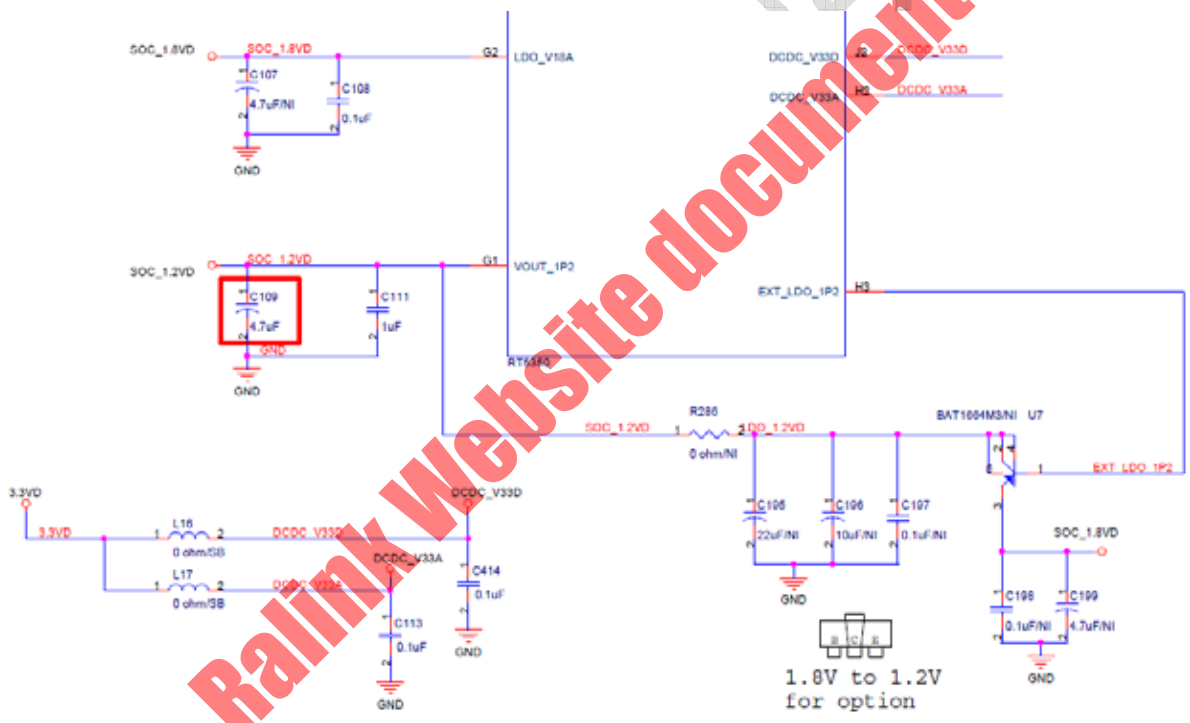


Figure 19: 1.2V LDO Regulator Connection

a) Convert 1.85V to 1.2V output and 500mA output current driving for default requirement.

b) The bond wire and substrate trace of VDA15 and VOUT_1P2 should be as short as possible.

c) The LDO_V18A and VOUT_1P2 path should be kept wide enough to handle the 0.5A of drive current and minimizes the parasitic resistance.

8.1.7 General Digital Power Connection

a) Put capacitors near the power input/output above and use a wide trace to maintain the low impedance for its loading.

b) Use two via as traces change to the bottom layer and the main trace must be wide enough to increase the isolation for different sub-stages.

c) There are independent capacitors for different stages to ensure the performance of each of the sub-stages.

d) The sub-stage capacitors must be put near their pins.

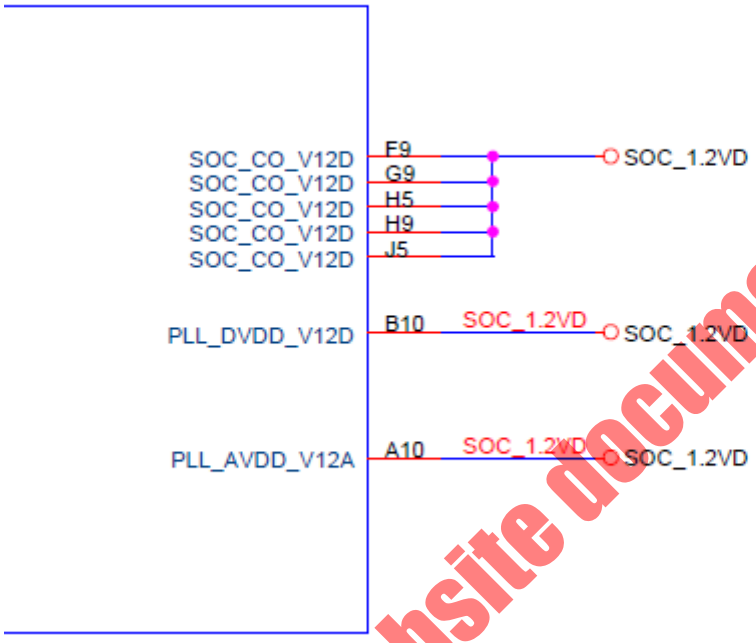


Figure 20: RT5350 Digital Important Power Pins Circuit

8.1.8 RF LDO CONNECTIONS

The healthy capacitor range is from 1uF to 10uF for all internal LDO regulators. This is total capacitance on the LDO regulator outputs, the cap larger than 20uF will pull LDO regulator to unstable region. The suggested value is 4.7uF for digital LDO regulator, 1uF for RF part LDO regulators.

Following are the suggested values for the RF LDOs.

i. 4.7µF for WL_LDORF_IN_VX

ii. 1µF for LDOPLL_OUT_V12, VCO_V12A and PLL_V12A.

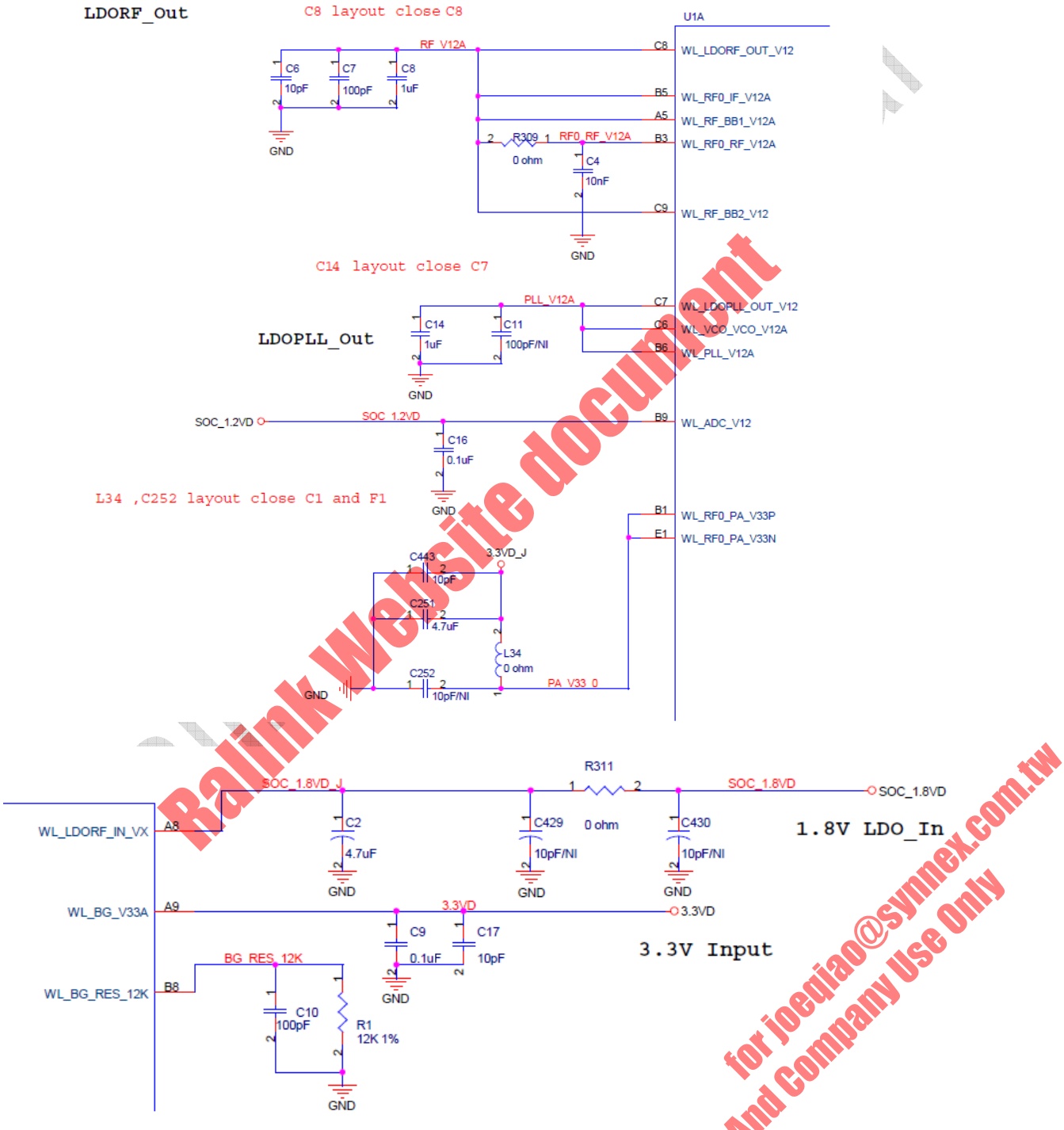


Figure 21: RT5350 RF Important Power Pins Circuit

a). Place C8 near the LDO output pin C8 on the bottom layer and use a wide trace to maintain the low impedance for its loading.
b). C8 and C6 at bottom layer, C7 at top layer and the position as show below.
c). The mapping capacitor value please sees the schematic, and don't remove anyone.

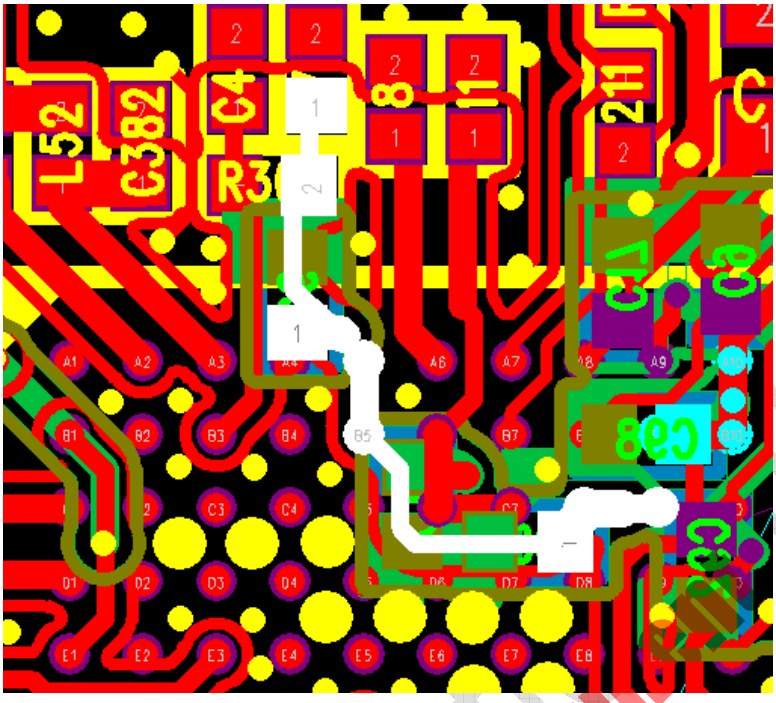


Figure 22: RT5350 RF_V12A Power Pins Layout

PLL_V12A supplies for PLL parts. Using decoupling capacitors to minimize the LDO noise for better PLL performance. Use the following guidelines.

a). Place C14 near the LDO output pin C7.
b). The mapping capacitor value please sees the schematic.

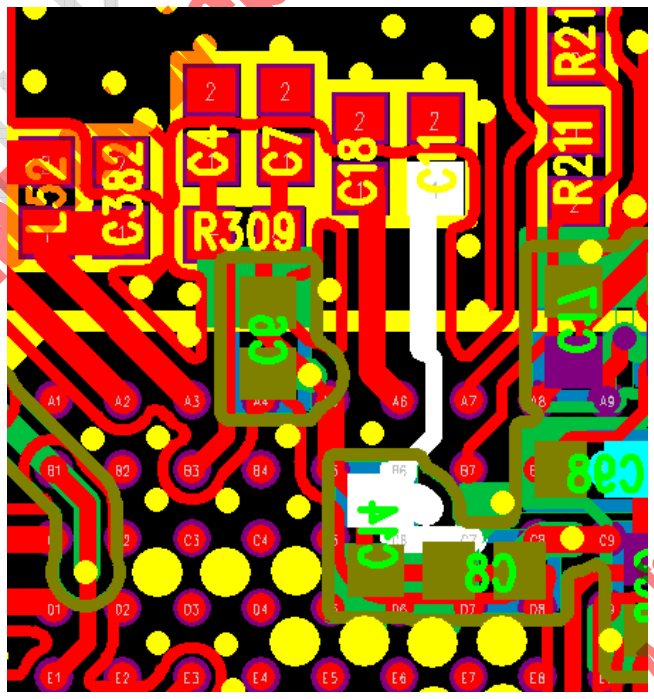


Figure 23: RT5350 RF PLL_V12A Power Pins Layout

8.2 USB Section of RT5350

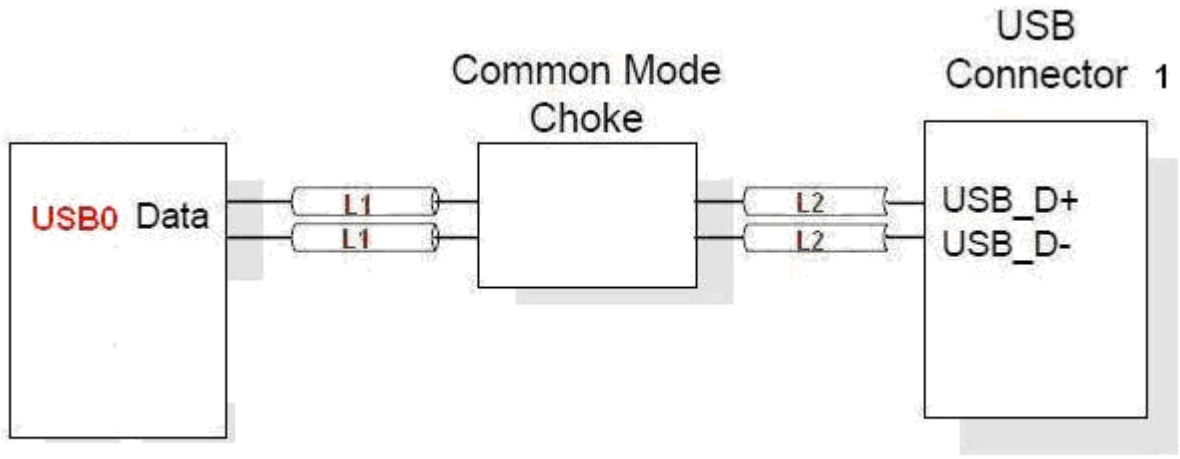


Figure 24: RT5350 USB Port Connection

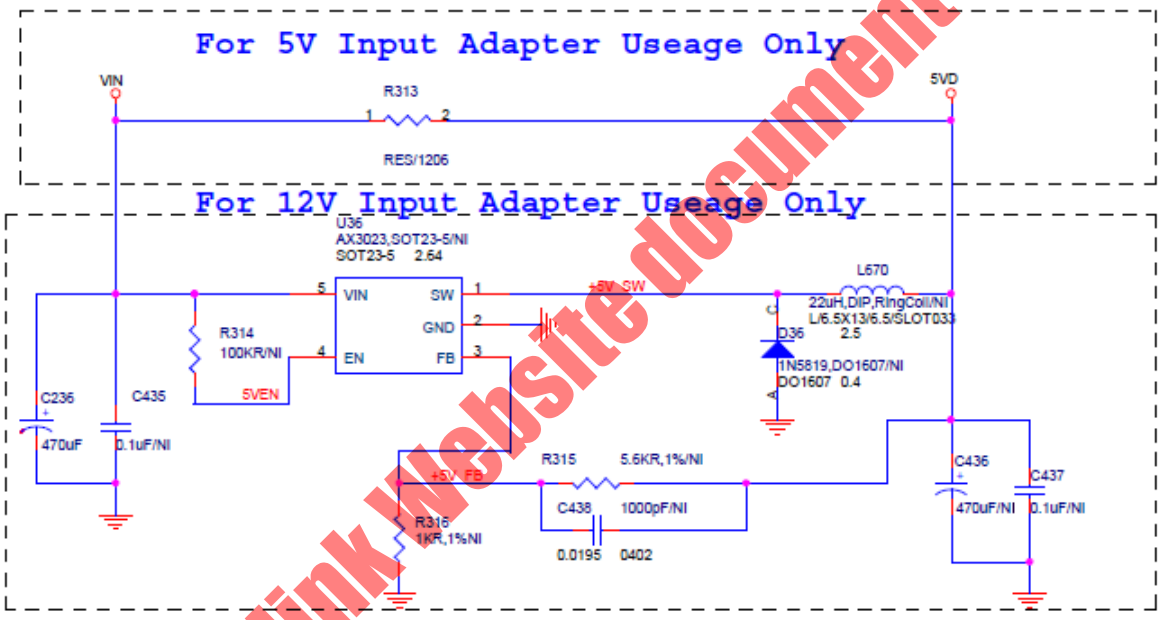


Figure 25: RT5350 USB power circuit diagram

a) The differential pair internal skew (L1, L2) is as short as possible.

b) L[x] impedance (L1, L2) is 90 ohm.

c) Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities.

d) Keep differential traces are the same routing lengths.

e) USB interface connector 5V is directly from VIN power, if used 12V adapter the U35 (DC to DC) must be existence.

8.3 USB Plane for ESD

a) The System ground and Frame ground must have a Minimum Conductor Width of 50 mils (ESD Only).

b) The USB traces must be as short as possible.

c) The USB differential trace impedance is 90 ohm.

d) Do not route USB traces near any noise sources (i.e. crystals and switching regulators).

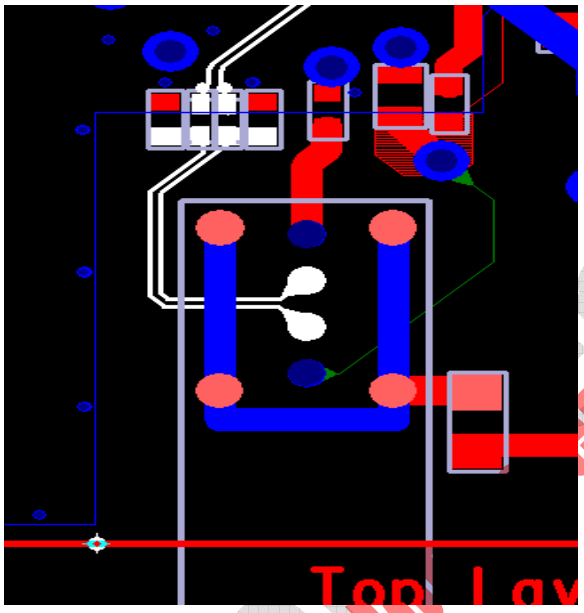


Figure 26: USB Layout for ESD

8.4 SDRAM Interface Connectivity

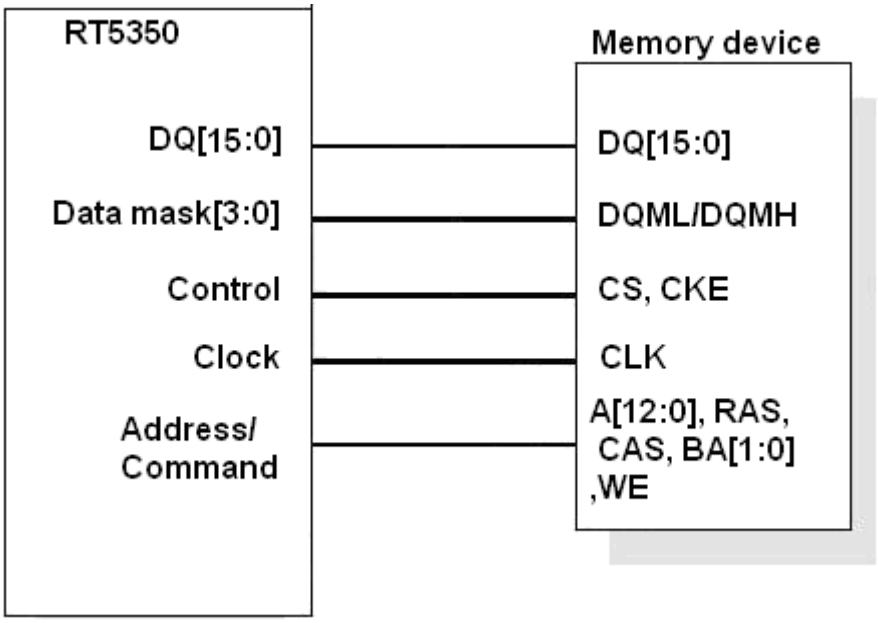


Figure 27: Data Bus 16 bits wide memory devices connected to the controller

8.5 SDRAM Ground Plane

A. Keep a continuous reference plane for each signal over its entire path.

B. SDRAM signals trace on PCB layer 1.

C. Reference Plane fills with PCB layer 2.

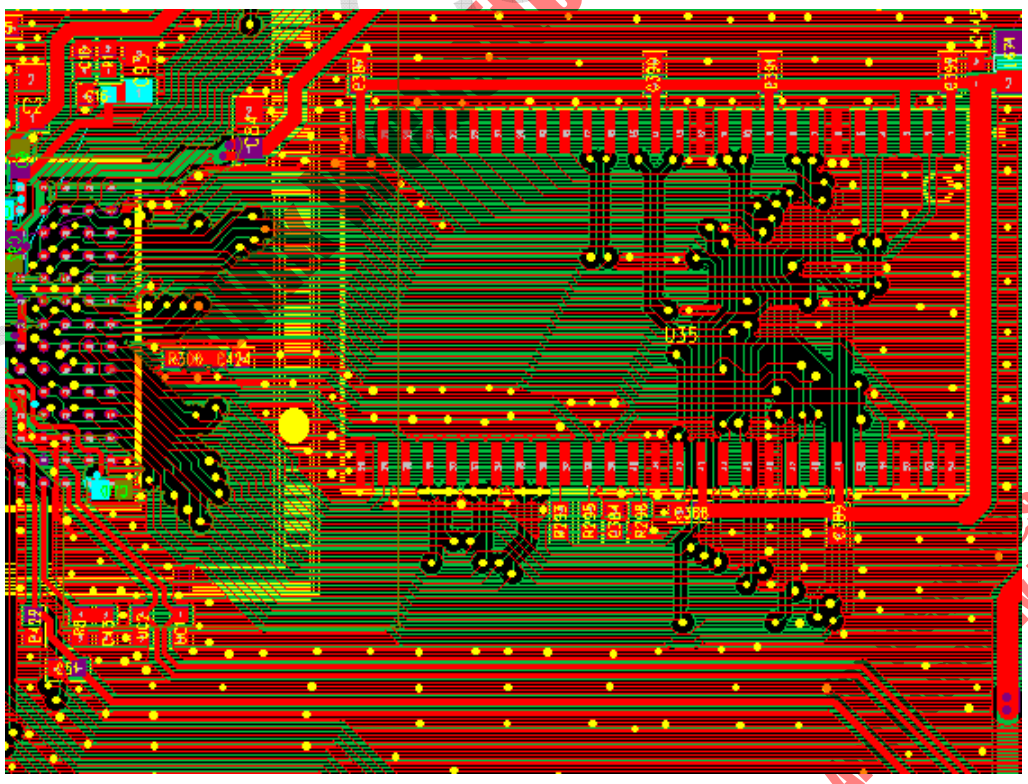


Figure 28: SDRAM Ground plane

8.6 SDRAM Routing Constraints

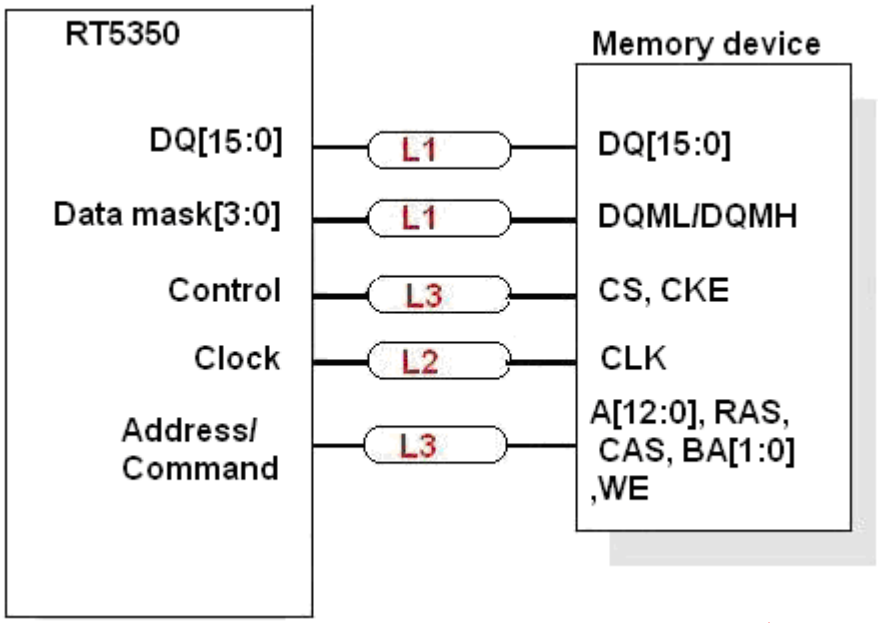


Figure 29: SDRAM 16 bit wide memory diagram

a). Clock cross-signal separation (L2) needs 3 signal widths.

b). Data to Clock skew (L1, L2) is as short as possible.

c). Address/Command/Control to Clock skew (L3, L2) is as short as possible.

d). L[x] impedance (all traces) is 50 ohm.

8.7 Ethernet Medium Dependent Interface (MDI) Routing Constraints

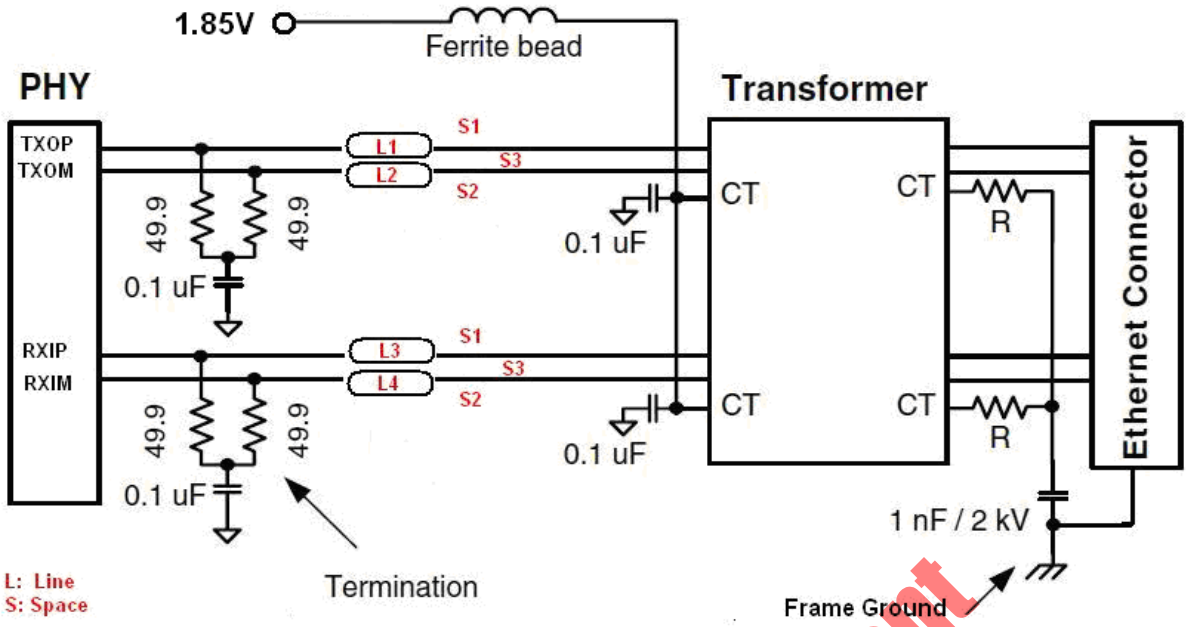


Figure 30: MDI Interface Connectivity

a). Internal-differential separation (S3) needs 1 signal width

b). Differential pair skew (L1, L2 & L3, L4) is as short as possible.

c). Differential pair impedance (L1,L2 & L3,L4) is 100ohm

8.8 Ethernet Power

EPHY_V33A must be adding 0.1u bypass cap before the trace into EPHY power pins, and trace shouldn't share with other 3.3v powers devices after the bypass cap.

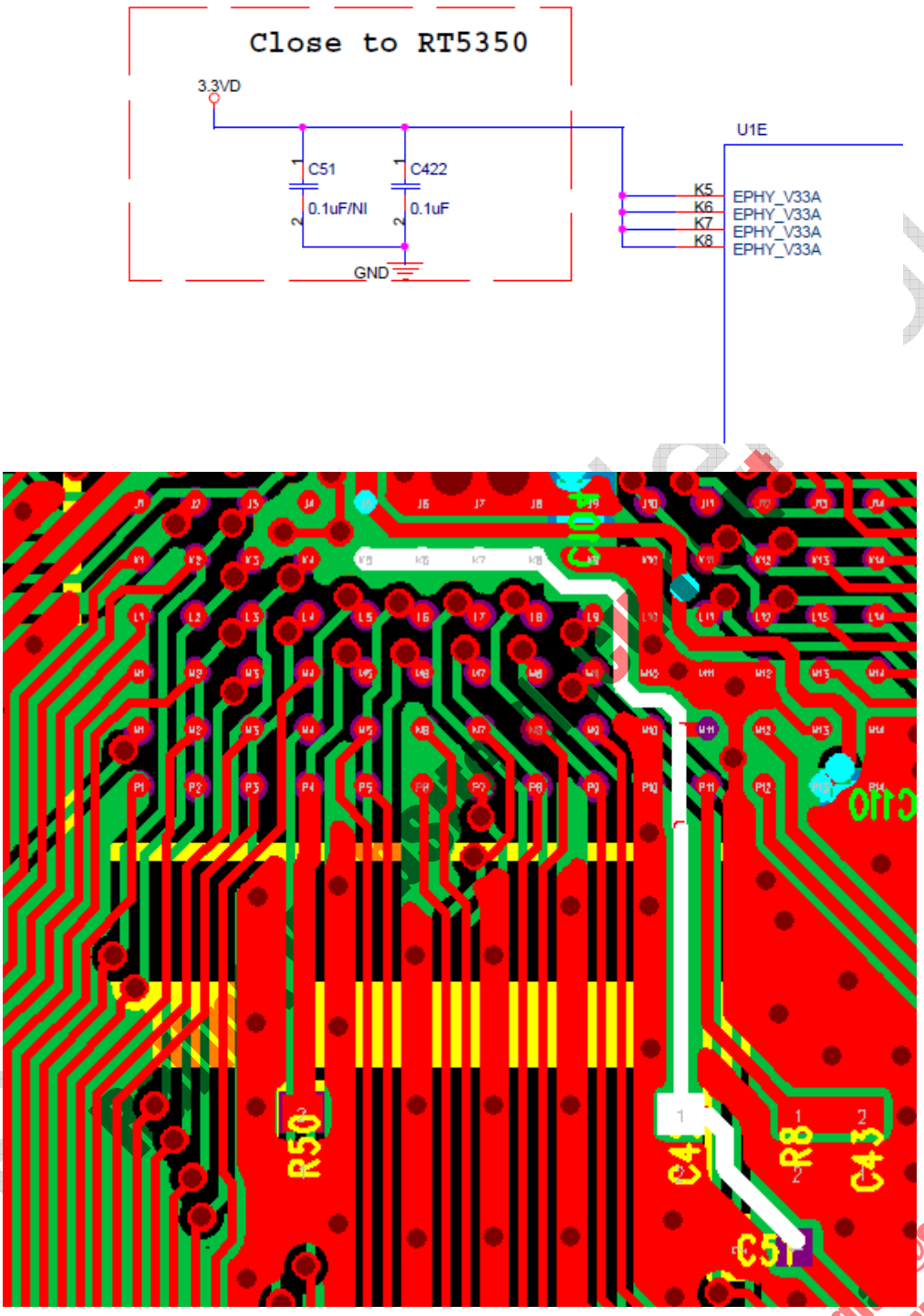
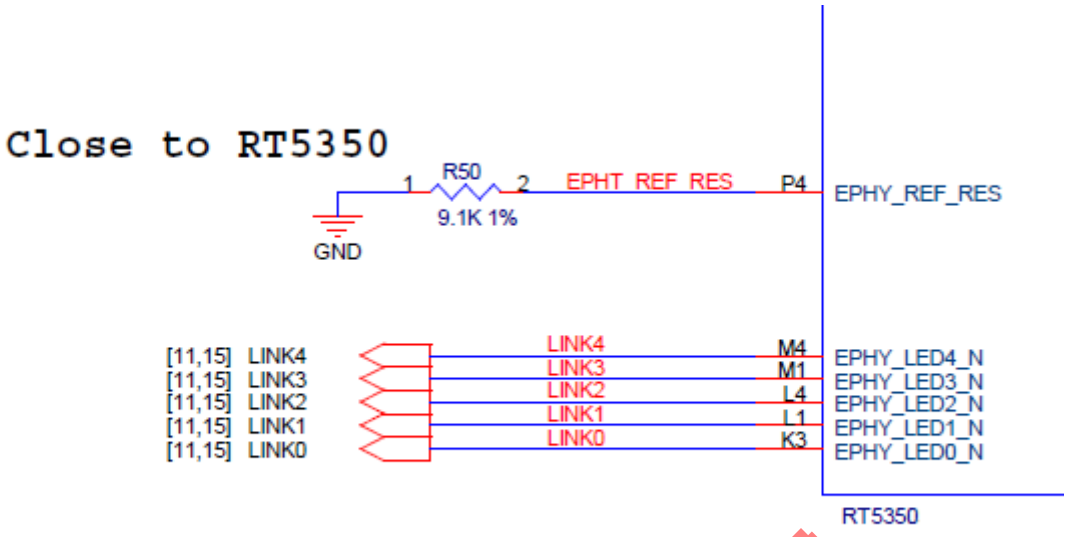


Figure 31: EPHY_V33A power trace

8.9 Ethernet EPHY_REF_RES

R50 needs to close to RT5350 pin “EPHY_REF_RES” pin as short as possible, and should separate from other signal pins with ground shield.



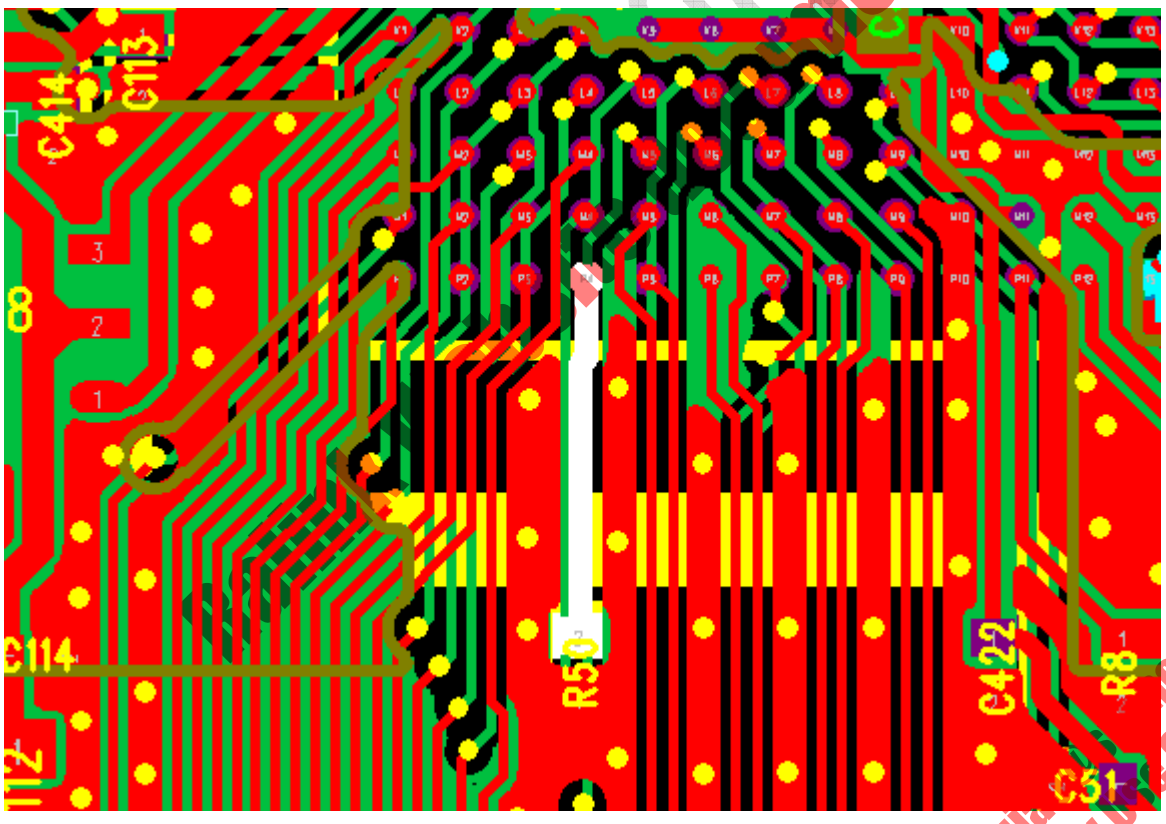


Figure 32: EPHY_REF_RES Signals

8.10 Ethernet Plane for ESD & Hi-Pot

System ground and Chassis ground need to isolate 80 mil at least.

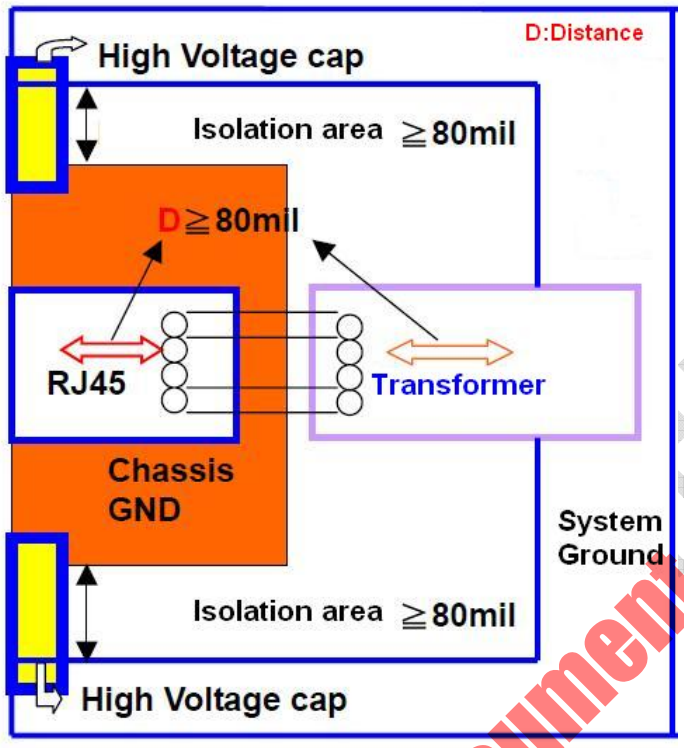


Figure 33: Ethernet Hi-Pot Layout

Ethernet Isolation Layout

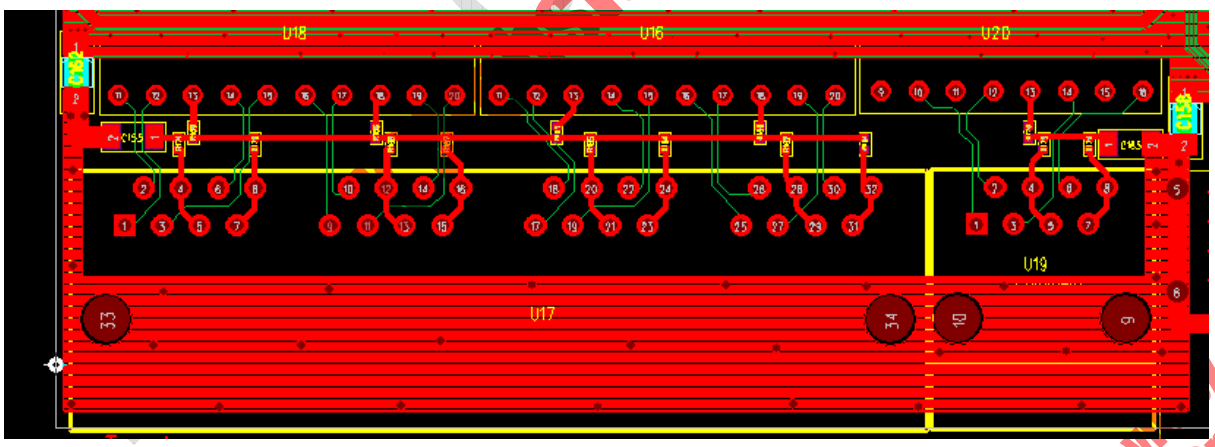


Figure 34: Ethernet Isolation Layout

9 ANTENNA LOCATION

a) The antenna body must be put far away from any noise source (i.e. Power Circuit, Crystal, SDRAM, etc)

b) The Antenna's GND (equal to Antenna Body size) must not be near any other parts. No traces can go through the ground.

10 UPDATE HISTORY

Version	Date	Description	Modified by
1.0	2010/11/24	● 1st release.	Kim
1.1	2011/01/18	● Add system SOC_1.8VD DC electrical characteristics.	Kim
		●	