Welcome to The Hardware Design & Lab!

Fall 2023

Lab 1: Gate-Level Verilog

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National Tsing Hua University

Agenda

- Lab 1 Outline
- Lab 1 Basic Questions
- Lab 1 Advanced Questions
- Basic Concept of Verilog Testbench

Lab 1 Outline

- Basic questions (1.5%)
  - Individual assignment
  - Due on 9/21/2023. In class.
  - Only demonstration is necessary. Nothing to submit.

- Advanced questions (5%)
  - Individual assignment
  - eeclass submission due on 9/28/2023. 23:59:59.
  - Demonstration on your FPGA board (In class, on 10/5/2023)
  - Assignment submission (Submit to eeclass)
    - Source codes and testbenches
    - Lab report in PDF

Lab 1 Rules

- Only gate-level description is permitted
  - Only basic logic gates are ALLOWED (AND, OR, NAND, NOR, NOT)
  - Sorry, no XOR & XNOR
- Please AVOID using
  - Continuous assignment and conditional operators
  - Behavioral operators (e.g., =,+, -, &, |, ^, &&, !, ~….., etc.)

Lab 1 Submission Requirements

- Source codes and test benches
  - Please follow the templates EXACTLY
  - We will test your codes by TAs' testbenches
- Lab 1 report
  - Please submit your report in a single PDF file
  - Please **draw** the gate-level circuits of your designs
    - Remember **not to draw them by hands**
  - Please **explain** your designs in detail
  - Please explain how you test your design
  - What you have learned from Lab 1

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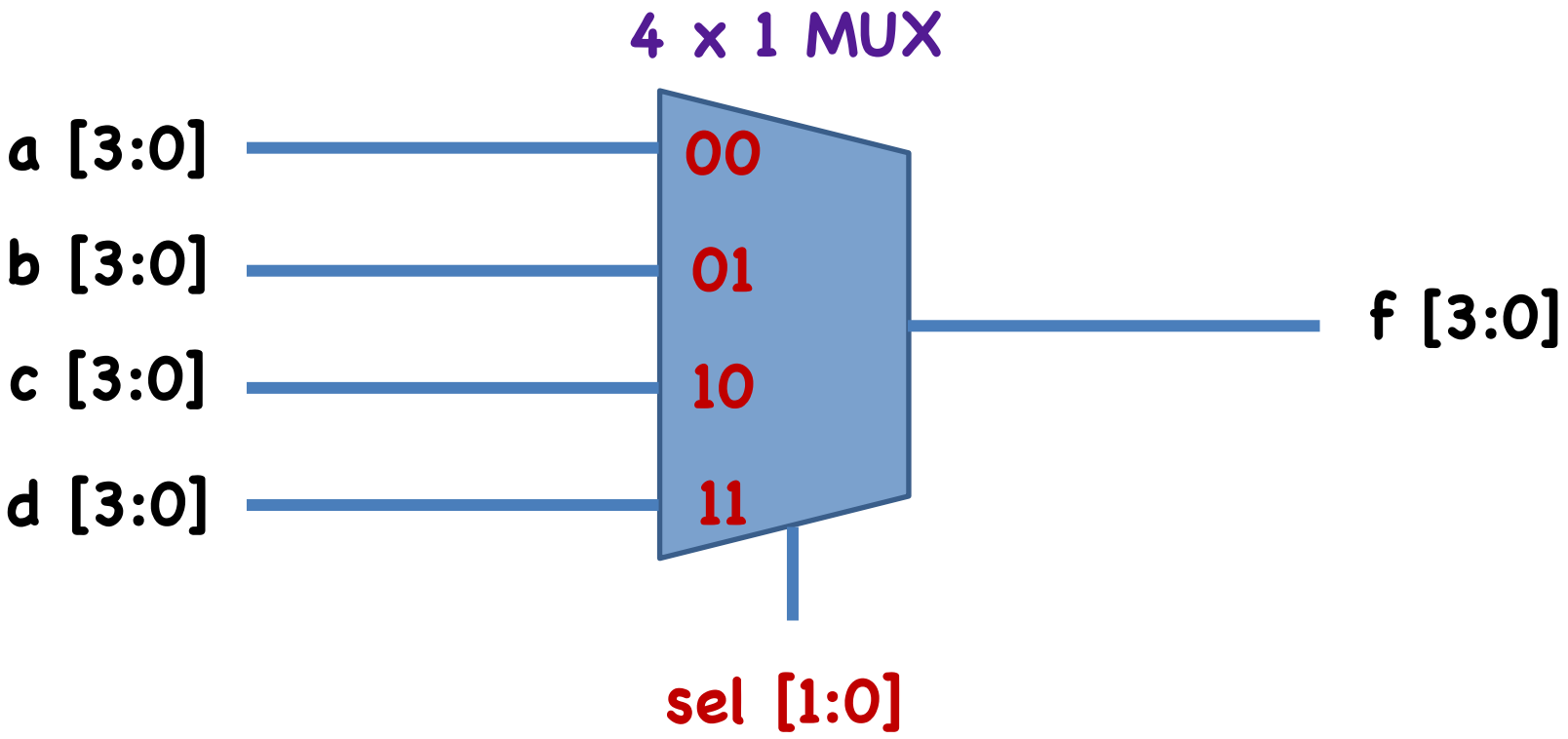
Basic Questions

- Individual assignment
- Verilog questions (due on 9/21/2023. In class.)
  - (Gate-level) 4-bit 4-to-1 multiplexer (abbreviated as MUX)
  - (Gate-level) 1-bit D flip-flop (DFF) with D Latches
- Please demonstrate your work by waveforms

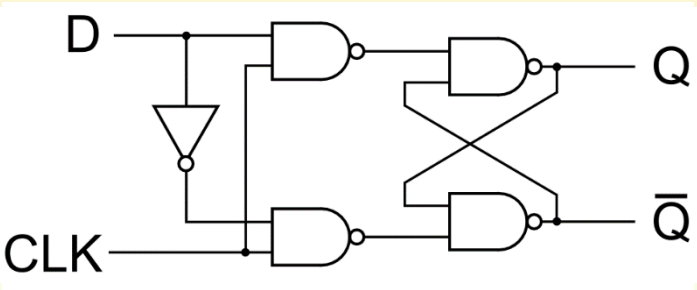
Verilog Basic Question 1

- (Gate-level) 4-bit 4-to-1 multiplexer (MUX)
- Construct your 4-to-1 MUX with three 2-to-1 MUXes

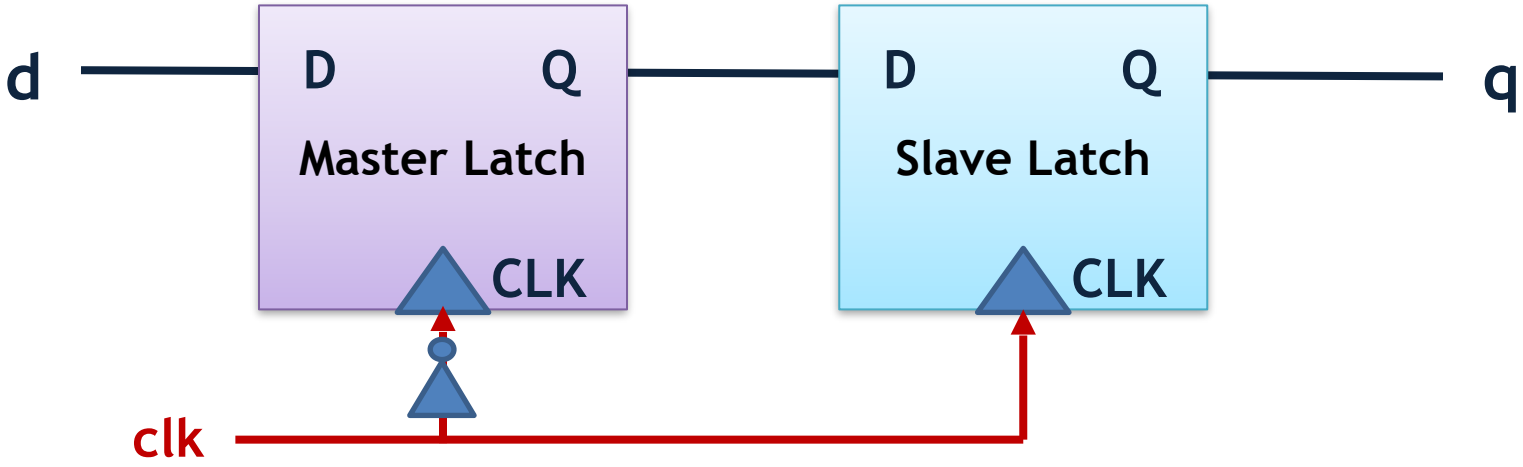


Verilog Basic Question 2

- (Gate Level) 1-bit D Flip-Flop (DFF) with D Latches
- Design a **latch** module as follows:



- Then design a **clk positive** edge trigger **flip-flop** module as:



- We will test your **latch** and **flip-flop** by TA's testbenches

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Advanced Questions

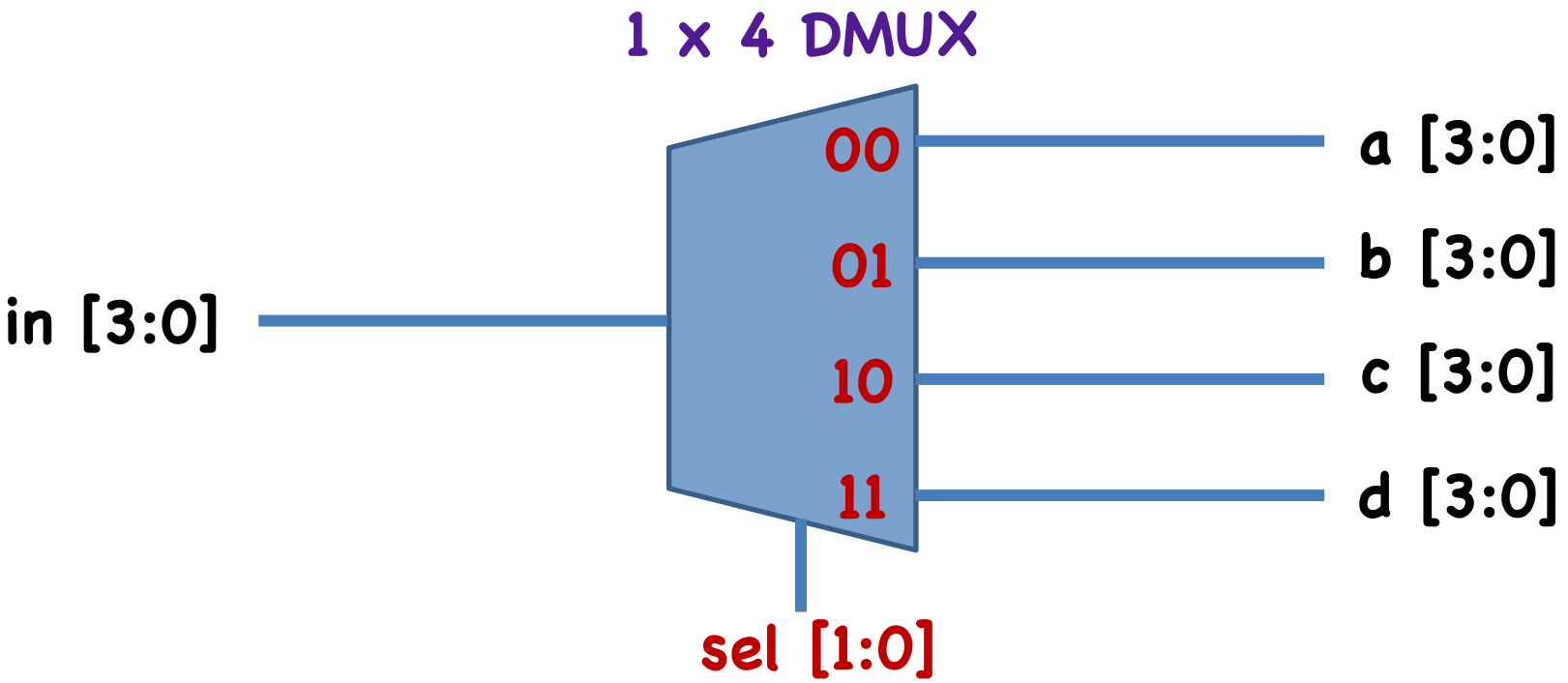
- Individual assignment

- Verilog questions (due on 9/28/2023. 23:59:59.)
  - Optional: (Gate-level) 4-bit 1-to-4 de-multiplexer (DMUX)
  - Necessary: (Gate-level) 4-bit simple crossbar switch with MUX/DMUX
  - Necessary: (Gate-level) 4-bit 4x4crossbar with simple crossbar switch
  - Optional:(Gate-level) 1-bit toggle flip flop (TFF)

- FPGA demonstration (due on 10/5/2023. In class.)
  - Necessary: (Gate-level) 4-bit simple crossbar switch with MUX/DMUX

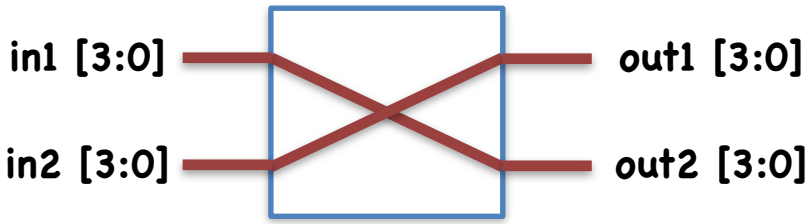
Verilog Advanced Question 1

- (Gate-level) 4-bit 1-to-4 de-multiplexer (DMUX)
- The value of the selected output is set to **in**, while the others' are set to **0**.
- Construct your 1-to-4 DMUX with three 1-to-2 DMUXes

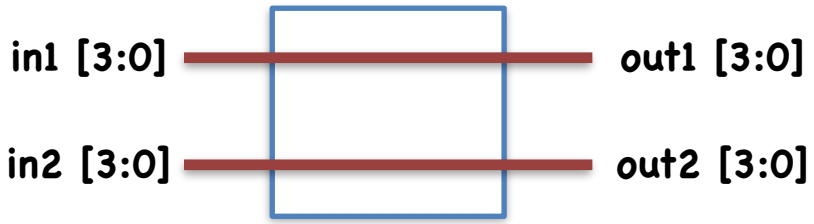


Verilog Advanced Question 2

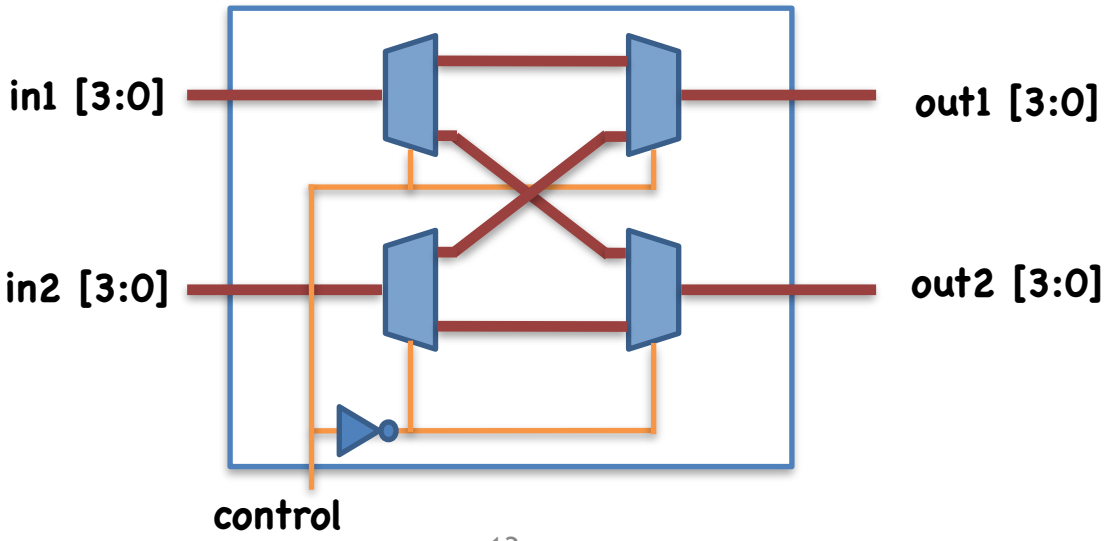
- (Gate-level) 4-bit simple crossbar switch with MUX/DMUX
- **Reuse** your 2-to-1 MUX and 1-to-2 DMUX modules



- **control** = 1'b1

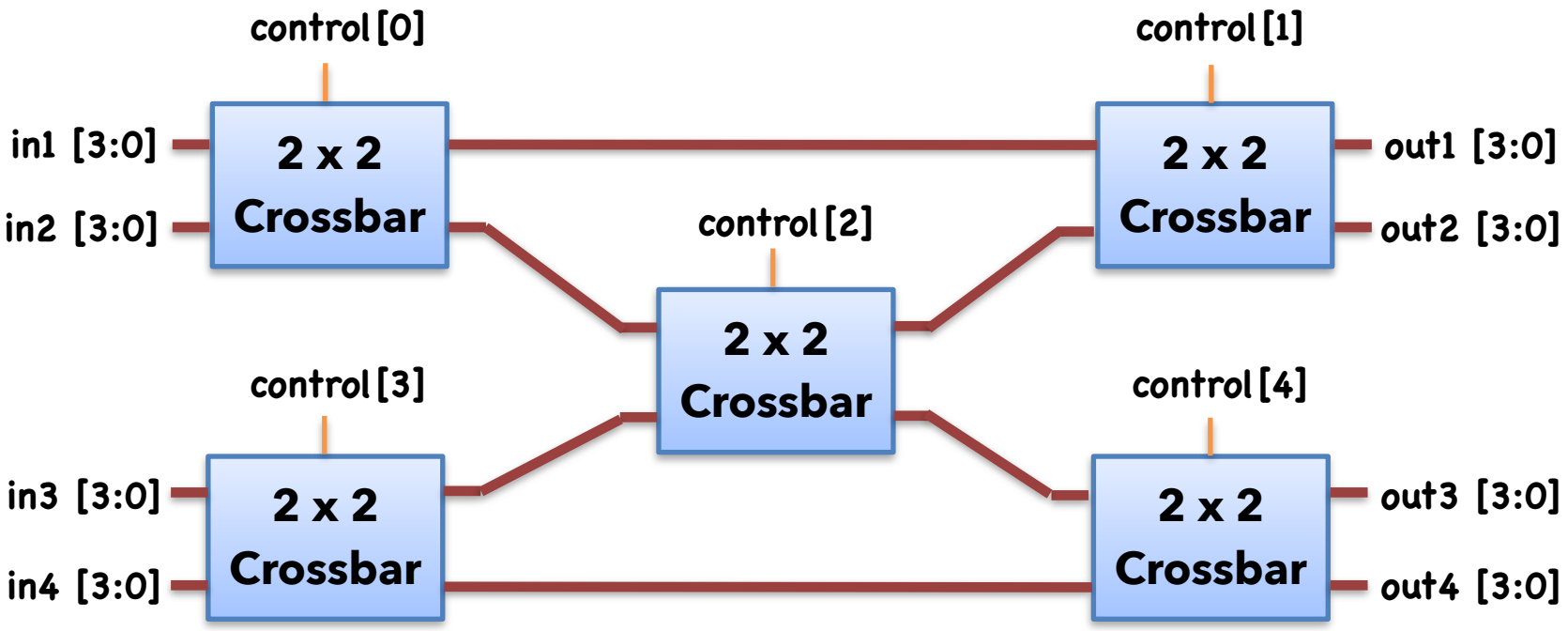


- **control** = 1'b0



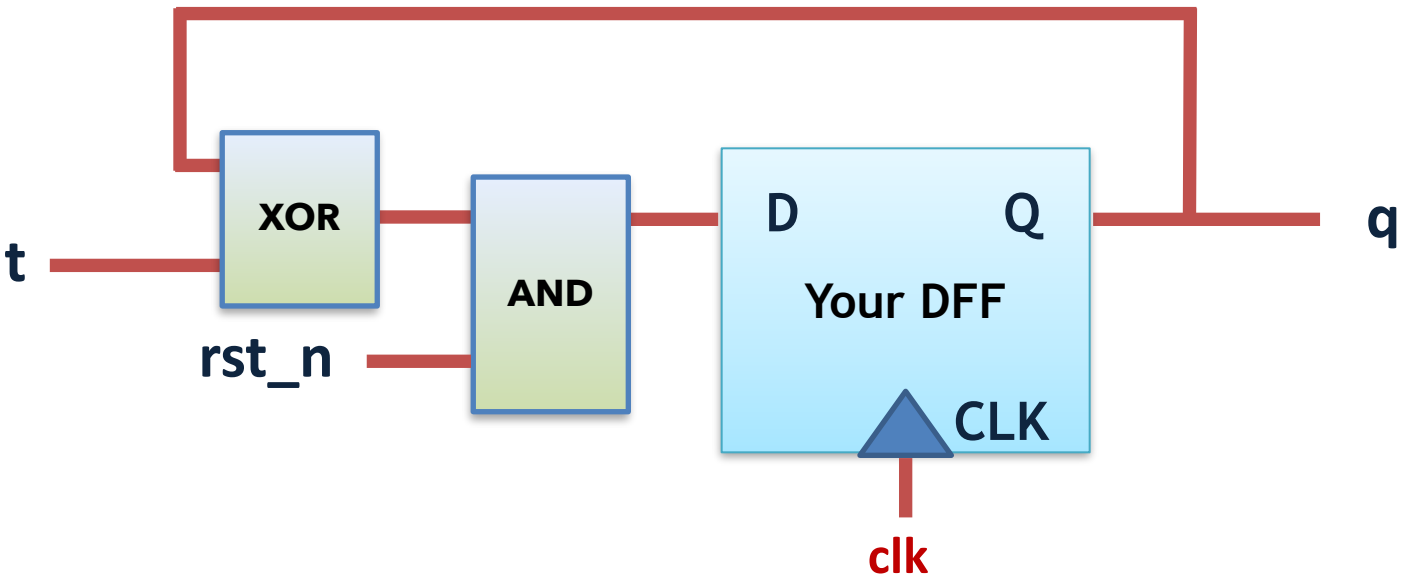
Verilog Advanced Question 3

- (Gate-level) 4-bit 4x4crossbar with simple crossbar switch
- Please reuse your module in the previous question
- Some combinations of input and output pairs cannot be achieved by such a crossbar (e.g., [(in1, out3), (in2, out4), (in3, out1), (in4, out2)]). Please list all of them in your report.



Verilog Advanced Question 4

- (Gate-level) 1-bit toggle flip flop (TFF)
- Please reuse your design of DFF, and avoid using XOR directly



Advanced Questions

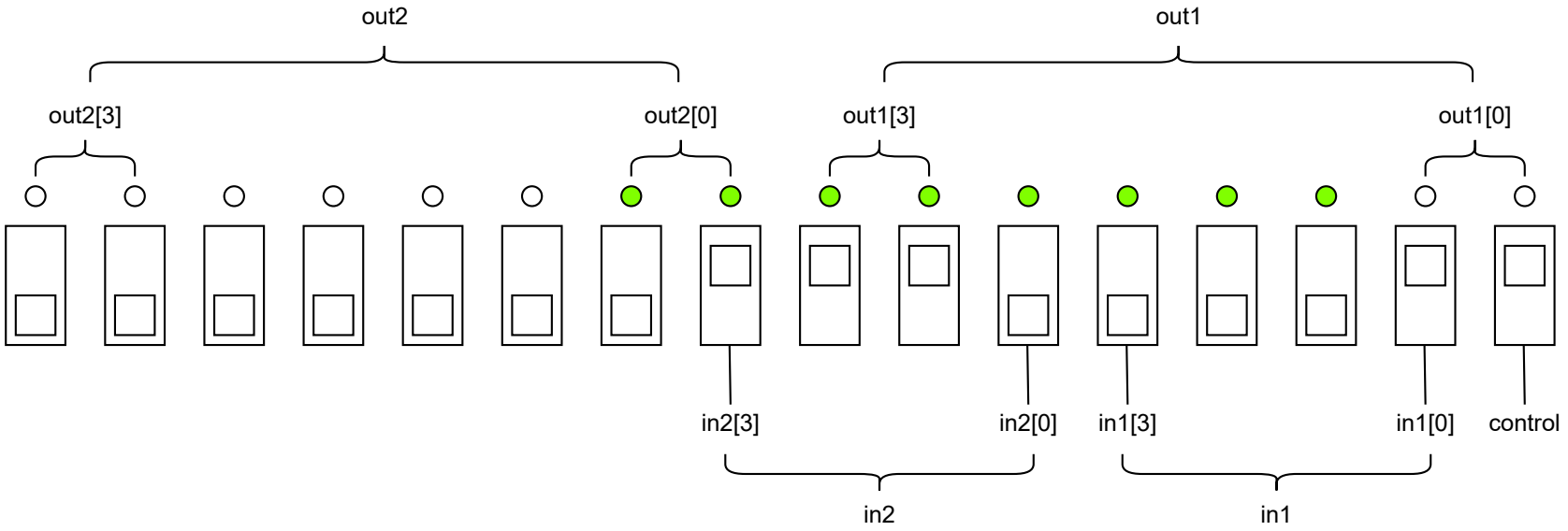
- Individual assignment

- Verilog questions (due on 9/28/2023. 23:59:59.)
  - Optional: (Gate-level) 4-bit 1-to-4 de-multiplexer (DMUX)
  - Necessary: (Gate-level) 4-bit simple crossbar switch with MUX/DMUX
  - Necessary: (Gate-level) 4-bit 4x4crossbar with simple crossbar switch
  - Optional:(Gate-level) 1-bit toggle flip flop (TFF)

- FPGA demonstration (due on 10/5/2023. In class.)
  - Necessary: (Gate-level) 4-bit simple crossbar switch with MUX/DMUX

FPGA Demonstration 1

- (Gate-level) 4-bit simple crossbar switch with MUX/DMUX
  - Please implement your gate-level 4-bit simple crossbar switch with MUX/DMUX on your FPGA board
  - Please use SWITCHes as your inputs, and LEDs as your outputs
  - Please assign your inputs/outputs as:
    - in2, in1, control: The rightmost nine SWITCHes , respectively
    - out2, out1: 16 LEDs (note that each output corresponds to TWO LEDs)
    - The detailed FPGA configuration is illustrated below.



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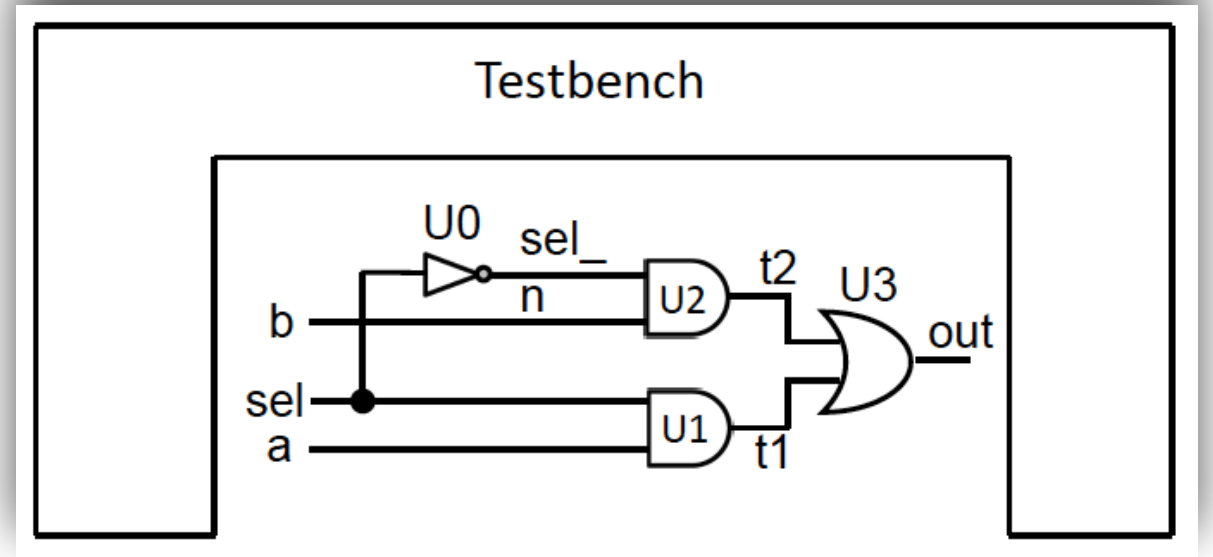
Verilog Simulation Framework

- Testbench verifies whether a module is correct or not
- Similar to the main function in C++
- Generate stimulus and check the outputs

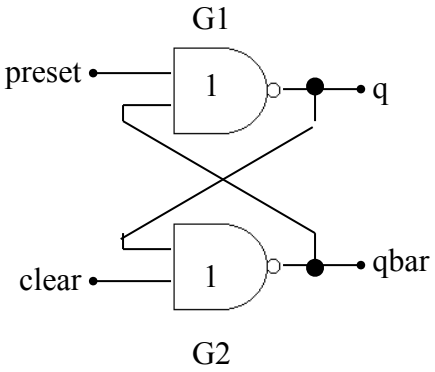


Verilog Testbench

Design

```
module   Nand_Latch_1 (q, qbar, preset, clear);
   output      q, qbar;
   input       preset, clear;

   nand #1     G1 (q, preset, qbar),
               G2 (qbar, clear, q);
endmodule
```



Testbench

```
`timescale 1ns / 1ps
module      test_Nand_Latch_1;
 reg        preset, clear;
 wire       q, qbar;

 Nand_Latch_1 M1 (q, qbar, preset, clear);

 always begin
    #20     clear = !clear;
 end

 initial
   begin
              preset = 1'b0;   clear = 1'b1;
    #10
              preset = 1'b1;
 end

endmodule
```

// Simulation Unit / Accuracy
// Testbench module
// Inputs should be declared as reg
// Outputs should be declared as wire

// Instantiate YOUR DESIGN module

// always condition: The description always happens
// The value of clear inverts every 20 ns

// Initial conditions

// Units of "Simulation Units". In this case, 10ns


Thank you for your attention!
*Seattle night view taken at LA County Museum of Arts, Los Angeles, CA.
This picture is taken by Chun-Yi Lee himself, who is also a fan of photography