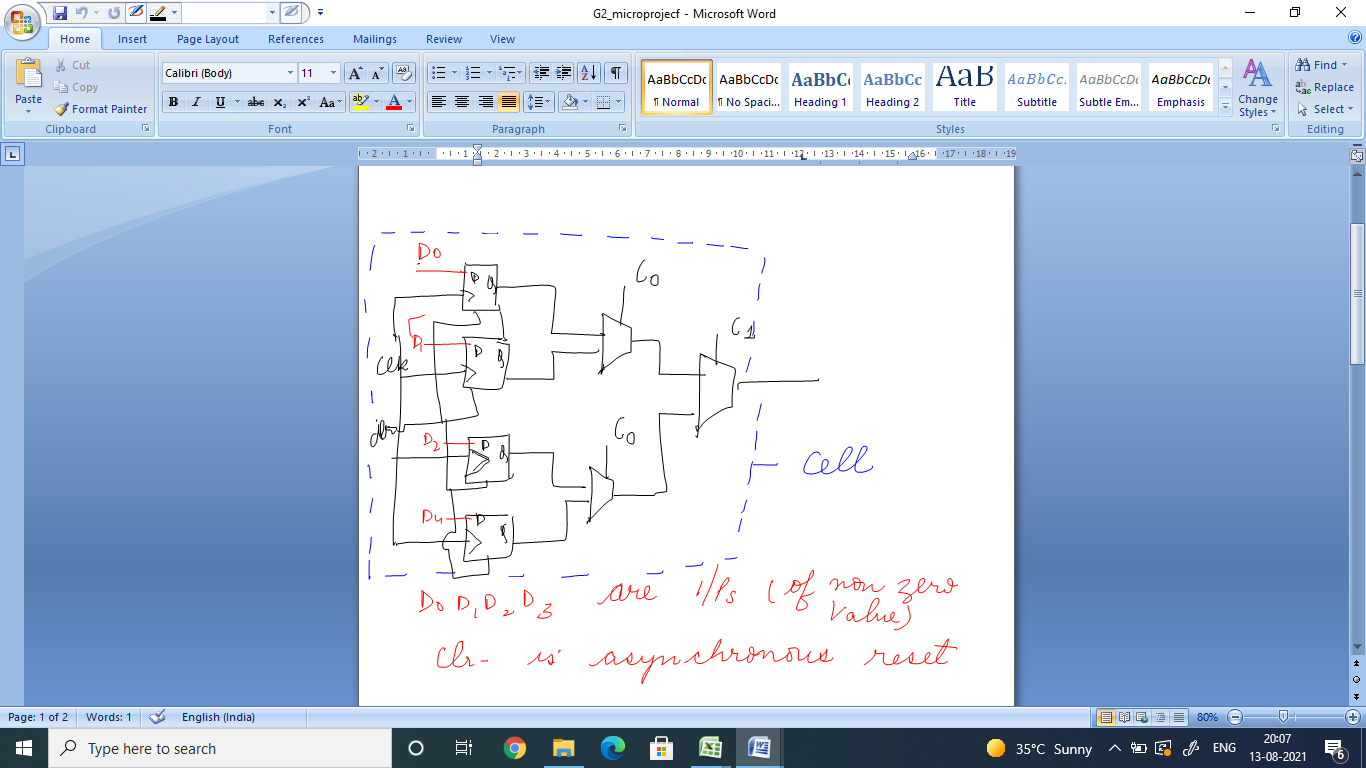
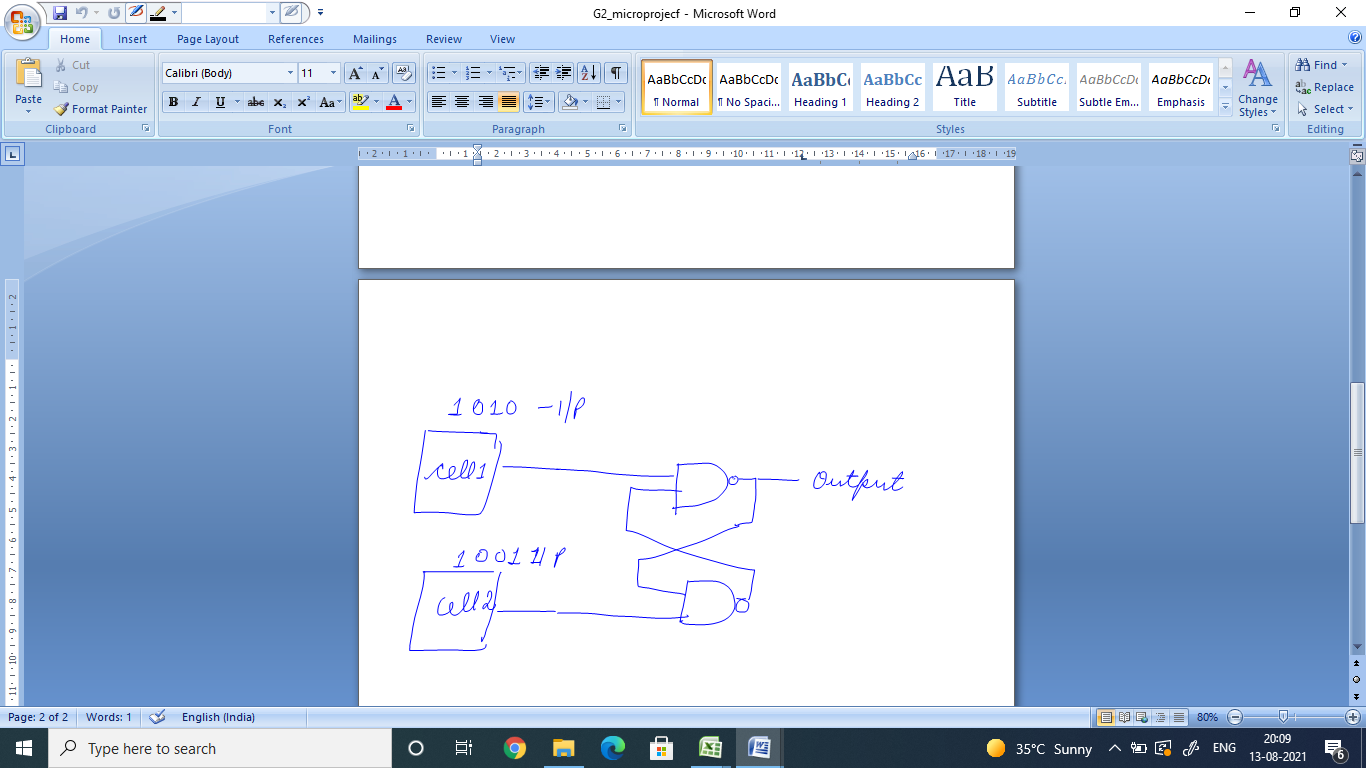
**Implement using VHDL/Verilog and Simulate to verify the results:**

LFSRs:

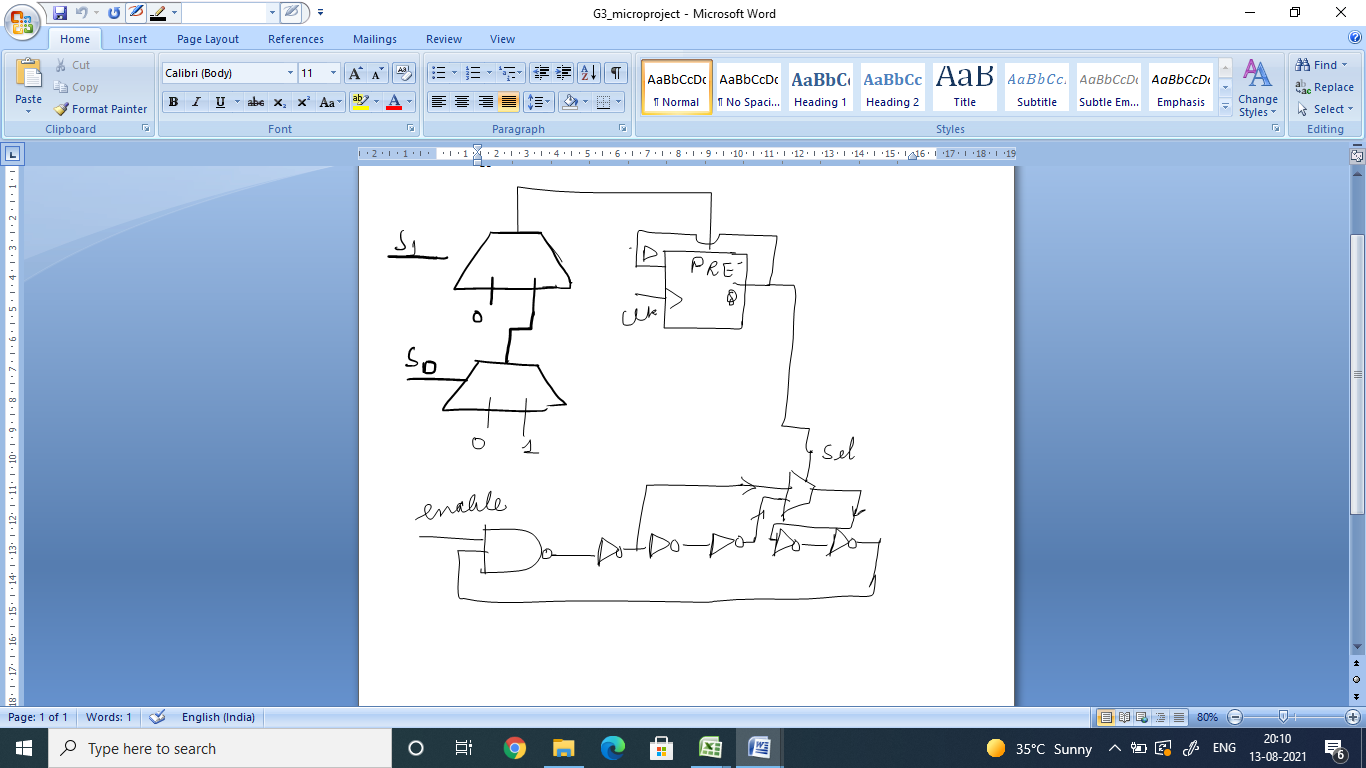
**Group 1-**

GROUP 2:

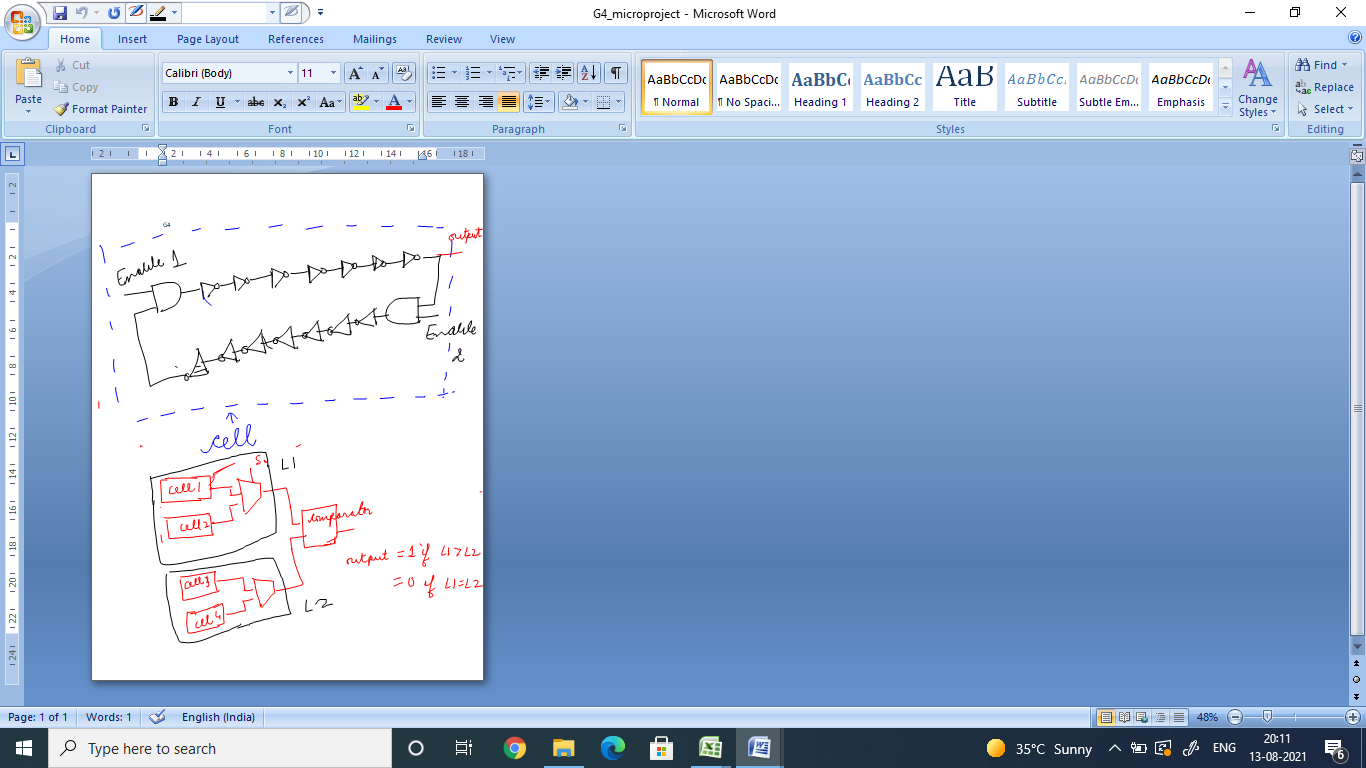




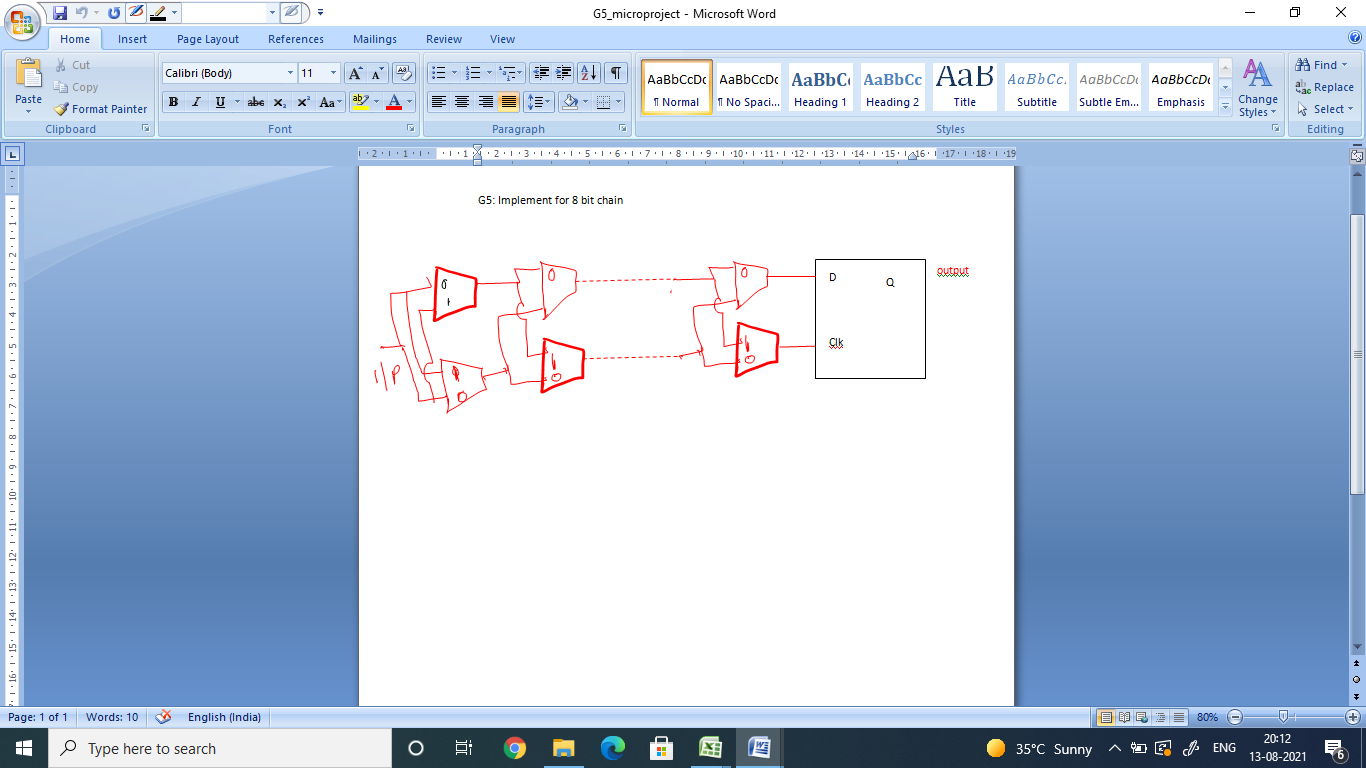
GROUP 3



Group 4



Group 5



Group 6

