**Experiment 3**

**Part 1:**

**Aim:**

Write the code to design a D Flip Flop and write test bench in System Verilog.

**Code:**

**DUT:**

module dff (

    input clk,

    input  d,

    output reg q

);

    always@(posedge clk)

        begin

            q<=d;

        end

endmodule

**TB:**

module tb;

  bit d,clk,q;

  dff uut(clk,d,q);

  initial forever #5 clk=~clk;

  initial begin

    repeat (10) begin

      @(negedge clk) d = $random;

      #5;

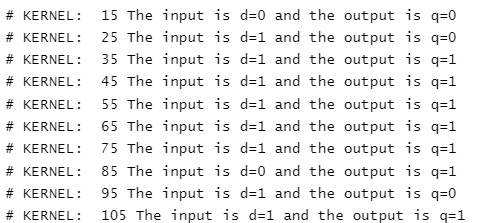
      $display(" %0d The input is d=%b and the output is q=%b ",$time,d,q);

    end

  end

endmodule

**Output**

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**Part 2:**

**Aim:**

Write the code to design a 4 bit adder and write its test bench is System Verilog

**Code:**

**DUT:**

module bitadder(input [3:0]a,b,

                 input cin,

                 output [3:0]sum,

                 output cout);

  assign {cout,sum} = a+b+cin;

endmodule

**TB:**

module tb();

  reg [3:0] a,b;

  wire [3:0] sum;

  reg cin;

  wire cout;

  bitadder uut(a,b,cin,sum,cout);

  initial begin

    repeat(10) begin

      {a,b,cin}=$random;

      #5;

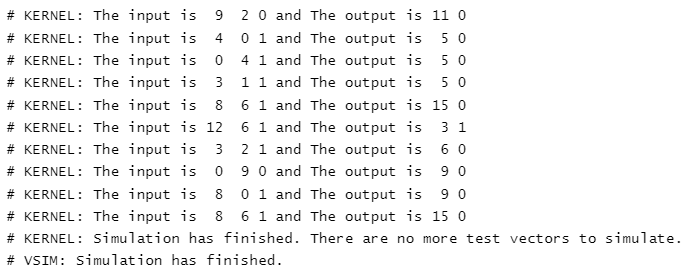
      $display("The input is %d %d %d and The output is %d %d",a,b,cin,sum,cout);

    end

  end

endmodule

**Output:**

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**Result:**

The given problem statement is executed and verified to be correct.