**Experiment 5**

**Aim:**

Familiarization with System Verilog task, function and void function.

1. Write the SV “task” code for the addition of two integer numbers and check it correctness.
2. Observe the difference between simple and automatic tasks:
3. Write a simple task which increments the value of a local variable by a specified amount.
4. Write an automatic task which increments the value of a local variable by a specified amount.

Hint: You can write a simple task which increments the value of a local variable by a specified amount.

1. Demonstrate the difference between static and automatic variables used in SV task. ◊Write the following SV code and simulate it. Study the output and comment on it.
2. Write the code using SV “function” for the addition of two integer numbers.
3. Write the SV void function to print the current simulation time. Check its corrections.

**Code:**

module experiment();

  integer a, b, y;

task add1(input int a, b, output int y);

    y=a+b;

    $display("The input %0d and %0d, output is %0d",a,b,y);

  endtask

  initial begin

    $display("\*\*\*\*\*\*\*\*\*\*\*\*\*ADDITION USING TASK\*\*\*\*\*\*\*\*\*\*\*\*\*\*");

    repeat(3) begin

       a=$random;

       b=$random;

      add1(a,b,y);

    end

  end

  task static increment(input integer value);

    integer i=1;

    i=i+value;

    $display("incremented value is %d",i);

  endtask

  initial begin

    $display("\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*STATIC TASK\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* ");

    increment(3);

    increment(3);

  end

  task automatic increment1(integer value1); begin

    integer j=1;

    j=j+value1;

    $display("incremented value is %d",j);

  end

  endtask

  initial begin

    $display("\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*AUTOMATIC TASK\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*");

    increment1(2);

    increment1(2);

  end

  function integer addition(input integer ia,

    input integer ib,

    output integer iy);

    begin

      iy = ia + ib;

      $display("addition of %0d and %0d is %d",ia,ib,iy);

    end

  endfunction

  initial begin

    a=3;

    b=2;

    addition(a,b,y);

  end

  function void addition1;

    input integer ai;

    input integer bi;

    output integer yi;

    begin

      yi=ai+bi;

      $display("addition of %0d and %0d is %d",ai,bi,yi);

    end

  endfunction

  initial begin

    a=5;

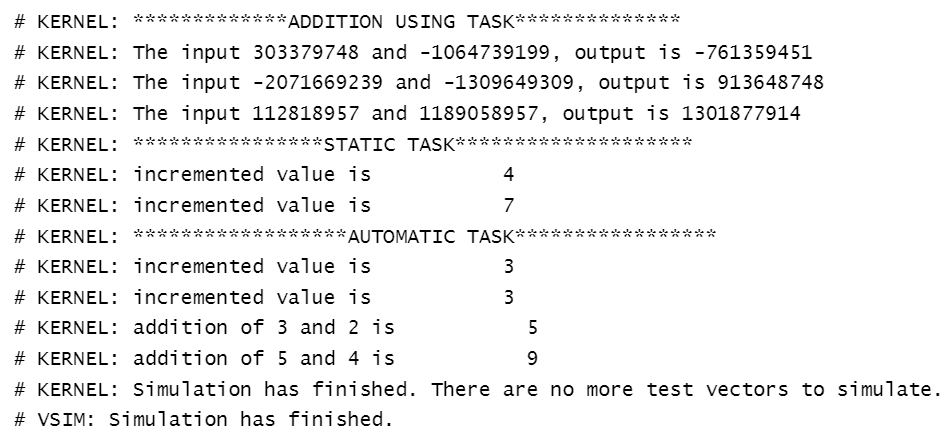
    b=4;

    addition1(a,b,y);

  end

endmodule

**Output:**

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**Aim: Demonstrate the difference between static and automatic variables used in SV task.**

**Code:**

module auto\_variable\_task;

task auto\_delay(input time delay);

logic static\_var = 1'b0;

automatic logic auto\_var = 1'b0;

$display("@time : %0d - static variable is %b, auto variable is %b",$time,static\_var, auto\_var);

#delay;

static\_var = !static\_var;

auto\_var = !auto\_var;

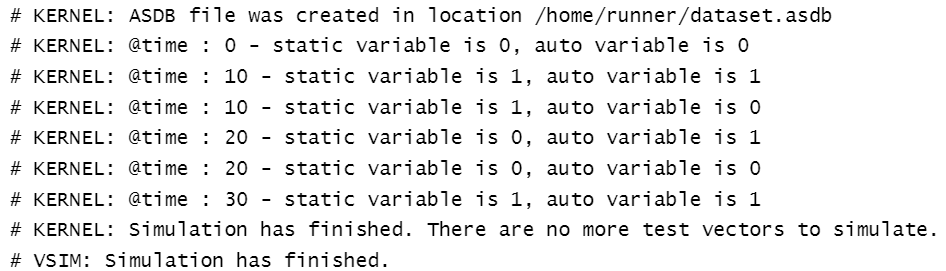
$display("@time : %0d - static variable is %b, auto variable is %b",$time,static\_var, auto\_var);

endtask : auto\_delay

initial repeat(3) auto\_delay(10ns);

endmodule

**Output:**

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**Result:**

The given problem statement is executed and verified to be correct.