

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING



THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

Embedded System

Experiment-9

Submitted by

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M.Tech (VLSI Design)

Experiment 9

Aim:

To write an ARM Assembly Language program for arranging the number in to ascending and descending order.

Tool Used:

Keil uVision4

Theory:

LDR loads the register with some value. One register can be used as a counter. STRCSB is used to store byte if carry is set. STRCCB is used to store byte if carry is clear. CMP is used to compare the values in two registers.

Code(ascending):

```
AREA PROGRAM, CODE, READONLY
ENTRY
MAIN
    MOV R0, #9
LOOP1    LDR R1, =0X00001000
        ADD R2, R1, #1
        MOV R3, R0
LOOP2    LDRB R4, [R1]
        LDRB R5, [R2]
        CMP R4, R5
        STRCSB R4, [R2]
        STRCSB R5, [R1]
        ADD R1, R1, #1
        ADD R2, R2, #1
        SUBS R3, R3, #1
        BNE LOOP2
        SUBS R0, R0, #1
        BNE LOOP1
    END
```

Input:

[illegible]

Output:

Memory 1															
Address:		0x00001000													
0x00001000:	00	00	15	20	21	34	43	45	54	76	00				
0x00001015:	00	00	00	00	00	00	00	00	00	00	00				
0x0000102A:	00	00	00	00	00	00	00	00	00	00	00				
0x0000103F:	00	00	00	00	00	00	00	00	00	00	00				

Register Content

Registers	
Register	Value
Current	
R0	0x00000000
R1	0x00001001
R2	0x00001002
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000003C
CPSR	0x600000D3

Code(descending):

```
AREA PROGRAM, CODE, READONLY
ENTRY
MAIN
    MOV R0, #9
LOOP1    LDR R1, =0X00001000
         ADD R2, R1, #1
         MOV R3, R0

LOOP2    LDRB R4, [R1]
         LDRB R5, [R2]
         CMP R4, R5
         STRCCB R4, [R2]
         STRCCB R5, [R1]
         ADD R1, R1, #1
         ADD R2, R2, #1
         SUBS R3, R3, #1
         BNE LOOP2
```

```

SUBS R0, R0, #1
BNE LOOP1
END

```

Input:

Memory 1												
Address: 0x00001000												
0x00001000:	23	74	78	25	54	45	87	98	19	00		
0x00001015:	00	00	00	00	00	00	00	00	00	00		
0x0000102A:	00	00	00	00	00	00	00	00	00	00		

Output:

Memory 1												
Address: 0x00001000												
0x00001000:	98	87	78	74	54	45	25	23	19	00	00	00
0x00001015:	00	00	00	00	00	00	00	00	00	00	00	00
0x0000102A:	00	00	00	00	00	00	00	00	00	00	00	00

Register Content:

Registers	
Register	Value
Current	
R0	0x00000000
R1	0x00001001
R2	0x00001002
R3	0x00000000
R4	0x00000098
R5	0x00000087
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000003C
CPSR	0x600000D3

Result:

The experiments on arranging the number in to ascending and descending order have been performed and verified to be correct.