

uops.info: Characterizing Latency, Throughput, and Port Usage of Instructions on Intel Microarchitectures

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Abstract

Modern microarchitectures are some of the world's most complex man-made systems. As a consequence, it is increasingly difficult to predict, explain, let alone optimize the performance of software running on such microarchitectures. As a basis for performance predictions and optimizations, we would need faithful models of their behavior, which are, unfortunately, seldom available.

In this paper, we present the design and implementation of a tool to construct faithful models of the latency, throughput, and port usage of x86 instructions. To this end, we first discuss common notions of instruction throughput and port usage, and introduce a more precise definition of latency that, in contrast to previous definitions, considers dependencies between different pairs of input and output operands. We then develop novel algorithms to infer the latency, throughput, and port usage based on automatically-generated microbenchmarks that are more accurate and precise than existing work.

To facilitate the rapid construction of optimizing compilers and tools for performance prediction, the output of our tool is provided in a machine-readable format. We provide experimental results for processors of all generations of Intel's Core architecture, i.e., from Nehalem to Coffee Lake, and discuss various cases where the output of our tool differs considerably from prior work.

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1 Introduction

Developing tools that predict, explain, or even optimize the performance of software is challenging due to the complexity of today's microarchitectures. Unfortunately, this challenge is exacerbated by the lack of a precise documentation of their behavior. While the high-level structure of modern microarchitectures is well-known and stable across multiple generations, lower-level aspects may differ considerably between microarchitecture generations and are generally not as well documented. An important aspect with a relatively strong influence on performance is how ISA instructions decompose into micro-operations (μ ops); which ports these μ ops may be executed on; and what their latencies are.

Knowledge of this aspect is required, for instance, to build precise performance-analysis tools like CQA [8], Kerncraft [18], or llvm-mca [6]. It is also useful when configuring cycle-accurate simulators like Zesto [27], gem5 [7], McSim+ [3] or ZSim [31]. Optimizing compilers, such as LLVM [26] and GCC [15], can profit from detailed instruction characterizations to generate efficient code for a specific microarchitecture. Similarly, such knowledge is helpful when manually fine-tuning a piece of code for a specific processor.

Unfortunately, information about the port usage, latency, and throughput of individual instructions at the required level of detail is hard to come by. Intel's processor manuals [23] only contain latency and throughput data for a number of "commonly-used instructions." They do not contain information on the decomposition of individual instructions into μ ops, nor do they state the execution ports that these μ ops can use.

The only way to obtain accurate instruction characterizations for many recent microarchitectures is thus to perform measurements using microbenchmarks. Such measurements are aided by the availability of performance counters that provide precise information on the number of elapsed cycles and the cumulative port usage of instruction sequences. A relatively large body of work [1, 2, 4, 9, 10, 19, 28–30, 32, 33, 35, 36] uses microbenchmarks to infer properties of the memory hierarchy. Another line of work [5, 13, 14, 25] uses automatically generated microbenchmarks to characterize the energy

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consumption of microprocessors. Comparably little work [8, 12, 17, 34] is targeted at instruction characterizations. Furthermore, existing approaches, such as [12], require significant manual effort to create the microbenchmarks and to interpret the results of the experiments. Furthermore, its results are not always accurate and precise, as we will show later.

In this paper, we develop a new approach that can automatically generate microbenchmarks in order to characterize the latency, throughput, and port usage of instructions on Intel Core CPUs in an accurate and precise manner.

Before describing our algorithms and their implementation, we first discuss common notions of instruction latency, throughput, and port usage. For latency, we propose a new definition that, in contrast to previous definitions, considers dependencies between different pairs of input and output operands, which enables more accurate performance predictions.

We then develop algorithms that generate assembler code for microbenchmarks to measure the properties of interest for most x86 instructions. Our algorithms take into account explicit and implicit dependencies, such as, e.g., dependencies on status flags. Therefore, they require detailed information on the x86 instruction set. We create a machine-readable XML representation of the x86 instruction set that contains all the information needed for automatically generating assembler code for each instruction. The relevant information is automatically extracted from the configuration files of Intel's *x86 Encoder Decoder (XED)* [21] library.

We have implemented our algorithms in a tool that we have successfully applied to all microarchitecture generations of Intel's Core architecture, i.e., from Nehalem to Coffee Lake. In addition to running the generated microbenchmarks on the actual hardware, we have also implemented a variant of our tool that runs them on top of Intel IACA [20]. IACA is a closed-source tool published by Intel that can statically analyze the performance of loop kernels on different Intel microarchitectures. It is, however, updated only infrequently, and its results are not always accurate, as we will show later.

The output of our tool is available in a machine-readable format, so that it can be easily used to implement, e.g., simulators, performance prediction tools, or optimizing compilers.

Finally, we discuss several interesting insights obtained by comparing the results from our measurements with previously published data. Our precise latency data, for example, uncovered previously undocumented differences between different microarchitectures. It also explains discrepancies between previously published information. Apart from that, we uncovered various errors in IACA, and inaccuracies in the manuals.

2 Related Work

In this section, we will describe existing sources of detailed instruction data for Intel microarchitectures. We will first

consider information provided by Intel directly, and then look at measurement-based approaches.

2.1 Information provided by Intel

Intel's *Optimization Reference Manual* [23] contains a set of tables with latency and throughput data for "commonly-used instructions." The tables are not complete; for some instructions, only throughput information is provided. The manual does not contain detailed information about the port usage of individual instructions.

IACA [20] is a closed-source tool developed by Intel that can statically analyze the performance of loop kernels on several microarchitectures (which can be different from the system that the tool is run on). The tool generates a report which includes throughput and port usage data of the analyzed loop kernel. By considering loop kernels with only one instruction, it is possible to obtain the throughput of the corresponding instruction. However, it is, in general, not possible to determine the port bindings of the individual μ ops this way. Early versions of IACA were also able to analyze the latency of loop kernels; however, support for this was dropped in version 2.2. IACA is updated only infrequently. Support for the Broadwell microarchitecture (which was released in 2014), for example, was added only in 2017. There is currently no support for the two most recent microarchitectures, Kaby Lake and Coffee Lake, which were released in 2016 and 2017, respectively.

The instruction scheduling components of LLVM [26] for the Sandy Bridge, Haswell, Broadwell, and Skylake microarchitecture were recently updated and extended with latency and port usage information that was, according to the commit message (<https://reviews.llvm.org/rL307529>), provided by the architects of these microarchitectures. The resulting models are available in the LLVM repository.

2.2 Measurement-based Approaches

Agner Fog [12] provides lists of instruction latency, throughput, and port usage data for different x86 microarchitectures. The data in the lists is not complete; e.g., latency data for instructions with memory operands is often missing. The port usage information is sometimes inaccurate or imprecise; reasons for this are discussed in Section 5.1. The data is obtained using a set of test scripts developed by the author. The output from these scripts has to be interpreted manually to build the instruction tables.

CQA [8] is a performance analysis tool for x86 code that requires latency, throughput, and port usage data to build a performance model of a microarchitecture. It includes a microbenchmark module that supports measuring the latency and throughput of many x86 instructions. For non-supported instructions, the authors use Agner Fog's instruction tables [12]. The paper briefly mentions that the module can also measure the number of μ ops that are dispatched to

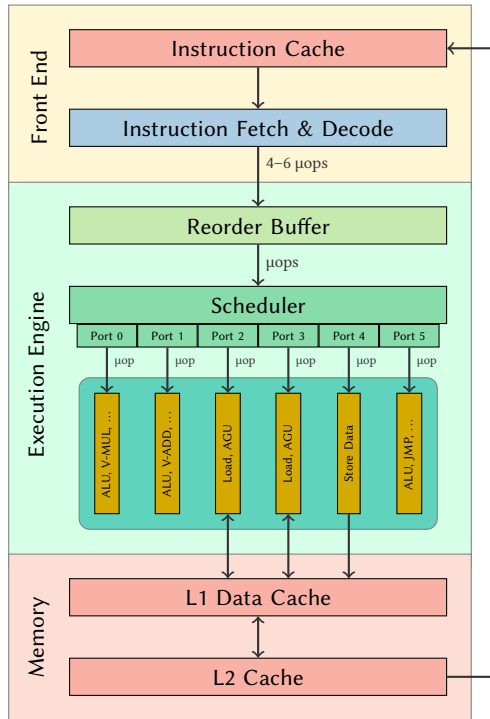


Figure 1. Pipeline of Intel Core CPUs (simplified).

execution ports using performance counters, but no further details are provided.

EXEgesis [16] is a project that can create a machine-readable list of instructions by parsing the PDF representation of Intel’s Software Developer’s Manual [24]. One of the goals of the project is also to infer latencies and μop scheduling information for different instruction/microarchitecture pairs.

Granlund [17] presents measured latency and throughput data for different x86 processors. He considers only a relatively small subset of the x86 instruction set.

AIDA64 [11] is a commercial, closed-source system information tool that can perform throughput and latency measurements of x86 instructions. Measurement results for many processors obtained using AIDA64 are available at [34].

3 Background

3.1 Pipeline of Intel Core CPUs

Figure 1 shows the general structure of the pipeline of Intel Core CPUs. The pipeline consists of the front end, the execution engine (back end), and the memory subsystem.

The front end is responsible for fetching instructions from the memory, and for decoding them into a sequence of micro-operations (μops).

The *reorder buffer* stores the μops *in order* until they are retired. It is also responsible for register allocation (i.e., mapping the architectural registers to physical registers), and register renaming (to eliminate false dependencies among μops).

On some microarchitectures, the reorder buffer can also directly execute certain special μops , including NOPs, zero idioms (e.g., an XOR of a register with itself), and register-to-register moves (“*move elimination*”).

The remaining μops are then forwarded to the *scheduler* (also known as the *reservation station*), which queues the μops until all their source operands are ready. Once the operands of a μop are ready, it is dispatched through an execution port. Due to *out-of-order* execution, μops are not necessarily dispatched in program order. Each port (Intel Core microarchitectures have 6 or 8 of them) is connected to a set of different functional units, such as an ALU, an address-generation unit (AGU), or a unit for vector multiplications. Each port can accept at most one μop in every cycle. However, as most functional units are fully pipelined, a port can typically accept a new μop in every cycle, even though the corresponding functional unit might not have finished executing a previous μop . An exception to this are the divider units, which are not fully pipelined.

3.2 Assembler Instructions

Throughout this paper, we will use assembler instructions in Intel syntax. They have the following form:

mnemonic op₁, op₂, ...

The mnemonic identifies the operation, e.g., ADD or XOR. The first operand op₁ is typically the destination operand, and the other operands are the source operands (an operand can also be both a source and destination operand). Operands can be registers, memory locations, or immediates. Memory operands use the syntax $[R_{base} + R_{index} * scale + disp]$, where R_{base} and R_{index} are general-purpose registers, $disp$ is an integer, and $scale$ is 1, 2, 4, or 8. All of these components are optional and can be omitted. In addition to these explicit operands, an instruction can also have implicit operands.

As an example, consider the following instruction:

ADD RAX, [RBX]

This instruction computes the sum of the general-purpose register RAX and the memory at the address of register RBX, and stores the result in RAX. We refer to RAX and [RBX] as *explicit* operands. In addition to that, the instruction updates the status flags (e.g., the carry flag) according to the result. The status flags are *implicit* operands of the ADD instruction.

There are often multiple variants of an instruction with different operand types and/or widths.

Note that there is not always a one-to-one correspondence between assembler code and machine code. Sometimes, there are multiple possible encodings for the same assembler instruction. It is, in general, not possible to control which of these encodings the assembler selects. Thus, some machine instructions cannot be generated using assembler code.

3.3 Hardware Performance Counters

Hardware performance counters are special registers that store the count of various hardware-related events. All recent Intel processors have counters for the number of elapsed core cycles, and for the number of μ ops that are executed on each port.

4 Definitions

In this section, we define the microarchitectural properties we want to infer, i.e., latency, throughput, and port usage.

4.1 Latency

The latency of an instruction is commonly [23] defined as the “number of clock cycles that are required for the execution core to complete the execution of all of the μ ops that form an instruction” (assuming that there are no other instructions that compete for execution resources). Thus, it denotes the time from when the operands of the instruction are ready and the instruction can begin execution to when the results of the instruction are ready.

This definition ignores the fact that different operands of an instruction may be read and/or written by different μ ops. Thus, a μ op of an instruction I might already begin execution before all source operands of I are ready, and a subsequent instruction I' that depends on some (but not all) results of I might begin execution before all results of I have been produced. To take this into account, we propose the following definition for latency instead. Let $S = \{s_1, \dots, s_m\}$ be the source operands, and $D = \{d_1, \dots, d_m\}$ be the destination operands of an instruction. We define the latency of the instruction to be the mapping $lat : S \times D \rightarrow \mathbb{N}$ such that $lat(s_i, d_j)$ denotes the time from when source operand s_i becomes ready until the result d_j is ready (assuming all other dependencies are not on the critical path). Thus, if t_{s_i} denotes the time at which source operand s_i becomes ready, then destination operand d_j is ready at time

$$t_{d_j} = \max\{t_{s_i} + lat(s_i, d_j) \mid s_i \in S\}.$$

With the usual approach of using a single value lat as the latency of an instruction, this value would be

$$t_{d_j} = \max\{t_{s_i} \mid s_i \in S\} + lat,$$

which might be significantly greater than what would be observed in practice.

4.2 Throughput

When comparing throughput data from different publications, it is important to note that these publications do not all use the same definition of throughput. Intel defines throughput in its manuals [22, 23] as follows:

Definition 1 (Throughput - Intel). *The number of clock cycles required to wait before the issue ports are free to accept the same instruction again.*

On the other hand, Agner Fog [12] uses the following definition for (reciprocal) throughput:

Definition 2 (Throughput - Fog). *The average number of core clock cycles per instruction for a series of independent instructions of the same kind in the same thread.*

Granlund [17] uses a similar definition as Fog.

These two definitions are not equivalent, as there can be factors other than contention for the issue ports that may reduce the rate at which instructions can be executed (e.g., the front end, or the memory subsystem). Moreover, it is not always possible to find instructions of the same kind that are truly independent, as many instructions have implicit dependencies on certain registers or flags. Hence, the second definition may yield higher throughput values (corresponding to a lower throughput) than the first definition for the same instruction.

Some publications (e.g., [12, 17]) use the term throughput to denote *instructions per cycle*, while others (e.g., [20, 22, 23]) use it to denote *cycles per instruction*. In this paper, we will use the term with the latter meaning.

4.3 Port Usage

Let P be the set of ports of a CPU, and U the set of μ ops of an instruction $instr$. Let $ports : U \rightarrow 2^P$ be a mapping such that $ports(u)$ is the set of ports which have a functional unit that can execute the μ op u .

We define the port usage $pu : 2^P \rightarrow \mathbb{N}$ of $instr$ to be a mapping such that $pu(pc) = |\{u \in U \mid ports(u) = pc\}|$, i.e., $pu(pc)$ denotes the number of μ ops of $instr$ whose functional units are at the ports in pc (we will call the set pc a *port combination*). Note that, e.g., for a 1- μ op instruction with a μ op u such that $ports(u) = \{0, 1\}$, we have that $pu(\{0, 1\}) = 1$, but $pu(\{0\}) = pu(\{1\}) = 0$.

For, e.g., an instruction with $pu(\{0, 1, 5\}) = 3$, $pu(\{2, 3\}) = 1$, and $pu(pc) = 0$ for all other port combinations pc , we will use the notation $3 * p015 + 1 * p23$ to denote the port usage. In other words, the instruction consists of three μ ops that may each be executed on ports 0, 1, and 5, and one μ op that may be executed on ports 2 and 3.

5 Algorithms

In this section, we describe the algorithms that we developed to infer the port usage, the latency, and the throughput.

5.1 Port Usage

The existing approach by Agner Fog [12] to determine the port usage measures the number of μ ops on each port when executing the instruction repeatedly in isolation. If the result of such a measurement is, e.g., that there is, on average, one μ op on port 0, and one μ op on port 5, the author would conclude that the port usage is $1 * p0 + 1 * p5$.

However, this might be incorrect: A port usage of $2 * p05$ could lead to exactly the same measurement result when the

instruction is run in isolation, but to a very different result when run together with an instruction that can only use port 0 (the PBLENDVB instruction on the Nehalem microarchitecture is an example for such a case).

In another example, if the measurement result is that there are, on average, 0.5 μ ops on each of port 0, 1, 5, and 6, the author would conclude that the port usage is $2 * p0156$, whereas the actual usage might be $1 * p0156 + 1 * p06$ (this is, e.g., the case for the ADC instruction on the Haswell microarchitecture).

In this section, we propose an algorithm that can automatically infer an accurate model of the port usage. Our algorithm is based on the notion of a *blocking instruction*: We define a *blocking instruction* for a set of ports P to be an instruction whose μ ops can use all the ports in P , but no other port that has the same functional unit as a port in P . In the following, we will call the set P a *port combination*. Blocking instructions are interesting because they can be used to determine whether or not an instruction can only be executed on a given set of ports, the set of ports blocked by the blocking instruction.

Before describing our algorithm to infer a model of the port usage we will now first describe how to find a suitable set of blocking instructions.

5.1.1 Finding Blocking Instructions

Let FU be the set of types of functional units that the CPU uses, and let $ports : FU \rightarrow 2^P$ be a mapping from the functional unit types to the set of ports P that are connected to a functional unit of the given type. The set of port combinations for which we need to find blocking instructions is the set $\{ports(fu) \mid fu \in FU\}$.

We assume that for each of these port combinations (except for the ports that are connected to the *store data* and *store address* units), there is a 1- μ op instruction that can use exactly the ports in the combination. This assumption holds on all recent Intel microarchitectures.

Our algorithm first groups all 1- μ op instructions based on the ports they use when run in isolation. We exclude system instructions, serializing instructions, zero-latency instructions, the PAUSE instruction, and instructions that can change the control flow based on the value of a register. From the remaining instructions, the algorithm chooses from each group an instruction with the highest throughput (see Section 5.3) as the blocking instruction for the port combination corresponding to this group.

As blocking instructions for the port combinations for the ports that are connected to the *store data* and *store address* units, we use the MOV instruction (from a general-purpose register to the memory). This instruction is a 2- μ op instruction; one of its μ ops uses the *store data* unit, and the other a *store address* unit.

To avoid SSE-AVX transition penalties when characterizing SSE or AVX instructions, our algorithm determines two

separate sets of blocking instructions for these two types of instructions. For SSE instructions, the blocking instructions should not contain AVX instructions, and vice versa.

5.1.2 Port Usage Algorithm

Algorithm 1: Port Usage

```

1  $portCombinationsList \leftarrow \text{sort}(portCombinations)$ 
2  $\mu opsForCombination \leftarrow []$  //list of pairs
3 foreach  $pc$  in  $portCombinationsList$  do
4    $blockRep \leftarrow 8 \cdot \text{maxLatency}(instr)$ 
5    $code \leftarrow \text{copy}(\text{blockingInstr}(pc), blockRep); instr$ 
6    $\mu ops \leftarrow \text{measureUopsOnPorts}(code, pc)$ 
7    $\mu ops \leftarrow \mu ops - blockRep$ 
8   foreach  $(pc', \mu ops')$  in  $\mu opsForCombination$  do
9     if  $pc' \subset pc$  then
10        $\mu ops \leftarrow \mu ops - \mu ops'$ 
11   if  $\mu ops > 0$  then
12      $\mu opsForCombination.add((pc, \mu ops))$ 
13 return  $\mu opsForCombination$ 

```

We use Algorithm 1 to infer the port usage of an instruction $instr$.

The algorithm first sorts the set of port combinations by the size of its elements. This ensures that, when iterating over the port combinations, combinations that are a subset of another port combination are processed first.

For each port combination pc , the algorithm determines the number of μops that may use all of the ports in pc but no others. To determine this set, the algorithm concatenates $blockRep$ copies of the corresponding blocking instruction with the instruction that we want to analyze (line 5). $blockRep$ is the product of the maximum latency of the instruction (see Section 5.2), i.e., the maximum over the latencies for all input/output pairs, and the maximum number of ports. This ensures that there is always a sufficient number of instructions available that can block the ports of the combination. The operands of the copies of the blocking instructions are chosen such that they are independent from the operands of $instr$, and independent from subsequent instances of the blocking instruction.

Executing the concatenation, instruction $instr$ will only be executed on one of the blocked ports if there is no other port that it can be executed on. The algorithm thus measures the number of μops that use the ports in the combination when executing the code of the concatenation (line 6). From this value, it subtracts the number of μops , $blockRep$, of the blocking instructions (line 7). The remaining number of μops can only be executed on the ports in pc , otherwise they would have been executed on other ports.

However, it may have been determined previously for a strict subset pc' of pc that some or even all of these μops can only be executed on that subset pc' . Thus, the number of $\mu ops'$ on subsets pc' of the port combination pc , which have been determined in previous iterations of the loop, are subtracted from μops (line 10). The remaining number of μops can be executed on all ports in pc but on no other ports.

The algorithm can be optimized by first measuring which ports are used when running the instruction in isolation. The loop then does not need to iterate over all port combinations, but only over those whose ports are also used when the instruction is run in isolation. Furthermore, we can exit the loop early when the sum of the μops in the $\mu opsForCombination$ list reaches the total number of μops of the instruction.

5.2 Latency

Let I be an instruction with source operands S and destination operands D . We use the following general approach to determine the latency $lat(s, d)$ for some $s \in S$ and $d \in D$.

Let us first consider the simplest possible case:

1. The type of the source operand s is the same as the type of the destination operand d .
2. All instruction operands are *explicit* register operands, and no register operand is both read from *and* written to by I .

Then we can create a *dependency chain* of copies of I , such that the register for the destination operand of an instance of I is the register used for the source operand of the next instance of I . The other registers should be chosen such that no additional dependencies are introduced. Given such a chain c of sufficient length, we can determine $lat(s, d)$ by measuring the run time of the chain and dividing it by the length of c .

Now let us consider the case that the types of the source operand s and the destination operand d are different. Then it is impossible to create a dependency chain consisting only of instances of I . To create a chain we need an instruction C that has a source operand s_C with the same type as d , and a destination operand d_C with the same type as s . We call such an instruction a *chain instruction*. Given a chain instruction C , we can create a chain by concatenating instances of I and C , such that the destination operand of I uses the same register as the source operand of C and vice versa. Assuming we already know the latency $lat_C(s_C, d_C)$ of C we can determine the latency $lat(s, d)$ by measuring the chain's run time, dividing it by the number of occurrences of I , and by subtracting $lat_C(s_C, d_C)$. Chain instructions should ideally be instructions that have as few as possible other operands, and their latency should either be known or easy to determine in isolation.

Now let us assume there are *implicit* operands or register operands that are both read from and written to by I . Such operands are a challenge as they may introduce *additional*

dependencies: This is the case if I has implicit operands that are both read from and written to (such as, e.g., status flags), or if $s \neq d$ and s or d are both read from and written to. If we do not “break” these dependencies, then the run time of a chain involving I may be determined by the latency of such an additional dependency, rather than the latency from s to d , which we would like to determine. We break these additional dependencies by adding suitable *dependency-breaking instructions*. Such instructions overwrite an operand that is part of an unwanted additional dependency, but do not read the same operand. This makes sure that the run time of the chain is not influenced by dependencies other than the one from s to d .

In the following subsections, we describe the most interesting cases of how we create dependency chains for different types of source/destination operands.

5.2.1 Register \rightarrow Register

Both registers are general-purpose registers If both registers are general-purpose registers, we use the MOVX (“Move with Sign-Extension”) instruction to create a dependency chain. We do not use the MOV or MOVZX instructions for this purpose, as these can be zero-latency instructions on some microarchitectures in some cases, which can be executed by the reorder buffer (*move elimination*, see Section 3.1). However, *move elimination* is not always successful (in our experiments, we found that in a chain consisting of only (dependent) MOV instruction, about one third of the instructions were actually eliminated). Using the MOVX instruction avoids this uncertainty. Moreover, because the MOVX instruction supports source and destination registers of different sizes, this also avoids problems with *partial register stalls* (see Section 3.5.2.4 of Intel’s Optimization Manual [23]). A *partial register stall* occurs when an instruction writes an 8 or 16-bit portion of a general-purpose register, and a subsequent instruction reads a larger part of the register.

If at least one of the two register operands is not an implicit operand, we can also use the same register for both operands. However, if one of the operands is both read and written, it is not possible to add a dependency-breaking instruction for this implicit dependency. Thus, it would not be possible to analyze the latency of the two operands in isolation in that case. Moreover, there are some instructions that behave differently if the same register is used for multiple operands. For example, some instructions with two register operands (like XOR and SUB) are *zero idioms* that always set the register to zero (independent of the actual register content) if the same register is used for both operands. In all recent microarchitectures, these instructions break the dependency on the register that is used; on some microarchitectures, they can in some cases be executed by the reorder buffer, and do not use any execution ports (see Section 3.5.1.8 of Intel’s Optimization Manual [23]). There are also other instructions

that behave differently on some microarchitectures when the same register is used, for example the SHLD instruction (for details see Section 7.3.2).

To be able to detect such a behavior, our algorithm therefore creates microbenchmarks for both scenarios (i.e., using a separate chain instruction, and using the same register for different operands).

A third option would be to chain the instruction with itself by reversing the order of the two operands (i.e., the destination operand of one instruction would use the same register as the source operand of the next instruction). However, as this would not work for instructions with implicit register operands, we do not pursue this alternative.

Both registers are SIMD registers Since all MOV instructions for SIMD registers (i.e., XMM, YMM, and ZMM registers) can be zero-latency instructions on some microarchitectures, we use shuffle instructions instead.

SIMD instructions can perform floating-point or integer operations. If a source for a floating-point operation comes from an integer operation (or vice-versa), a *bypass delay* can occur (see Sections 3.5.1.11 and 3.5.2.3 of the Optimization Manual [23]). To capture such cases, we perform measurements with both a floating-point and an integer shuffle instruction as chain instructions.

The registers have different types If the registers have different types (e.g., one is a vector register, and the other a general-purpose register), then it is, in general, not possible to find a chain instruction whose latency could be determined in isolation. Instead, we separately measure and report the execution times for compositions of the instruction with all possible chain instructions with the corresponding types (the number of such instructions is typically rather small). Note that these times might be higher than the sum of the latencies of the instruction and the chain instruction due to bypass delays. If we then take the minimum of these times and subtract 1, we can obtain an upper bound on the latency of the instruction.

5.2.2 Memory → Register

To measure the latency of a MOV instruction from the memory to a general-purpose register, we can use a chain of

```
MOV RAX, [RAX]
```

instructions, where we assume that register RAX contains the address of a memory location that stores its own address. As its address depends on the result of the previous load, the next load can only begin after the previous load has completed.

However, this simple approach would not work for most other instructions, as they usually do not just copy a value from the memory to a register. Instead, we generalize the approach as follows: Let R_a be the register that contains the

memory address, and R_d be the destination register. We use

```
XOR Ra, Rd; XOR Ra, Rd
```

to create a dependency from R_d to R_a . Note that the double XOR effectively leaves R_a unchanged. However, since XOR also modifies the status flags, we additionally add a dependency-breaking instruction for the flags to the chain. Furthermore, if R_d is an 8 or 16-bit register, we prepend a MOVSB instruction to the chain to avoid partial register stalls.

The base register of a memory operand is always a general-purpose register. If the destination register of the instruction is not a general-purpose register, we combine the double XOR technique with the approach for registers described in the previous section to obtain an upper bound on the latency.

5.2.3 Status Flags → Register

As there are no instructions that read a status flag and write a vector register, we only need to consider general-purpose registers here.

To create a dependency from a general-purpose register R to a flag, we use the instruction TEST R, R . This instruction reads both register operands (we use for both operands register R), and writes all status flags (except the AF flag). It has no other dependencies.

5.2.4 Register → Memory

It is not directly possible to measure the latency of a store to memory, i.e., the time until the data has been written to the L1 cache. We can, however, measure the execution time of a chain with a load instruction. For the MOV instruction, we could, e.g., measure the execution time of the sequence

```
MOV [RAX], RBX; MOV RBX, [RAX].
```

However, the execution time of this sequence might be lower than the sum of the times for a load and for a store. One reason for this is “store to load forwarding”, i.e., the load obtains the data directly from the store buffer instead of through the cache. The second reason is that the address of the load does not depend on the preceding store, and thus the address computation might already begin before the store.

While the time of such a sequence does not directly correspond to the latency, it still might provide valuable insights. We therefore measure the execution time in a chain with a suitable load instruction for all instructions that read a register, and store data to the memory.

5.2.5 Divisions

For instructions that use the divider units, it is known that their latency depends on the content of their register (and memory, where applicable) operands. We test these instructions both with values that lead to high latency, and with values that lead to a low latency (we obtained those values

from Agner Fog's [12] test scripts). As most of these instructions use one operand both as input and output operand, and the output of a division with a value that leads to a high latency is often a value that leads to a lower latency, the techniques described in the previous sections for automatically creating dependency chains cannot be used in this case. We therefore handle these instructions separately. If, e.g., R is a register that is both a source and a destination register, and R_c contains a value that leads to a high latency, we can use

$$\text{AND } R, R_c; \text{ OR } R, R_c,$$

or the corresponding vector instructions, to create a dependency chain that always sets R to the same value.

5.3 Throughput

As mentioned in Section 4.2, there are different ways of defining throughput. We will now first describe how we can measure the throughput according to Definition 2. Then, we will show how the throughput according to Definition 1 can be computed from the port usage.

5.3.1 Measuring Throughput

To measure the throughput of an instruction, we first try to find a sequence of independent instances of the instruction that avoids read-after-write dependencies as much as possible. To this end, we select registers and memory locations in a way such that they are not written by one instruction of the sequence and read by a subsequent instruction. This is, however, not possible for implicit operands that are both read and written.

We then measure the execution time over several repetitions of this sequence, and obtain the throughput by dividing this time by the total number of instruction that have been executed.

We observed that sometimes longer sequences of independent instruction instances can lead to higher execution times per instruction than shorter sequences, in particular, when they use many different memory locations or registers. We therefore perform measurements for sequences of different lengths (we consider sequences with 1, 2, 4, and 8 elements).

For instructions with implicit operands that are both read and written, we additionally consider sequences with dependency-breaking instructions. However, as the dependency-breaking instructions also consume execution resources, this does not necessarily lead to a lower execution time of the sequence in all cases.

For instructions that use the divider units, the throughput can depend on the value of their operands. We test these instructions both with values that lead to a high throughput, and with values that lead to a low throughput. For this, we use the same values that we used to measure the latency of such instructions.

5.3.2 Computing Throughput from Port Usage

Intel's definition of throughput (Definition 1) assumes that the ports are the only resource that limits the number of instructions that can be executed per cycle, and that there are no implicit dependencies.

If we execute an instruction, for which these requirements hold, repeatedly, then the average wait time until the next instruction can be executed corresponds to the average usage (per instruction) of the port with the highest usage, and the number of μops on this port will be equal to the execution time (however, this is not true for instructions that use the divider unit, which is not fully pipelined).

For instructions, for which the above requirements do not hold, it is not possible to directly measure the throughput according to Intel's definition.

However, for instructions that do not use the divider unit, it can be computed from the port usage measured in Section 5.1. For 1- μop instructions, the throughput is $\frac{1}{|P|}$, where P is the set of ports that the μop can use. More generally, the throughput is the solution of the following optimization problem, where PU is the result from Algorithm 1, and $f(p, pc)$ are variables:

$$\begin{aligned} \text{Minimize} \quad & \max_{p \in \text{Ports}} \sum_{(pc, \mu) \in PU} f(p, pc) \\ \text{Subject to} \quad & f(p, pc) = 0 \quad p \notin pc \\ & \sum_{p \in \text{Ports}} f(p, pc) = \mu \quad (pc, \mu) \in PU \end{aligned}$$

The variable $f(p, pc)$ captures the share of the μops that map to the port combination pc that are scheduled on port p . A schedule maximizing the throughput will minimize the maximum port load $\max_{p \in \text{Ports}} \sum_{(pc, \mu) \in PU} f(p, pc)$.

We can reduce this optimization problem to a linear program by replacing the maximum in the objective with a new variable z , and adding constraints of the form

$$\sum_{(pc, \mu) \in PU} f(p, pc) \leq z$$

for all $p \in \text{Ports}$. The linear program can be solved using standard LP solvers.

6 Implementation

In this section, we describe various aspects of our implementation of the algorithms developed in Section 5.

6.1 Details of the x86 Instruction Set

The algorithms described in Section 5 require detailed information on the x86 instruction set, including, e.g., the types and widths of (implicit and explicit) operands. While this information is available in Intel's *Software Developer's Manual* [24], there was, until recently, no sufficiently precise machine-readable description of the instruction set.

Fortunately, Intel recently published the source code of their *x86 Encoder Decoder (XED)* [21] library. The build process of this library uses a set of configuration files that contain a complete description of the x86 instruction set. While this description is very concise, it is not well documented, and quite complex to parse (collecting the information for a single instruction requires reading multiple files). It also contains a lot of low-level details, e.g., regarding the encoding, that are not needed for our purposes.

We therefore convert this format to a simpler XML representation that contains enough information for generating assembler code for each instruction variant, and that also includes information on implicit operands.

6.2 Measurements on the Hardware

To measure the number of μ ops on each port when executing a code sequence, we use hardware performance counters [24]. For measuring the execution time, we also use a performance counter, as this makes it possible to count core clock cycles, whereas other means to measure the execution time (e.g., using the RDTSC instruction), count reference cycles (which can be different from core clock cycles due to, e.g., frequency scaling).

Before the performance counters can be used, they need to be configured to count the events of interest by writing to a model-specific register. This requires using privileged instructions. While it would be possible to read the counters in user mode afterwards, we also perform the measurements in kernel space, as this allows us to also test system instructions. Moreover, it also allows us to disable preemption and interrupts during the measurements.

To perform one measurement, we generate the following code, where *AsmCode* consists of n (as explained below) copies of the assembler code sequence we want to analyze.

Algorithm 2: Measurement

```

1 saveState()
2 disablePreemptionAndInterrupts()
3 serializingInstruction
4  $start \leftarrow \text{readPerfCtrs}()$ 
5 serializingInstruction
6 AsmCode
7 serializingInstruction
8  $end \leftarrow \text{readPerfCtrs}()$ 
9 serializingInstruction
10 enablePreemptionAndInterrupts()
11 restoreState()
12 return  $end - start$ 
```

The routine `saveState()` in line 1 saves the content of all registers and flags to the memory, and sets the stack pointer and the base pointer to valid addresses in a large enough memory area that is not used by the main program; this

way, the code in line 6 can freely modify registers or the stack without corrupting the main program. We reserve two registers, however, that store the addresses of the saved state and of the initial performance counter data; the code in line 6 is not allowed to use these two registers.

We wrap the instructions that read the performance counters (in line 4 and 8) with serializing instructions because otherwise, they could be reordered with the preceding or succeeding code.

The algorithm returns the difference between the two performance counter read operations. However, this value includes the execution time (or the μ op counts, respectively) of the serializing instructions and (partly) the instructions to read the performance counters, which is undesirable. We therefore run this algorithm twice. The first time, we use $n = 10$ copies of the assembler code we want to analyze, and the second time, we use $n = 110$ copies. By taking the difference of these two measurements, and dividing the result by 100, we obtain the average run time for one execution of the assembler code sequence we want to analyze.

We then repeat all these steps 100 times (after a separate “warm-up run” to fill the caches), and finally return the average of the results to minimize the impact of measurement errors.

The values for n were chosen such that the code is small enough to fit in the instruction cache, but large enough to allow for accurate results.

6.3 Analysis Using Intel IACA

In addition to running the code sequences generated by our algorithms on the actual hardware, we also implemented a variant of our tool that automatically analyzes them with Intel IACA. IACA treats the code sequences as the body of a loop, and reports average throughput and port usage values for multiple iterations of this loop. Thus, the results should correspond to the measurements on the actual hardware, which are also averages over executing the code sequences multiple times.

We consider the IACA versions 2.1, 2.2, 2.3, and 3.0. Intel added support for more recent microarchitectures in the newer versions, but at the same time dropped support for older ones. For microarchitectures that are supported by multiple versions, we analyze the code sequences by all of these versions, as we observed (undocumented) differences between the result from different versions of IACA for the same instructions.

6.4 Machine-readable Output

We store the results of our algorithms in a machine-readable XML file. The file contains the results for all tested microarchitectures, both as measured on the actual hardware, and as obtained from running our microbenchmarks on top of IACA.

Table 1. Tested microarchitectures, number of instruction variants, and comparison with IACA

Architecture	Processor	# Instr.	IACA	μ ops	Ports
Nehalem	Core i5-750	1836	2.1–2.2	91.43%	95.27%
Westmere	Core i5-650	1848	2.1–2.2	91.36%	94.61%
Sandy Bridge	Core i7-2600	2538	2.1–2.3	93.25%	98.24%
Ivy Bridge	Core i5-3470	2549	2.1–2.3	91.36%	97.39%
Haswell	Xeon E3-1225 v3	3107	2.1–3.0	93.10%	96.45%
Broadwell	Core i5-5200U	3118	2.2–3.0	92.83%	92.64%
Skylake	Core i7-6500U	3119	2.3–3.0	92.29%	91.04%
Kaby Lake	Core i7-7700	3119	-	-	-
Coffee Lake	Core i7-8700K	3119	-	-	-

7 Evaluation

In this section, we first describe the platforms on which we ran our tool.

Then, we compare the results we obtained for the port usage by running our microbenchmarks on the actual hardware and by analyzing them with Intel IACA. We consider a high level of agreement between the two results as evidence that results obtained using performance counter based measurements on microarchitectures which are not supported by IACA are likely also accurate.

Finally, we present several insights that we obtained from the measurement results.

7.1 Experimental Setup

We ran our tool on the platforms shown in Table 1, which includes one processor from each generation of the Intel Core microarchitecture. The machines have between 4 and 16 GB of RAM. All experiments were performed using Ubuntu 16.04. On the Westmere machine, we disabled hyper-threading, as otherwise, the performance counters did not report correct results.

The third column shows the number of instruction variants for which we obtained results. The numbers are higher for newer microarchitectures due to their larger instruction sets.

The total run time of our tool ranges from 50 minutes, on the Coffee Lake system, to 110 minutes, on the Broadwell system.

7.2 Hardware Measurements vs. Analysis with IACA

For the microarchitectures from Table 1 that are also supported by IACA, IACA reports the same μ op count for between 84.65% (Westmere) and 90.06% (Broadwell) of the instruction variants that are supported by both tools (we assume that IACA reports the same count if at least one IACA version reports this count; the fourth column in the table shows the IACA versions that support each microarchitecture).

If we ignore instruction variants with a REP prefix (which can have a variable number of μ ops), and instructions with

a LOCK prefix (for which IACA in most cases reports a μ op count that is different from our measurements), then the μ op counts are the same for the percentages in the fifth column of Table 1.

If we consider only the instruction variants for which IACA and our tool report the same μ op count, then in between 91.04% and 98.24% of the cases, the port usage as obtained from measurements on the hardware, and as obtained from running our microbenchmarks on top of IACA, is also the same. The percentages for each microarchitecture are shown in the last column of Table 1.

Differences Between Hardware Measurements and IACA

While some of the discrepancies might be due to measurement errors on the hardware, in many cases we were able to conclude that the output of IACA was incorrect.

There are, for instance, several instructions that read from memory, but that do not have a μ op that can use a port with a load unit (e.g., the IMUL instruction on Nehalem). On the other hand, there are instructions (like the TEST mem, R instruction on Nehalem), that have a *store data* and a *store address* μ op in IACA, even though they do not write to the memory.

We also found several cases where IACA is not aware that different variants of an instruction have a different port usage. On the actual hardware, the 32-bit variant of the BSWAP instruction on Skylake, for example, has just one μ op, whereas the 64-bit variant has two μ ops. In IACA, both variants have two μ ops.

In a number of cases, the sum of the μ ops on each of the ports does not add up to the total number of μ ops reported by IACA. An example for this is the VHADDPD instruction on Skylake. According to our measurements on the hardware, the port usage of this instruction is $1 * p01 + 2 * p5$. IACA also reports that the instruction has three μ ops in total. However, the detailed (per port) view only shows one μ op.

Differences Between Different IACA Versions We found a number of cases where different IACA versions reported different port usages for the same instructions on the same microarchitecture. Often, the results from the newer versions correspond to our measurements on the hardware, so in these cases, the differences seem to be due to fixes of (undocumented) bugs in earlier versions of IACA. One example for this is the VMINPS instruction on the Skylake microarchitecture. In IACA 2.3, this instruction can use the ports 0, 1, and 5, whereas in IACA 3.0 and on the actual hardware, the instruction can only use ports 0 and 1.

On the other hand, we also found a few cases where the results of an older version of IACA correspond to the measurements on the hardware. An example for this is the SAHF instruction on the Haswell microarchitecture. On the actual hardware and in IACA 2.1, this instruction can use the ports 0 and 6. In IACA 2.2, 2.3, and 3.0, however, the instruction can additionally use the ports 1 and 5.

Latency/Throughput In many cases, it was not possible to obtain accurate latency and throughput data from IACA. One reason for this is that IACA ignores several dependencies between instructions. IACA 3.0, for instance, ignores dependencies on status flags; the CMC instruction, for example, which complements the carry flag, is reported to have a throughput of 0.25 cycles by IACA, which is impossible in practice due to the dependency on the carry flag (on the actual hardware, we measured a throughput of 1 cycle). IACA also completely ignores memory dependencies; the sequence `mov [RAX], RBX; mov RBX, [RAX]` is reported to have a throughput of 1 cycle. Furthermore, based on our observations, IACA does not seem to model latency differences between different pairs of input and output operands.

7.3 Interesting Results

7.3.1 AES Instructions

We will first look at an example where our new approach for determining the latencies of an instruction revealed undocumented performance differences between successive microarchitectures.

According to Intel's manual [22], the `AESDEC XMM1, XMM2` instruction has a latency of 8 cycles on the Sandy Bridge architecture. Agner Fog [12] and AIDA64 [34] report the same latency. According to IACA 2.1 and the LLVM model, the latency is 7 cycles.

The instruction reads and writes the first operand, and reads the second operand. Based on our measurements on the Sandy Bridge system, the latency $lat(XMM_1, XMM_1)$ is 8 cycles, while $lat(XMM_2, XMM_1)$ is only about 1.25 cycles. The instruction uses 2 μ ops.

According to Intel's instruction set reference [24], the instruction performs the following operations:

```

1 STATE  $\leftarrow$  XMM1
2 RoundKey  $\leftarrow$  XMM2
3 STATE  $\leftarrow$  InvShiftRows(STATE)
4 STATE  $\leftarrow$  InvSubBytes(STATE)
5 STATE  $\leftarrow$  InvMixColumns(STATE)
6 DEST[127:0]  $\leftarrow$  STATE XOR RoundKey

```

We can see that the second operand is only needed in the last step (line 6). So, our latency measurements suggest that one of the two μ ops probably computes the XOR operation in the last step (which has a latency of 1 cycle).

We obtained the same result on the Ivy Bridge system (i.e., Sandy Bridge's successor). On the Haswell system (i.e., Ivy Bridge's successor), on the other hand, the instruction has just one μ op, and the measured latency values for both cases are 7 cycles. The same latency is reported in Intel's manual, by IACA, by the LLVM model, and by Agner Fog.

On the Westmere microarchitecture (i.e., Sandy Bridge's predecessor), which was the first microarchitecture to support the AES instruction set, the instruction has 3 μ ops, and we measured a latency of 6 cycles for both operand pairs. The same latency is reported in the 2012 version of Intel's manual [22] (the current version contains no data for Westmere), by IACA 2.1, and by AIDA64. Agner Fog did not analyze a Westmere system; there is also no LLVM model for Westmere.

We observed the same behavior for the `AESDECLAST`, `AES-ENC`, and `AESENCLAST` instructions. To the best of our knowledge, the behavior on Sandy Bridge and Ivy Bridge has not been documented before.

There are also variants of these instructions where the second operand is a memory operand instead of a register operand. For these variants, our tool reports for the Sandy Bridge system a latency of 8 cycles for the register-to-register dependency (as before), and an upper bound on the memory-to-register latency of 7 cycles. According to IACA 2.1 and the LLVM model, the latency is 13 cycles (this value was probably obtained by just adding the load latency to the latency of the register-to-register variants of these instructions). Agner Fog and AIDA64 do not report the latency of the memory variants.

7.3.2 SHLD

We will now see an example that shows that our approach can explain differences among previously published data for the same instruction on the same microarchitecture.

According to the manual [22], as well as Granlund [17], IACA, and AIDA64, the `SHLD R1, R2, imm` instruction ("double precision shift left") has a latency of 4 cycles on the Nehalem microarchitecture. Agner Fog reports a latency of 3 cycles.

The instruction reads and writes the first operand, and reads the second operand. According to our measurements, $lat(R_1, R_1)$ is 3 cycles, whereas $lat(R_2, R_1)$ is 4 cycles. Thus, $lat(R_1, R_1)$ corresponds to Fog's result, while $lat(R_2, R_1)$ corresponds to the latency the other approaches report.

On the Skylake microarchitecture, the same instruction is reported to have a latency of 3 cycles by the manual [23], by the LLVM model, and by Agner Fog. According to Granlund and AIDA64, the latency is 1 cycle.

According to our results for the Skylake system, the latency is 3 cycles if different registers are used for the two operands, but only 1 cycle if the same register is used for both operands (the Nehalem system does not exhibit this behavior).

This suggests that Granlund and AIDA64 test the latency by using the same register for both operands, while Fog uses different registers for both operands, and thus considers only the implicit dependency on the first operand.

7.3.3 MOVQ2DQ

Next, we will show an example where the port usage is modeled inaccurately by existing work.

According to Agner Fog's instruction tables, the MOVQ2DQ instruction is decoded into 2 μ ops on Skylake, one of which uses port 0, while the other can use port 1 and port 5. This is probably based on the observation that if you execute the instruction repeatedly on its own, then, on average, there is 1 μ op on port 0, and about 0.5 μ ops on port 1 and 0.5 μ ops on port 5.

However, our approach shows that the second μ op can actually use port 0, port 1, and port 5. If we execute the instruction together with a blocking instruction for port 1 and port 5, then all μ ops of the MOVQ2DQ instruction will use port 0.

According to IACA and to the LLVM model, both μ ops of this instruction can only use port 5.

7.3.4 MOVDQ2Q

The following example shows a case where existing work reports an inaccurate port usage on one microarchitecture, and an imprecise usage on another microarchitecture for the same instruction.

On Haswell, the MOVDQ2Q has, according to our results, one μ op on port 5, and one μ op that can use port 0, 1, and 5. IACA 2.1 reports the same result. However, according to IACA 2.2, 2.3, 3.0, and the LLVM model, the port usage is $1 * p01 + 1 * p015$. According to Agner Fog, the usage is $1 * p01 + 1 * p5$.

On Sandy Bridge, our measurements agree with both IACA and the LLVM model for the same instruction ($1 * p015 + 1 * p5$). Agner Fog reports the usage as $2 * p015$.

7.3.5 Instructions with Multiple Latencies

Apart from the examples already described, we also found latency differences for different pairs of input and output operands for a number of other instructions. This includes most instructions that have a memory operand and another input operand, where such differences can be expected. We also found differences for the non-memory variants of the following instructions: ADC, CMOV(N)BE, (I)MUL, PSHUFB, ROL, ROR, SAR, SBB, SHL, SHR, (V)MPSADBW, VPBLENDD(B/PD/PS), (V)PSLL(D/Q/W), (V)PSRA(D/W), (V)PSRL(D/Q/W), XADD, and XCHG.

For the (I)MUL, ROL, and ROR instructions, this behavior is described in [23]; for the ADC, and SBB instruction, the behavior has been observed by [17]. For the remaining instructions, the differences have, to the best of our knowledge, so far been undocumented.

7.3.6 Zero Idioms

According to our results, the (V)PCMPGT(B/D/Q/W) instructions are also dependency-breaking idioms, even though

they are not in the list of dependency-breaking idioms in Section 3.5.1.8 of the Optimization Manual [23].

8 Limitations

Our tool currently has the following limitations:

- We only support instructions that can be used in 64-bit mode.
- We do not support the mostly obsolete x87 floating-point instruction set.
- A number of system instructions are not supported. This includes, e.g., instructions that write to segment or control registers, instructions that trigger interrupts, the VT-x instructions for virtual machines, and instructions that use I/O ports. It also includes instructions like the *undefined instruction* (UD), and the halt instruction (HLT), which cannot be measured in a meaningful way.
- Except for the division instructions, we do not consider performance differences that might be due to different values in registers, or different immediate values. We do, however, consider immediates of different lengths, e.g., 16 and 32-bit immediates.
- We do not consider differences due to different memory addressing modes, e.g., with scale and offset. We only test instructions that only use the base register.

9 Conclusions and Future Work

We have presented novel algorithms and their implementations to characterize the latency, throughput, and port usage of instructions on all Intel Core microarchitectures, which we believe will prove useful to predict, explain, and optimize the performance of software running on these microarchitectures, e.g., in performance-analysis tools like CQA [8], Kerncraft [18], or llvm-mca [6]. The experimental evaluation demonstrates that the obtained instruction characterizations are both more accurate and more precise than those obtained by prior work.

A machine-readable document with all instruction characterizations generated by our tool is available on our website <http://www.uops.info>. We also plan to release the source code of our tool as open source. We have also implemented a performance-prediction tool similar to Intel's IACA supporting all Intel Core microarchitectures, exploiting the results obtained in the present work.

Future work includes adapting our algorithms to AMD x86 CPUs. We would also like to extend our approach to characterize other undocumented performance-relevant aspects of the pipeline, e.g., regarding micro and macro-fusion, or whether instructions use the simple decoder, the complex decoder, or the Microcode-ROM.

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