Architectural Tradeoffs for Biodegradable Computing

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ABSTRACT

Organic thin-film transistors (OTFTs) have attracted increased attention because of the possibility to produce environmentally friendly, low-cost, lightweight, flexible, and even biodegradable devices. With an increasing number of complex applications being proposed for organic and biodegradable semiconductors, the need for computation horsepower also rises. However, due to the process characteristic differences, direct adaptation of silicon-based circuit designs and traditional computer architecture wisdom is not applicable.

In this paper, we analyze the architectural tradeoffs for processor cores made with an organic semiconductor process. We built an OTFT simulation framework based on experimental pentacene OTFTs. This framework includes an organic standard cell library and can be generalized to other organic semiconductors. Our results demonstrate that, compared to modern silicon, organic semiconductors favor building deeper pipelines and wider superscalar designs. To the best of our knowledge, this is the first work to explore the architectural differences between silicon and organic technology processes.

CCS CONCEPTS

• **Hardware** → **Emerging architectures**; *Carbon based electronics*; *Impact on the environment*; Standard cell libraries; Modeling and parameter extraction; Emerging simulation; • **Social and professional topics** → Sustainability;

KEYWORDS

Biodegradable computing, organic electronics, novel device architecture, emerging devices

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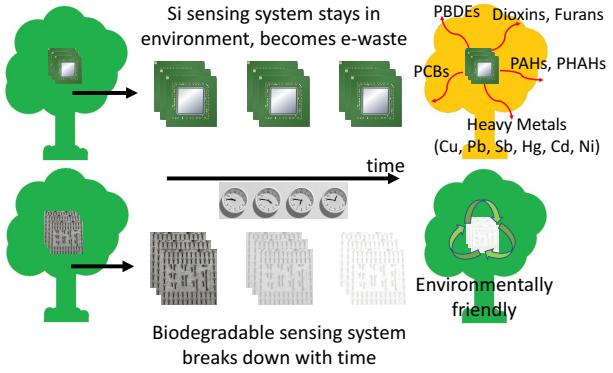


Figure 1: Schemes of non-sustainable and sustainable sensing systems. The top system stays in the environment while the bottom system will biodegrade with time. (PCBs: polychlorinated biphenyls, PBDEs: polybrominated diphenyl ethers, PAHs: polycyclic aromatic hydrocarbons, PHAHs: polyhalogenated aromatic hydrocarbons, classification of e-waste are referenced from [41].)

1 INTRODUCTION

Increasing consumer demand for the newest technologies and shortening life spans of consumer electronics has resulted in a fast-growing surplus of electronic waste (e-waste) around the globe. The number of personal computers, smartphones, tablets and other electronic gadgets discarded annually has grown rapidly and is causing serious environmental concerns [41]. There is thus an urgent need to design green electronics that are energy-efficient and made from environmentally-friendly materials [23].

Unlike most other waste, electronic devices are difficult to recycle due to their highly heterogeneous nature. Sustainable electronics recycling is labor intensive and usually requires expensive machinery that can prevent toxins found in e-waste from polluting the environment. In fact, less than 20 percent of e-waste is properly recycled [56]; most of it is buried in landfills with the risk of leaching toxins into the environment, burned in incinerators which can cause the emission of toxic fumes into the air, or exported to developing countries with relaxed environmental laws where worker exposure risks are exacerbated. Harmful materials such as lead, cadmium, and polychlorinated biphenyls (PCBs) leach out or are released into the environment upon improper processing of e-waste. When e-waste is disposed of or recycled without strict controls, there are predictable negative impacts on the environment and human health [53].

The issue of electronic waste management can partly be attributed to the stagnation in the development of technologies with

regard to the materials used. Recently, many efforts have been explored to solve the global e-waste problem, such as improving outdated regulatory policies on e-waste management, reducing the use of toxic materials, designing for easier disassembly and resource recovery to make recycling more feasible [29, 53] and extending lifetime of electronics by creating cloud servers out of decommissioned mobile phones [44]. Biodegradable organic electronics that are environmentally safe, low-cost, large-volume, and disposable have been proposed as a desirable and straightforward solution to this urgent e-waste pollution problem [23]. Biodegradable electronics exhibit transient behavior, being capable of serving their function over prescribed time frames before physically disappearing by being broken down by microorganisms into non-harmful constituents. These traits allow such systems to integrate with the environment or body with minimal harmful effects [42].

As shown in Figure 1, making electronic devices biodegradable enables electronics to be metabolized by microorganisms when devices reach their end-of-life, and thus negative effects are prevented. In addition to providing a solution to the problem of e-waste, the incorporated properties of biodegradability also enable the electronics to be used in expansive areas including environmental sensors, packaging, and medical implants [47]. The unique characteristics of such organic materials, such as flexibility and biocompatibility, suggest that they will be useful in applications that would be inaccessible for traditional inorganic compounds. Furthermore, unlike silicon, organic semiconductors can be fabricated at room temperature on thin flexible substrates.

However, moving to biodegradable computing poses many new challenges. First, organic semiconductors have an electron mobility approximately 1,000 times lower than silicon. Second, the minimum feature size is typically limited since photolithographic patterning of organic electronics is difficult due to material degradation and dissolution during wet photoresist subtractive methods. Third, the uniformity of organic semiconductors is low, which causes a significant variation in device current and threshold voltage. Finally, high-performance organic semiconductors are usually p-type. As such, the need to use unipolar p-type logic limits the frequency and noise margin of circuit design compared to complementary logic commonly used in silicon technology. The challenges of using organic semiconductors limit the operational frequency, uniformity, robustness, and integration density of organic computing systems.

Although it is hard to realize an organic technology with performance approaching that of silicon, we argue that such performance is not necessary for all use-cases of electronics and processors. Organic technology has its advantages, including less complicated fabrication processes, less stringent purity requirements, low process temperature, a nearly infinite material library, mechanical flexibility, biodegradability, and potential low-cost manufacturing. Since the first OTFTs were developed in 1986 [49], organic semiconductors' unique properties have demonstrated their utility in a variety of applications, most prominently in displays, but also in RFID tags, sensors, solar cells, lighting, and memory devices [6, 24, 28, 40, 43, 45, 48].

Moving forward, we envision exciting applications that will be enabled by biodegradable processors. First, the widespread use of environmental sensors will necessitate biodegradable sensor platforms. Unlike computers in a data center which are easy to remove from service after being placed, environmental sensors are difficult to retrieve from the environment. Additionally, applications that ship in huge volume but are seldom properly recycled are a fertile target for biodegradable computing. Examples include microprocessors and microcontrollers embedded in toys, remote controls, and RFID tags.

With a growing number of complex applications being proposed, the need for processing power with organic technology rises. While some of the use cases for organic and biodegradable computing require only modest compute power, it is still of the utmost importance to optimize the processor architecture in terms of performance, area, cost, and energy as embedded systems typically have less performance overhead to spare than desktop systems. In this work, we analyze the architectural tradeoffs for cores built with organic transistors and investigate how the constraints of organic semiconductors impact computer architecture design.

Our work makes the following contributions:

- Experimental OTFT data from devices fabricated by the authors at Princeton are used to build device models.
- A standard cell library based on experimental data is built and characterized for the organic process.
- The construction of a framework which allows a full simulation flow for organic devices.
- To the best of our knowledge, the first architectural implication analysis of an organic process across a wide range of processor design points.

The remainder of this paper is organized as follows: Section 2 introduces different applications for organic and biodegradable electronics, Section 3 describes organic semiconductor technology and our fabrication techniques, Section 4 focuses on our characterization of the organic transistors and how we use the developed device models to design a standard cell library, Section 5 presents our results and discusses computer architectural implications, Section 6 relates our work to prior research, and finally we conclude in Section 7.

2 APPLICATIONS

It is difficult to imagine living without electronic devices such as laptops, cell phones, OLED displays, etc. The ongoing technological and Internet of Things (IoT) revolutions indicate a growing demand for electronic devices. Such a revolutionary development will require an enormous number of nodes and trillions of electronic devices.

Building all of the emerging electronic devices based on traditional silicon electronics will cause a series of environmental concerns. First, a huge amount of e-waste is generated from end-of-life electronic products. The highly heterogeneous nature of silicon-based electronics makes e-waste difficult to recycle. The harmful materials, such as heavy metals, epoxy, and plastics cause long-term adverse effects. Second, a massive amount of energy is consumed during the fabrication process of high-quality inorganic semiconductors and other nanomaterials [22]. In fact, studies have shown that a modern laptop or a mobile phone contains more embodied energy, the total energy consumed in the production process, than a 1980s or 1990s automobile [54]. The increased embodied energy from electronic products hinders sustainability.

The fundamental limits of silicon electronics motivate research on biodegradable electronics which have a limited lifetime owing to their tendency to biodegrade. Biodegradable electronics have strong potential to solve the e-waste problem and reduce embodied energy. First, biodegradable electronics can decompose in a reasonable period as determined by the proposed application. The cost of recycling and end-of-life management can therefore be reduced or removed. Second, the energy cost of manufacturing biodegradable electronics is much less than silicon circuits. The less stringent requirements from materials regarding purity, combined with low-temperature deposition such as solution processing and printing, can reduce embodied energy considerably.

The research of sustainable and biodegradable electronics is rapidly developing. For example, a series of biodegradable and biocompatible materials have been developed for substrates, contacts, and active (semiconducting) materials. Synthetic polymers, paper, and even naturally occurring materials like silk have been demonstrated as potential materials for biodegradable electronics [4, 7, 12]. Demonstrations of biodegradable designs are not limited to materials and devices. Rather recent work have demonstrated the use of biodegradable electronics in more complex circuits [26, 38].

The rapid development of biodegradable electronics is motivated by a series of new potential applications. Biodegradable electronics enables the pervasive use of IoT devices without concern of creating e-waste at the devices' end-of-life. This allows everyday objects and environmental sensors to be connected (via wireless or wired connections) to the Internet without hurting the environment. Environmental sensing is especially a compelling use case of biodegradable sensors; when sensors reach their end-of-life, they can decompose in the natural environment without the need to retrieve any sensors from the environment. When used in medical electronics, drug release, and/or *in vivo* measurement, systems can degrade over time without the need for additional surgical procedures to remove the electronics.

We see many additional applications of biodegradable electronics which include anywhere electronics are embedded into devices that people do not typically think needs special recycling. Examples include electronic toys, remote controllers, temporary communication modules, RFIDs [6], clocks, watches, etc. Many of these applications are shipped in huge volume and are typically never properly recycled which makes them a prime candidate for biodegradable computing. These applications require embedded computing with modest computing requirements. While the computing requirements may be modest in embedded applications such as these, optimizing the energy, power, and performance efficiency is of the utmost importance, thus motivating work such as this paper.

Nothing is barring biodegradable electronics from being used in what is more traditionally thought of as computing devices (desktops, servers, etc.), though this work currently targets applications with embedded and modest computing needs as the current performance of OTFTs is a better match. Due to fundamental material limits (e.g., low electron mobility), the computing performance delivered by biodegradable electronics will likely always be much lower than silicon electronics even after optimization. However, organic processors can serve as a qualitative game changer, having a feature silicon will never realize: the ability to biodegrade.

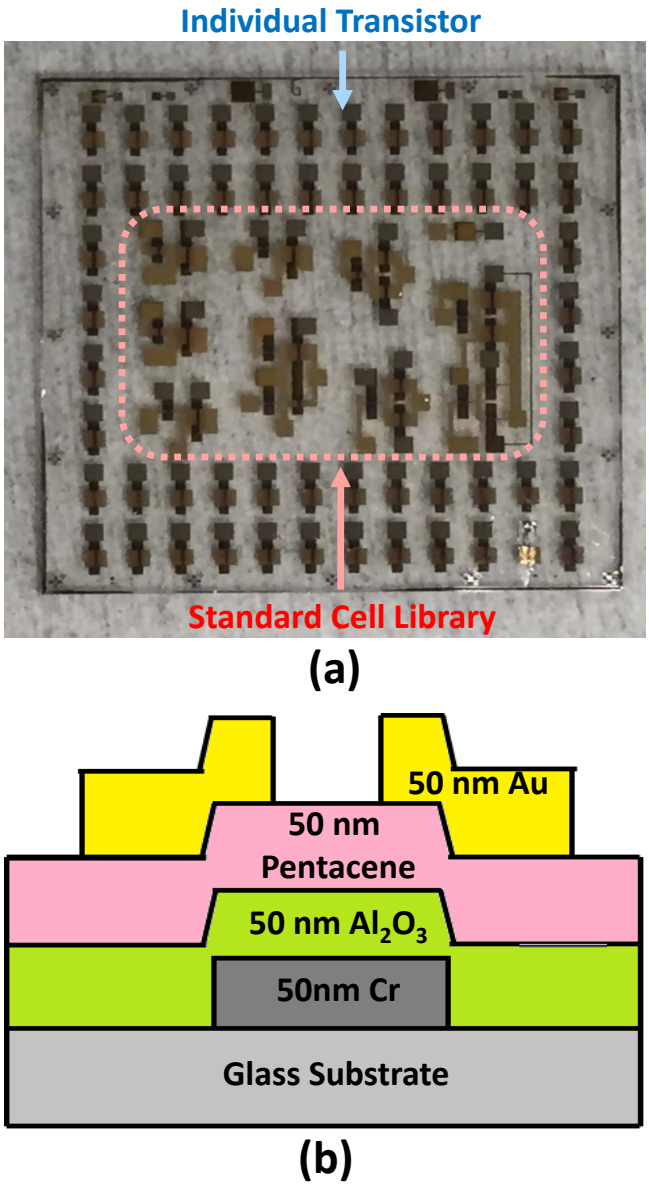


Figure 2: (a) Photograph of a 3×3 cm sample with pentacene OTFTs and group of standard library cells © Princeton University (b) Schematic view of a pentacene-based OTFT.

More advanced architectural techniques such as using massive parallelism could even be harnessed to help close the fundamental organic-silicon performance gap.

3 ORGANIC TECHNOLOGY

To construct a practical framework based on real-world organic transistors, we fabricate and characterize OTFTs to support high-level architecture research. In this section, we introduce the structure and characteristics of an OTFT.

3.1 Characteristics

Organic semiconductors have experienced substantial progress in the past thirty years, transitioning from a lab curiosity to commercially viable products. In particular, they have several unique processing characteristics. First, the processing temperature of organic semiconductors is usually at or near room temperature, which is much lower than the temperatures for other commonly used technologies like single crystalline silicon (>800 °C) and hydrogenated amorphous silicon (>200 °C) [27]. Second, organic semiconductors are not limited to high-vacuum coating, but may also be processed via low temperature and high throughput solution processing. Third, the strain and bending tolerance of organic semiconductors enable flexibility [12]. These advantages of organic semiconductors make it a competitive candidate in applications requiring low-cost, flexibility, and large area coverage [11, 13].

3.2 Challenges of Organic Thin Film Transistors

Circuits based on OTFTs that operate in accumulation mode with unipolar logic face several challenges. First, the carrier mobility of organic semiconductors is low. Although the record high mobility of 20-40 $cm^2V^{-1}s^{-1}$ can be reached on single crystal rubrene-based transistors [15], most of the system-level applications utilize organic semiconductors with mobility less than approximately 1 $cm^2V^{-1}s^{-1}$, 1,000 times lower than that of silicon. Second, photolithographic patterning of organic semiconductors is difficult due to material degradation and dissolution in wet photoresist subtractive methods [5]. Thus, shadow mask patterning that uses metal screens with patterned holes in front of the substrate, is the most widely used technique despite its limited resolution and alignment accuracy. Finally, high-performance organic semiconductors are usually p-type. Complementary application of an OTFT system often requires incorporating p-type OTFTs with either slower and less-reliable n-type OTFTs or inorganic TFT technologies (such as metal oxide TFTs), resulting in increased device area and fabrication complexity.

3.3 Fabrication Process

Our device model is based on the bottom gate, top contact pentacene OTFTs. The transistor and circuits fabricated by the authors at Princeton are illustrated in Figure 2. We use 3 × 3 cm Eagle XG glass as the substrate. The gate electrode is 50 nm sputtered Cr at 2 Å/s. Then a gate dielectric composed of 50 nm Al_2O_3 is grown by atomic layer deposition (ALD) at 175 °C. The Cr gate and the via through Al_2O_3 is patterned by photolithography and wet etching. Then the sample is treated with an octadecyl trichlorosilane (OTS) self-assembled monolayer (SAM). Finally, 50 nm pentacene (the organic semiconductor) and 50 nm Au S/D contacts are deposited by thermal evaporation as patterned by a shadow mask. The device model in the standard cell library is based on the DC characteristics measured from the fabricated transistor and inverter.

Some portions of the current OTFT design are not biodegradable, but our presented design was created to embody the most important characteristics of biodegradable electronics.

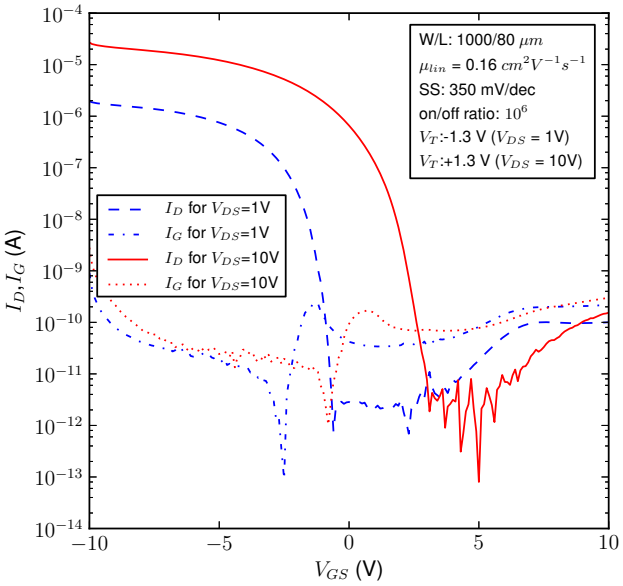


Figure 3: I_D-V_{GS} transfer characteristics of a pentacene OTFT.

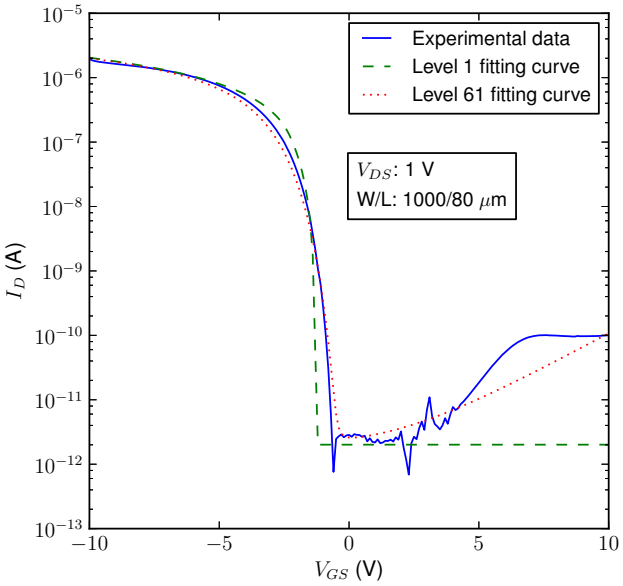


Figure 4: Fit of the I_D-V_{GS} transfer characteristics of a pentacene OTFT using level 1 and level 61 SPICE models. The solid blue line is the experimental transfer characteristic for a representative transistor we fabricated.

4 ORGANIC STANDARD CELL LIBRARY

To facilitate the design of large-scale organic circuits, we need to establish consistent design methodology and tools. The standard cell-based method allows large designs to be decomposed into basic

building block cells, which can reduce the design complexity and automate the design process. In this section, we present the development of the organic standard cell library based on the OTFTs we fabricated and measured in the lab.

4.1 Transistor Characterization

Current-voltage characteristics are measured with a probe station in an N_2 filled glove box, using an HP4155A parameter analyzer. As shown in Figure 3, the transistor shows good on-off characteristics, with a 10^6 on-to-off current ratio and a 350 mV/decade subthreshold slope. The 0.16 $cm^2V^{-1}s^{-1}$ linear mobility is extrapolated from the linear region of the I_D-V_{GS} curve. The threshold voltage (V_T) is -1.3 V when V_{DS} = 1 V, and +1.3 V when V_{DS} = 10 V, both are near the 0 V regime. The typical spread of threshold voltage across the sample is within 0.5 V.

4.2 Device Curve Modeling

From the transfer curve in Section 4.1, we construct a SPICE device model. We implement a level 1 Schichman-Hodges model and a level 61 RPI TFT model to fit the curve. The level 1 MOSFET model provides a fast and qualitative analysis regarding carrier mobility and threshold voltage. However, the level 1 model does not produce effects such as sub-V_T conduction and leakage current that are observed experimentally, making it insufficient to describe the OTFTs accurately. To solve this problem, we seek a more accurate solution in the level 61 model. Though originally developed for amorphous-Si rather than organic semiconductors, the model is designed for a 3-terminal accumulation mode transistor, with adequate parameters to describe carrier mobility, the sub-V_T region, and leakage current characteristics. As the fitting results show (see Figure 4), the level 61 model fits the device well when V_{DS} = 1 V.

4.3 Design of Standard Cells

The proposed standard cell library consists of 6 basic logic cells which can be used to cover all required logic functions. Due to the characteristic differences between technologies, the modern silicon-based CMOS design style cannot be directly applied. In the following section, we use the inverter as an example to illustrate the design flow of a standard cell.

4.3.1 Design Criteria for Organic Circuits. To demonstrate the functionality of OTFT circuits, we first focus on the design of an inverter since the same design methodology can be extended to more complex logic families. We analyze the static behavior by measuring the voltage transfer characteristic (VTC) of each type of inverter and comparing the DC parameters extracted from the curve. The switching threshold (V_M) is extracted from the intersect by mirroring the VTC, the maximum gain is obtained from the absolute value of the slope of the VTC, and the noise margin (NM) is extracted from the max equal criterion (MEC) [16].

4.3.2 Pseudo p-type Inverter: Design and Optimization. When employing unipolar designs, the simplest approach is to use conventions such as diode-load (enhancement-load) or zero-V_{GS} load (depletion-load) inverters [39]. However, due to the ratioed-logic property and a larger pull-down current, these designs usually suffer from poor gain and noise margin. Several approaches have been

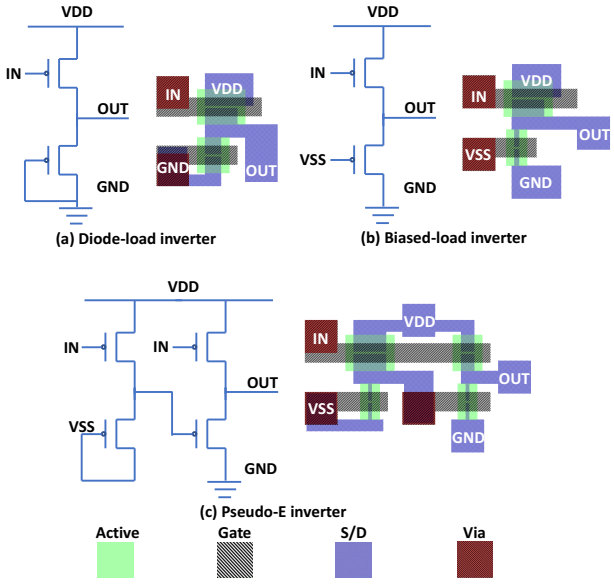
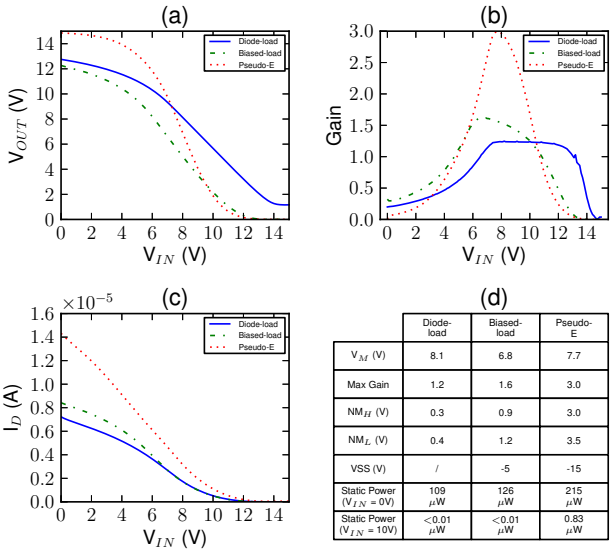


Figure 5: Schematics and layouts of pentacene-based inverters: (a) Diode-load, (b) Biased-load, and (c) Pseudo-E inverters.

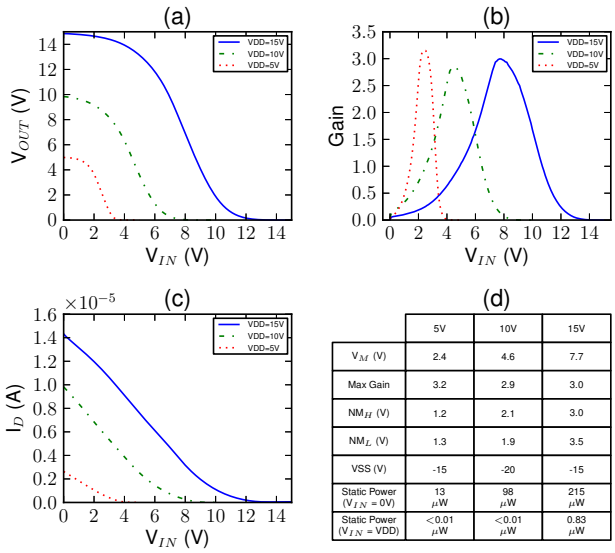


	Diode-load	Biased-load	Pseudo-E
V_M (V)	8.1	6.8	7.7
Max Gain	1.2	1.6	3.0
NM_H (V)	0.3	0.9	3.0
NM_L (V)	0.4	1.2	3.5
VSS (V)	/	-5	-15
Static Power (V_{IN} = 0V)	109 μW	126 μW	215 μW
Static Power (V_{IN} = 10V)	<0.01 μW	<0.01 μW	0.83 μW

Figure 6: Characteristics of diode-load, biased-load, and pseudo-E inverters: (a) VTC (b) gain (c) drain current (d) comparison of DC parameters.

investigated to further improve performance, such as dual-V_T [36], dual-gate [32], and pseudo-CMOS design [21].

In the following section, we implement a pseudo-E type pseudo-CMOS inverter and compare it with diode-load and biased-load inverters. The reason to choose a pseudo-E design is that it does not require extra processing steps compared to dual-V_T or dual-gate



	5V	10V	15V
V_M (V)	2.4	4.6	7.7
Max Gain	3.2	2.9	3.0
NM_H (V)	1.2	2.1	3.0
NM_L (V)	1.3	1.9	3.5
VSS (V)	-15	-20	-15
Static Power (V_{IN} = 0V)	13 μW	98 μW	215 μW
Static Power (V_{IN} = VDD)	<0.01 μW	<0.01 μW	0.83 μW

Figure 7: Characteristics of a pseudo-E inverter at VDD = 5 V, 10 V and 15 V: (a) VTC (b) gain (c) drain current (d) comparison of DC parameters.

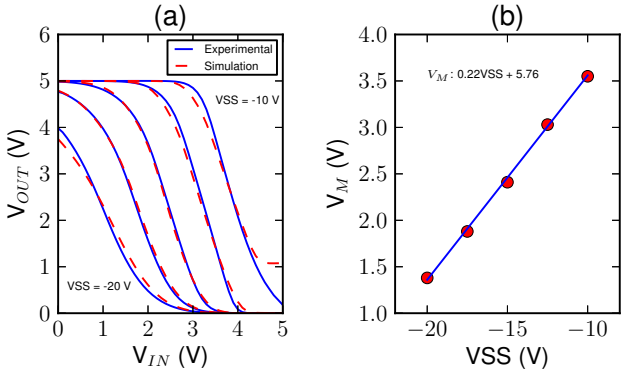


Figure 8: (a) VTC characteristics of a pseudo-E inverter at different VSS from experimental data and simulation. (b) The relationship between switching threshold and applied VSS from -10 V to -20 V.

implementations. It can be designed for enhancement mode transistors in the low V_{DS} regime, which fits our device model. Figure 5 shows the circuit design and layout of (a) diode-load inverter, (b) biased-load inverter, and (c) pseudo-E inverter.

Figure 6 shows the VTC of these three inverter designs. The diode-load inverter is the simplest structure with zero-V_{DS} bias. As expected, the VTC performance of the inverter is very weak, the gain is just barely larger than 1, and the noise margin is only around 0.3 V. The biased-load inverter adds one additional terminal with negative bias VSS to tune the switching threshold (V_M). The performance slightly improves with 1.6 maximum gain and 1 V noise margin. The shortcomings of designs (a) and (b) mainly come from the ratioed pull up network. Since the load transistor cannot be turned off when the input is low, the voltage output high (V_{OH}) of the circuit relies on the sizing difference between the drive (top) and load (bottom) transistor, which limits noise margin and gain. For the pseudo-E inverter, the left two transistors work as a level shifter stage, which makes the bias voltage of the load transistor depend on input voltage. Such design will effectively improve the low-input performance and allows V_{OH} to reach VDD. From the comparison of the VTC, we can see that the performance of the inverter can be increased dramatically with the negatively biased terminal and the level shifter, the noise margin increases ten times, and the gain improves 2.5 times compared to a diode-load inverter. From the above analysis, we select the pseudo-E inverter for future designs.

4.3.3 Pseudo-E Inverter Characterization. To analyze how to select VDD and VSS for a pseudo-E inverter, we set VDD at three different levels: 5 V, 10 V, or 15 V, and we set VSS to make V_M close to VDD/2. Figure 7 shows that the VTC at different VDD values maintains a similar shape, the gain is approximately 3, and the noise margin is about 20% to 25% of VDD. Reducing VDD can benefit the logic in a variety of ways. First, the worst case power consumption will be reduced dramatically. When the input is low, the static power consumption of the 5 V inverter will be only 6% that of the 15 V inverter. Second, with a small VDD, the impact of drain induced V_T shift will be less. As seen in the transfer characteristics, V_T increases with high VDD. Thus, reducing VDD can limit the range of drain-source voltage drop on each transistor, which can help to improve the uniformity of the device. We fix VDD to 5 V in our following simulation.

To choose the appropriate value for VSS, we analyze how VTC changes with various bias voltages. From Figure 8(a), with VSS changing from -10 V to -20 V, we can see the VTC can approximately shift horizontally with increasing VSS. Additionally, from Figure 8(b), the VSS and V_M exhibit a linear relationship, with slope = 0.22 (i.e. when VSS increases by 10 V, V_M increases by 2.2 V). When V_M = VDD/2, the regression shows that VSS should be -14.8 V. Therefore, we set VSS to be -15 V in our simulation. The linear relationship between V_M and VSS gives us the flexibility to design a robust circuit. For example, the cross-sample variation of V_M from process variation can be tuned by applying a different VSS.

To confirm the accuracy of the device model extracted from Section 4.2, we compare the simulation and experimental results for VSS by using the level 61 model obtained from Section 4.2. When V_M is close to VDD/2, the level 61 simulation model fits the experimental curve well. Since we set VSS at -15 V, we can precisely predict the static performance of the pseudo-E inverter. As a result, the level 61 SPICE model can be applied to predict the performance of the standard cell library.

4.3.4 Other Standard Cells. We repeat the above analysis for NAND and NOR gates and decide to use the pseudo-E design for both since only the pseudo-E design achieves full voltage swing with shorter gate delay. Figure 9 shows the schematics for NAND and NOR gates used in the standard cell library. To speed up the circuit and provide the synthesis tool more choices of gates, we also design three-input NAND and NOR gates, using similar structures

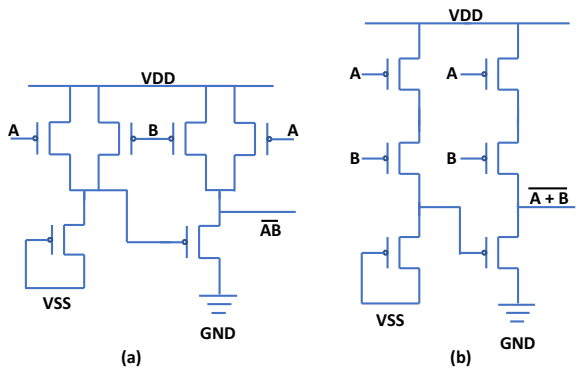


Figure 9: Schematics of pseudo-E based logic: (a) NAND gate (b) NOR gate.

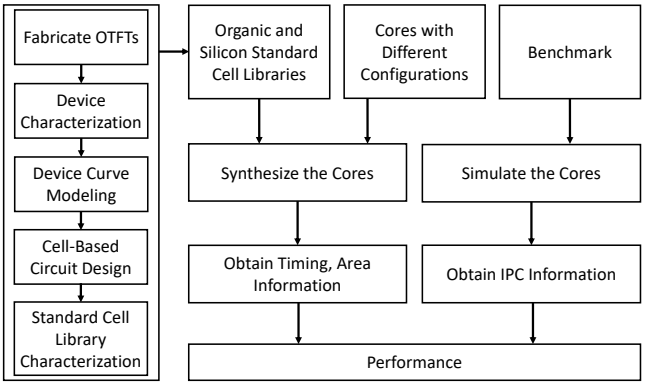


Figure 10: Architecture simulation flow applied to organic technology.

like the two input cases. In addition to the universal logic gate family, a register is also necessary for sequential logic. We build a D-flip-flop with preset and clear and use it throughout our designs.

The fine-tuning of circuit sizing is crucial for creating a good logic gate. However, adjusting the parameters and running simulations manually is time-consuming. Therefore, we utilized a script to explore the design space and select the best parameter sets for each gate. The switching threshold, noise margin, gate delay, and area are all taken into consideration when we define the utility function, which is used to evaluate the quality and efficiency of the gates built with different parameter sets.

4.4 Characterizing the Standard Cell Library

The organic standard cell library is characterized with the non-linear delay model (NLDM)[25]. The NLDM is a conventional and fast voltage-based model that relies on input signal slope and output capacitive loads. The delay information is obtained from the SPICE simulation and formatted into a look-up table (LUT) format. The capacitive load model used in the NLDM neglects the resistive and inductive effect for interconnection, which is suitable for both silicon and organic technologies.

Synopsys's SiliconSmart, a comprehensive tool for standard cell characterization, is used in our work to generate the Liberty library file. The tool identifies the logic function for the given netlist and runs an HSPICE simulation for all the characterization points over a range of input slopes and load capacitances to generate the LUT format library.

5 EVALUATION

In this section, we present results that quantify the performance of the same design synthesized with different semiconductor technologies. We measure and compare the performance and area costs of organic technology versus conventional silicon technology to demonstrate the architectural differences motivated by the underlying semiconductor. These results provide insights into high-level architecture design for the organic process as well as a comparison between silicon and organic processes.

5.1 Simulation Methodology

We synthesize cores with various configurations using both the organic standard cell library described in Section 4 and the reduced silicon library to observe how process technology affects core performance and determine the optimal design point. The reduced silicon library has been cut down to have the same number of cells as the organic library. It is important to reduce the fully-featured silicon library to a reduced library that matches the same cells in our organic cell library to provide a fair comparison and remove effects caused by library richness mismatch. The simulation flow we use is shown in Figure 10. A trimmed 6 gate TSMC 45 nm standard cell library for silicon and our organic standard cell library are adopted in the experiments.

There are several open source and synthesizable processors which enable researchers to conduct their own experiments [2, 3, 8, 10]. In this work, we seek to find a parameterized processor whose number of pipeline stages can be changed easily. Therefore, we choose the AnyCore toolset [10], the updated version of FabScalar [9], to generate superscalar cores with different configurations. AnyCore is a synthesizable register-transfer-level (RTL) design of an adaptive superscalar core that can mimic arbitrarily fixed cores in a large design space. The RTL description of the core is highly parameterized, providing the core the flexibility to change superscalar structure sizes, superscalar widths, and pipeline depth. To reduce simulation time, 100 million instructions of the Dhrystone benchmark [52] and of SimPoints derived from six SPEC CPU2000 [17] integer benchmarks are executed. We obtain the instructions per cycle (IPC) of a particular configuration by using AnyCore's cycle-accurate C++ simulator. Synthesis is performed with the Synopsys Design Compiler to measure the minimum clock period and area.

We present our results for three sets of experiments. First, we measure the minimum clock period and area for the execution stage in the execution pipelines of the AnyCore design. This execution stage includes a forward bypass check and two arithmetic logic units (ALUs), one for simple ALU operations and one for complex multiplication and division. The complex ALU consists of two Synopsys DesignWare stallable, pipelined multipliers and dividers,

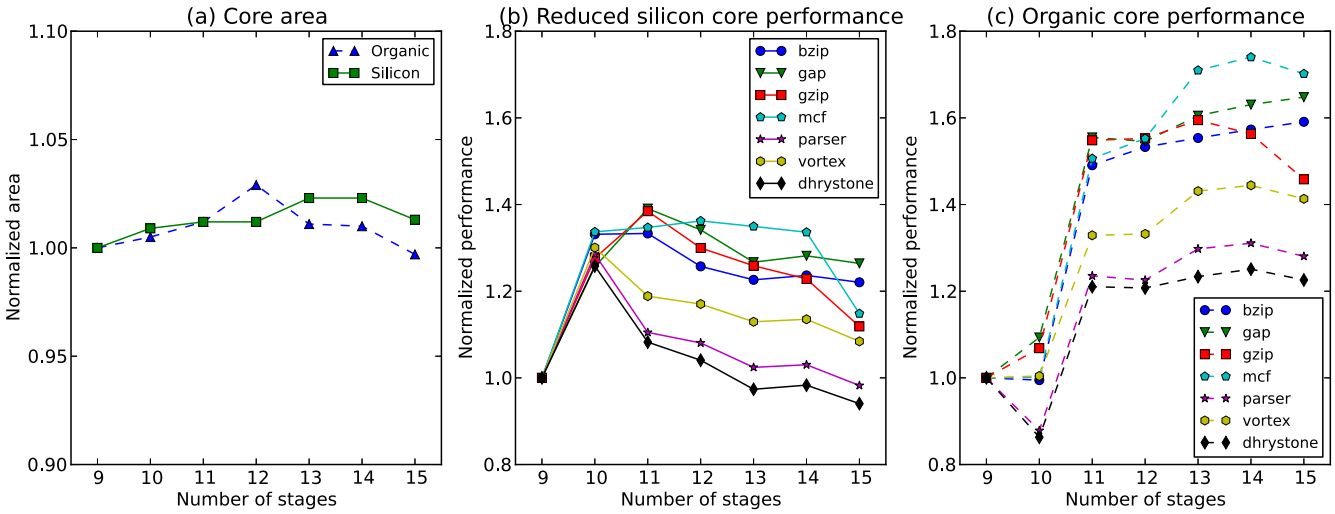


Figure 11: (a) Core area for organic and silicon processes versus number of pipeline stages. (b,c) Core performance versus number of pipeline stages for (b) silicon and (c) organic processes.

which implement a parameterized number of pipeline stages and automatic pipeline retiming.

Second, we explore the optimal pipeline depth for the whole core. Pipeline depth is a trade-off between improved clock rate and lower IPC caused by higher branch mispredict penalties and longer stalls to resolve hazards. To find the optimal pipeline depth, we need to expand the processor pipeline. We start with the baseline design of AnyCore, which is a single issue superscalar, out-of-order execution core with a nine stage pipeline. However, the stages that could be sub-pipelined in AnyCore are not on the critical path. By default, increasing the number of pipeline stages would only degrade the performance by decreasing IPC without achieving a higher clock frequency. Instead, we synthesize the baseline design and cut the stage which is on the critical path manually to ensure an improved clock rate. We created seven cores with different pipeline depths for both silicon and organic libraries.

Third, we measure the performance of superscalar cores with different widths. AnyCore provides good flexibility over a wide range of cores with different front-end issue widths and back-end execution widths. We select thirty designs with varying width combinations to conduct the experiment.

5.2 Optimal ALU Depth

Pipelining is widely used to improve the performance of digital circuits since it can increase throughput by shortening clock period. For a superscalar core, it is not practical to require multiplication and division to finish in one cycle. In this experiment, we exploit the complex ALU, which is composed of two multipliers and dividers, to check how the chosen semiconductor process changes the optimal pipeline depth.

Figure 12 shows the clock frequency and area that silicon and organic processors can achieve for ALUs with different numbers of stages. As Figure 12 shows, the operating frequency for the silicon-based ALU does not increase as the number of stages exceeds 8

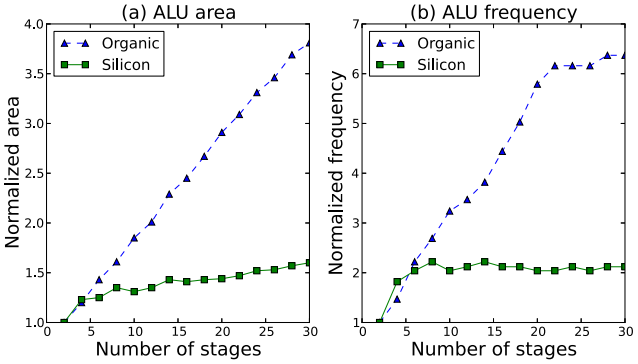


Figure 12: (a) Area and (b) clock frequency for ALUs built with different numbers of stages and synthesized with different libraries.

while the area still rises slowly. This implies that the optimal ALU pipeline depth for the silicon process is approximately 8. In contrast, both clock frequency and area for the organic processors grow linearly with pipeline depth, topping out around 22 stages. These results suggest that organic processors are better suited to a longer pipeline design.

5.3 Optimal Pipeline Depth

Pipeline depth is one of the fundamental design choices when designing a microprocessor. Theoretically, deeper pipelining improves throughput by increasing the clock frequency of a core. However, this improvement might be offset by additional stalls due to the longer critical path between dependent instructions as well as a higher branch mispredict penalty. Optimizing the pipeline depth is based on balancing the clock rate and IPC to maximize the number of instructions executed per second.

The underlying semiconductor technology, the processor microarchitecture, and the targeted workloads are all factors that affect the optimal pipeline architecture [20]. Previous work [1, 19, 51] has pointed out that, as feature size shrinks, the slower scaling of wiring compared to logic delay makes optimal pipeline depth for superscalars shallower than with ideal scaling. This is because superscalars do not have sufficient parallelism to hide the relatively higher wire delays. While the impact of pipeline architecture on the silicon microprocessors has been well studied previously [14, 20], there has not been effort devoted to pipeline architecture for the organic or biodegradable processes.

The baseline design is a nine stage superscalar core which has a front-end width of one along with three execution pipes handling different types of instructions. The operating frequency of the baseline design for OTFTs is approximately 200 Hz while for silicon it is 800 MHz. The optimized design frequency is approximately 40 Hz and 1.36 GHz respectively for organics and silicon. The modest performance of OTFTs can be a decent match for applications that need modest computing such as sensors, RFIDs, toys, remote controllers, etc., as described in Section 2. Many of these embedded processor use cases employ embedded processors in the kHz range [31, 35]. Opportunities also exist to improve the performance of OTFTs by decreasing the feature size of the OTFTs, creating a richer organic cell library, and using higher-performance organic semiconductors such as DNTT, which has roughly 10× the mobility of the archetypal pentacene used here [57]. The area and performance data for both processes are normalized to their own baseline performance (nine stages).

As shown in Figure 11, the respective areas of the two processes are flat as pipelines become deeper. The overall performance (IPC × clock frequency) for the two processes are also plotted in Figure 11. We simulate all benchmarks on seven pipeline depth configurations for both process technologies. One trend is that the optimal pipeline depth for the silicon process is smaller than that for the organic process. For most of the benchmarks, the best performance happens at pipeline depths of 10 or 11 stages when running on silicon cores while the optimal performance points for organic cores occur at 14 or 15 stages. The optimal points happen when the clock rate improvements gained from having a deeper pipeline can no longer compensate for the IPC loss.

5.4 Optimal Superscalar Width

In this section, we discuss the impact of the selected process technology on the optimal superscalar width for superscalar cores. In general, wider superscalar cores provide an increased level of instruction level parallelism (ILP). However, higher IPC comes at the cost of issue logic complexity that can have significant overhead in cycle time and latency due to the higher gate and interconnect delays. This is particularly the case for deep sub-micron designs, where interconnect delay is usually more dominant than gate delay. The overhead model depends on actual processor implementation, circuit design, and fabrication technology.

In this superscalar width experiment, we synthesize AnyCore with different front-end and back-end width configurations. The front-end width determines the width of fetch and dispatch stages, which is the number of instructions that can be fetched, decoded

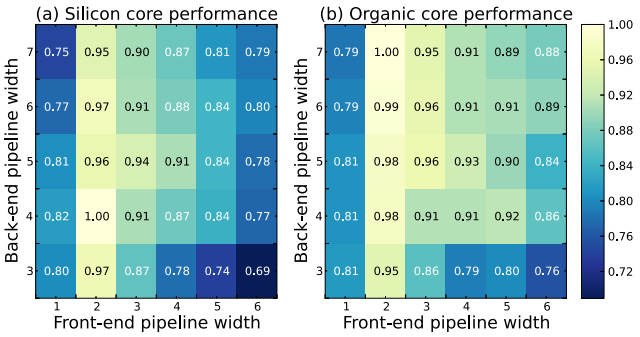


Figure 13: Core performance of (a) silicon and (b) organic processes for different width configurations.

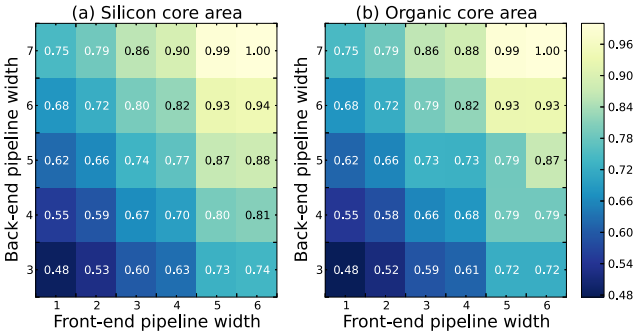


Figure 14: Core area of (a) silicon and (b) organic processes for different width configurations.

and dispatched into the issue queue. The back-end width decides how many execution pipes for ALU instructions are integrated into the core. The baseline design has one front-end along with three execution pipes: one each for memory instructions, control instructions, and all other ALU related instructions. Note that the back-end width only changes the number of ALU pipes, while the number of memory and control execution pipes stays the same. The performance number is obtained by averaging performance number (IPC × clock frequency) of seven SPEC CPU2000 integer and Dhrystone benchmarks.

Figure 13 and 14 show the matrix M for normalized performance and area of these synthesized cores, in which $M[i][j]$ represents the cores with i execution pipes and fetch width j. All performance and area data are normalized to the maximum performance/area for each technology. In the area matrices in Figure 14, we can see that the areas for silicon-based cores are similar to the organic core areas. In comparison, the optimal superscalar width for organic cores is three execution pipes wider than silicon. As shown in Figure 13(b), organic cores have better performance under conditions when the cores are wider.

The performance differences between configurations are more evident for the silicon process. The optimal point for silicon is located at $M[4][2]$ and has a more significant performance difference from nearby points compared to the organic process, implying that

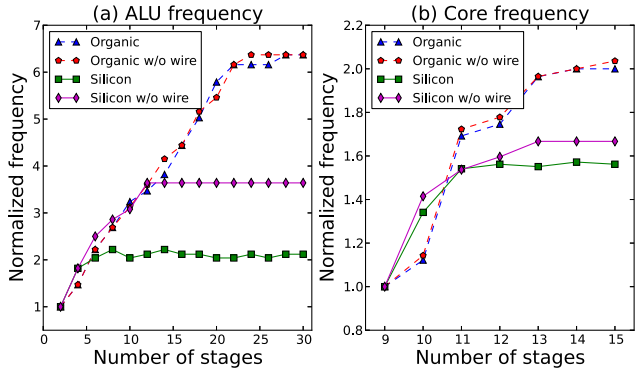


Figure 15: Frequency trend for (a) ALUs and (b) cores built with different numbers of stages and synthesized with different libraries.

organic technology is less sensitive to front-end and back-end width change.

5.5 Discussion

For the processor core pipeline depth experiment, we extend the pipeline by repeatedly cutting the stage which is on the critical path. Since the critical path might happen at different places when synthesizing the core using different cell libraries, the choice of this cutting strategy results in different designs for the same number of stages as shown in Figure 11. Though IPC is slightly different for designs with the same number of stages that are cut in different ways, the dominant factor of the trend is the frequency difference. As shown in Figure 15(b), for 14-stage processors, the frequency of the organic core is twice as high as its baseline frequency, while the silicon core can only achieve 1.5× improvement. Also, similar to the frequency trend of ALU depth, the frequency curve obtained for the silicon core reaches the maximum value at a lower number of stages.

As discussed in previous sections, processors designed using the organic process favor having deeper and wider pipelines than processors built in the silicon process. This is largely due to the difference in the ratio of wire delay to gate switching speed. When synthesizing the designs with zero wire delay, we observe that the amount of logic per pipeline stage becomes similar for both processes, which is different from when wire delay was taken into consideration. From Figure 15, we can see that the frequency is higher and the optimal pipeline depth is deeper for a silicon design without wire cost compared to a one with wire cost.

The organic process has relatively fast wires compared to the switching speed of the organic transistors. While it is true that current sub-micron silicon processes have seen less than ideal wire delay scaling, this is likely only a tiny portion of the difference in wire speed to logic ratio. A much larger component is the large differences in electron mobility (~1000x difference) and the fact that in the organic library, only unipolar PMOS designs are used (due to lack of n-type organic material), while in silicon, complementary logic is used.

One way that the differing wire-speed to gate-speed ratio affects architecture is that, as the pipeline length grows, a wire's length contributes more significantly to the clock cycle [46]. The feedback signals (bypassed data, stall signals, branch resolution, etc.) must travel farther from the end of the pipeline to the front in deeper-pipelined processors. One extreme solution to this problem is to add additional pipeline stages solely for driving long wires, as is done in the Pentium 4 pipeline [18]. A similar argument holds for wider-issue designs where communication between the pipelines becomes a significant portion of the clock cycle as more pipelines are added. In both examples, if the wire cost is inexpensive (as it is in the organic process), then longer pipelines and wider designs are favored. Previous works [1, 19, 51] have studied the effects of wire delay on processor design in greater detail.

In addition to the influence of wire delay, the results are affected by the differing timing delay ratio between the same logic gate of different cell libraries. In the ALU pipeline depth experiment, for earlier stages, the design synthesized using the silicon library tends to use more three input NAND gates and have less logic in one stage versus the organic one, which favors the two input NAND gate more. The weak pull-down nature of unipolar p-type logic results in the imbalance between rise time and fall time. This rise time and fall time difference make the three input NAND gate less desirable for the organic library. A more complete library is needed to fully characterize the effect of rise time/fall time imbalance caused by the PMOS-only organic library.

6 RELATED WORK

The research fields of designing complex systems utilizing organic semiconductors have developed rapidly. In this section, we compare our work with other groups in three related research fields: microprocessors based on organic thin film transistors, air-stable, high-performance organic semiconductors, and the standard cell library design.

6.1 Processors Made with Organic Technology

In 2008, a single cycle organic microprocessor based on unipolar p-type pentacene was reported by Myny et al. [34] with an 8-bit bus width and 40 Hz clock frequency. Their work proves that organic semiconductors can be integrated within a complex computing system. In 2014, with a similar architecture, their microprocessor was optimized with a hybrid organic/oxide complementary technology, reaching a 2.1 kHz operational speed [33], indicating that optimization in device technology can lead to more than 50 times increase in operational speed. The considerable room remains for core- and system-level optimization.

6.2 Organic Systems based on High Mobility, Air-Stable Organic Semiconductors

Considerable research has focused on the development of organic semiconductors with high mobility and air stability. Researchers found that heteroaromatics like fused thiophenes can be introduced to increase the stability. Organic semiconductors such as BTBT [50], DNTT [57], and DATT [37] represent a few examples. In 2012, C_{10}-DNTT based transistors and ring oscillators were

reported by Zschieschang et al. [57], with reported field-effect mobility of 4.3 $cm^2V^{-1}s^{-1}$ and 68 mV/dec sub-threshold slope. The ring-oscillator can function at 3 V with a fast 5 μs propagation delay per stage. In 2015, Yokota et al. [55] developed a real-time multipoint thermal sensing system using DNTT active-matrix circuits. The system can work with a sensitivity of less than 0.1 K and 100 ms response time. Instead of focusing on improving device performance or small-scale systems (ring-oscillators, active matrix circuits, etc.), our work focuses on high-level architectural trade-offs. Though our work is based on pentacene, the same methodology can be applied to systems based on other organic semiconductors or other thin film or nanostructured semiconductors.

6.3 Other Standard Cell Libraries for Organic Thin Film Transistors

Several standard cell libraries have been implemented for OTFTs previously. A 7-gate standard cell library built with interdigitated and corbino OTFTs is presented in [30]. As only p-type transistors are available, the standard cells follow the ratioed pseudo-PMOS style with three power rails. Another 8-gate standard cell library with mirror adder has been implemented and used to build a microprocessor [34]. These small combinational circuits and microprocessors have been built as proof-of-concept designs focusing on the physical layout by device research groups with **no architectural forethought**. In contrast, this work utilizes the timing information extracted from standard cell library and evaluates different architectural designs and applies computer architecture techniques to optimize system level core design given new technological constraints.

7 CONCLUSIONS AND FUTURE WORK

This work presents architectural tradeoffs in the creation of processors built on organic thin-film transistors. Because OTFTs have the potential to form the basis of biodegradable electronics, they represent a qualitative game changer to the environmentally friendly electronics field. Without the need to properly recycle electronics and microprocessors, electronics can be used in more applications without environmental pollution concerns. In this work, we constructed a standard cell library along with a complete simulation framework fueled by measurements of organic transistors and cells that we have fabricated in our lab. Using this framework, we have evaluated different architectural trends and found that organic transistors favor deeper pipelines and wider superscalar designs compared to their inorganic (silicon) counterpart. Deeper pipelines and wider designs are favored in organic electronics due to the relatively fast wires when compared to transistor/gate delay.

This work is the first work that investigates architectural tradeoffs in OTFT designs, but we hope that it is not the last. As future work, we envision investigating more architectural tradeoffs such as energy optimization, the extensive use of parallelism to mitigate the performance challenges of using organic materials, possible ISA-level implications of OTFT designs, and further device refinement as well as fabricating a complete and optimized microprocessor.

Additionally, as part of future work, we are investigating the use of dynamic logic as unipolar transistor design favors the use of dynamic logic because only roughly half the transistors are needed and switching time can be faster with the tradeoff being possibly worse power requirements.

ACKNOWLEDGMENTS

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