Title: **Back Panel**

Approved: YES

Rev: **04**Project: **PhyWhisperer-USB**License: **GPL**Date: **2019-11-11**Time: **10:05:06 PM**Sheet **1** of **8**

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File: **ct_back.SchDoc**

XC7S15-1FTGB196C

IO_25_34	L5	
IO_L24N_T3_34	N4	USB D7
IO_L24P_T3_34	P5	USB D6
IO_L23N_T3_34	M4	
IO_L23P_T3_34	M5	
IO_L22N_T3_34	L2	USB A1
IO_L22P_T3_34	L3	FPGA CWIO2
IO_L21P_T3_DQS_34	P3	USB A5
IO_L21N_T3_DQS_34	P4	USB A6
IO_L20N_T3_34	N1	FPGA CWIO7
IO_L20P_T3_34	P2	FPGA CWIO6
IO_L19N_T3_VREF_34	M2	FPGA CWIO1
IO_L19P_T3_34	M3	FPGA CWIO0
IO_L18N_T2_34	L1	USB A0
IO_L18P_T2_34	M1	FPGA CWIO8
IO_L17N_T2_34	L3	USB A7
IO_L17P_T2_34	L4	
IO_L16N_T2_34	K3	USB SPARE0
IO_L16P_T2_34	K4	F VBDC
IO_L15N_T2_DQS_34	J1	USB D3
IO_L15P_T2_DQS_34	J2	USB D4
IO_L14N_T2_SRCC_34	H1	USB A3
IO_L14P_T2_SRCC_34	H2	USB A4
IO_L13N_T2_MRCC_34	H3	USB D2
IO_L13P_T2_MRCC_34	H4	
IO_L12N_T1_MRCC_34	F4	
IO_L12P_T1_MRCC_34	G4	
IO_L11N_T1_SRCC_34	C1	FPGA CWIO5
IO_L11P_T1_SRCC_34	D1	USB CLK
IO_L10N_T1_34	D2	LED TRIG
IO_L10P_T1_34	E2	FPGA CWIO10
IO_L9N_T1_DQS_34	F1	FPGA CWIO4
IO_L9P_T1_DQS_34	G1	USB A2
IO_L8N_T1_34	F2	FPGA CWIO9
IO_L8P_T1_34	F3	FPGA CWIO3
IO_L7N_T1_34	D4	
IO_L7P_T1_34	E4	
IO_L6N_T0_VREF_34	C4	
IO_L6P_T0_34	C5	
IO_L5N_T0_34	B1	FPGA CWIO11
IO_L5P_T0_34	B2	USB NWE
IO_L4N_T0_34	A5	USB D1
IO_L4P_T0_34	B5	USB D5
IO_L3N_T0_DQS_34	A2	LED CAP
IO_L3P_T0_DQS_34	B3	USB NRD
IO_L2N_T0_34	A3	USB NCS
IO_L2P_T0_34	A4	USB SPARE1
IO_L1N_T0_34	C3	
IO_L1P_T0_34	D3	
IO_0_34	B6	USB D0

U2C

XC7S15-1FTGB196C

IO_25_34	M10	USERIO D7
IO_L24N_T3_D16_14	P11	USERIO D4
IO_L24P_T3_D17_14	P10	USERIO D6
IO_L23N_T3_D18_14	N11	USERIO D3
IO_L23P_T3_D19_14	N10	USERIO D5
IO_L22N_T3_D20_14	P13	USERIO D0
IO_L22P_T3_D21_14	P12	USERIO D2
IO_L21N_T3_DQS_D22_14	M14	F USB14
IO_L21P_T3_DQS_14	N14	F USB13
IO_L20N_T3_D23_14	M12	USERIO D1
IO_L20P_T3_D24_14	M11	F USB19
IO_L19N_T3_D25_VREF_14	K12	F USB16
IO_L19P_T3_D26_14	K11	F USB17
IO_L18N_T2_D27_14	L14	F USB9
IO_L18P_T2_D28_14	L13	F USB10
IO_L17N_T2_D29_14	L12	F USB15
IO_L17P_T2_D30_14	L11	
IO_L16N_T2_D31_14	L13	F USB11
IO_L16P_T2_CSI_B_14	L12	F USB20
IO_L15N_T2_DQS_DOUT_CSO_B_14	L14	F USB12
IO_L15P_T2_DQS_RDWR_B_14	M13	FPGA TRIGOUT
IO_L14N_T2_SRCC_14	H14	F USB8
IO_L14P_T2_SRCC_14	H13	F USBFE CLK
IO_L13N_T2_MRCC_14	H12	
IO_L13P_T2_MRCC_14	H11	
IO_L12N_T1_MRCC_14	F11	F USB27
IO_L12P_T1_MRCC_14	G11	USERIO CLK
IO_L11N_T1_SRCC_14	C14	F USB2
IO_L11P_T1_SRCC_14	D14	F USB4
IO_L10N_T1_D15_14	E13	F USB5
IO_L10P_T1_D14_14	F13	F USB6
IO_L9N_T1_DQS_D13_14	F14	F USB1
IO_L9P_T1_DQS_14	G14	F USB7
IO_L8N_T1_D12_14	D13	F USB3
IO_L8P_T1_D11_14	D12	
IO_L7N_T1_D10_14	E12	
IO_L7P_T1_D09_14	F12	
IO_L6N_T0_D08_VREF_14	C12	F USB30
IO_L6P_T0_FCS_B_14	C11	F USB25
IO_L5N_T0_D07_14	B14	F USB0
IO_L5P_T0_D06_14	B13	F USB32
IO_L4N_T0_D05_14	A13	F USB31
IO_L4P_T0_D04_14	A12	F USB29
IO_L3N_T0_DQS_EMCLK_14	A10	F USB21
IO_L3P_T0_DQS_PUDC_B_14	B10	F USB22
IO_L2N_T0_D03_14	C10	F USB23
IO_L2P_T0_D02_14	D10	F USB24
IO_L1N_T0_D01_DIN_14	B12	FPGA CDOUT
IO_L1P_T0_D00_MOSI_14	B11	F USB28
IO_0_14	E11	F USB26

U2D

VCCIO

10k

R32

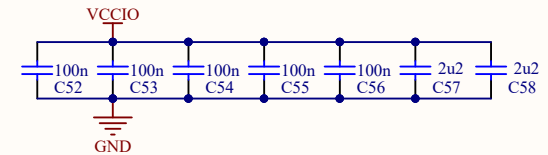
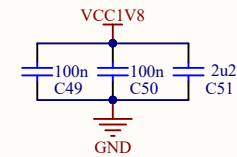
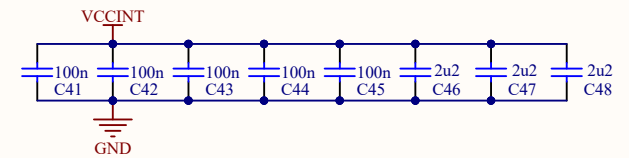
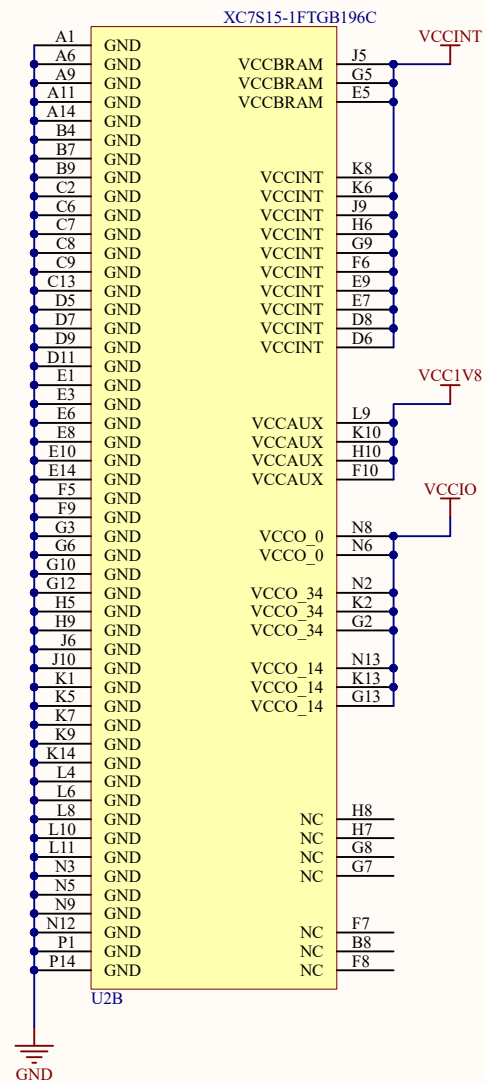
Title: **FPGA I/O**Rev: **04**Project: **PhyWhisperer-USB**Date: **2019-11-11** Time: **10:05:07 PM** Sheet2 of 8File: **ct_fpga_io.SchDoc**

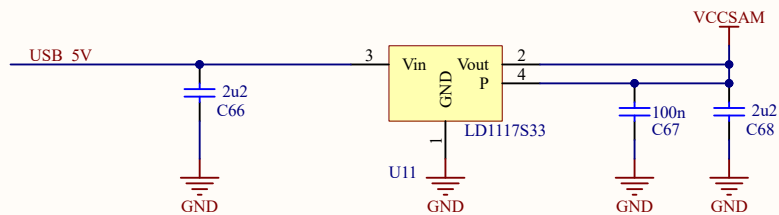
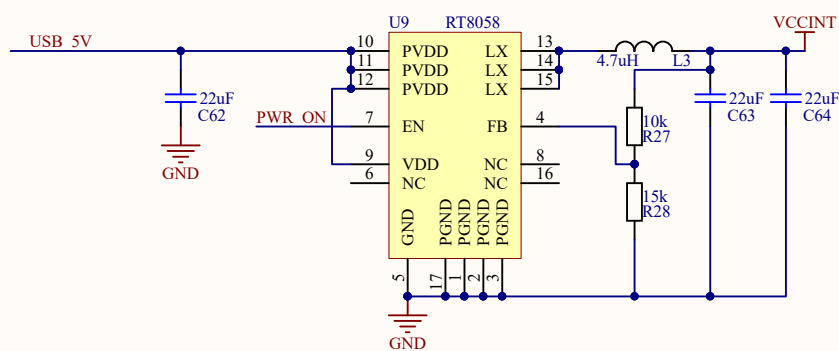
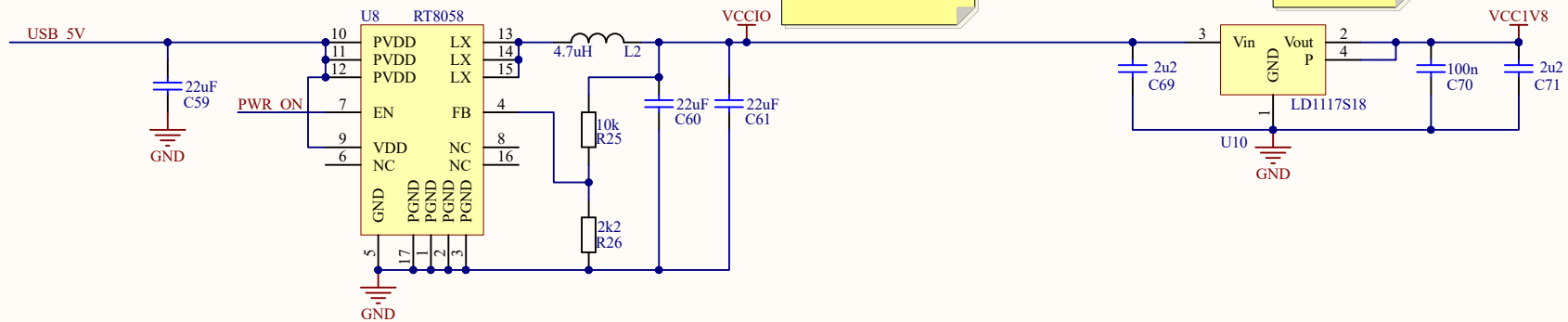
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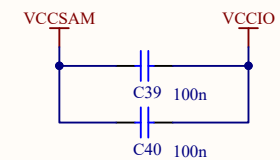
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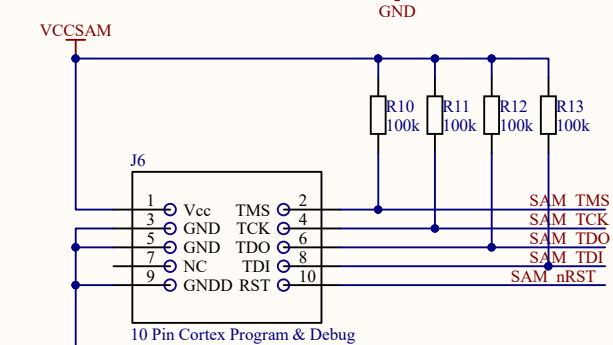
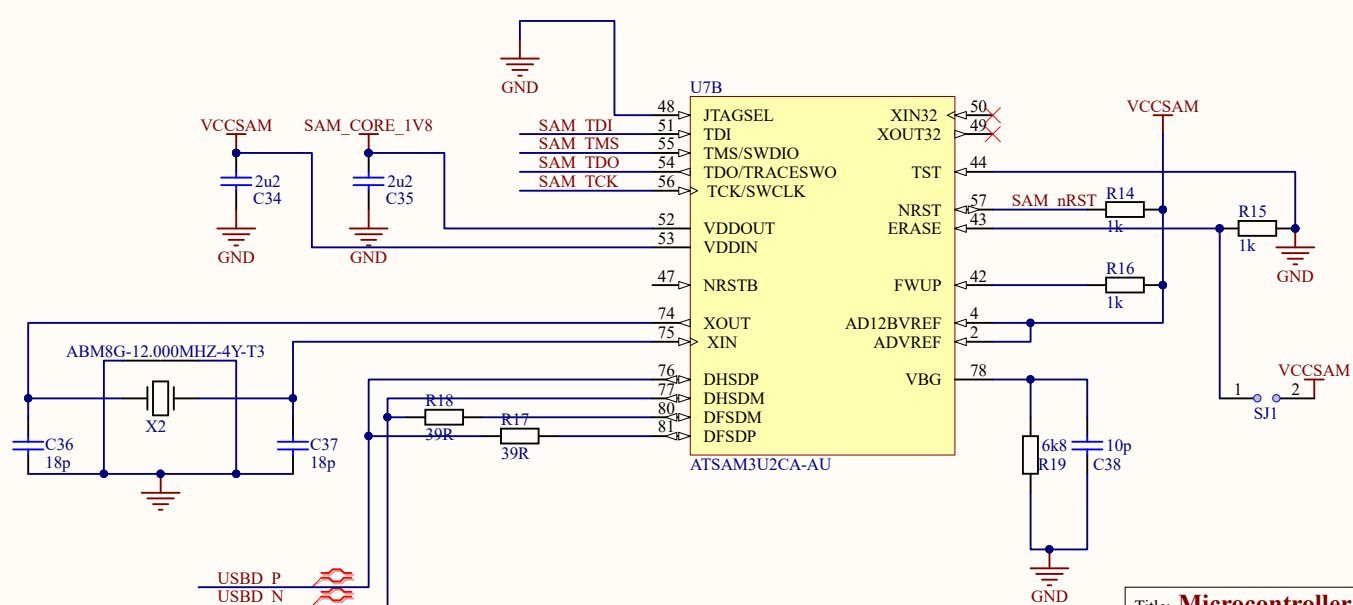
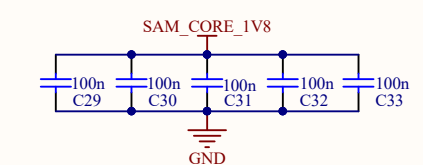
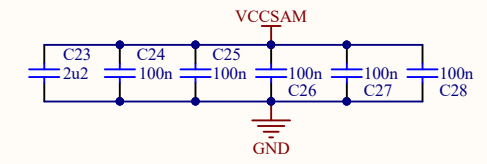
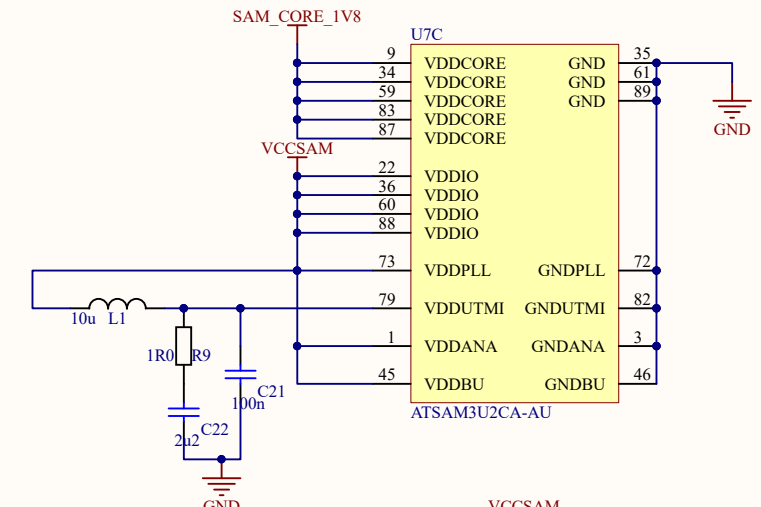
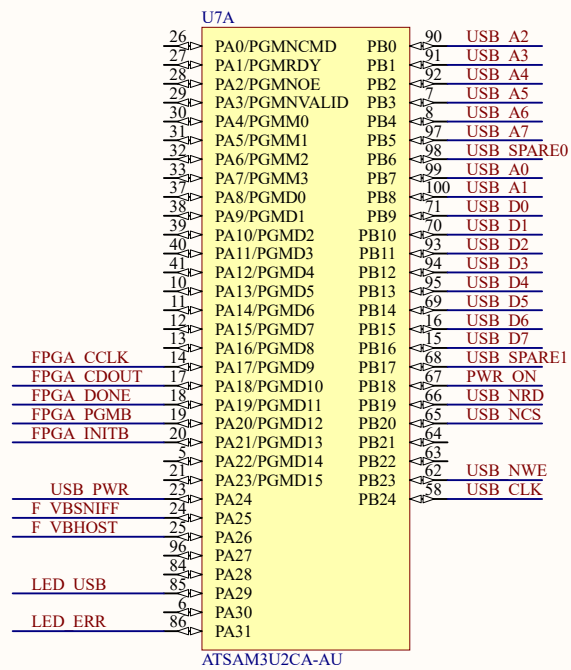


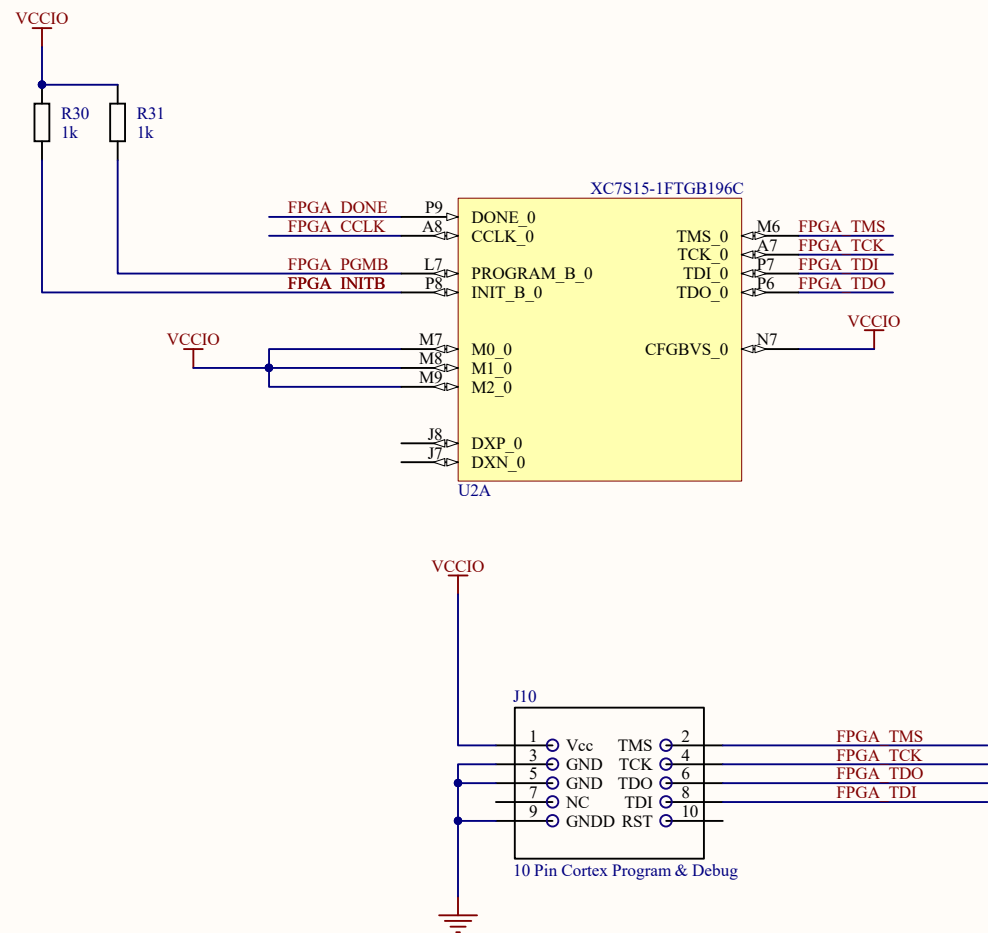




NOTE: The power domains for SAM3U and FPGA on 3.3V are different. Need caps when crossing planes, as high-speed signals are forced to somewhat cross this plane :(







A

A

B

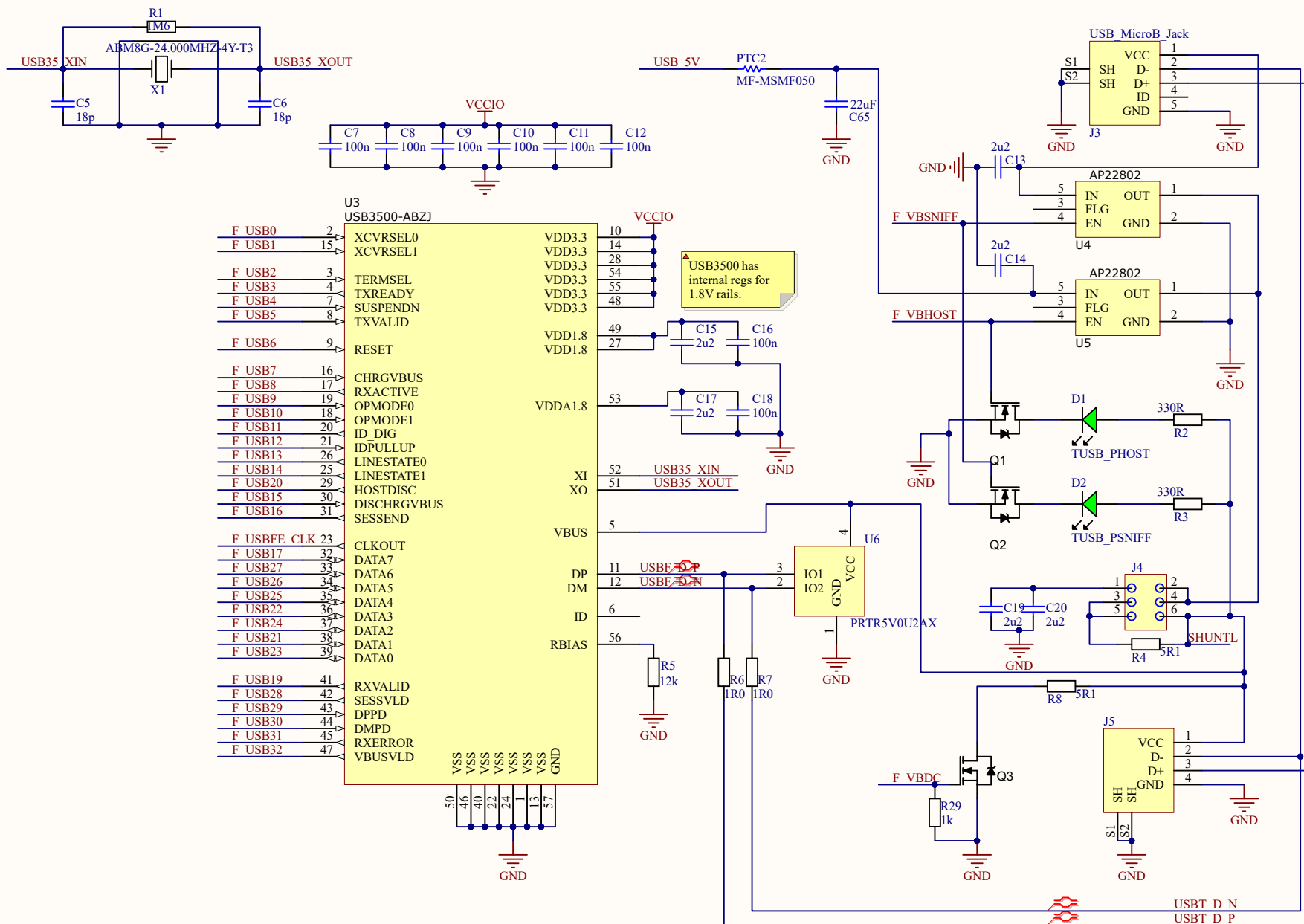
B

C

C

D

D



this will be a "stub" on USB routing, should be made as small as possible (i.e., route pairs in series as much as possible)

Keep USB impedance requirements!!

Title: **USB Interface**

Rev: **04**

Project: **PhyWhisperer-USB**

Date: **2019-11-11**

Time: **10:05:09 PM**

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File: **ct_frontend.SchDoc**

Approved: YES

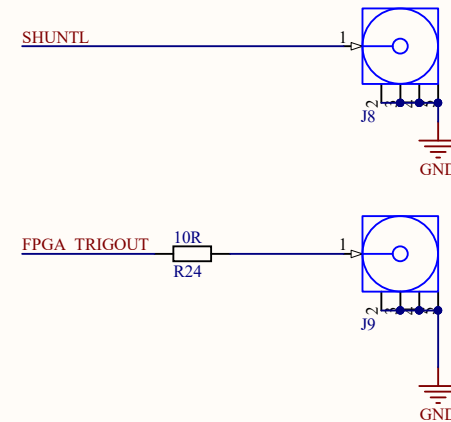
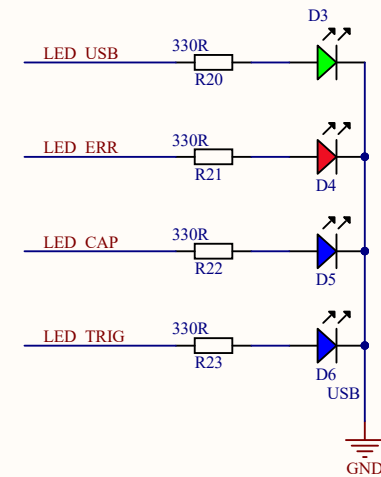
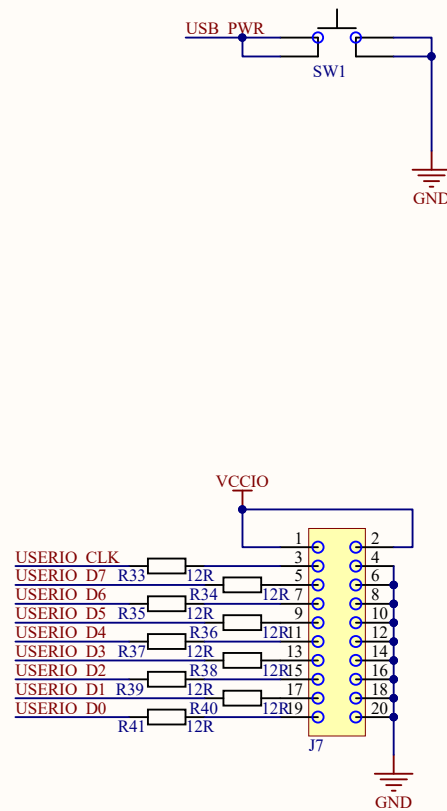
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Route to FPGA pins.
USERIO_CLK must go to
SRCC/MRCC pin, and _P pair.
Rest can go to any pins on same
bank as clock.



Title: **User I/O**

Rev: **04**

Project: **PhyWhisperer-USB**

Date: **2019-11-11** Time: **10:05:09 PM** Sheet **8** of **8**

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