

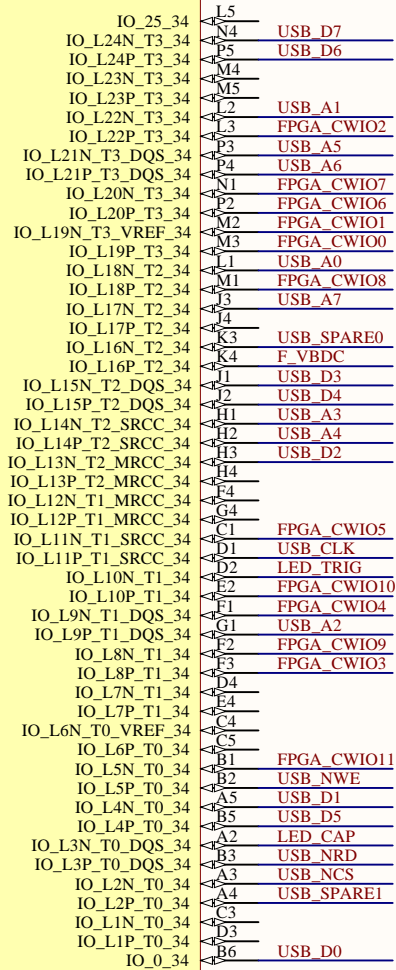


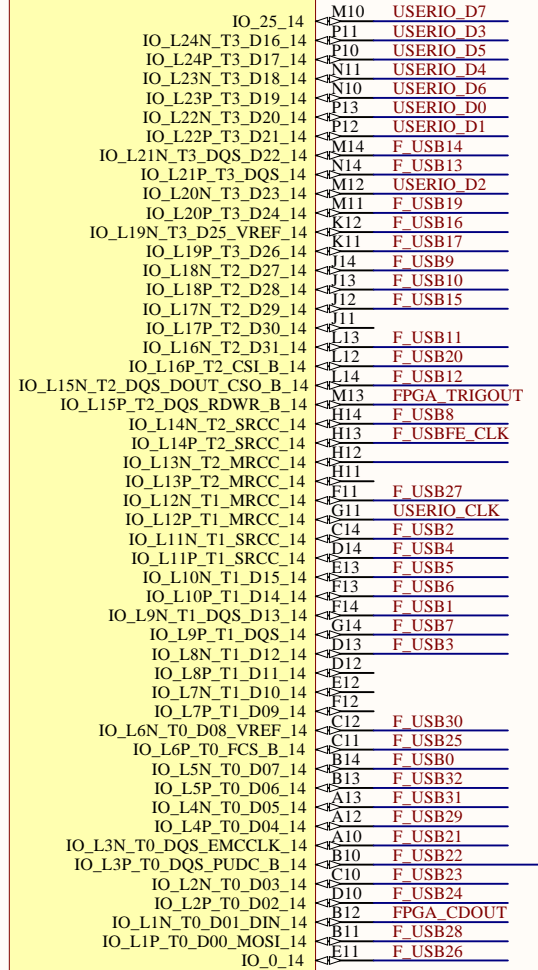
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Rev: 00	Project: <b>PhyWhisperer-USB</b>			License: GPL	
Date: 28/03/2019	Time: 9:42:57 PM	Sheet	of	Copyright © NewAE Technology Inc.	NewAE.com
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U2C

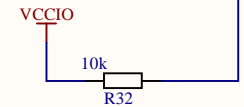


XC7S6-1FTGB196C

U2D



XC7S6-1FTGB196C

Title: **FPGA I/O**

Approved: NO



Rev: 00

Project: **PhyWhisperer-USB**

License: GPL

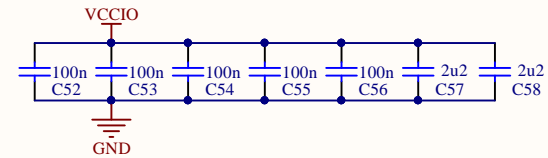
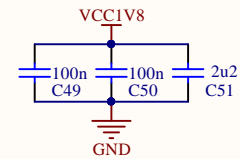
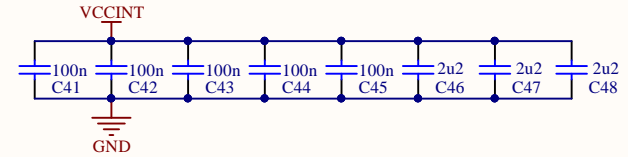
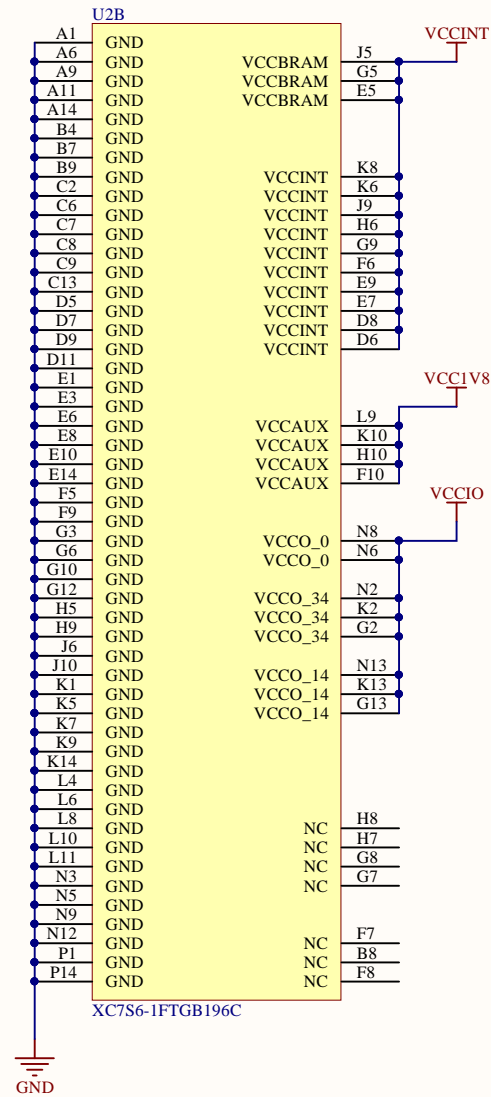
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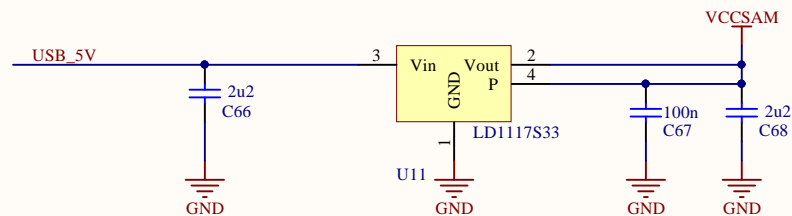
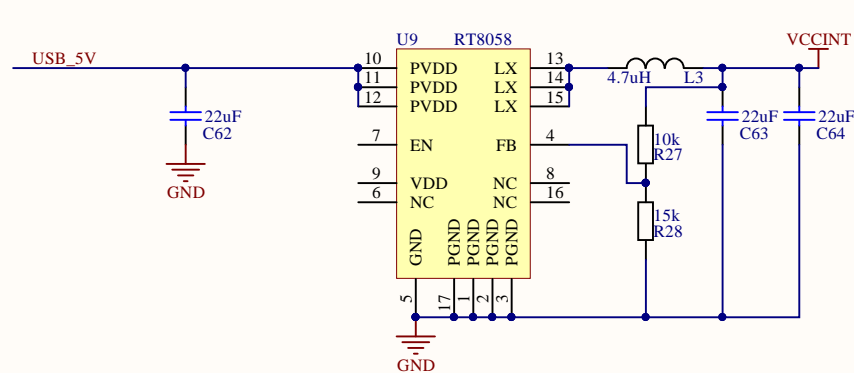
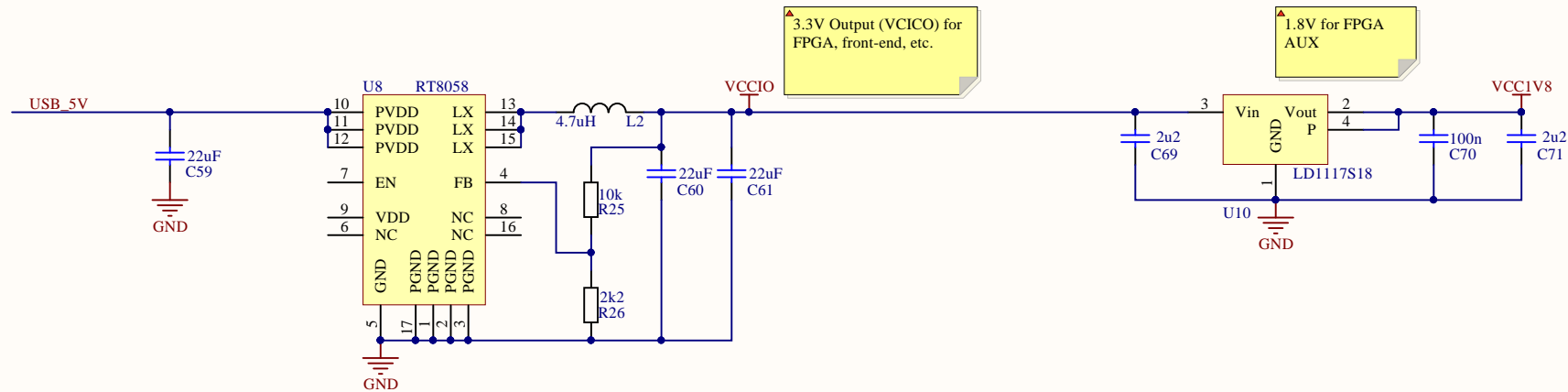
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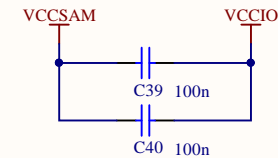
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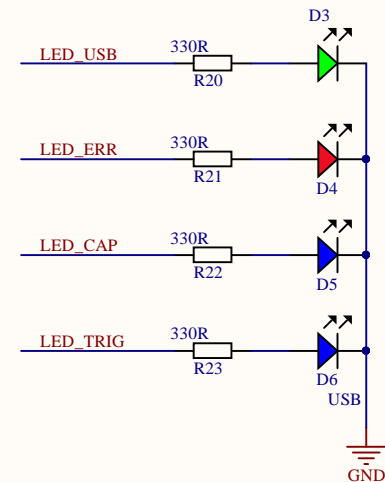
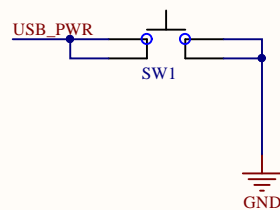




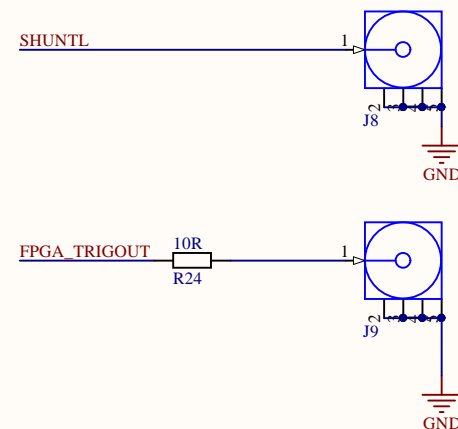
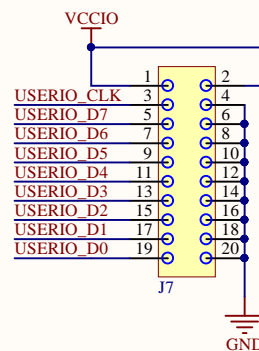
NOTE: The power domains for SAM3U and FPGA on 3.3V are different. Need caps when crossing planes, as high-speed signals are forced to somewhat cross this plane :( Probably need more caps...



Title: <b>Power Supply</b>			 Approved: NO		
Rev: 00	Project: <b>PhyWhisperer-USB</b>		License: GPL		
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Route to FPGA pins.  
USERIO\_CLK must go to  
SRCC/MRCC pin, and \_P pair.  
Rest can go to any pins on same  
bank as clock.



Title: **User I/O**

Approved: NO

Rev: 00

Project: **PhyWhisperer-USB**

License: GPL

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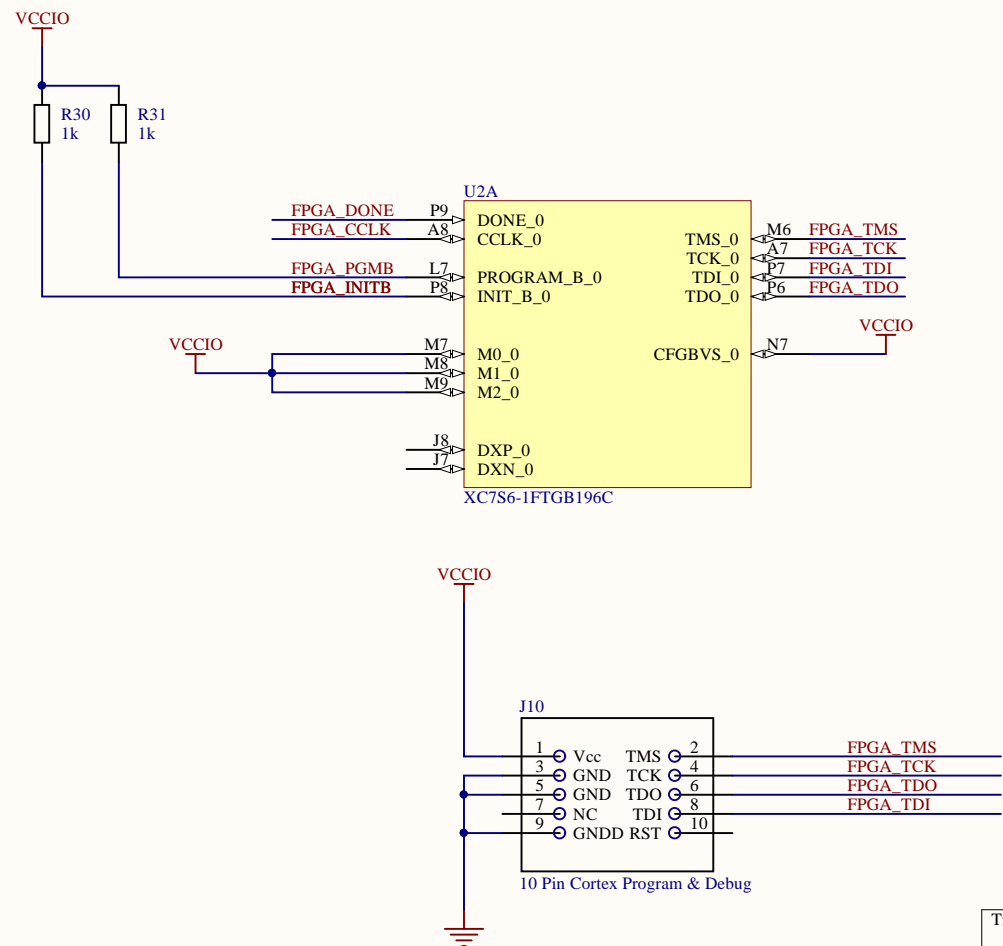
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Title		
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