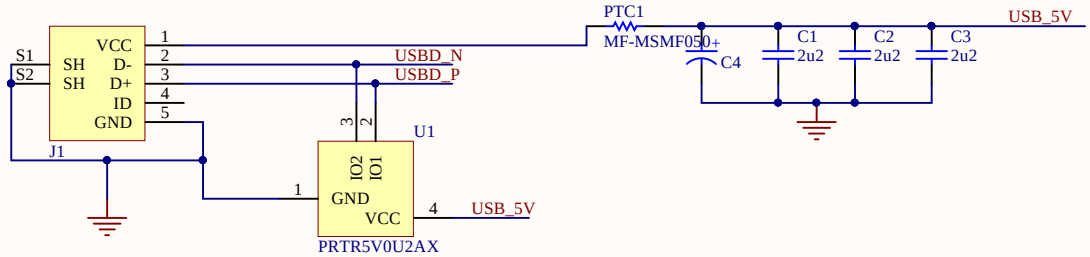

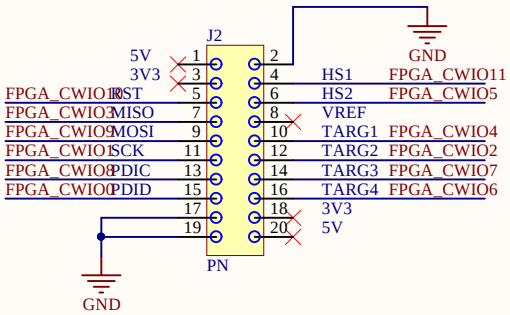

Title: **Back Panel**		Approved: NO	NewAE Technology
Rev: 02	Project: PhyWhisperer-USB	License: GPL	
Date: 28/05/2019	Time: 3:08:15 PM	Sheet of	Copyright © NewAE Technology Inc. NewAE.com
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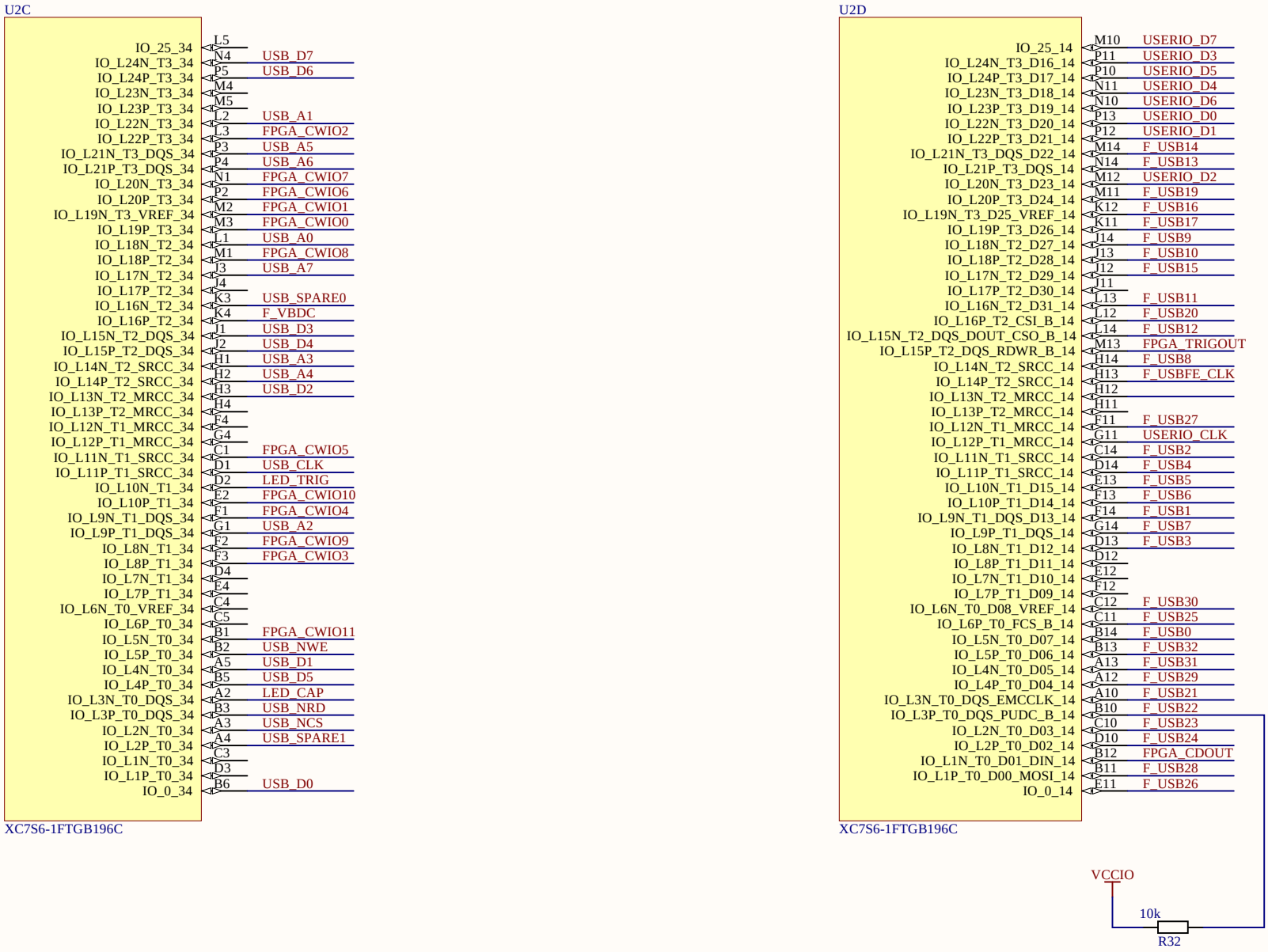

Title: **FPGA I/O**		Approved: NO	NewAE Technology
Rev: 02	Project: PhyWhisperer-USB	License: GPL	
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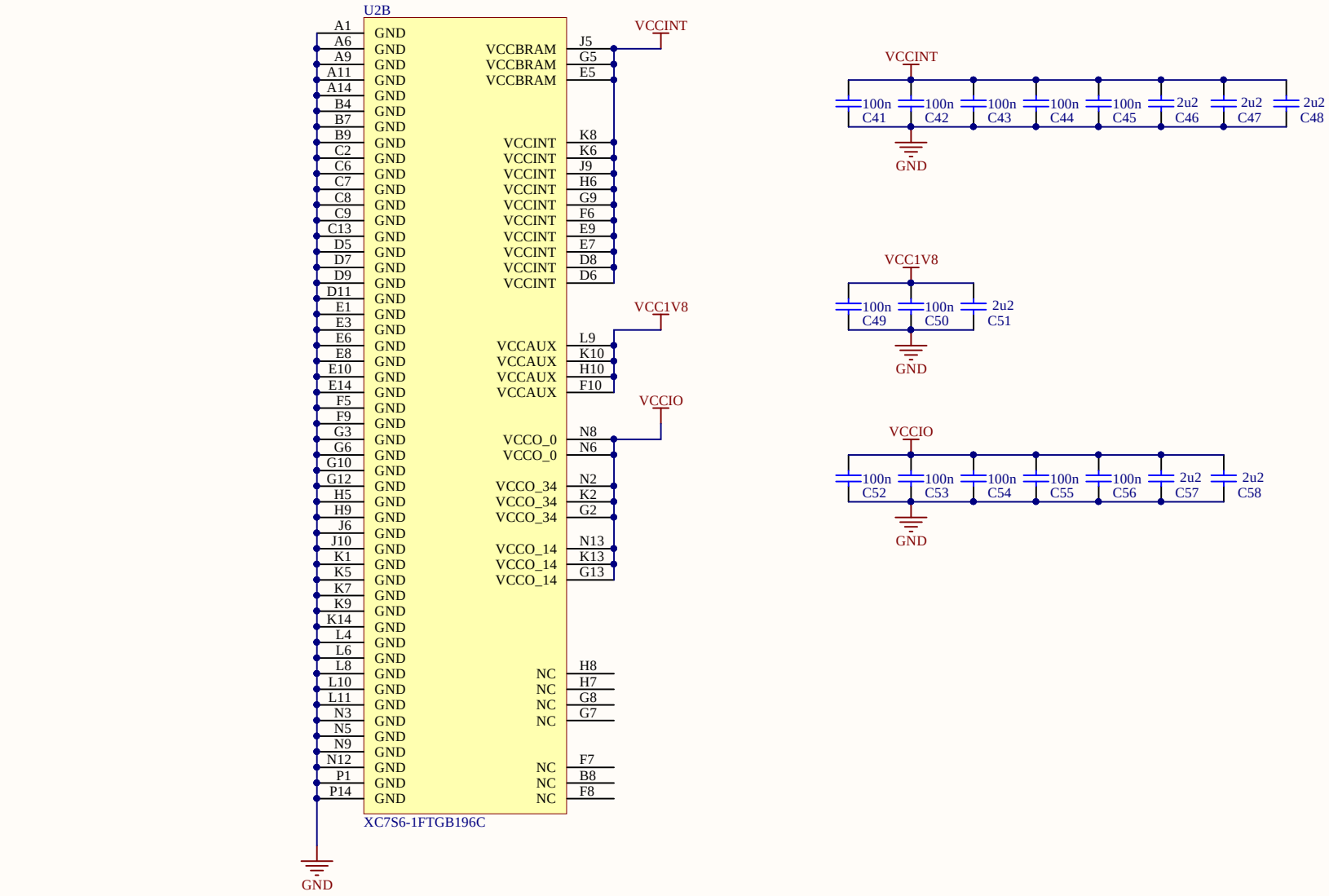

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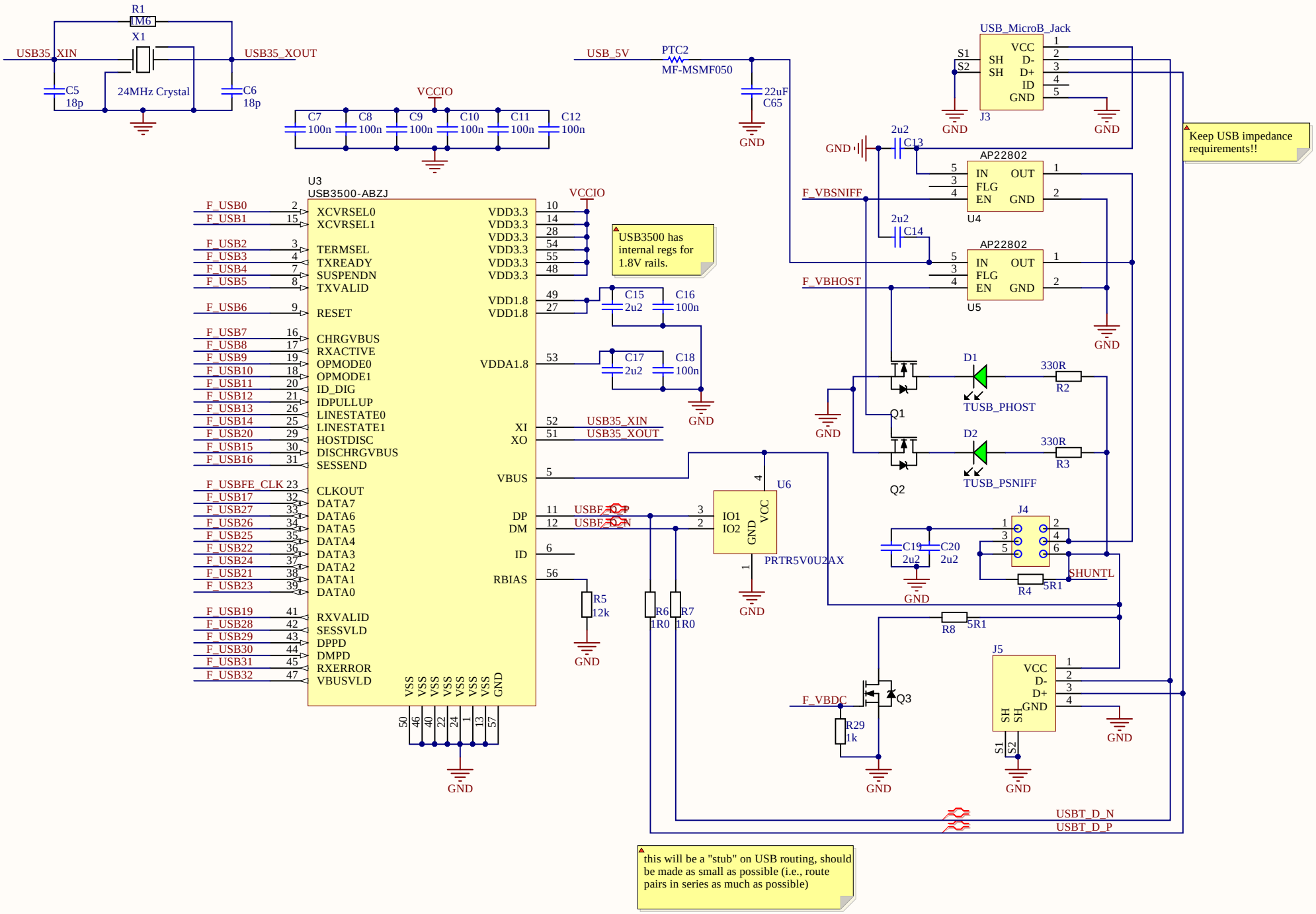

Title: **USB Interface**		Approved: NO	NewAE Technology
Rev: 02	Project: PhyWhisperer-USB	License: GPL	
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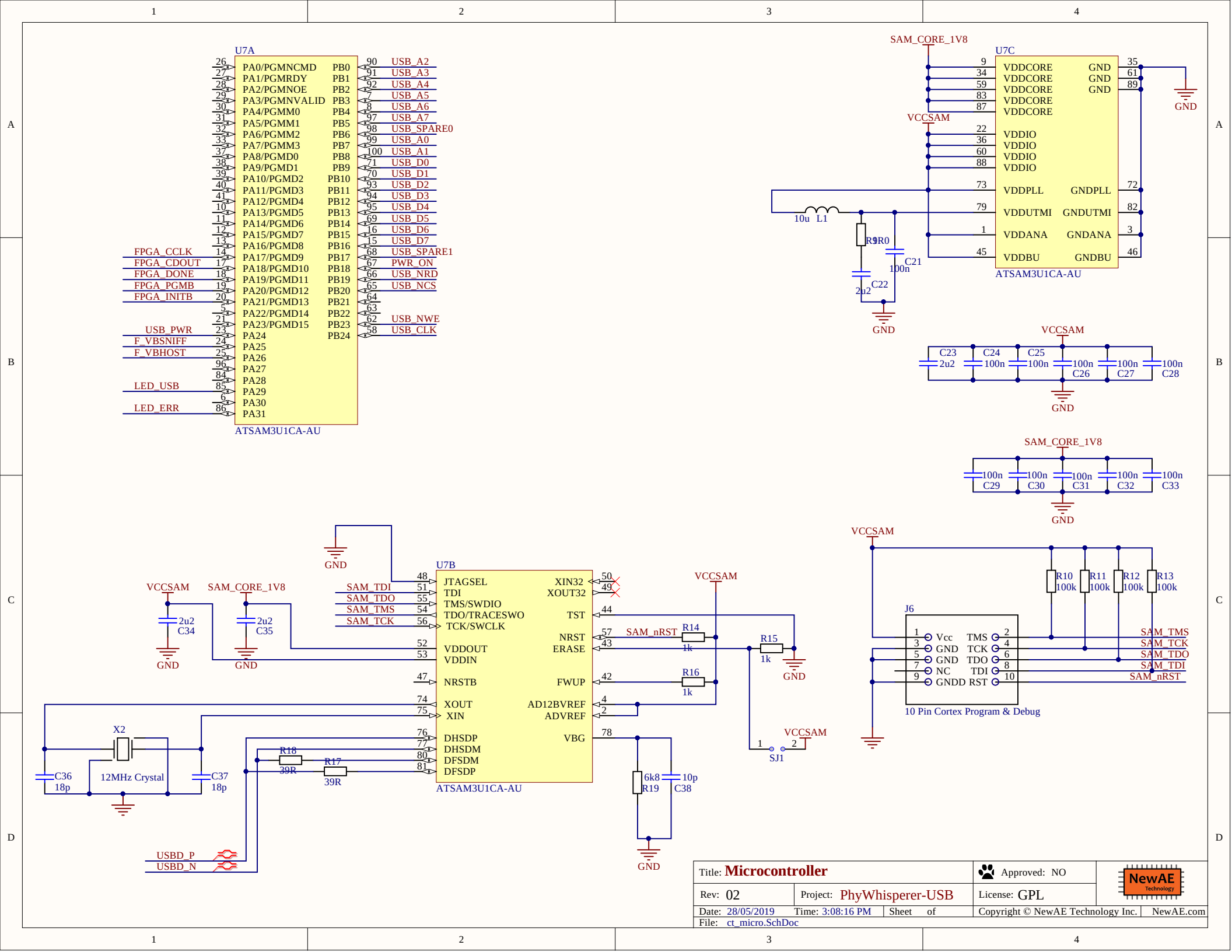
U7A
PA0/PGMNCMD PB0
PA1/PGMRDY PB1
PA2/PGMNOE PB2
PA3/PGMNVALID PB3
PA4/PGMM0 PB4
PA5/PGMM1 PB5
PA6/PGMM2 PB6
PA7/PGMM3 PB7
PA8/PGMD0 PB8
PA9/PGMD1 PB9
PA10/PGMD2 PB10
PA11/PGMD3 PB11
PA12/PGMD4 PB12
PA13/PGMD5 PB13
PA14/PGMD6 PB14
PA15/PGMD7 PB15
PA16/PGMD8 PB16
PA17/PGMD9 PB17
PA18/PGMD10 PB18
PA19/PGMD11 PB19
PA20/PGMD12 PB20
PA21/PGMD13 PB21
PA22/PGMD14 PB22
PA23/PGMD15 PB23
PA24 PB24
PA25
PA26
PA27
PA28
PA29
PA30
PA31
USB_A2
USB_A3
USB_A4
USB_A5
USB_A6
USB_A7
USB_SPARE0
USB_A0
USB_A1
USB_D0
USB_D1
USB_D2
USB_D3
USB_D4
USB_D5
USB_D6
USB_D7
USB_SPARE1
PWR_ON
USB_NRD
USB_NCS
USB_NWE
USB_CLK
FPGA_CCLK
FPGA_CDOUT
FPGA_DONE
FPGA_PGMB
FPGA_INITB
USB_PWR
F_VBSNIFF
F_VBHOST
LED_USB
LED_ERR
ATSAM3U1CA-AU
SAM_CORE_1V8
U7C
VDDCORE GND
VDDIO
VDDPLL GNDPLL
VDDUTMI GNDUTMI
VDDANA GNDANA
VDDBU GNDBU
VCCSAM
10u L1
R9 0R
C21 100n
C22 2u2
GND
C23 2u2
C24 100n
C25 100n
C26 100n
C27 100n
C28 100n
U7B
JTAGSEL
TDI
TMS/SWDIO
TDO/TRACESWO
TCK/SWCLK
VDDOUT
VDDIN
NRSTB
XOUT
XIN
DHSDP
DHSDM
DFSDP
DFSDM
XIN32
XOUT32
TST
NRST
ERASE
FWUP
AD12BVREF
ADVREF
VBG
SAM_TDI
SAM_TDO
SAM_TMS
SAM_TCK
SAM_nRST
R14 1k
R15 1k
R16 1k
SJ1
C34 2u2
C35 2u2
X2
12MHz Crystal
C36 18p
C37 18p
R18 39R
R17 39R
USBD_P
USBD_N
6k8 R19
10p C38
C29 100n
C30 100n
C31 100n
C32 100n
C33 100n
R10 100k
R11 100k
R12 100k
R13 100k
J6
Vcc TMS
GND TCK
GND TDO
NC TDI
GNDD RST
10 Pin Cortex Program & Debug
Title: Microcontroller
Approved: NO
Rev: 02
Project: PhyWhisperer-USB
License: GPL
Date: 28/05/2019
Time: 3:08:16 PM
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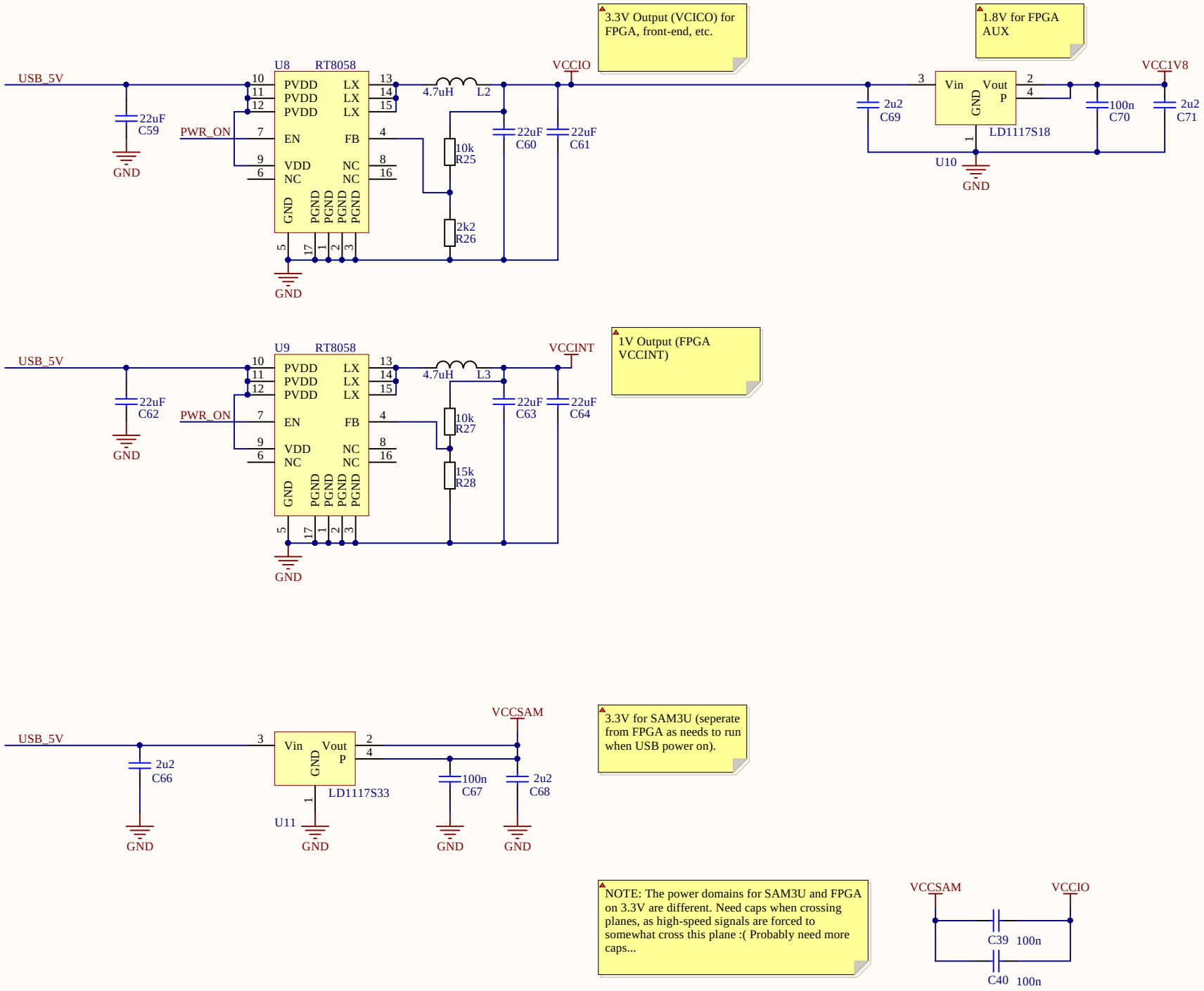

Title: **Power Supply**		Approved: NO	NewAE Technology
Rev: 02	Project: PhyWhisperer-USB	License: GPL	
Date: 28/05/2019	Time: 3:08:16 PM	Sheet of	Copyright © NewAE Technology Inc. NewAE.com
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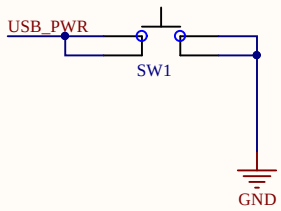
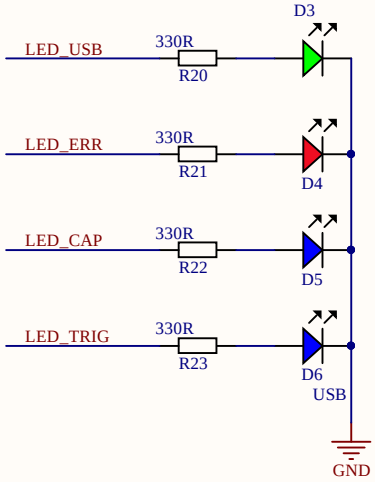
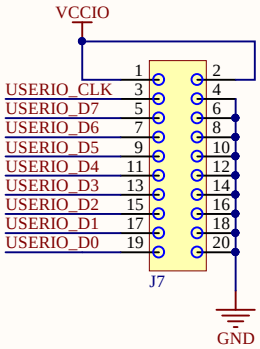
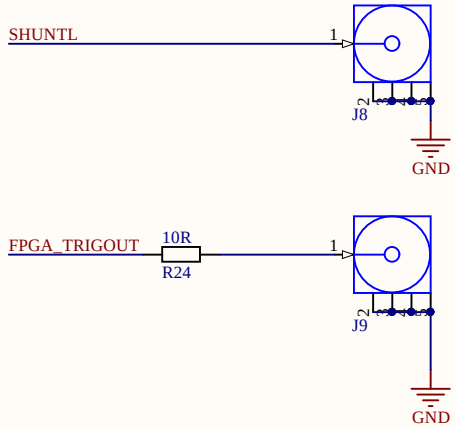




Route to FPGA pins.
USERIO_CLK must go to SRCC/MRCC pin, and _P pair.
Rest can go to any pins on same bank as clock.





Title: **User I/O**		Approved: NO	NewAE Technology
Rev: 02	Project: PhyWhisperer-USB	License: GPL	
Date: 28/05/2019	Time: 3:08:16 PM Sheet of	Copyright © NewAE Technology Inc.	NewAE.com
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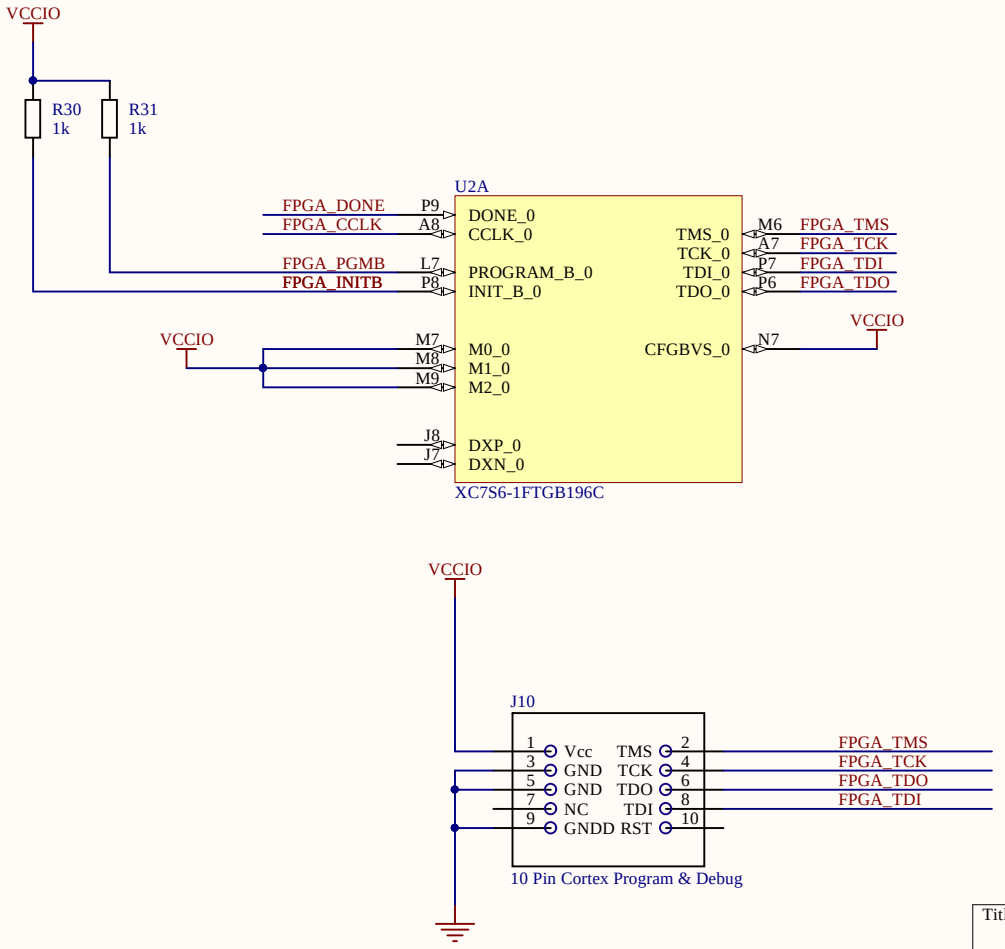

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