MYC-Y6ULX-V2
Hardware Design Guide

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History

Version	Author	Participants	Date	Description
V1.0	Leoric		20211221	The version is updated to V2
V1.1	Dana		20230523	Updated some content of RTC

Contents

1. Overview

This document is intended to assist hardware engineers in designing board-level circuits based on the MYC-Y6ULX-V2 core module. Please be fully aware of the document before you begin your design.The document contains common information such as design references, layout suggestions, and design checklists to assist hardware engineers.

Resources referenced in this document is from the Myirtech website, included in the MYC Y6ULX-V2 product information download page, you can download them in the following website: http://down.myir-tech.com/MYD-Y6ULX-V2.

In addition, Myirtech offers the following resources to speed up your design:

◆ core module/Evaluation Board Product Manual;

◆ Evaluation board schematic source file;

◆ Related device datasheet.

1.1. Supported products

This document applies to all models of the MYC-Y6ULX-V2 family of core modules.

1.2. Disclaimer

◆ Some of Reference designs in the document are based on mill electronic evaluation boards and cannot be guaranteed to be suitable for all application scenarios. If your product has special requirements for application scenarios or technical specifications, please adjust the design according to the actual situation.

◆ Reference design and Layout in the document are recommended for reference only and do not necessarily contain all the matters needing attention. Please make adjustments according to the actual situation.

◆ Mill Electronics shall not be liable for any form of technical endorsement or joint liability for any proposal contained in any document.

2. Power supply design

The design of the power supply system is of vital importance in the design of embedded products, engineers need to consider not only the basic electrical parameters of power itself, but also the stability of the power supply design, such as electromagnetic compatibility, temperature range, safety design, etc. Any neglect of these factors may lead to the entire system cannot work normally. Before starting to design a power supply system for a new product, the engineer should thoroughly understand the actual needs of the whole system, and comprehensively demonstrate a feasible design scheme based on cost and efficiency, so as to select an appropriate power supply method for the system.

2.1. Reference design

The core module needs to be provided 3.3V voltage for normal running, the average current in full load mode is about 285mA, while the peak current will reach 360mA. Considering that the power consumption of the product is relatively larger during start-up procedure and the performance of the circuit itself will be reduced under high temperature conditions, if the power supply is not enough, the system can not start normally. Therefore, the power supply design should have a enough margin to ensure the stability and reliability. It is recommended to use more than 1 A power chip to supply the core module separately. It is not recommended to use this power chip to drive the load outside the core module, especially some high-power load devices.

The power chip can be LDO or DCDC. LDO has the advantages of simple use, low cost and small electromagnetic interference, but high calorific value.DCDC has the advantages of strong current output capability, high conversion efficiency and low calorific value, but large electromagnetic interference.If the input voltage is close to 3.3V, LDO power chip can be used; if the input voltage is far from 3.3V, DCDC power chip is recommended.

The evaluation board uses LDO chip, because the input voltage of 5V is close to 3.3V, the model is RT9018A-18GSP, and the maximum output current is 3A.In order to ensure the accuracy of the output voltage, R6 and R9 are recommended to use more than 1% accuracy.
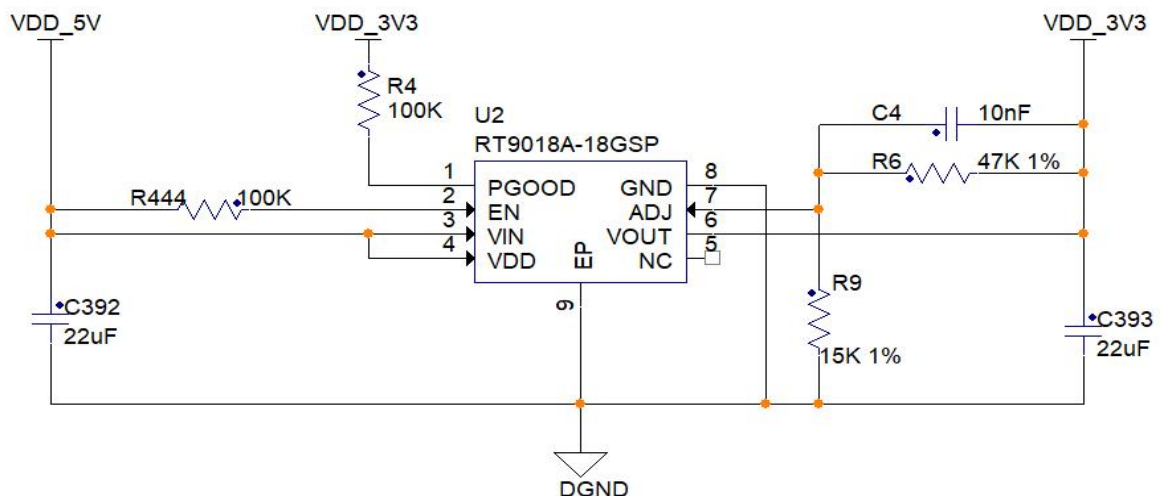
Figure 2-1 core module 3.3V power supply circuit

2.2. Power protection

In order to ensure the reliability of the power supply system, it is not recommended to directly supply the external untreated input voltage to the input end of LDO. Please refer to the protection circuit below to process the power supply before using it, so as to improve the reliability and safety of the input power supply and reduce electromagnetic interference.The carrier board input power in the reference design is 12V, as an example only, the value of the input power should be determined according to your actual needs.
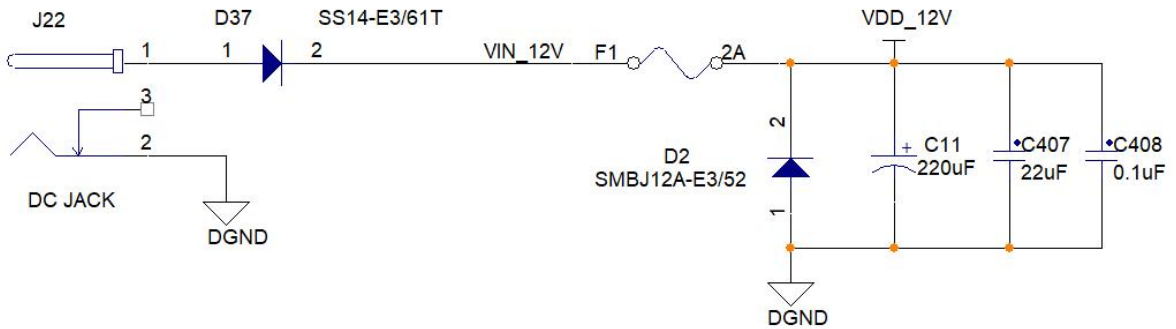
Figure 2-2 General power input circuit
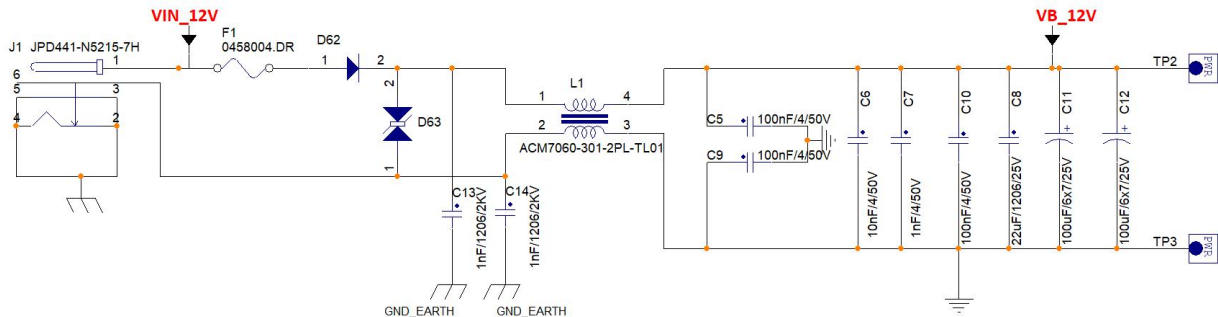
Figure. 2-3 Power input circuit for noise sensitive situations

2.3. Power sequence

Only in this way can the reliability of the chip be ensured. In the design, it is suggested that MYC-Y6ULX-V2 core module should be powered on first, whereafter the I/O equipment of the carrier board peripheral should be powered on. Failure to meet the power sequence may lead to the following situation:

♦ carrier board peripheral I/O current is poured back to the processor, results in start fail or even irreversible damage to the processor (worst case);

It is strongly recommended that VDD_3V3 be powered before other peripherals on the carrier board.

2.4. Layout guidelines

◆ The distance between different power supply planes should be at least 20mil;

◆ Widen the width of the power line and ground wire as far as possible, to meet the required rated current value, the width of the feedback signal should not be too narrow, it is recommended to be more than 10mil;

◆ If DCDC is used, the signal line is not recommended in the area below the inductance;

◆ If DCDC is used, the current loop path should be as short as possible, and the inductor and capacitor should be placed as close to the chip as possible, i.e. the red and green paths in the figure below
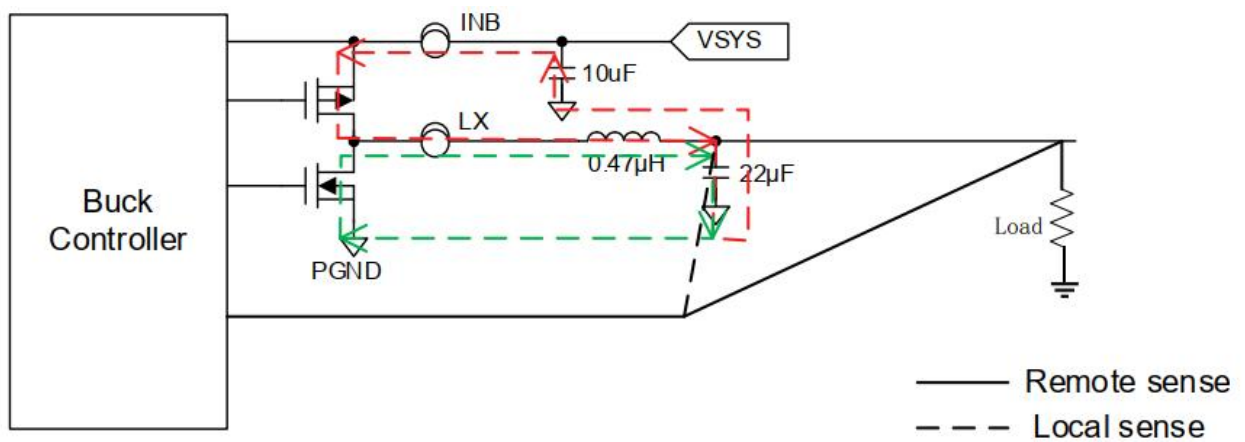
Figure 2-4 DCDC current backflow path

◆ If LDO is used, it is necessary to pay attention to the thermal resistance of the LDO chip, because the thermal resistance of the LDO chip is relatively high. It is recommended to add the grounding pad and make more ground vias on the grounding pad.

◆ Choose the capacitance of small ESR as far as possible

◆ The power chip with digital ground and analog ground shall be separated from each other and only connected at a single point at the input of the main power supply. The analog ground shall not be connected to the grounding pad.

3. Boot configuration design

After power-on reset, i.MX.6UL/6ULL chip first runs the built-in program in ROM, which detects the configuration of BOOT MODE pin to determine the boot mode, and then detects the configuration of CFGx[7:0] pin to select and configure the boot device.

Since these configuration pins have been configured on the core module, they do not need to be used in the design of the carrier board, only a few of the key pins need to be configured, which can be configured in the way of toggle switch. Depending on the selected core module storage device, the pins needed to be configured are also different, please refer to the reference design for details.

For more details on the boot configuration, go to the NXP website i.MX.6UL/6ULL product page and download Reference Manual:

https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors/i-mx-6ull-single-core-processor-with-arm-cortex-a7-core:i.MX6ULL? TAB = Documentation_Tab.

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

Table 3-1 Boot Mode configuration

BOOT_CFG1[7:4]	Boot device
0000	NOR/OneNAND (EIM)
0001	QSPI
0011	Serial ROM (SPI)
010x	SD/eSD/SDXC
011x	MMC/eMMC
1xxx	Raw NAND

Table 3-2 Configuration of Boot Device

3.1. Reference design

3.1.1. Nand version core module
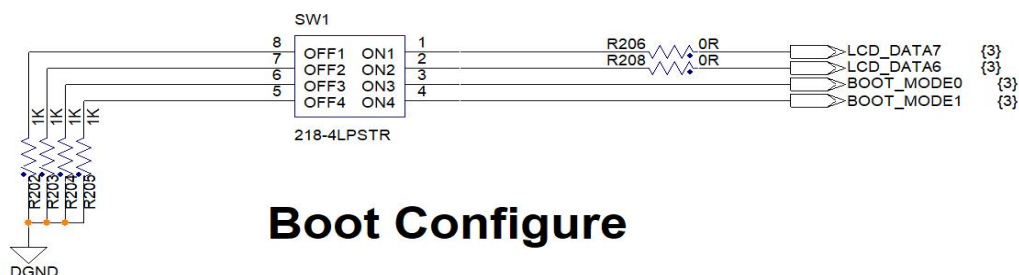
Figure 3-1 Configuration circuit

Pin	Signal Name	Configuration Bit	Default Function	Voltage Domain	Note
94	LCD_DATA7	BCFG1[7]	LCD data signal 7	VDD_3V3	Integrated with 10K pull-up resistor on core module
93	LCD_DATA6	BCFG1[6]	LCD data signal 6	VDD_3V3	Integrated with 10K pull-up resistor on core module
4	BOOT_MODE0	BOOT_MODE0	BOOT_MODE0	VDD_3V3	Integrated with 10K pull-up resistor on core module
5	BOOT_MODE1	BOOT_MODE1	BOOT_MODE1	VDD_3V3	Integrated with 10K pull-up resistor on core module

Table 3-3 Configuration pins

Boot Device	Switch Bit 1	Switch Bit 2
SD Card	ON	OFF
NandFlash	OFF	ON

Table 3-4 Toggle switch configuration 1

Boot mode	Switch Bit 3	Switch Bit 4
Boot From Fuses	ON	ON
Serial Download	OFF	ON
Internal Boot	ON	OFF
Reserved	OFF	OFF

Table 3-5 Toggle switch configuration 2

3.1.2. EMMC version core module

Figure 3-2 Configuration circuit

Pin	Signal Name	Configuration Bit	Default Function	Voltage Domain	Note
94	LCD_DATA5	BCFG1[5]	LCD data signal 5	VDD_3V3	Integrated with 10K pull-up resistor on core module
93	LCD_DATA11	BCFG2[3]	LCD data signal 11	VDD_3V3	Integrated with 10K pull-up resistor on core module
4	BOOT_MODE0	BOOT_MODE0	BOOT_MODE0	VDD_3V3	Integrated with 10K pull-up resistor on core module
5	BOOT_MODE1	BOOT_MODE1	BOOT_MODE1	VDD_3V3	Integrated with 10K pull-up resistor on core module

Table 3-6 Configuration pins

Boot Device	Switch Bit 1	Switch Bit 2
SD Card	ON	ON
NandFlash	OFF	OFF

Table 3-7 Toggle switch configuration 1

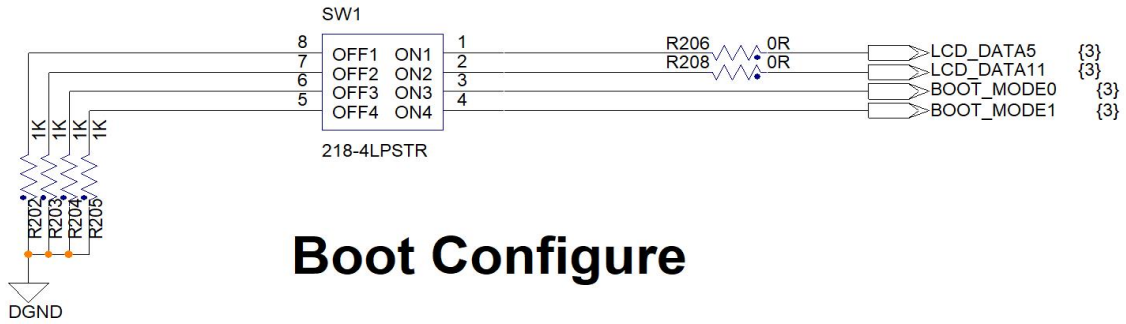| Boot mode	Switch Bit 3	Switch Bit 4
Boot From Fuses	ON	ON
Serial Download	OFF	ON
Internal Boot	ON	OFF
Reserved	OFF	OFF

Table 3-8 Toggle switch configuration 2

4. Reset and key circuit design

MYC-Y6ULX-V2 core module provides two dedicated reset pins, namely POR reset and ONOFF reset, which have different functions. It is recommended to connect them for different purposes.An additional pin is reserved in reference design as a user-defined key. The resistance and capacitance in reference design constitute a simple RC filter to eliminate the jitter interference when the key is pressed, and avoid the interference from the key to affect the reset signal. In the harsh electromagnetic environment, an ESD device can be connected in parallel in order to eliminate the electrostatic interference from the key and ensure the reliability of the system. If there are more stringent requirements for vibration, a logical circuit such as RS flip-flop can be considered to build a reset circuit.

POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.

Figure 4-1 Reset signal description

4.1. Reference design
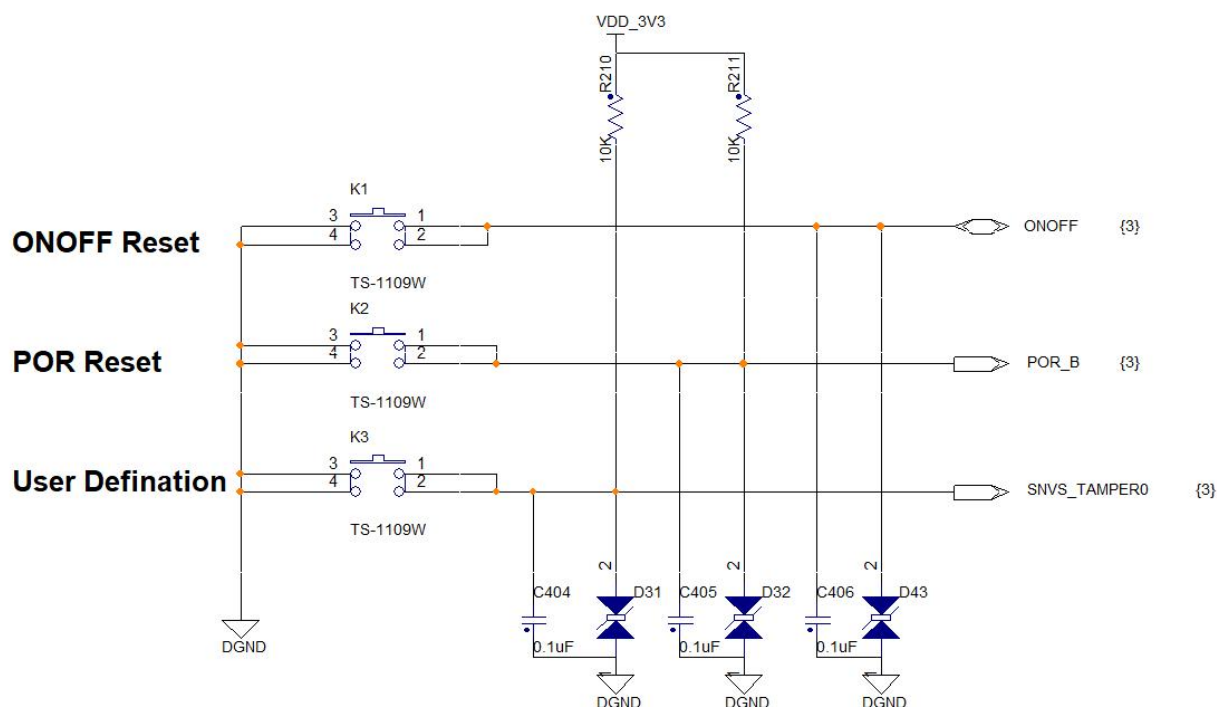
Figure 4-2 reset Reference design

4.2. Layout guidelines

♦ The width of reset signal line should not be too narrow, it is recommended not less than 8mil;

♦ Reset signal is sensitive signal, which is recommended to be surrounded by ground;

♦ Place TVS as close to the button as possible.

5. Interface circuit design

5.1. uSDHC interface

The Ultra Secured Digital Host Controller (uSDHC) is NXP's proprietary interface that provides secure communication between the CPU and external SD/SDIO//MMC card.MYC-Y6ULX-V2 core module is equipped with 2 channels of uSDHC interface, which can be used as SD card startup or SDIO communication. uSDHC2 can be only used on the nand version core module, on the eMMC version core module, uSDHC2 can not be used.

When designing the SD/SDIO/MMC card interface circuit, connect these interfaces to the SD/MMC card slot accordingly.
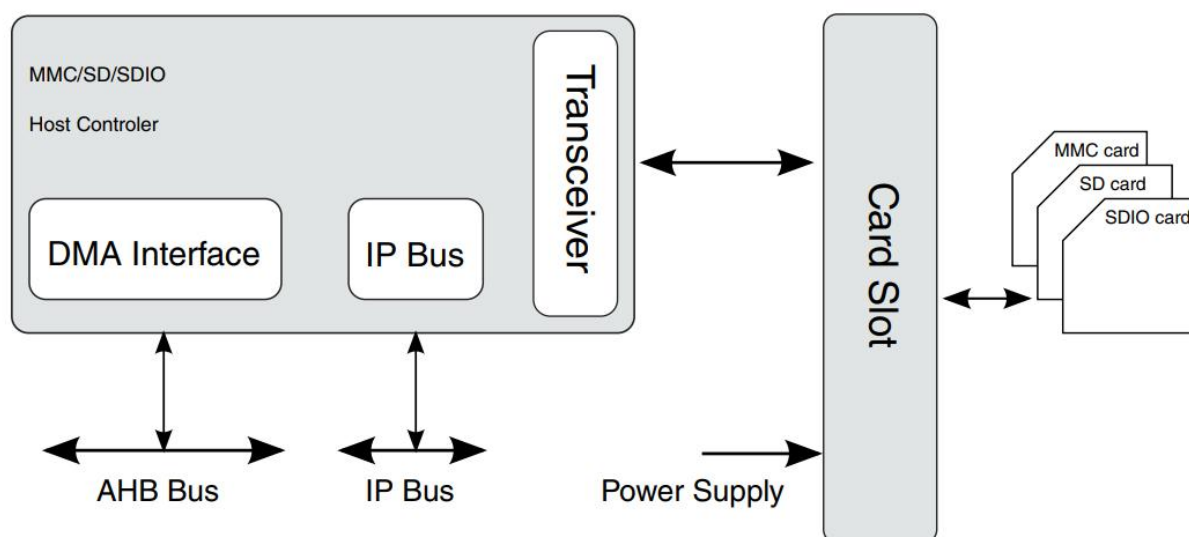
Figure 5-1 uSDHC interface

5.1.1. Reference design

Figure 5-2 SD card Reference design

5.1.2. Layout guidelines

♦ Single-ended signal 50 Ω impedance;

♦ Trace match the data line and control line to be within 100 mils;

♦ SD1_CLK is recommended to be surrounded with ground. If not, ensure the distance between the clock signal and other signals follow 3W rule.

5.2. UART interface

The MYC-Y6ULX-V2 core module offers up to 8 UART interfaces. Due to the chip pin multiplexing , the core module only uses 5 ports of them by default, among which UART3 has flow control (RTS and CTS signal) function, and the other 4 UARTS only has TXD and RXD signals by default.

In reference design, UART signals can be used in the following ways: UART to RS232, UART to RS485, and directly connected to pin header for debugging. Considering the harsh environment of industrial application, the circuit of UART to RS232 and UART to RS485 uses isolated method.

When using UART directly as debug port, since UART is TTL port with 3.3V voltage level, it needs to be combined with a UART to USB adapter for direct connection with PC. You can choose Myirtech`s adapter accessory MY-UART012U. Visit http://www.myir-tech.com/product/my_uart012U.htm to get detailed information.
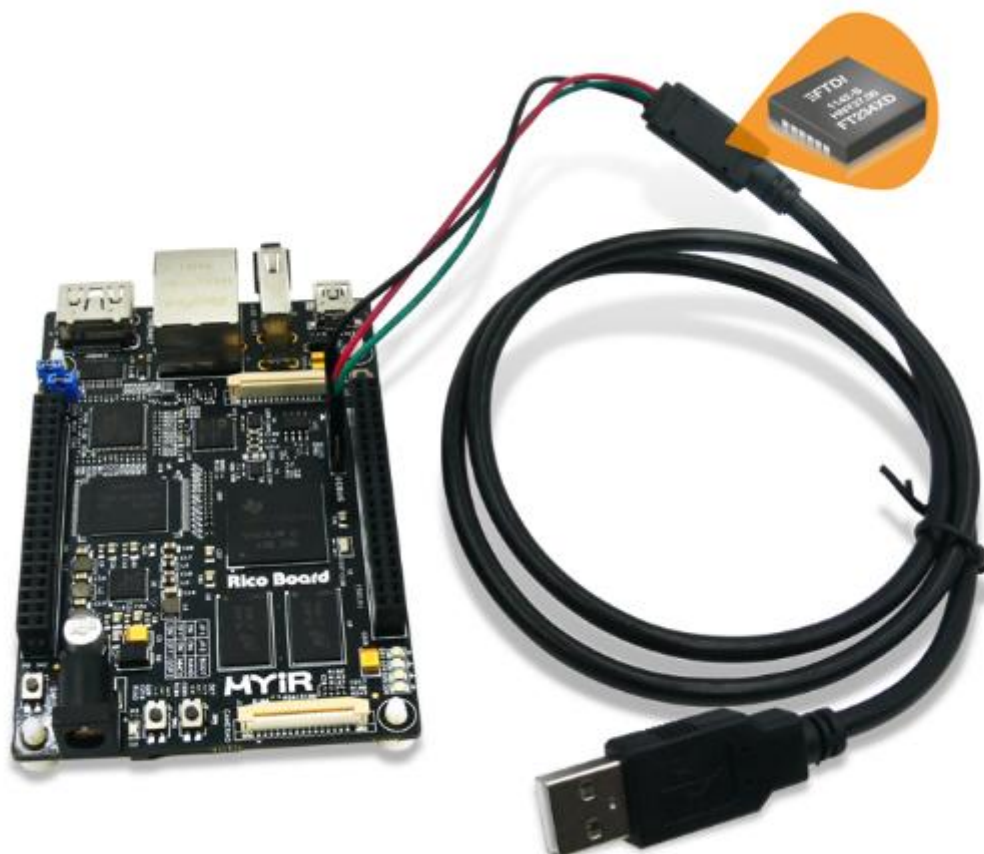
Figure 5-3 MY-UART012U Adapter

5.2.1. RS-232 Transceiver

Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. In reference design, SP3232EY-L converter chip from EXAR is used for convert TTL to ±5V EIA/TIA-232 levels, while chip ADUM1201BRZ from ADI is used for signal isolation. The converted signals RS232_TX/RX then can be directly connected to the RS232 connector.

The 5V_ISO is produced by a special isolated power supply chip, and in the reference design the isolated power chip B0505S-1WR2 from Mornsun is selected. Note that this power chip has a minimum load requirement, which requires a 10K resistance (R389) as the default load.
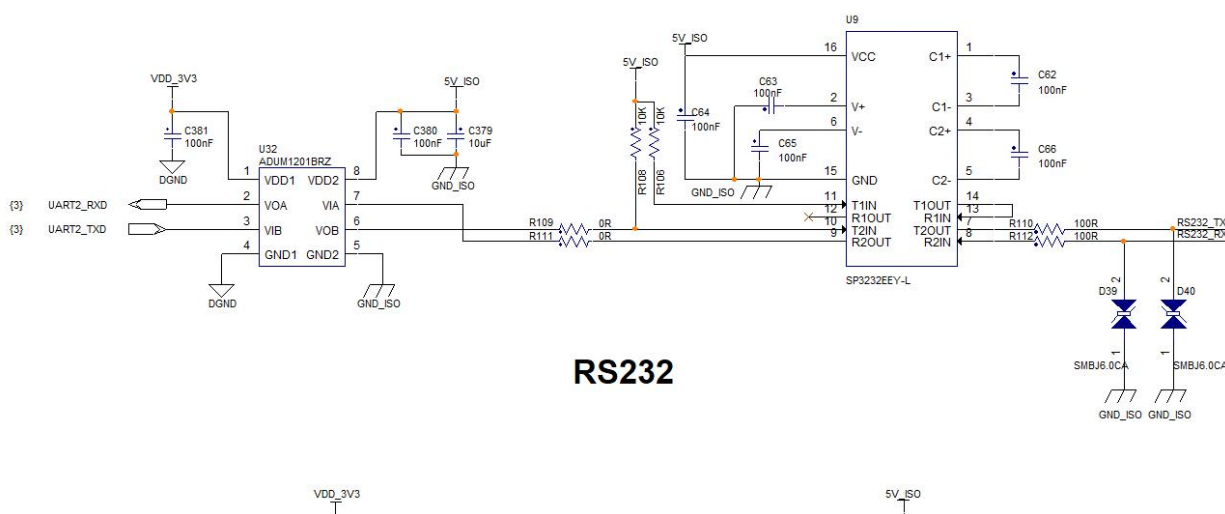
Figure 5-4 Isolated RS232 reference design
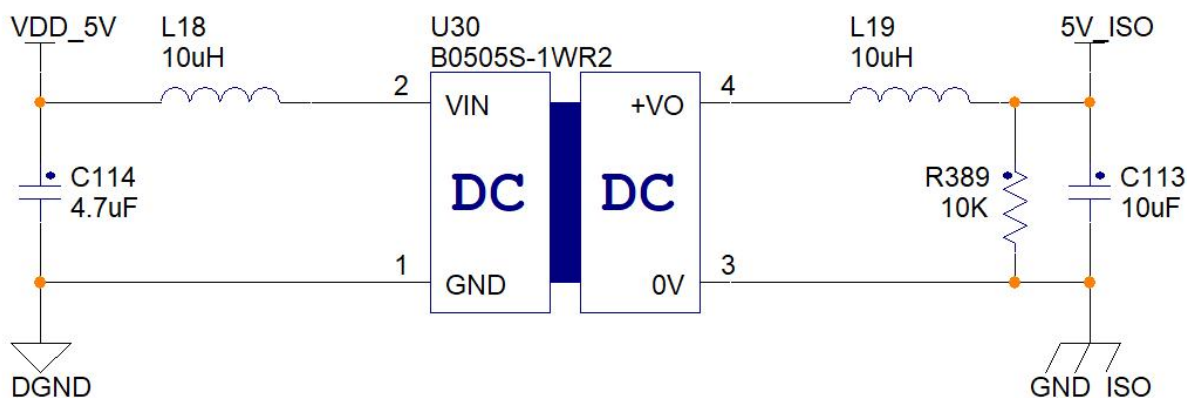
Figure 5-5 Isolated 5V power reference design

5.2.2. RS-485 Transceiver

In reference design, we use ISO3802DW isolation converter chip from TI, which integrates the signal isolation function and does not need to add additional signal isolation chip.The converted RS485_A/B can be directly connected to the RS485 connector.

The 5V_ISO is produced by a special isolated power supply chip, and in the reference design the isolated power chip B0505S-1WR2 from Mornsun is selected. Note that this power chip has a minimum load requirement, which requires a 10K resistance (R389) as the default load.

RS485
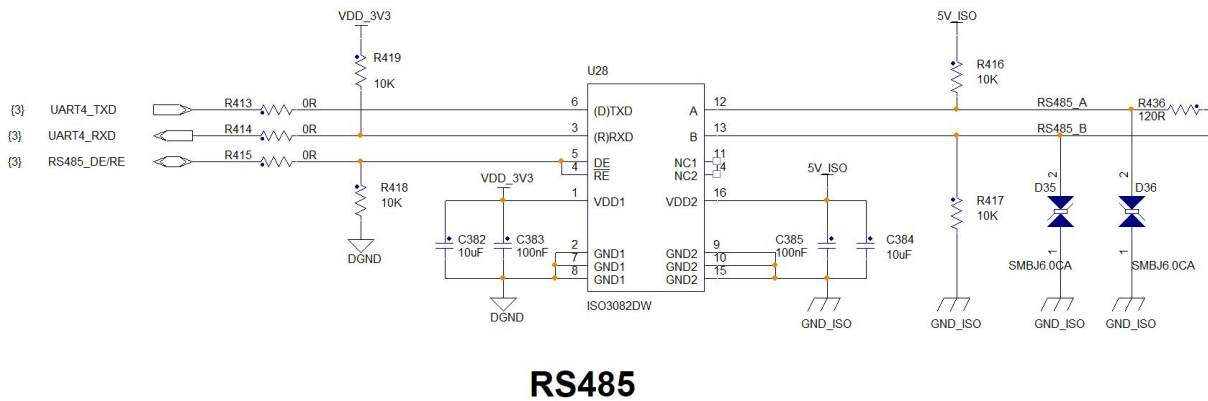
Figure 5-6 Isolated RS232 Reference design
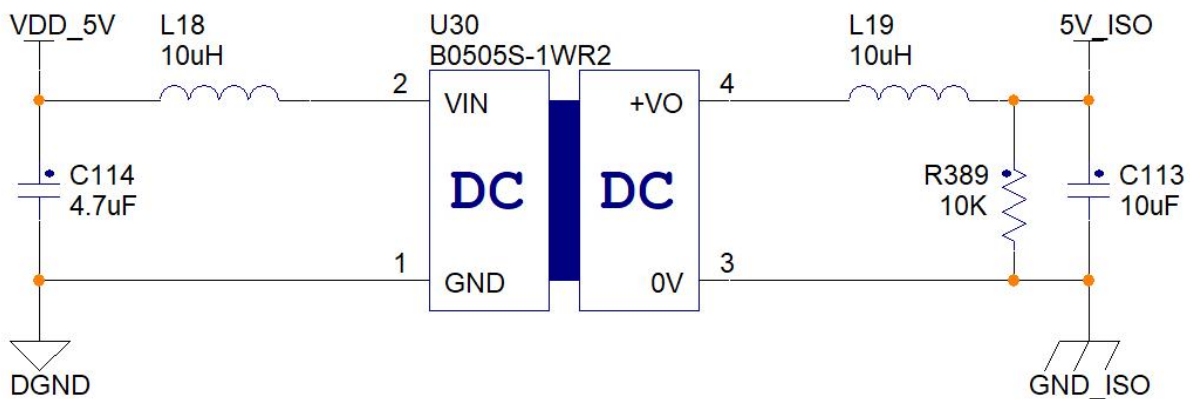
Figure 5-7 Isolated 5V power Reference design

5.2.3. UART for debugging serial port

JP1 is a general specification of 2.54mm pitch pin header for easy connection with the dupont head of the adapter.
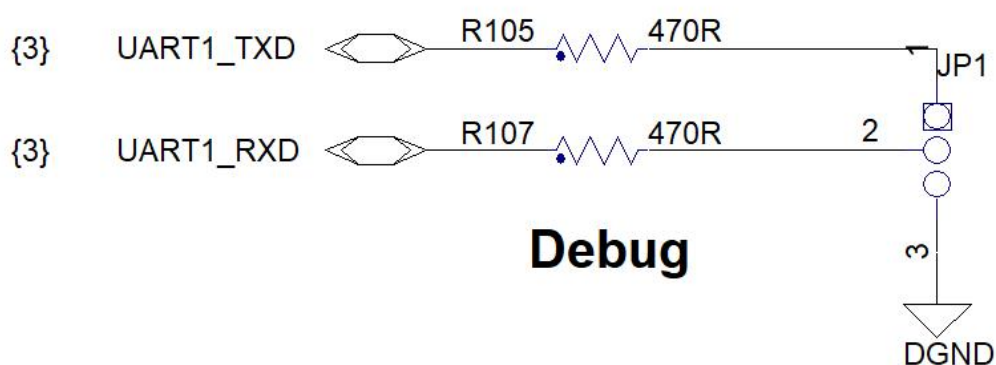
Figure 5-8 debug serial port Reference design

5.2.4. Layout guidelines

♦ Keep sufficient distance between signal and power supply plane before and after isolation;

♦ RS485 circuit Ω resistance (R436) close to 120 conversion chip placement;

♦ Place TVS close to connector;

♦ 100 Ω RS485 differential impedance signal, isometric control error of plus or minus 300 mil.

5.3. USB interface

The MYC-Y6ULX-V2 core module offers two USB2.0 interfaces and support OTG function. If the user wants to use OTG function of USB, micro-USB interface is recommended, because it`s a 5-wire connector with USB_ID signal, which can be used to identify HOST and DEVICE, so as to realize the OTG function. If the user does not use OTG function of USB and only uses it as USB HOST, then the USB connector can be either 4-wire or 5-wire.

USB switch chip is needed to use OTG function. The USB switch chip used in reference design is TPS2041BDBV, and the ID pin of the micro-USB connector is connected to U8 to realize OTG function.

When the HOST is used only, the USB switch chip can be avoided. Add a fuse between VDD_5V and the power supply of USB connector to protect the circuit. A 4-wire USB connector is used in reference design, if a 5-wire USB connector is used, the ID signal of the seat should be connected to GND shortly.

TVS and common mode choke are recommended for USB signal.

5.3.1. Reference design
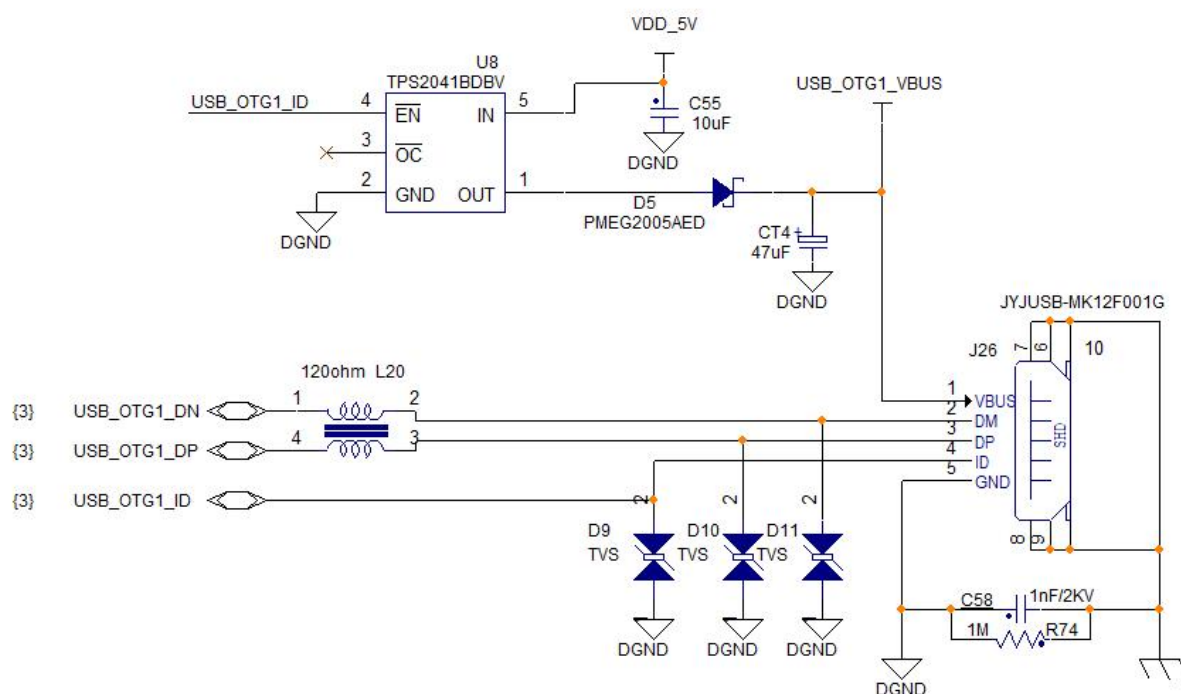
Figure 5-9 OTG reference design
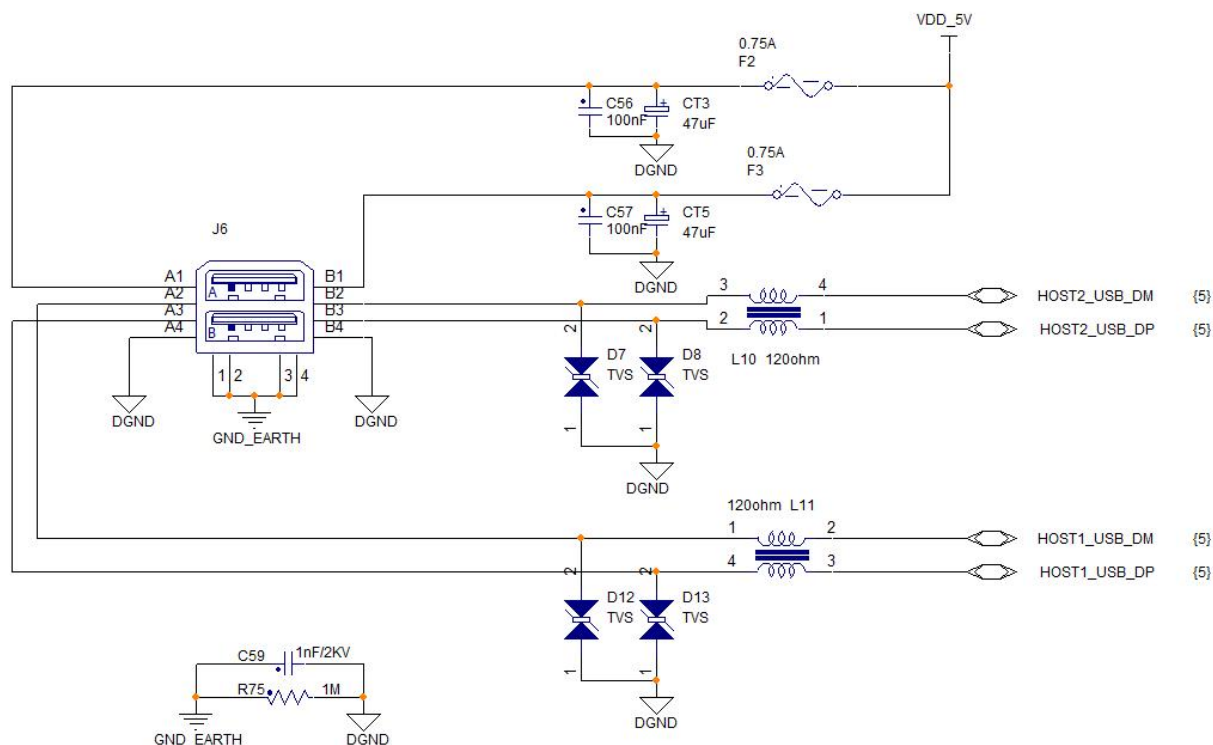
Figure 5-10 HOST reference design

5.3.2. Layout guidelines

♦ Match all segment lengths between differential pairs along the entire length of the pair. Trace match the differential pairs to be within +/-30 mils.

♦ Route all USB differential signals with 90 Ω differential impedance;

♦ USB signal length as short as possible;

♦ Place at least one GND stitching via within 50 mils of signal via when switching reference planes;

♦ USB signal traces never cross gap or slot in reference plane;

♦ USB signals are recommended to be routed on top or bottom layer.

5.4. Ethernet interface

MYC-Y6ULX-V2 core module offers two 10M/100M ethernet controllers.The first controller (Ethernet1) has integrated an ethernet PHY chip on the core module, so users only need to connect the RMII signals of Ethernet1 to the transformer on the carrier board.The other controller (Ethernet2) does not have PHY chip on the core module, so users need to place PHY chip on the carrier board o realize ethernet function.
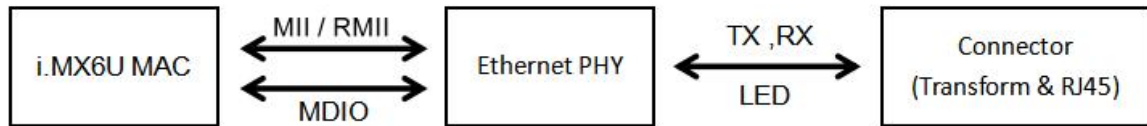
Figure 5-10 Ethernet links

The ethernet controller supports 10/100 Mbps RMII and MII interfaces. The number of signal lines of the RMII interface is half less than that of the MII interface, which can simplify the design and save resources, so the RMII interface is used by default to connect with Ethernet PHY on the core module.

For Ethernet2, The PHY chip used in the reference design is LAN8720A, the network port transformer is HR911105A. The PHY chip is 3.3V powerd, it is suggested to add beads between VDD_3V3 and VDD_PHY2_3V3, and add ESD protective devices similar to U14 in the front end of the network transformer.

5.4.1. Reference design
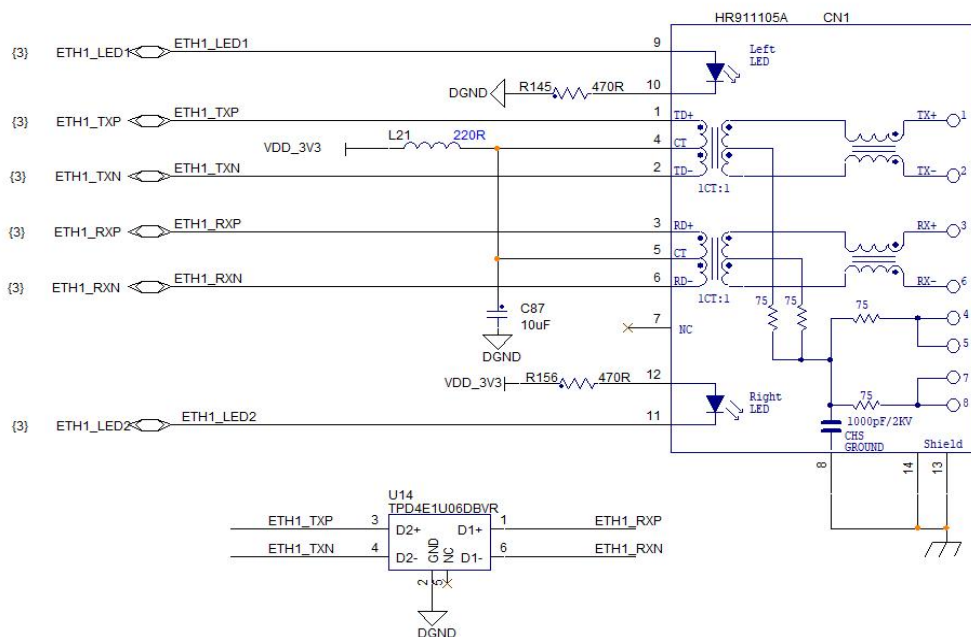
Figure 5-11 Ethernet1 reference design
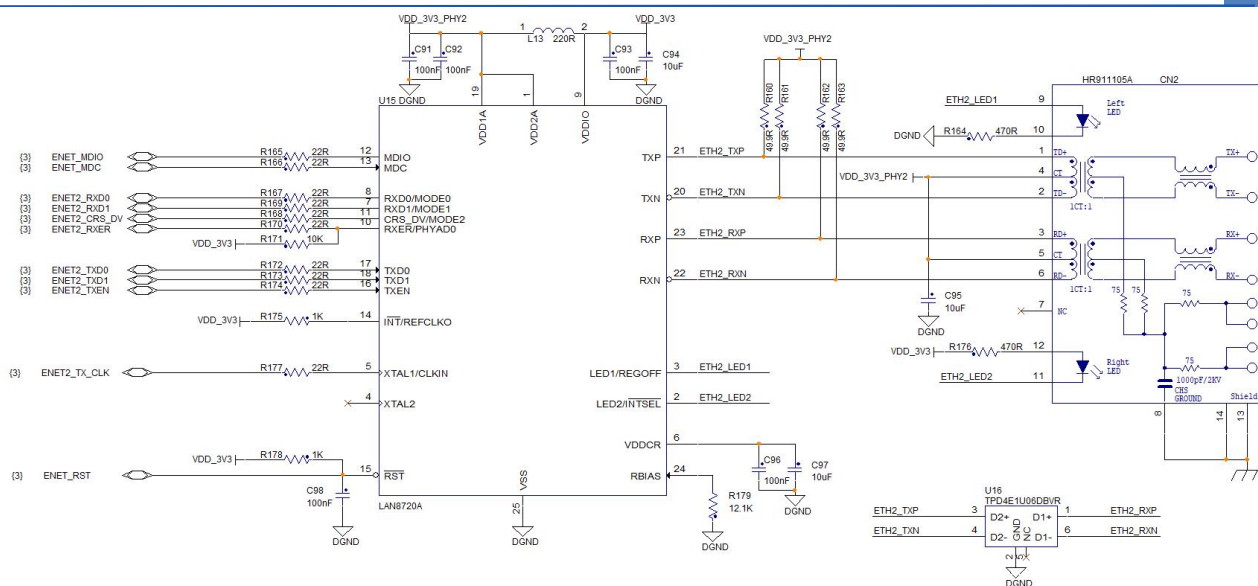
Figure 5-12 Ethernet2 reference design

5.4.2. Layout guidelines

◆ Trace match the RMII signals to be within +/-100 mils.

◆ Trace match the network differential pairs signals to be within +/-30 mils.

◆ Place the network transformer closed to the PHY chip and the recommended distance is not more than 20mm;

◆ The decoupling capacitor of the PHY chip is placed close to the PHY chip.

◆ Place R160\R161\R162\R163 closed to the PHY chip;

◆ Pin 8\13\14 of CN1\CN2 is recommended to be directly connected to the ground of the chassis;

5.5. CAN interface

MYC-Y6ULX-V2 core module offers two CAN controllers. User need add two CAN transceivers on these ports to realize CAN-BUS communication.Reference design is shown in the figure below, which adopts the isolated transceiver module ISO1050DUBR. The module integrates the necessary transceiver for CAN-BUS and the electrical isolation circuit, the isolation voltage is up to 2500 VDC, which greatly simplifies the circuit design and ensures the reliability of communication.

In order to achieve complete electrical isolation, it is also necessary to use the isolation power module to generate the isolation power dedicated to CAN. In reference design, the b0505S-1WR2 of Mornsun is selected to generate the isolation voltage of 5V. Note that this power supply module has the requirement of minimum load and 10K resistance (R389) should be added as the default load. Please refer to section 5.2 for referenced circuits.

CANH and CANL signals need to be well protected. TVS should be added in the normal environment, and TVS model in the referenced design isSMBJ6.0CA. If the CAN-BUS is used in a harsh environment, protective devices such as common mode choke, gas discharge tubes, and surge suppressors should also be considered.

5.5.1. Reference design
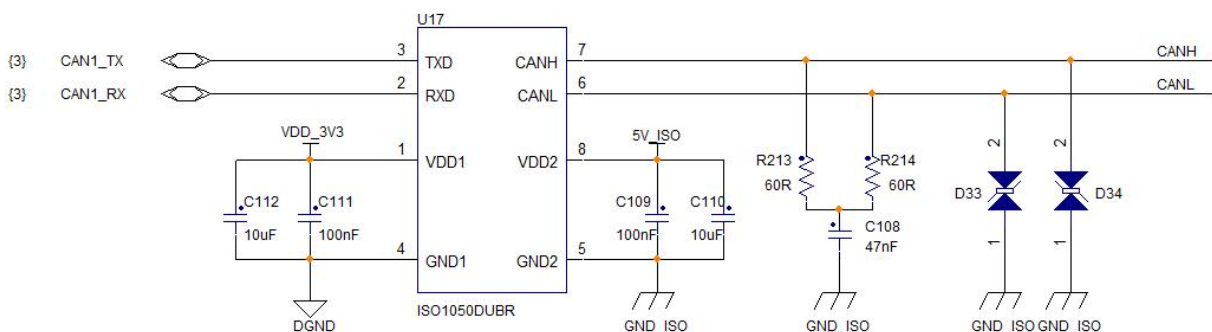
Figure 5-13 Isolated CAN transceiver Reference design

5.5.2. Layout guidelines

♦ Place R213\R214 closed to the transceiver, place D33/D34 closed to the CAN connector;

♦ Trace match the CAN signals to be within +/-300 mils.

♦ Don`t route signals in the area under the isolated power chip, including the inner layer.

5.6. The I2C interface

MYC-Y6ULX-V2 core module offers four I2C controllers and supports two modes, with the rate of 100Kbit/s in standard mode and 400Kbit/s in fast mode.

Several devices can be mounted under the same I2C bus. The following points should be paid attention to when designing the schematic:

♦ Check whether the device address under the same bus is in conflict;

♦ Ensure that each I2C bus has a pair of pull-up resistors, the resistance value is recommended to be 2.2K~10K, but do not repeatedly add;

♦ Check whether the level of I2C interface of the device is 3.3V. If not, add the level shift circuit.

♦ The number of devices under the same bus should not be too large, otherwise it is possible to exceed the load capacitance limit of 400 pF required by the I2C specification and affect the signal waveform.

5.6.1. Reference design
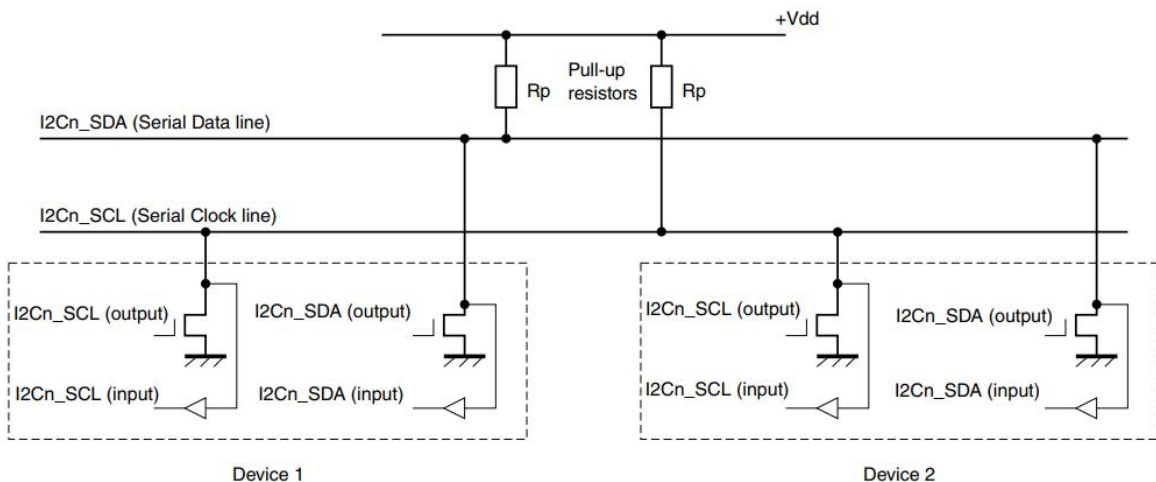
FIG. 5-14 I2C reference design

5.6.2. Layout guidelines

♦ I2C signal line width should not be too narrow, it is recommended to be 6mil or above;

♦ The location of each I2C device should be planned before layout, if the length of I2C bus is too long will also cause the increase of the bus load capacitance.

♦ Keep I2C signals away from interference source.

5.7. SPI interface

MYC-Y6ULX-V2 core module offers up to four SPI controllers, supporting master/slave modes.SPI signals include SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISO. Because of pin multiplexing, the SPI pin is used as another interface in the reference design. If you need to use the SPI function, please consult the pinmux section in the official i.MX 6UL/6ULL manual and visit this link for more information:

https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors/i-mx-6ultralite-processor-low-power-secure-arm-cortex-a7-core:i.MX6UL?&tab=Documentation_Tab&linkline=Data-Sheet

5.7.1. Reference design
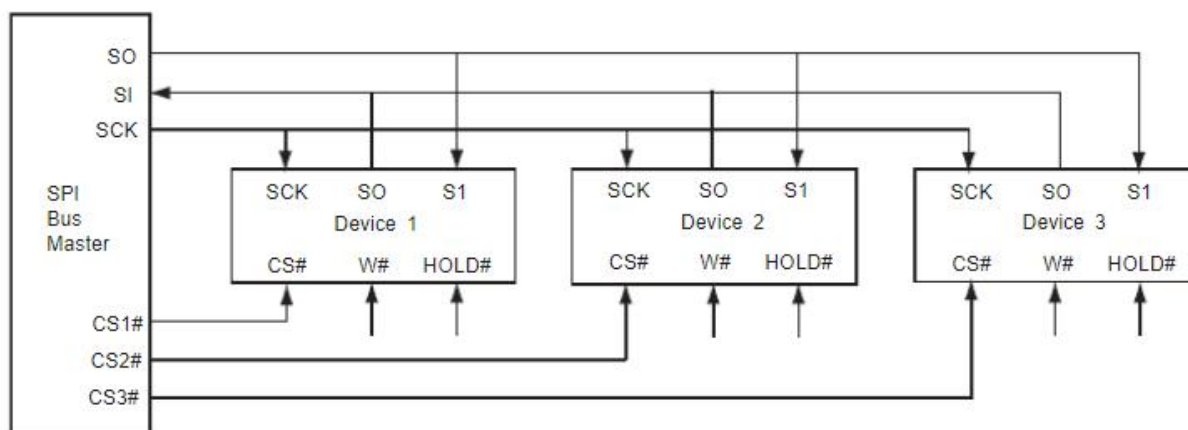
Figure 5-15 SPI reference design

5.7.2. Layout guidelines

♦ Route all SPI signals with 50 Ω single-ended impedance;

♦ Keep no less than 3 times trace width spacing from other signals.

♦ Ensure that the reference layer of the signal is continuous.

5.8. CSI interface

The CSI interface supports 8-bit or 24-bit data input in YCbCr, YUV and RGB formats, or data input in 8-bit, 10-bit, or 16-bit Bayer format with a maximum pixel clock of 238 MHz. Due to the relationship of pin multiplexing, 8-bit data signal is selected by default in the CSI interface of MYC-Y6ULX-V2 core module, and 8-bit parallel camera interface can be considered in the carrier board design.The FPC connector is selected as the camera input interface in reference design, and the connector model is FH12-30s to 0.5s.

It is recommended to use Myirtech's MY-Cam011B camera module to connect to J9. Please visit http://www.myir-tech.com/product/my_cam011b.htm for more information about this module.

名称		参数
Active Array Size		1632 x 1212
Power Supply	Core	1.5VDC ± 5%
	Analog	2.6 ~ 3.0VDC
	I/O	1.7V to 3.0V
Power Requirements	Active	224 mW
	Standby	75 µA
Temperature Range	Operation	-20℃ to 70℃
	Stable Image	0℃ to 50℃
Output Formats (8-bit)		• YUV422/YCbCr422 • RGB565/555 • GRB422 • 8-/10-bit raw RGB data
Lens size		1/5″
Lens chief ray angle		25.7°
Maximum Image Transfer Rate	UXGA(1600x1200)	15 fps
	SVGA(800x600)	30 fps
	720p(1280x720)	30 fps
	1366x768	24 fps
Sensitivity		960mV/Lux -sec
S/N Ratio		36 dB
Dynamic Range		66 dB
Scan Mode		Progressive
Maximum Exposure Interval		1228 x t_{ROW}
Gamma Correction		Programmable
Pixel Size		1.75 µm x 1.75 µm
Dark Current		4mV/s at 60℃
Well Capacity		6.3 Ke
Fixed Pattern Noise		1% of $V_{PEAK-TO-PEAK}$
Image Area		2856µm x 2121µm
Package Dimensions		4735µm x 4385µm

Figure 5-16 MY-CAM011B camera module specification

5.8.1. Reference design
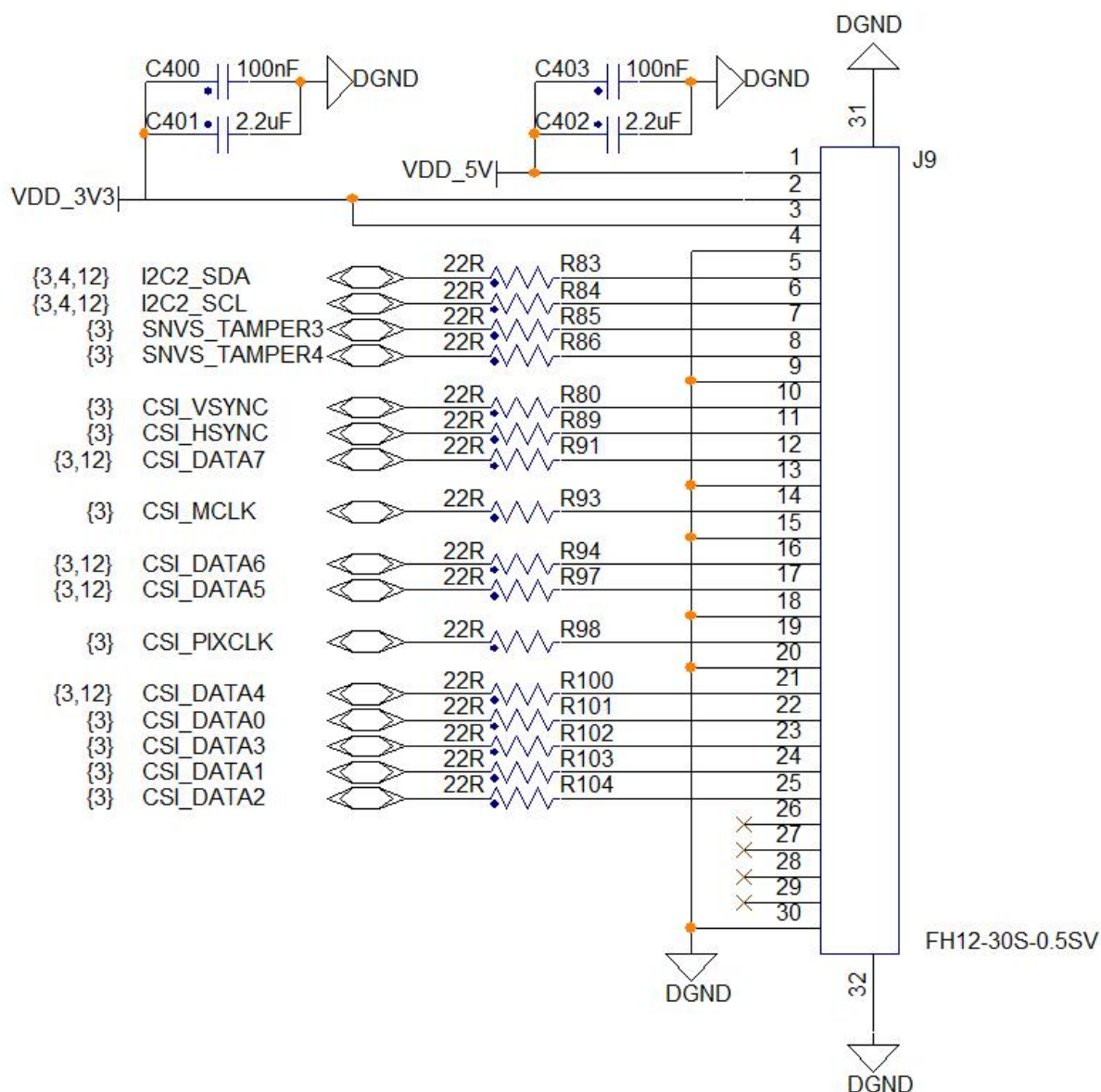
Figure 5-17 CSI interface reference design

5.8.2. Layout guidelines

♦ Place 22 Ω resistor closed to the FPC connector;

♦ Trace match the CSI signals to be within +/-100 mils;

♦ Keep no less than 2 times trace width spacing from other signals.

5.9. LCD interface

MYC-Y6ULX-V2 core module offers an LCD controller with 1 channel of 16bit RGB signal, which supports a variety of LCD screens such as TFT screen. The default resolution is 480x272 (4.3 inches) and 800x480 (7 inches).You can choose MY-TFT043RV2, MY-TFT070RV2 or MY-TFT070CV2 screen module provided by Myirtech.

MY-TFT043RV2 is a 4.3-inch LCD resistive touch screen, MY-TFT070RV2 is a 7-inch LCD resistive touch screen, and MY-TFT070CV2 is a 7-inch LCD capacitive touch screen. Please visit http://www.myir-tech.com/product for module details.

FPC connector is selected for LCD screen in the reference design, and the connector model is FH12-50s-0.5SV.

When you plan to use a 24-bit LCD screen, you can also connect the 16-bit interface to a 24-bit LCD screen. In this case, the 16-bit RGB signal of the processor is usually connected to the high bits for each color of the LCD screen, while the low bits of the LCD screen is grounding. Therefore, TFT_B2~TFT_B0、 TFT_G1~TFT_G0、 TFT_R2~TFT_R0 are connected to GND in the referenced design.

5.9.1. Reference design
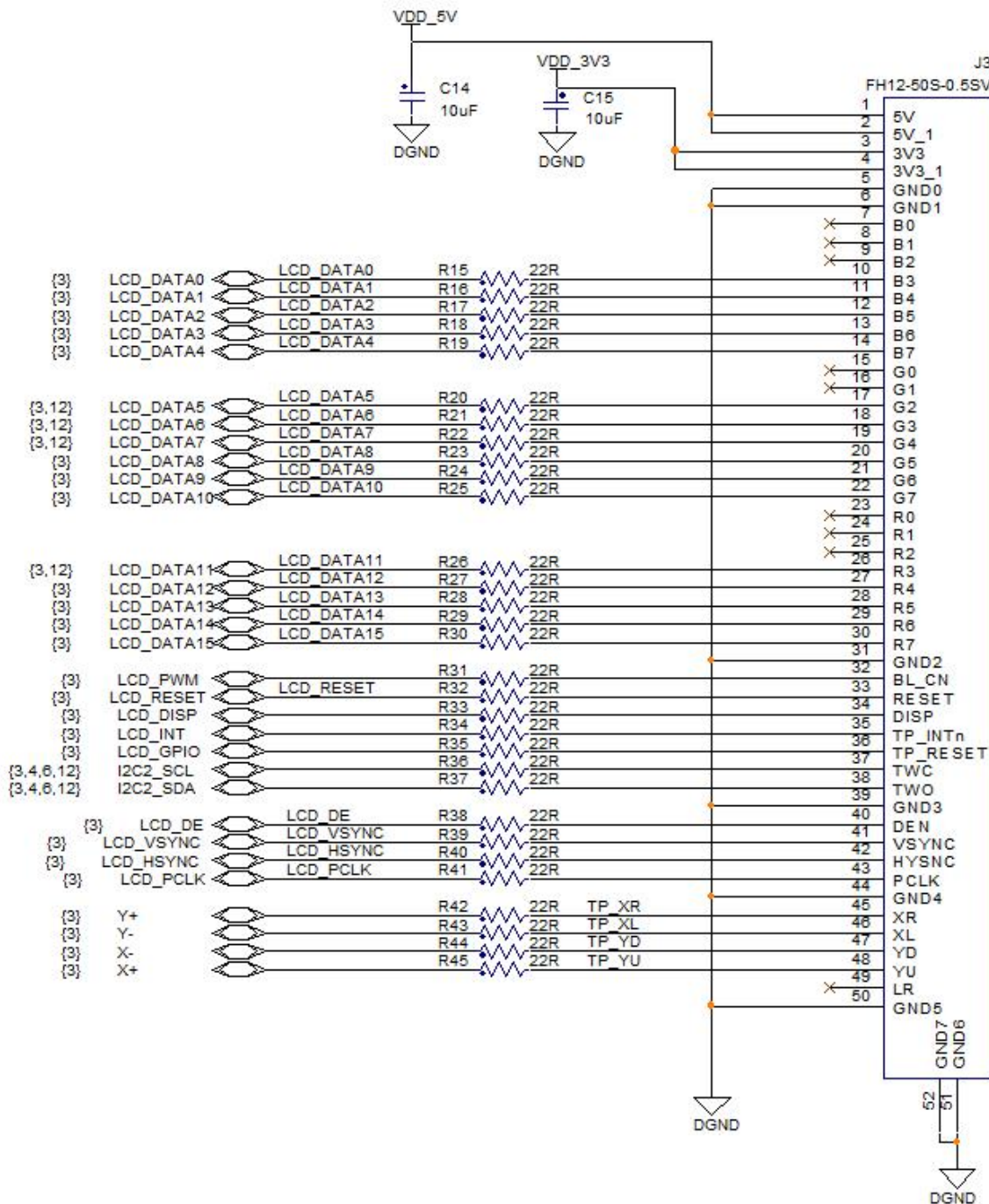
Figure 5-18 LCD interface reference design

5.9.2. Layout guidelines

♦ Place 22 Ω resistor closed to the core module stamp hole;

♦ Trace match the LCD signals to be within +/-100 mils;

♦ Keep no less than 2 times trace width spacing from other signals.

5.10. AUDIO interface

The MYC-Y6ULX-V2 core module offers up to two synchronous audio interfaces (SAI), which supports full-duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

When using AUDIO function, connect SAI signals to the audio codec chip first, and then add the external headset and microphone. The reference design uses the WM8904 chip for audio CODEC, which is a low power consumption, high performance CODEC chip, especially suitable for audio applications of stereo portable devices.

The AUDIO_GND in audio circuit is isolated from the DGND of digital circuit with 0Ω resistor. The capacitance of power supply pin and the filter capacitance of audio signal should also be connected to the AUDIO_GND. The MIC signal should be connected to 1N1L or 1N1R pin if the monophonic microphone is used, and the MIC signals should be connected to 1N1L and 1N1R pin seperately if the microphone has double channels. In the reference design, monophonic microphone is used.

5.10.1. Reference design

Figure 5-21 AUDIO interface reference design

5.10.2. Layout guidelines

♦ The isolation point (R61) of AUDIO_GND and DGND adopts star grounding and is as close as possible to the power input point of the carrier board.

♦ The layout of audio circuit is far away from the interference source. It is recommended to place the analog circuit in a separate area of PCB board.

♦ The audio chip should be as close to the earphone and microphone jack as possible, and the audio signal should be as short as possible.

5.11. Standby battery interface

The VDD_BAT pin (PIN39) of the MYC-Y6ULX-V2 core module is a backup battery pin that can be used to maintain the core module RTC function in the event of system power failure. J2 is a battery holder that can hold button batteries in the size of 1220/1225.

However, because the RTCS inside the core board consume more power, you are advised to use an external real-time clock module (RX-8025T/UC).

5.11.1. Reference design
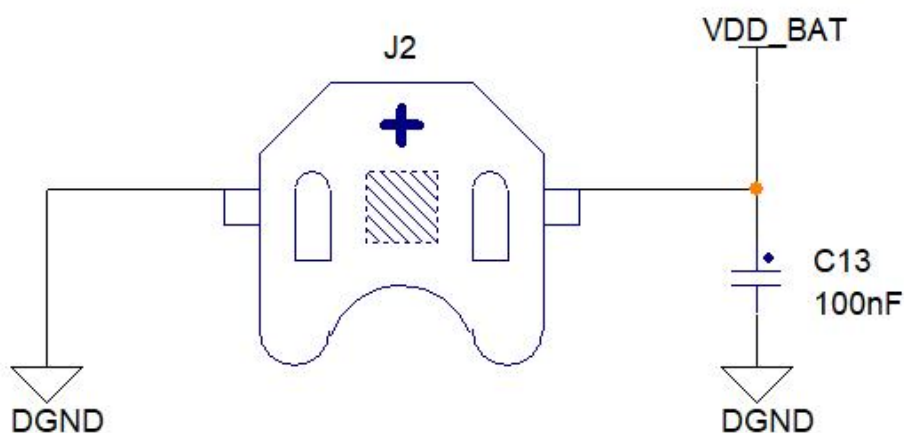
Figure 5-22 LCD interface reference design

5.11.2. Layout guidelines

♦ Place C13 close to J2.

5.12. WIFI module

Considering the universality of WIFI module, USI's 2.4G WIFI module WM-N-BM-02, is used in the reference design.This module is based on Broadcom's 43362 chipset, the communication interface is SDIO, and supports 802.11b/g/n.The SDIO interface of the module is connected to the uSDHC2 controller of the processor in the reference design, and the standard SMA antenna interface is reserved on the carrier board, which can be used with the complimentary WIFI antenna.

Note that since the eMMC and WIFI modules use the same uSDHC interface, the eMMC version the core module does not support this function. Moreover, the SDIO pins used in the reference circuit are already pulled down on the core module, and the pull-down resistance value is 47 K; So when designing the carrier board, these SDIO pins must be pulled up. The pull-up resistance value should be less than 4.7 K. In the reference design ,the 2.2 K pull-up resistor is selected. For more information about the module, see the relevant device manual provided by Myirtech.

5.12.1. Reference design

USI WIFI

Figure 5-23 Reference design of WIFI module

5.12.2. Layout guidelines

◆ Avoid placing unrelated devices and routing signals under the module PCB package area (including the BOTTOM layer);

◆ Trace match the SDIO signals to be within +/-200 mils.

◆ Route SDIO signals with 50 Ω signal impedance;

◆ SD2 CLK clock is recommended to be surrounded by ground if there is enough space;

◆ Route antenna signal WB_RF_ANT on the same layer with WIFI module, and ensure the single-ended impedance 50Ω; try not to change the signal layer of antenna signal.

◆ Place at least one GND stitching via within 50 mils of antenna signal via when switching reference planes.

◆ Place the antenna far away from the power supply and high frequency circuits, and the distance between the antenna signal and the antenna connector is as short as possible.

5.13. 4G module

Considering the wide application of 4G technology in the industrial field, the EC20 Mini PCIE-C module of Quectel was used as in the reference design. This module is a LTE module with PCI Express Mini Card 1.2 standard interface, based on the qualcomm MDM9215 platform, supports WinCE/Linux/Android embedded operating system.For more information about this module, please refer to the relevant device manual provided by Myirtech.

In the reference design, USB signal is used to control 4G module. Since GPIO of the core module is 3.3V level, and GPIO of the 4G module is 1.8V level, MOSFET is added for simple level conversion. J21 is the SIM card slot. The 4G module is equipped with IPEX antenna seat, J25 and J24 are reserved TO be compatible with SMA antenna, IPEX TO IPEX wiring can be used. The Mini PCIE connector is LOTES 'AAA PCI-047 PCI-E connector.

5.13.1. Reference design
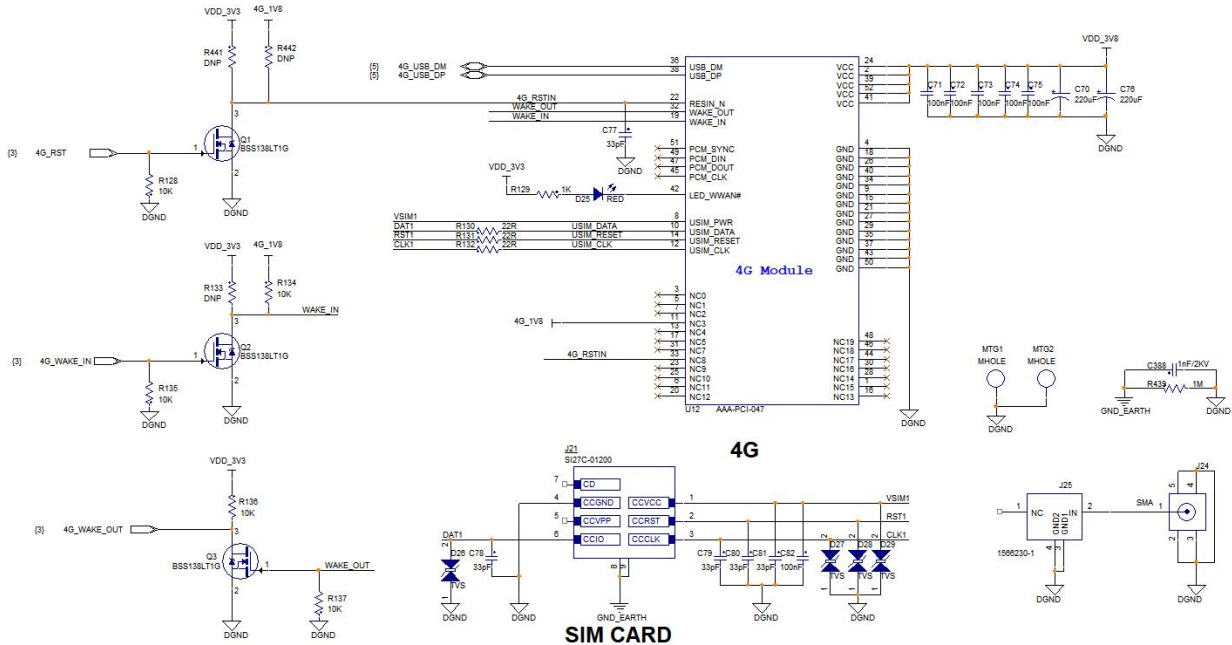
Figure 5-24 4G module Reference design

5.13.2. Layout guidelines

♦ Please pay attention to limit the height of 4G module connector. It is not recommended to place other devices or route other signals below the module.

♦ The 4G module should be away from sensitive circuits and other interference sources, and the SIM card should be as close to the 4G module as possible.

♦ Route USB differential signals with 90 Ω differential impedance;

♦ Trace match the differential pairs to be within +/-30 mils.

♦ In order to prevent USIM_CLK signal and USIM_DATA signal from crosstalk, the two signals should not be too close to each other, and the shielding should be added between the two paths.

♦ The parasitic capacitance of the TVS selected has to be no more than 10pF, and the capacitance of C79\C80C81 is recommended to be 33pF.

6. Design checklist

6.1. Power supply design

Check box	Proposal
1. core module supply voltage	The recommended value is 3.3V and the absolute value is 2.8V-3.6V
2. Decoupling capacitance	Use capacitors with 47uF and above value for core module power supply
3. PMIC_ON_REQ pin	This 3.3V output signal can be used as the enable pin of the carrier board peripheral power supply
4. IO level of carrier board peripherals	The IO voltage level of the peripheral should match the corresponding interface level of the core module
5. core module power sequence	It is recommended that the core module power start before the peripheral power
6. Power chip temperature rise	Confirm the thermal resistance of the power chip, and calculate the maximum temperature rise of the power chip based on the power consumption of the core module to ensure that the final temperature is within the specified range of the power chip

Table 6-1 Power supply checklist

6.2. System startup circuit design

Check box	Proposal
1. Configuration of BOOT_MODE pins	Choose the right BOOT MODE according to the needs of the product
2. Configuration of BOOT_DEVICE pins	Pay attention to distinguish whether the core module is eMMC version or NandFlash version
3. Reset pins	POR and ONOFF pins are both recommended to be used

Table 6-2 System startup checklist

6.3. Peripheral circuits design

Category	Check box	Proposal
USB	Capacitance value of USB D+/D- signal ESD device	The capacitance value of ESD devices is recommended to be less than 2pF
	Whether the capacitor of the supply pin is added series resistance	The interface 5V capacitor requires a 1-ohm resistor in series to limit the voltage surge at the USB port
Ethernet	PHY chip power supply	PHY chip power supply should be isolated with magnetic beads
	PHY chip clock signal source	The core module provides the clock signal needed by the PHY chip
	PHY chip differential signal	Each signal lines need to be pulled up to the VDD_3V3_PHY with 49.9 Ω resistance
	Connection of the center tap of the network transformer on the PHY chip side	Confirm the type of PHY chip, it can be found in the chip manual. If the PHY chip is current driven, the center tap needs to be pulled up to the VDD voltage of PHY. If the PHY is voltage driven, the tap does not need to be pulled up. If no descriptions about the PHY chip`s type in the manual, use the reference design or reserve a pull up resistor,
I2C	The value of pull up resistor of I2C	The more devices on the bus, the smaller the resistance value should be, otherwise the larger; Recommended resistance is 1.5K/ 2.2k /4.7K;
	How many pull-up resistors are required for each I2C bus	Just one pair
	The voltage value of the pulled up resistor	The pulled up resistor must be connected to the voltage that matches the I/O level
uSDHC	Whether the DATA and CMD signals are pulled up	Need to be pull up, i.e 47K resistor pulled up to 3.3V
CAN	Whetther the CAN-BUS should be isolated	In the cases of complex electrical environment，high reliability requirement or long CAN-BUS cable, CAN transceiver and its power supply circuit should be isolated
UART	UART signal connection	UART signals cannot be directly connected to the interface such as RS232\RS485, and only after the application of a special conversion chip can the corresponding interface be connected

Table 6-3 Check list of peripheral circuits

7. Explaination of common problems

7.1. Why use the connection method of stamp holes

If the board-to-board connector is selected, the advantage is the convenience to plug, but it also has the following disadvantages:

- ◆ Poor vibration performance;
- ◆ Not applicable to thin and light products;
- ◆ Easy to cause internal injury of PCBA.
- ◆ The yield rate of SMD is not high.

If the goldfinger is adopted, it will be more convenient to plug, but it also has the following disadvantages:

- ◆ It needs to place a high quality connector on the carrier board, which increases the cost;
- ◆ High production cost of goldfinger;
- ◆ Not applicable to thin and light products.

After weighing the pros and disadvantages, MYC-Y6ULX-V2 core module adopts the connection method of stamp hole, which does not have the above disadvantages.

7.2. Treatment of short circuit of module pin after SMT

- ◆ Check the solder paste of the module for continuous tin electrodeposit;
- ◆ Check whether the module is deviated from the original location;
- ◆ Verify that the SMT process and PCB design meet the requirements of Section 8 of the MYC-Y6ULX-V2 Product Manual.

Appendix A

Warranty & Technical Support Services

MYIR Electronics Limited is a global provider of ARM hardware and software tools, design solutions for embedded applications. We support our customers in a wide range of services to accelerate your time to market.

MYIR is an ARM Connected Community Member and work closely with ARM and many semiconductor vendors. We sell products ranging from board level products such as development boards, single board computers and CPU modules to help with your evaluation, prototype, and system integration or creating your own applications. Our products are used widely in industrial control, medical devices, consumer electronic, telecommunication systems, Human Machine Interface (HMI) and more other embedded applications. MYIR has an experienced team and provides custom design services based on ARM processors to help customers make your idea a reality.

The contents below introduce to customers the warranty and technical support services provided by MYIR as well as the matters needing attention in using MYIR's products.

Service Guarantee

MYIR regards the product quality as the life of an enterprise. We strictly check and control the core board design, the procurement of components, production control, product testing, packaging, shipping and other aspects and strive to provide products with best quality to customers. We believe that only quality products and excellent services can ensure the long-term cooperation and mutual benefit.

Price

MYIR insists on providing customers with the most valuable products. We do not pursue excess profits which we think only for short-time cooperation. Instead, we hope to establish long-term cooperation and win-win business with customers. So we will offer reasonable prices in the hope of making the business greater with the customers together hand in hand.

Delivery Time

MYIR will always keep a certain stock for its regular products. If your order quantity is less than the amount of inventory, the delivery time would be within three days; if your order quantity is greater than the number of inventory, the delivery time would be always four to six weeks. If for any urgent delivery, we can negotiate with customer and try to supply the goods in advance.

Technical Support

MYIR has a professional technical support team. Customer can contact us by email (support@myirtech.com), we will try to reply you within 48 hours. For mass production and customized products, we will specify person to follow the case and ensure the smooth production.

After-sale Service

MYIR offers one year free technical support and after-sales maintenance service from the purchase date. The service covers:

Technical support service

MYIR offers technical support for the hardware and software materials which have provided to customers;

➢ To help customers compile and run the source code we offer;

➤ To help customers solve problems occurred during operations if users follow the user manual documents;

➤ To judge whether the failure exists;

➤ To provide free software upgrading service.

➤ However, the following situations are not included in the scope of our free technical support service:

➤ Hardware or software problems occurred during customers' own development;

➤ Problems occurred when customers compile or run the OS which is tailored by themselves;

➤ Problems occurred during customers' own applications development;

➤ Problems occurred during the modification of MYIR's software source code.

After-sales maintenance service

The products except LCD, which are not used properly, will take the twelve months free maintenance service since the purchase date. But following situations are not included in the scope of our free maintenance service:

➤ The warranty period is expired;

➤ The customer cannot provide proof-of-purchase or the product has no serial number;

➤ The customer has not followed the instruction of the manual which has caused the damage the product;

➤ Due to the natural disasters (unexpected matters), or natural attrition of the components, or unexpected matters leads the defects of appearance/function;

➤ Due to the power supply, bump, leaking of the roof, pets, moist, impurities into the boards, all those reasons which have caused the damage of the products or defects of appearance;

➤ Due to unauthorized weld or dismantle parts or repair the products which has caused the damage of the products or defects of appearance;

➤ Due to unauthorized installation of the software, system or incorrect configuration or computer virus which has caused the damage of products.

Warm tips:

➤ MYIR does not supply maintenance service to LCD. We suggest the customer first check the LCD when receiving the goods. In case the LCD cannot run or no display, customer should contact MYIR within 7 business days from the moment get the goods.

➤ Please do not use finger nails or hard sharp object to touch the surface of the LCD.

➤ MYIR suggests user purchasing a piece of special wiper to wipe the LCD after long time use, please avoid clean the surface with fingers or hands to leave fingerprint.

➤ Do not clean the surface of the screen with chemicals.

➤ Please read through the product user manual before you using MYIR's products.

➤ For any maintenance service, customers should communicate with MYIR to confirm the issue first. MYIR's support team will judge the failure to see if the goods need to be returned for repair service, we will issue you RMA number for return maintenance service after confirmation.

Maintenance period and charges

MYIR will test the products within three days after receipt of the returned goods and inform customer the testing result. Then we will arrange shipment within one week for the repaired goods to the customer. For any special failure, we will negotiate with customers to confirm the maintenance period.

For products within warranty period and caused by quality problem, MYIR offers free maintenance service; for products within warranty period but out of free maintenance service scope, MYIR provides maintenance service but shall charge some basic material cost; for products out of warranty period, MYIR provides maintenance service but shall charge some basic material cost and handling fee.

Shipping cost

During the warranty period, the shipping cost which delivered to MYIR should be responsible by user; MYIR will pay for the return shipping cost to users when the product is repaired. If the warranty period is expired, all the shipping cost will be responsible by users.

Products Life Cycle

MYIR will always select mainstream chips for our design, thus to ensure at least ten years continuous supply; if meeting some main chip stopping production, we will inform customers in time and assist customers with products updating and upgrading.

Value-added Services

➢ MYIR provides services of driver development base on MYIR's products, like serial port, USB, Ethernet, LCD, etc.

➢ MYIR provides the services of OS porting, BSP drivers' development, API software development, etc.

➢ MYIR provides other products supporting services like power adapter, LCD panel, etc.

➢ ODM/OEM services.

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Hardware Design Guide