A 2-24GHz 360° Full-Span Differential Vector Modulator Phase Rotator with Transformer-Based Poly-Phase Quadrature Network

Tso-Wei Li, Jong Seok Park, and Hua Wang
School of Electrical and Computer Engineering, Georgia Tech, Atlanta, GA 30332 USA

***Abstract* — This paper presents a differential vector modulator phase rotator performing 360° full span phase interpolation over a first-ever decade-wide instantaneous bandwidth (2GHz-24GHz). A wideband poly-phase network based on folded transformer 90° couplers generates accurate differential quadrature signals with low passive loss (2dB) over a decade bandwidth. Two 5-bit linear digital variable gain amplifiers (VGAs) scale the quadrature signals, which are then combined for the target phase interpolations. Our phase rotator occupies a very compact chip size (1.2mm-by-1.8mm) in a standard 65nm CMOS process. Moreover, our design does not require any tuning element, band selection switch, or frequency-dependent code compensation/look-up table, ensuring that each phase interpolation code can be used for all the in-band operation frequencies. Additionally, the maximum RMS quantization phase error is only 1.22° within 1.5dB output magnitude variation for full 360° interpolation from 2GHz to 24GHz.**

***Index Terms*—Phase array, phase shifter, quadrature generation, poly-phase network.**

I. Introduction

Phase shifter is a key component in phased-array systems, and its performance governs the array beam-forming quality [1]. Broadband phase shifters are particularly useful in frequency-agile phased-array radars, hyperspectral imaging systems, and mm-Wave communication systems.

Reflective-type phase shifters (RTPS) utilize quadrature couplers and passive loads for phase shifting. However, a direct trade-off exists in RTPS between the phase shift range and the insertion loss, and they may also consume excessive chip areas due to the required λ/4 coupler [2]. A Cartesian vector modulator phase rotator can potentially address these issues [3] [4]. It typically utilizes a passive network to generate the quadrature signals from the RF input and then scales the I/Q signals to interpolate the desired phase (Fig. 1a). The operation bandwidth of a vector modulator phase rotator is chiefly determined by the passive quadrature generation network, which needs to provide phase/amplitude balanced I/Q signals over the entire bandwidth with minimum signal loss.

Lossy RC-CR network and its poly-phase extensions have been widely used for I/Q generations. However, their I/Q outputs are sensitive to the output loading. Moreover, there is a fundamental trade-off among phase/amplitude accuracy, bandwidth, and loss, which is governed by the number of poly-phase stages. As a result, the reported vector modulator phase rotators rarely achieve an instantaneous bandwidth larger than an octave [4].

In this paper, we present a Cartesian vector modulator phase rotator achieving a first-ever instantaneous decade-wide bandwidth (2GHz-24GHz) for 360° full span phase interpolation without any tunable element or band selection switch. A novel folded transformer-based poly-phase network generates high-quality I/Q signals over the entire decade-wide bandwidth with low signal loss.

This paper is organized as follows. Section II introduces the proposed wideband I/Q generation scheme. The vector modulator phase rotator is presented in Section III. The measurement results are shown in Section IV.

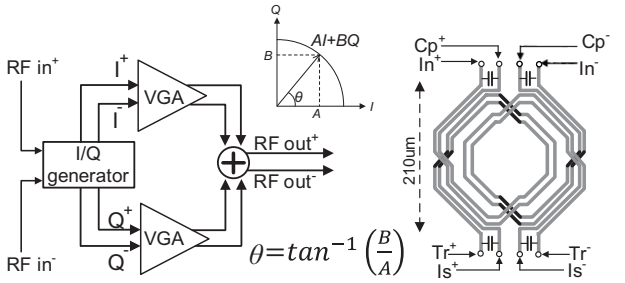

Fig. 1. (a) Vector modulator phase rotator block. (b) The proposed 8-port folded transformer 90° coupler layout.

II. Wideband Differential I/Q Generation

We propose and implement a 3-stage transformer-based poly-phase network to achieve an extremely wideband high-quality quadrature generation [5]. The poly-phase network is based on cascading five differential 90° couplers, each of which is composed of an 8-port folded differential transformer with loading capacitors (Fig. 1b and Fig. 2) [6]. Ports *In*±, *Cp*±, *Tr*±, and *Is*± represent the differential input, couple, through, and isolation ports in the 90° coupler, respectively. The phase relationship at each node of the poly-phase network is shown in Fig. 2a with the transformer 90° couplers unfolded for simplicity. Each isolation port is terminated by an on-chip 50ohm resistor. The details of the transformer poly-phase network are presented in [5]. Note that although the I/Q outputs provide equal RF output impedance, they present different DC output impedances due to the transformer DC routings in the poly-phase network. At DC, the I^+/I^- output ports each presents three paralleled 50ohm resistors, while the Q^+/Q^- output ports each presents two paralleled 50ohm resistors.

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Figure 3 shows the simulated phases and amplitudes of the output differential quadrature signals using full 3D electromagnetic (EM) modelling (Fig. 2b). High-quality I/Q outputs are achieved with a phase mismatch of less than 0.7° at 2GHz and less than 3.4° at 20GHz, and an amplitude mismatch of less than 3dB over a decade bandwidth (2.1GHz to 26.5GHz).

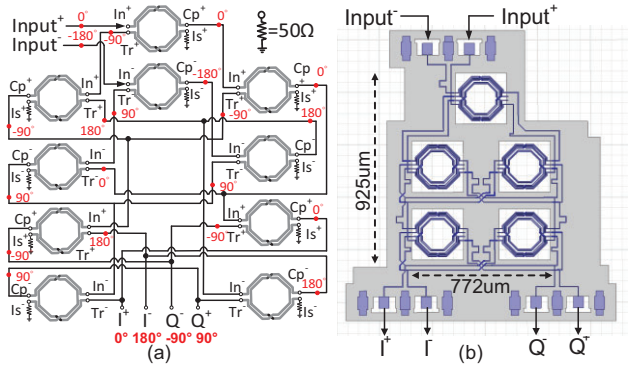

Fig. 2. Transformer-based differential poly-phase network for extremely wideband I/Q generation. (a) Simplified schematic with unfolded transformer 90° couplers. (b) 3D EM model with folded transformer 90° couplers.

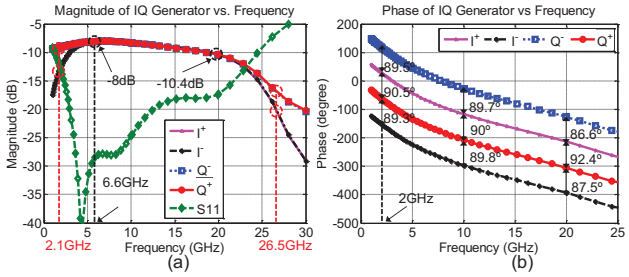

Fig. 3. Simulated (a) magnitudes and (b) phases of the I/Q outputs produced by the transformer-based poly phase network.

III. Vector Modulator Phase Rotator in CMOS

The schematic of our vector modulator phase rotator is shown in Fig. 4. The I/Q outputs of the transformer poly-phase network are independently amplified and scaled by two 5-bit variable gain amplifiers (VGAs). The resulting signals are then summed in current for desired phase shift. Inductors L_1-L_3 and resistors R_D form series-shunt-series peaking loads for bandwidth extension. An output differential open-drain (OD) buffer facilitates the measurement.

Each VGA is composed of five binary weighted VGA cells connected in parallel, and each cell is a differential common-gate (CG) cascode amplifier as a polarity selector controlled by digital switches [3]. Shown in Fig. 5 and Fig. 12, if S^+ is "High" (S^- as "Low"), transistors M1 and M4 are on, producing output RF currents. If S^+ is "Low" (S^- as "High"), M2 and M3 will be turned on, and the output current polarity is reversed. Therefore, the total output current weighting for each 5-bit VGA is given as

$$I_{out} = A_0 \times I_0 + A_1 \times I_1 + A_2 \times 2I_0 + A_3 \times 4I_0 + A_4 \times 8I_0, \quad (1)$$

where I_0 is the unity current; A_1 to A_4 are the control bits with ±1 values. An auxiliary VGA cell is introduced with an auxiliary bit of 0/+1 value, allowing the VGA to produce a true "zero" output. The 0/+1 auxiliary cell has the same weighting as the ×1 cell, while other cells are binary-weighted. Each 5-bit VGA achieves a normalized output current weighting from -15 to +15 (31 settings), which yields total 961 Cartesian interpolation points on the I/Q constellation plane. Note the I/Q VGA each consumes a constant DC current independent of the control bit settings.

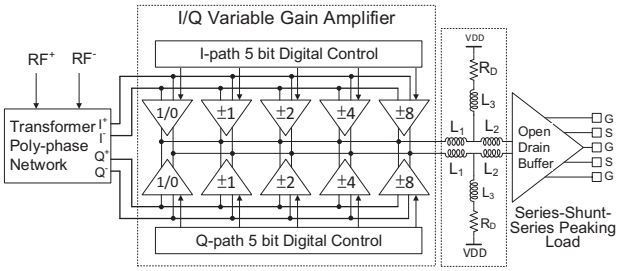

Fig. 4. Proposed vector modulator phase rotator schematic.

Since the transformer poly-phase network requires 50ohm RF output loading, a common-gate (CG) topology is used for the VGA cells to provide broadband matching. The CG VGA cells are sized to collectively provide a 50 ohm load at each I/Q input to match the poly-phase network.

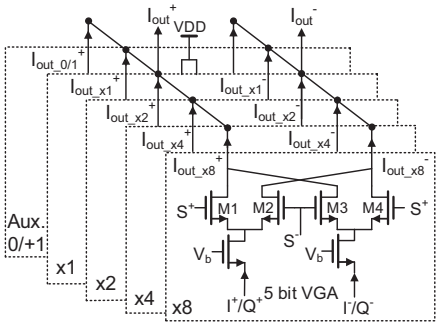

Fig. 5. The schematic of the 5-bit VGA amplifier.

IV. Bias Generation Circuit for I/Q VGAs

To ensure that the I/Q VGAs preserve well matched weighting, a constant biasing current density is needed. However, the two source terminals of the I-path CG VGA are DC connected to three paralleled 50ohm resistors in the transformer poly-phase network, while the Q-path CG VGA sources are each DC connected to two paralleled 50ohm resistors. A dedicated bias generation circuit is thus designed to accommodate this difference (Fig. 6).

Cascoded PMOS current mirrors use a common reference to bias the I/Q path biasing circuits, which have the identical device sizing to ensure equal biasing currents. Diode connected M_I and M_Q with corresponding parallel resistors generate the reference voltages of V_{bI} and V_{bQ} and bias the common-gate transistors in the I/Q VGAs (Fig. 5).

This design thus provides a constant current density for the I/Q VGAs and ensures their matching.

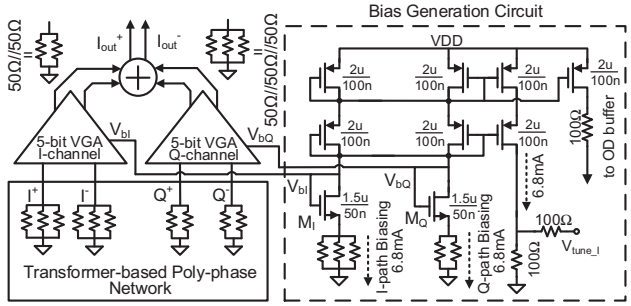

Fig. 6. The bias generation circuit for the I/Q-path VGAs.

V. Measurement Results

The phase rotator is implemented in a standard 65nm CMOS process with 1.2mm×1.8mm chip size (Fig. 7). The design consumes 46mA from 2V excluding the open-drain buffer. The differential phase rotator is characterized by a 4-port vector network analyzer (Rohde & Schwarz ZVA24). Off-chip DACs generate the VGA 10-bit I/Q control codes.

The measured normalized constellations with total 961 Cartesian interpolation points for 4GHz, 10GHz and 24GHz are shown in Fig. 8, demonstrating well balanced I/Q signals and matched 5-bit VGA operations over the frequencies. The phase rotator frequency responses for the interpolation points within the 1.5dB magnitude variation are shown in Fig. 9. The measurements show maximum in-band gain of -3.5dB, gain peaking of 1dB, and -3dB bandwidth is up to 20GHz. For these VGA settings, full-range 360° phase shifts with dense interpolations are achieved over 1GHz to 24GHz. The two 5-bit VGAs have maximum Differential Nonlinearity (DNL) of 0.28 Least-Significant Bit (LSB) and maximum Integral Nonlinearity (INL) of 0.84 LSB, respectively.

The digital phase rotator provides discrete phase interpolations that result in phase quantization errors (QPE), shown in the inset in Fig 10. During the 360° full-span phase interpolation, a given magnitude variation specification limits the allowable interpolation points on the Cartesian plane. The measured RMS QPEs at different frequencies are shown versus magnitude variations (Fig. 10). A larger magnitude variation allows more phase interpolation points and thus suppresses the QPE. Within 1.5dB magnitude variation, our phase rotator has its RMS QPE of less than 1.22° from 2GHz to 24GHz, achieving the first-ever over-a-decade bandwidth. This *phase interpolation bandwidth*, is defined by the achieved RMS QPE, which is governed by the quality of the quadrature generation and the matching of the VGAs over the frequency. For a phase rotator, this phase interpolation bandwidth is more critical than the -3dB gain bandwidth, since the latter can be extended by peaking or stagger-tuning, but phase errors cannot be easily corrected.

Finally, the frequency-independent operation of our phase rotator is demonstrated. The measured full span 360° interpolated phases with a 22.5° step are shown in Fig. 11a. For each interpolated phase, although the same I/Q VGA control codes are used across the frequency, accurate phase interpolations are achieved. Furthermore, the phase errors, i.e., the deviation between the interpolated and target phases, are plotted (Fig. 11b). The maximum phase error is less than 5° from 3.1GHz to 22.5GHz for fixed I/Q codes. These results verify that our phase rotator offers a "one-code-for-all-frequency" phase interpolation solution.

Table I summarizes the comparison with other vector modulator phase rotators that include I/Q generation network. Figure 12 illustrates the operation of the VGA unit cell for its "Plus" and "Minus" states.

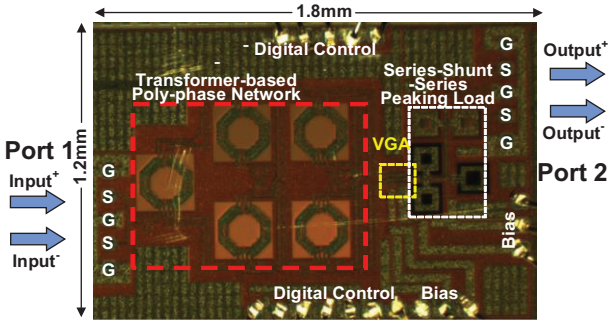

Fig. 7. The chip microphotograph of the 2-24GHz phase rotator.

VI. Conclusion

We present a 10-bit differential vector modulator phase rotator in a standard 65nm CMOS process, which achieves 360º full-span phase interpolation over a first-ever decade bandwidth (2GHz-to-24GHz) with no tuning component or band selection switch. A transformer-based poly-phase network achieves accurate quadrature signal generation over a decade bandwidth, which allows each phase interpolation setting to be used for all the in-band frequencies. The maximum RMS phase quantization error is only 1.22° within 1.5dB magnitude variation for 360° interpolation from 2GHz to 24GHz.

VII. Acknowledgment

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References

[1] S. Jeon, *et al.*, *IEEE JSSC*, 2008, pp. 2660–2673.
[2] H. Zarei, *et al.*, *IEEE TCSI,* 2007, pp. 1647–1656.
[3] H. Wang, *et al.*, *IEEE CICC,* 2007, pp. 671–674.
[4] J. Park, *et al.*, *IEEE RFIC,* 2014, pp. 75–78.
[5] J. Park *et al.*, *IEEE IMS*, 2015.
[6] J. Park *et al.*, *IEEE CICC*, 2013, pp. 1–4.
[7] K. Koh, *et al.*, *IEEE JSSC*, 2007, pp. 2535–2546.
[8] S. Sah, *et al.*, *IEEE T-MTT*, 2013, pp. 3024–3030.

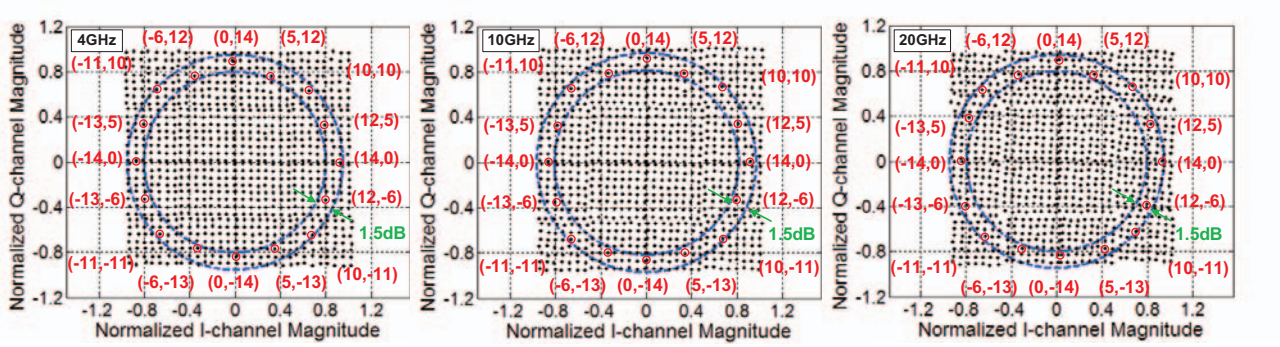
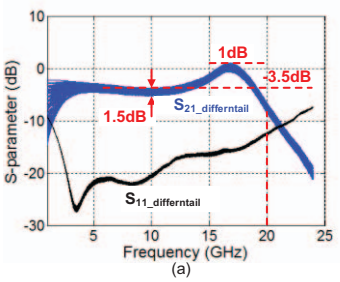


Fig. 8. Measured phase interpolation points on normalized I/Q constellation plane at 4 GHz, 10 GHz, and 20 GHz.



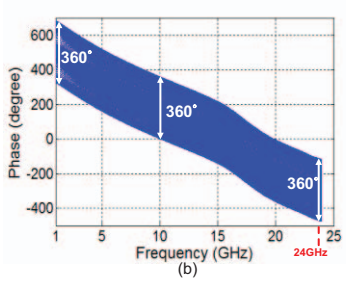


Fig. 9. Measured magnitude/phase responses with 1.5 dB magnitude variation. The differential input/output port definition is shown in Fig.7.

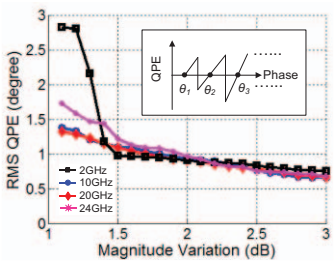
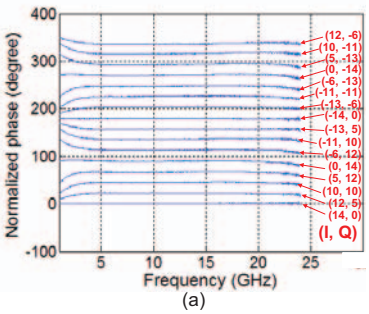


Fig.10. Measured RMS quantization phase error versus magnitude variations.

TABLE I Comparison of Vector Modulator Phase Rotator with I/Q Generation

	Frequency range (GHz)	Resolution (bit)	QPE	Quadrature generation circuit	Technology
This Work*	**2-20**	**10**	**<1.22°**	**Transformer-based poly-phase network**	**65 nm CMOS**
[7] JSSC 07'	5-18	8	<6.5°	Quadrature all-pass filter	130 nm CMOS
[4] RFIC 14'	20-27	10	<2°	Transformer based quadrature generation	90 nm BiCMOS
[8] TMTT 14'	15-35	10	<6.38°	RCCR poly phase network + inductor	180 nm BiCMOS

*Our design does not need frequency tuning element, band selection switch or frequency-dependent code compensation/lookup table.



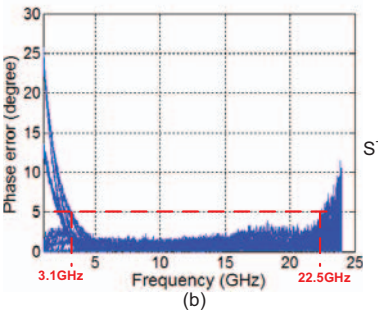


Fig. 11. (a) Measured 360° phase interpolation variation with a 22.5° phase step within 1.5dB magnitude variation. The I/Q VGA control codes are kept constant over the frequency. The intrinsic delay of the phase rotator is removed. (b) Phase error versus frequency using fixed I/Q VGA control codes.

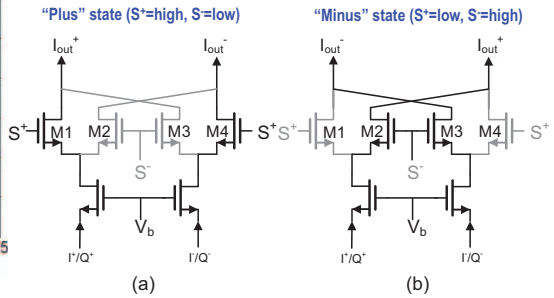


Fig. 12. Operation of the variable gain amplifier (VGA) unit cell in (a) "Plus" state and (b) "Minus" state.