0.13-μm CMOS Phase Shifters for X-, K*u*-, and K-Band Phased Arrays

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***Abstract*—Two 4-bit active phase shifters integrated with all digital control circuitry in 0.13-μm RF CMOS technology are developed for X- and K*u*-band (8–18 GHz) and K-band (18–26 GHz) phased arrays, respectively. The active digital phase shifters synthesize the required phase using a phase interpolation process by adding quadrature-phased input signals. The designs are based on a resonance-based quadrature all-pass filter for quadrature signaling with minimum loss and wide operation bandwidth. Both phase shifters can change phases with less than about 2 dB of RMS amplitude imbalance for all phase states through an associated DAC control. For the X- and K*u*-band phase shifter, the RMS phase error is less than 10° over the entire 5–18 GHz range. The average insertion loss ranges from −3 dB to −0.2 dB at 5–20 GHz. The input $P_{1\mathrm{dB}}$ for all 4-bit phase states is typically -5.4 ± 1.3 dBm at 12 GHz in the X- and K*u*-band phase shifter. The K-band phase shifter exhibits 6.5–13° of RMS phase error at 15–26 GHz. The average insertion loss is from −4.6 to −3 dB at 15–26 GHz. The input $P_{1\mathrm{dB}}$ of the K-band phase shifter is -0.8 ± 1.1 dBm at 24 GHz. For both phase shifters, the core size excluding all the pads and the output 50 Ω matching circuits, inserted for measurement purpose only, is very small, 0.33×0.43 mm^2. The total current consumption is 5.8 mA in the X- and K*u*-band phase shifter and 7.8 mA in the K-band phase shifter, from a 1.5 V supply voltage.**

***Index Terms*—Active phase shifters, CMOS analog integrated circuits, phased arrays, quadrature networks.**

I. Introduction

ELECTRONIC phase shifters (PSs), the most essential elements in electronic beam-steering systems such as phased-array antennas, have been traditionally developed using switched transmission lines [1]–[3], 90°-hybrid coupled lines [4]–[6], and periodic loaded lines [7]–[9]. However, even though these distributed approaches can achieve true time delay along the line sections, their physical sizes make them impractical for integration with multiple arrays in a commercial IC process, especially below K-band ($\leq \sim 30$ GHz) frequencies. The migrations from distributed networks to lumped-element configurations, such as synthetic transmission lines with varactors (and/or variable inductors) tuning [10]–[12], lumped hybrid-couplers with reflection loads [13]–[15], or the combined topologies of lumped low-pass filters and high-pass filters [16]–[18], seem to reduce the physical dimensions of the phase shifters with reasonable performance achieved. However, for fine phase quantization levels over wide operation bandwidth, the size of the lumped passive networks grows dramatically, mainly for the various on-chip inductors used, and is not suitable for integrated phased array systems on a chip. Also, in most cases, the relationships between the control signal (voltage or current) and output phase of the lumped passive phase shifters are not linear, which makes the design of the control circuits quite complex [19]. The passive phase shifters by themselves can achieve good linearity without consuming any DC power, but their large insertion loss requires an amplifier to compensate the loss, typically more than two stages at high frequencies ($> \sim 10$ GHz), which offsets the major merits of good linearity and low power dissipation of the passive phase shifters.

Compared with the passive designs, active phase shifters [20]–[27] where differential phases can be obtained by the roles of transistors rather than passive networks, can achieve a high integration level with decent gain and accuracy along with a fine digital phase control under a constrained power budget. Although sometimes referred to differently as an endless PS [20], a programmable PS [21], a Cartesian PS [23], or a phase rotator [24], the underlying principle for all cases is to interpolate the phases of two orthogonal-phased input signals through adding the I/Q inputs for synthesizing the required phase. The different amplitude weightings between the I- and Q-inputs result in different phases. Thus, the basic function blocks of a typical active phase shifter are composed of an I/Q generation network, an analog adder, and control circuits which set the different amplitude weightings of I- and Q-inputs in the analog adder for the necessary phase bits.

In this work, a 4-bit (phase quantization level $= 22.5°$) active phase shifters to be integrated on-chip with multiple phased arrays for X-, K*u*-, and K-band (8–26 GHz) applications are designed in a 0.13-μm RF CMOS technology ($f_t \approx$ 65–80 GHz). Section II describes the phase shifter architecture and performance requirements in detail. More specific circuit level descriptions of the building blocks are presented in Section III. The implementation details and experimental results are discussed in Section IV.

II. System Architecture

Fig. 1 briefly describes the phased array receiver system proposed for this work. The phased array adopts the conventional RF phase-shifting architecture, which is superior to other architectures such as local oscillator (LO) or IF phase-shifting systems in that the RF output signal has a high pattern directivity so that it can substantially reject an interferer before a RF mixer, relaxing the mixer linearity and overall dynamic range requirement [28]. A single-ended SiGe or GaAs low-noise amplifier (LNA) having variable gain function sets the noise figure (NF) and gain of

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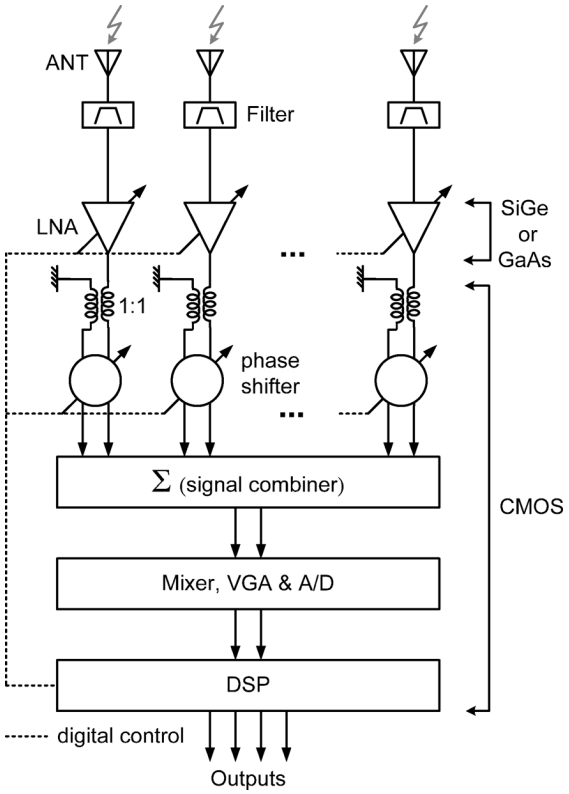


Fig. 1. Multiple antenna receiver for phased array applications. A SiGe or GaAs LNA is used depending on the required system noise figure.

the RF part, required from the overall system perspective. The system includes transformer-based (1:1) on-chip baluns for differential signaling after the LNA. The 4-bit differential phase shifter, presented in this work, should provide about $-5\sim0$ dB of insertion loss and higher than -5 dBm of input $P_{1\mathrm{dB}}$ level with less than 10 mW of power dissipation from a 1.5 V supply voltage. The input impedance of the phase shifter should be matched with the output impedance of the LNA ($=50\,\Omega$). As the phase shifter will eventually be integrated on-chip with an active signal combiner network whose input impedance is capacitive ($<\sim50$ fF, i.e., a gate input of a source follower), the output matching in the phase shifter is not necessary. However, the phase shifter should provide a digital interface to the DSP for 4-bit phase controls.

The building blocks of the differential active phase shifter are shown in Fig. 2. A differential input signal is split into quadrature phased I- and Q-vector signals using a quadrature all-pass filter (QAF), which provides differential 50 Ω matching with the previous stage as well. The QAF is based on L-C series resonators, utilizing the series resonance to minimize loss, which will be discussed in detail in the next section. An analog differential adder, composed of two Gilbert-cell type *signed* variable gain amplifiers (VGAs), adds the I- and Q-inputs from the QAF with proper amplitude weights and polarities, giving an interpolated output signal with a synthetic phase of $\angle\tan^{-1}(Q_{o\pm}/I_{o\pm})$ and magnitude of $\sqrt{(I_{o\pm}^2+Q_{o\pm}^2)}$. For 4-bit phase resolution, the different amplitude weightings of each input of the adder can be accomplished through changing the gain of each VGA differently. A current-mode 3-bit DAC takes this role by controlling the bias current of the VGAs. The logic encoder synthesizes the necessary control logic signals for the DAC and adder, using the 4-bit digital inputs from the DSP. The DAC is an indispensable element for fine digital phase controls in modern phased arrays. Decreasing the phase quantization level needs more sophisticated gain control from a higher resolution DAC, but will not result in any significant increase of the phase-shifter physical area.

III. Circuit Design

A. Quadrature All-Pass Filter (QAF)

In the phase synthesis, which is based on a phase interpolation method by adding two properly weighted quadrature vector signals, the accuracy of the output phase is dominated by the *orthonormal* precision of the I/Q seed vectors. Specifically, as the output phases heavily depend on the amplitude weightings of I- and Q-input, the output phase error is more sensitive to the amplitude mismatch than the phase mismatch of the I/Q inputs, which leads to the use of an all-pass polyphase filter ensuring equal I/Q amplitude for all ω, rather than a high-pass/low-pass mode one as an I/Q generation network as in [27]. However, although a polyphase filter provides a solid method of quadrature generation and is sometimes used in the LO signal path where the signal amplitude is very large, its loss often prevents it from being used in the main RF signal paths, and this is more true of multistage polyphase filters for wideband operations. To achieve high quadrature precision over wide bandwidth without sacrificing any signal loss, an L-C resonance based quadrature all-pass filter is developed.

1) Basic Operation: As shown in Fig. 3(a), the quadrature generation is based on the orthogonal phase splitting between $V_{OI}\,(=j\omega Li_s+Ri_s)$ and $V_{OQ}(=1/j\omega Ci_s+Ri_s)$ in the series R-L-C resonators. The transfer function of the single-ended I/Q network is

$$\begin{bmatrix} V_{OI} \\ V_{OQ} \end{bmatrix} = V_{\mathrm{in}} \times \begin{bmatrix} \dfrac{s\left(s+\frac{\omega_o}{Q}\right)}{s^2+\frac{\omega_o}{Q}s+\omega_o^2} \\ \dfrac{\frac{\omega_o}{Q}\left(s+Q\omega_o\right)}{s^2+\frac{\omega_o}{Q}s+\omega_o^2} \end{bmatrix} \tag{1}$$

where $\omega_o=1/\sqrt{LC}$ and $\mathrm{Q}=\sqrt{(L/C)}/R$. The benefits of this I/Q network are that it can guarantee 90° phase shift between I- and Q-paths for all ω due to a zero at DC from the I-path transfer function, and it can achieve 3 dB voltage gain at resonance frequency when $\mathrm{Q}=1$. The operating bandwidth is high due to the relatively low Q, although the I/Q output magnitudes are exact only at $\omega=\omega_o$ as the quadrature relationships rely on the low-pass and high-pass characteristics. Even with these advantages, the single-ended I/Q network does not seem to be very attractive because the quadrature accuracy in the single-ended I/Q network is very sensitive to any parasitic loading capacitance, discussed further in this section.

Fig. 3(b) and (c) show the transformation to a balanced second-order all-pass configuration to increase the bandwidth and to make it less sensitive to loading effects. After building up the resonators differentially [Fig. 3(b)], opening nodes A and B from the ground can eliminate the redundant series of L and C through resonance without causing any difference in the

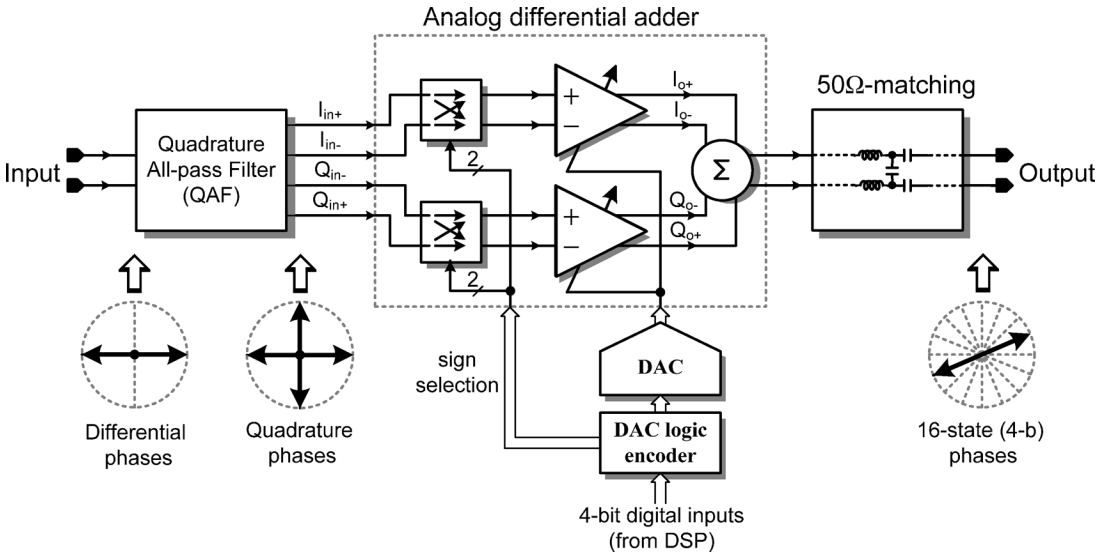


Fig. 2. Building blocks of the active phase shifter.

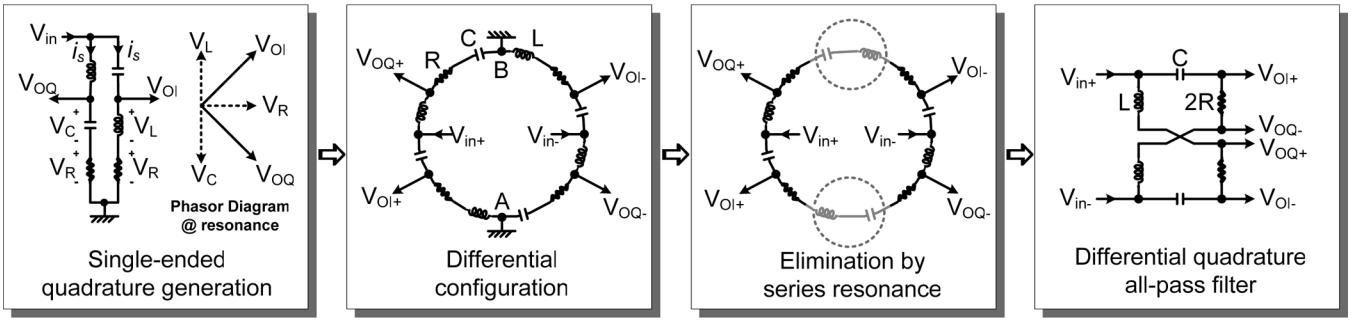


Fig. 3. Generation of the resonance-based second-order all-pass quadrature network. (a) Single-ended I/Q network based on low-pass and high-pass topologies. (b) Differential formation of (a). (c) Elimination of redundancy. (d) Differential quadrature all-pass filter.

quadrature operation [Fig. 3(c)]. The final form of the QAF [Fig. 3(d)] has a transfer function given by

$$\begin{bmatrix} V_{OI\pm} \\ V_{OQ\pm} \end{bmatrix} = V_{\text{in}} \times \begin{bmatrix} \pm\dfrac{s^2+\frac{2\omega_o}{Q}s-\omega_o^2}{s^2+\frac{2\omega_o}{Q}s+\omega_o^2} \\ \mp\dfrac{s^2-\frac{2\omega_o}{Q}s-\omega_o^2}{s^2+\frac{2\omega_o}{Q}s+\omega_o^2} \end{bmatrix} \tag{2}$$

where $V_{\text{in}} = V_{\text{in}+} = -V_{\text{in}-}$. Intuitively, in Fig. 3(d), while V_{OI+} shows high-pass characteristic in the view of $V_{\text{in}+}$, it also shows low-pass characteristics from the point of $V_{\text{in}-}$. Therefore, the linear combination of these characteristics leads to the all-pass operations shown in (2). The interesting point in (2), compared with (1), is that the Q is effectively divided by half, hence increasing the operation bandwidth, because of the elimination of a redundant series L-C during the differential transform. The differential I/Q network shows $|V_{OI\pm}| = |V_{OQ\pm}|$ for all ω and orthogonal phase splitting at $\omega = \omega_o$, which is the double-pole frequency of (2) when Q = 1.

2) Bandwidth Extension: A slight lowering of the Q from 1 can split the double-pole into two separate negative real poles. The equations in (3) show the poles and zeroes of the transfer functions, where $\omega_{\text{P}\pm}$ are the two left half-plane poles, and $\omega_{ZI\pm}$ and $\omega_{ZQ\pm}$ are the zeroes of the I- and Q-path transfer functions, respectively. The symmetric zero locations between the transfer functions can ensure equal I/Q amplitude for all ω. For the quadrature phase splitting between the I- and Q-paths at a frequency of ω_{IQ}, the difference of output phases contributed by each right half-plane zero of the transfer functions must be 45° at $\omega = \omega_{IQ}$. Another 45° contribution comes from the role of left half-plane zeroes at $\omega = \omega_{IQ}$. Equation (4) must therefore be satisfied, and the solutions are shown in (5).

$$\begin{pmatrix} \omega_{\text{P}\pm} = \left(-\frac{1}{Q} \pm \frac{1}{Q}\sqrt{1-Q^2}\right)\omega_o \\ \omega_{ZI\pm} = \left(-\frac{1}{Q} \pm \frac{1}{Q}\sqrt{1+Q^2}\right)\omega_o \\ \omega_{ZQ\pm} = \left(+\frac{1}{Q} \pm \frac{1}{Q}\sqrt{1+Q^2}\right)\omega_o \end{pmatrix}. \tag{3}$$

$$\underbrace{\tan^{-1}\left(\frac{\omega_{IQ}}{-\frac{\omega_o}{Q}+\frac{\omega_o}{Q}\sqrt{1+Q^2}}\right)}_{\substack{\text{output phase contribution} \\ \text{from } \omega_{ZI+}}} \underbrace{-\tan^{-1}\left(\frac{\omega_{IQ}}{+\frac{\omega_o}{Q}+\frac{\omega_o}{Q}\sqrt{1+Q^2}}\right)}_{\substack{\text{output phase contribution} \\ \text{from } \omega_{ZQ+}}} = 45^\circ. \tag{4}$$

$$\omega_{IQ} = \left(\frac{1}{Q} \pm \frac{1}{Q}\sqrt{1-Q^2}\right)\omega_o = -\omega_{\text{P}\pm}. \tag{5}$$

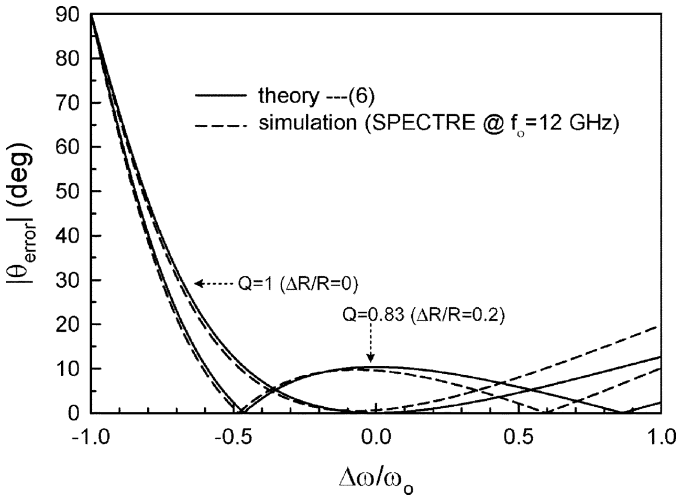


Fig. 4. I/Q phase error characteristics at the increase of R. $f_o = 12$ GHz, $L = 639$ pH ($Q_{\rm ind} = 18.6 @ 12$ GHz, $f_{\rm SR} = 50$ GHz), $C = 275$ fF and $R + \Delta R$; $R = 48.2, \Delta R/R = 0$ and $\Delta R/R = 0.2$.

It is noted that if Q < 1 in (5), which is possible by increasing R from the original value of $\sqrt{(L/C)}$, then one can obtain two frequencies where the QAF can generate an exact 90° phase difference between the I/Q outputs, extending the operation bandwidth further, and these two frequencies are identical to the pole frequencies of the I- and Q-path transfer functions. The phase error from the 90° relationships between $V_{OI\pm}$ and $V_{OQ\pm}$ at $\omega = \omega_o + \Delta\omega$, defined as $\theta_{\rm error} = 90° - |\angle V_{OI\pm} - \angle V_{OQ\pm}|$, can be expressed as

$$\theta_{\rm error} = 90° - 2 \times \tan^{-1}\left(\frac{\frac{1}{Q}\left(1+\frac{\Delta\omega}{\omega_o}\right)}{1+\frac{\Delta\omega}{\omega_o}+\frac{1}{2}\left(\frac{\Delta\omega}{\omega_o}\right)^2}\right) [\rm deg]. \quad (6)$$

$\Delta\omega$ is the offset frequency from the center frequency of ω_o.

Fig. 4 presents the simulation results of $\theta_{\rm error}$ according to $\Delta\omega/\omega_o$ for two cases of Q $= 1$ ($\Delta R/R = 0$) and Q $= 0.83$ ($\Delta R/R = 0.2$). ΔR means a net increment of R from the ideal value of $\sqrt{(L/C)}$. The simulations were done at $f_o = 12$ GHz by SPECTRE with process models, $L = 639$ pH ($Q_{\rm ind} = 18.6 @ 12$ GHz and $f_{\rm SR} = 50$ GHz), $C = 275$ fF, $R = 48.2\ \Omega$, given by the IBM 0.13-μm CMOS technology. The theoretical values agree well with simulations. The discrepancy at high frequencies is due to the limited $Q_{\rm ind}$ of the given inductor. Theoretically, one can achieve less than 5° of $\theta_{\rm error}$ from -35% to about $+50\%$ variation of $\Delta\omega$ with Q $= 1$. However, this error frequency range can be increased further with a slight increase of R. Typically, a 10% increment of R exhibits less than 5° of $|\theta_{\rm error}|$ over $-0.5 \sim 0.65$ of $\Delta\omega/\omega_o$. The penalty in this bandwidth extension by the pole-splitting technique is a small reduction of voltage gain which can be given as $\sqrt{(1+Q^2)}$ at ω_o. For example, when Q is 0.83, the gain is 0.7 dB lower from the ideal 3 dB voltage gain at $\omega = \omega_o$, and is acceptable for most applications.

It is also noteworthy that the effective decrement of Q by half in the QAF makes possible a real value of input impedance over a wider bandwidth and facilitates impedance matching. With input matched *differentially* to R, the input reflection coefficient ($= \Gamma$) at $\omega = \omega_o + \Delta\omega$ can be given as

$$|\Gamma| = \left|\frac{R - Z_{\rm in}}{R + Z_{\rm in}}\right|,$$
$$Z_{\rm in} = R\left\{1 + j\frac{Q}{2}\left(\left(1+\frac{\Delta\omega}{\omega_o}\right) - \left(1+\frac{\Delta\omega}{\omega_o}\right)^{-1}\right)\right\}. \quad (7)$$

Within $-45\% \sim 80\%$ variation of $\Delta\omega$, (7) results in $|\Gamma| < 0.3$, corresponding to roughly below -10 dB input return loss over more than 100% bandwidth.

3) Loading Effect: It is worthwhile to consider the errors caused by the loading effects on the QAF, which we have deliberately ignored for simplicity. Fig. 5 addresses this problem conceptually in a single-ended manner, where the parasitic loading capacitance C_L, mainly originated from the input gate capacitance of a transistor in the next stage, can modify the output impedances of Z_{OI} ($R + j\omega L$) and Z_{OQ} ($R + 1/j\omega C$) differently. Intuitively, C_L will lower the loaded Q of a high-pass network, Z_{OI}, hence increasing the resistance and decreasing the inductance of Z_{OI}. Also, C_L will reduce the resistance and increase capacitance of the low-pass network, Z_{OQ}, hence effectively increasing the loaded Q. The by-products of these impedance modifications by C_L are the degradation of Γ and quadrature errors at the output. The phase and amplitude errors from this loading effect will be mainly dependent on the ratio of C_L/C ($= \alpha$), as given in (8) and (9), respectively, for the case of the single-ended I/Q network. The $\Phi_{\rm error}$ is defined in the same manner as $\theta_{\rm error}$ and $A_{\rm error} = |20 \times \log(V_{OI}/V_{OQ})|$ at $\omega = \omega_o$.

$$\Phi_{\rm error} = 90° - \left(\tan^{-1}\left(1 - 2\frac{C_L}{C}\right) + \tan^{-1}\left(1 + 2\frac{C_L}{C}\right)\right) [\rm deg]. \quad (8)$$

$$A_{\rm error} = 10 \times \log\left(\frac{1 + 2\frac{C_L}{C} + 2\left(\frac{C_L}{C}\right)^2}{1 - 2\frac{C_L}{C} + 2\left(\frac{C_L}{C}\right)^2}\right) [\rm dB]. \quad (9)$$

The all-pass mode differential configuration can suppress these errors because any output node impedance in Fig. 3(d) is composed of low-pass and high-pass networks as mentioned, and provides counterbalances on the effect of C_L. Fig. 6 shows the simulation results of the quadrature errors caused by C_L at $f = f_o = 12$ GHz for the single-ended and differential QAF, along with the theoretical values evaluated from (8) and (9). For the most practical range of α ($\ll 1$), the differential I/Q network can reduce $\Phi_{\rm error}$ by more than half of that from the single-ended one, and the slope of $A_{\rm error}$ is much smaller in the differential case than in the single-ended one.

As the capacitance of the QAF becomes smaller with increasing operating frequencies, α can go up to moderate values for millimeter-wave applications, causing substantial errors. The lower impedance design of the QAF, where C can be increased while C_L kept constant, hence diminishing α, can relieve this potential problem at the expense of more power

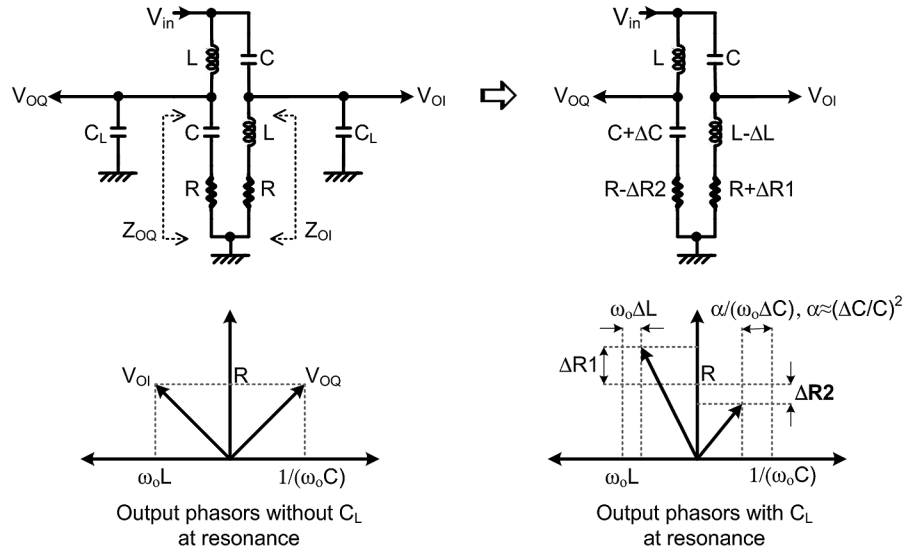


Fig. 5. Single-ended I/Q network under capacitive loading.

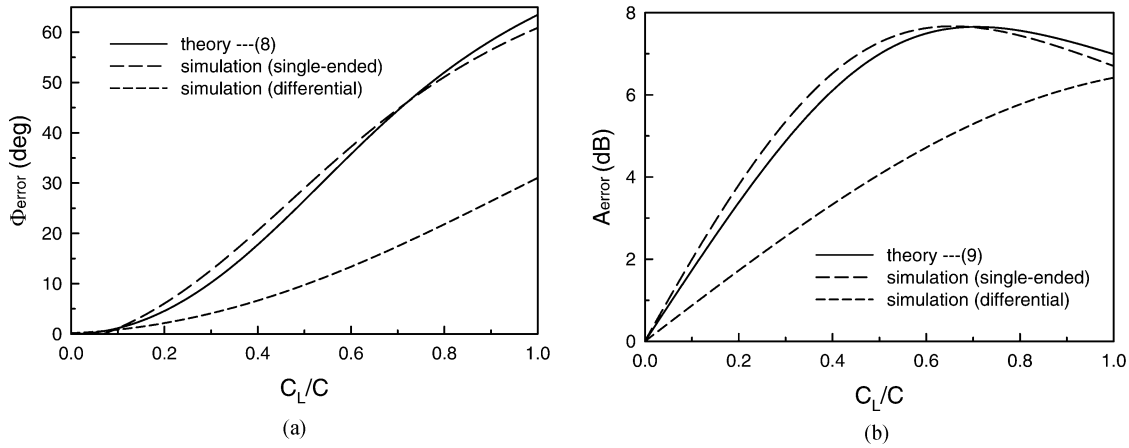


Fig. 6. Quadrature errors from the loading effect of C_L at $f = f_o = 12$ GHz. (a) Phase error. (b) Amplitude error. All simulations were done by SPECTRE with foundry passive models ($L = 639$ pH ($Q_{\rm ind} = 18.6$ @ 12 GHz, $f_{\rm SR} = 50$ GHz), $C = 275$ fF and $R = 48.2\ \Omega$.

consumption for driving the low impedance from the previous stage of the QAF. Another appropriate solution is to insert a source follower after the QAF, which will minimize C_L from the gate of an input transistor of the following stage.

In this work, for the X- and K*u*-band phase shifter, the QAF is designed with differential 50 Ω [$2R = 100\ \Omega$ in Fig. 3(d)] for impedance matching with the previous stage. For $f_o = 12$ GHz, the final optimized values of L and C through SPECTRE simulations are $L = 698$ pH ($Q_{\rm ind} = 18$ @ 12 GHz) and $C = 300$ fF. This takes into account about 70 fF of input pad capacitance and 50 fF of C_L which includes the input capacitance of the following stage (a differential adder) and the parasitic layout capacitance. For the K-band phase shifter, the optimized passive component values are $L = 296$ pH ($Q_{\rm ind} = 17.6$@24 GHz), $C = 153.5$ fF and $R = 47.5\ \Omega$ [$2R = 95\ \Omega$ in Fig. 3(d)]. The inductors are realized incorporating the parasitic layout inductance using the foundry models with full-wave electromagnetic simulations. With all the parasitic capacitances, Monte Carlo simulations assuming Gaussian distributions of $\Delta L_p/L$ ($\pm 5\%$), $\Delta C_p/C$ ($\pm 5\%$) and $\Delta R_p/R$ ($\pm 10\%$), show about a maximum $\pm 5^\circ$ of quadrature phase error within $\pm 1\sigma$ statistical variations at 12 GHz. Within $\pm 3\sigma$ variations, the maximum I/Q phase error is $\pm 15^\circ$ and I/Q amplitude mismatch is 1.2 ± 0.3 dB for the X- and K*u*-band QAF. For the K-band design, the phase error distribution is $-5^\circ \sim 13^\circ$ within $\pm 1\sigma$ variations at $f_o = 24$ GHz. Within $\pm 3\sigma$ variations, the phase error ranges from -15° to $+18^\circ$ and amplitude mismatch is 2.3 ± 0.6 dB, which are just enough for distinguishing 22.5° of phase quantization levels.

B. Analog Differential Adder

Fig. 7(a) shows the analog differential *signed*-adder, which adds the V-I converted I- and Q-input from a QAF together in the current domain at the output node, synthesizing the required phase. The size of the input transistors $M_{1\text{–}8}$ ($W/L = 40/0.12$) is optimized through SPECTRE simulations with respect to the linearity. The polarity of each I/Q input can be reversed by switching the tail current from one side to the other with

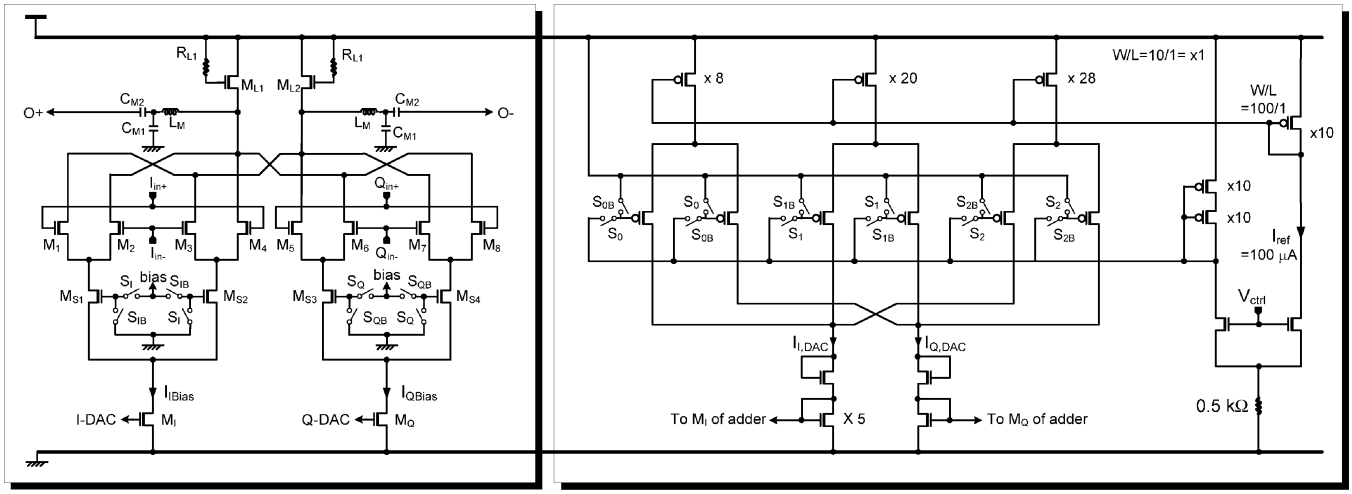


Fig. 7. (a) Analog differential adder with output impedance matching networks. (b) Three-bit differential DAC for bias current controls of the adder.

switches S_I/S_{IB} and S_Q/S_{QB}. As the phase shifter is designed to be integrated with multiple arrays on-chip, the small form factor is a critical consideration, leading to the use of an active inductor load composed of $M_{L1\text{–}2}$ and $R_{L1\text{–}2}$, instead of an on-chip spiral inductor. The equivalent output impedance from the active inductor load can be expressed as $R_{\rm eq}+j\omega L_{\rm eq}$, where $R_{\rm eq}=1/g_m$, $L_{\rm eq}=R_{L1,2}\times(C_{\rm gs}+C_{\rm gd})/g_m$ [29]. The $C_{\rm gs}$ and $C_{\rm gd}$ are gate-source and gate-drain parasitic capacitances of $M_{L1\text{–}2}$, respectively, and g_m is the transconductance of $M_{L1\text{–}2}$, expressed as $g_m=\sqrt{\{\mu_{\rm eff}C_{\rm ox}{\rm W}/L\times(I_{I\rm Bias}+I_{Q\rm Bias})\}}$. For measurement purposes only, L_M, C_{M1}, and C_{M2} constitute a wideband 50 Ω matching T-network (differentially 100 Ω) of which maximum circuit node Q looking toward the 50 Ω load from the matching network is less than 1.

For the X- and Ku-band phase shifter, the total bias current ($=I_{I\rm Bias}+I_{Q\rm Bias}$) in the differential adder is 5 mA from a 1.5 V supply voltage. This provides roughly $R_{\rm eq}\approx 30\ \Omega$ and $L_{\rm eq}\approx 1.3$ nH ($Q_{\rm ind}\approx 3.2$ @ 12 GHz) from the active inductor load with $R_{L1\text{–}2}=500\ \Omega$ and ${\rm W}/L=100/0.12$ of $M_{L1\text{–}2}$. In the SPECTRE simulations including I/O pad parasitics, the phase shifter shows $-2\sim 0$ dB of differential voltage gain at 5-20 GHz. The peak gain variance is less than 2.4 dB and the worst case phase error at 12 GHz is less than 5.2° for all 4-bit phase states. The phase shifter achieves typically −4.7 dBm of input $P_{1\rm dB}$ at 12 GHz. The S_{11} is below −10 dB at 8–16.7 GHz and S_{22} is less than −10 dB at 6.7–16 GHz with $L_M=691$ pH ($Q_{\rm ind}=18.5$ @ 12 GHz), $C_{M1}=76.8$ fF and $C_{M2}=535$ fF.

For the K-band phase shifter, with 7 mA of DC current in the adder, and with $R_{L1\text{–}2}=430\ \Omega$ and ${\rm W}/L=50/0.12$ of $M_{L1\text{–}2}$ ($R_{\rm eq}\approx 38\ \Omega$ and $L_{\rm eq}\approx 930$ pH), the differential voltage gain is $-6\sim -2.5$ dB at 15-30 GHz in simulations. At 24 GHz, the peak gain error is less than 3.5 dB and the peak phase error is less than 9.5° for all phase bits. The input $P_{1\rm dB}$ at 24 GHz is −1.3 dBm. The S_{11} is less than −10 dB at 15–33 GHz and S_{22} is below −10 dB at 15–28.2 GHz with $L_M=364$ pH ($Q_{\rm ind}=17.2$ @ 24 GHz), $C_{M1}=87.5$ fF and $C_{M2}=535$ fF in the SPECTRE simulations.

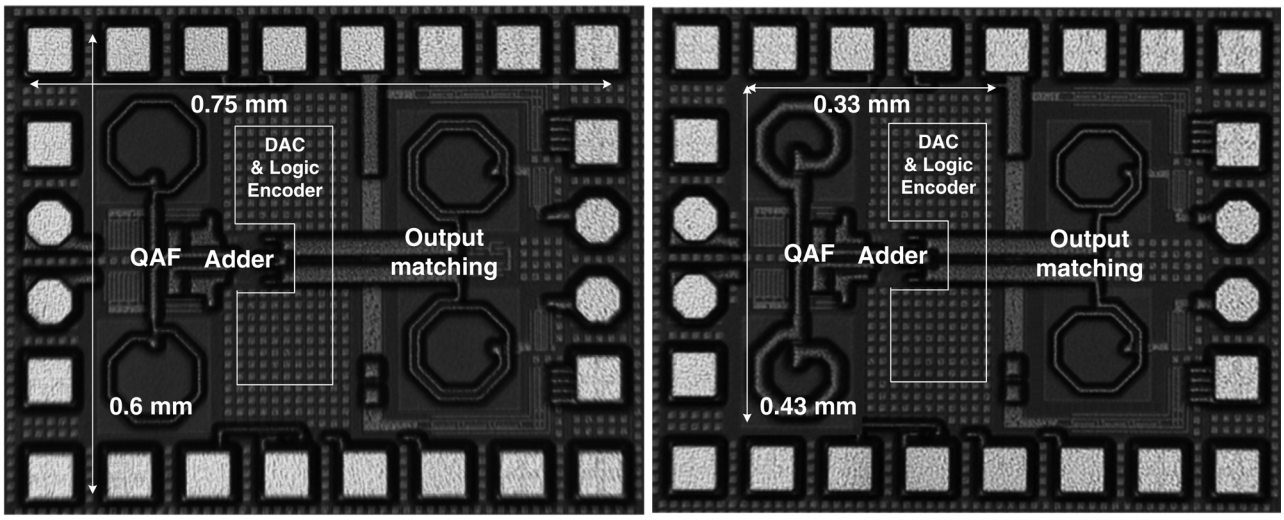
TABLE I
LOGIC MAPPING TABLE FOR THE SWITCH CONTROLS

4-bit Input ABCD	Output Phase	Adder S_I	Adder S_Q	DAC S_0	DAC S_1	DAC S_2	Control Logics
0000	0°	+	x	+	+	+	
0001	22.5°	+	+	−	+	+	$S_I=AB+\overline{A}\,\overline{B}$
0010	45°	+	+	−	−	+	
0011	67.5°	+	+	+	−	−	$S_Q=\overline{A}$
0100	90°	x	+	−	−	−	
0101	112.5°	−	+	+	−	−	$S_0=\overline{B}CD+\overline{B}\,\overline{C}\,\overline{D}+B\overline{C}\,\overline{D}$
0110	135°	−	+	−	−	+	
0111	157.5°	−	+	−	+	+	$S_1=\overline{B}\,\overline{C}+BCD$
1000	180°	−	x	+	+	+	
1001	202.5°	−	−	−	+	+	$S_2=C\overline{D}+\overline{B}\,\overline{C}+BCD$ $=S_1+C\overline{D}$
1010	225°	−	−	−	−	+	
1011	247.5°	−	−	+	−	−	
1100	270°	x	−	−	−	−	
1101	292.5°	+	−	+	−	−	
1110	315°	+	−	−	−	+	
1111	337.5°	+	−	−	+	+	

x=DON'T CARE, +=HIGH, −=LOW

C. DAC

The gain controls of the I- and Q-path of the adder for 4-bit phase resolution can be achieved by changing the bias current ratios between the two paths. For instance, a 6:1 ratio between $I_{I\rm Bias}$ and $I_{Q\rm Bias}$ results in $\sqrt{6}$:1 g_m ratio between the I- and Q-paths of the adder based on the long channel model, leading to an output phase of $\tan^{-1}(1/\sqrt{6})\approx 22.2°$, which is a good approximation for low-level gate overdriving and well matched with the simulation results. This is only 0.3° error from the 4-bit resolution, indicating that the phase shifter can achieve a high accuracy by simple DC bias current controls. A current-mode differential DAC shown in Fig. 7(b) sets the bias current ratios



(a) (b)

Fig. 8. Chip microphotograph. (a) X- and Ku-band phase shifter. (b) K-band phase shifter.

of the I- and Q-paths of the adder through mirroring to the current source of $M_{I,Q}$ for 4-bit phase synthesis. Table I shows the control logics for the pMOS switches S_0, S_1, and S_2 in the DAC, and nMOS switches S_I and S_Q in the adder. "+" means logically *high* (= *on*-state) and "−" is logically *low* (= *off*-state). S_{nB}, where $n = I$, Q, 1, 2, and 3, is just the logic inversion of S_n.

The differential architecture of the phase shifter causes the 0°-bit, 22.5°-bit, and 45°-bit to be fundamental bits, as the others can be obtained by reversing the switch polarities of these bits in the adder and/or in the DAC (see Table I). It should be also emphasized that the logic and scaling of current sources of the DAC are set such that for all 4-bit phase states, the load current in the adder keeps a constant value, i.e., $I_{I\mathrm{Bias}} + I_{Q\mathrm{Bias}} = constant$ for all phase bits. This results in a constant impedance of the active inductor load, and the same amplitude response proportional to $\sqrt{(I_{I\mathrm{Bias}} + I_{Q\mathrm{Bias}})}$ for all phase states. For instance, for all the cases of 0°-bit, 22.5°-bit, and 45°-bit, the scaling factors of the output load current in the adder have the same values of $5.6 \times I_{\mathrm{ref}}$ and the gain can be expressed as $\kappa \times \sqrt{(5.6 \times I_{\mathrm{ref}})}$, where κ is a constant determined by a transistor size of $M_{1\text{–}8}$, process parameters such as μ_{eff} and C_{ox}, load impedance and current mirroring ratio from DAC to adder. To improve current matching, the DAC is designed with long channel CMOS ($L = 1$ μm). The control logics are implemented with static CMOS gates.

IV. Experimental Results and Discussions

The phase shifters are realized in IBM 0.13-μm one-poly eight-metal (1P8M) CMOS technology. To improve signal balance, all the signal paths have symmetric layouts. The fabricated die microphotographs are shown in Fig. 8. The core size excluding output matching networks for both phase shifters is 0.33×0.43 mm^2, and the total size including all the pads and matching circuits is 0.75×0.6 mm^2. The phase shifters are measured on-chip with external 180° hybrid couplers (Krytar, loss = 0.5–1.5 dB @ 5–26 GHz) for differential signal inputs and outputs. The balun loss is calibrated out with a standard differential SOLT calibration technique using a vector signal network analyzer (Agilent, PNA-E8364B).

As the input reflection coefficient is dominantly set by the quadrature network, a changing phase at the adder does not disturb the S_{11} characteristic. The S_{22} characteristics also do not change for different phase settings, as the output load currents are the same for all phase states, resulting in a constant output impedance from the active load as discussed. Fig. 9 displays the typical measurement results of the input and output return losses, together with the simulation curves. For X- and Ku-band phase shifters, the S_{11}, converted into differential 50 Ω reference using ADS, is below −10 dB from 8.5 GHz to 17.2 GHz. In differential 100 Ω reference, the phase shifter shows less than −10 dB of S_{22} in the 6.3–16.5 GHz range. For the K-band phase shifter, the measured S_{11} is below −10 dB at 16.8–26 GHz and the S_{22} is less than −10 dB at 17–26 GHz. The external 180° hybrid couplers limit the maximum measurement frequency for the K-band case.

A. QAF Characteristics

The measurement of the 0°-/180°-bit and 90°-/270°-bit at the final output of the phase shifters should reflect the QAF characteristics exactly (Fig. 10). The dashed curves correspond to simulations with 50 fF loading capacitance. For the QAF of the X- and Ku-band phase shifters, the peak I/Q phase error is less than 5.5° and gain error is less than 1.5 dB at 12 GHz. The 10° phase error frequency range is from 5.5–17.5 GHz. The peak I/Q gain error at 5–20 GHz is less than 2.4 dB. For the K-band QAF, the quadrature phase error varies from 2.7° at 15 GHz to a maximum of 15.2° at 26 GHz. The I/Q amplitude error of the K-band QAF is 1.76–3.3 dB at 15–26 GHz.

B. X- and Ku-Band Phase Shifters

For the X- and Ku-band phase shifters, Fig. 11(a) and (b) shows the frequency responses of the unwrapped insertion phases and insertion gains according to the 4-bit digital input

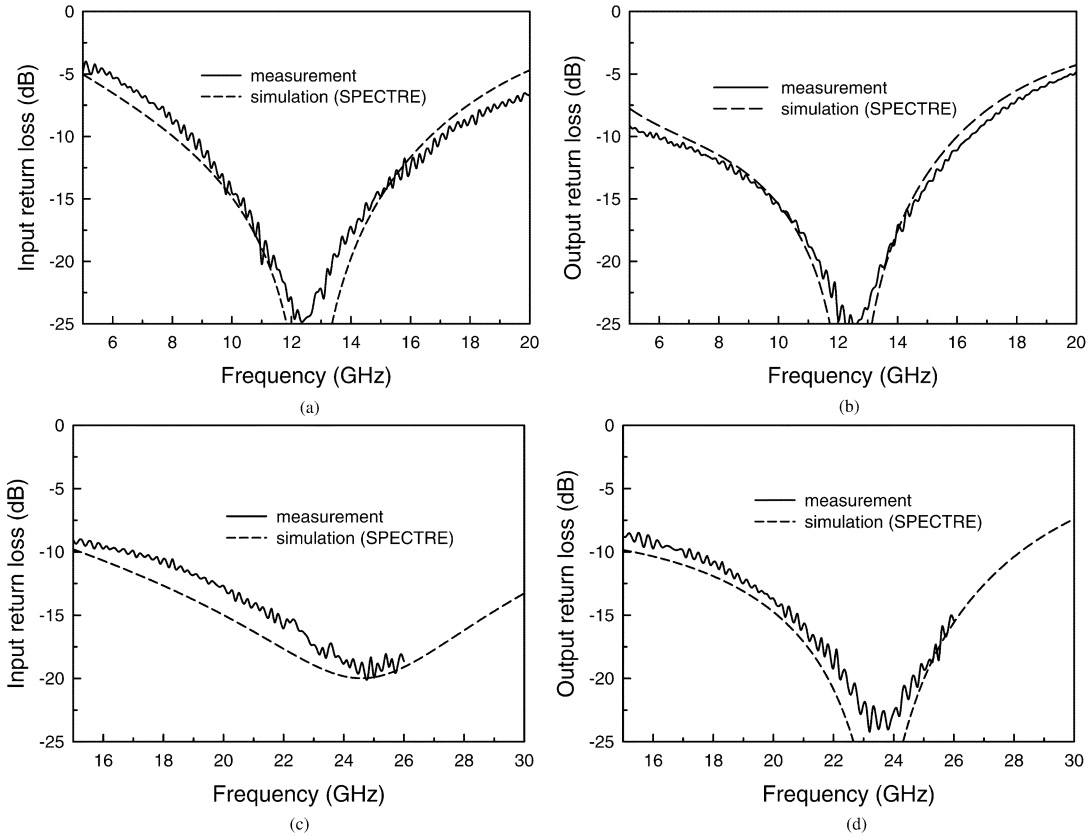


Fig. 9. Measured results of input and output return loss of the phase shifters. (a) S_{11} of the X- and K*u*-band phase shifter. (b) S_{22} of the X- and K*u*-band. (c) S_{11} of the K-band phase shifter. (d) S_{22} of the K-band phase shifter.

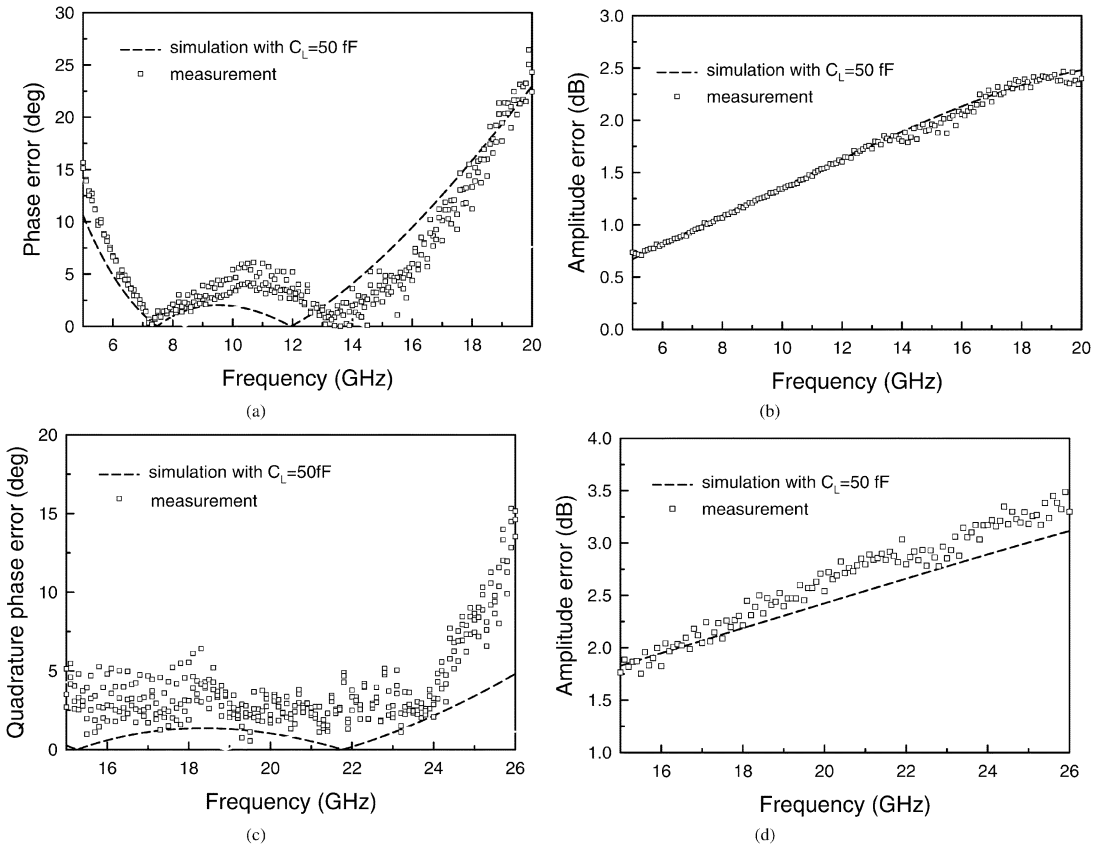


Fig. 10. Quadrature error characteristics of the I/Q networks measured at the output of the adder. (a) I/Q phase error of the X- and K*u*-band QAF. (b) I/Q amplitude error of the X- and K*u*-band QAF. (c) I/Q phase error of the K-band QAF. (d) I/Q amplitude error of the K-band QAF. All simulations were done with SPECTRE.

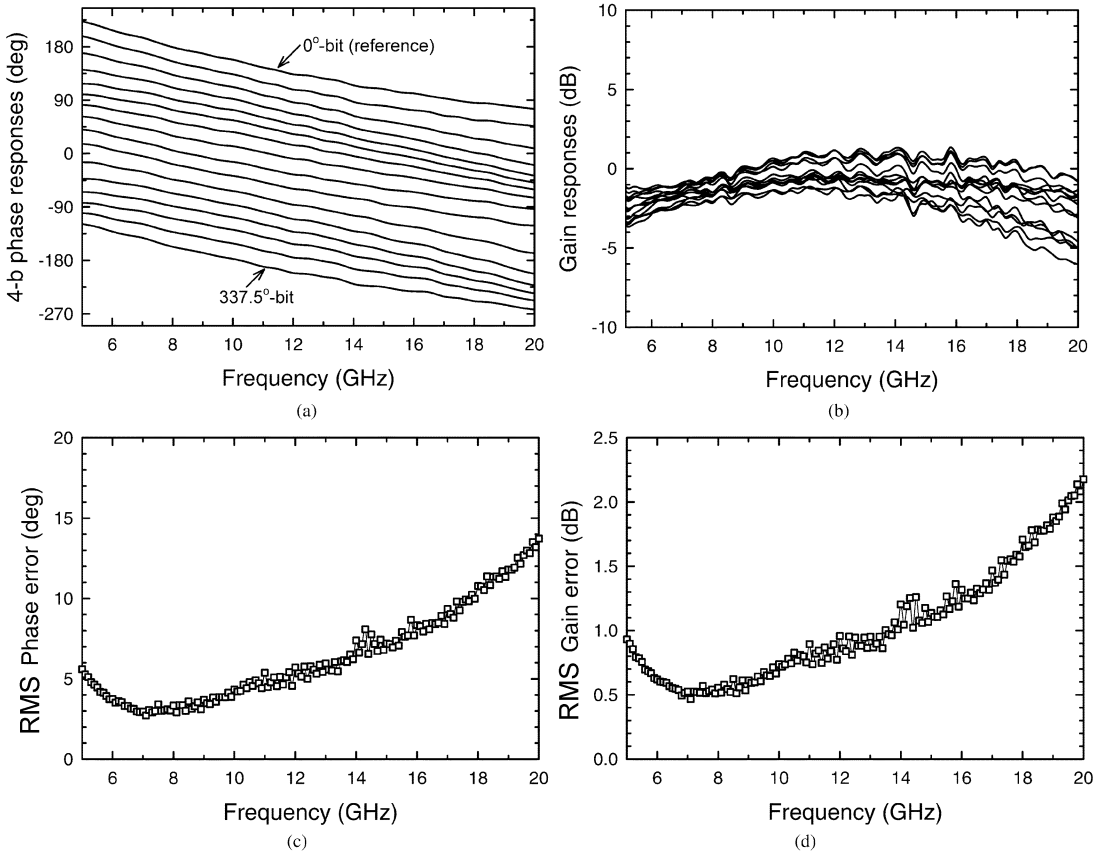


Fig. 11. Measured insertion phase and gain of the X- and K*u*-band phase shifter with 4-bit digital inputs. (a) Insertion phase. (b) Insertion gain. (c) RMS phase error. (d) RMS gain error.

codes, measured from 5 to 20 GHz. At 12 GHz, the measured peak-to-peak phase error is $-8.5^\circ \sim 9.1^\circ$ and the peak-to-peak insertion gain is $-1.5 \sim 1.2$ dB for all phase states. The average differential gain ranges from -3 dB at 20 GHz to -0.2 dB at around 11–12 GHz. The peak-to-peak gain variations are minimum 1.4 dB at 7 GHz and maximum 5.4 dB at 20 GHz. With reference to 0°-bit which comes from a 0000 digital input code, the RMS phase error can be defined as

$$\theta_{\Delta,\mathrm{RMS}} = \sqrt{\frac{1}{N-1} \times \sum_{i=2}^{N} |\theta_{\Delta i}|^2} \ (\mathrm{deg}) \tag{10}$$

where $N = 16$ and $\theta_{\Delta i}$ means the ith output phase error from the ideal phase value corresponding to the ith digital input sequence in Table I. Similarly, the RMS gain error can be defined as

$$A_{\Delta,\mathrm{RMS}} = \sqrt{\frac{1}{N} \times \sum_{i=1}^{N} |A_{\Delta i}|^2} \ (\mathrm{dB}) \tag{11}$$

where $A_{\Delta i}\ (\mathrm{dB}) = A_{vi}\ (\mathrm{dB}) - A_{\mathrm{ave}}\ (\mathrm{dB})$. The A_{vi} is ith insertion gain in dB-scale corresponding to ith digital input order and A_{ave} is the average insertion gain in dB-scale also.

The RMS phase error and gain error, calculated at each measured frequency, are shown in Fig. 11(c) and (d), respectively. The phase shifter exhibits less than 5° RMS phase error from 5.3 GHz to about 12 GHz. The 10° RMS error frequency range goes up to 18 GHz, achieving 5-bit accuracy across more than 3:1 bandwidth. The RMS gain error is less than 2.2 dB for 5–20 GHz. The phase shifter achieves -5.4 ± 1.3 dBm of input $P_{1\mathrm{dB}}$ at 12 GHz for all 4-bit phase states with 5.8 mA of DC current consumption from a 1.5 V supply voltage.

C. K-Band Phase Shifter

Fig. 12(a) shows the measured insertion phases with 4-bit digital input codes of the K-band phase shifter. The insertion loss characteristics are shown in Fig. 12(b), and the RMS phase errors and gain errors versus frequency are presented in Fig. 12(c) and (d), respectively. The RMS phase error is 6.5°–13° at 15–26 GHz. The average insertion loss varies from -4.6 dB at 15 GHz to -3 dB at around 24.5–26 GHz. The peak-to-peak gain variations are minimum 3.3 dB at 15.4 GHz and maximum 6.3 dB at 25.6 GHz. The RMS gain error is less than about 2.1 dB from 15 to 26 GHz. As shown in Fig. 11(c) and (d) and in Fig. 12(c) and (d), the RMS phase errors versus frequency have strong correlations with the RMS gain error patterns versus frequency. This is a typical characteristic of the proposed phase shifter; because the output phase in the phase shifter is set by the gain factors of the I- and Q-

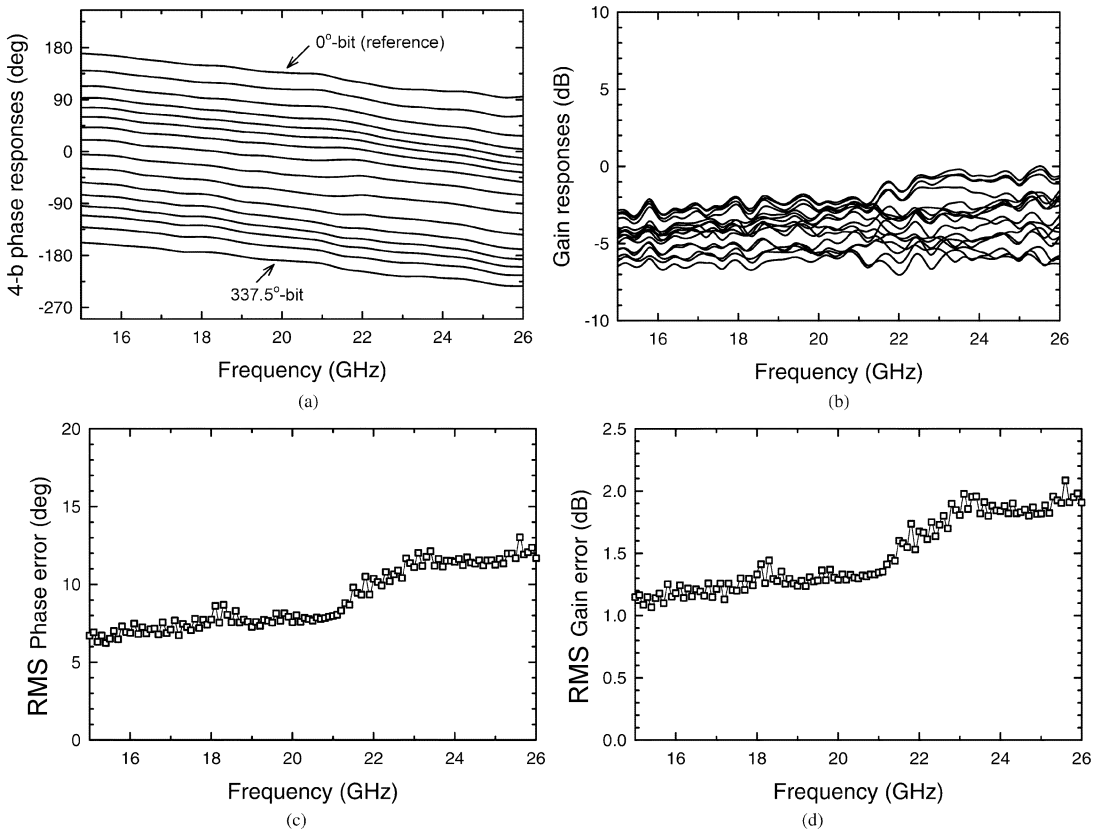


Fig. 12. Measured insertion phase and gain of the K-band phase shifter with 4-bit digital inputs. (a) Insertion phase. (b) Insertion gain. (c) RMS phase error. (d) RMS gain error.

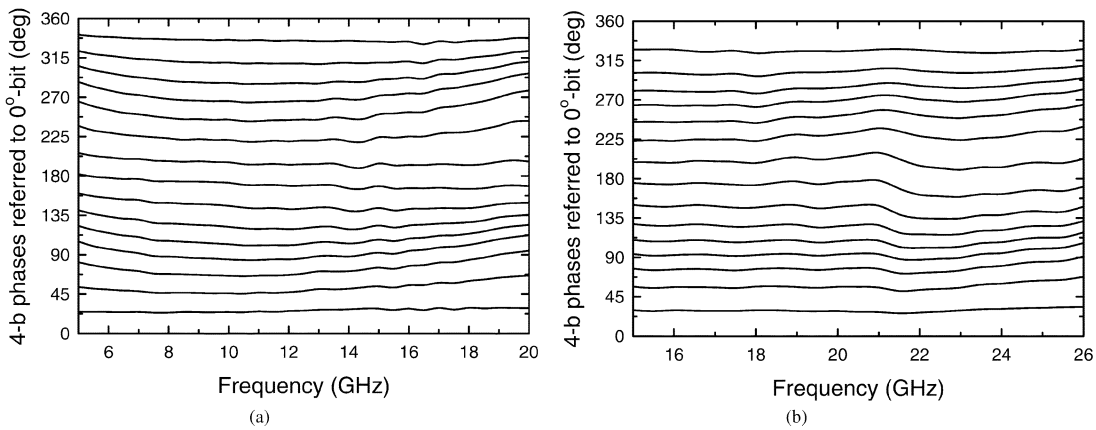


Fig. 13. Measured 4-bit phases referred to 0°-bit. (a) X- and K*u*-band phase shifter. (b) K-band phase shifter.

input of the adder, any gain error indicates the scale of the phase error. The measured input $P_{1\mathrm{dB}}$ is -0.8 ± 1.1 dBm for all phase states at 24 GHz. The total current consumption is 7.8 mA from a 1.5 V supply voltage.

Finally, the 0°-bit response is subtracted from all the measured 4-bit phase responses and the results show nearly constant 4-bit phase shift versus frequency for each phase shifter (Fig. 13). These results also imply that although the phase accuracy is dependent on the accuracy of the I/Q network, the phase shifter can guarantee the output phase monotonicity versus input digital control sequences, one of the fundamental merits of the active phase shifters over passive designs. All the measured results are summarized in Table II.

V. Conclusion

In this work, we demonstrate 0.13-μm CMOS 4-bit active digital phase shifters for X-, K*u*-, and K-band multiple antenna array applications. The fundamental operation of the active phase shifters is to interpolate the phases of the quadrature input signals by adding two I/Q inputs. Resonance-based differential quadrature networks are developed to minimize loss and to increase the operating bandwidth with excellent signal

TABLE II
PERFORMANCE SUMMARIES OF THE PHASE SHIFTERS

Quantity	Measured Results	
Technology	0.13-μm CMOS (1P8M)	
Phase resolution	4-bit	
Frequency band	X- and K*u*-band (6-18 GHz)	K-band (15-26 GHz)
Power consumption	8.7 mW (I_{DC}=5.8 mA, V_{DC}=1.5 V)	11.7 mW (I_{DC}=7.8 mA, V_{DC}=1.5 V)
Insertion gain (*ave.*)	-2.1 ~ -0.2 dB (max @11 GHz, min @6 GHz)	-4.6 ~ -3 dB (max @24.6 GHz, min @15 GHz)
Phase error (*rms*)	2.7 ~ 10° (max @18 GHz, min @7 GHz)	6.5 ~ 13° (max @25.6 GHz, min @15 GHz)
Gain error (*rms*)	0.5 ~ 1.7 dB (max @18 GHz, min @7 GHz)	1.1 ~ 2.1 dB (max @25.6 GHz, min @15 GHz)
Input P1dB	-5.4 (+/- 1.3) dBm @ 12 GHz	-0.8 (+/- 1.1) dBm @ 24 GHz
Input return loss	< -10 dB @ 8.5-17.2 GHz	< -10 dB @ 16.8-26 GHz
Output return loss	< -10 dB @ 6.3-16.5 GHz	< -10 dB @ 17-26 GHz
Chip area	0.33 x 0.43 mm^2 (core) 0.75 x 0.6 mm^2 (including pads)	

precision in the phase shifters. The measured characteristics are well matched with theory and simulations from SPECTRE. The core size of the integrated phase shifters with all digital control circuitry is 0.33×0.43 mm^2, which is a very small area. With all the performance figures, power consumption and size, the proposed active CMOS phase shifters are excellent candidates for integrated phased array systems.

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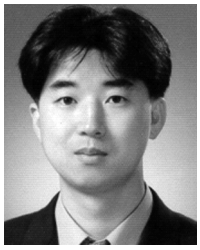

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Prof. Rebeiz is an IEEE Fellow, an NSF Presidential Young Investigator, an URSI Koga Gold Medal Recipient, an IEEE MTT Distinguished Young Engineer (2003), is the recipient of the IEEE MTT 2000 Microwave Prize. He also received the College of Engineering Teaching Award, the 1998 Eta-Kappa-Nu Professor of the Year Award, and the 1998 Amoco Teaching Award given to be best undergraduate teacher, all at the University of Michigan. He has been an Associate Editor of IEEE MTT (2000–2003), and a Distinguished Lecturer for IEEE MTT and IEEE AP societies. He leads a group of 18 Ph.D. students at UCSD in the area of mm-wave RFIC, microwaves circuits, RF MEMS, planar mm-wave antennas and terahertz systems.