A Tunable All-Pass MMIC Active Phase Shifter

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***Abstract*—This paper describes a novel structure for a monolithic-microwave integrated-circuit active phase shifter based on a bridge all-pass network. The design procedure has been developed, leading to a fixed-frequency circuit with large tunable phase variation, associated to a low-gain ripple, and requiring nearly no design optimization. Simulated results predicted an analog tunable 180° phase variation, at 5-GHz operation frequency. The circuit was implemented using GEC-Marconi pseudomorphic high electron-mobility transistor H40 technology, and measured results validated the proposed design method and circuit structure.**

***Index Terms*—All-pass filter, HEMT, microwave, MMIC, monolithic circuit, phase shifter.**

I. Introduction

MANY communication and radar systems are based on phased-array antennas for achieving electronic beam control and fast beam scanning [1]–[3]. Such systems can be used for military (e.g., missile interceptors) and commercial applications, such as flight control, collision avoidance, and the global positioning system (GPS) [4], [5].

Satellites systems also require phased arrays for producing multiple spot beams, providing more efficient use of transmitted power [6]. A typical application is found in several mobile satellite systems that employ multiple beam configuration, which provides more efficient area distribution [7], [8].

A phased-array system is composed of a large amount of receiver and transmitter elements that includes: 1) the antenna elements; 2) amplifier circuits; 3) combiners; 4) power dividers; and 5) phase shifters. Technological trends in their implementation point toward the integration of the passive and active devices with the radiating elements on the same GaAs substrate monolithic microwave integrated circuits (MMICs). This integration is necessary when frequency becomes high and the circuits must be small and light, presenting high reliability and reproducibility, as well as efficient use of dc power and decreasing cost [6].

One of the most important circuits in phased-array systems is the phase shifter, which electronically controls the phase of the transmitted or received microwave signals from the radiating array elements, causing the effect of beam scanning or multiple beam distribution. Phase shifters are also used in other microwave systems such as power splitters [9]–[11], frequency converters [12], active baluns [13], [14], and phase modulators [15].

In this paper, a novel structure for a monolithic phase shifter is presented. Its topology is derived from a passive balanced all-pass network. This network was modified in order to accommodate for active circuitry.

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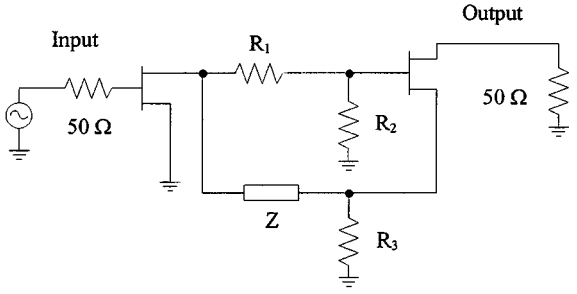

Fig. 1. All-pass filter topology.

II. Circuit Configuration

The phase-shifter circuit topology is derived from an all-pass filter configuration. The active all-pass network proposed in [16] has been studied: such a circuit was originally designed for a fixed insertion phase, and required an optimization process in order to achieve gain flatness over the desired bandwidth. The gain ripple is due to the parasitic elements of nonideal components, e.g., the Cgs and Cgd capacitances of a high electron-mobility transistor (HEMT).

We modified the network presented in [16] so that a circuit with tunable phase variation could be obtained at a fixed frequency, associated with low-gain ripple, and requiring nearly no design optimization. This new topology is shown in Fig. 1.

The impedance Z is a series association of a capacitor and an inductor, and the HEMT transistors were modeled, in a preliminary analysis, as an ideal voltage-controlled current source (Fig. 2).

The transfer function of the circuit results as

$$S_{21} = K \cdot \frac{s^2 - \dfrac{R_1 \cdot R_3}{R_2 \cdot L} \cdot s + \dfrac{1}{L \cdot C}}{s^2 + \dfrac{R_1 + R_2 + R_3 + g_{m1} \cdot R_1 \cdot R_3}{L \cdot (1 + g_{m1} \cdot R_3)} \cdot s + \dfrac{1}{L \cdot C}}. \quad (1)$$

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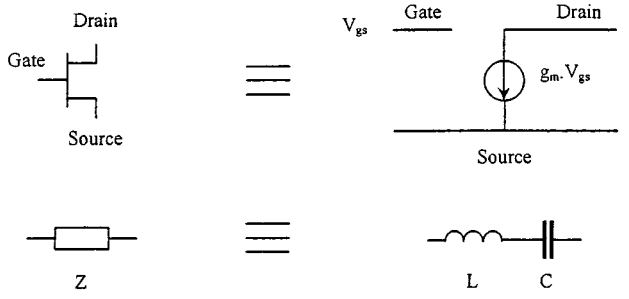

Fig. 2. Equivalent HEMT circuit and Z impedance.

The general second-order transfer function of an all-pass network is given by

$$T(s) = \frac{s^2 - \frac{\omega_0}{Q} \cdot s + \omega_0^2}{s^2 + \frac{\omega_0}{Q} \cdot s + \omega_0^2}. \tag{2}$$

The condition upon (1) to represent an all-pass network is given by

$$\frac{R_1 \cdot R_3}{R_2} = \frac{R_1 + R_2 + R_3 + gm1 \cdot R_1 \cdot R_3}{1 + gm1 \cdot R_3}. \tag{3}$$

Given $R2$, $R3$, R_{load} (50 Ω) R_{source} (50 Ω), g_{m1} (transconductance), Q, and ω_0 (frequency rad per seconds), we have

$$K = 2 \cdot g_{m1}^2 \cdot \frac{R_2 \cdot R_{\text{Load}}}{1 + g_{m1} \cdot R_3} \tag{4}$$

$$R_1 = -R_2 \cdot \frac{R_2 + R_3}{R_2 - R_3 - g_{m1} \cdot R_3^2 + g_{m1} \cdot R_2 \cdot R_3} \tag{5}$$

$$L = \frac{1}{\omega_0 \cdot R_2} \cdot Q \cdot R_1 \cdot R_3 \tag{6}$$

$$C = \frac{R_2}{R_1 \cdot R_3 \cdot Q \cdot \omega_0}. \tag{7}$$

Analyzing (2), it can be seen that there is a phase variation, which depends on the frequency (shown in Fig. 3). ω_0 is the natural frequency of the filter, and ω is the signal frequency. It can also be seen that there is no gain variation with frequency. For a fixed signal frequency, an all-pass network can operate as a variable phase shifter if its natural frequency (ω_0) is varied. Considering (1) as an all-pass network transfer function, the ω_0 frequency variation can be achieved by varying either the capacitance C or inductance L values.

In this study, the capacitance C was chosen as a phase element control. It can be seen in (1) that if the capacitance value is changed, the all-pass characteristic is maintained.

In practice, the variable capacitor can be implemented by using an HEMT with the drain and source connected, and varying the voltage applied to this terminal.

A schematics of the phase shifter using transistors is presented in Fig. 4.

III. Design

An important component in this design is the varactor. This component is the key element for phase variation and, in order to achieve the aimed range, its behavior was studied. The varactor was implemented using transistors with drain and source terminals connected, and a reverse bias was applied to the gate terminal. Several pseudomorphic high electron-mobility transistors (pHEMTs) 0.2-μm transistors with different dimensions (number of fingers and gatewidth) were simulated, and their capacitance variation was analyzed. Fig. 5 shows a schematics of a simulated varactor, with a positive bias voltage applied to the drain and source terminals, resulting in a reverse gate voltage. This voltage was varied from 2.5 to 6.5 V, as the gate terminal had a fixed 2.5-V bias voltage.

The simulation results are presented in Fig. 6, performed for transistors with the following dimensions: 2 × 60 μm (two fingers, and 60 μm length), 4 × 150 μm, 4 × 20 μm, 4 × 40 μm, and 4 × 60 μm.

It can be observed that the largest capacitance variation is achieved with the largest area pHEMT (4 × 150 μm). Its capacitance varies from 0.1 to 0.7 pF, for a 4-V control voltage variation.

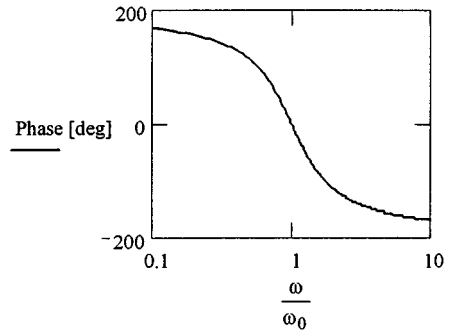

Fig. 3. All-pass phase variation versus frequency.

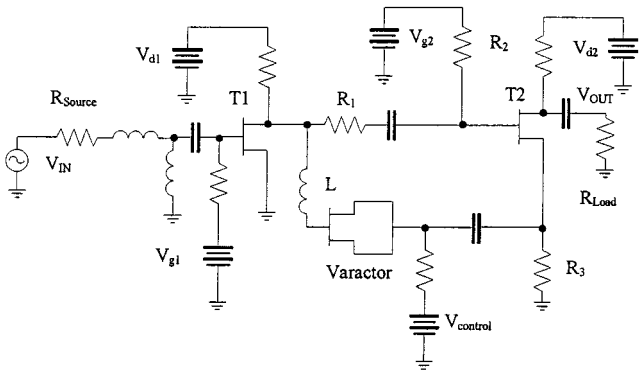

Fig. 4. Phase-shifter schematics.

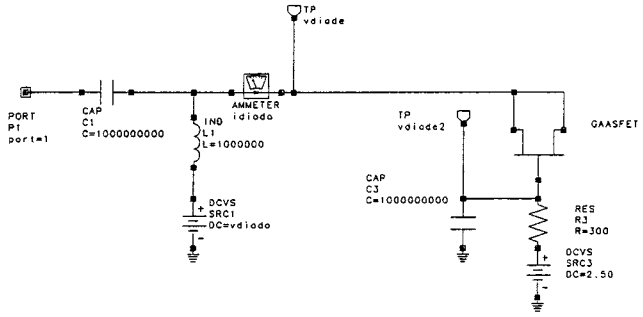

Fig. 5. Schematics of a simulated varactor.

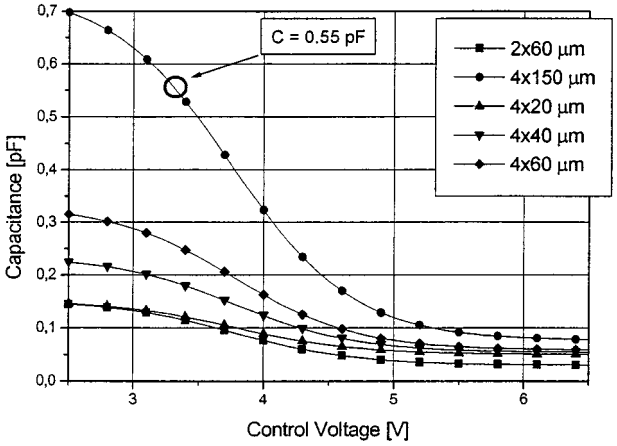

Fig. 6. Varactor simulation results.

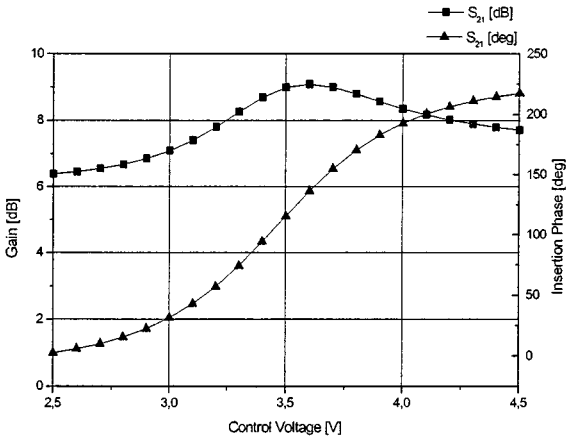

Fig. 7. Phase-shifter circuit simulation results.

In this design, low capacitance values were avoided because parasitic capacitances can load the varactor. These parasitic capacitances are due to transmission lines, transistors, and other circuit components. In order to overcome this problem, an appropriate value of the capacitance variation must be chosen.

A capacitance variation from 0.35 to 0.7 pF (1.5 V of the control voltage variation) was chosen, by using the 4×150 μm pHEMT, which means an average capacitance (Cv) of 0.55 pF.

In order to obtain a specific phase variation, an appropriate value of Q [see (2)] must be calculated. Using (7) and (5) results in

$$Q = \frac{R3 - R2 + g_{m1} \cdot R3^2 - g_{m1} \cdot R2 \cdot R3}{(R2 + R3) \cdot R3 \cdot \omega_0 \cdot Cv} \tag{8}$$

where Cv is the average capacitance value.

By setting values for $R2$, $R3$, and g_{m1}, Q can then be calculated, and the phase variation can be checked from (9) by replacing C for its minimum and maximum values

$$\phi = 2 \cdot \tan^{-1}\left[Q \cdot \left(\frac{1}{\sqrt{L \cdot C} \cdot \omega} - \sqrt{L \cdot C} \cdot \omega\right)\right]. \tag{9}$$

Imposing a phase variation of 180°, the circuit elements were calculated according to (3)–(8), with the following component and variable values set to:

$$\begin{aligned} R2 &= 20\ \Omega \\ g_{m1} &= 160\ \text{mS} \\ R3 &= 50\ \Omega \\ \text{Frequency} &= 5\ \text{GHz} \\ R\text{load} &= 50\ \Omega. \end{aligned}$$

That results in $R1 = 5.18\ \Omega$, $L = 1.84$ nH, $Q = 4.4$, and a gain of 15 dB.

The schematics of this circuit is shown in Fig. 4.

The transistors $T1$ and $T2$ (Fig. 4) were biased in order to obtain the adopted transconductance g_{m1} (160 mS): $V\text{ds} = 2.5$ V, $V\text{gs} = -0.8$ V, resulting in $I\text{ds} = 24$ mA. The transistors have dimensions of 4×150 μm.

High-value resistors were used in drain biasing to provide isolation between the phase shifter and external bias circuitry.

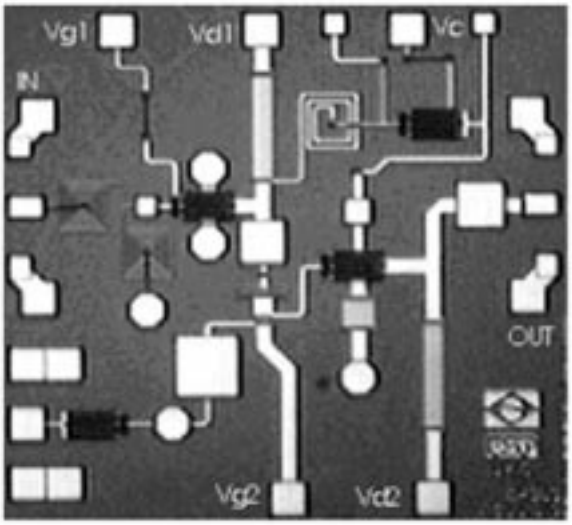

Fig. 8. Photograph of a phase-shifter MMIC.

Bias chokes were avoided because they occupy large areas of substrate and present undesirable parasitic effects.

Using the calculated component values and the transistor model given by the foundry, simulation of the phase shifter, as presented in Fig. 4, was performed and the results are shown in Fig. 7.

A summary of the simulated results for a variation of the control voltage from 2.5 to 4.5 V is

$$\begin{aligned} S_{21\_\max.} &= 9.1\ \text{dB} \\ \Delta S_{21} &= 2.7\ \text{dB} \\ \text{Phase insertion} &= 215^\circ \\ S_{11} &< -14.7\ \text{dB} \\ S_{22} &< -5.1\ \text{dB}. \end{aligned}$$

The layout of the MMIC phase shifter was constructed according to GEC-Marconi H40 design rules [17] (Fig. 8). The circuit was fabricated under multiuser scheme.

Fig. 9 shows a photograph of the constructed varactor diode, with details of the transistor drain and source terminals short circuited.

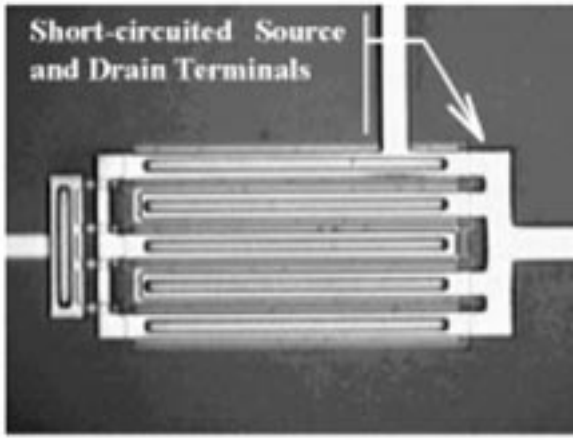

Fig. 9. Constructed varactor.

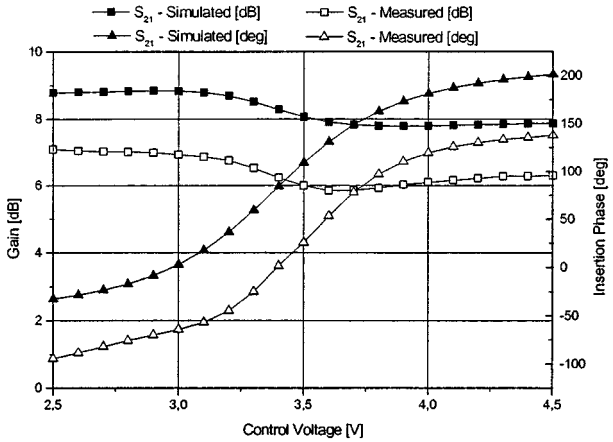

Fig. 10. Phase-shifter final simulation and measured results.

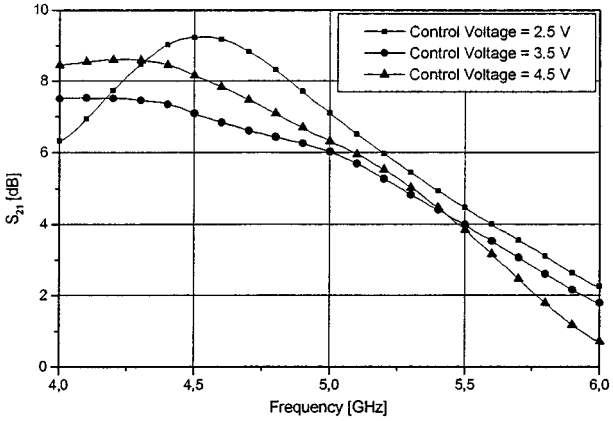

Fig. 11. Gain versus frequency.

Simulation and measured results of this final circuit (after layout design) are displayed in Fig. 10.

The simulated results can be summarized as follows for the same control voltage variation (2.5–4.5 V):

$$S_{21\_\max} = 8.8\ \text{dB}$$
$$\Delta S_{21} = 1\ \text{dB}$$
$$\text{Phase insertion} = 223.8^\circ$$
$$S_{11} < -3.6\ \text{dB}$$
$$S_{22\_} < -7.9\ \text{dB}.$$

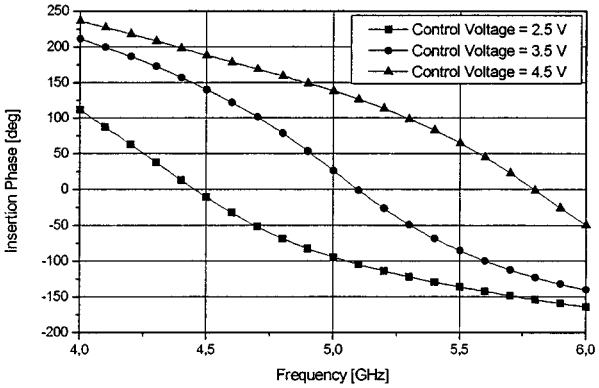

Fig. 12. Insertion phase versus frequency.

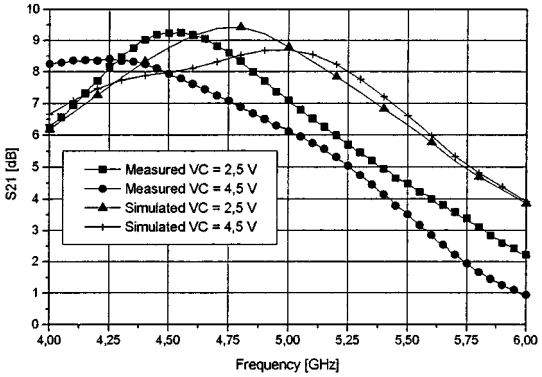

Fig. 13. Comparison between simulated and measured gain results.

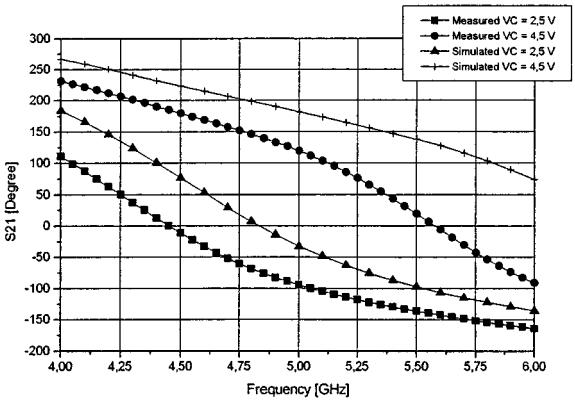

Fig. 14. Comparison between simulated and measured insertion phase results.

In our design approach, no optimization process was performed until layout construction. At this step, some transmission lines and bypass capacitors were tuned, aiming at decreasing the gain ripple.

The measured circuit results are presented in Fig. 10 compared to simulated curves, and a summary of the measured results is as follows:

$$S_{21\_\max} = 7.1\ \text{dB}$$
$$\Delta S_{21} = 1.3\ \text{dB}$$
$$\text{Phase insertion} = 232.4^\circ$$
$$S_{11} < -4.4\ \text{dB}$$
$$S_{22\_} < -2.4\ \text{dB}.$$

In Figs. 11 and 12, the phase-shifter measured performance with frequency and control voltage variations is presented. It

can be noticed that the largest insertion phase variation, associated with low-gain variation, occurs at the design frequency of 5 GHz.

Fig. 13 shows a comparison between simulated and measured gain results, and Fig. 14 shows a comparison between simulated and measured results for insertion phase. Both figures present results for two different control voltages.

IV. Conclusion

A novel structure for a tunable active MMIC phase shifter has been proposed and demonstrated. It employs a modified all-pass filter network, which produces a low-gain ripple. The design procedure for this structure has demanded only a few steps of optimization during layout construction.

A preliminary gain of 15 dB has been specified based on the circuit analysis when using ideal voltage-controlled current sources for representing the transistors. Final simulated results of the circuit indicated an average gain of 8.3 dB and measured average gain value was 6.5 dB.

These differences are mainly due to parasitic elements of the transistor (e.g., $C\mathrm{gs}$ and $C\mathrm{gd}$ capacitances), which change the ideal all-pass transfer function of the circuit. Other effects that move the gain function away from the ideal specification are impedance mismatch between the input transistor and the all-pass network and a non 180° phase difference between gate and drain terminals of the output transistor at the resonance frequency ω_0.

We also expect that the transistor model is not adequate for simulating the varactor performance with good precision, as the parameters' model are primarily fitted for the transistor linear region of operation.

An analog 232° of phase variation has been obtained from the constructed MMIC, at 5-GHz operation frequency, with the control voltage varying from 2.5 to 4.5 V. The measured gain was 6.5 ± 0.6 dB.

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