A 2.4–4-GHz Wideband 7-Bit Phase Shifter With Low RMS Phase/Amplitude Error in 0.5-μm GaAs Technology

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***Abstract*— This article presents a 2.4–4-GHz wideband 7-bit switch-type phase shifter (STPS) with a switch driver. Three switch-type phase shifting topologies are employed for the design of the phase shifter (PS), including the switched L/C structure, T-type structure, and high-/low-pass network. For minimizing the phase and amplitude deviations, an improved T-type structure with a switched filter structure has been proposed to boost the performance of the PS. Besides, a phase compensation cell also has been adapted to further decrease the phase error of the STPS. Based on the topology choice of each cell and the amplitude compensation among cells, a systematic design method is developed to extend the bandwidth of the PS. The proposed 7-bit STPS was implemented in the 0.5-μm GaAs pHEMT process. The measured root-mean-square (rms) phase error of the proposed STPS is less than 3.1° from 2.4 to 4 GHz and less than 1.5° at 2.8–3.7 GHz. The average insertion loss (IL) is 4.5–4.9 dB with an rms amplitude error of less than 0.34 dB. $IP_{1\,dB}$ is about 30 dBm. To the best of our knowledge, this PS achieves the highest resolution and the lowest rms amplitude error among the published GaAs/GaN PSs over a similar frequency band. The IL, bandwidth, and rms phase error of the proposed PS also show good performance.**

***Index Terms*— 0.5-μm GaAs, low root-mean-square (rms) phase/amplitude error, monolithic microwave integrated circuit (MMIC), S-band, wideband phase shifter (PS).**

I. Introduction

PHASE shifters (PSs) are key components of phased-array systems for radar, high-speed communication, and navigation applications. With the emergence of the fifth-generation (5G) and other high-speed communications, a higher requirement for the PS has been brought forward, which consists of high phase resolution, high phase accuracy, low insertion loss (IL), low IL variation, high linearity, and wide bandwidth. Due to the high quality factor of passives and low IL field-effect transistor (FET) switches in III-V technologies and silicon-on-insulator (SOI) processes, the monolithic microwave integrated circuit (MMIC) passive PSs fabricated by these technologies are attractive to meet the requirements for low IL and high linearity applications. Many efforts have been made to realize this kind of high-performance wideband PSs based on these advanced semiconductor processes [1]–[7].

To extend the operating bandwidth, the PS in [1] adopted modified switch-type phase shifting cells and optimized the cascade order of cells to achieve a 66.7% relative bandwidth. A tunable active inductor-loaded all-pass network has been designed in [2] to improve the bandwidth of the PS. In [3], an SOI PS has been reported; the input $P_{1\,dB}$ reached 29.6 dBm, which is comparable with the pHEMT-based product design. The compact size is attractive for phased-array systems. A GaN-based 5-bit PS with a control logic circuit on-chip is demonstrated for the first time in [4], which overcomes the issue of the negative control voltage. However, there are few reported PSs based on these processes considering improving phase accuracy and IL variation. The main reason is that the phase accuracy and IL variation are limited by unavoidable nonideal effects of the circuit structures presented in the above literature. Besides, as the number of metal layers in III-V technologies is usually very small, it is difficult to realize complex passive blocks and interconnection structures. Therefore, the methods of phase accuracy improvement and IL variation reduction, which is based on fine vector sum presented in [7]–[9], are unsuitable for III-V technologies. However, the phase accuracy and IL variation of PSs have a huge impact on the beam pointing and sidelobe rejection ratio of phased-array systems [10]–[12], and they are nonnegligible performances for PSs.

To address the design challenges of high phase accuracy and low IL variation, this article introduces a 2.4–4-GHz 7-bit switch-type PS (STPS) that employs three kinds of phase shifting topologies, and the configuration is shown in Fig. 1. An improved T-type phase shifting cell for reducing phase deviation and IL variation is proposed, and a systematic design method is also developed based on topology choice and the amplitude compensation, so as to achieve low IL, low root-mean-square (rms) phase/amplitude error, and broad bandwidth simultaneously. The proof-of-concept STPS is implemented in the 0.5-μm GaAs pHEMT process.

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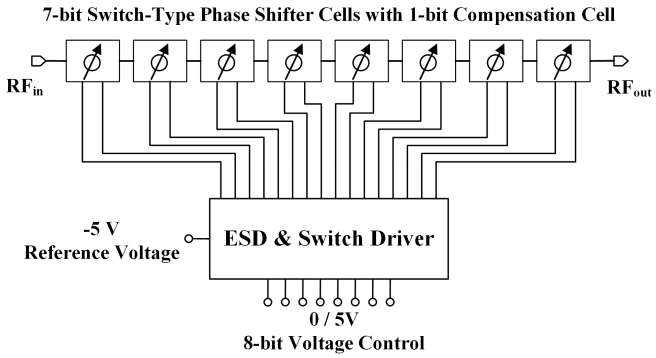

Fig. 1. Configuration of the proposed 7-bit PS.

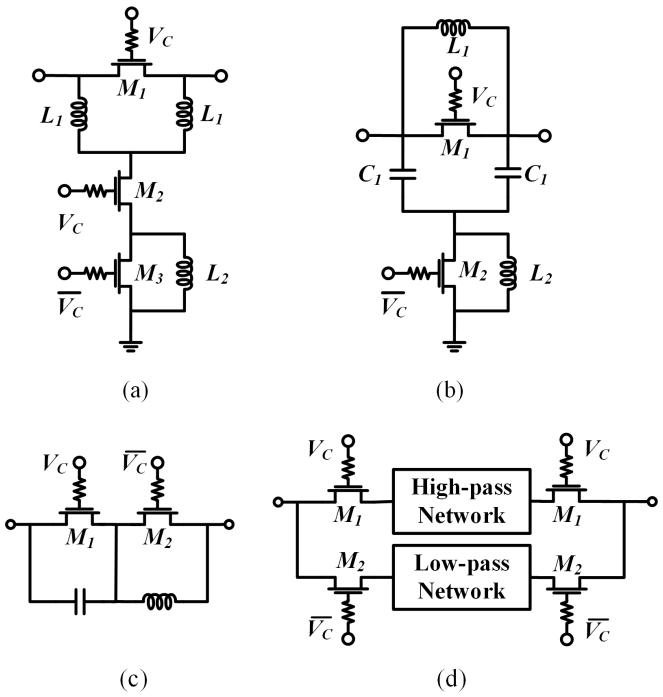

Fig. 2. Typical switched-type phase shifting topologies: (a) inductor-based T-type, (b) capacitor-based π-type, (c) switched L/C-type, and (4) high-/low-pass network.

Measured results prove that it can achieve broadband operation from 2.4 to 4 GHz with low rms IL error (i.e., <0.34 dB) and low rms phase error (i.e., <3.1°). Hence, the proposed STPS has the potential for high-performance phased array system applications.

This article is organized as follows. Section II analyzes the limitations of the conventional T-type switch-type phase shifting cell and proposes an improved T-type topology. A systematic cascade optimization method for STPSs based on topology selection and amplitude compensation is also described. In Section III, the measured results will be shown, followed by a discussion. Finally, the conclusion is drawn in Section V.

II. Design Considerations and Circuit Optimizations

The STPS is composed of cascaded switch-type phase shifting cells to satisfy the demand of phase resolution.

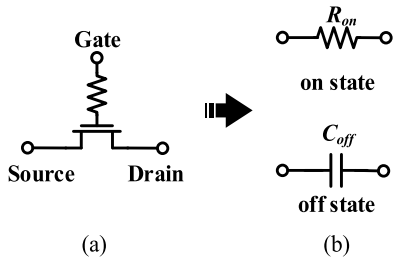

Fig. 3. (a) Structure of an FET switch. (b) Symmetrical physical model of FET. (b) Simplified model for the ON-state and the OFF-state of the switch.

Typical switch-type phase shifting topologies are shown in Fig. 2, including inductor-based T-type, capacitor-based π-type, switched L/C-type, and high-/low-pass networks. Each topology can operate in two states: the reference state and the phase shifting state. The phase difference between the two states is the relative phase shifting, whose deviation from the desired phase shifting degrades the rms phase error of PSs. The loss difference between the two states results in IL variation. Since the four topologies exhibit different phase and amplitude properties, they should be carefully picked up and optimized for the design of STPSs. In this work, based on the analyses of the limitation of conventional T-type structures, the improved T-type phase shifting structure is developed, which considers the phase and amplitude compensation. In order to further expand the operation bandwidth, the systematic cascade optimization method is discussed.

A. Simplified Model of Switched FET

For STPSs, since the FET switches are in series in the RF signal path, the IL of the FET switches is the major contributor to the IL of an STPS [13]. The GaAs pHEMT process that we used provides high electron mobility transistors that are suitable as low IL switches. The low IL systems based on the III-V technology are partly attributed to the characteristics of the FETs.

Fig. 3(a) shows the configuration of an FET switch, which consists of an FET and a large series gate resistor. The resistor in the switch will reduce the leakage of RF signal and weaken the coupling effect of parasitic capacitors. When the switch is adopted in STPS, we expect that the switch should have not only very low IL at the ON-state but also very low coupling at the OFF-state. However, the performance of low IL requires a transistor with a large gate width, which will increase the coupling effect between the input and output. Since the IL and coupling effect are mainly decided by the ON-resistance and OFF-capacitance of the switch FET, respectively, the switch can be modeled by an ON-resistance at the ON-state and an OFF-capacitance at the OFF-state, respectively, as shown in Fig. 3(b). Fig. 4 shows simulated results of the ON-resistance (R_{ON}) and OFF-capacitance (C_{OFF}) of the switches versus the total gate width of the FET based on the adopted process. Ideally, both R_{ON} and C_{OFF} are usually expected to be zero in switches design. However, in Fig. 4, C_{OFF} increases to several hundred femtofarads, while a large transistor gate width is adopted to achieve low R_{ON}. The opposite trend of R_{ON} and C_{OFF} brings undesired design conflict between the IL and phase accuracy of the phase shifting cell.

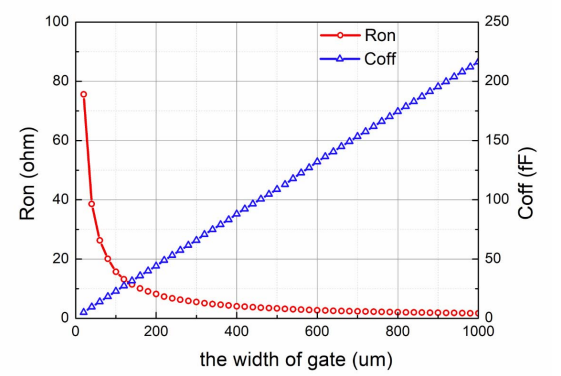

Fig. 4. Simulated results of the ON-resistance (R_{ON}) and OFF-capacitance (C_{OFF}) of the FETs versus the total gate width based on the adopted process.

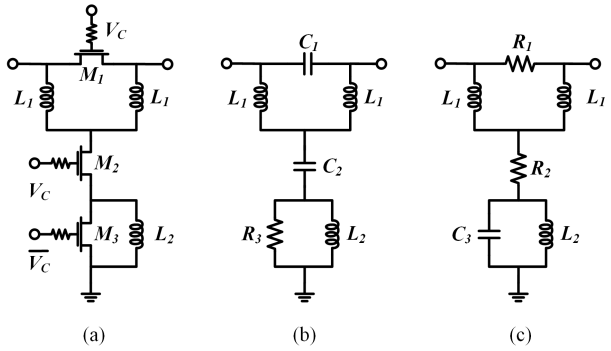

Fig. 5. (a) Inductor-based T-type phase shifting cell. (b) Equivalent circuits at the OFF-state. (c) Equivalent circuits at the ON-state.

Besides, the transistor gate width also has a crucial influence on the switching speed of the FET switches, which decides the phase shifting state built-up time of the PS. For the STPS, the built-up speed of PSs approximately depends on the switching speed of the widest switch transistor in the circuit, and the simulation built-up time of the whole STPS is about 35 ns when all cells switch the state after the control code changes.

B. Limitations of the Conventional T-Type Switched Phase Shifting Cell

Fig. 2 shows the four kinds of typical phase shifting topologies; the inductor-based T-type cells [6], [14], [15] and the capacitor-based π-type cells [3], [4], [16] are the most common structures, which are often adopted to realize 5.6°–90° phase shifting. In comparison, the T-type cells can achieve a relatively wideband constant phase shifting with low phase deviation. Besides, the group delay of the T-type phase shifting cell is less than that of π-type cells [14]. The poor design accuracy limits the application of the capacitor-based π-type cells [15]. Hence, the inductor-based T-type cells are a candidate to realize STPS for high phase accuracy and broadband applications.

The analysis of the conventional T-type switch-type phase shifting cell has been presented in [14] and [17]. Fig. 5 shows the equivalent circuits of the T-type structure. The assumed condition of the analysis is that the ON-resistance of M_{1-3} is nearly 0 and the OFF-capacitance C_1 is far less than $1/\omega^2 L_1$.

However, with the increase in phase shifting, the inductor L_1 will increase to several nanohenries for S-band applications. As shown in Fig. 4, if a transistor with a large gate width is applied to decrease the IL of RF signal path, the value of OFF-capacitance may be above 200 fF, which becomes comparable to the value of $1/\omega^2 L_1$. It will invalidate the assumption of the analysis in the above literature.

To evaluate the effect of the OFF-capacitance for optimizing switch-type phase shifting cells, the S-parameters of the networks were calculated using the transmission matrix parameters.

For the low-pass state in Fig. 5(b), we treat it as the state of phase shifting, while Fig. 5(c) represents the reference state. To omit the ON-resistance of transistors, the transmission coefficient S_{21} of phase shifting state and reference state can be expressed in (1-2), as shown at the bottom of the next page.

From (1) and (2), the insertion phase of the reference state and phase shifting state can be calculated as

$$\varphi_{\text{t-type},r} = -\tan^{-1}\left(\frac{Z_0\left(\omega^2 L_2 C_3 - 1\right)}{2\omega L_2 + \omega L_1\left(1-\omega^2 L_2 C_3\right)}\right) \tag{3}$$

$$\varphi_{\text{t-type},p} = -\tan^{-1}\left(\frac{Z_0\omega C_2}{2-\omega^2 L_1 C_2}\right) - \tan^{-1}\left(\frac{\omega L_1}{Z_0\left(1-2\omega^2 L_1 C_1\right)}\right). \tag{4}$$

The relative phase shifting $\varphi_{\text{t-type}}$ can be expressed with the following equation:

$$\varphi_{\text{t-type}} = \tan^{-1}\left(\frac{Z_0\omega C_2}{2-\omega^2 L_1 C_2}\right) + \tan^{-1}\left(\frac{\omega L_1}{Z_0\left(1-2\omega^2 L_1 C_1\right)}\right) - \tan^{-1}\left(\frac{Z_0\left(\omega^2 L_2 C_3 - 1\right)}{2\omega L_2 + \omega L_1\left(1-\omega^2 L_2 C_3\right)}\right). \tag{5}$$

Compared to the ideal state, the OFF-capacitance C_1 brings a phase variation $\Delta\varphi_{\text{t-type}}$ to the phase shifting state, which can be given as follows:

$$\Delta\varphi_{\text{t-type}} = \varphi_{\text{t-type}} - \varphi_{\text{t-type}}|_{C_1=0} = \tan^{-1}\left(\frac{\omega L_1}{Z_0\left(1-2\omega^2 L_1 C_1\right)}\right) - \tan^{-1}\left(\frac{\omega L_1}{Z_0}\right). \tag{6}$$

As this equation suggests, the phase deviation increases with the increase in the OFF-capacitance C_1. This situation aggravates when the operating frequency raises. Taking the 45° and 90° phase shifting cells as examples, Fig. 6 shows the phase shifting impact brought by the nonideal OFF-capacitance.

For the 45° cell, the insertion phase of phase shifting state decreases 7.6° at 4 GHz due to the introducing a 200-fF OFF-capacitance. At the same time, the phase variation of the 45° phase shifting cell also increases from 1° to 5.5° at the operating frequency range. The OFF-capacitance reduces the phase bandwidth of the T-type phase shifting cell. With the phase shifting degree increasing, C_1 will more approach to the value of $1/\omega^2 L_1$. The 90° phase shifting is almost close to the limitation of the T-type cell. The large design parameter

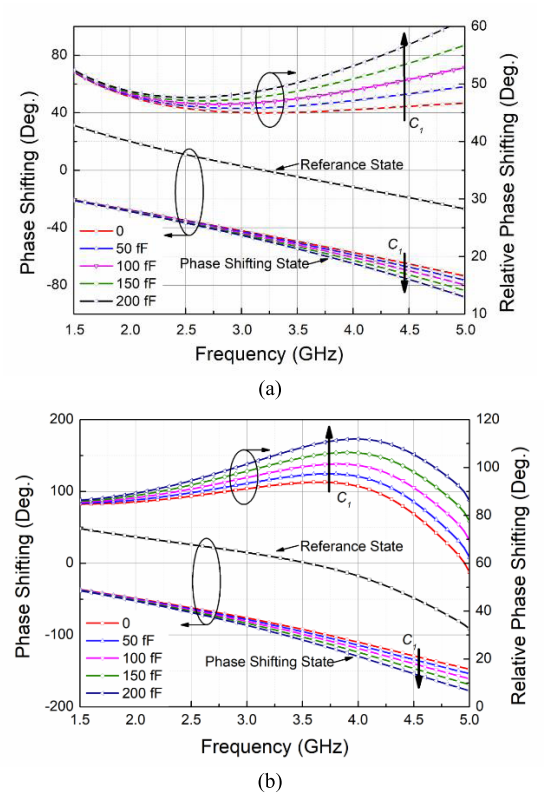

Fig. 6. Calculated the phase shifting and relative phase shifting: (a) 45° phase shifting cell and (b) 90° phase shifting cell.

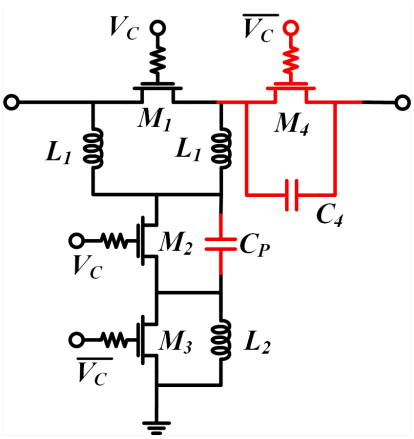

Fig. 7. Schematic of the proposed improved T-type switched phase shifting cell.

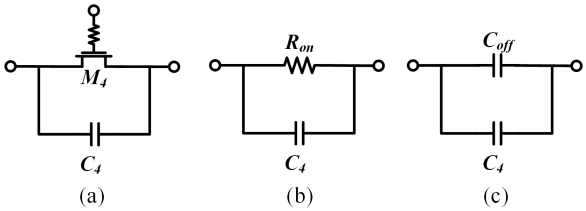

Fig. 8. (a) Switched filter structure. (b) Bandpass mode at the ON-state. (c) High-pass mode at the OFF-state.

of devices in 90° cells already sensitizes the performance of the bandwidth and the phase variation. The OFF-capacitance C_1 will make the issue of phase variation more serious and degrades the rms phase error and bandwidth of the whole PS. Fig. 6(b) shows the calculated the phase shifting and relative phase shifting of 90° cell, the 200 fF OFF-capacitance can result in 20° phase shifting at the original basis at 4 GHz, and the phase bandwidth deteriorates obviously due to the OFF-capacitance C_1.

C. Improved T-Type Phase Shifting Cell With Switched Filter Compensation

To address the limitations of conventional T-type phase shifting cells, an improved T-type phase shifting cell is proposed to achieve large phase shifting. The improved T-type phase shifting cell, which adds a parallel capacitance C_P and a switched filter structure, is shown in Fig. 7. Since the OFF-capacitance of M_2 is too small alone to achieve desired large phase shifting degree, the addition of C_P is a supplement of M_2's OFF-capacitance. The cascaded switched filter structure can be treated as a mini phase shifting cell, and it also has two states. The control voltages of M_1 and M_4 are reversed, and the switched filter structure is a high-pass network when V_C is high level, corresponding to the reference state of phase shifting cell. When V_C is biased at a low level, it is a bandpass network. With a careful selection of the capacitance C_4 and transistor M_4, the amplitude response trend of the switched filter can be contrary to the T-type network, and the relative phase shifting with frequency also shows opposite change with the T-type network at the operating frequency range. Therefore, the cascaded switched filter structure can compensate for the amplitude and phase shifting of the T-type network to improve the bandwidth and phase shifting accuracy.

To derive the equations for better understanding the operating principle of switched filter structure, the *S*-parameters of the switched networks were derived using transmission matrix parameters. For the bandpass state of Fig. 8(b), S_{21} can be expressed as follows:

$$S_{21,s-C,p} = \frac{2Z_0}{2Z_0\left(1+\omega^2 C_4^2 R_{\mathrm{ON}}^2\right) + R_{\mathrm{ON}} - j\omega C_4 R_{\mathrm{ON}}^2}. \quad (7)$$

$$S_{21,\text{t-type},r} = \frac{2\omega^2 L_2 L_1 + \omega^2 L_1^2\left(1-\omega^2 L_2 C_3\right)}{2\omega^2 L_2 L_1 + \omega^2 L_1^2\left(1-\omega^2 L_2 C_3\right) - j\omega Z_0 L_1\left(1-\omega^2 L_2 C_3\right)} \quad (1)$$

$$S_{21,\text{t-type},p} = \frac{2Z_0\left(2\omega^2 L_1 C_1 - 4\omega^4 L_1^2 C_1 C_2 - 1\right)\left(1-2\omega^2 L_1 C_1\right)}{\left[\omega^2 L_1 C_2 - 2 + 4\omega^2 L_1 C_1 - 2\omega^4 L_1^2 C_1 C_2 - Z_0\left(1-2\omega^2 L_1 C_1\right) j\omega C_2\right]\left[j\omega L_1 + Z_0\left(1-2\omega^2 L_1 C_1\right)\right]} \quad (2)$$

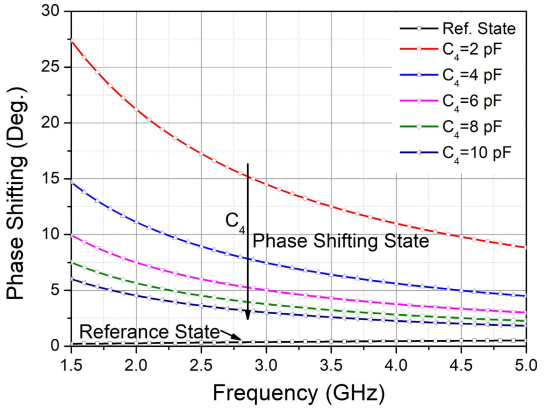

Fig. 9. Calculated the phase shifting of the switched filter structure for different C_4's.

From (7), the phase response at the bandpass state can be expressed as

$$\varphi_{s-C,p} = \tan^{-1}\left(\frac{\omega C_4 R_{\text{ON}}^2}{2Z_0 + R_{\text{ON}} + 2Z_0\omega^2 C_4^2 R_{\text{ON}}^2}\right). \tag{8}$$

For the high-pass state in Fig.8(c), the transmission coefficient S_{21} is expressed as

$$S_{21,s-C,r} = \frac{2Z_0\omega(C_4 + C_{\text{OFF}})}{2Z_0\omega(C_4 + C_{\text{OFF}}) - j}. \tag{9}$$

The phase shifting of the high-pass network can be deduced as

$$\varphi_{s-C,r} = \tan^{-1}\left(\frac{1}{2Z_0\omega(C_4 + C_{\text{OFF}})}\right). \tag{10}$$

In order to reduce the IL of the network, transistor M_4 with a large gate width is adopted, and we assume that the ON-resistance can be omitted. C_{OFF} of M_4 is also far less than C_4 for small phase shifting degrees at the operating frequency range. Therefore, from (8) and (10), the relative phase shifting φ_{s-C} can be approximated as

$$\varphi_{s-C} \approx \varphi_{s-C,r} \approx \tan^{-1}\left(\frac{1}{2Z_0\omega C_4}\right). \tag{11}$$

Fig. 9 shows the relative phase shifting versus frequency at different C_4's. By tuning the value of C_4, we can achieve desired relative phase shifting degree and the rate of phase shifting change versus frequency. The design parameter C_4 for the desired phase shifting φ_{s-C} can be obtained as follows:

$$C_4 = \frac{1}{2Z_0\omega\tan(\varphi_{s-C})}. \tag{12}$$

By comparing the relative phase shifting trend of the conventional T-type PS and the switched filter structure, we can combine the T-type PS and the switched filter structure to achieve desired accurate wideband switch-type phase shifting cell. To avoid solving the complex phase shifting and amplitude equations, a convenient design method of improved T-type cell is proposed, as shown in Fig. 10. The graphs on the right-hand side of Fig. 10 show the operating principle of the improved T-type phase shifting cell concisely. The 45° and 90° phase shifting cells have been designed based on the proposed

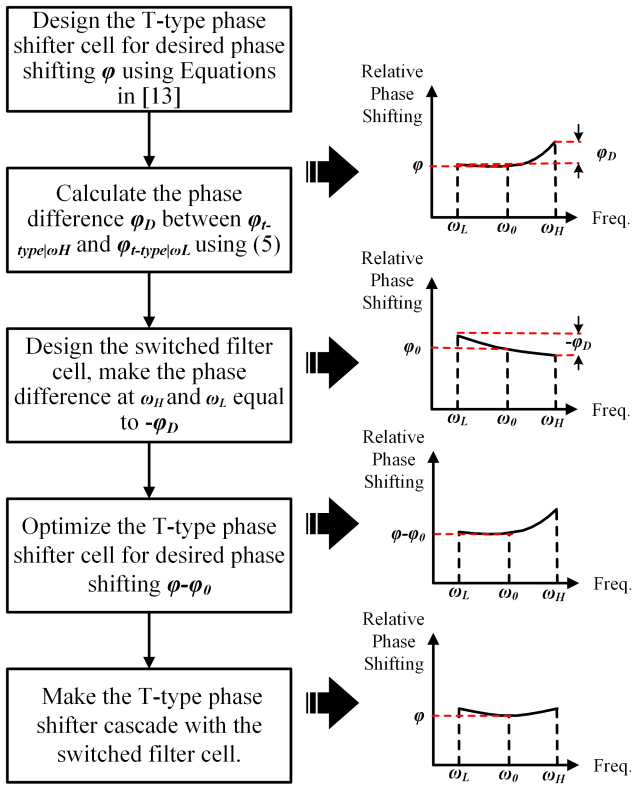

Fig. 10. Flowchart of the improved T-type cell design.

design method; the simulated phase deviation and amplitude variation at the operating frequency are plotted in Fig. 11. For the 45° cell, the phase deviation of the proposed improved T-type cell is ±0.5° at the operating frequency range, while the phase deviation of the conventional cell is about ±1.2°. The amplitude variation of the improved T-type cell is also smaller. Since the 90° phase shifting has almost reached the limitation of the T-type cell, the large device parameters in the circuit result in a large absolute phase deviation. With the phase and amplitude compensation of the switched filter cells, the proposed improved T-type cell achieves ±2.1° phase deviation and about ±0.5-dB amplitude variation.

To compare with the results of conventional T-type phase shifting cells, the proposed improved T-type phase shifting cell obviously has lower phase deviation and amplitude variation.

D. Phase Shifting Cell Topology Selection and Systematic Cascade Optimization

The main design goal of the SPTS is to achieve the target phase shifting range with the desired phase resolution while ensuring low rms phase/amplitude error, low IL, good impedance matching, and wideband operation simultaneously, since the SPTS consists of multistage cascaded phase shifting cells, which has the reference state and phase shifting state, respectively. When each cell achieves a good matching, the IL, phase deviation, and amplitude variation of each phase shifting cell will be independent, and they will be hardly impacted by adjacent cells. The accumulation of each cell's IL and phase/amplitude deviation makes the main contribution to the

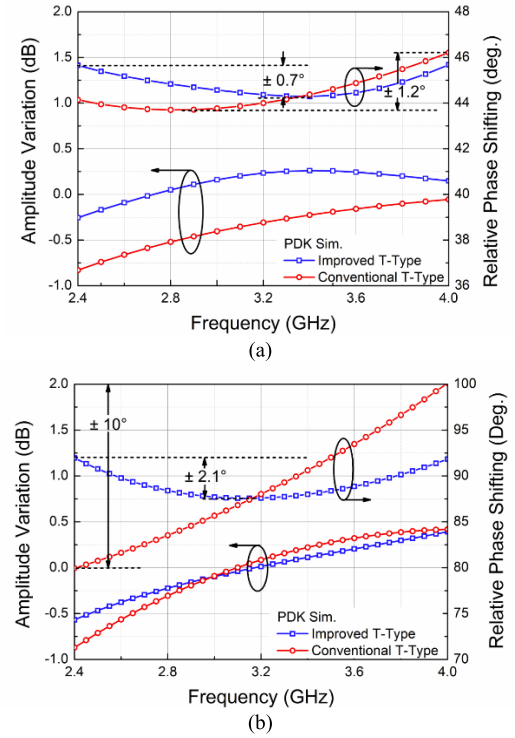

Fig. 11. Simulated amplitude variation and relative phase shifting of the conventional T-type and improved T-type.

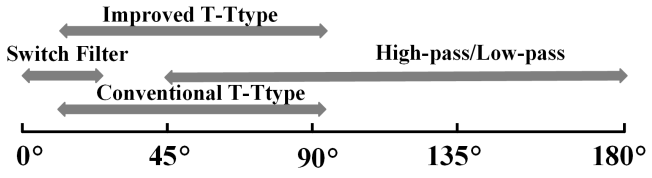

Fig. 12. Brief summary about the phase shifting capability based on a statistical analysis of the published literature.

whole PS performance. Therefore, the choice and optimization of each phase shifting cell are crucial to reduce the IL and rms phase/amplitude error of the PS.

For the 7-bit STPS, the seven phase shifting cells need to be designed to achieve 2.8°, 5.6°, 11.25°, 22.5°, 45°, 90°, and 180° phase shifting, so as to cover 360° phase shifting range with a 2.8° phase step. In order to compensate for the phase deviation of the 7-bit PS, an additional 1.4° cell is also adopted.

The capability of phase shifting should be considered as a priority during selecting the topology for each cell. A brief summary of the phase shifting capability, which is based on a statistical analysis of the published literature, has been given in Fig. 12. The switch L/C structures are usually adopted to realize the phase shifting below 11.25°, while the conventional T-type can achieve less than 90° phase shifting. The proposed improved T-type has a similar phase shifting capability. For the large phase shifting requirement, the high-/low-pass networks are suitable. The overlap region in Fig. 12 shows that multiple candidates can be picked up to achieve the desired phase shifting.

According to the design goal of high-performance STPS, a tradeoff should be made among the IL, phase deviation, amplitude variation, and area of the structure during the selection of topologies. In this work, for the 180° phase shifting cell, the high-/low-pass network is adopted. The order of the network will influence the bandwidth of cells [1]; a fifth-order network is used in this work. For the 45° and 90° phase shifting cells, the area and IL of T-type structures are less than those of high-/low-pass networks. The proposed improved T-type structure can overcome the influence of the OFF-capacitance, as the analysis above, and achieve the comparative low phase/amplitude deviation. For the 22.5° and 11.25° phase shiftings, the influence of the switch FET OFF-capacitance becomes weak; the conventional T-type structure can achieve a similar phase and amplitude performance in comparison with the improved T-type structure and has simpler topology.

When the value of the phase shifting is less than 11.25°, the T-type structure and switched L/C structure both have the capability to achieve the desired phase shifting with low phase deviation. However, the characteristics of the IL and area of the two structures are different. Only one inductor is used in the switched L/C structure, and its area is much less than the area of the T-type. For the amplitude response, the average IL of the states of the T-type cell is decided by the LCL π-resonator, which is a low-pass network. The average IL of the switched L/C structure can be designed as a high-pass network.

Compared to the other performances of STPS, the average IL of PS is the summation of the average IL of each cell, and the flatness of IL decides the bandwidth of the STPS. In order to design a wideband PS, we expect that the average IL of the PS remains constant with frequency. In the premise of low phase deviation and amplitude variation, the average IL of reference and phase shifting state of each cell should be carefully optimized. The 180° cell is realized by a fifth-order network, whose amplitude and relative phase shifting are wideband. For the proposed 90° and 45° improved T-type structures, the topology exhibits high- and low-pass transfers, respectively, when the control signal switches. Due to the neutralization of the high- and low-pass states, the average IL of improved T-type structure can realize wideband design easily. However, the amplitudes of the cells, which are designed for less than 45° phase shifting, are frequency-dependent. In order to expand the bandwidth of the PS, a systematic optimization based on the average IL of the five cells, which are the 1.4°, 2.8°, 5.6°, 11.25°, and 22.5° cells, should be taken into consideration.

As mentioned above, the average IL of the T-type cell increases with frequency increasing, while that of the switched L/C network mainly exhibits an opposite state. Therefore, while designing the PS, the switched L/C structure is selected for the 1.4° compensation cell and 2.8° phase shifting cell, while the T-type structure is adopted to achieve 5.6° and 11.25° phase shiftings. By optimizing the average IL of the 1.4° and 2.8° cells, we can systematically compensate for the IL of the 5.6°, 11.25°, and 22.5° cells. Table I lists the simulated IL of each phase shifting cell versus frequency. Based on the

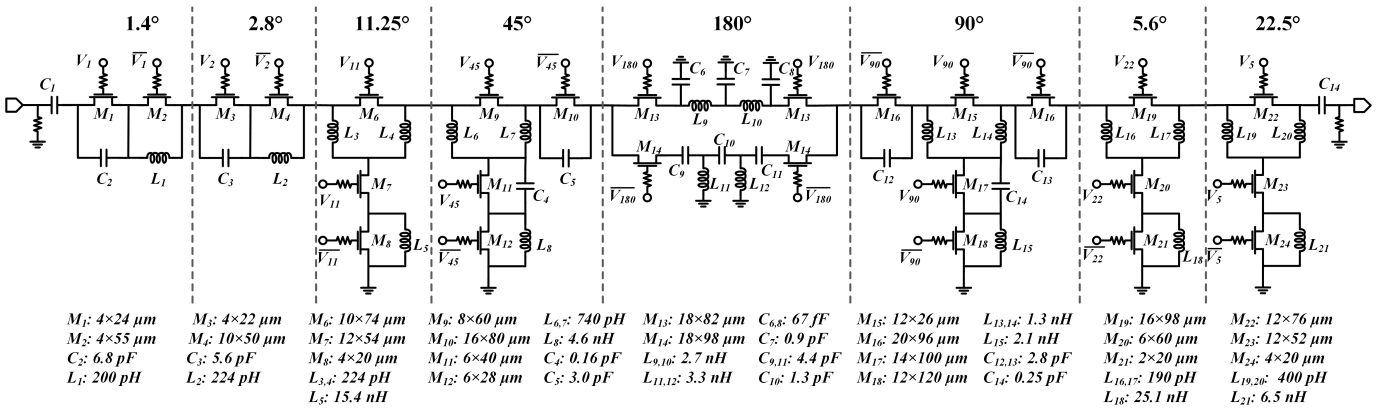

Fig. 13. Simplified schematic of the proposed 7-bit switched-type PS with a 1-bit compensation cell.

TABLE I
SIMULATED IL AND $IP_{1\,dB}$ OF EACH PHASE SHIFTING CELL

Cell	1.4°	2.8°	5.6°	11.25°
IL (dB)	0.31-0.25 ↓	0.36-0.25 ↓	0.12-0.17 ↑	0.18-0.23 ↑
IP1dB (dBm)	-	-	32.5	32.5
Cell	**22.5°**	**45°**	**90°**	**180°**
IL (dB)	0.26-0.32 ↑	0.52 →	0.87 →	1.20 →
IP1dB (dBm)	32.5	32	29.5	30.5

↓: the IL decreases with frequency increasing.
↑: the IL increases with frequency increasing.
→: the IL nearly keeps constant with frequency.

systematic compensation method, a relative wideband PS can be achieved.

Based on the above discussion, the schematic of the proposed 7-bit STPS is shown in Fig. 13. The 1.4° and 2.8° cells employ the switched L/C structure; the conventional T-type topology is adopted to realize the 5.6°, 11.25°, and 22.5° phase shifting cells. For the large phase shifting cell, the 45° and 90° cells adopted the proposed improved T-type structure, while the high-/low-pass network is used in the 180° phase shifting cell. The series capacitor and the shunt resistor at input and output ports are used to block the dc and optimize the matching. The parameter of the devices is listed in Fig. 13.

The cascade order of these cells is mainly dependent on the linearity and the layout of each cell. First, the high linearity cells need to be placed at the front of the circuit structure. Table I also lists the input 1-dB compression point. For the STPS, the compression occurs because the transient voltage of the high-power RF input signal changes the original state of FET switches. Due to the change of the switch state, the RF signal leaks from the tail transistor of the T-type structure, and the impedance of the cells becomes unmatched. Then, the IL of cells increases. Second, the shape of each cell is different, and the cascade order needs to be considered to minimize the area of the STPS.

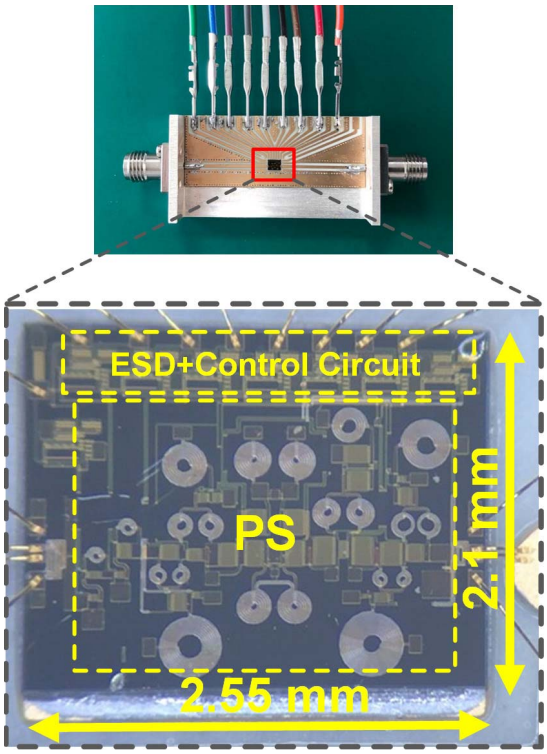

Fig. 14. Evaluation board and the chip micrograph of the proposed 7-bit PS.

III. MEASUREMENT RESULTS

The 7-bit PS that we proposed is fabricated in the 0.5-μm GaAs pHEMT process, and the micrograph of the PS is shown in Fig. 14. The chip occupies an area of 2.1 mm × 2.55 mm, and the core PS circuit area without the ESD and logic control circuit is 1.6 mm × 2.2 mm. The chip is bonded on the Rogers 4350B board to perform measurements. The 50-Ω grounded coplanar waveguides are utilized to extract the input and output RF signals, and the dc bias and 0-/5-V digital phase control signal are connected to the chip by narrow conductive traces.

The measured input and output reflection coefficients for all phase states are plotted in Fig. 15. The results show that the input and output reflection coefficients of all states are below −10 dB from 2.4 to 4 GHz; it implies

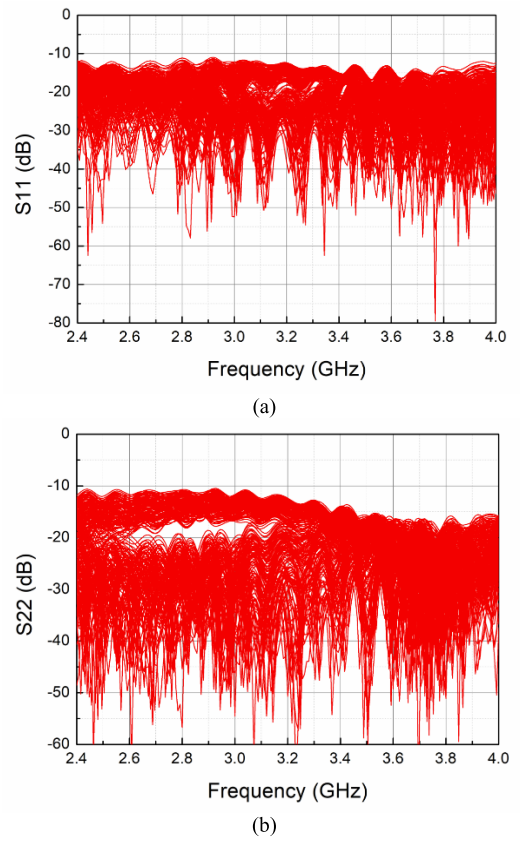

Fig. 15. Measured input and output reflection coefficient.

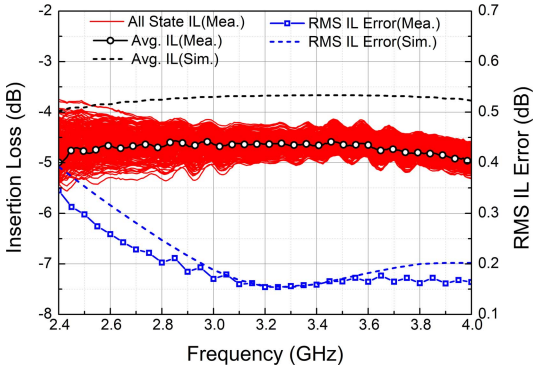

Fig. 16. Simulated and measured IL and the rms amplitude error.

broadband impedance matching at both input and output ports.

Fig. 16 depicts the measured IL results versus frequency. The PS exhibits an average IL of 4.5–4.9 dB after eliminating the evaluation board IL of 0.22–0.43 dB over the operating frequency. The measured IL is higher by about 1 dB than the simulation results, and the main part of the gap is due to the bonding wires of the input and output. The rms amplitude error of the PS is also very low and less than 0.34 dB over the whole operating band, and it agrees with the simulation. From 2.9 to 4 GHz, the rms amplitude error of less than 0.2 dB, which is the lowest result compared to state-of-the-art PSs, used a similar process and operated at a similar frequency.

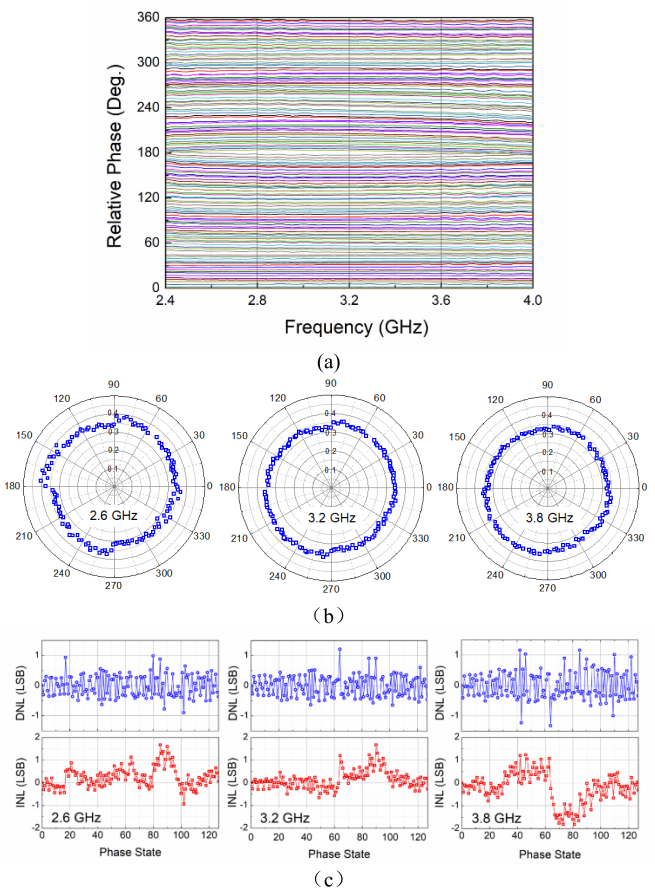

Fig. 17. Results of the phase shifting states. (a) Measured the relative phase shift of each bit. (b) Measured S_{21} of 128 states in the polar chart at 2.6/3.2/3.8 GHz. (c) Measured phase integral nonlinearity (INL) and differential nonlinearity (DNL) versus phase state at 2.6/3.2/3.8 GHz.

Fig. 17(a) shows the relative phase shift states of the proposed 7-bit PS. The relative phase shift and amplitude of 128 states at 2.6/3.2/3.8 GHz are also plotted in the polar chart in Fig. 17(b), which shows the phase shifting coverage and amplitude variation clearly. Fig. 17(c) shows the measured DNL and INL of the proposed STPS for 128 phase states. For most control codes, the measured DNL is less than ±0.5 LSB. Due to the phase error accumulation of several cells, the DNL error of six states is outside the range of ±1 LSB at 3.2 and 3.8 GHz. The INL is between ±1.8 LSB. When the phase state turns into 64, the phase shifting cells all switch the operating states, and the accumulated phase error changes instantly. Besides, due to the phase error of each cell increasing at the high-frequency section, the INL results degenerate when the phase state is near 64 at 3.8 GHz. The rms phase error is depicted in Fig. 18. When the 7-bit main phase shifting cells work alone, the rms phase error is less than 3.5°, and it cannot maintain the phase error requirement of a 7-bit PS. With the calibration of a 1.4° compensation cell, the rms phase error is less than 1.5° from 2.8 to 3.7 GHz.

The power performance of the reference state of the STPS has also been tested. Fig. 19 shows the input 1-dB compression point and the third-order intercept point (IIP3) in the frequency range from 2.4 to 4 GHz. The IIP3 is obtained using the two-tone test with a frequency spacing of 10 MHz. The measured

TABLE II
PERFORMANCE COMPARISON OF REPORTED SIMILAR PSS

Ref.	[1]	[2]	[3]	[4]	[5]	[6]	This work
Process	0.5-μm GaAs	0.5-μm GaAs	0.18-μm SOI	0.5-μm GaN	0.15-μm GaAs	0.5-μm GaAs	**0.5-μm GaAs**
Frequency (GHz)	3–6	1.5–3	5–6	8–12	2.5–4	S-Band	**2.4–4**
Bandwidth (%)	66.7	66.7	18	40	46	10	**50**
Resolution (bit)	6	5	6	5	6	5	**7**
Gain (dB)	>-6.7	10#	-4.8	-14	-5	-5.5– -6.7	**-4.5– -4.9**
RMS Gain Error (dB)	0.3–0.6	<1.5	0.4	0.8	0.4	0.58	**< 0.34**
RMS Phase Error (°)	< 4	<9	10	6.4	5	2.8	**< 3.1 <1.5 @2.8-3.7 GHz**
P1dB (dBm)	29	12	29.6	34.8	29	21	**> 29.6**
Area(mm^2)	1.8	12.15#	1.03	23.5*	5.28	1.63	**5.3***
FOM	15.6	-	4.7	7.8	8.1	0.31	**19.8**

*: with logic control circuit.
#: with Amplifier.

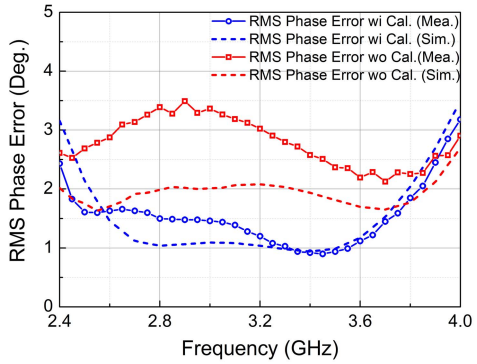

Fig. 18. Simulated and measured the rms phase error.

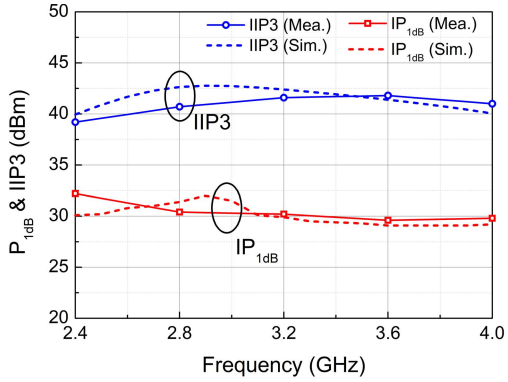

Fig. 19. Simulated and measured $IP_{1\,dB}$ and IIP3 of the STPS against the operation frequency.

$IP_{1\,dB}$ is higher than 29.6 dBm, while the IIP3 is above 39.2 dBm. They are high and will not limit the phased-array system linearity.

Table II gives a performance comparison among the proposed PS and previously published similar state-of-the-art MMIC PSs. The proposed STPS has a low IL and lowest rms amplitude error while cascading most phase shifting cells and achieving a 7-bit phase resolution. Besides, the bandwidth, the rms phase error, and the linearity of this PS are also close to the best performance in comparison with previously reported works. The FOM [18] of the proposed STPS is the best compared to the counterparts.

IV. CONCLUSION

In this article, a 2.4–4-GHz 7-bit STPS using the 0.5-μm GaAs pHEMT process is presented. Various switch-type phase shifting topologies, such as the switched L/C structure, T-type structure, and high-/low-pass networks, are applied for different bits. In order to minimize the amplitude/phase deviation and broaden the bandwidth, we proposed an improved T-type phase shifting structure to realize the 45° and 90° phase shifting cells. According to the amplitude characteristic of each cell, systematic optimization based on the amplitude compensation is performed. The proof-of-concept design exhibits that the average IL is 4.5–4.9 dB with an rms amplitude error of less than 0.34 dB at a 50% frequency bandwidth range. The rms phase error of the phase shift is less than 3.1° over the operating frequency. Compared to those low-resolution PSs, the PS we proposed has a 7-bit phase resolution while achieving lower IL variation with similar rms phase error.

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REFERENCES

[1] J. Chen, S. Mou, K. Ma, and F. Meng, "A 3–6-GHz wideband compact 6-bit phase shifter in 0.5-μm GaAs technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 8, pp. 794–797, Aug. 2020, doi: 10.1109/LMWC.2020.3007836.

[2] D. M. Zaiden, J. E. Grandfield, T. M. Weller, and G. Mumcu, "Compact and wideband MMIC phase shifters using tunable active inductor-loaded all-pass networks," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1047–1057, Feb. 2018.

[3] H. Jeon and K. W. Kobayashi, "A high linearity +44.5-dBm IP 3*C*-band 6-bit digital phase shifter using SOI technology for phased array applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 11, pp. 733–736, Nov. 2019.
[4] W. Luo, H. Liu, Z. Zhang, P. Sun, and X. Liu, "High-power *X*-band 5-b GaN phase shifter with monolithic integrated E/D HEMTs control logic," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3627–3633, Sep. 2017.
[5] Qorvo. *TGP2108, 2.5–4 GHz 6-Bit Digital Phase Shifter*. Accessed: Dec. 2016. [Online]. Available: https://www.qorvo.com/products/control-products/phase-shifters
[6] M. Hangai, M. Hieda, N. Yunoue, Y. Sasaki, and M. Miyazaki, "*S*- and *C*-band ultra-compact phase shifters based on all-pass networks," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 1, pp. 41–47, Jan. 2010.
[7] T. W. Li, J. S. Park, and H. Wang, "A 2–24-GHz 360° full-span differential vector modulator phase rotator with transformer-based polyphase quadrature network," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 12, pp. 2623–2635, Dec. 2020.
[8] M.-M. Mohsenpour and C. E. Saavedra, "Variable 360° vector-sum phase shifter with coarse and fine vector scaling," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2113–2120, Jul. 2016.
[9] H. J. Qian, B. Zhang, and X. Luo, "High-resolution wideband phase shifter with current limited vector-sum," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 820–833, Feb. 2019.
[10] K. Carver, W. Cooper, and W. Stutzman, "Beam-pointing errors of planar-phased arrays," *IEEE Trans. Antennas Propag.*, vol. AP-21, no. 2, pp. 199–202, Mar. 1973.
[11] A. M. Niknejad and H. Hashemi, *Mm-Wave Silicon Technology 60 GHz and Beyond*. New York, NY, USA: Springer, 2008, pp. 243–292.
[12] T.-W. Li and H. Wang, "A millimeter-wave fully integrated passive reflection-type phase shifter with transformer-based multi-resonance loads for 360° phase shifting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 4, pp. 1406–1419, Apr. 2018.
[13] M. Meghdadi, M. Azizi, M. Kiani, A. Medi, and M. Atarodi, "A 6-bit CMOS phase shifter for S-band," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3519–3526, Dec. 2010.
[14] W.-T. Li, Y.-C. Chiang, J.-H. Tsai, H.-Y. Yang, J.-H. Cheng, and T.-W. Huang, "60-GHz 5-bit phase shifter with integrated VGA phase-error compensation," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1224–1235, Mar. 2013.
[15] F. Meng, K. Ma, K. S. Yeo, and S. Xu, "A 57-to-64-GHz 0.094-mm^2 5-bit passive phase shifter in 65-nm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 5, pp. 1917–1925, May 2016.
[16] B.-W. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2239–2250, Oct. 2008.
[17] D.-W. Kang, H. D. Lee, C.-H. Kim, and S. Hong, "Ku-band MMIC phase shifter using a parallel resonator with 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 294–301, Jan. 2006.
[18] D. Pepe and D. Zito, "Two mm-wave vector modulator active phase shifters with novel IQ generator in 28 nm FDSOI CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 344–356, Feb. 2017.

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