Design and Simulation of 6-bit MMIC Digital Attenuator using GaN pHEMT

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***Abstract*— This paper introduces the simulation and design of high performance 5-20 GHz MMIC 6-bit digital attenuator realized on 100 µm GaN substrate. Suitable topologies for each attenuation bit are selected. GaN PHEMTs switches are used to design this attenuator. The simulated results show the total attenuation range from 0.5dB to 31.5dB. Worst case insertion loss of ~ 3 dB is achieved for all the six bits of the attenuator over entire operating frequency band. All practical aspects of the design are incorporated while doing simulations.**

Keywords*— *digital attenuators; 6-bit; GaN pHEMT; Insertion loss.

I. INTRODUCTION

Attenuator is an essential component in a transreceiver module for controlling amplitude of incoming signal from a high frequency system. Various topologies with stringent parameters' control such as low phase, high linearity and amplitude variations and large attenuation range have been reported till date. Among various microwave RF attenuators, a digital attenuator offers some distinguishing features such as high linearity, large power handling, easy and accurate control of attenuation at high speed. The small-signal equivalent circuit model of GaN HEMT switch employed in this work is taken from [1]. An ultra-wide band (2-18GHz) 6-bit digital attenuator is implemented with low insertion phase shift in [2, 3] on 0.5µm GaAs PHEMT MMIC process t. In [4], circuit consisting of second order low pass phase correction network is used for phase compensation to implement 6-bit digital phase shifter. [5] employed capacitor in parallel with the improved structure and cascaded structure for high isolation was proposed. In [6] a control circuitry to provide voltages from a single control voltage and a linear relationship between rf attenuation and the control voltage is established. 5-bit MMIC wideband digital attenuator using Bridged Tee Topology with better performance as compared to Pi Topology has been proposed in [7-9].

This paper summarizes the design of 5GHz to 20GHz 6 bit MMIC digital attenuator implemented on 100 µm GaN substrate utilizing PHEMTs switches. It is different from others in matching of each bit input and output impedances which are different from 50Ohms. So designing gets relaxed by putting constraint of 50ohm at the input and output. It consists of 6 attenuation bits viz. 0.5, 1, 2, 4, 8 and 16dB. The shunt switched resistance, T, Pi, and switched bridged-Pi type topologies are used to implement (0.5 and 1 dB), (2dB), (4 and 8 dB) and 16dB attenuation states respectively. Using the above mentioned 6 bits of attenuation, all 64 states of attenuation starting from 0.5dB (LSB) to31.5dB (MSB) are obtained. The phase error have been adjusted by introducing the elements which are compensating the phase error in all the bits.

II. CIRCUIT DESIGN

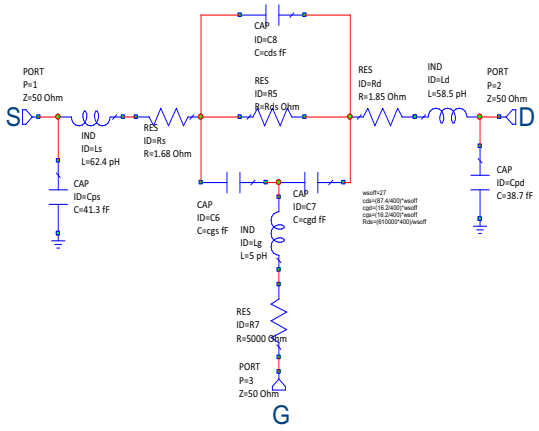

Fig. 1. ON/OFF switch model of GaAs PHEMT

Fig. 1 shows the ON/OFF model of GaN PHEMT switch. In ON state of PHEMT switch, drain to source voltage (Vds) is zero and gate to source voltage (Vgs) is either zero or slightly positive. Under this condition of bias, transconductance (gm) is zero for all practical purposes and channel under the gate is open and conducting thereby allowing RF current (signal) to flow through. Thus, the dissipation of RF energy in the channel is quite small due to very small resistance offered to RF current i.e., of the order of 2-5Ω only. The (Cgs) gate to source capacitance and (Cgd) gate to drain capacitance are very high in ON state. To isolate gate from RF leakage in high frequency and high power condition, generally a high resistance around 3KΩ to 5KΩ is put in series with gate. There is a drain to source capacitance in parallel with channel resistance under the gate arising out of planar geometrical arrangement of source and drain electrodes. The gate capacitances, channel resistance and to some extent drain-source capacitance are gate bias dependent i.e., values of these model elements will be different in OFF state than in ON state.

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In OFF state condition of switch i.e. when no drain source RF current flows through the channel under the gate, is achieved by keeping the gate below the pinch off gate voltage for Vds=0V. In addition to this, the channel resistance in OFF state is very high i.e., of the order of 10 KΩ to 30 KΩ and Cgs and Cgd are smaller compared to those in ON state. Rest of the elements as shown in the electrical equivalent circuit of ON/OFF state are gate and drain bias independent parasitic elements as they depend on the geometry of the PHEMT layout including drain, source and gate electrodes. These elements are known as extrinsic parasitic elements.

ON and OFF model for 4x100µm PHEMT switch are shown in Fig. 2(a), (b) respectively. The model elements values of 4x100µm PHEMT switch are given as –

For OFF state –

Cgs=16.2 fF, Cgd=16.2fF, Cds=87.4fF and Rds=610KΩ

For ON state –

Cgs=84.5 fF, Cgd=84.5fF, Cds=326fF and Rds=8.52Ω

Extrinsic parasitic elements are –

Cps=41.3fF, Ls=62.4pH, Rs=1.68Ω, Cpd=38.7fF, Ld=58.5pH, Rd=1.85Ω , Lg= 5pH and Rg=5KΩ

Using the intrinsic model elements values for 4x100µm PHEMT switch, intrinsic model elements values for other sizes of gate width of PHEMT switch can be found out using the scaling equations driven from the relations between the model elements values and gate width –

Rds (channel resistance) ∝ 1/W (gate width)

Cgs(gate source capacitance) ∝ W (gate width)

Cgd(gate drain capacitance) ∝ W (gate width)

Cds(drain source capacitance) ∝ W (gate width)

The scaling equations are –

For OFF state –

$$cds = \left(\frac{87.4}{400}\right) * wsoff\,, \qquad cgd = \left(\frac{16.2}{400}\right) * wsoff$$

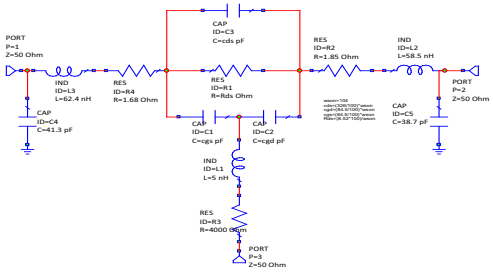
$$cgs = \left(\frac{16.2}{400}\right) * wsoff, \qquad Rds = \frac{610000*400}{wsoff}$$

For ON state –

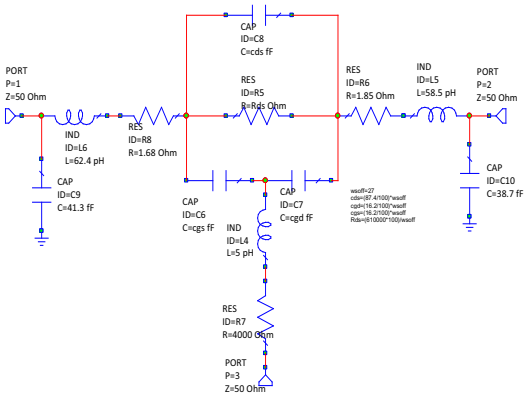
$$cds = \left(\frac{326}{400}\right) * wson, \qquad cgd = \left(\frac{84.5}{400}\right) * wson$$

$$cgs = \left(\frac{84.5}{400}\right) * wson, \qquad Rds = \frac{8.52*400}{wson}$$

The scaled ON state and OFF state model of GaN PHEMT switch are shown below.



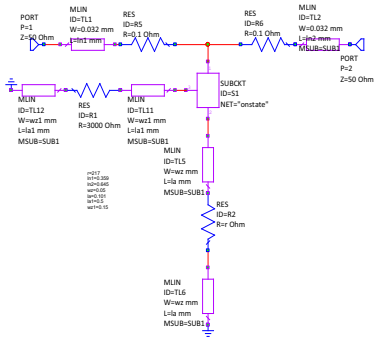
(a)



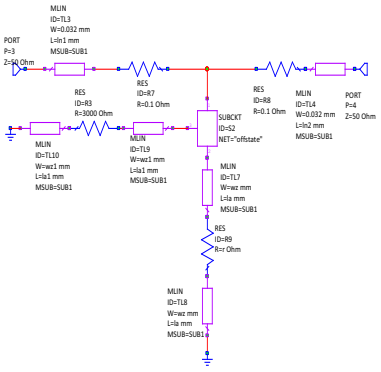
(b)

Fig. 2. (a) Transistor model for (a) ON state and (b) OFF state of switching PHEMT.

Using the ON and OFF state models, the attenuator is designed with high value resistor at gate to provide isolation between controlled gate voltage and RF signal through the channel. Fig. 3, 4, 5 and 6 show the T, Pi, cascaded Pi and switched bridged-Pi attenuator topologies used for designing 0.5dB, 1dB, 2dB, 4dB, 8dB and 16 dB attenuation bits .

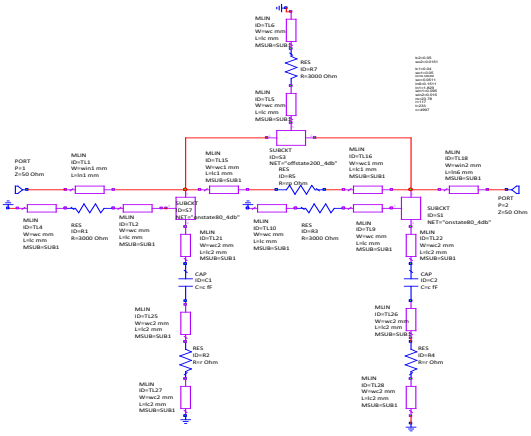


(a)

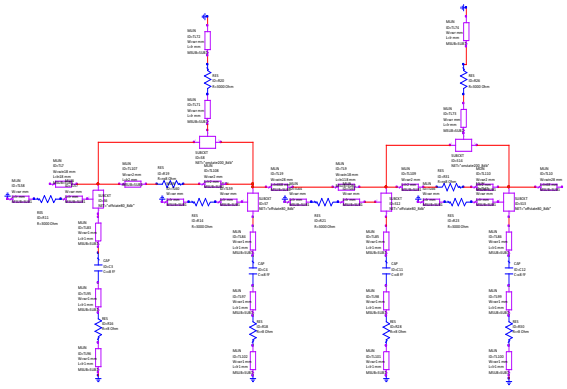


(b)

Fig. 3. T topology for0.5dB and 1dB attenuation (a). ON state (b) OFF state

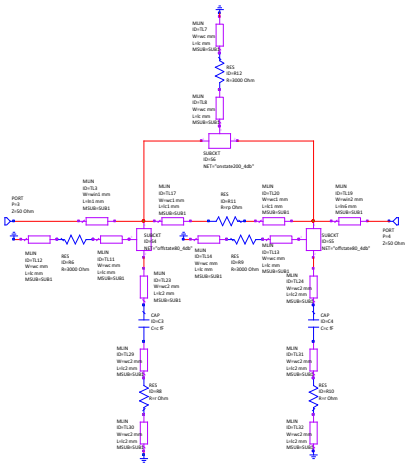


(a)



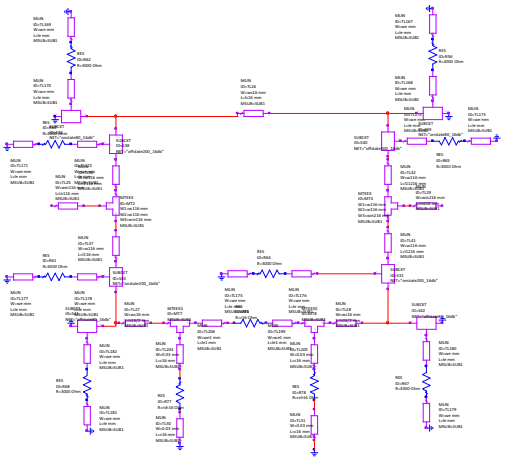
(b)

Fig. 5. Cascaded Pi topology for 8 db attenuation (a) ON state (b) OFF state

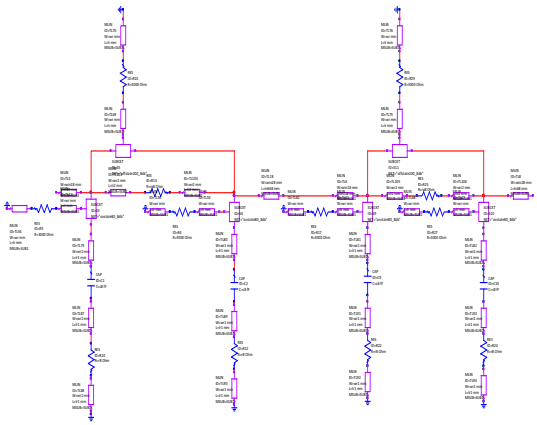


(b)

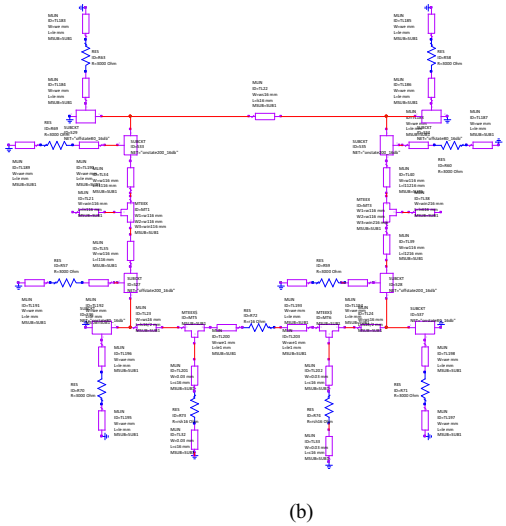
Fig. 4. Pi topology for 2db and 4dB attenuation (a) ON state (b) OFF state



(a)



(a)



(b)

Fig. 6. Bridged- Pi topology for16dB attenuation (a) ON state (b) OFF state

The T type topology is used for designing 0.5dB and 1 dB attenuation bits because small series resistances and high shunt resistance offer low attenuation and less insertion loss as well as good I/O return loss, whereas Pi topology is chosen for 2dB and 4dB bits. This Pi bit arrangement provides good I/O match, required attenuation and improvises insertion loss performance by offering two shunt resistances of medium to high values and a series resistance of small to medium value over entire band of 5-18GHz. The Pi-type topology is generally chosen for moderate value (2dB and 4dB) of attenuation since for low attenuation values series resistance becomes too low to realize as well as desensitize. For high attenuation values, the large series resistance values and lower values of shunt resistances are required. The higher values of series resistance tend to interact with off state impedance of series PHEMT switch resulting into more capacitive leakage at high frequency and also for higher power RF signal. Similarly, low values of shunt resistances causes the shunt branches to draw more leakage current when the shunt PHEMT switches are in off state. These phenomenon's causes more insertion loss to occur and also deteriorate the input output return loss. Therefore, for 8dB and 16dB cascaded Pi and switched-Pi topologies are designed to ensure low insertion loss and minimum phase shift respectively. For 8 dB attenuation bit, to reduce phase shift to minimum level over the entire band of 5-18GHz, compensatory capacitances are added in shunt branches of cascaded Pi type topologies to compensate the inductive phase shift introduced by inductive interconnects to connect switching PHEMTs and resistances in shunt branches as well as to keep the insertion loss low by reducing the leakage through the OFF state shunt PHEMTs switch as it makes capacitive impedance high in shunt branches. As attenuation value increases, it becomes difficult or impossible to obtain the optimum level of insertion loss, return loss and minimum phase shift over the bandwidth ranging from 5GHz to 18 GHz. Therefore for 8dB attenuation, two 4dB Pi-type attenuator bits are cascaded. For 16 dB attenuation bit, SPDT switches are used at the input and the output for highly isolating the reference path from the attenuation path so that pure Pi –type attenuator can be used in attenuation path without any switches to be used in series or shunt paths and thus easily achieves optimum insertion loss and optimum return loss for minimum phase shift. Also, 16dB switched path topology is adopted to minimize the space constraint of cascading 8dB attenuation states and improving attenuation accuracy and insertion phase shift over entire bandwidth at the same time.

Since the total attenuator consists of 6 bits and therefore 64 states each having its own attenuation, return loss, insertion loss and phase shift. So there placing must be done so as to minimize phase error and attenuation error at output for minimum required I/O return loss as well as insertion loss as shown in Fig. 7.

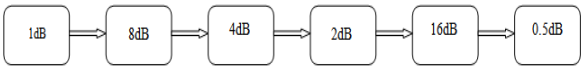


Fig. 7. Block Diagram of 6-bit attenuator

In order to further minimize the phase difference between reference path and attenuation path, in integrated six bits digital attenuator as shown in Fig. 8, the capacitances of series switches in OFF state are also compensated using smaller width (~20µm) microstrip line interconnects.

Transmission line parameters and lumped resistors are optimized during integration to have broadband performance.

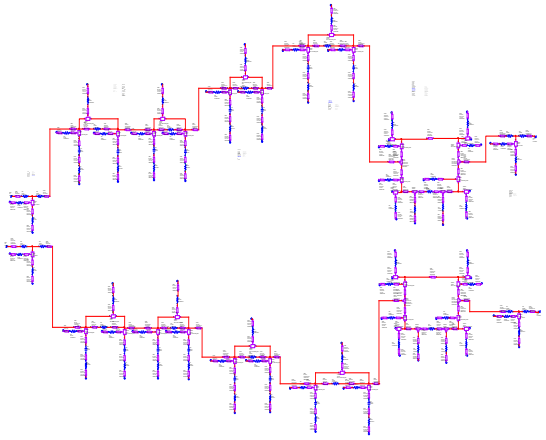


Fig. 8. Integrated 6-bit attenuator

TABLE I. COMPARISON SUMMARY

Fre (GHz)	Technology	Attenuation (dB)	Error (dB)
2-18	GaAs	31.5	-0.5 to +2.31
2-18	GaAs	31.5	-0.5 to +2.31
20-24	SiGe BiCMOS	31.5	±0.43
25-30	GaAs	31.5	±0.5
2-18	GaAs	10	±0.25
4-20	GaN	31.5	±0.5

III. RESULT AND DISCUSSION

6-bit ultra-broadband (5-20GHz) digital attenuator is designed and simulated as shown in Fig. 7and 8. GaN substrate of 100 µm thickness is chosen. Simulated results show high performance attenuator with the attenuation dynamic range of 0.5 to 31.5dB in steps of 0.5dB. The return loss and attenuation results of 6-bit digital attenuator are shown in Fig. 9.

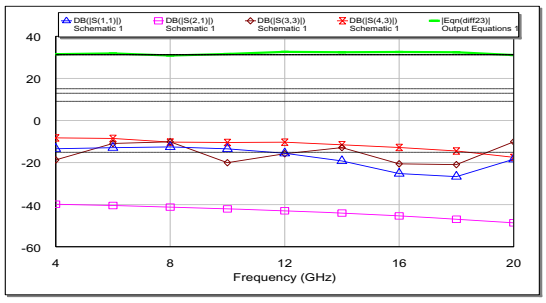


Fig. 9. Simulated result of attenuation and return loss

The return loss is relatively flat over the entire bandwidth with a value of approximately -15 dB for all attenuation states. Attenuation is also monotonic over the entire frequency range as depicted in Fig. 9. The accuracy is typically ±0.5dB over the entire frequency range for all attenuation states.

IV. CONCLUSION

A 5-20GHz MMIC digital attenuator has been simulated using AWR MWO. The attenuator is simulated using GaN PHEMT switches model for 0.25μm gate length process. All bits have been properly arranged to give attenuation and phase shift with minimum error for required I/O return loss and insertion loss.

REFERENCES

[1] M. Geng, P. X. Li, W. J. Luo, P. P. Sun, R Zhang, X. H. Ma, "Small-signal modeling of GaN HEMT switch with a new intrinsic elements extraction method" Chinese Physics B, vol. 25, No. 11, 2016.

[2] Y.S. Dai, P. Li, Q. F. Han, S. B. Chen, X. Chen, L. J. Wang, L. Xu, R. Q. Chen, "A Novel 2-18GHz PHEMT MMIC Digital Attenuator with Low Insertion Phase Shift" International Conference on Microwave and Millimeter Wave Technology (ICMMT), May 2012.

[3] Y. S. Dai, J. Zhang, B. Q. Dai, Z. D. Song, G. X. Qian, S. B. Chen, W. K Zhou, "An Ultra Broadband 2-18GHz 6-Bit PHEMT MMIC Digital Attenuator with Low Insertion Phase Shift" IEEE International Conference on Ultra-Wideband, 2010.

[4] M. Zhang, Sarfraz, M.M. Ullah, H. Liu, F. Wang, "A 6-Bit 0.13 μm SiGe BiCMOS Digital Step Attenuator with Low Phase Variation for K-Band Applications" Electronics, vol. 7, No. 74, 2018.

[5] J. Zhao, B. Zhang, X. Yang, "A 25-30 GHz 6-bit Digital Attenuator with High Accuracy and Low Insertion Loss" IEEE MTT-S International Wireless Symposium (IWS), March 2016.

[6] R. Mozzi, Y. Tajima, T. Tsukii, L. Hanes, E. Tong, B. Wrona, "GaAs monolithic wideband (2-18 ghz) variable attenuators" IEEE MTT-S International Microwave Symposium Digest, June 1982.

[7] A.M Osipov, L.M Semyonova, V.V Radchenko, "5-6 GHz band GaAs MMIC five bit digital attenuator," in Proc. Microwave & Telecommunication Technology, 2008, pp.118-119.

[8] N. Kinayman, M. Bonilla, M.F. Kelcourse, J. Redus, K.Anderson, "High-accuracy digital 5-bit 0.8-2 GHz MMIC RFattenuator for cellular phones," IEEE Trans. on Microwave Symposium Digest, vol. 3, pp.2231-2234,2001

[9] D. Krafcsik, F. Ali, S. Bishop, K. Anderson, "Broadband, low loss 5- and 6-bit digital attenuators," IEEE Trans. on Microwave Symposium Digest, vol. 3, pp.1627-1630,1995