A 6-Bit CMOS Phase Shifter for S-Band

Masoud Meghdadi, Mehrdad Azizi, Mehdi Kiani, *Student Member, IEEE*, Ali Medi, *Member, IEEE*, and Mojtaba Atarodi, *Member, IEEE*

***Abstract*—A 6-bit passive phase shifter for 2.5- to 3.2-GHz frequency band has been designed and implemented in a standard 0.18-μm CMOS technology. A new switched-network topology has been proposed for implementing the 5.625° phase shift step. The insertion loss of the circuit is compensated with an on-chip bidirectional amplifier. The measured return losses of the circuit are better than 8 dB with output 1-dB compression point of +9.5 dBm in the transmit mode and noise figure of 7.1 dB in the receive mode. The fabricated phase shifter demonstrates an average rms phase error of less than 2° over the entire operation bandwidth, which makes it suitable for high-precision applications.**

***Index Terms*—CMOS switch, impedance matching, phase-array system, phase shifter, rms phase error.**

I. Introduction

PHASE shifters are the key elements of beam steering systems such as phase array antennas. By using multiple antennas and adding the signal of each antenna with appropriate delay, the path difference of free space can be compensated. This compensation occurs at a predefined receiving angle and results in spatially selective signal and increased signal-to-noise ratio (SNR) at the receiver output [1]. A phased array can also utilize beamforming to transmit a signal in a specific direction and reduce the power dissipation of the transmitter.

Since phase array systems use many phase shifters both in transmit and receive paths, compact, low-power, and low-cost phase shifters are essential. Traditionally, phase shifters are implemented using III-V technologies such as GaAs [2], [3]. The high mobility of electrons and the high quality factor of passives in these technologies results in low insertion loss phase shifters. However, realization of phase shifters on silicon substrates will reduce their implementation costs significantly. In addition, other analog and digital circuits can be integrated on the same die, which makes the phase array system more compact and reliable.

The scanning accuracy and side lobe rejection of the beam former depends on the resolution of the phase shifter employed to implement variable delays [4]. The phase shift quantization error also reduces the SNR of the receiver at some receiving angles as the effect of different path delays are not fully compensated at these angles [5].

Manuscript received October 12, 2009; revised February 15, 2010; accepted August 12, 2010. Date of publication November 15, 2010; date of current version December 10, 2010.

M. Meghdadi, M. Azizi, A. Medi, and M. Atarodi are with the Department of Electrical Engineering, Sharif University of Technology, Tehran, Iran (e-mail: meghdadi@ee.sharif.edu; medi@sharif.edu).

M. Kiani is with the GT-Bionics Lab, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30308 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2010.2086310

Variable phase shifts can be achieved in different ways. In the vector summing method, the signal is decomposed into two quadrature signals. By weighting the amplitude of these signals and adding them, different phase shifts can be synthesized [6]. This method results in smaller die area, but unlike passive phase shifters, it only works in one direction. Also, the small dynamic range of the variable gain adder reduces the linearity of the phase shifter built using this method.

In passive implementations, the phase of the signal is changed either by changing electrical characteristics of its path or by switching it between different paths. In the first method, usually the electrical length of the synthetic line is changed by changing its capacitance, inductance, or both [7]–[9]. But this type of phase shifter produces the required phase shift steps only at a single frequency and the phase error increases linearly as the frequency offset becomes larger.

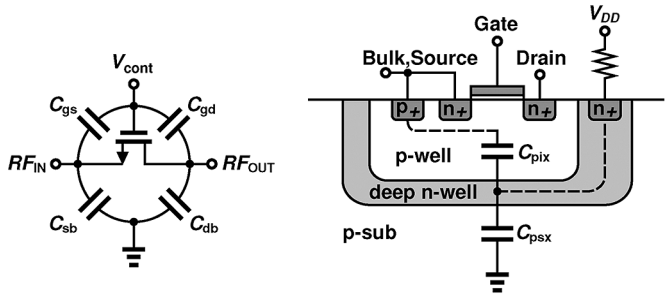
The signal path is switched between two networks in the switched-network topology [10], [11]. The phase response difference of these networks is the phase shift of the circuit. Potentially, this method has a wider bandwidth as the phase-frequency variations of one of the networks can be designed in a way that compensates variations of the other network within the frequency band of interest.

In this work, a 6-bit passive phase shifter has been implemented in a standard 0.18-μm CMOS technology using the switched network method. Section II describes methods for improving loss and linearity of MOS switches. Design details of different phase shift blocks are discussed in Section III. The proposed topology for implementing the 5.625° phase shift step is presented in Section IV. Design issues of the phase shifter are reviewed in Section V, followed by measurement results in Section VI.

II. Optimization of MOS Switches

The MOS switch is a major contributor to the insertion loss of a switched-network phase shifter as the switches are in series with the RF signal path. In silicon technologies, the MOS transistor suffers from low electron mobility and high parasitic capacitances compared to their III-V technology counterparts. The insertion loss of the switch is increased due to its on-resistance and capacitive coupling of the signal to ground.

Fig. 1(a) shows an NMOS transistor with its parasitic capacitances. To reduce the effect of gate-drain capacitance $(C_{\rm gd})$ and gate-source capacitance $(C_{\rm gs})$, the gate control voltage can be applied through a large resistor (e.g., 20 kΩ). This resistor also increases the linearity of the switch as the bootstrapping of the signal through $C_{\rm gd}$ reduces the variations of gate-source voltage $(V_{\rm GS})$ and hence lowers variation of the on-resistance of the transistor with respect to the input signal level. However,



(a) (b)

Fig. 1. MOS switch. (a) NMOS transistor and its parasitic capacitances. (b) Cross section of a triple well device and well parasitic capacitances.

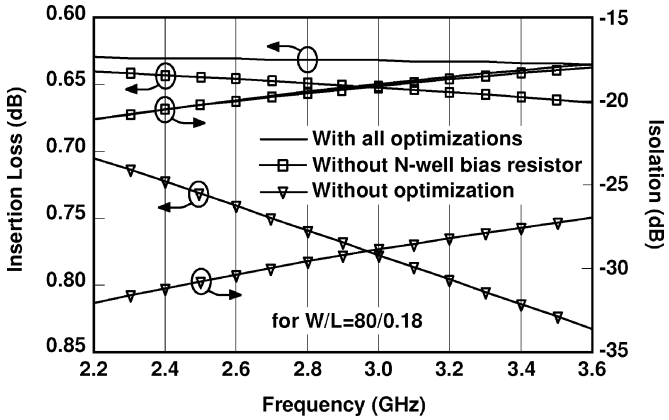


Fig. 2. Insertion loss and isolation of different MOS switches.

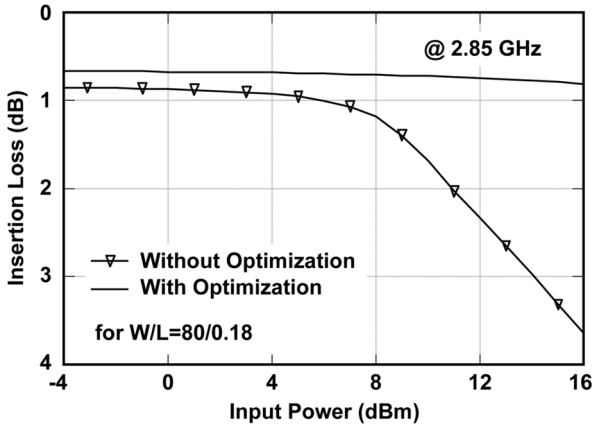


Fig. 3. Effect of optimizations on the linearity of switch.

adding this resistor results in series connection of $C_{\rm gd}$ and $C_{\rm gs}$ in off-state and decreases the isolation of the switch.

To omit the effect of source-bulk capacitance $(C_{\rm sb})$, the source and the body of the transistor can be tied together. In order to be able to do so, a triple well device [Fig. 1(b)] has to be used to realize the switch. Connecting source and body also improves the switch linearity as the threshold voltage $(V_{\rm TH})$ remains independent of the signal variations. However, by connecting source and body terminals, the effect of $C_{\rm pix}$ [Fig. 1(b)] should also be considered in the insertion loss of the switch. This capacitance is normally neglected in transistor models but for large transistors it can have a significant effect on the performance of the switch. Since the $C_{\rm psx}$ [Fig. 1(b)] is smaller than $C_{\rm pix}$, the effect of $C_{\rm pix}$ can be reduced by biasing the deep n-well with a large resistor [12]. Also, source and drain of the switches are biased at 0.9 V to improve the linearity and the operation range of them. The control voltage is changed between 2.7 and 0 V for turning the switches on and off, respectively. Consequently, the signal level which turns on the switch in the off-state is increased.

Fig. 2 shows effects of the discussed techniques on the insertion loss and the off-state isolation of an MOS switch. As this figure shows, tying body to source and biasing the gate and deep n-well with large resistors reduces the insertion loss of the switch by more than 0.13 dB while its isolation is still reasonable. Since in the designed 6-bit phase shifter, nine switches were used in series with the RF signal path, the overall loss can be reduced by more than 2.4 dB. The effect of these optimizations on the linearity of a switch is depicted in Fig. 3. The optimized switch shows significant improvement in the 1-dB compression point.

III. Phase Shifter Circuit Design

In S-band, the required die area of the distributed elements such as microstrip lines would be too large. Thus, to have a compact phase shifter, lumped elements must be used. The topologies of the phase shifting blocks must be chosen in a way that results in reasonable component size, insertion loss, and flat phase shift-frequency response in the band of interest.

To obtain 6-bit resolution, the individual blocks must have small phase shift errors. In addition to the phase shift variations with frequency, the component variations also add up to the phase error. In this work, different network topologies were compared for each phase shifting block at different process corners and temperatures. Eventually, the networks with the lowest sensitivity to the component and temperature variations were selected for implementing the circuits in the chosen technology.

A. 180° and 90° Phase Shift Blocks

For realizing the 180° phase shift block, the high-pass/low-pass topology is used. The filters in this topology are designed to have similar phase-frequency slope while they have 180° phase difference. Thus, the phase shift difference between the two states of the circuit remains constant in a wider frequency bandwidth.

The low-pass and high-pass filters are usually realized by third-order networks, but to reduce the loss of the circuit in the operation bandwidth while improving the constant phase shift bandwidth simultaneously, a fifth-order low-pass network is employed (Fig. 4). This network provides 110° of phase lag while the 70° of phase lead is provided by the high-pass network. The sizes of the switches were optimized to make the insertion loss of the block equal at both states.

As suggested in [10], the 90° phase shift can be achieved by switching signal between the $\lambda/4$ transmission line and a parallel resonator. At lower frequencies, the transmission line can be replaced with low-pass network (Fig. 5). Once again, the low-pass section is realized by a fifth-order network to improve

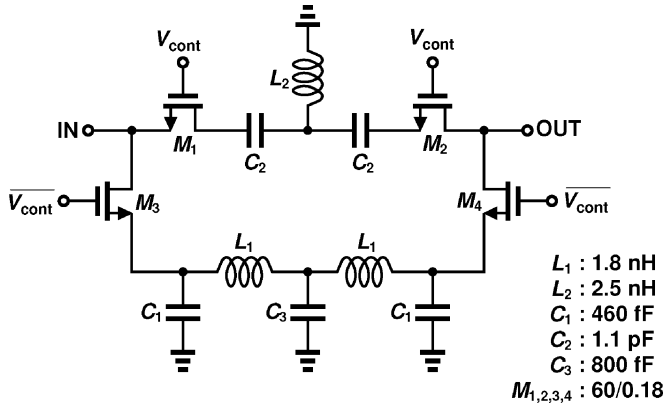


Fig. 4. Schematic of the 180° phase shift circuit.

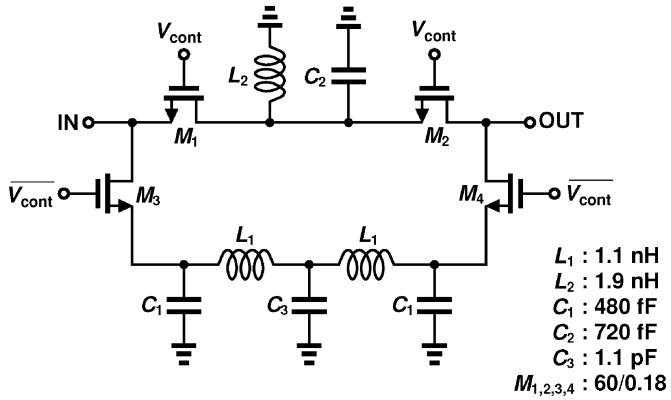


Fig. 5. Schematic of the 90° phase shift circuit.

insertion loss and the flat phase shift in the band of interest. This section provides 90° phase shift at 2.85 GHz. The band-pass section compensates the phase-frequency slope of the low-pass section while it has zero phase shift at 2.85 GHz.

B. 45°, 22.5°, and 11.25° Phase Shift Blocks

The topology of Fig. 6(a) is commonly used for realizing these blocks. In this topology, the signal path is switched between the low-pass and band-pass networks. In one state, M_1 and M_2 are off and M_3 is on, the circuit is equivalent to the circuit of Fig. 6(b) where C_1 is the sum of C_a and the off-state capacitances of M_2. At the center frequency of operation, this network is designed to give the desired phase shift. In the other state, M_1 and M_2 are turned on and M_3 is turned off. The equivalent circuit of this state is shown in Fig. 6(c), where C_2 is the sum of C_a, C_b, and the off-state parasitic capacitances of M_3. This configuration provides zero phase shift at the center frequency while its phase-frequency slope is equal to the phase-frequency slope of the low-pass network. Compared to the topologies of Figs. 4 and 5, this topology has lower insertion loss as it has only one series switch in the RF signal path.

As it is shown in [10], the optimum component values for maximum constant phase shift bandwidth and best matching at

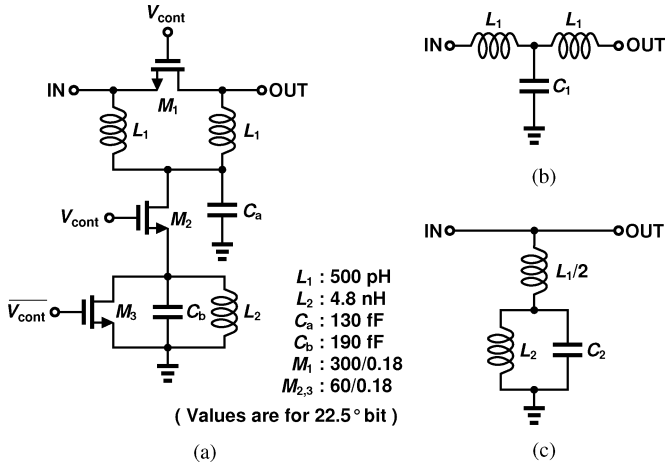


Fig. 6. The circuit for 45°, 22.5°, and 11.25° blocks. (a) Schematic of the phase shift block. (b) Equivalent circuit at phase shifting state. (c) Equivalent circuit for compensation of phase variation.

the center frequency of operation can be calculated by using the following equations:

$$C_1 = \frac{\sin(\Delta\varphi)}{Z_0\omega_0}, \quad L_1 = \frac{Z_0\tan(\Delta\varphi/2)}{\omega_0} \tag{1a}$$

$$C_2 = \frac{2\tan(\Delta\varphi/2)}{Z_0\omega_0}, \quad L_2 = \frac{1}{C_2\omega_0^2} \tag{1b}$$

where $\Delta\varphi$ is the desired phase shift, ω_0 is the center frequency, and Z_0 is the termination impedance. In physical implementations, a single center-tap inductor is used for realizing two L_1 inductors. This would result in reduced die area and shorter paths with lower parasitics.

IV. The Proposed 5.625° Phase Shift Block

According to (1), achieving small phase shift steps in a wide frequency range using the topology of Fig. 6 results in impractical component values, i.e., large L_2 and very small C_2. In addition to occupying a large chip area, the parasitic capacitance of a large inductor makes the realization of very small C_2 nearly impossible.

The suggested circuit in Fig. 7 can provide small phase shifts using small inductors at the cost of an additional series switch. In this configuration, the series LC section is used to compensate the phase variations of the low-pass section. To derive the equations for calculating the optimum component values, the S parameters of the networks were calculated using the transmission matrix parameters. For the low-pass T-section of Fig. 7, S_{11} and S_{21} of the circuit can be expressed with the following equations:

$$S_{11} = \frac{j\left(2L_1\omega - L_1^2C_1\omega^3 - Z_0^2C_1\omega\right)}{2Z_0(1-L_1C_1\omega^2) + j\left(2L_1\omega - L_1^2C_1\omega^3 + Z_0^2C_1\omega\right)} \tag{2}$$

$$S_{21} = \frac{2Z_0}{2Z_0(1-L_1C_1\omega^2) + j\left(2L_1\omega - L_1^2C_1\omega^3 + Z_0^2C_1\omega\right)}. \tag{3}$$

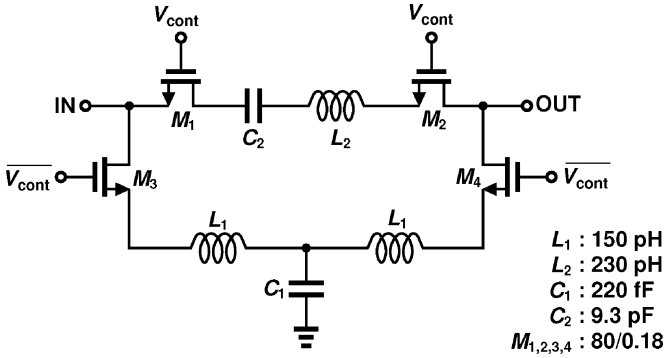


Fig. 7. Schematic of the 5.625° phase shift circuit.

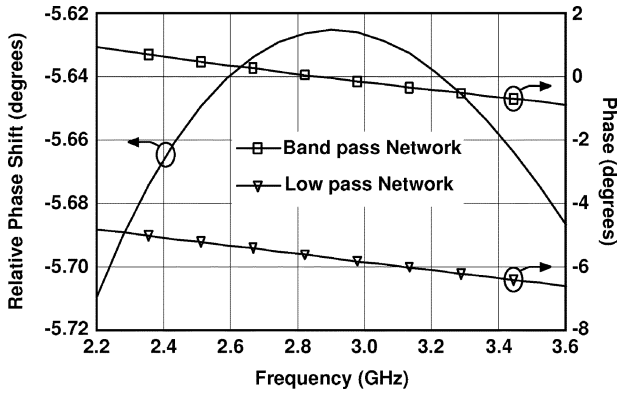


Fig. 8. Phases of the two networks in Fig. 7 and their difference.

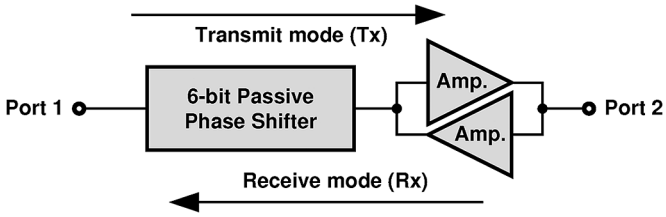


Fig. 9. RF signal path in transmit and receive modes.

The phase of S_{21} at the center frequency is equal to the desired phase shift of this block:

$$\Delta\varphi = -\tan^{-1}\left(\frac{2L_1\omega_0 - L_1^2C_1\omega_0^3 + Z_0^2C_1\omega_0}{2Z_0\left(1 - L_1C_1\omega_0^2\right)}\right). \quad (4)$$

In order to satisfy the impedance matching condition of the network, S_{11} is set to zero at the center frequency. This results in the following relation between L_1 and C_1:

$$C_1 = \frac{2L_1}{L_1^2\omega_0^2 + Z_0^2}. \quad (5)$$

Solving (4) and (5) together for L_1 and C_1 leads to the following equations:

$$L_1 = \frac{Z_0\tan(\Delta\varphi/2)}{\omega_0}, \quad C_1 = \frac{\sin(\Delta\varphi)}{Z_0\omega_0}. \quad (6)$$

To obtain the phase frequency slope of this network at center frequency of operation, the derivative of the insertion phase has to be found by applying the conditions in (6):

$$\frac{d}{d\omega}\left(-\tan^{-1}\left(\frac{2L_1\omega - L_1^2C_1\omega^3 + Z_0^2C_1\omega}{2Z_0(1 - L_1C_1\omega^2)}\right)\right)\Bigg|_{\omega=\omega_0} = \frac{-2L_1}{Z_0}. \quad (7)$$

For wideband performance, the band-pass section is designed to have the same phase slope at the center frequency. The scattering parameters of the band-pass section are expressed with the following equations:

$$S_{11} = \frac{j(L_2C_2\omega^2 - 1)}{2Z_0C_2\omega + j(L_2C_2\omega^2 - 1)} \quad (8)$$

$$S_{21} = \frac{2Z_0C_2\omega}{2Z_0C_2\omega + j(L_2C_2\omega^2 - 1)}. \quad (9)$$

Impedance matching condition for this network requires

$$L_2 = \frac{1}{C_2\omega_0^2}. \quad (10)$$

By satisfying the impedance matching condition, the derivative of phase at the center frequency can be expressed with the following equation:

$$\frac{d}{d\omega}\left(-\tan^{-1}\left(\frac{L_2C_2\omega^2 - 1}{2Z_0C_2\omega}\right)\right)\Bigg|_{\omega=\omega_0} = \frac{-1}{Z_0C_2\omega_0^2}. \quad (11)$$

Equating (7) and (11) results in the following set of equations for calculation of C_2 and L_2:

$$L_2 = \frac{2Z_0\tan(\Delta\varphi/2)}{\omega_0}, \quad C_2 = \frac{1}{2Z_0\omega_0\tan(\Delta\varphi/2)}. \quad (12)$$

As these equations suggest, the circuit can achieve wideband performance with small inductor sizes. Fig. 8 shows the simulation results for the individual phases of the discussed networks and their difference which is the relative phase shift of the block. The simulated phase shift of this circuit has less than 0.1° error in the operation bandwidth while realizing a 5.625° phase shift step. The insertion loss of this block is 2.2 dB.

V. The 6-Bit Phase Shifter

All the phase shift blocks have been cascaded to form the 6-bit phase shifter. The simulation results show an insertion loss of 13 dB for the cascaded blocks. To compensate this loss, a bidirectional amplifier is used. As the input power to the phase shifter is higher in the transmit mode, the amplifier is placed at the receiving end of the circuit as shown in Fig. 9 to have minimum effect on 1-dB compression point in the transmit mode and to improve noise figure in the receive mode.

Fig. 10 shows the simplified schematic of this amplifier. At transmitting state, M_3 is turned off by lowering its gate voltage

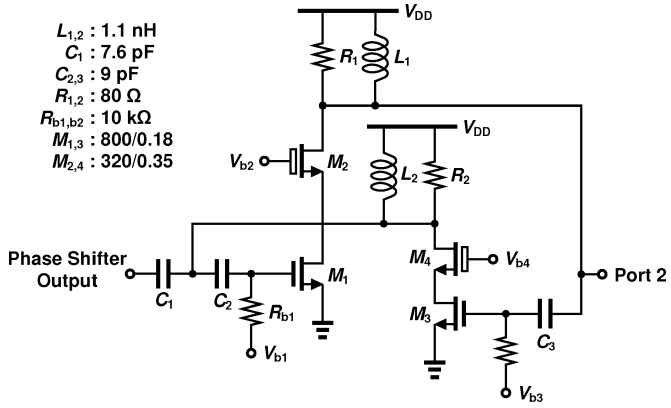


Fig. 10. Schematic of the bidirectional amplifier.

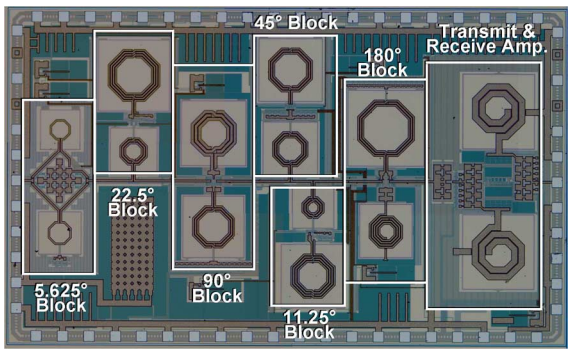


Fig. 11. Die micrograph of the phase shifter (2.6×1.6 mm^2).

while M_1 is biased in its active region. The cascode transistor is used to increase the stability of the circuit and to improve reverse isolation. The bias voltage of the cascode transistors are lowered when their respective amplifiers are turned off. The input and output matching of the amplifier is achieved by canceling out the parasitic capacitances of the transistors with inductors at the center frequency of operation.

The bias current of M_1 and M_3 can be adjusted between 10 and 50 mA with 4-bit resolution through the bias network (not shown). Therefore, the gain of the phase shifter can be adjusted between -10 and 5 dB, which makes it more suitable for phase array systems.

The phase shift of each block is sensitive to its termination impedances, and therefore cascading blocks affects the phase performance. Thus, the arrangement of blocks in the chain has been selected to minimize their loading effects. Afterward, the sizes of the components of each block have been readjusted considering the loading effect of the other blocks, parasitic components of the package, and ESD protection circuits. Finally, in order to extract and evaluate coupling effects, different parts of the layout have been exported to Agilent ADS Momentum for EM simulations and further optimizations.

VI. Measurement Results

The phase shifter is fabricated in a 0.18-μm 1P6M standard CMOS process with on chip inductors ($Q = 9$) and MIM capacitors. Fig. 11 shows the die micrograph of the fabricated chip. The die area including the bonding pads and the bidirectional

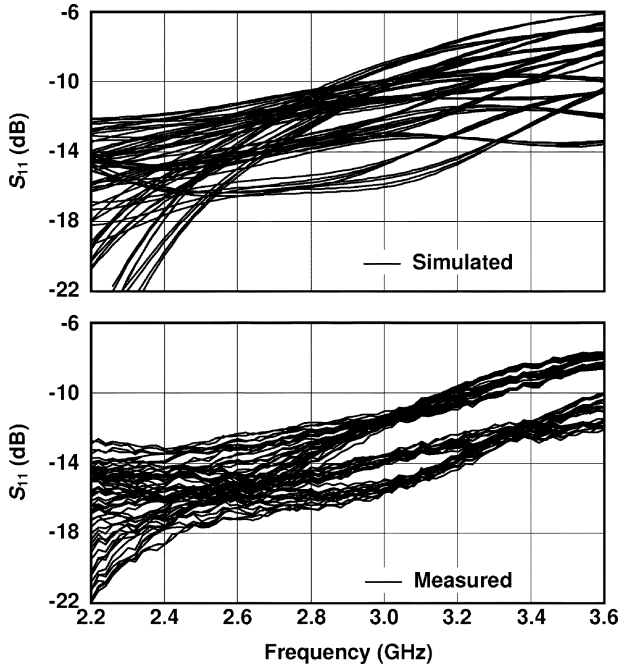


Fig. 12. Measured and simulated S_{11} of the circuit in Tx mode.

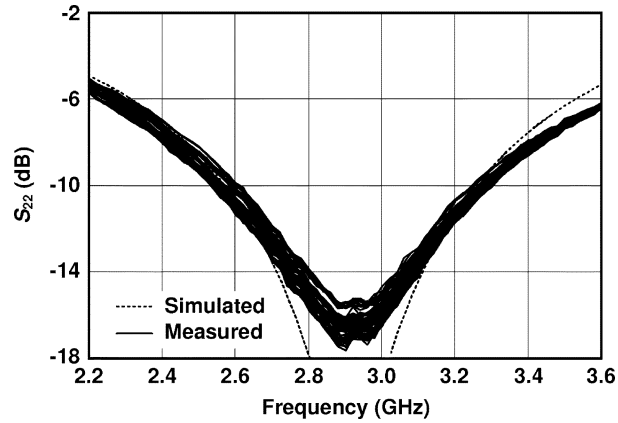


Fig. 13. Measured and simulated S_{22} of the circuit in Tx mode.

amplifier is 2.6 mm $\times$ 1.6 mm. The dies were packaged in a 40-pin QFN package. The scattering parameters of the circuit were measured using an Agilent 8722 network analyzer.

The measured and simulated scattering parameters of the circuit for all 64 phase shift states are shown in Figs. 12–15 for the transmit mode of operation. The port numbers in the figures are chosen with reference to Fig. 9. Since the bidirectional amplifier is fully symmetric, the phase shifter shows similar scattering parameters in the receive mode.

The measured return losses for Ports 1 and 2 over the 2.5- to 3.2-GHz frequency band are better than 10 dB and 8 dB, respectively. As Fig. 13 shows, the S_{22} of the circuit does not change considerably by changing the phase shift states, which is caused by the reasonable reverse isolation of the amplifier. Fig. 14 shows the reverse isolation of the chip, and Fig. 15 shows the insertion losses of the phase shifter. Compared to the simulation, the measurement results show 1 dB increase in the insertion loss, which is around 2.5 dB at the center frequency when

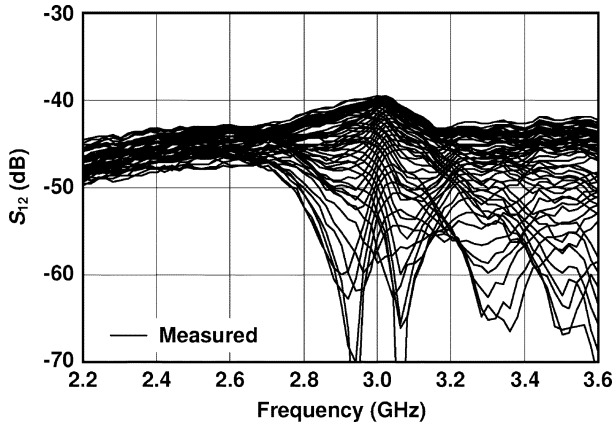


Fig. 14. Measured S_{12} of the circuit in Tx mode (The simulated S_{12} is not shown due to the lack of modeling accuracy).

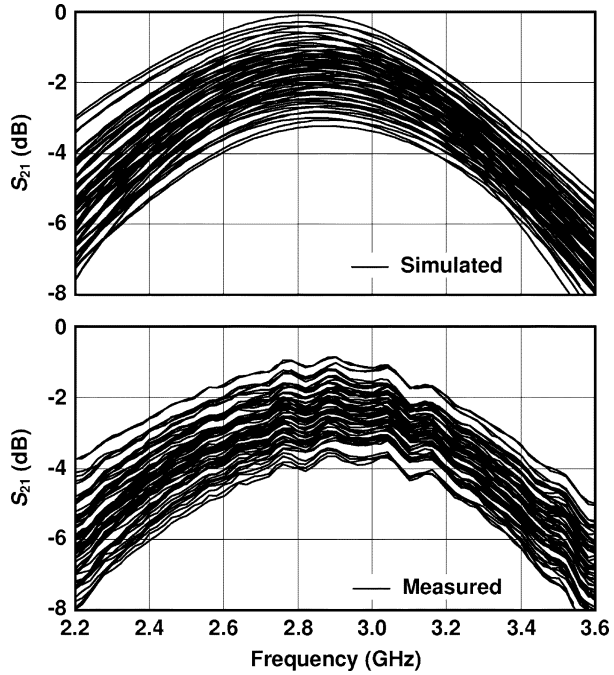


Fig. 15. Measured and simulated S_{21} of the circuit in Tx mode.

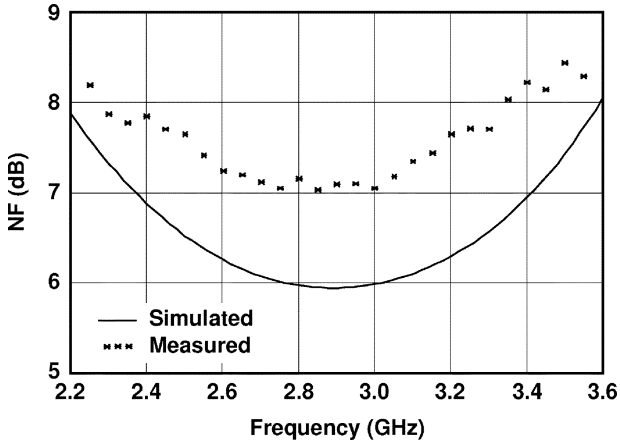


Fig. 16. Measured and simulated noise figure of the circuit in Rx mode.

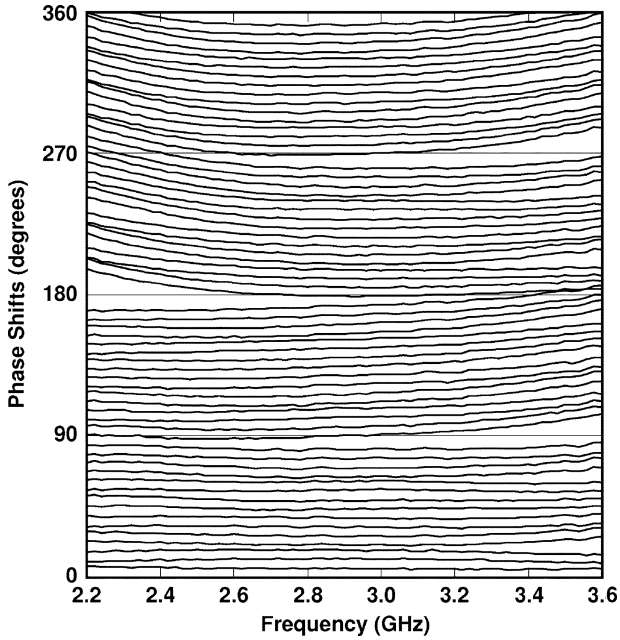


Fig. 17. Measured phase shifts of the circuit at all states.

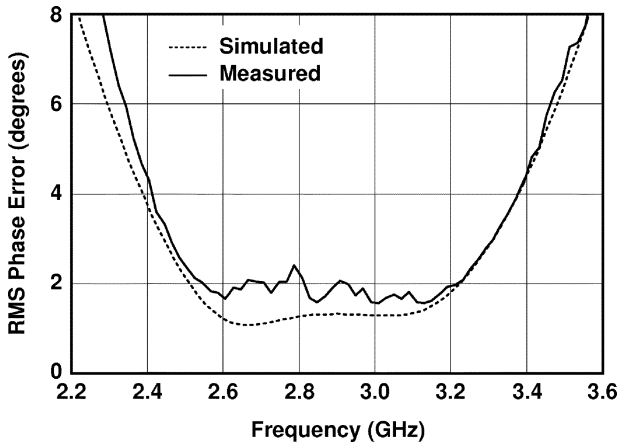


Fig. 18. Measured and simulated rms phase error.

the amplifier consumes 18 mA. The insertion loss has less than ± 1.5 dB variations by changing the states of the phase shifter.

The measured noise figure of the phase shifter in the center frequency is 7.1 dB in receive mode as shown in Fig. 16. The measured noise figure profile is consistent with the simulation results; however, an increase of more than 1 dB can be noticed which is mostly due to the increase in the insertion loss. The output 1-dB compression point of the phase shifter plus amplifier is measured to be $+9.5$ dBm in the transmit mode.

Fig. 17 shows the phase shift of all 64 states of the circuit with respect to the reference state. The phase shift increases monolithically but the limited constant phase shift bandwidth of 180° and 90° blocks increases the phase shift error at the both ends of the band of interest.

The rms phase error of the circuit is depicted in Fig. 18. The average measured rms phase error over the entire operation bandwidth is less than 2°, which is smaller than half of the LSB step. This small phase error reduces the size of lookup tables and calibration time for high-precision phase array systems.

TABLE I
COMPARISON OF SOME RECENT PHASE SHIFTERS

Ref.	[3]	[13]	[14]	[10]	[15]	[16]	This work
Technology	0.4-μm GaAs	0.18-μm SiGe	0.18-μm CMOS	0.18-μm CMOS	0.5-μm GaAs	0.13-μm CMOS	0.18-μm CMOS
Implementation Method	Switched Network	Vector Summing	Synthetic Line	Switched Network	Switched Network	Vector Summing	Switched Network
Frequency (GHz)	2.3 - 3.8	6 - 18	11.6 - 12.6	9 - 15	S-Band	23 - 24.4	2.5 - 3.2
Normalized Bandwidth	0.49	1	0.08	0.5	0.1	0.06	0.25
Phase Resolution (bits)	4	4	4	5	5	6	6
Input 1-dB Compression (dBm)	N/A	N/A	N/A	N/A	+21	-29 [a]	+12 / +2 (Tx / Rx)[b]
Noise Figure (dB)[c]	4	N/A	N/A	15.5	6.1	6	18 / 7.1 (Tx / Rx)
Gain (dB)	-4$\pm$0.8	N/A	3.5$\pm$0.5	-15.5$\pm$3.5	-6.1$\pm$0.6	14	-2.5$\pm$1.5
Return Loss (dB)	$>$10	N/A	15	8	10	$>$10	8
RMS Phase Error	3°	5.7°	5.5°	12°	2.8°	2.8°	2°
Die Area (mm^2)	2.4$\times$1.1	N/A	1.88$\times$0.91	3.1$\times$1.4	1.87$\times$0.87	1.25$\times$0.66	2.6$\times$1.6
DC Power (mW)	0	N/A	26.6	0	0	45	60

[a]Limited by the used three-stage amplifier.
[b]The output referred 1-dB compression point is +9.5 dBm in the transmit mode.
[c]Noise figure is assumed to be equal to insertion loss in passive phase shifters.

Table I compares the measured performance of the fabricated circuit with some recently reported works. For fair comparison of constant phase shift bandwidth, the bandwidths of different circuits are normalized to their center frequency of operation. The reported phase shifter has a small rms phase error with a reasonable fractional bandwidth.

VII. CONCLUSION

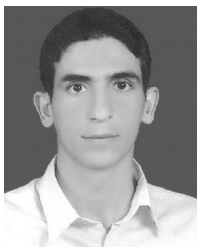
A 6-bit passive phase shifter has been implemented in a 0.18-μm CMOS technology. The design employs the switched-network topology for achieving wide bandwidth with flat phase shifts. It covers the frequency band from 2.5 to 3.2 GHz with an average rms phase error of less than 2°. Loss and linearity of MOS switches have been optimized considering all parasitic capacitances of the triple well devices. The uncompensated insertion loss of the fabricated passive circuit is around 13 dB. The input and output return losses of the circuit are better than 10 dB and 8 dB, respectively. A new topology is proposed for implementing small phase shift steps. The measurement results show the practicality of this topology for small phase shift steps.

REFERENCES

[1] A. M. Niknejad and H. Hashemi, *mm-Wave Silicon Technology: 60 GHz and Beyond*. Berlin, Germany: Springer-Verlag, 2008.
[2] C. F. Campbell and S. A. Brown, "A compact 5-bit phase-shifter MMIC for K-band satellite communication systems," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 12, pp. 2652–2656, Dec. 2000.
[3] I. J. Bahl and D. Conway, "L- and S-band compact octave bandwidth 4-bit MMIC phase shifters," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 2, pp. 293–299, Feb. 2008.
[4] R. J. Mailloux, *Phased Array Antenna Handbook*. Boston, MA: Artech House, 1991.
[5] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe phased-array receiver-LO phase-shifting approach," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 614–626, Feb. 2005.
[6] K. J. Koh and G. M. Rebeiz, "0.13-μm CMOS phase shifters for X-, Ku-, and K-band phased arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535–2546, Nov. 2007.
[7] F. Ellinger, H. Jackel, and W. Bachtold, "Varactor-loaded transmission-line phase shifter at C-band using lumped elements," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 4, pp. 1135–1140, Apr. 2003.
[8] L. H. Lu and Y. T. Liao, "A 4-GHz phase shifter MMIC in 0.18-μm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 10, pp. 694–696, Oct. 2005.
[9] T. M. Hancock and G. M. Rebeiz, "A 12-GHz SiGe phase shifter with integrated LNA," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 3, pp. 977–983, Mar. 2005.
[10] D. W. Kang, H. D. Lee, C. H. Kim, and S. Hong, "Ku-band MMIC phase shifter using a parallel resonator with 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 294–301, Jan. 2006.
[11] M. A. Morton, J. P. Comeau, J. D. Cressler, M. Mitchell, and J. Papapolymerou, "Sources of phase error and design considerations for silicon-based monolithic high-pass/low-pass microwave phase shifters," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4032–4040, Dec. 2006.
[12] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1–10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.
[13] K. J. Koh and G. Rebeiz, "An X- and Ku-band 8-element phased-array receiver in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1360–1371, Jun. 2008.
[14] D. W. Kang and S. Hong, "A 4-bit CMOS phase shifter using distributed active switches," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 7, pp. 1476–1483, July 2007.
[15] M. Hangai, M. Hieda, N. Yunoue, Y. Sasaki, and M. Miyazaki, "S- and C-band ultra-compact phase shifters based on all-pass networks," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 1, pp. 41–47, Jan. 2010.
[16] T. Yu and G. M. Rebeiz, "A 24 GHz 6-bit CMOS phased-array receiver," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 6, pp. 422–424, Jun. 2008.

Masoud Meghdadi received the B.Sc. degree from Amirkabir University of Technology, Tehran, Iran in 2005, and the M.Sc. degree from Sharif University of Technology, Tehran, Iran, in 2007, both in electrical engineering. Currently, he is working toward the Ph.D. degree at the ISDL Laboratory, Sharif University of Technology. His general research interests are high-speed and low-power CMOS circuits and RF building blocks.

Mehrdad Azizi received the B.Sc. degree in electrical engineering (with honors) from K. N. Toosi University of Technology, Tehran, Iran, in 2007, and the M.Sc. degree in electronic engineering from Sharif University of Technology, Tehran, Iran, in 2009. His research interests include design of analog and RF CMOS integrated circuits.



Mehdi Kiani (S'09) received the B.Sc. degree from Shiraz University, Shiraz, Iran, in 2005 and the M.Sc. degree from Sharif University of Technology, Tehran, Iran, in 2008.

He joined GT-Bionics Lab at Georgia Institute of Technology, Atlanta, in 2009.

Ali Medi (S'98-M'08) received the B.Sc. degree from the Sharif University of Technology, Tehran, Iran, in 2001, and the M.Sc. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, in 2003 and 2007, respectively.

He is currently an Assistant Professor in the Electrical Engineering Department of the Sharif University of Technology. He was a Research Assistant with the UltRaLab, where he worked in the field of analog and RF circuit design for ultra-wideband systems. He was with Broadcom Corporation developing RF blocks for GSM cellular phone transceivers. His research interests are CMOS transceivers, RF front-ends, frequency synthesizers, and wideband analog circuit design.

Mojtaba Atarodi (M'93) received the B.S.E.E. degree from Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran, in 1985, the M.Sc. degree in electrical engineering from the University of California, Irvine, in 1987, and the Ph.D. degree from the University of Southern California (USC), Los Angeles, on the subject of analog IC design in 1993.

From 1993 to 1996, he worked with Linear Technology Corporation as a senior analog design engineer and participated in the design of two IC products in the field of high-frequency high dynamic range continuous-time G_m–C filters. Since then, he has been consulting with different IC companies. He is currently an Associate Professor at Sharif University of Technology. He has published more than 80 technical journal and conference papers in the area of analog/RF and mixed-signal integrated circuit design. He is the author of "Analog CMOS IC Design." He has managed several IC design projects resulted in several IC products, namely, SIM card IC, smart card IC, PCM codec, and DVB-T/H tuner. He holds one U.S. patent. His main research interests are integrated bioelectronics, RF/analog/mixed-signal ICs, and integrated circuits for digital TV receivers.