# A 77-101GHz 6-Bit Vector-Modulated Phase Shifter with Low RMS Error in 65nm SOI CMOS

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***Abstract*—This paper presents a 77-101 GHz active 6-bit phase shifter based on a vector-modulated technique in 65nm SOI CMOS technology for W-band phased-array systems. Optimizations of the impedance-invariant variable gain amplifier (VGA) are performed to reduce the phase error and gain error among the phase states. In addition, a quadrature signal generator composed of a 90-degree hybrid and a pair of Marchand balun is exploited for wideband applications. The proposed phase shifter achieves 5.6° phase step, < 2.0° RMS phase error and < 0.8dB RMS gain error over 77-101 GHz. The total power consumption is 31mW and the core area of the phase shifter is only 0.2mm$^2$.**

***Keywords*—W-band, phase shifter, vector-modulated, SOI CMOS**

## I. Introduction

W-band (75-110 GHz) provides a promising opportunity for implementation in highly directive wireless communications and high-resolution imaging systems. Therefore, as an important part of phased-array systems, the W-band phase shifter have been an active research field in recent years [1]-[4].

Phase shifter is component in phased-array systems to provide phase shifting, which can be divided into passive form and active form. Passive phase shifters, mainly including reflective-type phase shifter (RTPS) and switched-type phase shifter (STPS), typically exhibit high linearity performance, but also high losses, high noise figure (NF) and large chip area. For active phase shifters, such as vector modulation phase shifters, compared with passive phase shifters, typically exhibit higher gain, smaller chip area, higher phase shift resolution and full phase shifting range [2].

This paper presents a vector modulation phase shifter with a wideband quadrature signal generator composed of a 90° hybrid and a pair of Marchand balun and an impedance-invariant variable gain amplifier (VGA) in 65nm SOI CMOS technology. This design enables large bandwidth, low RMS phase error, low RMS gain error, and compact chip design.

## II. Phase Shifter Design

Fig. 1 shows an architecture of a vector modulation active phase shifter. The vector modulator phase shifter is based on an IQ signal Generator, two impedance-invariant VGAs and an output combiner.

### A. IQ Signal Generator

As we know, the phase error and amplitude imbalance of the IQ signal generator have a critical effect on the overall performance of the phase shifter. Thus, as a crucial part of the IQ signal generator, the 90° Hybrid and Balun designs with good phase and amplitude characteristics are necessary.

Lange coupler has symmetrical layout and ultra-wideband characteristics, and is more suitable for use in high frequency environment, such as W-band, than spiral coupler [3]. The structure of the Lange coupler is shown in Fig. 2(a). Fig. 2(c) shows the EM simulation results of the Lange coupler. It can be found that the Lange coupler has a flat intersection area between the I path and the Q path, which greatly improves the bandwidth, and also has good phase characteristics in the frequency range of 70-110 GHz.

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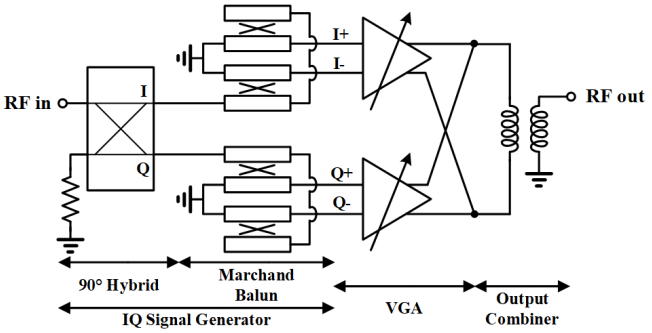


Fig. 1. Architecture of vector-modulated phase shifter

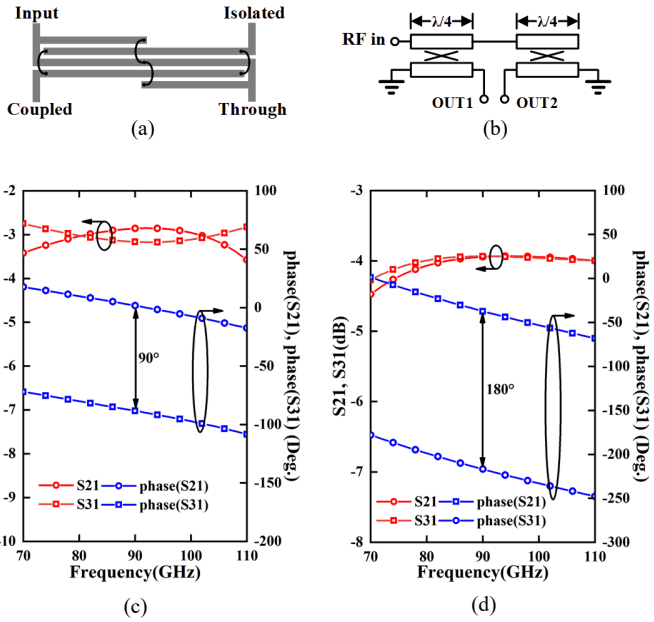


Fig. 2. (a) Lange Coupler. (b) Marchand Balun. (c) Simulation amplitude and phase of S21 and S31 of (a). (d) Simulation amplitude and phase of S21 and S31 of (b)

Marchand balun has the advantage of bandwidth compared with the transformer structure in high frequency environment [5]. The structure of Marchand Balun is shown in Fig. 2(b). Fig. 2(d) is the EM simulation results of Marchand balun, in the frequency range of 70-110 GHz, its amplitude imbalance and phase error are less than ±0.2 dB and ±1.4° respectively.

### B. Impedance-Invariant VGA

In [6], a one shack impedance-invariant VGA to reduce phase and amplitude error of phase shifter is presented. For this architecture, a large number of capacitors are used to isolate DC control signals and RF signals, which greatly increases the layout area and is difficult to apply in high-resolution phase shifters.

To further overcome the aforementioned issues and improve the performance of phase shifters, an impedance-invariant VGA based on cascode structure is proposed, as shown in Fig. 3. First, to keep the input impedance and the output impedance of the VGA remain constant for all gain states, digital signals are used to control the size of transistors. The details of its work are as follows. A large transistor is divided into N unit transistors to form a transistor array, so that the equivalent transistor size of the access circuit can be adjusted by turning on and off the number of unit transistors. The signal path of VGA is divided

2022 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA) | 978-1-6654-9269-0/22/$31.00 ©2022 IEEE | DOI: 10.1109/ICTA56932.2022.9963067

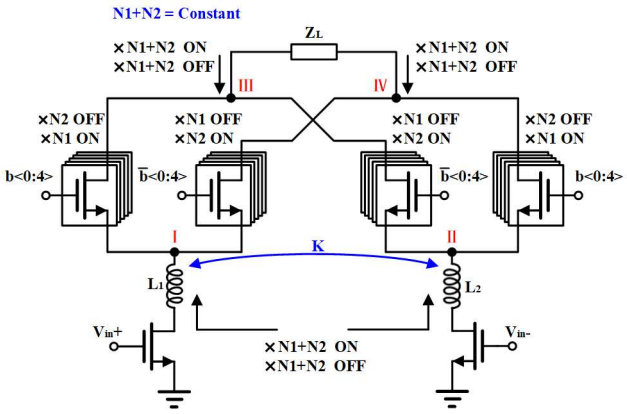


Fig. 3. Schematic of Impedance-Invariant VGA

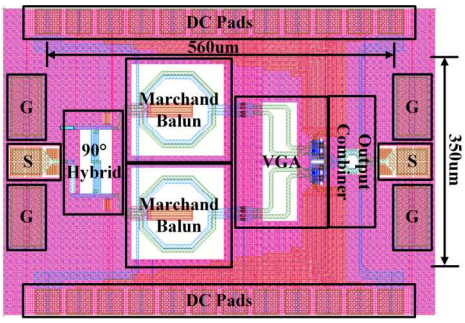


Fig. 4. Layout of vector-modulated phase shifter

into two paths, to ensure that one path has N1 transistors with on-state and N2 transistors with off-state at the same time, while the other path has N2 transistors with on-state and N1 transistors with off-state. By making N1+N2 to be a constant (N1+N2 = N), there will always be N transistors turned on and N transistors turned off at nodes I and II. Similarly, nodes III and IV also maintain N on-state transistors and N off-state transistors. Second, the DC control signals and RF signals use different paths to drive the common-gate transistors and common-source transistors respectively, eliminating the dependence on isolation capacitors. Third, $L_{1\text{-}2}$ can improve the gain of the VGA [2], but inductors will occupy a large chip area. Therefore, the introduction of weakly coupling (K=0.2) inductors allows for a more compact design.

## III. Simulation Results

The proposed 77-101 GHz 6bit vector-modulated phase shifter is implemented in a 65nm SOI CMOS technology. Fig. 4 shows the layout and the core area of the phase shifter. It occupies an area of $0.56\times0.3\text{mm}^2$ excluding pads. Fig. 5 is the simulation results of the phase shifter with its passive part evaluated by the full layout EM simulation. Fig. 5(a), (b) are the simulation results of S11 and S22 in all states, respectively. S11 remains below than -10dB from 70 to 104 GHz. S22 is below than -10dB from 83 to 104.5 GHz. S21 for all states and RMS gain error are shown in Fig. 5(c). The proposed phase shifter exhibits the 3-dB bandwidth from 77 to 101 GHz. The RMS gain error amounts to 0.4dB at 92GHz and is less than 0.8dB from 77 to 101 GHz. The simulation results of phase shifter for the 64 phase states are shown in Fig. 6. The phase shifter provides a phase turning range of 360° with 6-bit resolution. The RMS phase error is 1.8° at 92 GHz and remain below 2° from 77 to 101 GHz.

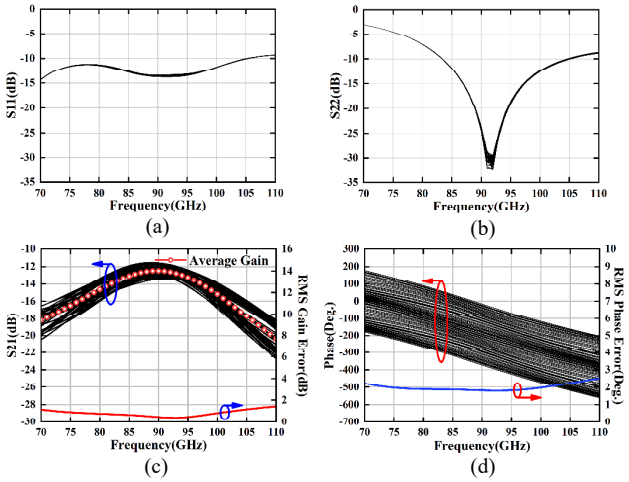


Fig.5. Simulated (a) S11, (b) S22, (c) S21 and RMS gain error, (d) phase shift and RMS phase error

TABLE I. PREFORMANCE COMPARISON

| | [1] | [2] | [4] | This Work |
|---|---|---|---|---|
| **Process** | 0.13um SiGe BiCMOS | 28 nm FDSOI | 40 nm CMOS | **65 nm SOI** |
| **Architecture** | Vector Modulator | Vector Modulator | Vector Modulator | **Vector Modulator** |
| **Resolution (bits)** | 5 | 4 | 6 | **6** |
| **Freq. (GHz)** | 92-100 | 78.8-92.8 | 70-90 | **77-101** |
| **RMS Phase Error (deg)** | <10 | <11.9 | <2.4 | **<2** |
| **RMS Gain Error (deg)** | <1.8 | <2 | -- | **<0.8** |
| **DC Power (mW)** | 37 | 21.6 | 0 | **31** |
| **Core Area ($mm^2$)** | 1.04 | 0.12 | 0.15 | **0.2** |

## IV. Conclusion

This paper presents a 77-101GHz 6-bit vector-modulated phase shifter in 65nm SOI CMOS technology. Based on impedance-invariant VGA technique and wideband quadrature signal generator, the proposed phase shifter achieves 5.6° phase step, a low RMS phase error of < 2.0° and a low RMS gain error of <0.8dB over the bandwidth.

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