A 0.38 THz Fully Integrated Transceiver Utilizing a Quadrature Push-Push Harmonic Circuitry in SiGe BiCMOS

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***Abstract*—A fully integrated transceiver operating at 0.38 terahertz (THz) has been demonstrated in 0.13 μm SiGe BiCMOS with $f_T = 230$ GHz. We present a quadrature push-push harmonic circuitry consisting of the clamping pairs driven by balanced quadrature LO signals coupled through the transformers and the Coplanar Stripline (CPS). Harmonic generation of the clamping circuit is analyzed with a clamped sinusoidal model. Several terahertz circuits such as a quadrupler, a THz subharmonic mixer, and an IQ quadrature generator are implemented with the quadrature push-push circuitry to realize a homodyne FMCW radar. Radar functionality is demonstrated with ranging and detection of a target at 10 cm. The measured Equivalent Isotropically Radiated Power (EIRP) of the transmitter is -11 dBm at 0.38 THz and the receiver noise figure (NF) is between 35–38 dB while dissipating a power of 380 mW.**

***Index Terms*—BiCMOS, BJT, FMCW radar, harmonic generation, terahertz integrated circuits.**

I. Introduction

THE terahertz (THz) frequency, widely conceived as 0.3 THz to 3 THz whose wavelength (λ) is between 1 mm to 0.1 mm, is the transition region between electronics and photonics [1]. There have been several sensing applications reported in THz range. Specifically in nondestructive imaging applications, it has great potential in security imaging for concealed weapon detection [2], or medical diagnostics which can substitute for ionizing X-ray radiation [3]. THz-rays can penetrate dielectric materials, and the wavelength is long enough that it does not cause destructive ionization. In gas remote sensing and molecule spectroscopy [4], a THz-ray is a good candidate as it can produce a unique fingerprint depending on the type of dielectric materials. A short-range ultrafast wireless communication for chip-to-chip interconnection is another promising application [5].

The "terahertz gap" arises due to the lack of compact, reliable, and tunable sources and detectors in THz range [6]. While a long wavelength of THz source limits energy generation ($E = h\nu$) from the photonic approach, the performance of the electronic THz source and detector is severely limited by active device performance using traditional electronic approaches. Moreover, the measurement instrumentation at THz range is scarce and expensive.

In this paper, we explore the feasibility of a fully integrated THz transceiver in silicon technology with f_T and $f_{\max}$ are less than operating THz range. Because of the performance limitations of the silicon based devices, a THz signal beyond $f_{\max}$ is generated from the harmonics of nonlinear (trans)-resistance/conductance or nonlinear reactance. Ideally, lossless nonlinear reactive element can provide a power gain of one, since they can have power dissipation only at desired k^{th} harmonic frequency [7]. However, active devices such as BJT and CMOS transistors are mainly considered as nonlinear conductors or transconductors with several junction diodes. Theoretically, it has been shown that the efficiency of generating a k^{th} harmonic power is limited by $1/k^2$ [8]. Therefore it is essential to find an efficient way to combine harmonics to generate the required output power at THz frequencies. Practically, a strong fundamental signal at the output should be effectively rejected to prevent undesired intermodulation signals. The push-push structure has been widely used since its introduction in [9], especially for high frequency oscillators [10]–[15] and frequency multipliers [16], [17]. Its simplicity in generating high harmonic frequency with fundamental signal rejection at the output is one reason for its popularity.

In Section II, we describe a generalized clamping harmonic generator, followed by the THz homodyne FMCW radar transceiver architecture. The detailed circuit design for the transmitter and the receiver utilizing quadrature push-push pairs driven by the quadrature I/Q balanced signals coupled through transformers are presented, and the effect of phase mismatch in the LO driving signal is discussed. In the next section, on-chip antenna design is discussed in detail and characterization of the CPS is presented. In Section IV, we present the measurement results followed by the conclusion in Section V.

II. Terahertz FMCW Transceiver Architecture

A. Generalized N-Push Harmonic Generator

The generalized N-push harmonic generator utilizes N coupled clamping devices in parallel driven by 0 to $2\pi(N-1)/N$ phase-shifted fundamental input signals as presented in Fig. 1.

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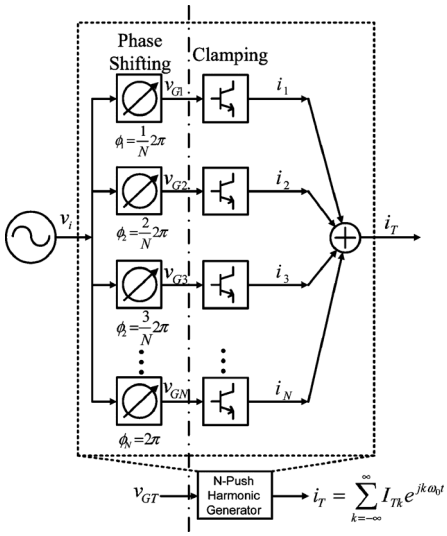

Fig. 1. Schematic diagram of the N-push harmonic generator using clamping circuits having equally spaced phase-shifted inputs.

We can express the phase shifted input voltage signals (V_{GT}) driving the N-clamping circuits given by

$$V_{GT} = \sum_{n=1}^{N} V_{Gn} \cos\left(\omega_0 t - n\frac{2\pi}{N}\right). \tag{1}$$

By using the time shifting property of the Fourier series, the phase-shifted N inputs generate the total output current component ($I_{T(k)}$) at $k\omega_0$ given by

$$\begin{aligned} I_{T(k)} &= \sum_{n=1}^{N} I_{n(k)} e^{-jn(2\pi k/N)} \\ &= \begin{cases} NI_{(k)} & (k = mN, m = 0, 1, 2, \ldots) \\ 0 & (k \neq mN, m = 0, 1, 2, \ldots) \end{cases} \end{aligned} \tag{2}$$

where $I_{1k}, \ldots, I_{nk}$ are the Fourier series coefficients of the output current of the respective clamping devices at $k\omega_0$. The desired $k = N^{th}$ harmonics are constructively added, but undesired harmonic elements lower than N^{th} harmonic are ideally cancelled. The advantage of the N-push harmonic generator is that it does not require a bulky and lossy fundamental rejection filter, and input signals can be selectively frequency multiplied by controlling the phase of the respective input signals. We generate the 2nd harmonic utilizing a push-push pair as the basic building block and the 4th harmonic component is generated with two push-push building blocks driven by the balanced I and Q quadrature signals.

The generated harmonics from the clamping circuit are a function of the conduction angle (θ) for the hard switching device. As presented in Fig. 2, the clamped output current can be modeled with a clamped cosinusoidal waveform given by

$$i_{out}(t) = \begin{cases} I_{\max} - I_p\{1 - \cos(\omega_0 t)\} & (-\theta \leq \omega_0 t \leq +\theta) \\ 0 & (\text{o.w.}) \end{cases}. \tag{3}$$

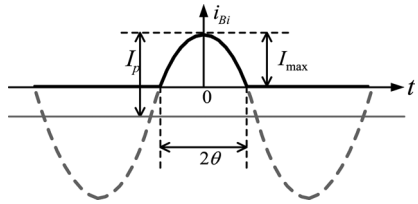

Fig. 2. Clamped output current modeled with a clamped cosinusoidal waveform.

By taking a Fourier series on a generic clamped cosinusoidal current model, the $i_{out}(t)$ is expressed in the cosine series given by

$$i_{out}(t) = \frac{\gamma_0(\theta) I_p}{2} + \sum_{k=1}^{\infty} \gamma_k(\theta) I_p \cos(k\omega_0 t). \tag{4}$$

The coefficients of expansion ($\gamma_k(\theta)$) of the clamped cosinusoidal current is given by [18]

$$\gamma_0(\theta) = \frac{1}{\pi}(\sin\theta - \theta\cos\theta) \tag{5}$$

$$\gamma_1(\theta) = \frac{1}{\pi}\left(\theta - \frac{\sin 2\theta}{2}\right) \tag{6}$$

$$\gamma_k(\theta) = \frac{2}{\pi}\frac{\sin(k\theta)\cos(\theta) - k\sin(\theta)\cos(k\theta)}{k(k^2-1)} \tag{7}$$

Fig. 3 shows the calculated coefficients of expansion ($\gamma_k(\theta)$) as a function of the conduction angle (θ). The k^{th} harmonic component becomes relatively large when the turn-on duration of the clamping device is set to a multiple number of the period of the desired harmonic frequency, given by nT/k. Therefore there exists $(k-1)$ number of harmonic peaks as a function of θ for the k^{th} harmonic component. For example, two optimal biasing points are at $\theta = 120°$ and $\theta = 60°$ when the desired k equals to 3. Practically, the $\theta = 60°$ case requires a relatively low biasing point where a strong input swing can be limited by ground. Hence, the optimal conduction angle (θ_{opt}) for a specific k^{th} harmonic is given by

$$2\theta_{opt} = \begin{cases} \pi & (k = \text{even}) \\ \frac{2\pi}{k}\left(\left[\frac{k}{2}\right] + 1\right) & (k = \text{odd}) \end{cases} \tag{8}$$

where $[\cdot]$ rounds to the nearest integer less than the input number $[\cdot]$. For this clamping circuit, the rectification is performed in the base-emitter junction diode which is not limited by the device f_T. However, the k^{th} harmonic component from the collector current is degraded by $\beta(k\omega_0) \approx \omega_T/k\omega_0$ from the roll-off characteristic of the current gain [19]. Because the device is under the hard switching mode, the device ω_T could be significantly lower than the optimal ω_T that can be achievable in small signal conditions. Therefore it is better approach to use the emitter current composed of the abundant harmonics from base-emitter diode current and the collector current in the BJT. For the N-push circuitry consisting of N clamping devices, the output current is scaled up by N, but Z_{out} of the circuit is scaled down by N which results ideally in N times improvement in the output power. However increasing the number of the clamping devices is limited by the size of the high parasitic capacitance

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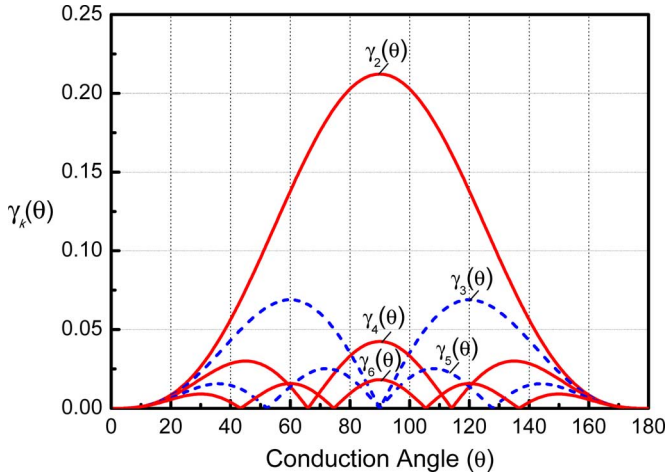

Fig. 3. Coefficient of Expansion ($\gamma_k(\theta)$) of the clamped cosinusoidal output current as a function of the conduction angle(θ).

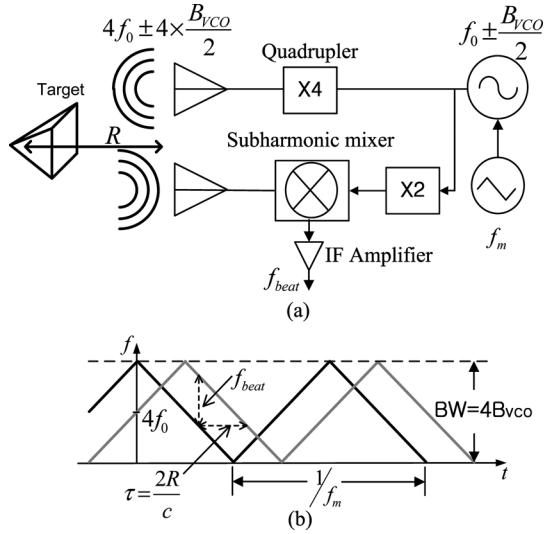

Fig. 4. (a) Block diagram of designed homodyne FMCW transceiver. (b) The concept of ranging with homodyne FMCW radar.

which causes narrow band matching that is sensitive to model inaccuracy and process variation.

B. Terahertz Transceiver Architecture

This section describes the design of a homodyne transceiver of the FMCW radar based on the quadrature push-push architecture [17]. Fig. 4(a) shows a schematic diagram of the FMCW radar transceiver. Fig. 4(b) presents basic concept of the FMCW radar [20]. Briefly, in an FMCW radar, the frequency of the transmitter signal chirps linearly according to the modulation signal. The echo signal has the time delay due to the round-trip propagation of the transmitter signal. By mixing the Tx and Rx signals, the round-trip time delay of the reflected wave is mapped to the frequency difference of two signals as a beat frequency. From the linear relationship between time delay (τ) and the frequency chirp rate (BW/T_m), the beat frequency can be calculated as a function of sweep bandwidth (BW) given by

$$f_{beat} = \frac{2\tau}{T_m} BW = \frac{4 f_m R}{c} \cdot 4B_{\mathrm{VCO}} \tag{9}$$

where f_m is the modulation frequency, $BW = 4 \cdot B_{\mathrm{VCO}}$ is the expanded sweep bandwidth of the transmitting signal due to the Tx quadrupler, and R is the range to the target. Therefore the operation of the transceiver can be verified by measuring the beat signals for a given range. As a homodyne receiver uses the same source to transmit and receive a signal, the down converted IF signal is relatively robust to the frequency shift of the signal generator. This homodyne architecture also reduces the effect of the source's phase noise because the noise of the received signal is correlated to the transmitted signal [21]. The phase noise correlation factor for received target signal is given by

$$K_{rx}^2 = 4\sin^2(\pi f_{beat}\tau) = 4\sin^2\left(\frac{2\pi\tau^2}{T_m} BW\right). \tag{10}$$

As shown in (10) the phase noise effect is a very strong function of detection range. In short ranges less than 1 m, the phase noise effect is negligible. The transmitter consists of on-chip patch antennas and a quadrupler with a quadruple-push clamping circuit. The receiver uses a subharmonic mixer, an IF buffer, and two frequency doublers with $\lambda_l/4$ delay transmission-line (T-line) to generate balanced I and Q LO signals for the subharmonic mixer. Because the strength of the output harmonic signal of the quadrature push-push harmonic generator is proportional to the input power level (hard switching conditions), it is important to provide strong enough power to drive the clamping circuits. As presented in Fig. 5(a), the W-band balanced signal ($\{0°, 180°\}$) is generated with a differential voltage-controlled oscillator (VCO). The branch-line hybrid takes one single VCO output and produces I and Q output signals. The single-to-differential driver amplifies the hybrid outputs to generate the quadrature signal (I:$\{0°, 180°\}$ and Q:$\{90°, 270°\}$). The balanced I and Q quadrature signals drive the quadruple-push clamping circuitry. For the transmitter, a transformer architecture is used to combine the balanced IQ signals to the input of the clamping circuits. An on-chip patch antenna radiates the generated 4th harmonic outputs as shown in Fig. 5(b). A double balanced subharmonic mixer requires a 2nd harmonic quadrature LO signal as presented in Fig. 5(c). The 2nd harmonic quadrature LO generator consists of two differential frequency doublers and a $\lambda_l/4$ CPS delay line. Each frequency doubler is designed with two push-push pairs combined with a 1:1 overlay transformer for the balanced outputs. The down-converted IF signal is amplified by a differential IF buffer to drive external instruments.

C. Fundamental Signal Generator

The Colpitts oscillator architecture is chosen for its wide tuning range and its low phase noise. Furthermore, the cascode topology does not require an additional buffer stage. The branch-line hybrid takes one single VCO output and produces I and Q output signals. The single-to-differential amplifier amplifies the hybrid outputs to generate the quadrature signal (I:$\{0°, 180°\}$ and Q:$\{90°, 270°\}$). Fig. 6 shows the circuit diagrams of the VCO and the driving amplifier. The driving amplifier followed by the hybrid uses the differential cascode topology with an overlay balun at the input-stage of the amplifier to provide the balanced output signal as shown in Fig. 6(b).

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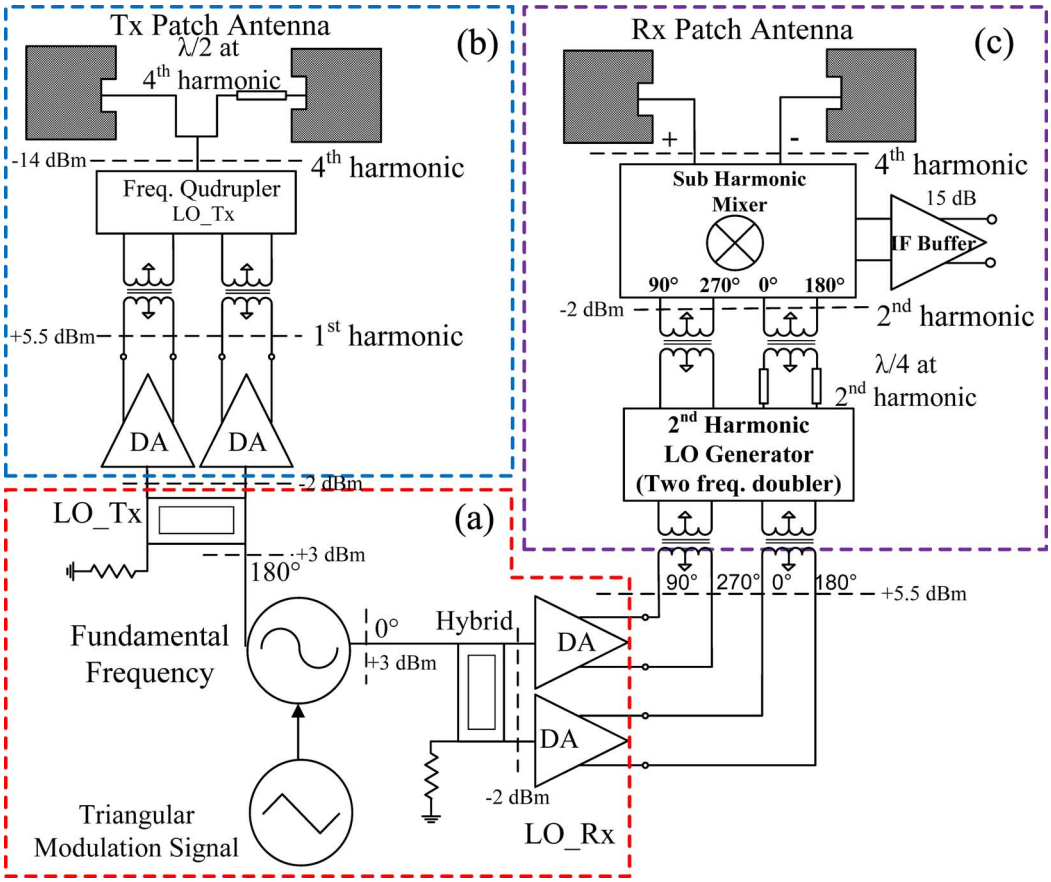

Fig. 5. Schematic diagram of (a) W-band balanced I and Q signal generator. (b) The transmitter with a frequency quadrupler. (c) The homodyne receiver with subharmonic mixer and 2nd harmonic LO generator.

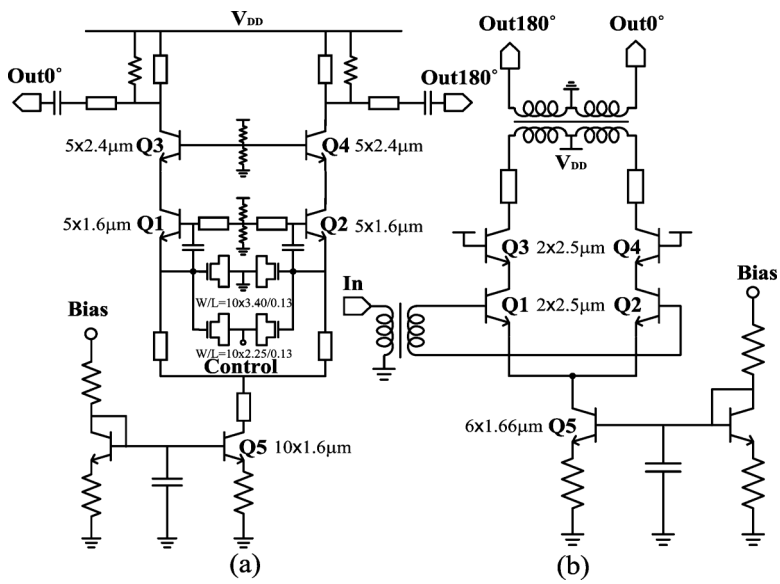

Fig. 6. Circuit diagram of (a) Colpitts VCO with cascade topology, and (b) Single-to-differential driving amplifier.

The balanced gain is 10 dB, and P_{sat} is 6 dBm in simulation. A quadrature hybrid is designed to generate I and Q signals in the transmitter. The hybrid is made of four Micro-Strip Transmission Line (MSTL) segments and four MIM capacitors in order to reduce the length of the MSTL ($W = 3$ μm). The designed hybrid occupies 115 μm$\times$ 210 μm. For the capacitive loading, four 46 fF of MIM capacitors are attached at each edge of the branchlines as shown Fig. 7. The amplitude and phase mismatch for the I and Q signals in the designed hybrid are shown in Fig. 8. The insertion loss is around 1.3 dB with less than 0.3 dB of magnitude mismatch between I and Q, and the phase mismatch is $\pm 0.5^{\circ}$ between 85 GHz and 95 GHz.

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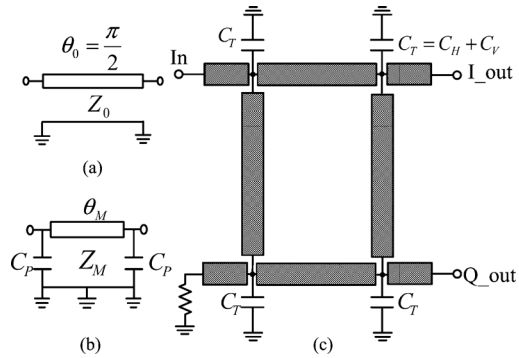

Fig. 7. (a) Desired $\theta_0 = \pi/2$ T-line with Z_0, (b) Equivalent size reduced T-line (θ_M) with Z_M, and (c) Size reduced hybrid with four MIM capacitors.

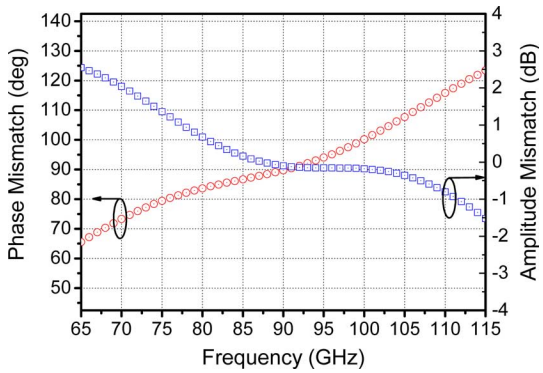

Fig. 8. Simulated phase mismatch and amplitude mismatch of the designed size reduced hybrid.

D. Transmitter Circuit Design

We utilize a push-push pair ($L_E = 2 \times 1.6\ \mu$m for Q1 = Q2) driven by a 1:1 transformer and the CPS as the basic building block for the quadrature push-push circuitry. Fig. 9 presents the circuit diagram of the quadrupler. The transmitter quadrupler is designed using two push-push building blocks driven by the balanced I and Q quadrature input signals employing a 1:1 stacked transformer and the CPS. We choose an emitter coupled pair to utilize base-emitter currents to maximize the harmonic currents considering the low current gain where the desired harmonic frequency is much higher than the operating f_T of the device. The fundamental balanced I and Q driving signals are coupled through the compact transformer coupled architecture for the dc biasing and the matching network [22], [23] with 21 dB of return loss with $Z_0 = 100\ \Omega$. The CPS ($W = 4\ \mu$m, $G = 7\ \mu$m) with $Z_0 = 100\ \Omega$ between the transformer and the push-push pair provides a resonant inductance (L_g) combined with the transformer for the matching network. In simulation, the HiCUM2 model [24] from the foundry is used with the Harmonic-Balance (HB) simulation. The designed push-push pair driven by the transformer coupled architecture achieves relatively wide bandwidth. The ideal load of a frequency multiplier or frequency conversion circuit should provide full rejection of unwanted harmonics and provide optimal impedance (conjugated matching) at the desired harmonic. As shown in Fig. 10(a), the on-chip patch antenna with ground center tap dramatically reduces the antenna resistance at the fundamental

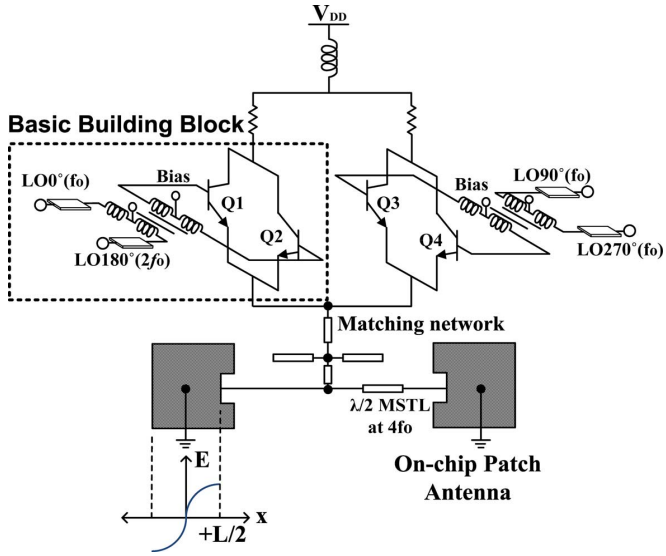

Fig. 9. Circuit diagram of the Tx quadrupler with two push-push building blocks driven by the balanced quadrature LO signals.

frequency without affecting the antenna input impedance at resonant frequency ($4f_0$). Fig. 10(b) compares two output voltage waveforms of the transmitter with Tx antenna and the ideal load which produces a short circuit load for the undesired harmonics and optimal impedance at the desired 4th harmonic. In the HB simulation, -14 dBm of output power is generated from the two differential I and Q inputs, each of which is driven by 5.5 dBm of differential input power, which shows 22.5 dB of conversion loss.

Let us consider the effects of phase mismatch on the fundamental rejection performance of the quadrature push-push circuitry. Because the quadruple-push clamping circuit used in the transmitter consists of two push-push building blocks, all the odd harmonics are essentially eliminated. Hence the strongest fundamental signals can be easily eliminated if we drive the push-push circuits with differential signals. The transformer coupled architecture with the CPS has very high common-mode to differential-mode rejection. Therefore the phase characteristic in the balanced signal ($\{0°, 180°\}$) is well preserved in our proposed circuit. Fig. 11 shows the simulated 4th, 3rd, 2nd harmonics and the fundamental component as a function of the I and Q imbalance. Within $\pm 10°$ of phase error, the quadrupled output signal degrades only by 0.8 dB.

E. Receiver Circuit Design

In order to drive the double balanced harmonic mixer, balanced I and Q quadrature LO driving signals are needed at $2f_0$. This is realized with two frequency doublers consisting of the four push-push building blocks driven by the fundamental balanced IQ signal from the LO generator as shown in Fig. 12. Because the 2nd harmonic frequency is reasonably low, we choose the common-emitter structure. Each frequency doubler consists of two push-push pairs driven by I:$\{0°, 180°\}$ and Q:$\{90°, 270°\}$ that generates differential 2nd harmonic output through the output transformer. The quadrature signal is created using a $\lambda_l/4$ delay line implemented with a CPS line (loss of 0.3 dB). The transformer coupled architecture is used for the

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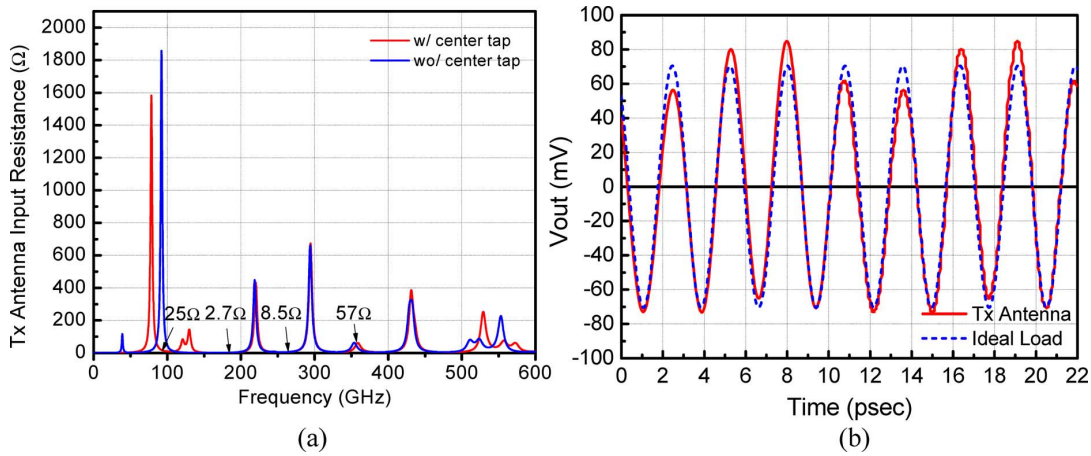

Fig. 10. (a) Comparison of the transmitter antenna input impedance with and without the ground center tap. (b) Output waveforms of the quadrupler with the Tx antenna versus an ideal load (short at undesired harmonics and a matched load at the desired harmonic).

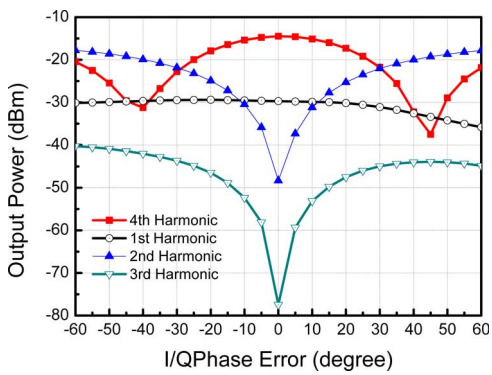

Fig. 11. Output harmonics of the transmitter as a function of I/Q phase mismatch.

dc biasing and the matching network between the LO input of the subharmonic mixer and differential output of the frequency doubler with 28 fF of MIM capacitor in parallel for matching. With 5.5 dBm of balanced I and Q LO driving signals (total $+8.5$ dBm) driving doublers, the conversion loss of the 2nd harmonic quadrature LO generator is 7.5 dB including loss of the $\lambda_l/4$ delay T-line, the input and output transformers, and it provides about -2 dBm of balanced 2nd harmonic I and Q signals to the mixer LO ports. Fig. 13 shows the simulated 4th, 3rd, 2nd harmonics and the fundamental component as a function of the I and Q imbalance. Only 0.3 dB of the 2nd harmonic LO generator power is lost when the phase error is below $\pm 10^\circ$.

As a homodyne down-converter, we designed a double balanced subharmonic mixer as shown in Fig. 14. From the system perspective, LO to RF isolation is one of the critical issues in a homodyne transceiver, which desensitize the receiver. The subharmonic mixer naturally achieves better LO to RF isolation. Throughout the common base devices, both RF+ and RF− input signals from the on-chip patch antenna are fed into four push-push building blocks. For RF+, the quadrature push-push structures are driven by the 2nd harmonic quadrature LO signals from the quadrature frequency generator. The emitter coupled pairs are driven by the balanced I($\{0^\circ, 180^\circ\}$), which generates frequency doubled components with positive polarity which generate IF+. Likewise, the IF- is generated by

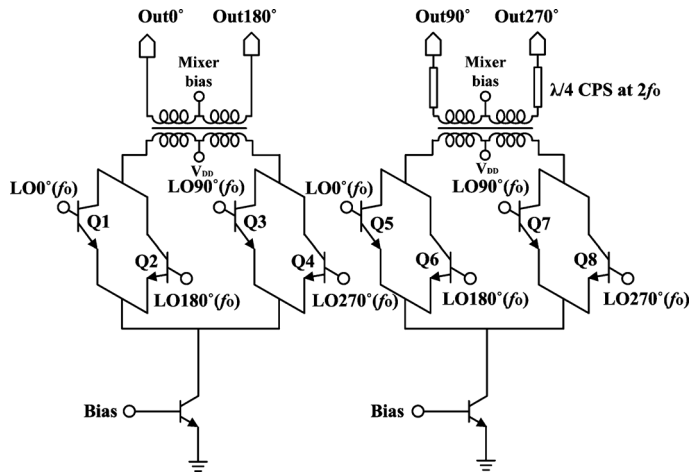

Fig. 12. Circuit diagram of the 2nd harmonic quadrature LO generator.

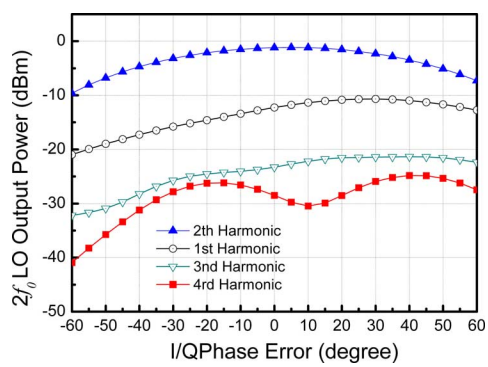

Fig. 13. Output harmonics of the 2nd harmonic LO generator as a function of I/Q phase mismatch.

the pair driven by the Q($\{90^\circ, 270^\circ\}$). RF- is mixed with the quadrature LO signals in the same way. Q1 and Q2 are biased using a $\lambda/4$ line at the base, which is open at 4th harmonic RF frequency. As such, Q1 and Q2 provide coupling capacitance for the input RF signal while providing high output impedance at the lower frequencies. Since Q3-Q6 and Q7-Q10 are pumped in push-push mode at a sub-harmonic, the high tail impedance helps to improve the NF of the mixer. The differential IF signals are fed into the cascode IF buffer having 15 dB of power

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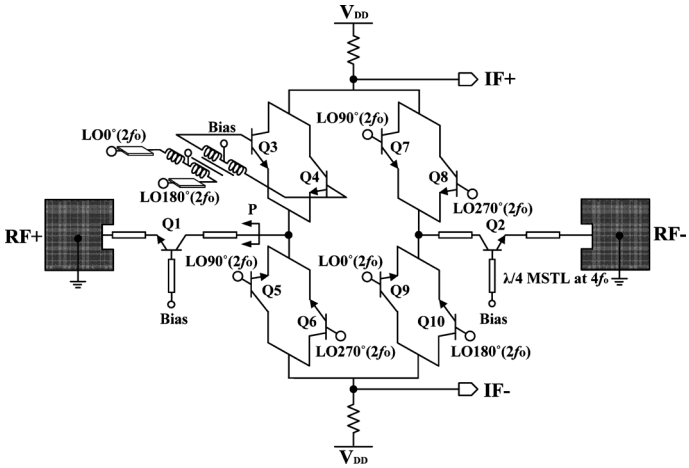

Fig. 14. Circuit diagram of the Rx subharmonic double balanced mixer with the quadrature push-push harmonic structure.

gain and NF = 4.8 dB to drive external instruments for the measurement purpose. In simulation, the receiver has −7.2 dB of conversion power gain for a differential 100 Ω load, and a noise figure of 27.4 dB. The differential RF input impedance is 83.5 + j3.94 Ω when the subharmonic mixer is driven by −2 dBm of LO power. Fig. 15 shows the conversion power gain and noise figure of the receiver as a function of the LO driving power level.

III. Passive Elements

A. Coplanar Stripline Characterization

In this THz integrated transceiver design, the coplanar stripline (CPS) [25] is widely used to route balanced signals to the quadrature push-push circuits, providing better signal integrity and higher common mode rejection with a comparable propagation loss compared to CPW and MSTL counterparts [26]. To implement the CPS, the top metal (M7) with 3 μm of thickness is used. Considering non-negligible effects of the thick signal trace and the complex dielectric layers on the electric field distribution, the CPS structure was analyzed with 3D EM simulator HFSS. The complex dielectric stacks from the BEOL process were simplified into five equivalent dielectric layers, each of which is calculated based on series capacitance approximation. From extracted four port S-parameters, we analyzed the CPS using mixed-mode scattering parameters. Then we approximate it as T-line parameters. It should be noted that the ideal CPS hardly propagates common mode (CM) to its balanced structure. However the ground plane around the CPS decreases the CM impedance. Therefore the ground plane should be well controlled in design. We placed the ground plane 30 μm apart from the signal trace lines. For 4 μm < G < 14 μm, and 4 μm < W < 12 μm, Z_0 ranges from 75 Ω to 145 Ω with attenuation less than 1 dB/mm at 180 GHz. When G is less than 2 μm, the attenuation starts to drop drastically.

B. On-Chip Patch Antenna Design

For a given antenna gain, the propagation loss is inversely proportional to the wavelength (λ) squared due to aperture loss.

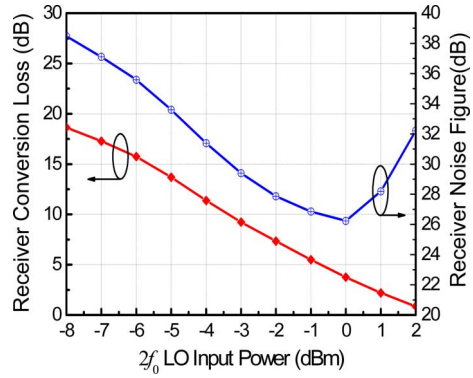

Fig. 15. Power conversion loss and noise figure of the down conversion receiver as a function of $2f_0$ LO input power.

However when the received signal power from the radar equation [20] in terms of the physical antenna aperture size, the signal to noise ratio (S/N) is given by

$$\left(\frac{S}{N}\right)_{Rx} = \frac{P_{Tx}\sigma}{k_B T_S B_n}\frac{\lambda_0^2 G_{Tx} G_{Rx}}{(4\pi)^3 R^4} = \frac{P_{Tx}\sigma}{k_B T_S B_n}\frac{e_{Tx} A_{pTx} e_{Tx} A_{pRx}}{4\pi R^4 \lambda_0^2} \quad (11)$$

where P_{Tx} is the transmitter output power, σ is the radar cross-section, R is the detection range, λ_0 is the wave-length of the radiating wave, $k_B T_S B_n$ is the system noise power, G_{Tx} and G_{Rx} are the antenna gains, e_{Tx} and e_{Rx} are the antenna radiation efficiencies, A_{pTx} and A_{pRx} are the physical aperture areas for Tx and Rx respectively. As shown in (11), the SNR at the receiver exhibits quadratic increase with frequency when we fix the size of the antenna aperture.

To realize reasonable radar or communication range at high frequencies, it is critical to realize a large antenna aperture (relative to λ_0) with high radiation efficiency to achieve a desired signal to noise ratio (SNR) for a THz transceiver which has low output power and receiver sensitivity. However, a conventional on-chip dipole antenna in a lossy silicon substrate has been reported very poor radiation efficiency, around 10–15% [27], [28]. There are two main loss mechanisms in the on-chip antenna element on the lossy silicon substrate. One is caused by the resistive loss in the silicon substrate [28], [29], and another is the surface-wave mode excitation caused by the multimode excitation from relatively thick substrate with high dielectric constant ($\varepsilon_r = 11.8$) [30]. On-chip patch antennas are used to achieve high radiation efficiency (e_{rad}). The ground plane implemented with Metal-1 (M1) and M2 isolates the signals from the lossy silicon substrate. It also minimizes surface-wave excitation caused by the high permittivity of the silicon substrate. The on-chip antenna utilizes the top-most aluminum layer and its height is about 12 μm from M2. The aluminum layer has relaxed metal density rules in layout and also provides better quality factor in performance. The on-chip patch antenna design was performed with a 3D EM simulation (HFSS). Each patch is placed in opposite excitation direction for the balanced RF input. The Rx antenna has 6.6 dBi of antenna gain with e_{rad} of 44% at 0.36 THz in HFSS simulation. The Tx antenna has two patches placed in opposite directions. The signals are combined in phase with

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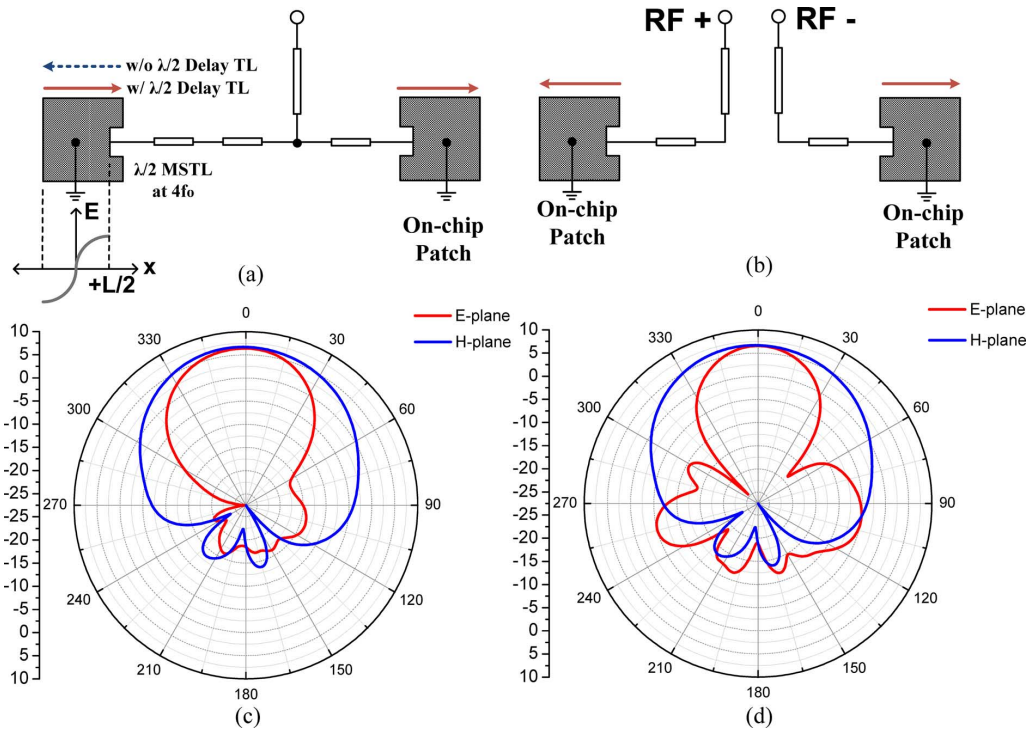

Fig. 16. The structure of the on-chip patch antennas for (a) Tx, (b) Rx and the respective radiation pattern for (c) Tx antenna, and (d) Rx antenna.

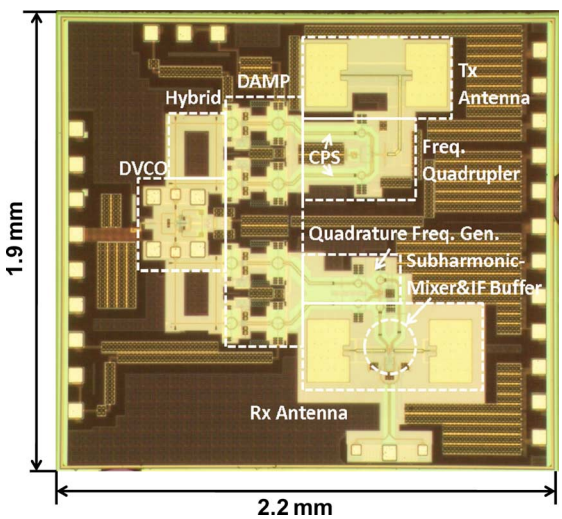

Fig. 17. Microphotograph of the fabricated fully integrated 0.38 THz FMCW transceiver (Dimension: 2.2×1.9 mm^2).

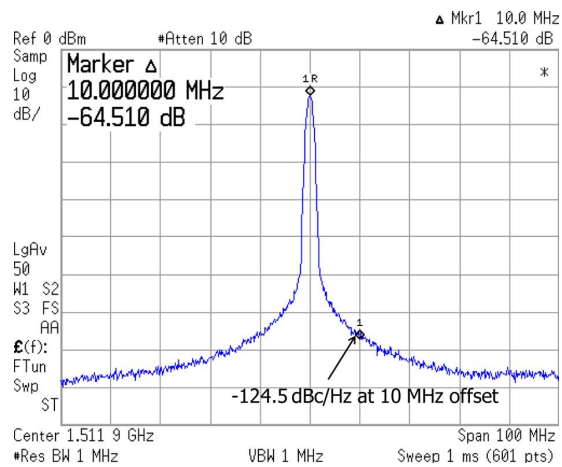

Fig. 18. Measured phase noise of the stand-alone VCO with the spectrum analyzer.

a $\lambda_l/2$ delay line at 4th harmonic frequency, which aligns to the same antenna direction as the Rx antenna. The $\lambda_l/2$ delay line rejects power combining of the residual 1st and 2nd harmonics. The implemented on-chip patch antenna uses thin dielectric layers between M2 and aluminum layer which results in a narrow bandwidth. The input bandwidth is 7.2 GHz with VSWR = 2:1. The Tx antenna has 6.3 dBi of antenna gain with e_{rad} of 46% at 0.36 THz in HFSS simulation. The structure and radiation pattern of the Tx and Rx on-chip antennas are presented in Fig. 16.

IV. Measurement

The designed THz homodyne FMCW transceiver was implemented with STMicroelectronics 0.13 μm SiGe B9MW process with an optimal $f_T = 230$ GHz. The fabricated chip measures 2.2×1.9 mm^2 as shown in Fig. 17. From the on-chip probe measurement of a stand-alone structure, the VCO has the phase noise of -124.5 dBc/Hz at 10 MHz offset, 8.3% of available tuning range, and 3 dBm (single-ended) output power with $f_0 = 92.7$ GHz. Fig. 18 presents the measured phase noise of the stand-alone VCO.

We measure the weakly radiating W-band fundamental signal while the transceiver is operating as presented in Fig. 19(a). The *in-situ* VCO in the transceiver was characterized using a W-band horn antenna, an external down-converter, and a spectrum analyzer. For the down converter, a W-band LO signal was generated from an external frequency multiplier with an external microwave signal generator. A WR-10 standard horn antenna is used to gather the radiated W-band fundamental

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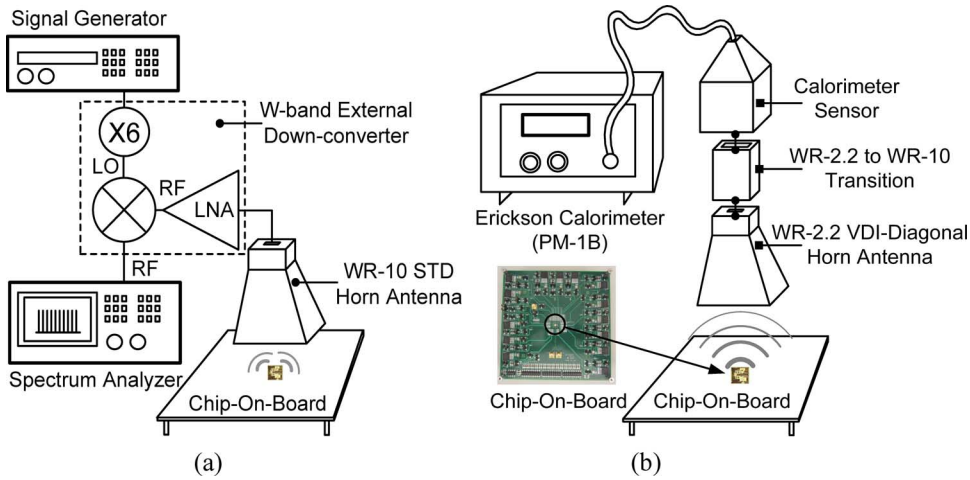

Fig. 19. (a) Measurement setup for (a) VCO characterization of the in-situ VCO. (b) Equivalent Isotropically Radiated Power (EIRP) of the transmitter.

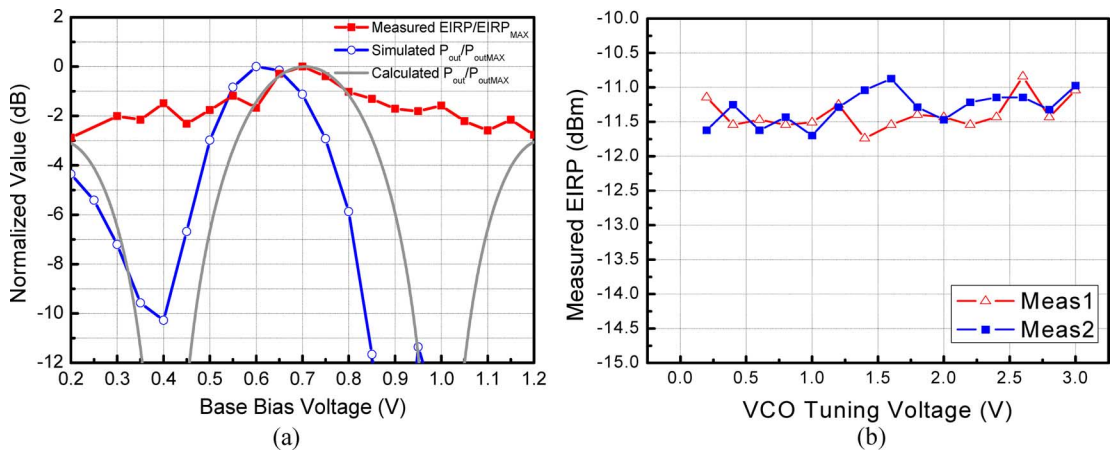

Fig. 20. (a) Comparison between the measured normalized EIRP and simulated output power as a function of the base bias voltage. (b) Measured EIRP as a function of VCO tuning voltage (frequency).

signal from the chip on board. The VCO sweep bandwidth ($B_{\rm VCO}$) used in the transceiver is about 3.65 GHz considering the VCO sweep linearity [30]. The transmitting frequency ranges from 0.367 THz to 0.382 THz. Using the Erickson calorimeter (PM-1B), WR-2.2 horn antenna, and WR-2.2 to WR-10 transition (Fig. 19(b)), the Equivalent Isotropically Radiated Power (EIRP) is measured as a function of base bias voltage and compared with simulation results after normalizing both with the maximum values (Fig. 20(a)), and the VCO tuning voltage (Fig. 20(b)). The measured EIRP ranges about -14 dBm to -11 dBm depending on the base bias voltage which is maximized around 0.65 V $\sim$ 0.75 V with about 0.5 dB of measurement deviation from the calorimeter. The disagreement in $V_{bias(opt)}$ between the simulation and the measurement is likely due to the discrepancy in the simulated saturation current (I_{sat}) of the base-emitter junction diode. Our theoretically calculated values using (4) correspond quite well with the measured results around $V_{bias(opt)}$ when an estimated I_{sat} was applied from the measurement as shown in Fig. 20(a).

The noise figure of the receiver was estimated from the output noise floor. As the antenna is covered with an absorber, the antenna temperature is equal to the ambient temperature. Therefore the noise figure of the lossy receiver is approximated by

$$F = \frac{G_{Rx}\cdot k_B TB + N_{Rx}}{G_{Rx}\cdot k_B TB} \approx \frac{N_{Rx}}{G_{Rx}\cdot k_B TB} \approx \frac{N_{floot}}{G_{Rx}\cdot k_B TB_{res}} \tag{12}$$

where G_{Rx} is the total gain of the receiver, k_B is the Boltzmann's constant, T is the ambient temperature, B is noise bandwidth, B_{res} is the resolution bandwidth of the spectrum analyzer, N_{Rx} is output noise only from the receiver, N_{floor} is the measured output noise floor in the spectrum analyzer. Considering the dominant noise contribution from the receiver itself and $+15$ dB of power gain of the IF buffer, the noise from spectrum analyzer is neglected. From the measured noise floor, simulated G_{Rx}, and the mismatch from the frequency shift, the estimated receiver noise figure is about 35 dB to 38 dB.

We verify the functionality of the entire system from the IF beat signals for a given target. To reduce the effect of incident angle between target and sensor, we used WR-2.2 and WR-10 horn antennas with shorted load as corner reflectors as shown in Fig. 4(b). Fig. 21 presents the target at 5 cm distance from the FMCW radar transceiver when the modulation frequency f_m

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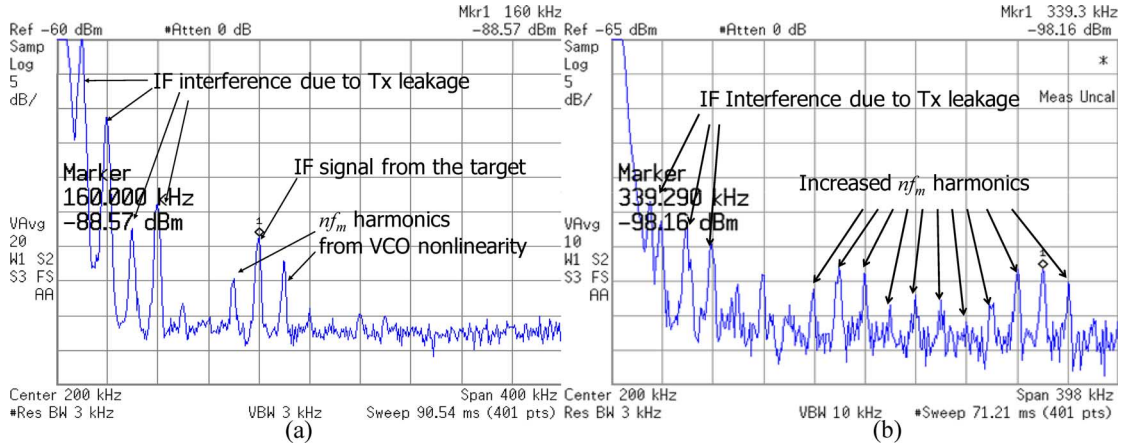

Fig. 21. (a) Measured IF output spectrum with a target positioned at normal direction at 5 cm distance from the FMCW transceiver with $f_m = 20$ kHz. (b) The IF output spectrum with with maximized frequency chirp in VCO which exhibits a highly nonlinear sweep characteristic.

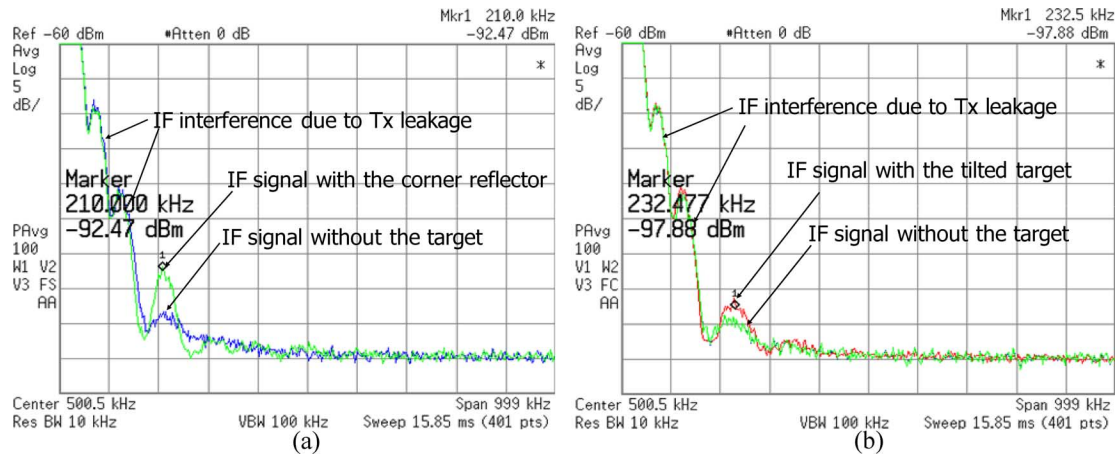

Fig. 22. (a) Measured IF output spectrum with and without the corner reflector positioned at normal direction at 10 cm distance from the THz FMCW transceiver. (b) The IF output spectrum for the target with misaligned case.

is 20 kHz. The estimated beat frequency is 195 kHz with BW ($= 4 \times B_{\mathrm{VCO}}$) equal to 14.6 GHz in the transmitting THz signal. The measured IF spectrum shows that there exist three peaks caused by the VCO control voltage nonlinearity, since the control voltage time domain waveform is periodic with the modulation period $T_m = 1/f_m$ (Fig. 21(a)). The largest peak exists at 160 kHz with -88.5 dBm, and the beat frequency and received signal strength varies depending on the target alignment. The effect of the VCO's sweep nonlinearity becomes even more evident when we maximize the chirp range of the control voltage as shown in Fig. 21(b) [31]. The measurements are also performed for a target at 10 cm distance from the FMCW radar transceiver. To exclude the effects of frequency dependency in the measurement setup, we set the modulation frequency f_m equal to 10 kHz which keeps the same beat frequency (195 kHz) in the ideal case. The measured beat frequency of the peak is 210 kHz with -92.47 dBm as shown Fig. 22(a). The discrepancy is mainly due to the alignment errors in the target and the nonlinear VCO sweep which smears the beat spectrum as before. All the measured IF beat signals show strong interferences around dc due to the Tx leakage which has relatively short propagation delay [32]. In the radar test setup we aligned the target until it produces maximum received power. Fig. 22(b) shows the measured IF output when the target is slightly misaligned. The IF beat spectrum shows that the beat signal is changed by 22 kHz while the received signal power is reduced by more than 5 dB.

V. Conclusion

We have presented an emitter combined quadrature push-push harmonic generator with push-push pairs, transformer-coupled stages and CPS transmission-lines. By utilizing the quadrature push-push harmonic generator, we demonstrated several high frequency core building blocks, such as the balanced IQ quadrature LO generator operating at 0.19 THz, a 0.38 THz quadrupler, and a 0.38 THz subharmonic mixer driven by the 0.19 THz LO generator. The CPS on silicon substrate has proven to be useful in routing balanced signals in this frequency range. These blocks are integrated to realize a 0.38 THz fully integrated homodyne FMCW radar. Measurements confirm target ranging and detection.

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