6-bit CMOS Digital Attenuators With Low Phase Variations for X-Band Phased-Array Systems

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***Abstract*—This paper presents 6-bit CMOS digital step attenuators with low phase variations. To mitigate the insertion phase variation of conventional switched Pi/T attenuators, the proposed attenuators employ a compensation circuit. This includes a low-pass filter for phase/amplitude correction. Analysis and comparison of two types of Pi-attenuators with the inductive and capacitive correction circuits are described. The two types of attenuators are fabricated using a 0.18-μm CMOS process. The attenuators have a maximum attenuation range of 31.5 dB with 0.5-dB steps (64 states). The attenuators with the inductive and capacitive correction structures, respectively, exhibit root mean square (rms) amplitude errors of less than 0.3 and 0.4 dB, and rms phase errors of less than 3.5° and 2° at 8–12 GHz. The insertion losses are 8.7 and 10.5 dB at 10 GHz, respectively. The input 1-dB compression points are 15 and 13 dBm at 10 GHz, and the total chip sizes, excluding pads, are 1.25 $\times$ 0.4 mm^2 and 0.67 $\times$ 0.5 mm^2.**

***Index Terms*—Attenuator, CMOS switch, digital step attenuator, phase correction, phased-array phase variation, root mean square (rms) phase error.**

I. Introduction

AMPLITUDE control circuits such as variable attenuators and variable gain amplifiers are required in a variety of applications, including the automatic gain control of transmitter/receiver systems, amplitude weighting in phased-array radars, and temperature compensation of power amplifiers [1]–[3].

In phased-array antennas and beam-forming systems, accurate and wide amplitude control is required to adjust the sidelobe levels and null points precisely, and constant transmission phase during amplitude control is required to avoid tracking errors and complex phase/amplitude calibrations [4], [5]. Low device power consumption is an important requirement since the phased-array systems consist of a large number of individual transmit/receive modules integrated with respective antenna elements so that many power amplifiers and phase/amplitude control circuits are utilized. Power-handling capability and performance insensitivity over temperature variations are also required.[1,2] Given the listed requirements, a digitally controlled step attenuator is preferable to a variable gain amplifier or an analog attenuator in terms of control complexity, power consumption, phase variation, and linearity [6], [7].

Several designs of digital step attenuators, shown in Fig. 1, have been demonstrated in the literature: switched path attenuators [8],[3] distributed attenuators using p-i-n diodes and CMOS switches as a varistor [9], [10], and switched Pi/T attenuators [11]–[18]. These attenuators mainly achieve relative attenuations from insertion loss differences by on/off control of RF switches. Switched path attenuators use single-pole-double-throw (SPDT) switches to steer the signal path between a thru line and a resistive network, as shown in Fig. 1(a). This topology provides low phase variation over attenuation states, but it exhibits high insertion losses at reference states due to the cumulative losses of all SPDT switches for a multibit design, and it occupies a large chip area. Accordingly, it is not suitable for the design of CMOS digital step attenuators. Distributed step attenuators have the advantage of low insertion loss by virtue of having no series switches in the signal path, as shown in Fig. 1(b). The number of varistors and quarter-wavelength transmission lines, however, increases linearly with the number of attenuation states. Therefore, this topology occupies a large chip area to have high-resolution/ high-attenuation range. The switched Pi/T attenuators in Fig. 1(c) have series and shunt single-pole-single-throw (SPST) switches merged with a resistive network for attenuation. These topologies have a single series switch in a signal path. The parasitic difference of the switch on/ off state, however, causes the transmission phase change.

In this paper, 6-bit CMOS digital step attenuators with two types of phase/amplitude correction networks are demonstrated. Analysis of the proposed 6-bit attenuator and the bit ordering of the attenuators are also studied. In Section II, we discuss the limitations of conventional switched Pi/T structure. In Section III, the design concept of the proposed topology to alleviate the limitations is explained. In Section IV, we describe the analysis and design of two types of the proposed topologies and compare these two structures. In Sections V and VI, the circuit implementation and measured results are presented.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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[1]Attenuator, digital, 5-bit 0.1–20.0 GHz, part MAATGM0004-DIE, M/A-Com Inc., Lowell, MA, 2007.

[2]DC–18.0-GHz GaAs MMIC 5-bit digital attenuator, part A1000-BD, Mimix Broadband Inc., Hsinchu, Taiwan, 2007.

[3]0.5-dB LSB GaAs monolithic microwve integrated circuit (MMIC) 6-bit digital attenuator, dc–13 GHz, part HMC424, Hittite, Chelmsford, MA 2007.

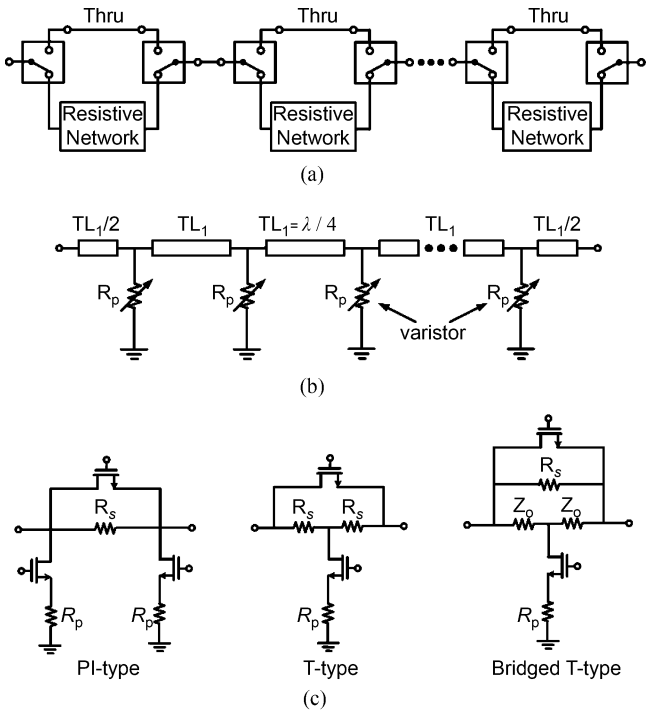

Fig. 1. Topologies of digital step attenuators. (a) Switched path attenuator. (b) Distributed step attenuator. (c) Switched Pi/T and bridged-T attenuators.

II. Design Limitations of Conventional Structures

A. Conventional Switched Pi/T Attenuators

The conventional switched Pi/T attenuators are composed of series/shunt switches and resistors. The nMOS transistor as the series/shunt switches is a key component of the digital step attenuators. In this work, the nMOS switch with a source-body tied in Fig. 2(a) that was modeled by using the equivalent-circuit model, as shown in Fig. 2(b), has been used [19]. For simple analysis, the switch model in Fig. 2(b) can be approximated by ignoring the body parasitics and series parasitic inductance. The on-state resistance $R_{\rm on}$ and off-state capacitance $C_{\rm off}$ in Fig. 2(b) remain as the dominant elements. Fig. 3(a) shows a circuit schematic of the conventional switched Pi attenuator and Fig. 3(b) and (c) shows equivalent circuits of reference and attenuation states.

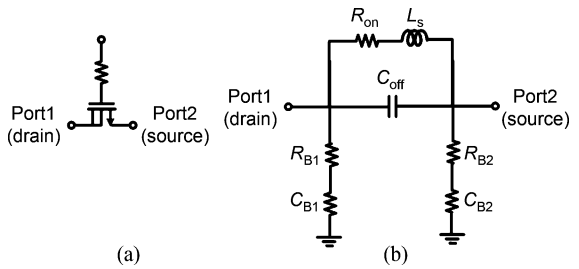

Fig. 2. (a) nMOS switch with a source-body tied. (b) Equivalent-circuit model of the nMOS switch.

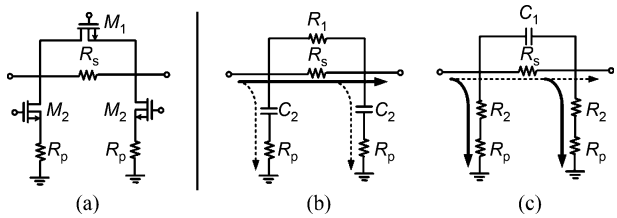

Fig. 3. (a) Conventional switched Pi attenuator using nMOS switches, and its equivalent circuits at: (b) reference and (c) attenuation state.

B. Limitations of Conventional Design

To explore the condition of having no transmission phase difference, which is the condition of the conventional switched Pi attenuator, the transmission phases are derived from the transmission matrices at the reference and attenuation states. The transmission ($ABCD$) matrix for the reference state, as shown in Fig. 3(b), is given by (1), shown at the bottom of this page. The transmission coefficient S_{21} from the transmission matrix is given by (2), shown at the bottom of this page. Here, R_1 is the on-resistance of the series transistor M_1, C_2 is the off-capacitance of the shunt transistor M_2, and Z_o is the characteristic impedance. Using (2), the transmission phase at reference state ϕ_R can be written as

$$\phi_R = \tan^{-1}\left(\frac{2(R_1R_s + Z_oR_s + Z_oR_1)C_2\omega Z_o}{2Z_oR_s + 2Z_oR_1 + 2R_1R_s}\right) \tag{3}$$

where $\omega^2C_2^2R_p^2 \ll 1$

The transmission matrix for the attenuation state, as shown in Fig. 3(c), and the transmission coefficient S_{21} from the matrix can also be derived as for the reference state. Using these

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1+\frac{\omega^2C_2^2R_pR_1R_s}{R_s+R_1}+\frac{j\omega C_2R_1R_s}{R_s+R_1} & \frac{R_sR_1}{R_s+R_1} \\ 2\omega^2C_2^2\left(R_p-\frac{R_sR_1}{R_s+R_1}\right)+j2\omega C_2 & 1+\frac{\omega^2C_2^2R_pR_1R_s}{R_s+R_1}+\frac{j\omega C_2R_1R_s}{R_s+R_1} \end{vmatrix} \tag{1}$$

$$S_{21} = \left(\frac{2}{A+\frac{B}{Z_o}+Z_oC+d}\right) = \frac{2}{1+\frac{R_1R_s}{R_s+R_1}\left(\frac{\omega^2C_2^2R_p}{2}+jC_2+\frac{1}{2Z_o}\right)+\omega Z_oC_2\left(\omega C_2R_p-\frac{\omega C_2R_pR_1R_s}{2(R_s+R_1)}+j\right)} \tag{2}$$

equations, the transmission phase at attenuation state ϕ_A can be written as

$$\phi_A = \tan^{-1}\left(\frac{\omega C_1 R_s^2(R_p + Z_o)}{R_s R_p + Z_o R_s + 2Z_o R_p}\right) \tag{4}$$

where $\omega^2 C_1^2 R_s^2 \ll 1$, R_2 is the on-resistance of the shunt transistor M_2, and C_1 is the off-capacitance of the series transistor M_1.

To yield no transmission phase difference, it is necessary to satisfy the following equation:

$$\Delta\phi = \phi_A - \phi_R = 0. \tag{5}$$

One can find the series and shunt switch off-capacitances C_1 and C_2 to realize zero transmission phase difference $\Delta\phi$. It can be derived as (6) and (7), shown at the bottom of this page. These capacitances C_1 and C_2 are negative because no other variables can be negative values; therefore, they must ideally be zero so as to have no transmission phase difference.

For example, to have 16-dB attenuation of the conventional Pi attenuator, the gatewidths of the series/shunt transistors and resistor values are determined by considering the insertion loss, return loss, attenuation level, insertion phase difference, bandwidth, etc. The resistor values of each series and shunt path R_s and R_p are chosen as 154 and 29 Ω, respectively. The gatewidths of the series and shunt switch M_1 and M_2 are determined as 30 and 20 μm. The series switch has the on-resistance R_1 of 18 Ω and the off-capacitance of 21 fF, and the shunt switch has the on-resistance R_2 of 29 Ω and the off-capacitance of 15 fF. Fig. 4 shows the simulation results of the conventional Pi attenuator for 16-dB attenuation. The insertion loss is 1.3 dB at 10 GHz with 0.1-dB loss variation at 0–20 GHz. Having 16-dB attenuation, as shown in Fig. 4(a), the transmission phase difference increases quite a bit with respect to frequency, as shown in Fig. 4(b). The insertion phase of the attenuation state is relatively lead phase in comparison with that of the reference state. This is because of the existence of the switch off-capacitance. As shown in Fig. 5(a), the transmission phase difference increases as the series switch off-capacitance C_1 is swept from 0 to 45 fF when C_2 is 15 fF for 16-dB attenuation. The phase difference can be zero only when C_1 and C_2 are negligible simultaneously; however, this is not possible in real MOSFET switches. Fig. 5(b) shows the insertion loss variation with the gatewidth of the series transistor M_1 swept from 10 to 70 μm. If one reduces the size of the transistor to have small C_1 and C_2, the insertion loss is increased. It is, therefore, concluded that this conventional topology cannot have both low insertion loss and a small phase difference.

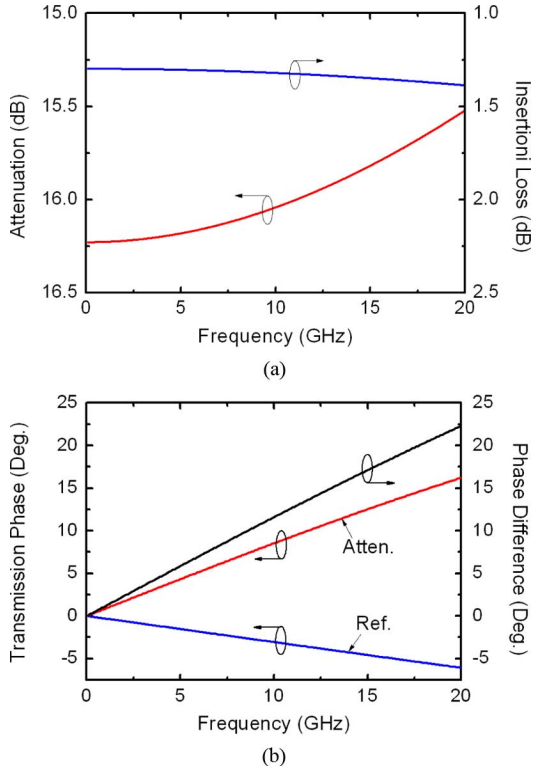

Fig. 4. Simulation results of conventional switched Pi attenuator for 16-dB attenuation. (a) Attenuation level and insertion loss. (b) Transmission phases of reference and attenuation states and phase difference.

III. Proposed Structure

A. Phase Characteristics of High-Pass/Low-Pass Filter

The proposed structure is introduced to reduce the transmission phase difference of the switched Pi/T attenuator induced by switching. As shown in Fig. 4(b), the attenuation state has a phase-lead comparing with the reference phase. This is due to the phase-shift characteristics of a high-pass filter. In contrast, a low-pass filter has a phase lag to the reference phase. Generally, these specific phase characteristics are widely used in high-pass/low-pass filter-type phase shifters [19], [20]. Fig. 6 shows the Pi-type high-pass/low-pass filter network.

From the transmission coefficient S_{21} of the low-pass filter in Fig. 6(b), the transmission phase ϕ_{LPF} is given by

$$\phi_{\mathrm{LPF}} = \tan^{-1}\left[-\frac{\omega Z_o\left(\frac{L_s}{Z_o}^2 + 2C_p - \omega^2 L_s C_p\right)}{(1-\omega^2 L_s C_p)}\right] \tag{8}$$

$$C_1 = -\frac{2C_2 Z_o(R_1R_s + Z_oR_s + Z_oR_1)(R_2R_s + R_sR_p + 2Z_oR_2 + Z_oR_s + 2Z_oR_p)}{R_s^2(2Z_oR_s + 2Z_oR_1 + R_1R_s)(R_2 + R_p + Z_o)} \tag{6}$$

$$C_2 = -\frac{C_1 R_s^2(2Z_oR_s + 2Z_oR_1 + R_1R_s)(R_2 + R_p + Z_o)}{2Z_o(R_1R_s + Z_oR_s + Z_oR_1)(R_2R_s + R_sR_p + 2Z_oR_2 + Z_oR_s + 2Z_oR_p)} \tag{7}$$

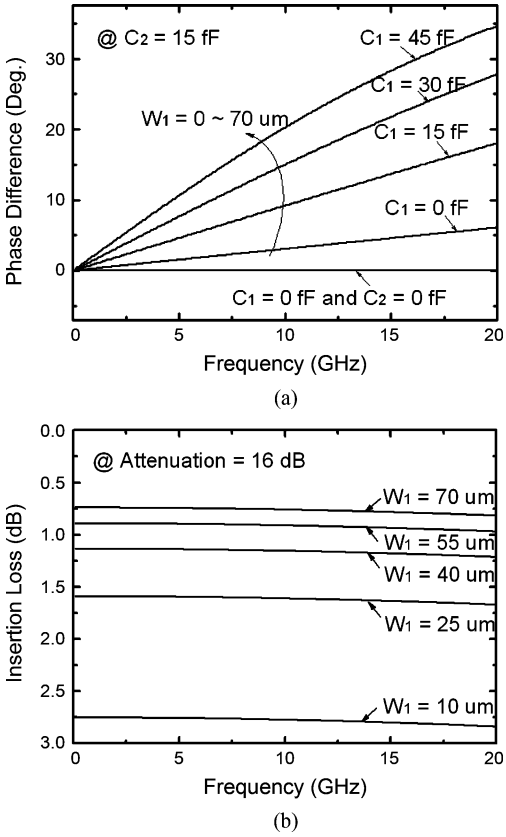

Fig. 5. Simulation results of conventional switched Pi attenuator for 16-dB attenuation. (a) Transmission phases difference. (b) Insertion loss.

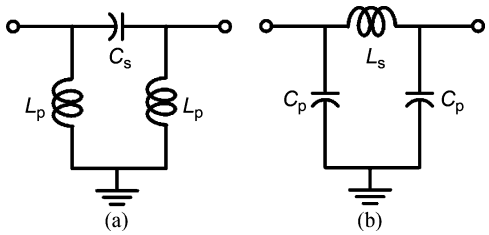

Fig. 6. Pi-type: (a) high-pass filter network and (b) low-pass filter network.

$$\omega_{\mathrm{LPF}} = \sqrt{\frac{2+\left(\frac{L_s}{C_p Z_o^2}\right)}{L_s C_p}}. \tag{9}$$

For a specified frequency lower than ω_{LPF}, the transmission phase ω_{LPF} is always negative; i.e., the low-pass filter has a phase-lag characteristic.

B. Phase/Amplitude Correction Network

Using the phase-lag characteristic of a low-pass filter, we can effectively reduce the transmission phase difference of a conventional switched Pi attenuator. Fig. 7(a) shows the structure of a switched Pi attenuator with a low-pass filter network. By optimizing the low-pass filter elements L_s and C_p in Fig. 6(b), the transmission phase of the attenuation state can be similar to the reference phase at the desired frequency, as shown in Fig. 7(b).

The low-pass network also reduces the attenuation level. As shown in Fig. 8(a), the low-pass filter is connected in parallel with the resistive network so that the attenuation level becomes much lower. To avoid this, the series resistor R_c is inserted in series with the low-pass filter network, as shown in Fig. 8(b). These correction resistors can be implemented with the series resistor R_s of the resistive network in Fig. 8(a). Each correction resistor value of R_c is set to $R_s/2$. As shown in Fig. 9(a) and (b), one can make the three-element low-pass filter function as a series inductor L_c or as a shunt capacitor C_c. This operates as a phase corrector, although the slope of the transmission phase over frequency becomes smaller due to the decrease of the number of poles. There are two noteworthy cases: in case 1,

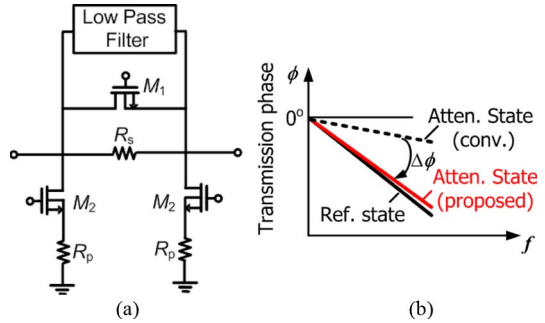

Fig. 7. (a) Switched Pi attenuator with low-pass filter network. (b) Transmission phase characteristics of conventional and proposed structures.

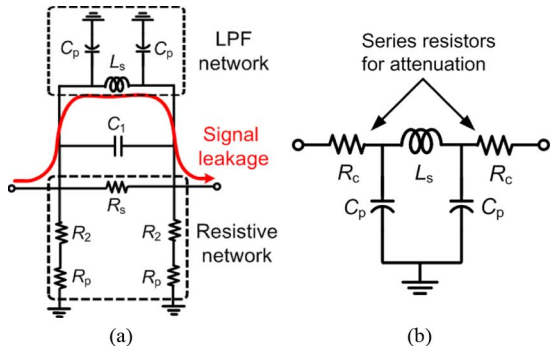

Fig. 8. (a) Equivalent circuit of switched Pi attenuator with low-pass filter at attenuation state. (b) Phase/amplitude correction network in which a Pi-type low-pass filter network merged with series resistors R_c.

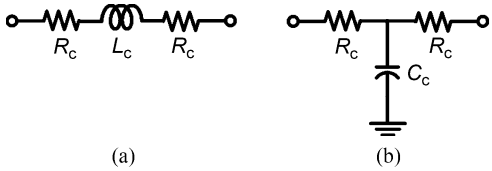

Fig. 9. (a) Inductive and (b) capacitive phase/amplitude correction networks.

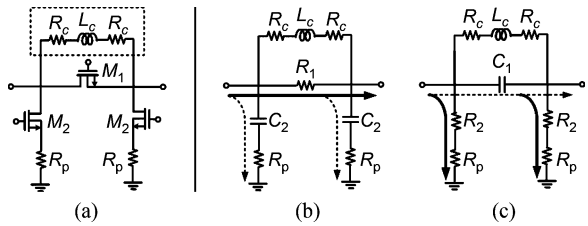

Fig. 10. (a) Pi attenuator with inductive correction network, and its equivalent circuits at: (b) reference state and (c) attenuation state.

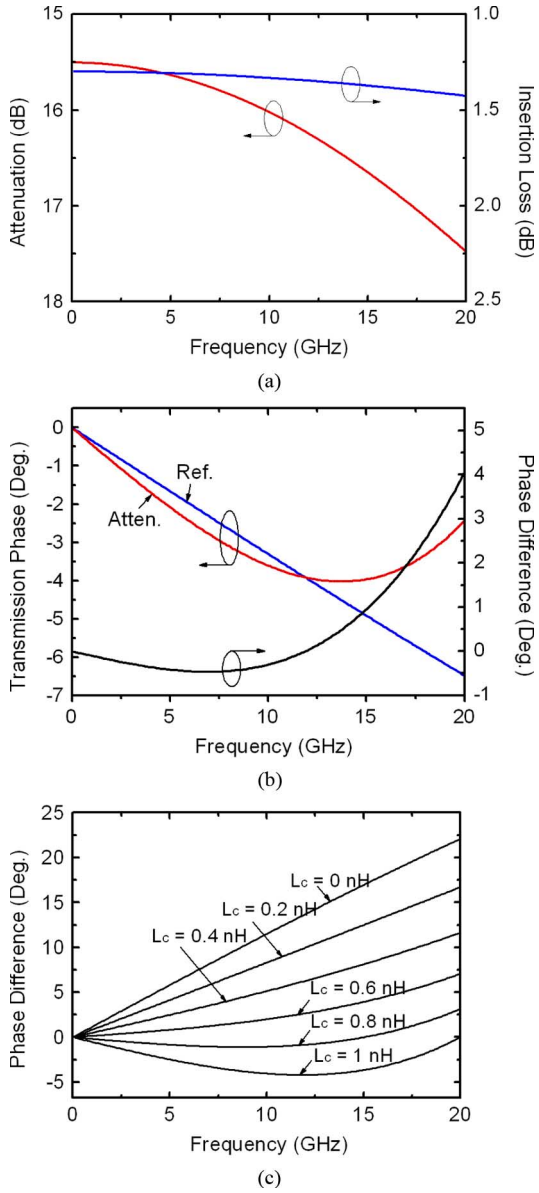

Fig. 11. Simulation results of proposed switched Pi attenuator for 16-dB attenuation with inductive correction network. (a) Attenuation level and insertion loss. (b) Transmission phases of reference and attenuation states and phase difference. (c) Phase differences with various L_c.

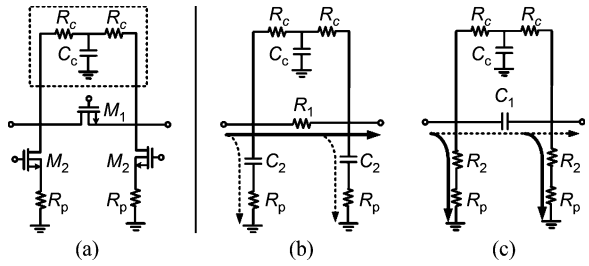

Fig. 12. (a) Proposed switched Pi attenuator with capacitive correction network and its equivalent circuits at: (b) reference state and (c) attenuation state.

the inductive phase/amplitude correction network has lower insertion loss than the capacitive network, and in case 2, the capacitive phase/amplitude correction network has no inductor. In Section IV, a comparison between these two structures will be briefly outlined.

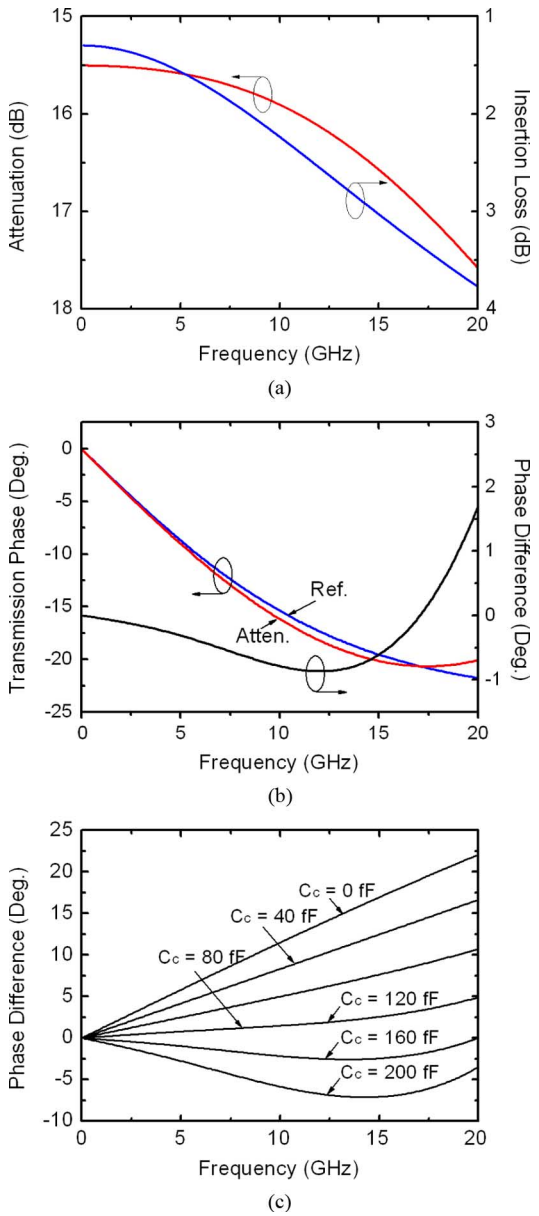

Fig. 13. Simulation results of proposed switched Pi attenuator for 16-dB attenuation with capacitive correction network. (a) Attenuation level and insertion loss. (b) Transmission phases of reference and attenuation states and phase difference. (c) Phase differences with various C_c.

IV. Design of the Proposed Structures

In this section, two types of switched Pi attenuators with inductive and capacitive correction networks are analyzed. The proposed scheme is also applicable to the switched T or bridged-T attenuators.

A. Inductive Correction Structure

Fig. 10 shows the switched Pi attenuator with inductive correction network and its equivalent circuits at reference and attenuation states. For simple analysis, the body parasitics and series parasitic inductance are neglected.

The transmission phases at reference and attenuation states ϕ_R and ϕ_A can be written as (10) and (11), shown at the bottom

of this page, where $\omega^2 C_2^2 R_p^2 \ll 1$ and $\omega^2 C_1^2 R_c^2 \ll 1$, respectively. To achieve no transmission phase difference, it is necessary to satisfy (5). The inductance L_c required to realize the transmission phase difference $\Delta\phi$ as zero is derived as follows:

$$L_c = \frac{1 - \sqrt{1 - 16\omega R_c^2 C_1^2}}{2\omega^2 C_1}. \tag{12}$$

With this L_c, the gatewidths of the series and shunt transistors, resistances, and series inductance are optimized considering insertion loss, return loss, attenuation level, insertion phase difference, bandwidth, etc. When R_c and C_1 have large values simultaneously, which means a high attenuation level (large R_c) with a large gatewidth for the series transistor (large C_1), there may be no solution for L_c. For 16-dB attenuation, the gatewidths of W_s and W_p are 30 and 20 μm. Also R_p is 35 Ω, R_c is 77 Ω, and L_c is 0.75 nH, respectively. Fig. 11(a)–(c) shows the simulation results. As shown in Fig. 11(a), insertion loss is 1.3 dB at 10 GHz with 0.1-dB loss variation at 0–20 GHz, which is almost the same as the insertion loss for the conventional switched Pi attenuator in Fig. 4(a). In Fig. 11(b), the transmission phase difference becomes very small at the broadband frequencies. This shows a big improvement in comparison with the graph for the conventional switched Pi attenuator shown in Fig. 4(b). Fig. 11(c) shows the phase difference between the reference and attenuation states of the switched Pi attenuator with an inductive correction network where L_c is swept from 0 to 1 nH (0.2-nH step).

B. Capacitive Correction Structure

Fig. 12 shows the switched Pi attenuator with a capacitive correction network and its equivalent circuits at reference and attenuation states.

The transmission phase at the reference and attenuation states ϕ_R and ϕ_A can be written as (13) and (14), shown at the bottom of this page, where $\omega^2 C_2^2 R_p^2 \ll 1$ and $\omega^2 C_1^2 R_c^2 \ll 1$, respectively. To achieve no transmission phase difference, it is necessary to satisfy (5). The capacitance required to realize the transmission phase difference $\Delta\phi$ as zero can be derived as (15), shown at the bottom of this page. With this equation of C_c, the gatewidths of the series and the shunt transistors, resistances, and shunt capacitance are optimized considering insertion loss, return loss, attenuation level, insertion phase difference, bandwidth, etc. When R_c and C_1 have large values simultaneously, there may be no solution for C_c. For 16-dB attenuation, the gatewidths of W_s and W_p are 30 and 20 μm. Also R_p is 35 Ω, R_c is 77 Ω, and C_c is 145 fF, respectively. Fig. 13(a)–(c) shows the simulation results. The insertion loss is 2.3 dB at 10 GHz with a 2.5-dB loss variation at 0–20 GHz, as shown in Fig. 13(a). In Fig. 13(b), the transmission phase difference becomes very small with broadband frequency in comparison with that of the conventional switched Pi attenuator in Fig. 4(b). Fig. 13(c) shows the phase difference between the reference and attenuation states of the switched Pi attenuator with a capacitive correction network where C_c is swept from 0 to 200 fF (40-fF step).

$$\phi_R = -\tan^{-1}\left(\frac{\omega(2Z_oC_2(4R_c^2(Z_o+R_1)+2R_cR_1(R_1+4Z_o)+Z_oR_1^2)+L_c(R_1^2+2\omega^2L_cC_2Z_o(Z_o+R_1)))}{4R_c^2(R_1+2Z_o)+2R_cR_1(R_1+4Z_o)+2Z_oR_1^2-\omega^2L_c(2C_2R_1^2Z_o-L_cR_1-2L_cZ_o)}\right) \tag{10}$$

$$\phi_A = \tan^{-1}\left(\frac{\omega(4C_1R_c^2+3\omega^2L_c^2C_1-L_c)(R_p+Z_o)}{2(R_cR_p+Z_oR_c+2Z_oR_p)(1-2\omega^2L_cC_1)}\right) \tag{11}$$

$$\phi_R = -\tan^{-1}\left(\frac{\omega(2Z_oC_2(R_1+2R_c)(2R_1R_c+2Z_oR_c+Z_oR_1)+C_c(R_1R_c+2Z_oR_c+Z_oR_1)^2)}{2(R_1+2R_c)(R_1R_c+2Z_oR_c+Z_oR_1)}\right) \tag{13}$$

$$\phi_A = \tan^{-1}\left(\frac{\omega\,(4C_1R_c^2(R_p+Z_o)^2-C_c((R_cR_p+Z_oR_c+Z_oR_p)^2-\omega\,C_1R_c^2M))}{(R_p+Z_o)(R_cR_p+Z_oR_c+Z_oR_p)+\omega\,R_c^2C_cC_1(3Z_oR_p^2+6Z_oR_cR_p+4R_cR_p^2+4Z_o^2R_c+4Z_o^2R_p)}\right) \tag{14}$$

$$\begin{aligned} M &= 2C_1R_c(4R_c(R_p+Z_o)^2-Z_oR_p(4R_c-R_p))-C_c(2(R_c^2R_p^2+Z_o^2R_c^2+Z_o^2R_p^2)+Z_oR_cR_p(3R_c+3R_p+4Z_o)) \\ C_c &= R_c+Z_o-2\omega^2C_1^2Z_oR_cR_1 \\ &\quad \frac{-\sqrt{(R_c+Z_o)^2-4\omega^2C_1^2R_c4R_c^3+2R_c^2(R_1+2Z_o)-3Z_oR_1R_c+Z_o^2R_1-\omega^2C_1^2Z_o^2R_1^2R_c}}{2\omega^2C_1R_c(R_c+Z_o)} \end{aligned} \tag{15}$$

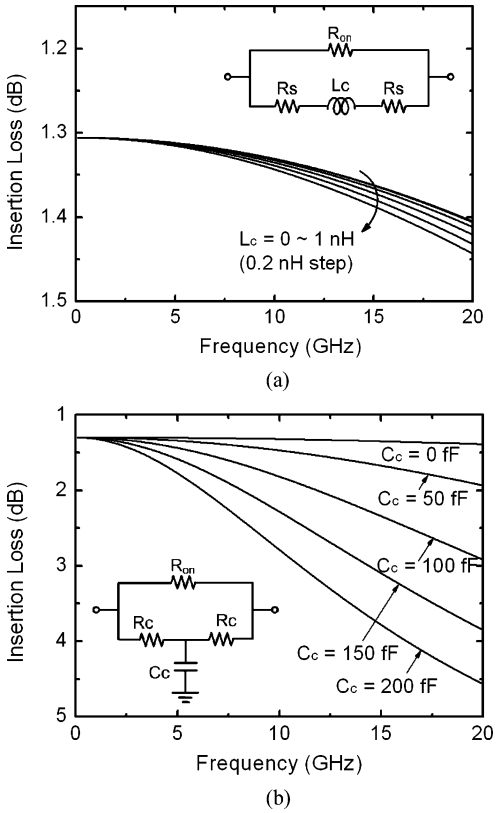

Fig. 14. Simulated insertion loss variation of: (a) inductive and (b) capacitive correction structures as varying L_c and C_c, respectively.

C. Comparison of Inductive and Capacitive Correction Structures

To compare the insertion losses of two structures, the magnitude of transmission coefficient S_{21} from the transmission matrix at the reference state is given by (16) and (17), shown at the bottom of this page. The off-capacitances of the shunt path switch are neglected for the convenience of analysis. When L_c and C_c are set to be zero, (16) and (17) become as follows:

$$|S_{21}|_{\text{Ind.}} = |S_{21}|_{\text{Cap.}} = \frac{Z_o(R_{\text{on}} + 2R_c)}{(R_{\text{on}}R_c + Z_oR_{\text{on}} + 2Z_oR_c)}. \quad (18)$$

Fig. 14(a) and (b) shows the insertion loss with L_c swept from 0 to 1 nH, and C_c swept from 0 to 200 fF. The insertion loss and loss variation of the inductive correction network are much lower than those of the capacitive correction network. From (16), the term of ω^2 is much smaller than the other square terms in the denominator of (16), and thereby the degradation of the insertion loss with frequency is not critical. From (17), we can see that the term of ω^2 is dominant in the denominator of (17) so that the insertion-loss degradation with frequency is greater.

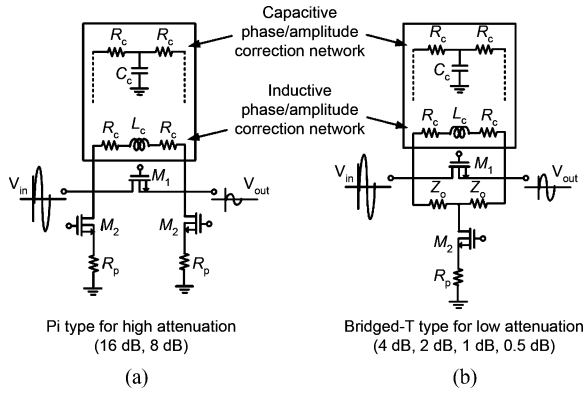

Fig. 15. Proposed switched: (a) Pi attenuator (for high attenuation) and (b) bridged-T attenuator (for low attenuation).

TABLE I
COMPONENT VALUES FOR DESIGNED 6 bits OF INDUCTIVE CORRECTION STRUCTURE

Atten.	Type	*R_s /R_p (Ω)	W_1 (μm)	W_2 (μm)	L_c (nH)
0.5 dB	Bridged-T	7/1245	80	40	0.12
1 dB	Bridged-T	9.2/313	90	40	0.15
2 dB	Bridgd-T	15/108	90	40	0.15
4 dB	Bridged-T	29/32.4	70	35	0.17
8 dB	Pi	54/95	50	45	0.42
16 dB	Pi	200/40	30	20	0.75

*$R_s = 2R_c$

TABLE II
COMPONENT VALUES FOR DESIGNED 6 bits OF CAPACITIVE CORRECTION STRUCTURE

Atten.	Type	*R_s /R_p (Ω)	W_1 (μm)	W_2 (μm)	C_c (fF)
0.5 dB	Bridged-T	12/1245	20	20	0
1 dB	Bridged-T	10/1245	90	20	0
2 dB	Bridged-T	20/877	75	20	67
4 dB	Bridged-T	46/95	70	15	123
8 dB	Pi	62/95	60	15	110
16 dB	Pi	180/35	30	20	135

*$R_s = 2R_c$

V. IMPLEMENTATION OF THE 6-bit DIGITAL STEP ATTENUATORS

Fully integrated X-band 6-bit digital step attenuators have been fabricated using commercially available 1P6M 0.18-μm CMOS technology. The digital step attenuator circuit consists of six digital bits corresponding to binary-weighted attenuations of 16, 8, 4, 2, 1, and 0.5 dB. As shown in Fig. 15, bridged-T configurations for 4 dB or less and Pi configurations for large

$$|S_{21}|_{\text{Ind.}} = 2Z_o\sqrt{\frac{(R_{\text{on}} + 2R_c)^2 + \omega^2L_c^2}{\omega^2L_c^2(R_{\text{on}} + 2Z_o)^2 + 4(R_{\text{on}}R_c + Z_oR_{\text{on}} + 2Z_oR_c)^2}} \quad (16)$$

$$|S_{21}|_{\text{Cap.}} = \frac{2Z_o\sqrt{(R_{\text{on}} + 2R_c)^2 + \omega^2C_c^2R_c^4}}{(R_{\text{on}}R_c + Z_oR_{\text{on}} + 2Z_oR_c)\sqrt{4 + \omega^2C_c^2(R_c + Z_o)^2}} \quad (17)$$

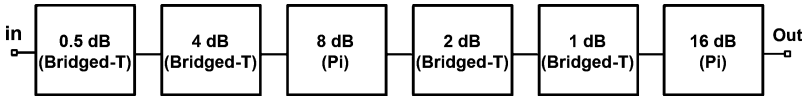

Fig. 16. Bit ordering of the designed 6-bit digital step attenuators.

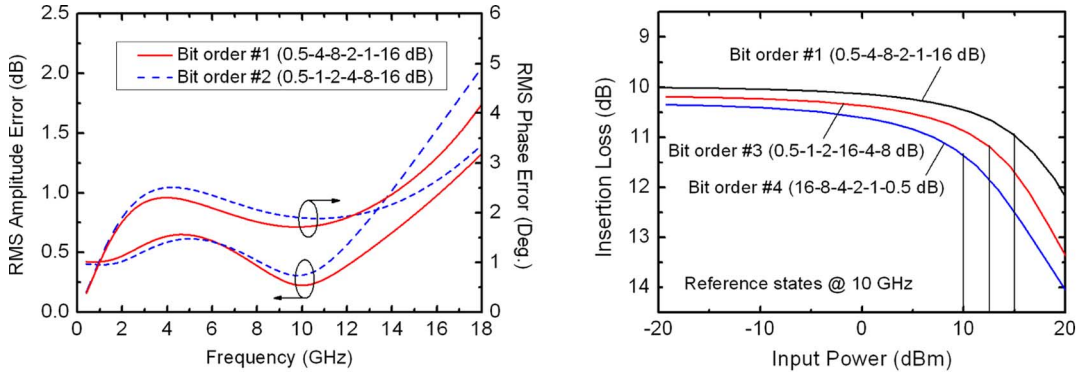

Fig. 17. Simulated: (a) rms amplitude and phase errors and (b) power-handling capabilities of the reference states at 10 GHz according to the different bit orderings (capacitive correction structure).

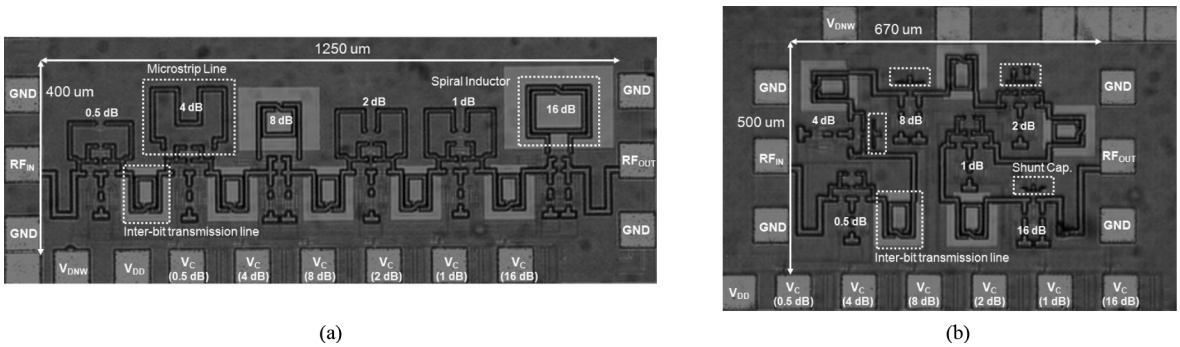

Fig. 18. Chip photograph of 6-bit digital step attenuators. (a) Inductive and (b) capacitive correction structure.

attenuations, such as 8 and 16 dB, are adopted. The component values of each bit attenuator using the proposed structure are shown in Tables I and II. For a higher attenuation bit, the smaller gatewidth W_1 of the series switch is chosen for the large isolation of a series switch. As mentioned in Section IV, the large attenuation bits (8 and 16 dB) also have larger R_c so that the smaller W_1 and the larger L_c or C_c are required to effectively alleviate the transmission phase difference. In the 16- and 8-dB attenuation bits, spiral inductors are used to achieve the desired inductance L_c, as shown in Table I, and microstrip lines with the bottom-layer metal M1 as a ground plane are employed in other attenuation bits.

After bit designs are finished, they have to be ordered appropriately to achieve the optimal performance. The bit ordering should be considered in terms of: 1) loading effects and 2) power-handling capability. When the attenuation is changed from the reference state to the 64th state (maximum attenuation), each attenuation bit has to preserve its accurate attenuation independent of the state that may cause the different loading effect. Power-handling capabilities are strongly dependent on the maximum voltage swing, which can be applied to drain/source node of the nMOS switch. The higher attenuation bits have the lower power-handing capabilities since they have the larger voltage difference between the drain and source of the series switch M_s. Also, the higher attenuation bits in each Pi or bridge-T configurations have the lower shunt resistor R_p so that the even larger voltage swing is applied between the drain and source of the shunt switch M_p. When the signal voltage amplitude is high in a negative swing, it can push the drain junction diode of the nMOS switch into a forward biased region so that the output signal is distorted.

Considering these loading effects and the power-handling capability, appropriate bit ordering has been determined as shown in Fig. 16. The 16-dB attenuation bit has the lowest power-handling capability so that it is located at the end of the attenuator. Although there is a little degradation of linearity, the 8- and 4-dB attenuation bits are separated from the 16-dB attenuation bit because a relatively large variation in attenuation by loading effects is experienced. Fig. 17(a) shows rms amplitude and phase errors according to the different bit orderings for the capacitive correction structure. The bit ordering #1 (0.5-4-8-2-1-16 dB) has better accuracy than the bit ordering #2 (0.5-1-2-4-8-16 dB)—ascending bit ordering—in the desired frequencies because of the different loading effect. Also, the degradation of power-handling capability according to the different bit orderings, particularly the location of the most high attenuation bit (16 dB) is shown in Fig. 17(b). As the 16-dB attenuation bit is placed near the input stage, the input 1-dB compressed power $(P_{1\,\mathrm{dB}})$ becomes lower. Comparing with the bit ordering #1 (0.5-4-8-2-1-16 dB) with the input $P_{1\,\mathrm{dB}}$

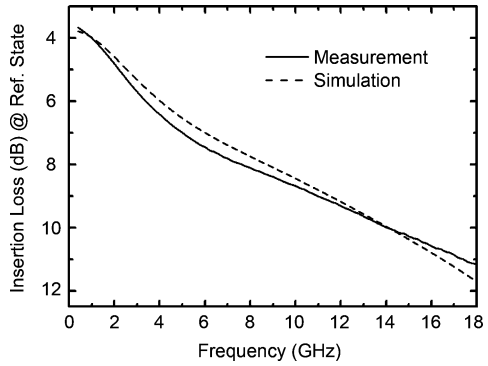

Fig. 19. Measured and simulated insertion loss at reference state (inductive correction structure).

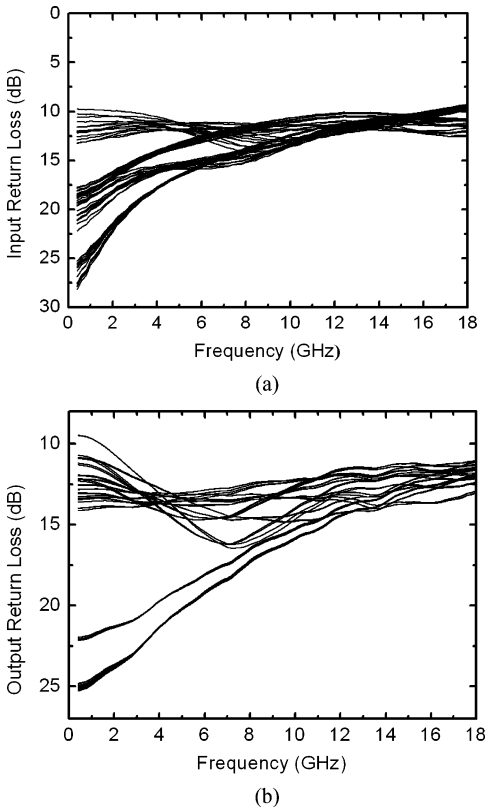

Fig. 20. Measured: (a) input and (b) output return loss (inductive correction structure).

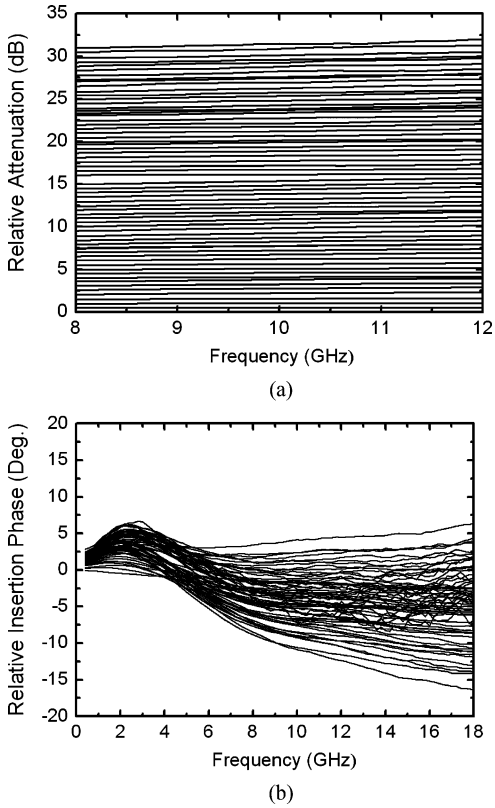

Fig. 21. Measured: (a) relative attenuation, and (b) relative insertion phase of 64 different states of the digital step attenuator (inductive correction structure).

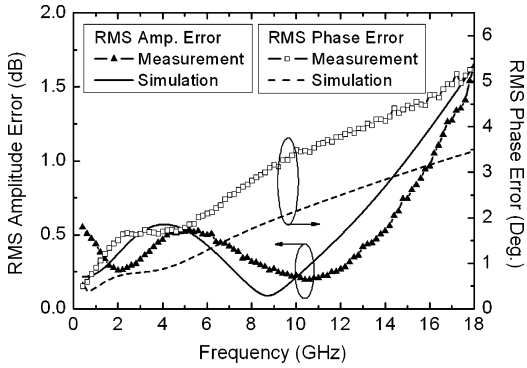

Fig. 22. Measured and simulated rms amplitude error and rms phase error (inductive correction structure).

of 15 dBm, the bit ordering #3 (0.5-1-2-16-4-8 dB) and #4 (16-8-4-2-1-0.5 dB) have the input $P_{1\ \mathrm{dB}}$ of 12.5 and 10 dBm, respectively, in simulation. In the case of applying the digital attenuators to bidirectional transmit/receive systems, the most high attenuation (16 dB) bit should be put in the middle of the attenuation bits such as the bit order #3 (0.5-1-2-16-4-8 dB). Power-handling capabilities can be improved by using the stacked series/shunt nMOS transistors in which the signal voltage is equally divided into each stacked transistor.

The transmission line is used to interconnect attenuation bits. It improves the matching performance and also can adjust the transmission phase characteristics. A two-and-one-half dimensional (2.5-D) electromagnetic (EM) simulation was performed to accurately predict the characteristics of the inductors, transmission lines, interconnects, and pads. The layout of the series/shunt resistors, which are the crucial components in the attenuator design, was carefully chosen. To reduce the process variation effects of the very small resistors, the resistors connected in parallel with several larger resistors were used.

VI. Measured Results

Fig. 18 shows photographs of 6-bit digital step attenuators: the (a) inductive and (b) capacitive correction structures and chip areas, excluding the pads, are $1250 \times 400\ \mu\mathrm{m}^2$ $(0.5\ \mathrm{mm}^2)$ and $670 \times 500\ \mu\mathrm{m}^2$ $(0.34\ \mathrm{mm}^2)$, respectively. They were fabricated in 1P6M 0.18-μm CMOS technology. The digital step attenuators were measured with on-chip probing using an Anritsu

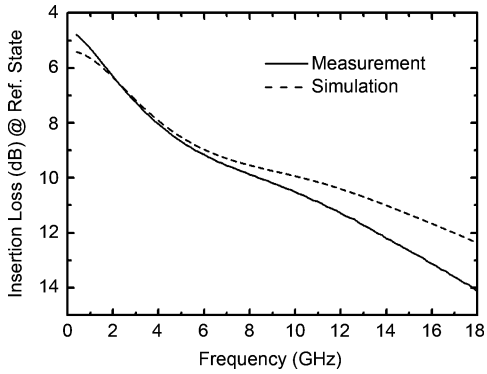

Fig. 23. Measured and simulated insertion loss at reference state (capacitive correction structure).

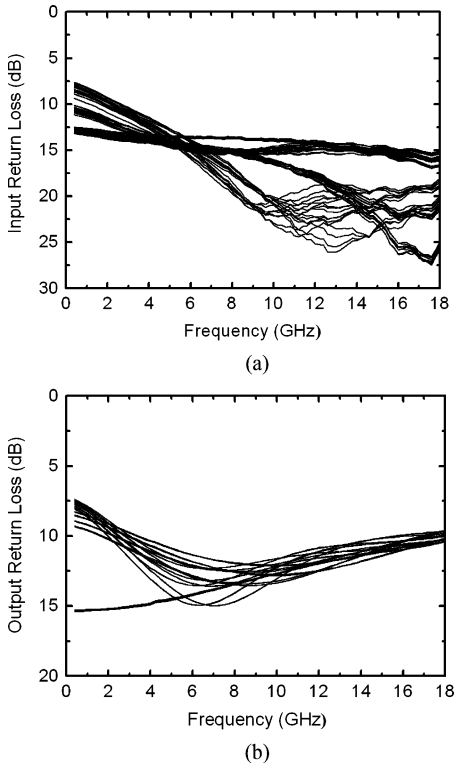

Fig. 24. Measured: (a) input and (b) output return loss (capacitive correction structure).

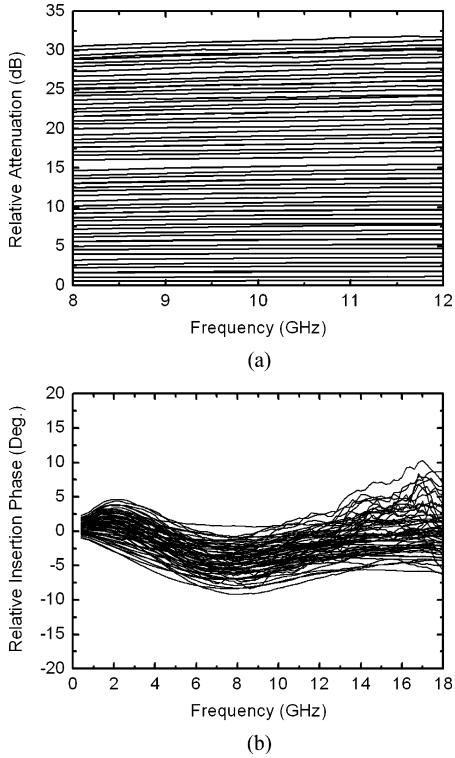

Fig. 25. Measured: (a) relative attenuation, and (b) relative insertion phase of 64 different states of the digital step attenuator (capacitive correction structure).

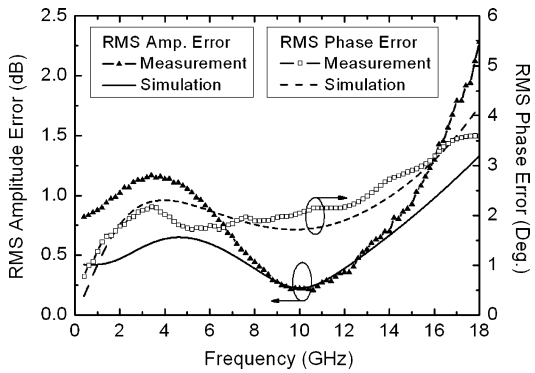

Fig. 26. Measured and simulated rms amplitude error and rms phase error (capacitive correction structure).

37397D network analyzer. The gate control voltage of 1.8 V was used. They consume no dc power.

A. Inductive Correction Structure

Fig. 19 shows the measured and simulated insertion losses at the reference state of the inductive correction structure. The attenuator has an insertion loss (of the reference state) of 8.7 dB at 10 GHz and 8–9.3 dB at 8–12 GHz. The measured input and output return losses of all attenuation states are shown in Fig. 20. The return loss is higher than 10 dB at 8–12 GHz, and higher than 9 dB at 0–14 GHz. Fig. 21(a) shows the measured attenuation relative to that of the reference state. The attenuation range is 31.5 dB at 10 GHz, and 31.5 ± 0.5 dB at 8–12 GHz. Fig. 21(b) shows the measured insertion phase relative to that of the reference state. The insertion phase is varying from -12° to 5° over 8–12 GHz. Fig. 22 shows the measured and simulated rms amplitude and phase errors. The rms amplitude deviation is less than 0.3 dB at 8–12 GHz, and is less than 0.5 dB at dc–14 GHz. The rms phase error is less than 3.8° at 8–12 GHz, and is less than 4.2° at dc–14 GHz.

B. Capacitive Correction Structures

Fig. 23 shows the measured and simulated insertion losses at the reference state of the capacitive correction structure. The attenuator has an insertion loss (of the reference state) of 10.5 dB at 10 GHz and 9.8–11.3 dB at 8–12 GHz. The measured input and output return losses of all attenuation states are shown in Fig. 24. The return loss is higher than 11 dB at 8–12 GHz. Fig. 25(a) shows the measured attenuation relative to that of the reference state. The attenuation range is 31.2 dB at 10 GHz,

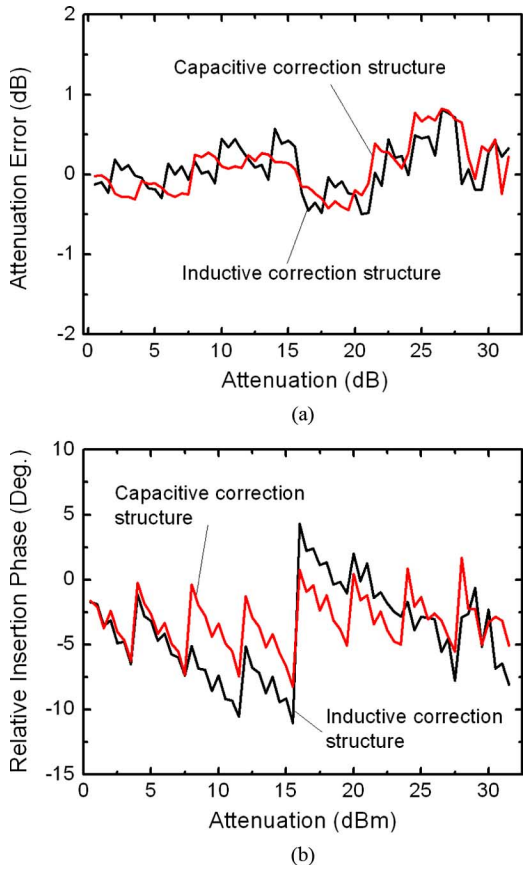

Fig. 27. Measured: (a) attenuation errors and (b) insertion phases of the inductive and capacitive correction structures over the 64 attenuation states at 10 GHz, respectively.

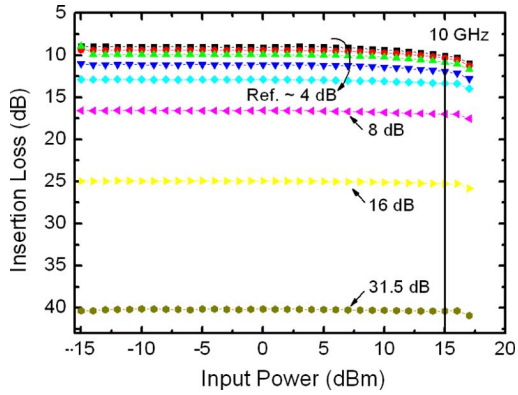

Fig. 28. Measured power-handling capabilities of the major states (ref., 0.5, 1, 2, 4, 8, 16, 31.5 dB) at 10 GHz (inductive correction structure).

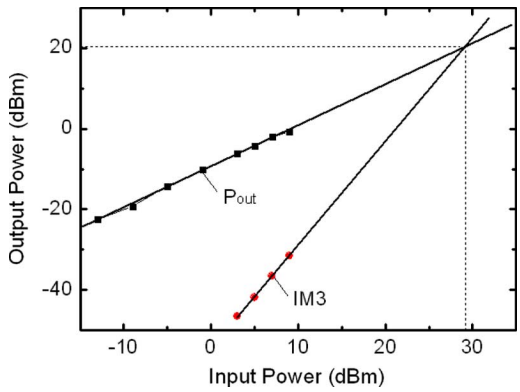

Fig. 29. Measured two-tone intermodulation ($f_1 = 9.995$ GHz, $f_2 = 10.005$ GHz) response at 10 GHz versus input power (inductive correction structure).

31.2 ± 0.5 dB at 8–12 GHz. Fig. 25(b) shows the measured insertion phase relative to that of the reference state. The insertion phase varies from -9° to 3° over 8–12 GHz. Fig. 26 shows the measured and simulated rms amplitude and phase errors. The rms amplitude deviation is less than 0.4 dB at 8–12 GHz. The rms phase error is less than 2.2° at 8–12 GHz.

C. Accuracy Comparison Between Inductive and Capacitive Correction Structures

Fig. 27 shows the attenuation errors and insertion phases of the inductive and capacitive correction structures over the 64 different attenuation states at 10 GHz, respectively. The attenuation error is the difference between the desired attenuation (from 0 to 31.5 dB with 0.5-dB step) and the measured attenuation. The inductive and capacitive structures have the attenuation errors varying from -0.5 to 0.7 dB overall 64 states, as shown in Fig. 27(a). The insertion phases of the inductive and capacitive structures, as shown in Fig. 27(b), vary from -11° to 4° and from -8° to 2° over all 64 states, respectively. Here, the ripples of the insertion phase are occurred from the phase changes by the on and off transition of each attenuation bit according to the attenuation states. The insertion phase variations by the on and off transitions of the lower 4-bits (0.5, 1, 2, and 4 dB) are nearly the same, e.g., the insertion phases of the attenuation states from 0.5 to 7.5 dB or from 8.5 to 15.5 dB, as shown in Fig. 27(b). For 8- and 16-dB attenuation bits, however, the insertion phase changes of the two structures are quite different. Comparing with the inductive correction structure, the phase variation of capacitive correction structure is even lower and better agree with the simulation results, as shown in Figs. 22 and 26. The inductive correction structure employs the spiral inductors not supported by the foundry model library in 8- and 16-dB attenuation bits. Some errors caused by EM simulation brought more or less the differences between the simulated results and the measured results.

D. Power-Handling Capabilities

Fig. 28 shows the measured power-handling capabilities of the inductive correction structure. The insertion losses of the major states (ref., 0.5, 1, 2, 4, 8, 16, 31.5 dB) versus input power are measured at 10 GHz. The input $P_{1\,\mathrm{dB}}$ of the inductive correction structure is 15 dBm at 10 GHz. The capacitive correction structure has also the input $P_{1\,\mathrm{dB}}$ of 13 dBm at 10 GHz. The two tone measurement is performed to characterize the input third-order intercept point (IIP3). The spacing of the two tones is 10 MHz. Fig. 29 shows the measured two-tone intermodulation ($f_1 = 9.995$ GHz, $f_2 = 10.005$ GHz) response of the inductive correction structure at 10 GHz versus input power. The measured input IP_3 values are 29 dBm for the inductive correction structure and 28 dBm for the capacitive correction structure, respectively.

TABLE III
SUMMARY OF DIGITAL STEP ATTENUATORS

Ref.	Freq. (GHz)	Attenuation range (dB)	Tech.	Insertion Loss (dB)	Return loss (dB)	P1dB/ IIP3 (dBm)	RMS Attenuation Error (dB)	RMS Phase Error (°)	Structure	Size (mm^2)
[6]	0.1 – 20	23 (5-Bit) (LSB = 0.75 dB)	GaAs	3-5	> 15	26/ 32	< 1 < 0.4 (Cal.)	-13-21	N/A	2.34 x 1.5 (3.51)
[7]	DC – 18	27.9 (5-Bit) (LSB = 0.9 dB)	GaAs	3-7	> 17	24/ -	< 0.5	10 (0 - 18)	N/A	2.4 x 1.6 (3.84)
[14]	DC – 20	23.5 (4-Bit) (LSB = 1.5 dB)	GaAs	< 5	> 13	24/ -	0.5	Not Available (N/A)	Switched T	2.6 x 1.6 (4.16)
[16]	8 – 15	23.5 (6-Bit) (LSB = 0.5 dB)	GaAs	< 4.5	> 8	N/A	< 0.45	N/A	Switched Pi/T	3 x 2 (6)
[17]	DC – 40	23 (5-Bit) (LSB = 1 dB)	GaAs	4-10	> 14	N/A	N/A	N/A	Switched T	2.8 x 1.6 (4.48)
[18]	0.045-50	70 (LSB = 2 dB)	GaAs	2-4	> 11	N/A	N/A	N/A (< ±0.86)	Switched T	3.68 x 1.58 (5.81)
[19]	8.5-11.5	15.5 (5-Bit) (LSB = 0.5 dB)	GaAs	N/A	N/A	N/A	N/A	N/A (< ±6)	Switched T	N/A
[13]	10 – 50	11 (12-Bit) (LSB = 0.9 dB)	0.12-μm BiCMOS	2-3	> 9	4/ -	N/A	3	Distributed	*0.75 x 0.2 (0.15)
This work 1	8 – 12 (X-band)	31.5 (6-Bit) (LSB = 0.5 dB)	0.18-μm CMOS	8 – 9.3	> 10	15/ 29	< 0.3	< 3.5 (-12 – 5)	Switched Pi/T w/ inductive phase correction	*1.25 x 0.4 (0.5)
	DC – 14			3.7 – 10	> 9		< 0.5	< 4.2 (-14 – 5)		
This work 2	8 – 12 (X-band)	31.5 (6-Bit) (LSB = 0.5 dB)	0.18-μm CMOS	9.8 – 11.3	> 11	13/ 28	< 0.4	< 2.2 (-9 – 3)	Switched Pi/T w/ capacitive phase correction	*0.67 x 0.5 (0.34)

* The chip sizes are excluding pads

E. Comparison to Other Digital Step Attenuators

Table III compares the performance of the reported digital step attenuators. Compared with the GaAs attenuators [11], [13], [14], the proposed attenuators demonstrates the highest attenuation of 31.5 dB (6-bit) and the highest resolution of 0.5 dB with the lowest insertion phase variation and the smallest chip size. The insertion losses are higher and $P_{1\ \mathrm{dB}}$ values are lower than those of the GaAs attenuators because of the relatively poor performance of the CMOS transistors. The proposed attenuators are also the first fully integrated CMOS digital step attenuators with wideband characteristics covering dc–14 GHz.

VII. CONCLUSION

The proposed CMOS digital step attenuators have been designed with a method of alleviating the tradeoff between the insertion phase characteristic and the insertion loss of conventional switched Pi/T attenuators. The attenuators employ a phase/ amplitude correction network that includes a low-pass filter. Appropriate bit ordering to obtain the optimal performance is discussed in terms of loading effects and power-handling capability. The 6-bit digital step attenuators were fabricated with inductive and capacitive correction structures in 0.18-μm CMOS technology with the high attenuation range of 31.5 dB and the high resolution of 0.5 dB. The digital step attenuator with inductive correction exhibits less than 0.3 dB/3.5°rms amplitude/phase errors at 8–12 GHz, and has broadband characteristics over dc–14 GHz. The attenuator with capacitive correction shows less than 0.4 dB/2.2°rms amplitude/phase errors over 8–12 GHz. Die areas are 0.5 mm^2 and 0.34 mm^2, respectively. The insertion losses are 8.7 and 10.5 dB at 10 GHz, and the return losses are higher than 10 and 11 dB at 8–12 GHz. The input $P_{1\ \mathrm{dB}}$ and input IP_3 values are 15 and 29 dBm for the inductive correction structure, and 13 and 28 dBm for the capacitive correction structure, respectively. For phased-array systems at X-band, the proposed CMOS digital attenuators are competitive with GaAs attenuators due to its high attenuation and phase accuracy, wide band of operation, compact chip area, etc.

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REFERENCES

[1] F. Ellinger, R. Vogt, and W. Bachtold, "Calibratable adaptive antenna combiner at 5.2 GHz with high yield for laptop interface card," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 12, pp. 2721–2720, Dec. 2000.

[2] B. A. Kopp, M. Borkowski, and G. Jerinic, "Transmit/receive modules," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 827–834, Mar. 2002.

[3] M. Hangai, H. Asao, M. Hieda, M. Yamaguchi, and M. Miyazaki, "Amplitude/phase temperature compensation attenuators with variable-Q FET resonators," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 12, pp. 3058–3065, Dec. 2008.

[4] D. Roques, J. Cazaux, and M. Pouysegur, "A new concept to cancel insertion phase variation in MMIC amplitude controller," in *Proc. IEEE Microw. Millimeter-Wave Monolithic Circuits Symp.*, Dallas, TX, May 1990, pp. 59–62.

[5] S. Walker, "A low phase shift attenuator," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 2, pp. 182–185, Feb. 1994.

[6] H. Dogan, R. G. Meyer, and A. M. Niknejad, "Analysis and design of RF CMOS attenuators," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2269–2283, Oct. 2008.

[7] R. Kaunisto, P. Korpi, J. Kiraly, and K. Halonen, "A linear-control wideband CMOS attenuator," in *Proc. IEEE Int. Circuits Syst. Symp.*, Sydney, Australia, 2001, vol. 4, pp. 458–461.
[8] L. Sjogren, D. Ingram, M. Biedenbender, R. Lai, B. Allen, and K. Hubbard, "A low phase-error 44-GHz HEMT attenuator," *IEEE Microw. Guided Wave Lett.*, vol. 8, no. 5, pp. 194–195, May 1998.
[9] J. K. Hunton and A. G. Ryals, "Microwave variable attenuators and modulators using PIN diodes," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-10, no. 7, pp. 262–273, Jul. 1962.
[10] B.-W. Min and G. M. Rebeiz, "A 10-50-GHz CMOS distributed step attenuator with low loss and low phase imbalance," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2547–2554, Nov. 2007.
[11] B. Khabbaz, A. Pospishil, and H. P. Singh, "DC-to-20-GHz MMIC multibit digital attenuators with on-chip TTL control," *IEEE J. Solid-State Circuits*, vol. 27, no. 10, pp. 1457–1462, Oct. 1992.
[12] D. Krafcsik, F. Ali, and S. Bishop, "Broadband, low-loss 5- and 6-bit digital attenuators," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Orlando, FL, May 1995, pp. 1627–1630.
[13] J. C. Sarkissian, M. Delmond, E. Laporte, E. Rogeaux, and R. Soulard, "A Ku-band 6-bit digital attenuator with integrated serial to parallel converter," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Anaheim, CA, Jun. 1999, pp. 1915–1918.
[14] I.-K. Ju, Y.-S. Noh, and I.-B. Yom, "Ultra broadband DC to 40 GHz 5-bit pHEMT MMIC digital attenuator," in *Proc. Eur. Microw. Conf.*, Paris, France, Oct. 2005, pp. 995–998.
[15] Y. S. Dai, D. G. Fang, and Y.-X Guo, "A novel UWB (0.045–50 GHz) digital/analog compatible MMIC variable attenuator with low insertion phase shift and large dynamic range," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 1, pp. 61–63, Jan. 2007.
[16] W. Ciccognani, F. Giannini, E. Limiti, and P. E. Longhi, "Compensating for parasitic phase shift in microwave digitally controlled attenuators," *Electron. Lett.*, vol. 44, no. 12, pp. 743–744, Jun. 2008.
[17] N. D. Doddamani and A. V. H. Nandi, "Design of SPDT switch, 6 bit digital attenuator, 6 bit digital phase shifter for L-band T/R module using 0.7 μm GaAs MMIC technology," in *Int. Signal Process. Commun. Network. Conf.*, Feb. 22–24, 2007, pp. 302–307.
[18] R. Baker, "CMOS-based digital step attenuator designs," *Wireless Design Dev.*, pp. 46–50, May 2004.
[19] D.-W. Kang, H. D. Lee, C.-H. Kim, and S. Hong, "Ku-band MMIC phase shifter using a parallel resonator with 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 294–301, Jan. 2006.
[20] M. A. Morton, J. P. Comeau, J. D. Cressler, M. Mitchell, and J. Papapolymerou, "Sources of phase error and design considerations for silicon-based monolithic high-pass/low-pass microwave phase shifters," *IEEE Microw. Theory Tech.*, vol. 54, no. 12, pp. 4032–4040, Dec. 2006.

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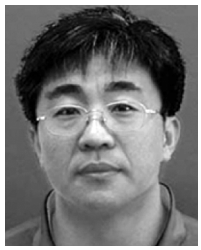

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