The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's

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***Abstract*—The results of a comprehensive investigation into the characteristics and optimization of inductors fabricated with the top-level metal of a submicron silicon VLSI process are presented. A computer program which extracts a physics-based model of microstrip components that is suitable for circuit (SPICE) simulation has been used to evaluate the effect of variations in metallization, layout geometry, and substrate parameters upon monolithic inductor performance. Three-dimensional (3-D) numerical simulations and experimental measurements of inductors were also used to benchmark the model accuracy. It is shown in this work that low inductor Q is primarily due to the restrictions imposed by the thin interconnect metallization available in most very large scale integration (VLSI) technologies, and that computer optimization of the inductor layout can be used to achieve a 50% improvement in component Q-factor over unoptimized designs.**

***Index Terms*— Computer-aided design, HF analog integrated circuits, MMIC's, modeling, monolithic inductors, RFIC's, silicon integrated circuit technology.**

I. Introduction

RADIO frequency (RF) circuits fabricated in monolithic microwave integrated circuit technologies (such as GaAs MMIC) make extensive use of on-chip transmission lines to realize an inductance, the inductor being a key component in many high-performance narrowband circuit designs. Silicon IC technologies have rarely been used for analog applications in the radio and microwave range of frequencies, primarily because transmission line structures perform poorly on the semiconducting substrates used to manufacture silicon IC's [1]. In order to exploit the capabilities offered by a monolithic inductance, the limitations imposed by silicon technology upon the component performance must be accurately modeled and characterized. The ability to optimize and refine silicon circuit designs incorporating on-chip inductors has been identified by others [2] as lacking in the present state of the design art.

A computationally efficient, scalable, lumped-element model which can be applied to an arbitrary configuration of microstrip transmission lines, such as the monolithic spiral inductor [3]–[5], will be described in this paper. An efficient and scalable inductor model can be used to rapidly optimize the electrical performance of an inductor for an RF IC application. The accuracy of the lumped element model is evaluated for variations in metallization thickness, layout geometry, and substrate parameters, using a combination of three-dimensional (3-D) numerical simulations and experimental measurements. The results of this investigation highlight areas where process improvements and parameter optimization can be applied to maximize the performance of RF circuits using silicon-based inductor designs. Some design guidelines for maximizing the inductor performance in similar technologies will also be described.

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II. The Monolithic Inductor

Resonant-tuned (*LC*) circuits offer numerous benefits to the designer of high-frequency circuits. Operation at a low supply voltage, simplified impedance matching between stages, and low dissipation for reduced circuit noise are just a few of the properties of *LC* circuits that can be exploited to achieve a higher level of performance from a given fabrication technology. However, an on-chip inductance is required for the realization of *LC* networks for these purposes. At radio and microwave frequencies, a purely passive inductor is often preferable to synthesis of an inductive reactance with an active circuit. Passive components introduce less noise, consume less power, and have a wider bandwidth and linear operating range than their electronic equivalents, such as the gyrator.

Passive inductors can be implemented on-chip using transmission lines. The input impedance (Z_{in}) of a short section of transmission line which is terminated in a short circuit can be written as follows:

$$Z_{\mathrm{in}} = Z_0 \cdot \gamma l = (r + j\omega L)l \tag{1}$$

where Z_0 is the characteristic impedance and γ is the propagation constant for a transmission line of length, l. Here it is assumed that the physical length of the line is shorter than one-tenth of a wavelength at the desired frequency of operation, that is, the line appears to be "electrically short." From (1), the input impedance will be either resistive or inductive, depending upon the value of the resistance/unit length, r, compared to the inductance/unit length, L, of the transmission line. For low resistivity metals such as the interconnect metallization used on an integrated circuit chip, the input impedance can be made to appear predominantly inductive. The ratio of the series inductance to shunt capacitance per unit length defines the characteristic impedance (Z_0) of the transmission line. Maximizing the characteristic impedance (e.g., using a narrow metal line) will reduce the length of line that is required to realize a given inductance.

The microstrip transmission line structure on a silicon IC consists of a metal strip above a conducting (or ground) plane, with the substrate and intermetal oxide layers sandwiched between the two conductors. For dimensions typically encountered in a commercial IC fabrication process (metal linewidths between 5–50 μm on a 350-μm thick substrate), the characteristic impedance of a microstrip line ranges from approximately 100–200 Ω. The substrate behavior depends upon both the resistivity and the frequency of the propagating wave. However, the substrate tends to behave as a lossy dielectric in modern silicon very large scale integration (VLSI) processes [6], where resistivities are typically in the 1–100 Ω-cm range and operation is in the GHz range of frequencies.

The largest inductive reactance that can be realized on-chip is determined from the following equation:

$$\text{Inductive reactance} < 2\pi Z_{0,\max} \bullet \frac{l}{\lambda} = 40\pi\,\Omega \qquad (2)$$

where l is the transmission line length and λ is the guided wavelength. A short transmission line (i.e., less than one-tenth of a wavelength long) is assumed here, with a maximum characteristic impedance of 200 Ω. The inductive reactance from (2) corresponds to an inductance of 20 nH at a frequency of 1 GHz. This is close to the upper limit that can be realized monolithically in a standard silicon process. The smallest inductance value for most practical circuit applications in the 1–3 GHz range of frequencies is on the order of 1 nH. The losses introduced by the semiconducting substrate in a silicon IC technology restrict the Q-factor to less than ten for most commercial IC processes.

In addition to the rectangular geometry used here, circular and octagonal geometries are also widely used to implement microstrip spiral inductors. Although an improvement in Q-factor of up to 10% is possible using a circular rather than square design, the circular spiral consumes greater chip area, and introduces difficulties in the efficient generation of photomasks [7], [8]. In addition, the interaction between the magnetic field components on adjacent sides of a nonrectangular spiral inductor adds extra complexity to the development of a circuit model. Thus, only the rectangular spiral inductor will be considered in the following discussion.

The spiral inductor structure, while compact and more space efficient than an equivalent straight wire inductor, is more difficult to analyze. The accurate characterization of this structure at microwave frequencies requires an analysis of the fringing fields, parasitics, ground plane effects, and most importantly for silicon IC design, an analysis of the effect of the conductive substrate on the component performance. These effects cannot be fully analyzed to yield closed-form expressions which adequately predict the inductor behavior, and hence, numerical analysis is required in order to determine the parameters of the inductor's electrical model.

III. The Monolithic Inductor in Silicon Technology

The performance of rectangular spiral microstrip inductors in a 0.8-μm silicon BiCMOS technology was reported by Nguyen and Meyer in 1990 [10]. The inductors were fabricated using a microstrip transmission line wound as a square spiral, and their electrical behavior was modeled adequately by a lumped inductance with a few additional parasitic (RC) components. Some simple *LC* filtering and signal processing circuits using these inductors were also demonstrated [11], [12], although the performance of the circuits was limited by the low Q of the inductors, which was less than five. Silicon RF integrated circuits incorporating monolithic inductors for product applications have subsequently been developed and demonstrated by a number of manufacturers [13]–[15].

The characteristics of inductors fabricated in various silicon technologies have been studied and reported in the literature. The main motivation behind these studies has been improvement in the inductor quality through a modification of the metallization scheme and/or the properties of the underlying substrate. The methods which have been employed to date have included: thicker metallization [16], stacking of metal layers in a multilevel metal process [17], thicker intermetal oxide [18], fabrication using high-resistivity silicon substrates [16], and the selective removal of silicon from beneath the inductor structure by chemical etching [19]. Justification for these experimental investigations has come from a heuristic assessment of the parameters limiting inductor performance or from numerical simulations of the inductor's electrical characteristics using commercially available electromagnetic field solvers.

IV. Silicon Monolithic Inductor Model

A circuit model which describes the electrical behavior of the monolithic inductor at RF and microwave frequencies is required for the computer simulation and optimization of tuned circuits fabricated in silicon IC technologies. Modeling of spiral inductors on silicon has been limited to reports of numerical simulation results [20] and/or parameter fitting of lumped-element equivalent circuits to measured data [16], [17]. Electrical circuit models for an inductor that are derived in this way cannot be scaled to reflect changes in the layout or fabrication technology.

Numerical simulators are now commercially available [21] which compute the electromagnetic field distribution of planar-type conductor configurations in three dimensions. These simulators can extract the circuit parameters (i.e., RLCG parameters) of the spiral inductor from the field solutions for use in a circuit simulator such as SPICE. However, a disadvantage of 3-D numerical simulation is that some sophistication on behalf of the user is required in order to get meaningful results. Another drawback is the limitation that processing speed and memory size place upon the structures which can be analyzed within a reasonable amount of time. Optimization of the Q-factor in a planar structure requires closely spaced microstrip lines for tight coupling of the magnetic field and wide microstrip lines in order to reduce the Ohmic losses in the microstrip. Hence, a large ratio of linewidth to line spacing is necessary, and this requires a substantial amount of computer memory and computation time in order to determine the circuit model parameters if a commercially available field solver package is employed.

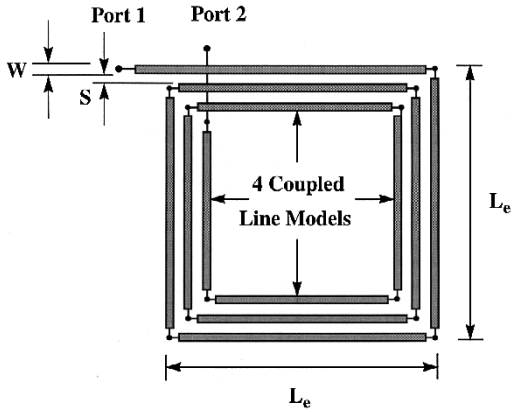


Fig. 1. Simplified microstrip spiral inductor layout (three turns).

TABLE I
MICROSTRIP LINE PARAMETERS [24]

Parameter	Value
Substrate resistivity, ρ	10 Ohm-cm
Substrate thickness, b_2	380 μm
Silicon dielectric constant	11.7
Oxide thickness, b_1	5 μm
Oxide dielectric constant	3.9
Metal resistivity	0.03 Ohm-μm

A. Scalable Inductor Model

A scalable inductor circuit model allows the circuit designer the flexibility to tailor the inductor design for a given RF application. Scalability implies that the electrical circuit parameters of the inductor model can be extracted from geometric and technological parameter specifications. A fully scalable model will allow any inductance value to be designed for use in an RF circuit. It also simplifies integration of the model into a typical CAD framework. The ability to generate inductor parameters on-demand eliminates the need to develop an inductor design library, which can be costly to generate and maintain.

Ohmic losses in the conductive substrate must be accounted for in the scalable model. These losses can be related to the three possible modes for the propagation of signals on transmission lines fabricated in the SiO_2/Si system: the skin-effect, slow-wave, and quasi-TEM modes. Lumped-element equivalent circuits for each propagating mode were proposed by Hasegawa [6], where the shunt parasitic components of the microstrip line can be represented (in general) by a combination of two capacitors and a resistor. This simplifying approximation can be applied to the spiral inductor as shown in Fig. 1, where the inductor is shown as a collection of short microstrip transmission line sections. Each transmission line section is physically short in length, and is therefore adequately described by a lumped-element model that includes series elements to model the inductance and resistance per unit length and shunt elements to model the substrate parasitics and losses. These lumped element models are then joined serially to model the entire spiral structure. The electric and magnetic coupling between parallel conducting strips must be accounted for in the model; however, the weak coupling between orthogonal strips is neglected in order to reduce the model complexity.

This segmented approach to microstrip inductor modeling was originated by Greenhouse [22], refined by others [23], and then extended to an arbitrary configuration of orthogonal microstrip lines by Rabjohn [3]. The flexibility and computational efficiency afforded by this approach have been adopted for the scalable inductor model developed in this work. The model capabilities have been extended to include the Ohmic losses in the conductive substrate.

A computer program, GEMCAP2 [3], [4], was used to extract the electrical parameters for a lumped-element circuit model from the inductor's specifications. The parameters of the lumped-element model for each microstrip line are computed from the layout geometry, using the substrate and metallization properties. Table I lists the technological parameters for the BiCMOS process [24] used to fabricate the inductors described in this paper. The self and mutual inductances for all parallel line segments are calculated from closed-form expressions, where the nonzero metallization thickness is incorporated in the self and mutual inductance calculations using the geometric mean distance of the conductor cross section [25].

The self-inductance, L (in nH), of a straight conductor with a rectangular cross section can be calculated from Grover's formulation for the mutual inductance between two current carrying filaments [26]. The self and mutual capacitances are computed using a two-dimensional (2-D) numerical technique developed for coupled microstrip lines [27]. The shunt resistance of the semiconducting layer can then be estimated directly from the quasistatic capacitance, $C_{\rm Si}$ [6]. Dissipation of the mutual capacitances is neglected because the microstrip lines are closely spaced. The frequency dependent resistance, r_{sk}, is approximated from closed form expressions [28] to form a complete lumped-element equivalent circuit representation.

As an example of the GEMCAP2 analysis technique, a circuit model can be derived for the spiral inductor illustrated in Fig. 1. The physical layout of the microstrip spiral is first partitioned into groups of multiple coupled lines for analysis; one group per side of the rectangular layout as shown in the figure. The parameters of a lumped-element π-equivalent circuit are then extracted for the individual microstrip lines in each group. Four such π-equivalents are required for a single turn of the spiral, as illustrated in Fig. 2, as well as lumped capacitors to model mutual capacitive coupling between the lines (represented by capacitors C_m in Fig. 2). Dependent current sources account for the mutual magnetic coupling between parallel strips in a group of coupled lines.

As the number of turns of the spiral increases, more lumped element sections are added to account for the additional coupled lines within each group. For an eight-turn spiral inductor with $N = 8$ microstrip lines per side, for example, there would be $4N$ or 32 lumped-element sections in total, along with the additional interconnecting elements to model the mutual capacitance between strips as in Fig. 2.

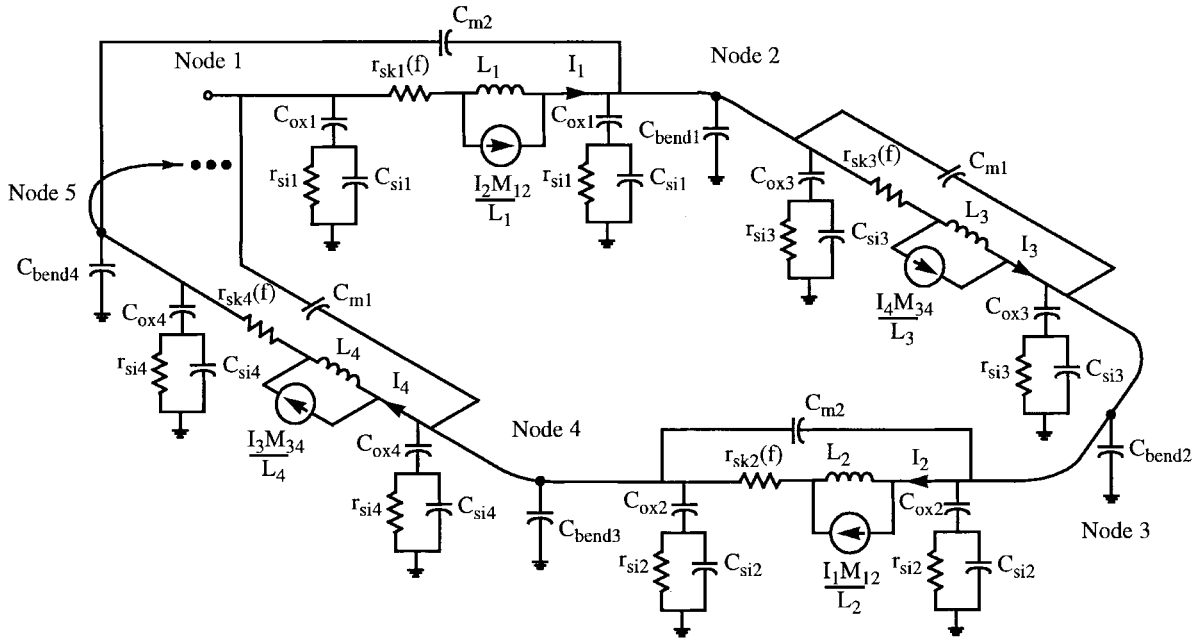


Fig. 2. Lumped-element circuit model for one turn of a spiral inductor.

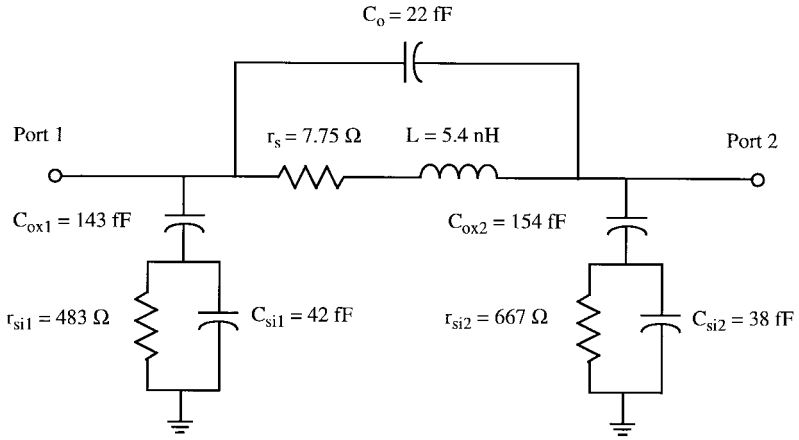


Fig. 3. Compact lumped-element circuit model for a spiral inductor ($N_t = 4.5$, $W = 10\,\mu$m, $S = 5\,\mu$m).

There are a number of other parasitics and higher-order effects which should be taken into consideration. Interwinding capacitance to the conductor used to contact the center of the spiral (usually an "underpass" in a multilevel metal process) can be modeled using lumped capacitors between the external terminal and the appropriate lumped-element sections. These capacitors are not shown in Fig. 2. Current crowding at the corners of the rectangular spiral adds parasitic inductance and capacitance which is accounted for by a connection of lumped elements $L_{\rm bend}$ and $C_{\rm bend}$ at each corner node (note that only $C_{\rm bend}$ is shown in Fig. 2). For frequencies in the low GHz range, this effect is quite small and is often neglected [29]. Coefficients are also added to the dissipative components of the model to account for the dependence of the inductor losses upon operating temperature.

The scalable circuit model can be used directly in a time domain (e.g., SPICE transient analysis) or frequency domain (e.g., Touchstone) circuit simulation along with other active and passive RF circuit elements. The complete model would normally be reduced to a compact model or S-parameter representation for faster optimization of a complex RF circuit.

B. Compact Inductor Model

A simplified or compact version of the fully scalable inductor model (i.e., a model with the minimum possible number of circuit elements) is required for hand calculations and to facilitate optimization of more complex RF circuit structures. For efficient optimization, the compact model should be easily derived from the complex scalable model structure.

A single π-type lumped-element section (as shown in Fig. 3) has been used by others as a compact model to fit experimental measurements of silicon monolithic inductors [10], [16], [17]. The L, C, and r parameters of the compact model can be established through a combination of parameter identification and fitting with the aid of a computer-driven optimizer.

Frlan [30] has shown that the compact model can be estimated directly from the parameters of the scalable model. Using this technique, the series resistance and inductance of the single π-model (r_s and L in Fig. 3) are obtained by simply summing the inductance and resistance of each individual microstrip section connected in series. The parasitic capacitances of the individual sections can be similarly summed into a single lumped capacitance for the compact model, with one shunt arm of the π-model representing the outer windings and the other arm modeling the inner winding parasitics. Resistances r_{Si} in the compact model are computed from the shunt capacitance, C_{Si}, making the complete parameter set consistent. From this initial estimate, it is possible to closely match to the electrical characteristics of the scalable model by refinement of the parameters using a computer optimizer. This approach is simple to implement with most commercial simulators that have the capability to optimize circuit parameters (e.g., HSPICE or Touchstone), and it requires little additional computation time to refine the small number of parameters in a single lumped-element section. The component values for the compact model shown in Fig. 3 were derived by estimation and fitting the scalable (GEMCAP2) model of a 4.5-turn spiral inductor. The shunt parasitics are not symmetric (i.e., C_{ox1} is not equal to C_{ox2}), which is a consequence of the asymmetry inherent in the spiral inductor layout. This model is simple enough to be useful for hand calculations in a circuit and it fits the GEMCAP2 model up to the first self-resonant frequency of the inductor. However, the parameters of the compact model cannot be easily adjusted for slight changes in the inductor design because of the nonphysical nature of this simple model.

C. Q-Factor Extraction and Computation from a Compact Model

The inductor Q-factor is used as a figure of merit to compare the performance of the spiral inductors studied in this work. The Q factor is defined by the ratio of the inductive reactance to the total dissipation, $(\omega L_S)/r_T$, for an equivalent circuit consisting of inductance L_S in series with a resistor (representing the total dissipation), r_T [31]. A measurement or simulation of the impedance parameters for a monolithic inductor will normally include the effect of capacitive parasitics, and therefore the inductive reactance and the total dissipation must be properly identified in order to determine the component Q. For a one-port, the Q-factor is often estimated by taking the ratio of the imaginary and real components of the one-port impedance. While this approximation is valid at low frequencies (less than 500 MHz), a significant error is caused by the parasitic capacitances of a spiral inductor as the frequency increases. This error is avoided by computing the Q-factor directly from the parameters of the compact model.

The procedure for compact model extraction from the fully scalable inductor model was outlined in the previous section of this paper. For experimental data, the compact model parameters (see Fig. 3) are determined by first estimating the inductance, L, and series resistance, r_s, from the impedance measured between Ports 1 and 2 at low frequency (i.e., where the parasitic capacitances have little effect), and then fitting the remaining parameters of the model using a computer-driven optimizer. Once the compact model parameters have been determined, the inductive reactance, the total dissipation, and the Q-factor are easily computed. For example, the Q-factor of an inductor connected as a one-port (i.e., with Port 2 in Fig. 3 grounded) can be estimated from the following equation:

$$Q\text{-factor} \approx \frac{\omega L}{r_s + \dfrac{\left(\dfrac{\omega}{\omega_{ox}}\right)^4 \cdot r_{\mathrm{Si1}}}{1+(\omega C_{ox1} r_{\mathrm{Si1}})^2}} \tag{3}$$

where ω_{ox} is the oxide resonant frequency defined by inductance L and capacitance C_{ox1}. Here the parasitic capacitances C_o and C_{Si} of the compact model have been assumed negligible in order to simplify the resulting expression. The two terms in the denominator represent the sources of dissipation in the monolithic inductor, which consist of the resistance of the metal lines (r_s) and the dissipation added by the conductive substrate.

Some insight into the relationships between circuit parameters and the Q-factor can be gained through examination of (3). It can be seen that decreasing C_{ox} through the use of a thicker oxide layer will increase both the oxide resonant frequency and the substrate corner frequency, $f_{sub} = 1/(2\pi C_{ox1} r_{\mathrm{Si1}})$, resulting in an improvement in the inductor Q-factor. Equation (3) also predicts that an increase in the substrate resistivity will cause a drop in the Q factor for frequencies much less than f_{sub} and an improvement in Q-factor for frequencies much greater than f_{sub}. However, it should be realized that the lumped equivalent model for the inductor shown in Fig. 3 is invalid when highly conductive substrates are used (less than approximately 1 Ω-cm), and hence (3) can only be used to approximate the inductor Q over a limited range of substrate resistivities.

V. Model Validation

In order to verify the accuracy of the scalable model, the behavior of a spiral inductor predicted by the lumped-element model (GEMCAP2 simulator) was compared with a 3-D electromagnetic field simulation. The 3-D numerical simulations were performed using a full-wave simulator for planar structures [21]. A 4.5-turn square spiral 5 nH inductor with a 10-μm wide line and a 5-μm line spacing was selected for this comparison. The ratio of line width to line spacing was kept small to ensure that the memory requirements and simulation time for the 3-D numerical computations were not excessive. It would be possible to optimize the inductor design for the best possible circuit performance, such as optimization of the inductor Q-factor, but this is not necessary for model validation.

The substrate and metallization parameters from the BiCMOS process from Table I were used to obtain the simulation results shown in Fig. 4. The inner terminal of the spiral was connected to ground and the impedance of the resulting one-port network as a function of frequency was computed in both cases. Excellent agreement is seen between the real

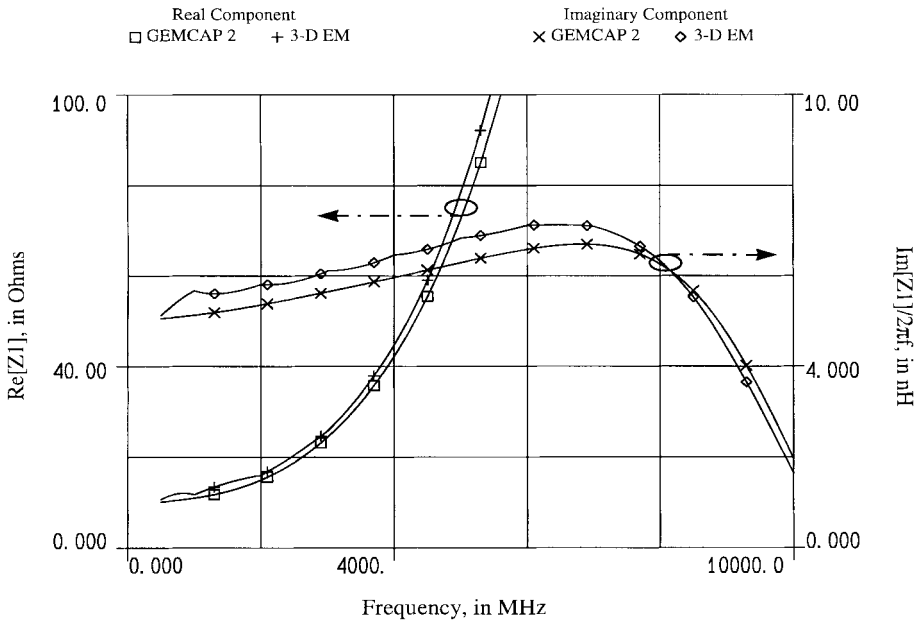
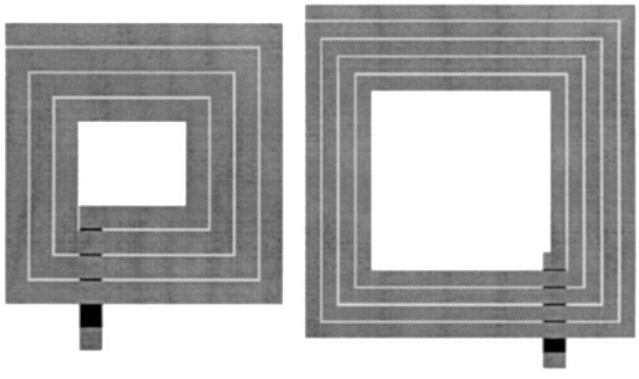


Fig. 4. Simulated one-port impedances for a 5 nH inductor ($N_t = 4.5$, $W = 10\,\mu$m, $S = 5\,\mu$m).

and imaginary parts of the one-port impedance simulated using numerical simulation (3-D EM) and the lumped-element model (GEMCAP2) almost up to the self-resonant frequency (i.e., where the imaginary part of the impedance is zero). Both simulations predict a low-frequency inductance (which is given by the reactive portion of the impedance divided by the radian frequency) close to 5 nH with a self-resonant frequency of approximately 10 GHz. The consistent difference in the reactive component of the impedance is due in part to the fact that the finite thickness of the conducting strip is not accounted for in the numerical simulations. An increase in the conductor thickness causes the inductance, and hence the inductive reactance, to decrease. At low frequencies, the resistive component of the impedance is close to the dc resistance of the inductor, which is about 8.5 Ω. As the frequency increases, the resistive component of the loss increases greatly due to losses in the substrate and skin effect in the metal conductors.

Design of an inductor to fit a particular application would require extensive simulation work in order to determine the number of turns, line width, and line spacing necessary to achieve the best performance within a given technology. Extraction of a lumped element component model is faster than other simulation methods, making this type of optimization more practical. In this particular example, the computation of the lumped-element model parameters was performed in less than 2 min on a SUN SPARC-2 work station. By comparison, 3-D EM simulation of the one-port impedance required approximately 5 min per frequency point on the same work station (equipped with 64 MBytes of RAM), or 50 min for 11 data points between 0.5–10 GHz. It should be noted that a large ratio of line width to line spacing is desirable in order to maximize the coupling between adjacent microstrip lines in the spiral inductor. The time required for a 3-D numerical simulation increases with the ratio of line width to line spacing, while computation time for the lumped-element model is unaffected by the choice of line width or line spacing. This fact, combined with the large advantage in computational efficiency for even simple structures, lends a considerable advantage in both speed and flexibility to the lumped-element modeling approach when compared to 3-D numerical simulation.



(a) (b)

Fig. 5. Inductor layouts used for characterization experiments.

VI. Experimental Measurement

The effect of layout geometry, metallization thickness, and substrate parameters upon the inductor performance has been investigated experimentally. The number of turns of the rectangular spiral, the metal line width, and the metal spacing were each varied independently in order to determine the effect of the physical layout upon the inductor performance. In addition, the effect of changes in the oxide thickness and the silicon substrate resistivity were also explored experimentally. A 3.5-turn spiral inductor with a nominal inductance of 1800 pH (as shown in part (a) of Fig. 5) was used for the metal and oxide thickness experiments, while the 4.5-turn 5 nH

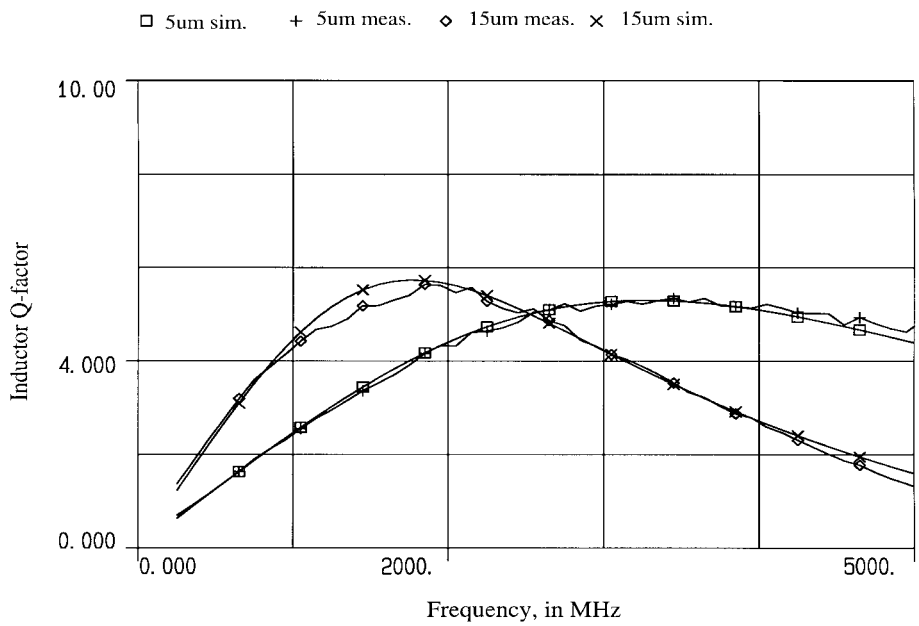


Fig. 6. Q-factor as a function of metal width ($L = 5$ nH).

inductor (shown in part (b) of the same figure) was used to characterize the effect of layout and substrate variations upon the inductor performance. It should be noted that both of these designs exploit the large line width to line spacing ratio that is possible in modern silicon VLSI technologies and would require excessively long simulation times if 3-D numerical simulation were used to predict the inductor behavior. The results of the experimental measurements are useful as a benchmark to confirm the predictions of the lumped-element (i.e., GEMCAP2) computer model and also to provide insight into the possible optimization of different aspects of the inductor performance, such as the Q-factor.

The experimental data was collected from on-wafer measurements of the two-port S-parameters for each inductor test structure using coaxial RF probes. The measured data in each case was fitted to a compact model for the inductor, as described in Section IV-C, and the one-port impedance parameters (or the Q-factor) computed from the resulting parameter set by grounding Port 2 of the inductor compact model (refer to Fig. 3).

A. Inductor Layout (Metal Width, Spacing, and Number of Turns)

The measured Q-factor of a rectangular spiral inductor and the performance predicted by the lumped-element computer model for conductor widths of 5 and 15 μm are shown in Fig. 6. A layer of top-level aluminum 1 μm thick was used to fabricate a 4.5-turn spiral with an inductance of 5 nH in each case. The outside dimensions of the inductor (L_e in Fig. 1) were increased in order to maintain a constant inductance value in both cases.

At frequencies well below the peak in the inductor Q, the shunt parasitics of the spiral inductor have little effect and consequently the inductive reactance and inductor Q increase with frequency. However, as the operating frequency continues to rise, the dissipation of energy in the semiconducting substrate and the ac resistance of the metallization begin to increase faster than the inductive reactance. Thus, the Q-factor peaks, and then decreases. The larger surface area of the inductor with wide conductor metallization results in higher parasitic capacitances, which lowers the inductor self-resonant frequency and increases the substrate dissipation. This confirms the behavior predicted by (3). In addition, the distribution of current across the conducting strip is nonuniform as a result of the skin effect, causing the ac resistance of the metallization to increase at higher frequencies. As the strip widens, the penalty in ac resistance due to the skin effect will increase at a given frequency [28]. Thus, the peak of the inductor Q-factor shifts to a lower frequency as the conductor width increases. However, this can be used to advantage in the optimization of a given inductor for the maximum Q within a desired range of frequencies.

The effect of the spacing between conductor lines on inductor Q-factor has also been investigated. Narrow line spacings were found to increase the magnetic coupling between windings, which causes an increase in the inductance and the Q-factor for a given layout area as shown in Fig. 7. For the thin metallization used to fabricate on-chip inductors, interwinding capacitance was found to have a negligible effect upon the performance as shown in the figure. However, there is a significant improvement in the Q-factor when the minimum spacing is used.

The relationship between the number of turns of the spiral and the peak Q-factor for a given inductance was also investigated experimentally, and the results are listed in Table II. The outer dimensions of the spiral were varied in order to realize an inductance of 5 nH for each design. The line width and line spacing were kept constant at 10 and 1.5 μm, respectively. The drop in inductor Q as the number of turns increases is related to the distance (or gap) between opposite sides at the center

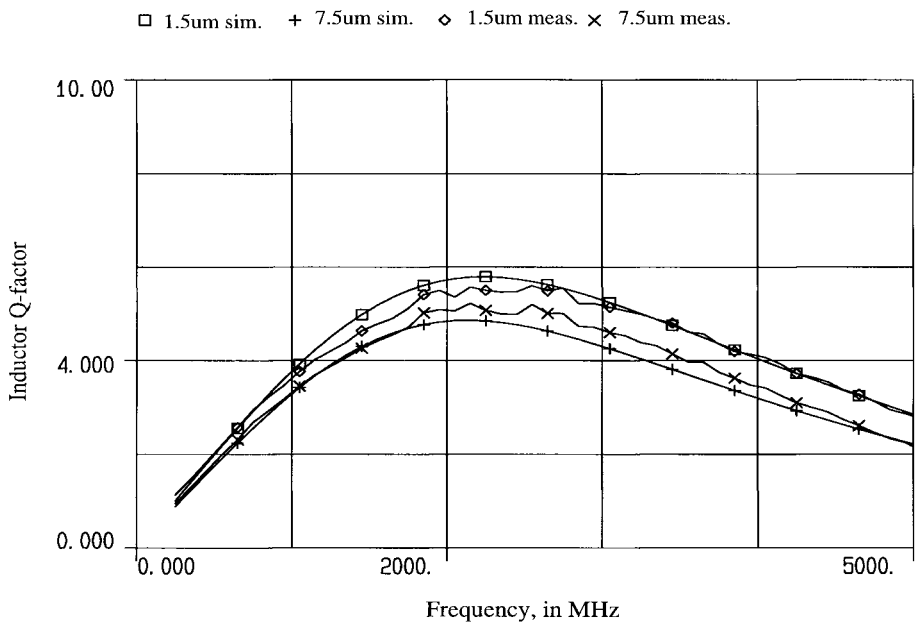


Fig. 7. Q-factor as a function of metal spacing ($L = 5$ nH).

TABLE II
NUMBER OF TURNS VERSUS THE PEAK INDUCTOR Q-FACTOR FOR A CONSTANT INDUCTANCE OF 5 nH ($W = 10\,\mu$m, $S = 1.5\,\mu$m)

Number of Turns	Peak Q-factor	Outer Length, Le	Gap Between Opposite Sides	Total Length of Spiral
3.5	5.8	255 μm	177 μm	3.02 mm
4.5	5.7	216 μm	115 μm	2.98 mm
5.5	5.6	199 μm	75 μm	3.00 mm
6.5	5.3	191 μm	45 μm	3.06 mm
7.5	5.0	190 μm	20 μm	3.12 mm

of the spiral. As the number of turns increases, the spacing between opposite sides of the spiral shrinks, causing a drop in inductance because of negative mutual coupling. Thus, more metal is required to maintain a constant inductance value of 5 nH, and the total length of the spiral begins to increase as seen from the data listed in the table. Increasing the number of turns reduces the outer dimension of the spiral (L_e) and conserves chip area; however, some space is required at the center of the spiral in order to realize the highest Q-factor.

B. Metallization Thickness

Thin metallization in most VLSI processes limits the quality factor of microstrip inductors, because energy is dissipated by the finite resistivity of the metallization as well as in the conductive substrate. The quality of the spiral inductor, or Q-factor, could therefore be improved by increasing the conductor thickness. The measured quality factor for a 1.8-nH spiral inductor fabricated with 1–3 μm thick metal layers is plotted in Fig. 8. This inductor consists of 3.5 turns of 15-μm wide top-level metal in the BiCMOS process with a line spacing of 1.5 μm. The measured behavior of the inductor fabricated with thicker metal shows close agreement with the predictions of the lumped-element circuit model. The Q-factor initially rises with frequency as the reactive component of the impedance increases, peaks, and then decreases due to the increasing dissipation of energy at higher frequencies. The inductor Q-factor at 3 GHz improves from five to ten when the thickness of the aluminum metal layer is increased from 1 to 3 μm. The improvement in inductor Q is less than a factor of three (as would be expected from resistance considerations) because the inductance is inversely proportional to the thickness of the conductor. Hence, the inductance decreases with increasing metal thickness, lowering the Q. The frequency dependence of the conductor resistance, or the skin effect, is more pronounced as the thickness of the metallization is increased, which also contributes to higher dissipation and a lower Q-factor at RF. The measured behavior of the inductor fabricated with thicker metal also showed close agreement with the predictions of the lumped-element circuit model. These results indicate that inductors suitable for many RF IC applications could be fabricated in production silicon technologies, if a low resistivity metal of adequate thickness were available.

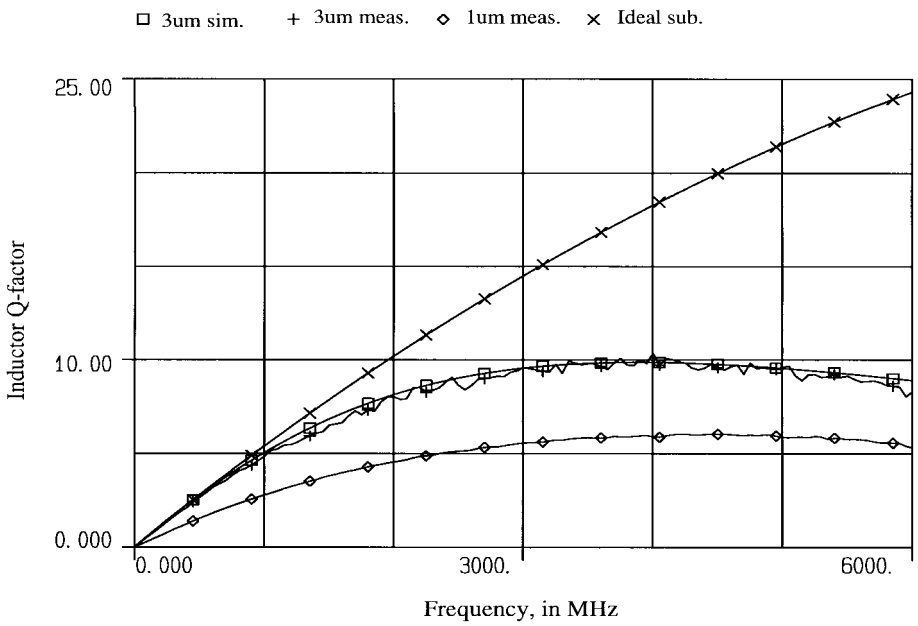


Fig. 8. Q-factor for different metal thickness ($L = 1.8$ nH).

The Q-factor predicted by GEMCAP2 for the same planar spiral on a lossless substrate (Ideal sub.) is also plotted in the Fig. 8 for comparison. The slight downward curvature is the result of capacitive parasitics which cause self-resonance. In addition to ac losses in the metallization, the data shows that the substrate conductivity also introduces a significant degradation in the component Q. This demonstrates that the effect of the substrate conduction on the inductor Q-factor is significant at higher frequencies, but also that operation close to the ideal curve is obtained for frequencies below approximately 1.5 GHz. These results also indicate that inductors with a Q-factor of ten, which is suitable for many RF IC applications, could be fabricated in silicon production technologies if a low resistivity metal of adequate thickness were available.

C. Substrate Effects

The ability to predict the substrate effects on the inductor performance is key to the design and realization of inductors with acceptable performance in silicon technology. When substrate effects are properly accounted for in a circuit simulation, the inductor design can be optimized to minimize these losses and improve circuit performance. In production silicon technologies, an insulating oxide layer separates the top level metal and the semiconducting silicon wafer. The thickness of the oxide layer is an important parameter which influences the inductor performance. The measured effect of changes in the oxide thickness upon the component Q factor is illustrated in Fig. 9, for the 1.8 nH inductor discussed previously (refer to Fig. 8, metal thickness of 3 μm). A thicker oxide layer reduces the parasitic capacitance of the structure, which improves the inductor self-resonant frequency. This is seen in Fig. 9 as a broadening of the inductor Q-factor with frequency as the oxide thickness increases. Performance closer to that predicted for an ideal (i.e., nonconductive) substrate can be achieved when the oxide thickness is maximized.

The measured behavior of the 5 nH spiral inductor of Fig. 6 is shown in Fig. 10 for two different substrate conductivities (10 and 0.01 Ω-cm). A layer of aluminum 1 μm thick and 10 μm wide was used to fabricate the 4.5-turn spiral in both cases. At low frequencies, the real or resistive component of the impedance ($\mathrm{Re}[Z_1]$) is close to the dc resistance of the inductor, which is about 8.5 Ω. As the frequency increases, the resistive component increases, primarily due to dissipation in the conductive substrate. As seen in the figure, the dissipation of the inductor fabricated on a low resistivity substrate (0.01 Ω-cm) is substantially greater than for the substrate resistivity normally used in the BiCMOS process (10 Ω-cm). As a result, the peak Q-factor is reduced by a factor of two because of the increased dissipation, which makes the inductor unsuitable for most RF circuit applications.

In Fig. 10, the inductance, which is given by the reactive portion of the measured impedance ($\mathrm{Im}[Z_1]$) divided by the frequency, is 5 nH at low frequencies in each case. The effect of parasitic capacitance between the metal and substrate is larger when a highly doped substrate is used to fabricate the inductor, which leads to a lower self-resonant frequency. The reactance of the inductor fabricated on the 0.01 Ω-cm substrate rises to a peak at 4 GHz and then falls rapidly as the inductor approaches self-resonance. However, the low frequency inductance is unaffected. Current flow in the substrate beneath the spiral would cause negative mutual coupling and thus a reduction in the low frequency inductance of the spiral. These results indicate that the substrate current that is induced by the magnetic field is small.

VII. Component Tolerances

It is important to characterize the effects of processing and temperature variations upon the parameters of a monolithic component in order to estimate the yield of working circuits that meet the design specifications. Parameter variations due

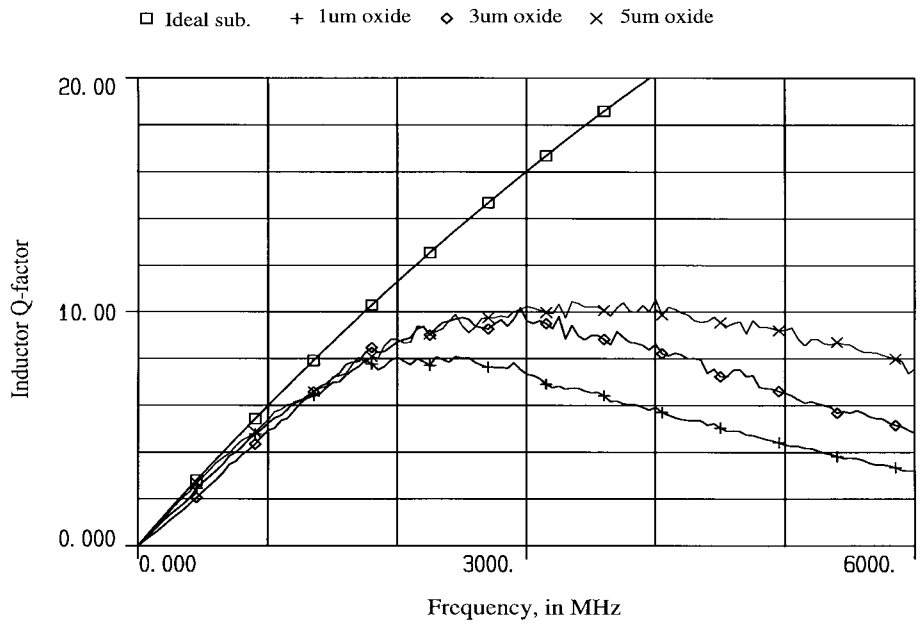


Fig. 9. Q-factor as a function of oxide thickness ($L = 1.8$ nH).

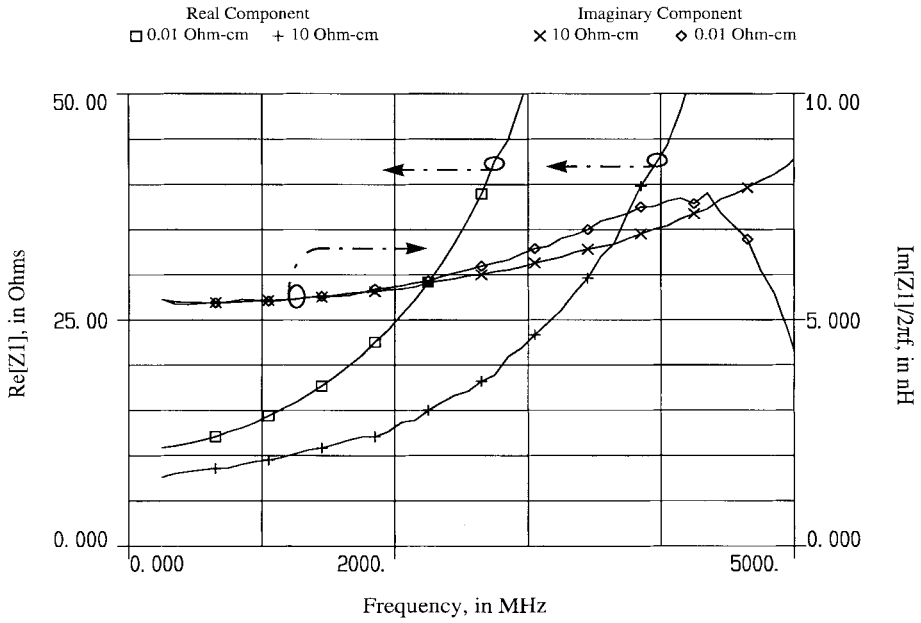


Fig. 10. Measured one-port impedance versus substrate resistivity ($L = 5$ nH).

to fluctuations in the ambient temperature should also be characterized and modeled so that circuit operation over a wide temperature range can be ensured during the design phase. Thus, the processing and temperature induced tolerances in the behavior of the monolithic inductor and transformer are of interest to the RF circuit designer.

The metal lines used in the inductor or transformer layout have dimensions on the order of microns, however, these dimensions are defined photolithographically to within one-tenth of a micron in a submicron IC process. The inductive reactance of a monolithic inductor is set by metal line width and line spacing, and thus the inductance is insensitive to the small lithographic variations in modern silicon IC processes. Simulations predict that the tolerance on the self and mutual inductances of the inductors described in this study will be less than 3% for a ± 0.2 μm change in the line width and line spacing. A larger and more subtle tolerance is introduced by variations in the intermetal oxide thickness and changes in substrate resistivity, both of which affect the parasitic capacitances of the inductor structure. However, simulations also predict that the variation in self-resonant frequency will be less than 5% for a ± 1 μm change in oxide thickness and a $\pm 50\%$ change in substrate resistivity from the nominal BiCMOS process parameters listed in Table I. These tolerances are far less

than those typically encountered for other passive monolithic components, such as resistors and capacitors.

Other sources of variation are the metallization and silicon substrate resistivities, both of which depend upon temperature. The aluminum–copper alloy typically used in silicon VLSI technologies (98% aluminum) has a temperature coefficient of +0.44%/°C [32], which can cause a large increase in the metal losses with increasing temperature. Other interconnect metals, such as gold, also exhibit a strong positive temperature coefficient (0.4%/°C). The shift in metal resistance with temperature directly affects the component quality factor [as seen from (3)], and it must be carefully considered in the design and optimization of an RF circuit.

The substrate resistivity also has a positive temperature coefficient, which is approximately +0.7%/°C [33]. As seen from (3), an increase in substrate resistivity with temperature can cause a degradation in the Q-factor at frequencies much less than the substrate corner frequency ($f_{sub} = 1/2\pi C_{ox} r_{\mathrm{Si}}$), and an improvement in Q-factor for frequencies higher than f_{sub}. Choosing to operate in a frequency band close to the peak Q reduces the effect (over temperature) of the substrate resistivity upon the inductor performance.

VIII. Inductor Design and Optimization

The design of a spiral inductor in silicon VLSI technologies involves a complex tradeoff between the various layout and technological parameters, as demonstrated by the experimental results presented in the previous section of this paper. The following set of guidelines or "design rules" summarize the results of this study.

1) Maintain a space of at least five line widths (i.e., $5W$, or further if possible) between the outer turn of the spiral and any surrounding metal features. Parasitic electric and magnetic coupling between conductors is inversely proportional to the separation. Maintaining sufficient space between the inductor and its surroundings will keep unwanted parasitic effects from disturbing the inductor's electrical characteristics.
2) The magnetic coupling between adjacent metal lines is maximized by using the closest spacing (S) between lines that is allowed by the technology. The additional interwinding capacitance from tighter coupling of the electric field between adjacent conductors has only a slight impact on performance, given that metal thickness in most VLSI technologies is usually less than 3 μm. Tight coupling of the magnetic field maximizes the Q-factor and reduces the chip area for a given inductor layout.
3) A strip width of between 10–15 μm is close to the optimum for most inductor designs fabricated with the technological parameters listed in Table I. Increasing the conductor width causes a downward shift in the peak Q-factor and also makes the Q-factor more sensitive to changes in operating frequency. This tradeoff requires extensive computer simulation in order to establish the optimum strip width for a given technology and inductance value.
4) Magnetic flux must be allowed to pass through the center of the spiral. This ensures that negative mutual coupling between opposite sides of the inductor does not significantly affect the inductance and the Q-factor. Thus, the four groups of coupled lines which form the sides of the inductor must be spaced sufficiently apart. Following the previous guideline, a space of greater than five line widths (i.e., $5W$) is recommended.
5) The oxide layer which isolates the metal conductors from the silicon substrate should be kept as thick as possible in order to minimize shunt parasitics and dissipation.
6) The inductor Q is most sensitive to the thickness and resistivity of the metal layer used in fabrication. Although the metal thickness is fixed in production technologies, metal layers in a multilevel metal process can be connected in parallel (metal stacking) to reduce Ohmic losses. This technique has demonstrated a 20% improvement in Q-factor when compared to inductors fabricated using only top metal [17] in some technologies. However, there is a tradeoff between the improvement in metal thickness and the reduction in oxide thickness as a result of metal stacking.

The results of this study have shown that a silicon technology with a substrate resistivity in the 10 Ω-cm range and a 5-μm thick oxide between metal and substrate can be used to fabricate inductors with acceptable Q-factors in the 1–3 GHz frequency range. The metallization thickness has a large effect upon the inductor quality factor, and a Q-factor of five is achievable with 1-μm thick aluminum top metal. However, a Q-factor of ten can be achieved if the metal thickness is increased to 3 μm.

A substantial improvement in inductor performance can also be realized through careful optimization of other aspects of the inductor layout using the lumped-element computer model. A plot of a Q-factor surface (at 1.9 GHz) that is defined by variations in the conductor width and the number of turns of the spiral is shown in Fig. 11. The substrate parameters for the BiCMOS technology given in Table I were used for the simulations, with a 1.5-μm line spacing. The points corresponding to an inductance of 5 nH are plotted onto the surface with an asterisk. These points indicate that an optimum geometry can be identified which maximizes the inductor Q-factor for a given inductance. The spiral geometry which yields the highest Q-factor at 1.9 GHz is also easily identified from this figure. The 3-D plot is a powerful design aid which can be used to visualize the effects of the many parameters which influence the inductor performance. A fast and efficient computer-based model is required in order to generate these types of design aids.

IX. Conclusions

A scalable lumped-element computer model has been described which adequately models the performance of inductors fabricated in a silicon VLSI process for a wide range of layout geometries. Both the measured and simulated results

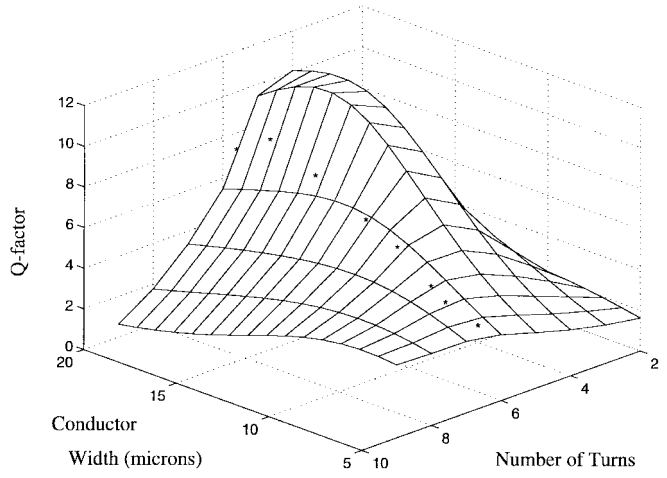


Fig. 11. Q-factor surface at 1.9 GHz.

indicate that the quality factor of the inductor is dominated by losses in the metallization at lower frequency and can be improved through the use of thicker metal in fabrication. Losses introduced by the conductive substrate tend to dominate performance at higher frequencies. However, these losses do not significantly degrade the performance in the low GHz frequency range, making these devices potentially useful in many RF IC applications. Substrate losses can be minimized by proper selection of the conductor width, spacing, and metal thickness for a given set of substrate parameters. The lumped element modeling approach is computationally efficient, fully scalable, and can be used to develop optimized inductor and transformer designs for various RF circuit applications.

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