A 53-62 GHz Two-channel Differential 6-bit Active Phase Shifter in 55-nm SiGe Technology

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***Abstract*— In this paper, a two-channel 6-bit active differential phase shifter is presented. A novel optimization technique is proposed to achieve accurate I/Q signals from the poly-phase filter, ultimately resulting in low gain and phase errors for the phase shifter. Unlike conventional matching methods between poly-phase filter and vector modulator, a capacitive loading is proved to reduce the sensitivity of phase error to impedance variation of the vector modulator. With the appropriate selection of circuit parameters for the poly-phase filter, reasonable phase and gain errors can be achieved without making any unnecessary modifications to the vector modulator. Using this technique, a two-channel phase shifter is fabricated in a 55-nm SiGe process. The peak differential gain of the phase shifter is around 2.6 dB. Moreover, in the frequency range of 53-62 GHz, both channels exhibit maximum gain and phase errors of 1.6 dB and 3.3°, respectively.**

***Keywords*— High-gain amplifier, phase shifter, vector modulator, phased array, 5G, mm-Wave.**

I. Introduction

With the emergence of 5G [1], and multi-user MIMO high-capacity wireless access [2], as well as the ever-growing need for car radars [3], phased-array techniques have become pervasive in the millimeter-wave band. The Phase shifters are the critical block in the phased-array systems to realize phase shift for the beam-steering mechanism. The phase and gain errors of phase shifters directly impact the beam-pointing precision and beam-steering resolution of the phased arrays, affecting the signal-to-noise ratio (SNR) at the receiver side. Therefore, optimizing the phase shifter block at millimeter-wave frequencies is crucial to ensure accurate phase and low-error gain phase shifters.

Phase shifters are generally categorized into two main classes: active and passive. Passive phase shifter topologies usually have significant insertion loss and occupy a massive area. In contrast, active phase shifters can be implemented using vector modulator topology [4], achieving high resolution and low loss in a compact area. Vector modulators (VM) require I/Q signals calling for an I/Q generator. The accuracy of the I/Q directly affects the phase and gain error of the phase shifter. I/Q accuracy is usually limited by the impedance variation of VM for different phase states. Recently, an impedance-invariant VM is reported [5] to tackle this problem. One of the main challenges of this approach is the increased loading, albeit invariant, from the vector modulator on the I/Q generator, which can lead to bandwidth limitations and other issues.

In this work, an optimization technique is proposed which determines the optimum impedance for the I/Q generator without altering the vector modulator. With this approach, I/Q accuracy is minimally affected by the vector modulator's impedance variation, resulting in a more robust design that is less susceptible to process variations. Using this technique, a well-optimized two-channel 6-bit active phase shifter is designed, operating from 53-62 GHz with a peak differential gain of 2.6 dB and maximum phase and gain errors below 3.3° and 1.6 dB, respectively. By avoiding unnecessary blocks and components in the design, chip area is significantly reduced, even below that of a single channel designs [5], [6], [7].

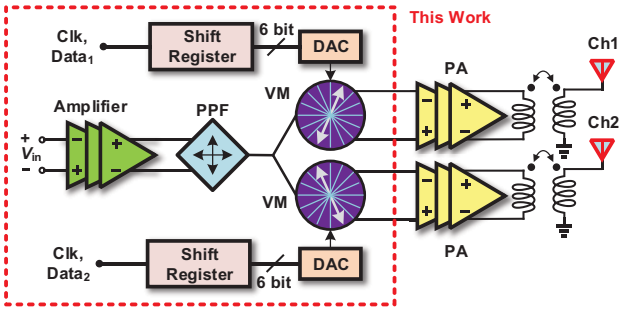

Fig. 1. Block diagram of the two-channel phased array transmitter.

II. Phase Shifter Architecture

The figure provided in Fig. 1 demonstrates the block diagram of a proposed two-channel phase shifter, which is an integral part of a two-channel phased-array transmitter. It is worth noting that the transmitter design of this work excludes the power amplifier (PA) since the PA can also affect the output constellation. To fully characterize the system before the PA, the output of the phase shifter is designed to be differential. The active phase shifter comprises a VM and a poly-phase filter (PPF). An R-C PPF topology is chosen to achieve wide bandwidth in a compact area at the cost of increased loss. Furthermore, a three-stage cascode amplifier is designed to compensate for the loss of PPF.

III. Amplifier Design

A three-stage cascode amplifier is designed to achieve high gain and stability. Given that PPF requires differential signals, either a differential amplifier or a single-ended one followed by a balun is required. However, an on-chip balun at 60 GHz tends to be very large, which increases the die area; hence a differential amplifier is chosen at the expense of higher power consumption. Fig. 2(a) demonstrates the amplifier circuit schematic. The input transistors are biased at

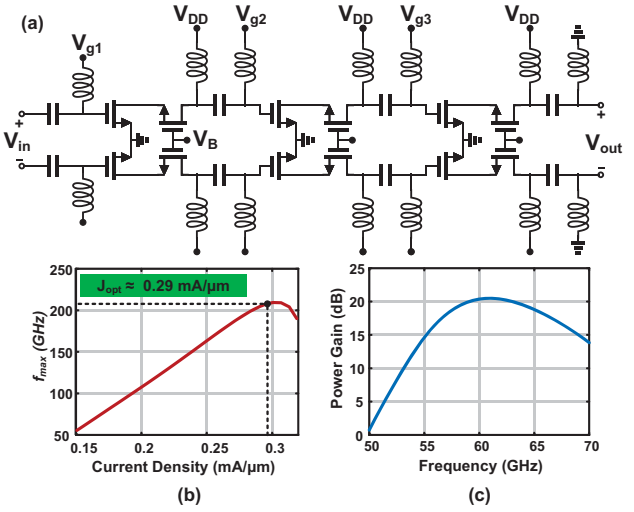

Fig. 2. (a) A three-stage cascode amplifier, (b) simulated f_{max} vs. current density of the cascode structure, (c) simulated transducer power gain of the amplifier.

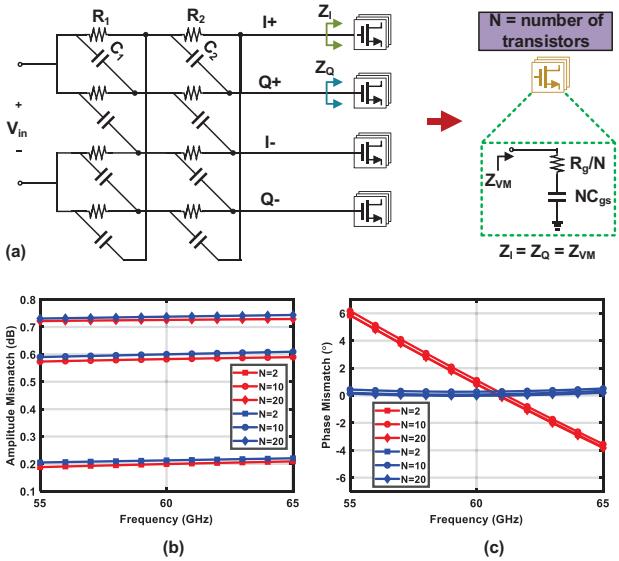

Fig. 3. (a) PPF schematic with loading effect from the VM, (b-c) amplitude and phase error of I/Q signals generated by PPF versus the number of transistors inside VM (red: one-stage, blue: two-stage).

the current density of 0.29 mA/μm to maximize their f_{max} and hence power gain as shown in Fig. 2(b). Wideband inter-stage matching is employed to attain large gain and bandwidth. Fig. 2(c) presents the simulated gain, demonstrating a gain of 21 dB with a 3-dB bandwidth of 10 GHz. Although transformers and large differential inductors can yield a slightly higher gain, they are avoided because they significantly increase the area of the chip.

IV. Poly-phase Filter Design

The amplifier is followed by PPF. To ensure small amplitude and phase errors across a wide bandwidth, a two-stage type-II R-C filter, as shown in Fig. 3(a), is chosen. In order to minimize the loss, two conditions must be satisfied [8]: 1. $\omega_1 > \omega_2$, 2. $k_c << 1$, where $\omega_1 = 1/R_1C_1$, $\omega_2 = 1/R_2C_2$, and $k_c = C_2/C_1$. However, these conditions can change if the load impedance variation from the following stage, VM, is considered [5]. This is primarily due to the bias-current variation of transistors inside the VM for different phase states, resulting in impedance variation. To address this issue, [5] suggests an impedance in-variant vector modulator that achieves different I and Q weightings by activating certain transistors in both I^+ and I^- paths as well as in Q^+ and Q^- paths. This approach ensures that the total number of transistors seen by each I^+/I^- and Q^+/Q^- path remains constant, resulting in a constant input impedance of the VM for different phase states. However, additional transistors must be employed for each path to compensate for the impedance variation, which can be cumbersome, especially if multiple channel phase shifters share one PPF. In such cases, the loading on the PPF increases exponentially with the number of channels, making it even more challenging to compensate for the impedance variation.

To investigate this phenomenon, Fig. 3(a) illustrates a two-stage PPF considering the loading effect from the transistors of the VM. The total loading from N parallel transistors is calculated as $R_g/N + 1/j\omega NC_{gs}$, which is equally seen by the I and Q paths. However, process variation can lead to different loading on each path, resulting in an unavoidable mismatch. Fig. 3(b-c) display the amplitude and phase error of the PPF when there is a 10% mismatch between the impedances seen from VM for I and Q paths, i.e., $Z_Q = 0.9Z_I$. The results demonstrate that increasing N results in a higher amplitude error for both one- and two-stage PPF, while the phase error remains relatively constant. This highlights the susceptibility of the in-variant impedance method to process variation, despite its ability to maintain a constant input impedance. The situation worsens for high-resolution multi-channel phase shifters, where more parallel transistors are required, making this approach extremely sensitive to process variations.

Here, the optimization of PPF and inter-stage matching is proposed to compensate for the impedance variation of the vector modulator. In designing a multi-channel phase shifter, there are two options for generating quadrature signals: (1) designing a separate PPF for each channel, and (2) designing a single PPF for all channels. The first approach is commonly employed in the design of multi-channel phased arrays [9]. Because of the process variation, the value of passive components inside the I/Q generators changes independently for each channel, resulting in a different phase and amplitude accuracy. Therefore, this work utilizes the second approach to design a two-channel phase shifter.

Based on the previous discussions, two-stage PPF is preferred over one-stage to minimize the phase error over a wide bandwidth. Assuming $Z_I = R_L + jQ_LR_L$, phase and amplitude errors are calculated and plotted for different values of R_L and Q_L for a starting point of [ω_1, ω_2, R_1, R_2] =

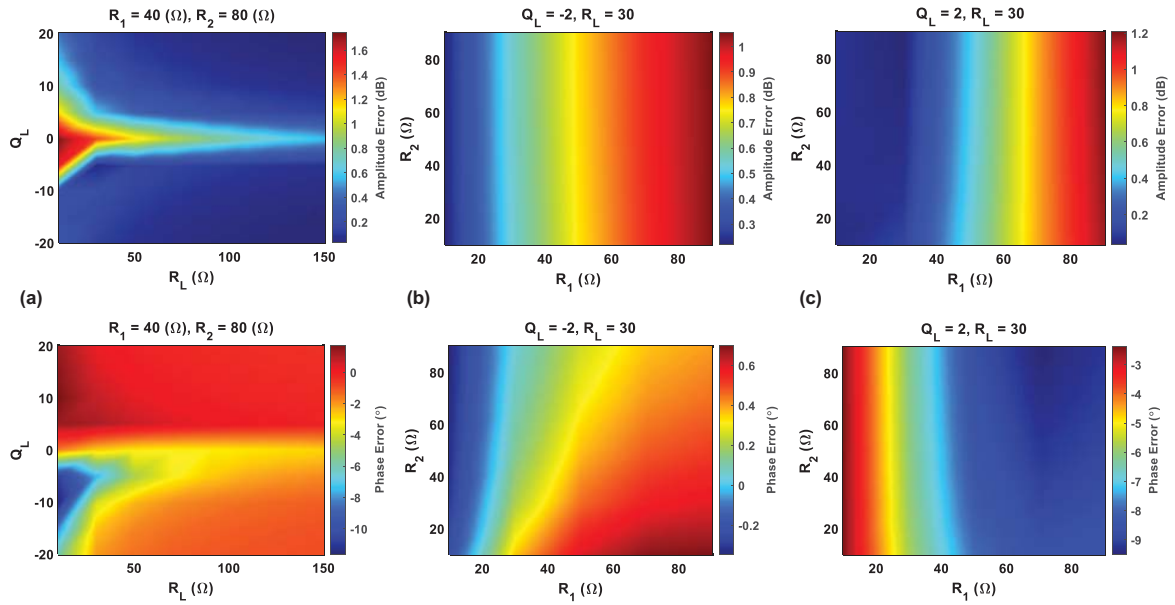

Fig. 4. (a) Effect of Q_L and R_L on the phase and amplitude error, peak amplitude and phase error vs. R_1 and R_2 assuming (b) capacitive ($Q_L < 0$) and (c) inductive ($Q_L > 0$) loading.

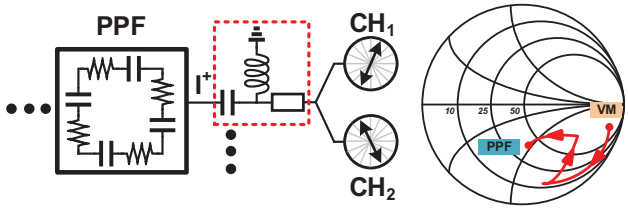

Fig. 5. Impedance matching network, which provides optimum impedance for PPF.

$[2\pi \times 50 \times 10^9, 2\pi \times 70 \times 10^9, 40, 80]$. From Fig. 4(a), $|Q_L|$ = 2 and R_L = 30 Ω are selected because phase and amplitude errors can be simultaneously minimized. It is noteworthy that large R_L values are impractical as the VM resistive part cannot be too large and hence are avoided in the iterations. Next, R_1 and R_2 are swept for the selected load impedance. Comparing Fig. 4(b) and (c), it is evident that the absolute value and variations of phase error are much less for capacitive loading than inductive loading. Additionally, based on Fig. 4(b), smaller R_1 values result in better phase and amplitude error while the effect of R_2 is minimal. However, reducing R_1 increases C_1 (for a constant ω_1) and limits the bandwidth of the amplifier. Therefore, R_1 = 56 Ω and R_2 = 76 Ω are selected in the final design after post-layout to reduce the PPF loading on the amplifier and also decrease the overall loss of PPF ($\sim 1/R_2$). In order to provide the optimum impedance for the PPF, as depicted in Fig. 5, an inductor is used in conjunction with a T-line and a capacitor to transfer the input impedance of VM to the proper load impedance for PPF (Q_L = -2, R_L = 30 Ω). The T-line is also useful for routing from PPF to each channel of the VM.

Lastly, a conventional topology for the vector modulator [4] is selected for each channel. Each vector modulator is biased at a total current of 9 mA to ensure stability for both common and differential modes and also achieve larger bandwidth. The vector modulator phase is controlled by an 8-bit digital-to-analog converter (DAC) similar to [4] with a current of 80 μA for the LSB transistor. Since a phase resolution of 5.6 ° (6 bits) is required for the phase shifter, an 8-bit DAC design gives more degrees of freedom to select the proper 64 phase states.

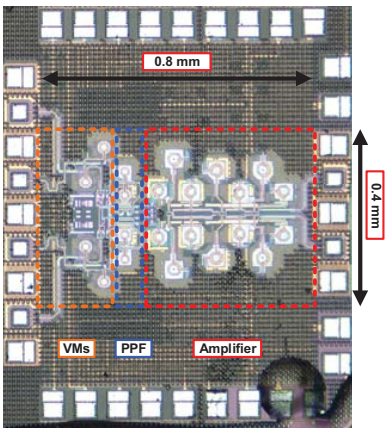

Fig. 6. Chip Micrograph.

V. Measurement Results

The phase shifter is fabricated using MOS transistors in the STMicroelectronics 55-nm SiGe process. Fig. 6 displays the chip micrograph of the two-channel phase shifter occupying an area of 0.32 mm^2, excluding the pads. The chip with two channels consumes 79 mA from a 1.5 V supply. Furthermore, the chip is calibrated with an on-wafer probe calibration substrate, and an Agilent 4-port precision network analyzer

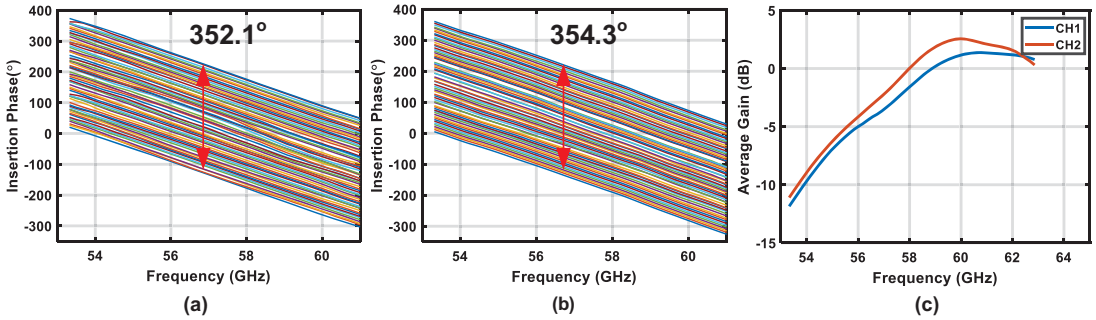

Fig. 7. Measured phase response of (a) channel 1 and (b) channel 2, (c) measured average gain of both channels.

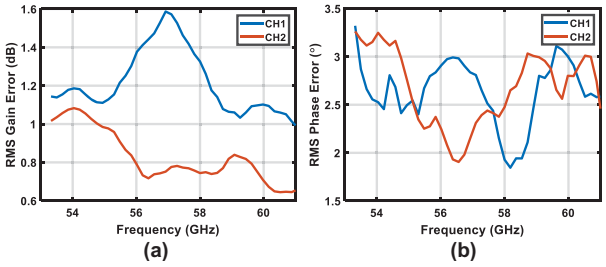

Fig. 8. RMS phase and gain errors of channel 1 and 2.

(PNA) is employed to characterize the phase shifter. The measured insertion phase for channels 1 and 2 for all phase states are presented in Fig. 7(a-b), where both channels demonstrate similar performance with phase coverage of $352.1°$ and $354.3°$, respectively. The average gain of all states for the two channels is also plotted in Fig. 7(c). The phase shifter achieves a maximum differential gain of 1.4 and 2.6 dB corresponding to channels 1 and 2. Fig. 8(a-b) illustrate the root mean squared (RMS) error of gain and phase of channels 1 and 2. The phase shifter achieves maximum phase and gain errors of $3.3°$ and 1.6 dB from 53-62 GHz for both channels, respectively. The RMS phase errors become large, close to the band limits, due to difficulty in differential calibration and limited phase stability of the cables.

Table 1 compares the performance of our chip to the state-of-the-art phase shifters in this frequency band. Compared to [6] and [10], our work achieves a much higher figure-of-merit (FOM). Moreover, compared to [5], our design achieves a comparable FOM and a much smaller area, considering two channels without any gain control units.

VI. Conclusion

This paper presents a dual-channel differential 6-bit active phase shifter that is well-optimized for use in highly accurate mm-wave phased-array systems for communications and ranging applications. The phase shifter features an R-C poly-phase filter and vector modulator, which are preceded by a three-stage amplifier for further amplification. The proposed technique minimizes the loading-mismatch effect of the vector modulator (VM) on the I and Q signals, leading to low phase and gain errors without requiring any modification to the VM. To reduce the sensitivity of the phase shifter to process variation, the design shares a single poly-phase filter for the two channels of VM. The resulting phase shifter offers high accuracy and is well-suited for use in mm-wave phased arrays.

Table 1. Comparison Table

Reference	This work	[5]	[6]	[10]
Process	55-nm SiGe	65-nm CMOS	40-nm CMOS	55-nm CMOS
Method	**VM (2-Ch)**	VM (1-Ch)	Hybrid (1-Ch)	VM (1-Ch)
Peak Gain (dB)	2.6	6.2	-9	-4.2
BW (GHz)	53-62	55-65	52-57	55-65
Phase Error (°)	1.8-3.3	1.17-2.01	2.8-3.76	< 2.5
Gain Error (dB)	0.6-1.6	0.16-0.29	2-2.2	< 0.5
Resolution (bit)	**6**	4	6	6
P^*_{dc} (mW)	59	25.2	14.3	16
Area (mm^2)	**0.32**	0.38	0.32	NA
FOM (dB)	**66.5**	67.5	41	58.4

FOM = $20\log_{10}(\frac{\text{Gain (linear)}\times\text{BW (GHz)}\times f_0\text{(GHz)}\times\text{Bits}\times Nch}{\text{Phase error (°)}\times\text{Gain error (linear)}})$, *Per channel

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