A 17-33GHz 6-bit Vector-Sum Phase Shifter with Wideband All-Pass I/Q Generator using an LC Compensation Network in 28-nm CMOS

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***Abstract*—This paper presents an enhanced wideband all-pass I/Q generator using an LC compensation network, which mitigates the impact of the loading capacitance of Gilbert vector summer in a wideband phase shifter. A 17-33 GHz 6-bit vector-sum phase shifter (VSPS) is designed and implemented in 28-nm CMOS technology, which achieves a maximum average insertion loss of 2dB, <0.5dB root means square (RMS) gain error, and 0.2~1.65° RMS phase error over the operation bandwidth. The power consumption of the VSPS is 12mW with a core size of 0.16 mm².**

***Index Terms*—phase shifter, all-pass I/Q generator, LC compensation**

I. Introduction

With the ever-increasing demand for 5G millimeter wave communication on high data rate, transceivers are continuously evolving towards the millimeter-wave frequency band. However, the millimeter-wave frequency band suffers from high path loss. To address this challenge, phased array transceivers have emerged as a promising technology to mitigate the issue in millimeter-wave communication [1]–[3]. The phase shifter is a key component in phased-array transceivers. Based on the operating mechanism, phase shifters can normally be classified into two types, namely passive ones and active ones. Passive phase shifters offer the benefits of high linearity and near-zero power consumption but also suffer from high insertion loss [4-5]. The active ones, which typically adopt vector-sum topology, exhibit higher gain, lower RMS phase error, and smaller chip size than the passive counterparts. As shown in Fig. 1, it is composed of a quadrature (I/Q) generator and a vector-summer based on the Gilbert structure.

Various techniques have been employed to design the quadrature generator as one of the most significant elements in the active phase shifts, including RC polyphase filters (PPF) [6], couplers [7], and quadrature all-pass filters (QAF) [8-10]. Although the RC PPF presents low phase and amplitude imbalance, its large insertion loss (IL) and narrow bandwidth (BW) make it less favorable for wideband mmW applications. The classical QAF can achieve better broadband performance and lower IL. However, its amplitude and phase characteristics are sensitive to the capacitive loading effect from the following vector summer, reducing the BW of the phase shifter [8]. To overcome this issue and achieve larger BW, resistors can be added to the QAF, but resulting in higher IL [9]. Another wideband QAF using a pair of serial inductors and resistors is reported in [10]. It achieves good performance in terms of bandwidth, phase, and gain errors. However, it still suffers from IL deterioration due to the additional resistors.

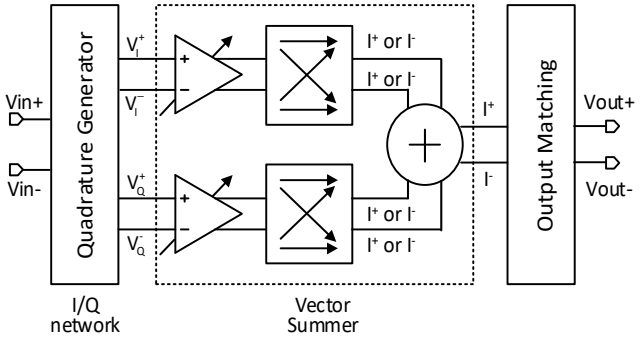

Fig. 1. The basic structure of a VSPS.

In this paper, to alleviate the impact of the loading capacitance from the Gilbert vector summer, an improved wideband all-pass I/Q generator using an LC compensation network is proposed for a wideband phase shifter. A 6-bit VSPS in 28-nm CMOS adopting the proposed QAF is designed, which exhibits 0.5dB RMS gain error and 0.2~1.65° RMS phase error over 17~33 GHz. The maximum average IL is less than 2dB.

II. Circuit Design

Fig. 1 shows the architecture of the wideband VSPS. It consists of an I/Q network based on the proposed QAF with an LC compensation network and Gilbert sector summer with wideband output matching, as shown in Fig. 2 (c) and (d).

A. Wideband All-pass I/Q generator

The traditional QAF is shown in Fig. 2(a). It consists of two inductors, two capacitors, and two resistors. The phase difference and amplitude imbalance are impacted by the capacitive load of Gilbert vector summer. The improved QAF is designed based on the traditional QAF, as presented in Fig. 2(b). The pair of serial resistors R_1 and inductors L_1 (highlighted in blue) in the diagram are designed parallel to C_L. The proposed wideband all-pass filter with an LC compensation network, which includes a pair of inductor L_2 and capacitor C_2, is shown in Fig. 2(c). The performance of three QAF designs in terms of voltage gain, amplitude imbalance, and phase difference is simulated, as illustrated in Fig. 3(a)-(c), where

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R=200Ω, and C_L=40fF. The improved QAF features an additional resistor, resulting in a lower voltage gain compared to the other two designs. However, the resistor can decrease the *Q* factor to enhance the bandwidth of the I/Q network. Besides, it exhibits excellent performance with respect to amplitude imbalance and phase difference from 20 to 35GHz. The proposed QAF circuit, under the same conditions, demonstrates better voltage gain than the other variants. Moreover, it also can realize good performance in terms of amplitude imbalance and phase difference between 20 to 35GHz, thanks to the added LC compensation network that effectively absorbs capacitive loads induced by Gilbert vector-summer. To achieve a compact chip size and improved differential performance, inductors L1 and L2 are designed as differential transformers, as shown in Fig. 3(d). Compared to the traditional QAF, the proposed QAF has demonstrated better performance in terms of amplitude imbalance and phase difference over a wide range of frequencies.

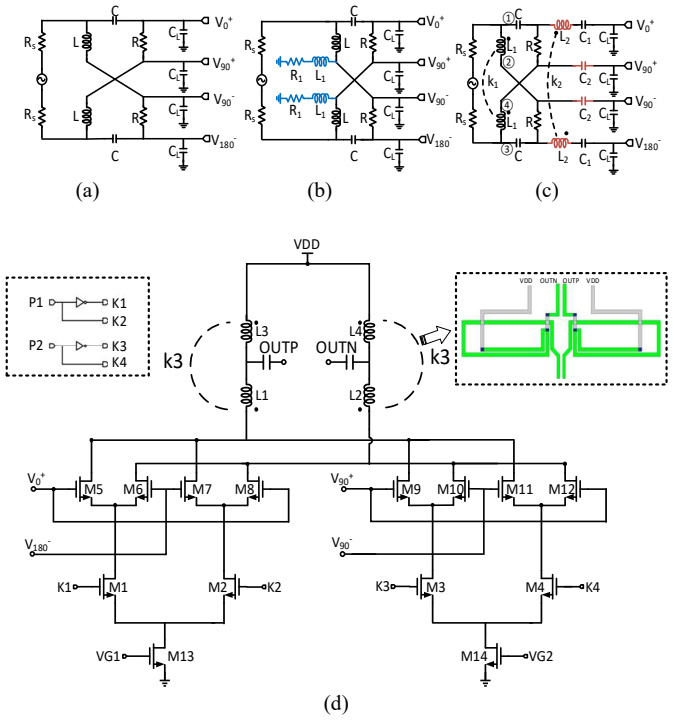

Fig. 2. The schematics of (a) the traditional QAF. (b) the improved wideband QAF with a pair of serial inductors and resistors [10]. (c) the proposed QAF with LC compensation network, and (d) the Gilbert vector summer.

B. Gilbert Vector Summer with Wideband Output Matching

Gilbert structure is used to construct the vector summer, as shown in Fig. 2(d). The transistors M1, M2, M3, and M4 are designed as switches for quadrant selection in the phase shifter. M13 and M14 provide phase control through VG1 and VG2. The output matching transformer with multi-resonant characteristics, which includes inductors L1, L2, L3, and L4, is designed to broaden BW while keeping a compact transformer size.

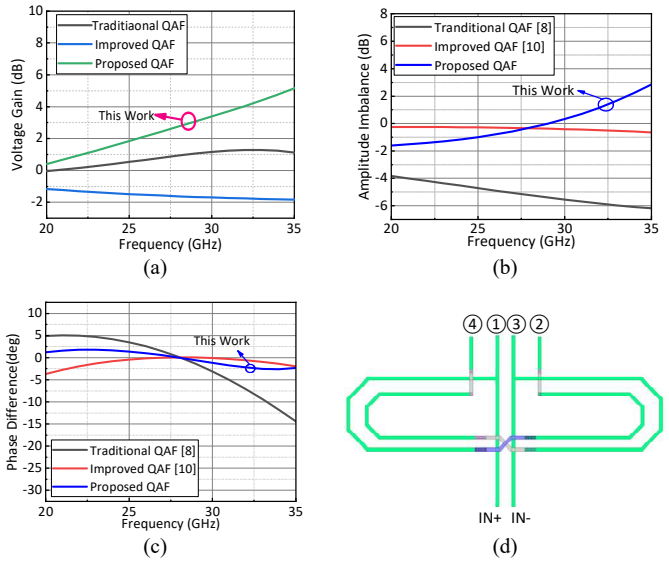

Fig. 3. The simulated (a) voltage gains. (b) amplitude imbalance and (c) phase differences of traditional, improved, and proposed QAF. (d) The layout of the input differential transformer in the proposed QAF.

III. Simulation Results of The Proposed VSPS

A 6-bit vector-sum phase shifter adopting the proposed QAF is designed using a TSMC 28nm process. Its overall layout occupies 590μm×570μm with a core size of 400μm×400μm, as shown in Fig. 4.

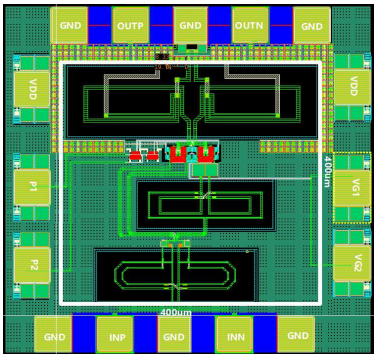

Fig. 4. Layout of the proposed 6-bit VSPS.

With a 0.9V voltage supply, the phase shifter is designed to consume 12mW dc power. Fig. 5 depicts the simulation results. QAF's amplitude imbalance is controlled to within 1dB, and the phase difference is less than 2 degree between 20 and 35GHz. Moreover, the simulated S11 magnitude is below -8dB, and the output return loss is greater than 10dB over the whole band. The phase shifter exhibits a maximum S21 of -2dB and a 3-dB bandwidth ranging from 18 to 37GHz (Fig. 5(d)). Furthermore, the phase shifter achieves 0.2~1.6° RMS phase error and 0.25~0.75dB RMS gain error from 17 to 33GHz, as illustrated in Fig. 5(f). Table I summarizes the performance of the proposed phase shifter and compares with prior arts.

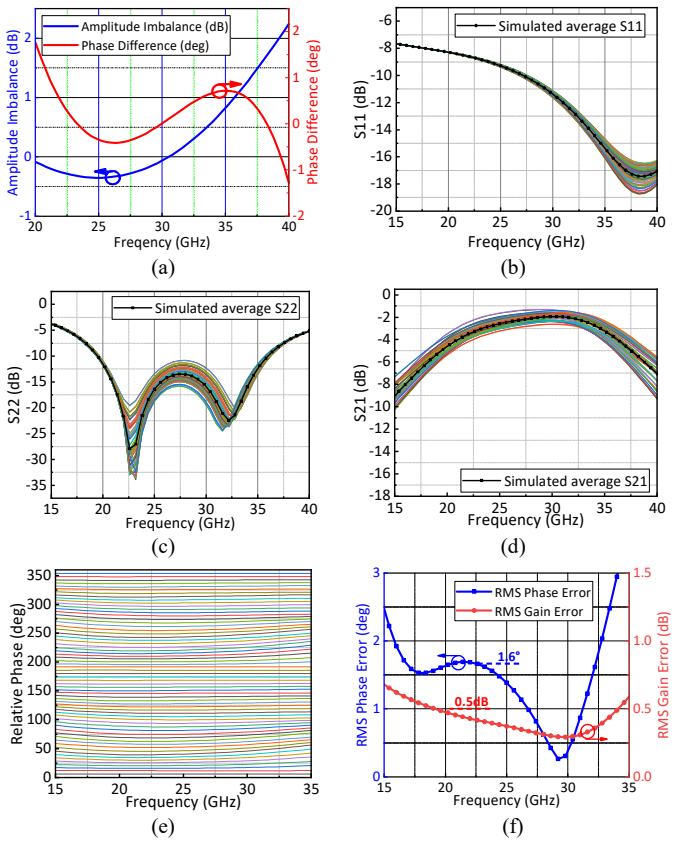

Fig. 5. (a) The amplitude imbalance and phase difference of QAF with LC compensation network. The simulation results of the proposed phase shifter: (b) S11, (c) S22, and (d) S21 magnitude for all 64 states. (e) Relative phase (0~360°) for all 64 states. (f) RMS phase error and RMS gain error.

TABLE I
SUMMARY OF TYPOGRAPHICAL SETTINGS

Ref.	JSSC 2007 [8]	TMTT 2012 [9]	TCAS2 2021 [10]	This Work
Technology	0.13 um CMOS	0.13um BiCMOS	65nm CMOS	**28nm CMOS**
Frequency (GHz)	15~26	55~80	15-38	**20~33**
Phase Resolution (deg)	11.25	22.5	5.625	**5.625**
RMS Phase Error (deg)	2.8~5.6	9.1	2~3.5	**0.2-1.65**
Gain (dB)	-4.6~-3	-	-4.7~ -1.7	**-2dB**
RMS Gain Error (dB)	1.1~2.1	1.3	0.7~1	**0.25~0. 5**
Power Consumption (mW)	11.7	34.8	19.2	**12**
Chip Size (mm^2) w/o pads	0.15	-	0.16	**0.16**

IV. CONCLUSION

A 6-bit vector-sum phase shifter using the proposed QAF has been designed using the TSMC 28nm process. The proposed design incorporates a QAF with an LC compensation network to achieve wideband performance while mitigating the impact of the load effect. The phase shifter demonstrates high precision in phase maintenance and low gain error over a large bandwidth. This makes it an excellent choice for 5G millimeter-wave applications.

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