Design and Analysis of a 21–29-GHz Ultra-Wideband Receiver Front-End in 0.18-μm CMOS Technology

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***Abstract*—This paper reports the design and analysis of 21–29-GHz CMOS low-noise amplifier (LNA), balun and mixer in a standard 0.18-μm CMOS process for ultra-wideband automotive radar systems. To verify the proposed LNA, balun, and mixer architectures, a simplified receiver front-end comprising an LNA, a double-balanced Gilbert-cell-based mixer, and two Marchand baluns was implemented. The wideband Marchand baluns can convert the single RF and local oscillator (LO) signals to nearly perfect differential signals over the 21–29-GHz band. The performance of the mixer is improved with the current-bleeding technique and a parallel resonant inductor at the differential outputs of the RF transconductance stage. Over the 21–29-GHz band, the receiver front-end exhibits excellent noise figure of 4.6 $\pm$ 0.5 dB, conversion gain of 23.7 $\pm$ 1.4 dB, RF port reflection coefficient lower than -8.8 dB, LO-IF isolation lower than -47 dB, LO-RF isolation lower than -55 dB, and RF-IF isolation lower than -35.5 dB. The circuit occupies a chip area of 1.25×1.06 mm^2, including the test pads. The dc power dissipation is only 39.2 mW.**

***Index Terms*—Balun, Gilbert-cell mixer, low-noise amplifier (LNA), low power, port-to-port isolation, receiver front-end.**

I. Introduction

RECENTLY, ultra-wideband (UWB) technology has attracted a lot of academic and industrial interests. In 2002, the Federal Communications Commission (FCC), Washington, DC, regulated the 22–29-GHz band for the UWB automotive radar system applications [1]. In 2005, the European Conference of Postal and Telecommunications Administrations (CEPT) released bandwidth of 5 GHz, from 21.65 to 26.65 GHz, for the UWB short-range radar applications to fulfill the requirement of range resolution of a few centimeters [2]. An UWB receiver front-end is a critical block in UWB transceiver design. To amplify and down-convert the small radio signals received from the whole UWB band with a good signal-to-noise ratio (SNR) property, in addition to flat and high S_{21}, flat and low noise figure (NF) is also required. Besides, for pulsed radar systems, good phase linearity is required in order to keep the shape of the pulse when receiving RF signals from an antenna. There are some reports of CMOS narrowband receiver front-ends designed for frequencies around 24 GHz [3]–[8], but only a few for CMOS wideband receiver front-ends for 21.65–26.65- or 22–29-GHz UWB short-range radar applications [9], [10].

In this paper, we present a 21–29 GHz (covering both the 21.65–26.65- and 22–29-GHz band of interest) CMOS UWB receiver front-end with flat and high conversion gain (CG) and flat and low NF [11]. The receiver front-end comprises a low-noise amplifier (LNA), a mixer, and two Marchand baluns. The wideband Marchand baluns can convert the single RF and local oscillator (LO) signals to nearly perfect differential signals over 21–29 GHz. In this work, we do not adopt the complicated sub-harmonic mixer (SHM) [12], whose LO input frequency is about half of the RF input frequency to mitigate the dc-offset problem. Instead, we propose a high-performance double-balanced Gilbert-cell-based mixer using the current-bleeding technique and a parallel resonant inductor at the differential outputs of the RF transconductance stage. In addition, instead of the complicated quadrature voltage-controlled oscillator (QVCO) for differential in-phase/quadrature (I/Q) LO signal generation needed in an SHM, a simple single LO signal generator in conjunction with a quadrature coupler (QC) is used in the proposed receiver architecture. This paper is organized as follows. In Section II, the receiver architecture is described. The design and analysis of the LNA, Marchand balun, and mixer are introduced in Section III. In Section IV, we discuss the measurement results of the CMOS receiver front-end and make comparisons with previous work. Section V presents a conclusion.

II. Receiver Architecture

The basic requirements of a short-range radar system include high dynamic range, close-range detection, and high-range resolution [9], [10], [13]–[19]. In CMOS technology, the generation of a wideband low phase-noise chirp is challenging since normally a complex frequency synthesizer is needed. This makes the frequency-chirped radar normally unsuitable for short-range radar applications. The pseudorandom noise (PN) coded radar is resilient to interferers, but normally suffers from a relatively low dynamic range (i.e., limited range) [18]. Compared with the frequency-chirped and PN-coded radar, the key difference of the pulse radar is a better isolation between its transmitter and receiver, especially with a single antenna. This is because its transmitter and receiver are operated in a time-duplex mode. In addition, generally speaking, the complexity of the pulse radar is relatively lower [10]. These advantages make the pulse radar very suitable for UWB 21.65–26.65-, 22–29-, and 76–81-GHz millimeter-wave short-range radars.

Manuscript received February 19, 2012; accepted March 13, 2012. Date of publication June 01, 2012; date of current version July 30, 2012. This work was supported by the National Science Council of the R.O.C. under Contract NSC100-222-E-260-011-MY3 and Contract NSC100-2221-E-260-006-MY2.

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Digital Object Identifier 10.1109/TMTT.2012.2198234

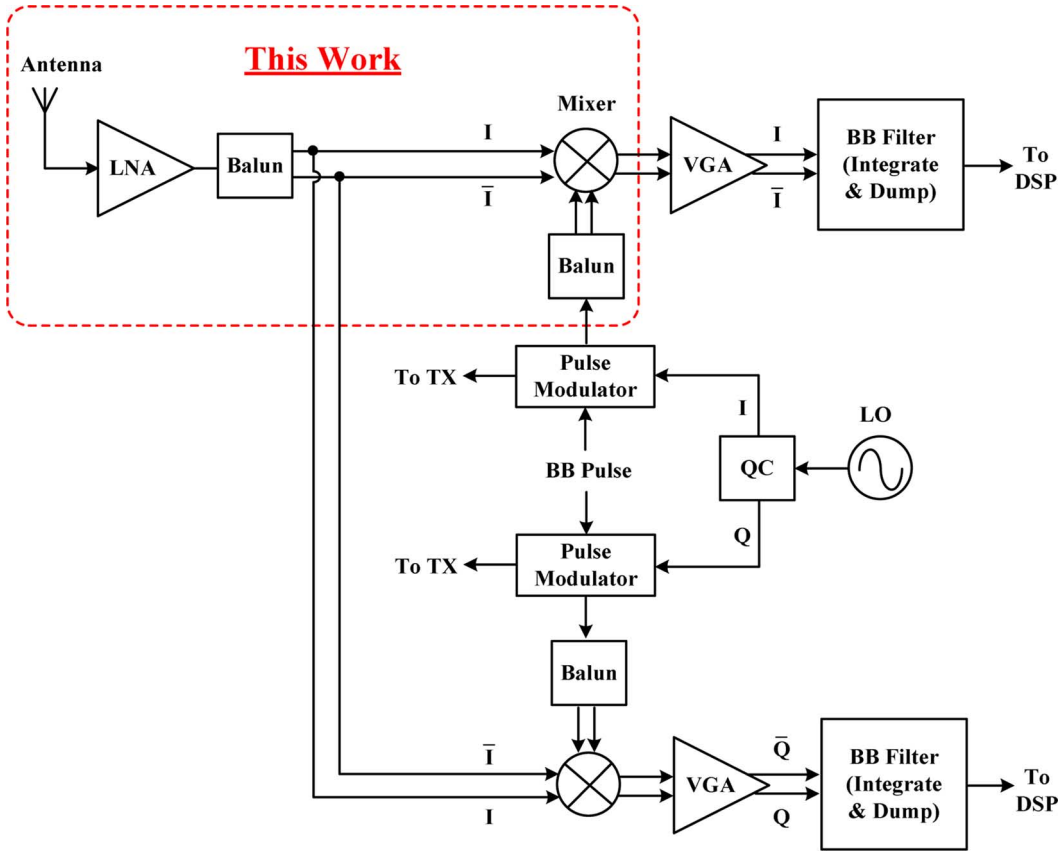


Fig. 1. Block diagram of a typical UWB pulse-radar receiver.

Fig. 1 shows the block diagram of a typical pulse-radar receiver for UWB automotive radar systems. The receiver comprises a 21–29-GHz UWB LNA, two 21–29-GHz UWB mixers, three 21–29-GHz Marchand baluns, two baseband variable-gain amplifiers (VGAs), two baseband filters, two pulse modulators, a QC, and an LO signal generator. The function of the UWB LNA is to amplify the received modulated pulses with small magnitude and phase distortion. Thus, the basic requirements of the LNA include flat and high S_{21}, flat and low NF, and good phase linearity (i.e., small group-delay variation). The baseband pulse signals are up-converted to the automotive radar band by the pulse modulators through the modulation of the 24.15 GHz (for 21.65–26.65-GHz radar sensors) or 25.5 GHz (for 22–29-GHz radar sensors) LO signals. The locally generated modulated pulses from the pulse modulator are delayed reproductions of the transmitted ones. The UWB I/Q mixers correlate them with the amplified received modulated pulses. The cross-correlation products are amplified by the VGAs, and then become dc-coupled outputs by integration in the baseband filters [18]. The purpose of this work is to verify the proposed LNA, balun and mixer architectures are suitable for 21–29-GHz automotive radar systems so only one mixer is included for simplicity. The QC, pulse modulator, baseband VGA and filter, and LO signal generator are being developed as a sequel of this work.

III. Receiver Front-End Design

The 0.18-μm 1P6M CMOS process (with substrate resistivity of 8–12 $\Omega \cdot$cm) provided by the commercial foundry TSMC was adopted to design and implement the 21–29-GHz receiver front-end. The interconnection lines, as well as the coils of the baluns, were implemented by the 2.34-μm-thick topmost metal (M_6) to minimize the resistive loss. The design of the LNA, balun, and mixer of the receiver front-end is introduced as follows.

A. LNA Design

Fig. 2 shows the schematic of the LNA with the important device parameters labeled. The LNA is composed of a common-source stage followed by a cascoded stage. The equivalent Miller capacitance of C_{gd2} (gate–drain capacitance of transistor M_2) at the gate and drain terminal of transistor M_2 can be parallelly resonated by inductor L_{g2} and L_1, respectively. This, in turn, results in a low S_{12} (or excellent stability) because the reverse signal flow is suppressed. All transistors (M_1, M_2, and M_3) have the same gate length of 0.18 μm. The gatewidth per finger of M_1, M_2, and M_3 is 4.6, 3, and 4 μm, respectively. The finger number of M_1, M_2, and M_3 is 10, 16, and 27, respectively. The reason why different finger widths (and total gatewidths) are chosen for M_1–M_3 is as follows. First, to achieve flat and low NF over the 21–29-GHz band, M_1 adopts the size (i.e., 4.6 μm $\times$ 10) and bias ($V_G = 0.7$ V) that corresponds to the optimum minimum NF ($\mathrm{NF}_{\min}$) and maximum oscillation frequency ($f_{\max}$) performance. Second, the signal level at the second stage is significantly larger. Thus, a relatively wider gatewidth is adopted for M_2 and M_3 to achieve better power and phase linearity performance. Finally, the finger widths and total gatewidths of M_2 and M_3 are finely

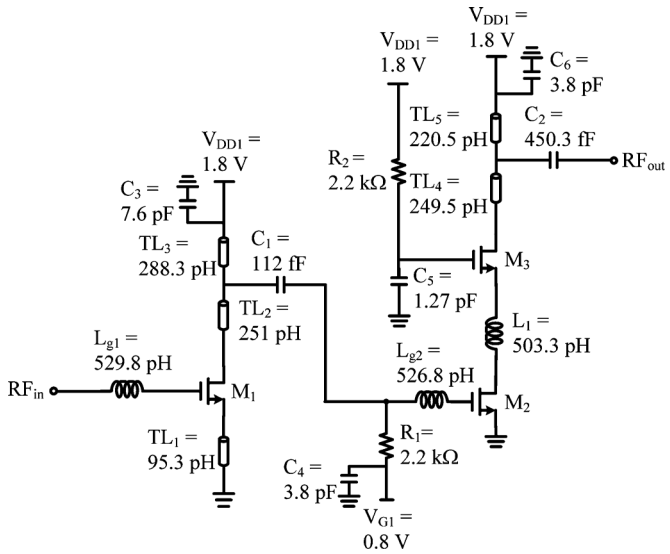


Fig. 2. Schematic of the LNA.

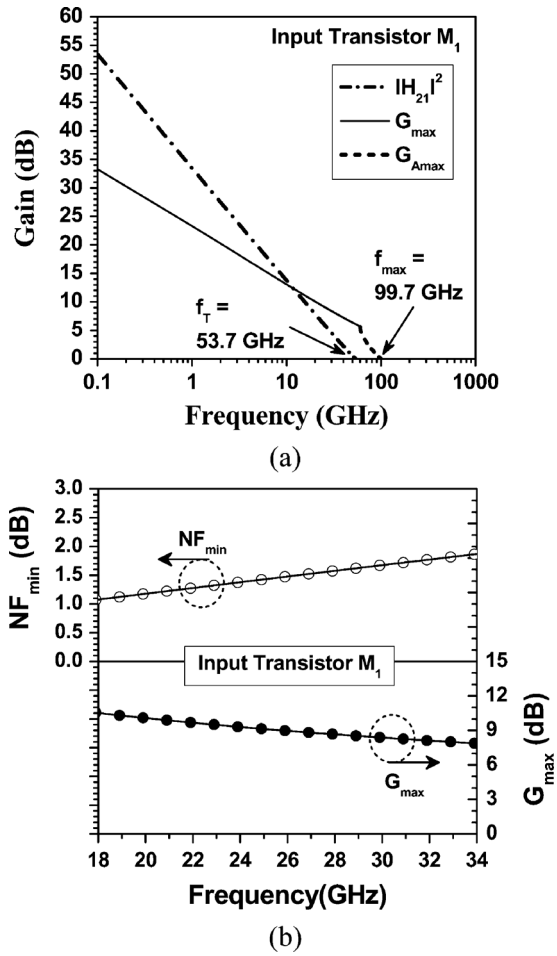


Fig. 3. Simulated: (a) $|H_{21}|^2$ and $G_{\max}/G_{A\max}$ versus frequency characteristics and (b) $\mathrm{NF}_{\min}$ and $G_{\max}$ versus frequency characteristics of the input transistor M_1.

tuned for performance optimization. This, in turn, results in different finger widths (and total gatewidths) being chosen for M_1–M_3. Simulated results show the LNA achieves input 1-dB compression point $(P_{1\,\mathrm{dB}})$ better than -15 dBm and group-delay variation smaller than ± 15 ps for frequencies 21–29 GHz.

Compared with the two-stage CMOS LNA with a third-order Cauer bandpass filter (BPF) matching network at the input for UWB input impedance-matching in [9] and [10], this work exhibits better performances. This is because the adoption of the BPF at the input requires a number of additional reactive elements (four, i.e., C_1, L_1, C_2, and L_2 in [9] and [10]), which inevitably results in larger die size and higher NF (due to the finite quality factor (Q factor) of the reactive elements).

In addition, note that the two-stage LNA is different from the four-stage 21–27-GHz LNA reported in [20]. The main difference is the current-reused second and third stages in [20] are not included in this work. Instead, a parallel-peaking inductor TL_2 is added to the input stage, and a series-peaking inductor L_{g2} and a parallel-peaking inductor TL_4 are added to the output stage. To optimize the NF frequency response over the 21–29-GHz band, the input transistor M_1 adopts the size and bias that correspond to the best $\mathrm{NF}_{\min}/f_{\max}$ performance. A slightly under-damped Q factor for the NF frequency response is achieved based on the derived analytical equations, which will be introduced later. This, in turn, results in a comparable gain (14.22 ± 0.65 dB versus 14.89 ± 1.14 dB), a lower power consumption (15.2 mW versus 27 mW), and a better NF (3.08 ± 0.14 dB versus 3.87 ± 0.47 dB) for frequencies 21–27 GHz.

Fig. 3(a) shows the simulated square of the short-circuit current gain $|H_{21}|^2$, maximum stable power gain $(G_{\max})$, and maximum available power gain $(G_{A\max})$ versus frequency characteristics of the input transistor M_1. The current-gain cutoff frequency f_T is defined as the frequency corresponding to $|H_{21}| = 1$ (i.e., 0 dB), while $f_{\max}$ is defined as the frequency corresponding to $G_{A\max} = 1$. As can be seen, the simulated f_T and $f_{\max}$ are 53.7 and 99.7 GHz, respectively. The result is reasonable since it is close to our previous measured result ($f_T = 64$ GHz and $f_{\max} = 79$ GHz) of an NMOSFET with different gatewidth (i.e., not optimized for $\mathrm{NF}_{\min}/f_{\max}$), but fabricated in the same technology [21]. The good f_T and $f_{\max}$ performance of the transistors indicates that it is possible to apply this CMOS process on the implementation of high-performance 21–29-GHz LNA and receiver front-end.

Fig. 3(b) shows the simulated $\mathrm{NF}_{\min}$ and $G_{\max}$ versus frequency characteristics of the input transistor M_1. Over the frequencies of 21–29 GHz, the input transistor M_1 achieves low $\mathrm{NF}_{\min}$ of 1.23–1.63 dB, and high $G_{\max}$ of 9.87–8.52 dB. The high $G_{\max}$ indicates that it is reasonable to approximate the NF of the receiver front-end by the NF of the first-stage of the LNA.

Fig. 4 shows the simulated S-parameters versus frequency characteristics of the LNA. Flat and high S_{21} of 13.7 ± 1.2 dB and flat and low S_{12} of -35.48 ± 1.51 dB are achieved over the frequency range of 21–29 GHz. The excellent S_{21} and S_{12} performances are partly due to the introduction of the parallel-peaking inductor L_1.

In addition, S_{11} is lower than -8.7 dB for frequencies 20.5–31.3 GHz, and S_{22} is lower than -10 dB for frequencies 20.6–29 GHz. The wideband input impedance matching is

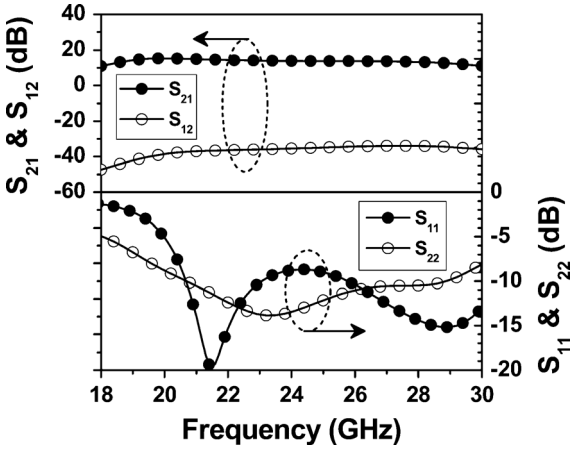


Fig. 4. Simulated S-parameters versus frequency characteristics of the LNA.

mainly attributed to the two intrinsic S_{11} dips (at 21.5 and 28.9 GHz), which will be explained shortly.

Fig. 5(a) shows the equivalent circuit for calculating S_{11} of the LNA. Note that there are two *RLC* impedance branches $Z_{\rm in1}$ and $Z_{\rm in2}$ in parallel. For frequencies around the lower corner frequency (21 GHz), $Z_{\rm in1}$ is the dominant one (i.e., $Z_{\rm in1} < Z_{\rm in2}$). The input network can be simplified to the series *RLC* network shown in Fig. 5(b). Thus, there is a dip in S_{11} at frequency around

$$f_{01} \approx \frac{1}{2\pi\sqrt{[C_{\rm gd1}(1+g_{m1}R_{o1})]\left[L_{g1}+\frac{C_{\rm gs2}(TL_2+L_{g2})}{C_{\rm gd1}(1+g_{m1}R_{o1})}\right]}} \tag{1}$$

in which R_{o1} is the output resistance of the input transistor $\rm M_1$. According to (1), the calculated f_{01} is 20.6 GHz, close to the simulated one (21.5 GHz) in Fig. 4. In addition, for frequencies around the upper corner frequency (29 GHz), $Z_{\rm in2}$ is the dominant one (i.e., $Z_{\rm in2} < Z_{\rm in1}$). The input network can be simplified to the series *RLC* network shown in Fig. 5(c). Thus, there is another dip in S_{11} at frequency around

$$f_{02} \approx 1/(2\pi\sqrt{C_{\rm gs1}(L_{\rm g1}+TL_1)}) \tag{2}$$

According to (2), the calculated f_{02} is 29.35 GHz, close to the simulated one (28.9 GHz) in Fig. 4.

Fig. 6(a) shows the simulated S_{11} versus frequency characteristics of the LNA at various L_{g2} values. As can be seen, f_{01} increases with the decrease of L_{g2}, consistent with (1). Fig. 6(b) shows the simulated S_{11} versus frequency characteristics of the LNA at various L_{g1} values. As can be seen, f_{02} increases with the decrease of L_{g1}, consistent with (2).

The inductive-peaking technique is used in the output of each stage so that the output of each stage is equivalently loaded with a bandpass combination of L (with an equivalent series resistance R) and C to provide a low-Q (wideband) parallel resonance at a frequency within the 21–29-GHz band. In addition, inductor L_1 in the second stage resonates with the parasitic capacitance at the drain terminal of $\rm M_2$ and the source terminal of $\rm M_3$, which leads to a gain peaking at frequencies around 29 GHz. In conjunction with the gain peaking of L_{g2} and C_{gs2} at frequencies around 21 GHz, the gain degradation of the first stage at high frequencies can be compensated. This is the method to achieve flat and high S_{21} and good phase linearity property.

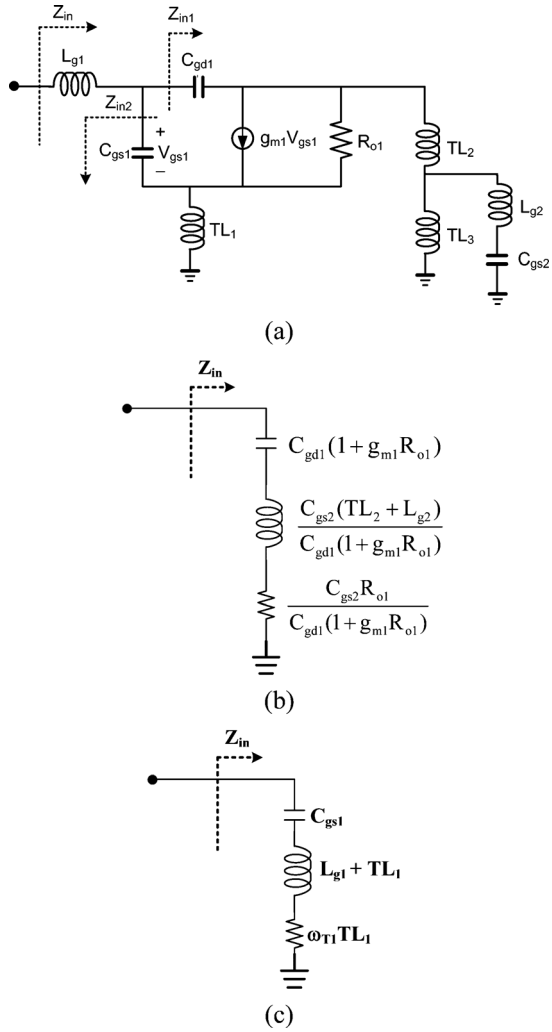


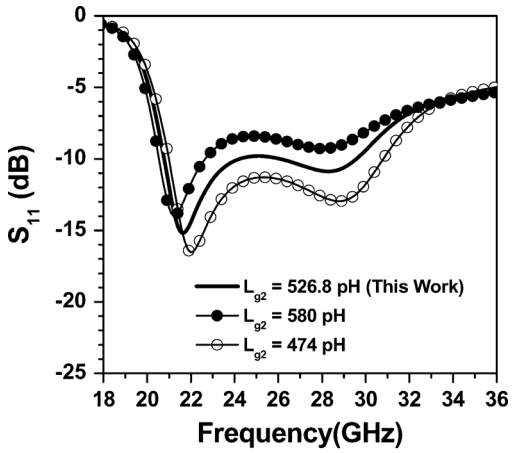
Fig. 5. Input equivalent circuit of the LNA for S_{11} calculation. (a) Complete circuit and simplified circuit at frequencies around (b) lower corner frequency and (c) upper corner frequency.

The stability parameter $\mu(S)$ and its dual parameter $\mu'(S)$ are defined as follows [22]:

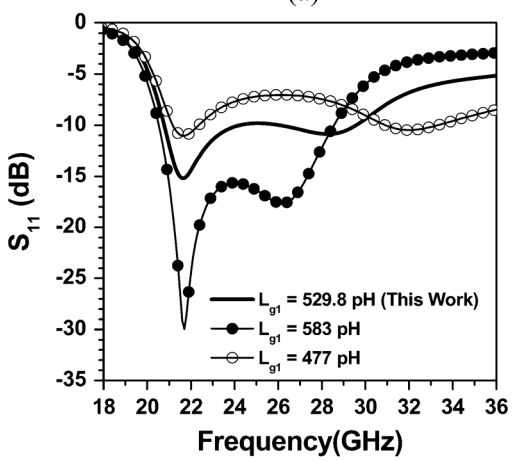
$$\mu(S) = \frac{1-|S_{11}|^2}{|S_{22}-S_{11}^*\Delta|+|S_{21}S_{12}|} \tag{3}$$

$$\mu'(S) = \frac{1-|S_{22}|^2}{|S_{11}-S_{22}^*\Delta|+|S_{21}S_{12}|} \tag{4}$$

in which $\Delta = S_{11}S_{22}-S_{12}S_{21}$. It has been shown that $\mu(S) > 1$ (or $\mu'(S) > 1$) alone is necessary and sufficient for a circuit to be unconditionally stable. Fig. 7 shows the simulated stability parameters $\mu(S)$ and $\mu'(S)$ versus frequency characteristics of the LNA. As can be seen, the LNA is unconditionally stable from dc to 50 GHz. The good stability of the LNA is partly attributed to its two-stage structure, which is intrinsically stable [23]. What is also shown in Fig. 7 is the simulated results at fast–fast (FF) corner (i.e., the devices with minimal possible



(a)



(b)

Fig. 6. Simulated S_{11} versus frequency characteristics of the LNA: (a) at various L_{g2} values and (b) at various L_{g1} values.

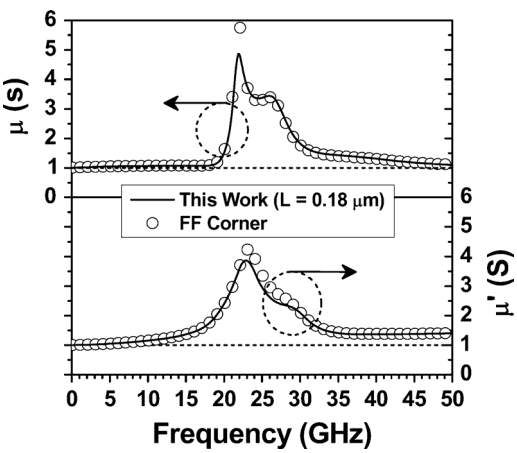


Fig. 7. Simulated stability parameters $\mu(S)$ and $\mu'(S)$ versus frequency characteristics of the LNA.

gate length due to process variation). The LNA is still unconditionally stable from dc to 50 GHz. This result indicates that this technique is scalable to shorter channel technologies.

In wideband applications, flat and low-NF frequency response is also required in addition to wideband input impedance matching and flat and high-gain frequency response. Traditional low-noise design based on optimum NF at each frequency is not suitable for wideband design because the resulting NF frequency response is not flat. In order to achieve flat NF response, the factors that control the shape of NF frequency response must be derived first. Fig. 8 shows the equivalent circuit of the LNA in Fig. 2 for its NF calculation. The noise factor F of the LNA ($\mathrm{NF} = 10 \cdot \log_{10} F$) can be expressed as follows [24]:

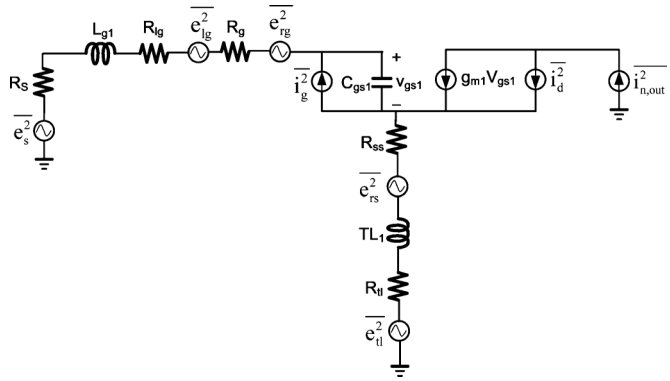


Fig. 8. Equivalent circuit of the LNA for noise calculation.

$$
\begin{aligned}
F_{\mathrm{LNA}} &\approx 1 + \frac{R_g + R_{lg} + R_{ss} + R_{ls}}{R_S} \\
&\quad + \frac{\delta\alpha\omega^2 C_{\mathrm{gs1}}^2}{5 g_{m1} R_S} \cdot \left(R_S^2 + \omega^2 L_{g1}^2\right) \\
&\quad + \frac{\gamma (L_{g1} + TL_1)^2 C_{\mathrm{gs1}}^2}{\alpha R_S g_{m1}} \\
&\quad \cdot \left| s^2 + s\left(\frac{\omega_{0,\mathrm{dn}}}{Q_{\mathrm{dn}}}\right) + \omega_{0,\mathrm{dn}}^2 \right|^2 \\
&\equiv 1 + \frac{R_g + R_{lg} + R_{ss} + R_{ls}}{R_S} + F_{\mathrm{gn}} + F_{\mathrm{dn}} \qquad (5)
\end{aligned}
$$

where

$$
\omega_{0,\mathrm{dn}} = \frac{1}{\sqrt{(L_{g1} + TL_1) C_{\mathrm{gs1}}}} \qquad (6)
$$

$$
Q_{\mathrm{dn}} = \frac{1}{R_S + \omega_{T1} TL_1} \cdot \sqrt{\frac{L_{g1} + TL_1}{C_{\mathrm{gs1}}}} \qquad (7)
$$

F_{gn} and F_{dn} represent the corresponding noise factor contributions of gate noise and drain noise to the LNA, respectively. In this work, F_{dn} is larger than F_{gn} over the 21–29-GHz band. α (the ratio of g_{m1} to zero-bias drain conductance g_{d0}) of 0.85 is normally adopted for the NF calculation [25], [26]. Since the NF [see (5)] has been put in the form of a second-order function of s, its frequency response is well known and controlled by quality factor Q_{dn}. That is, flat and low NF can be achieved if the values of L_{g1}, TL_1, and the size and bias of the input transistor M_1, i.e., C_{gs1} and g_{m1}, are selected appropriately to make Q_{dn} of the derived second-order NF frequency response slightly greater than 0.707, i.e., slightly under-damped. Finally, the second stage is optimized for linearity. The LNA consumes

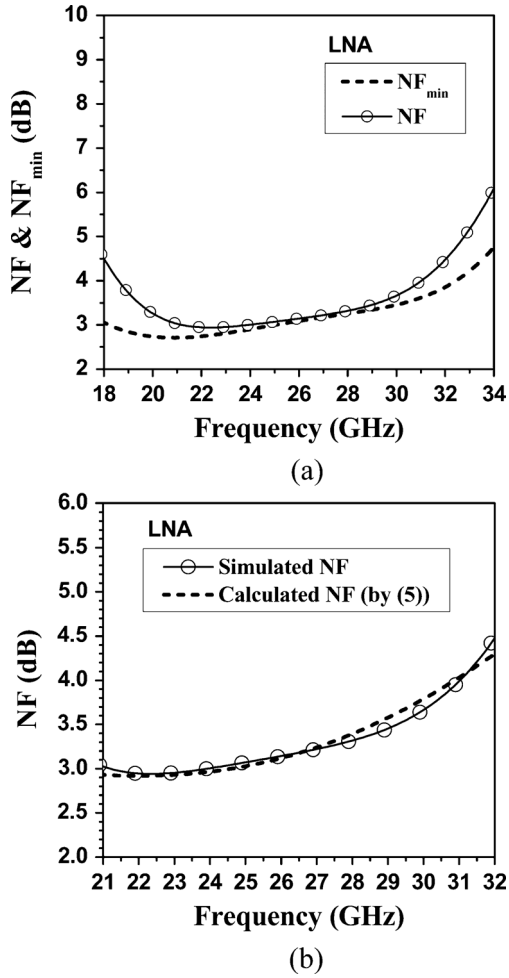


Fig. 9. (a) Simulated $\mathrm{NF_{min}}$ and NF. (b) Simulated and calculated NF versus frequency characteristics of the LNA.

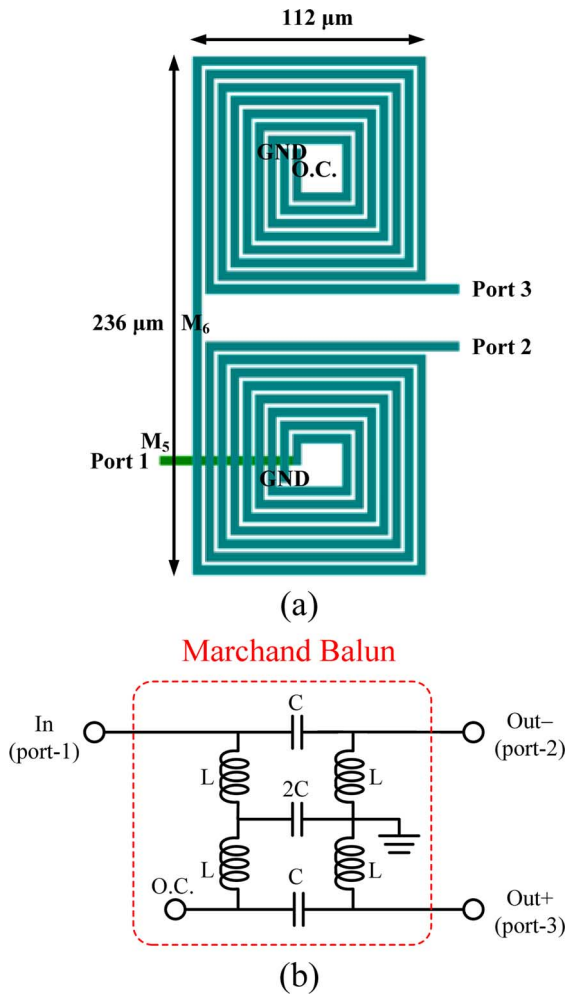


Fig. 10. (a) Schematic diagram and (b) lump-element equivalent circuit of the Marchand balun.

13 mW in the bias condition of $V_{DD1} = 1.8$ V, $V_{G1} = 0.8$ V, and $V_{\mathrm{RFin}} = 0.7$ V (by bias-T).

Fig. 9(a) shows the simulated $\mathrm{NF_{min}}$ and NF versus frequency characteristics of the LNA. Flat and low NF of 3.19 ± 0.25 dB is achieved over the frequencies of 21–29 GHz, close to that (3.02 ± 0.31 dB) of the simulated $\mathrm{NF_{min}}$.

Fig. 9(b) shows the simulated and calculated [by (5)] NF versus frequency characteristics of the LNA. To calculate the NF frequency response, C_{gs1} and g_{m1} of the input transistor $\mathrm{M_1}$ should be extracted first. According to the methodology introduced in [26], $C_{\mathrm{gs1}} = 47$ fF and $g_{m1} = 19$ mS are obtained. From (6), the calculated $\omega_{0,dn}/2\pi$ is equal to 29.36 GHz, a reasonable value since it is very close to the upper corner frequency (29 GHz) of the LNA. From (7), the calculated Q_{dn} is equal to 1.3, also a reasonable value since it means the frequency response of the dominant term F_{dn} of the NF expression is slightly under-damped, which, in turn, results in the NF frequency response being relatively flat and low. The result shows the calculated NF is 3.25 ± 0.28 dB for frequencies 21–29 GHz, close to that (3.19 ± 0.25 dB) of the simulated one.

B. Balun

The needed 21–29-GHz baluns were designed based on the "lumped-element" Marchand balun structure proposed in [27]. Such a balun structure is advantageous in terms of its excellent amplitude/phase match and broadband response compared with the traditional single-to-differential transformers [28], [29]. Instead of the area-consumed microstrip line (MSL) structure, the miniature spiral coil structure is adopted to implement the needed inductor elements in the baluns. Fig. 10(a) shows the schematic diagram of the Marchand balun. The metal width and space are 4 and 2 μm, respectively. The balun consists of an unbalanced input (port-1), an open terminal (O.C.), two short terminals (GND), and two balanced outputs (port-2 and port-3). Note that the coils of the balun are implemented by the 2.34-μm-thick topmost metal $(\mathrm{M_6})$ to minimize the resistive loss. Only the underpass interconnection line of port-1 is realized by $\mathrm{M_5}$.

Fig. 10(b) shows the lump-element balun equivalent circuit [27]. The spiral coil couple-line is modeled by the lump inductor L, and the capacitor C modeled the coupling capacitance effect, which is produced from the spiral coil couple line. That is, the capacitors are realized as the parasitic components of the inductors. Port-1 is the unbalanced RF (or LO) input port, and port-2 and port-3 are the balanced $\mathrm{RF-}$ and $\mathrm{RF+}$ (or $\mathrm{LO-}$ and $\mathrm{LO+}$) output ports, respectively. From the network's perspective, this lump-element balun can be regarded as an out-of-phase

power splitter, including a parallel-connected high-pass filter and a BPF. The signals through the output ports of the ideal balun have equal power, but are 180° out-of-phase; all ports (except the O.C. port) have an input impedance of 50 Ω (i.e., Z_0). Suppose

$$\frac{1}{\sqrt{LC}} = \omega_0 \tag{8}$$

in which ω_0 is the geometrical mean of 21 and 29 GHz. According to Fig. 10(b), the input admittance Y_{in} of the balun for frequencies around ω_0 can be represented as follows:

$$Y_{\text{in}} \approx \frac{1}{sL} + sC + \frac{2Z_0C}{L} \equiv \frac{1}{sL} + sC + Y \tag{9}$$

It is a common practice to choose $Y = Y_0(= 1/Z_0)$ in order to achieve excellent matching for frequencies around ω_0. According to (8) and (9), the ideal values of L and C are as follows:

$$L = \frac{\sqrt{2}Z_0}{\omega_0} \tag{10}$$

$$C = \frac{1}{\sqrt{2}Z_0\omega_0}. \tag{11}$$

In addition, according to (9), the input return loss S_{11} can be represented as follows:

$$S_{11} = \frac{Y_0 - Y_i}{Y_0 + Y_i} = -\frac{s^2LC - sL(Y_0 - Y) + 1}{s^2LC + sL(Y_0 + Y) + 1}. \tag{12}$$

By plugging $s = j\omega$ into (12) and assuming $Y = Y_0$, $|S_{11}|$ can be expressed as

$$|S_{11}| \approx \left|\frac{s^2 + \omega_0^2}{s^2 + s\frac{2Y_0}{C} + \omega_0^2}\right| \equiv \left|\frac{s^2 + \omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}\right|. \tag{13}$$

Now it is clear that $|S_{11}|$ is a standard notch function with -3-dB matching bandwidth $(\Delta f_{3\text{ dB}})$ equal to $\omega_0/(2\pi Q)$ (or Y_0/πC). In general, $|S_{11}|$ should be smaller than -10 dB over the band of interest, i.e.,

$$20\log|S_{11}| \le -10 \text{ dB}. \tag{14}$$

The corresponding matching bandwidth $\Delta f_{10\text{ dB}}$ is equal to

$$\Delta f_{10\text{ dB}} = \frac{\Delta f_{3\text{ dB}}}{3} = \frac{Y_0}{3\pi C} = \frac{1}{3Z_0\pi C} = \frac{2Z_0}{3\pi L}. \tag{15}$$

The equivalent inductance [i.e., L in Fig. 10(b)] and Q factor of a single spiral coil couple-line inductor of the balun in Fig. 10(a) can be obtained from the simulated Y-parameters (which can be transformed from the simulated S-parameters) by the following equations [30]:

$$L = \frac{\text{Im}(1/Y_{11})}{\omega} \tag{16}$$

$$Q = \frac{\text{Im}(1/Y_{11})}{\text{Re}(1/Y_{11})}. \tag{17}$$

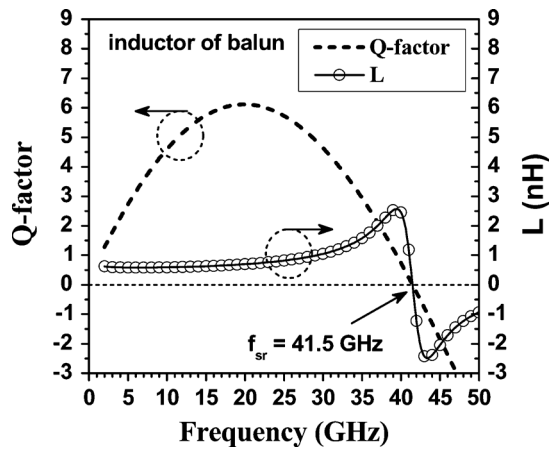


Fig. 11. Simulated L and Q factor of a single spiral coil couple-line inductor of the balun in Fig. 10(a).

Fig. 11 shows the simulated L and Q factor of a single spiral coil couple-line inductor of the balun. At 25 GHz, L is equal to 0.818 nH, and C is equal to 49.5 fF (not shown here). In addition, over the 21–29-GHz band, an L of 0.716–0.987 nH and a Q factor of 4.91–6.04 are obtained. The self-resonance frequency (f_{sr}), i.e., the frequency corresponding to $L = 0$ or $Q = 0$, is 41.5 GHz. That is, the structure is inductive for frequencies lower than 41.5 GHz, covering the 21–29 GHz of interest.

Fig. 12(a) shows the simulated and calculated S_{11} of the balun. The calculated result is consistent with the simulated one. The simulated S_{11} is equal to -14.8 dB at 24 GHz, and is smaller than -10 dB for frequencies 16.2–52 GHz. What is also shown in Fig. 12(a) is the simulated S_{21} and S_{31}. S_{21} is equal to -5.17 dB at 24 GHz, and is smaller than -5.37 dB for frequencies 21–29 GHz. In addition, S_{31} is equal to -5.15 dB at 24 GHz, and is smaller than -5.37 dB for frequencies 21–29 GHz.

Fig. 12(b) shows the simulated amplitude imbalance (AI) and phase difference (PD) versus frequency characteristics of the balun. AI between port-2 and port-3 is 0.02 dB at 24 GHz, and is smaller than 0.03 dB for frequencies 21–29 GHz. PD between port-2 and port-3 is 181.3° at 24 GHz, and is 181.3°–181.5° for frequencies 21–29 GHz.

The designed Marchand balun shows excellent robustness to process, voltage, and temperature (PVT) and modeling errors. For example, for a 5% variation of metal width and unchanged metal pitch (i.e., metal width plus metal space), the variation in S_{31} (or S_{21}), AI, and PD is slight, which are described in more detail as follows.

Fig. 13(a) shows the simulated S_{31} of the balun with various metal widths. Note that the metal pitch is kept the same, i.e., 6 μm. The simulated results for the case with a narrower metal width of 3.8 μm (i.e., -5.17 dB at 24 GHz, and smaller than -5.34 dB for frequencies 21–29 GHz) and the case with a wider metal width of 4.2 μm (i.e., -4.98 dB at 24 GHz, and smaller than -5.22 dB for frequencies 21–29 GHz) are close to that of this work (i.e., -5.15 dB at 24 GHz, and smaller than -5.37 dB for frequencies 21–29 GHz).

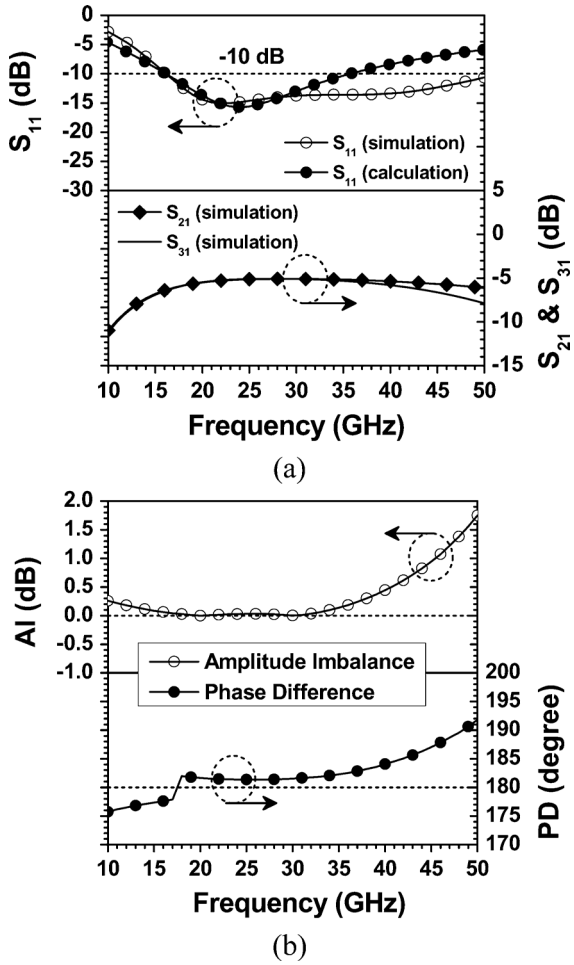


Fig. 12. (a) Simulated and calculated S_{11}, and simulated S_{21} and S_{31}. (b) AI and PD versus frequency characteristics of the Marchand balun.

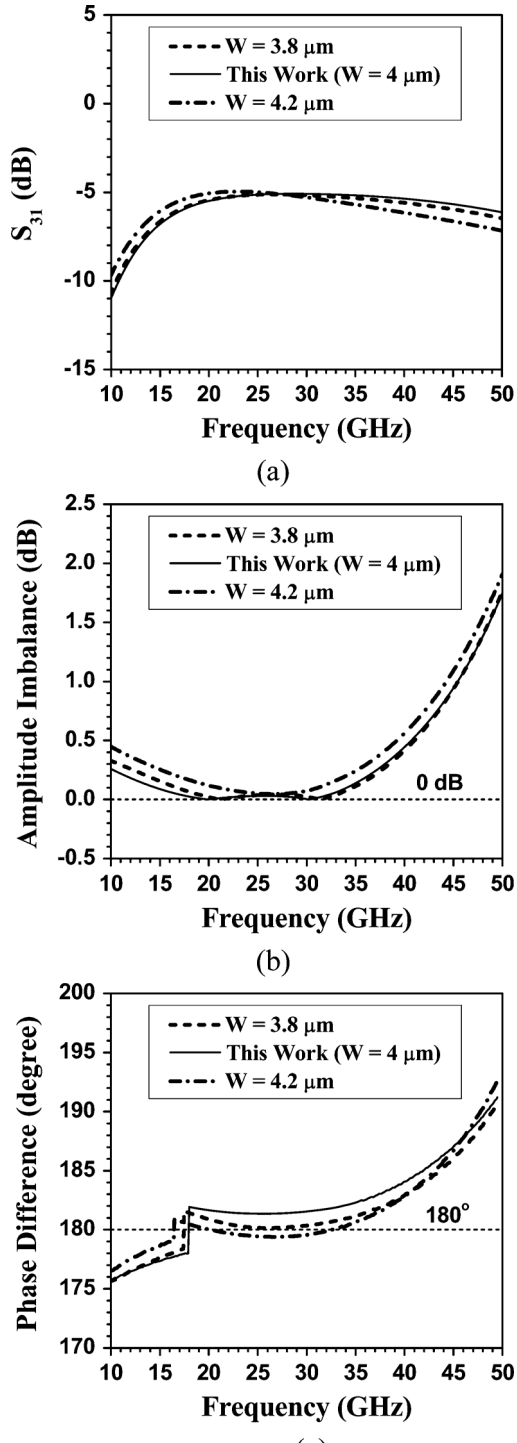


Fig. 13. Simulated: (a) S_{31}, (b) AI, and (c) PD versus frequency characteristics of the Marchand balun with various metal widths.

Fig. 13(b) shows the simulated AI between port-2 and port-3 of the balun with various metal widths. The simulated results for the case with a narrower metal width of 3.8 μm (i.e., 0.03 dB at 24 GHz, and smaller than 0.04 dB for frequencies 21–29 GHz) and the case with a wider metal width of 4.2 μm (i.e., 0.06 dB at 24 GHz, and smaller than 0.1 dB for frequencies 21–29 GHz) are close to that of this work (i.e., 0.02 dB at 24 GHz, and smaller than 0.03 dB for frequencies 21–29 GHz).

Fig. 13(c) shows the simulated PD between port-2 and port-3 of the balun with various metal widths. The simulated results for the case with a narrower metal width of 3.8 μm (180.23° at 24 GHz, and 180.15°–180.67° for frequencies 21–29 GHz) and the case with a wider metal width of 4.2 μm (179.51° at 24 GHz, and 179.4°–179.86° for frequencies 21–29 GHz) are close to that of this work (181.3° at 24 GHz, and 181.3°–181.5° for frequencies 21–29 GHz).

C. Mixer Design

Fig. 14 shows the schematic of the proposed Gilbert-cell-based double-balanced mixer with integrated RF- and LO-port baluns. The important device parameters are also labeled. The gain peaking inductor L_2 between the differential outputs of the RF transconductance stage can enhance the performances of the mixer, which will be discussed later. The wideband Marchand baluns can convert the single RF and LO signals to nearly perfect differential signals over the 21–29-GHz band. This topology is balanced for RF, LO, and IF signals so the corresponding isolations are better than those of a traditional single-balanced mixer [9], [10]. For example, compared with the corresponding receiver front-end with the traditional single-balanced mixer, simulated results demonstrate that an

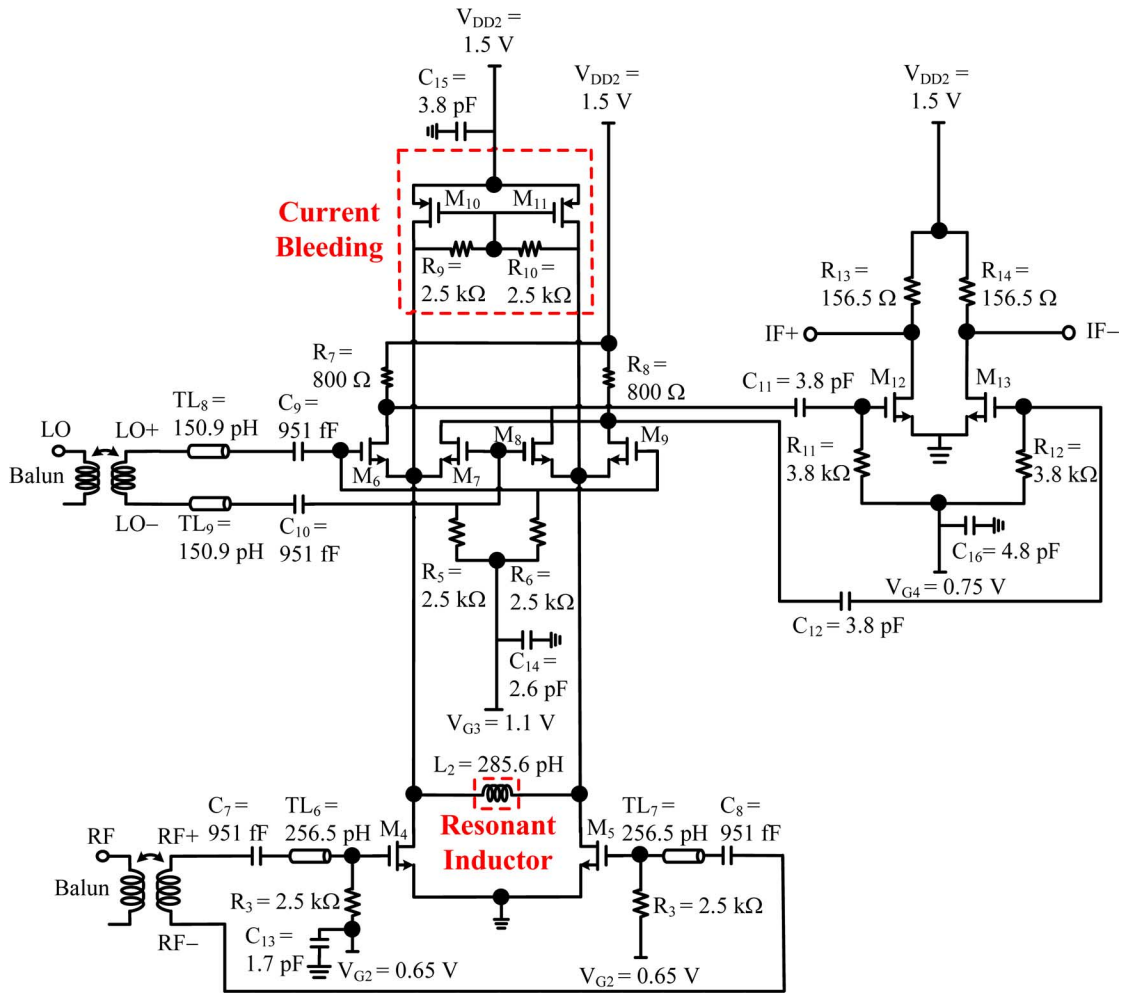


Fig. 14. Schematic of the mixer.

improvement of 17.74–18.28, 51.98–61.06, and 22.12–27.8 dB are achieved for RF-IF, LO-IF, and LO-RF isolation, respectively. All transistors (M_4–M_{11}) have the same gate length of 0.18 μm. The gatewidth per finger of M_4–M_9 and M_{10}–M_{13} is 5 and 4 μm, respectively. The finger number of M_4–M_9, M_{10}–M_{11} and M_{12}–M_{13} is 10, 9, and 25, respectively. The mixer consumes 24 mW in the bias condition of $V_{DD2} = 1.5$ V, $V_{G2} = 0.65$ V, $V_{G3} = 1.1$ V, and $V_{G4} = 0.75$ V.

The differential transconductance stage, which converts the differential RF input voltage signals (RF+ and RF−) to output current signals, is composed of nMOS transistors M_4 and M_5 biased in the saturation region. Based on the theory in [31], the input matching bandwidth is inversely proportional to the equivalent input series inductance L_s of the equivalent input series *RLC* network. The theoretical L_s corresponding to 8 GHz (21–29 GHz) of input matching bandwidth is 0.663 nH. However, in this work, a smaller inductance of 0.256 pH is selected for a larger design margin. The needed equivalent 50-Ω series resistance is mainly contributed by the parallel *RLC* load of transistors M_4/M_5 through the feedback capacitance C_{gd4}/C_{gd5}. Analytical expressions can be obtained according to the methodology introduced in [32]. Excellent RF-port input impedance matching can then be achieved if the values of TL_6–TL_7, C_7–C_8, L_2,and the size and bias of transistors M_4–M_5, i.e., C_{gs4}, C_{gs5}, C_{gd4}, C_{gd5}, g_{m4}, and g_{m5} are selected appropriately to make the equivalent input series *RLC* network resonant at around the center frequency (25 GHz) and has an equivalent input series resistance R_s of about 50 Ω. The LO switching quad consists of nMOS transistors M_6–M_9, which are biased in the near pinch-off region to act as switches. In order to minimize the noise of the mixer, the bias current of the LO switching quad should be small enough. Therefore, a current supplying circuit (based on the current bleeding technique), composed of pMOS transistors M_{10}–M_{11} and resistors R_9–R_{10}, is incorporated to provide most of the needed drain current of the RF transconductance stage such that the bias current of the LO switching quad could be largely reduced. Furthermore, since a relatively larger load resistance can be adopted, a higher CG can be achieved [33].

The single-stage differential IF amplifier comprises transistors M_{12}–M_{13} and load resistors R_{13}–R_{14} provides additional gain to compensate the loss caused by the passive components. The resonant inductor L_2 can parallelly resonate with the parasitic capacitance at the drain terminals of transistors M_4–M_5 and M_{10}–M_{11}, and the parasitic capacitance at the source terminals of transistors M_6–M_9. This leads to not only an enhancement of

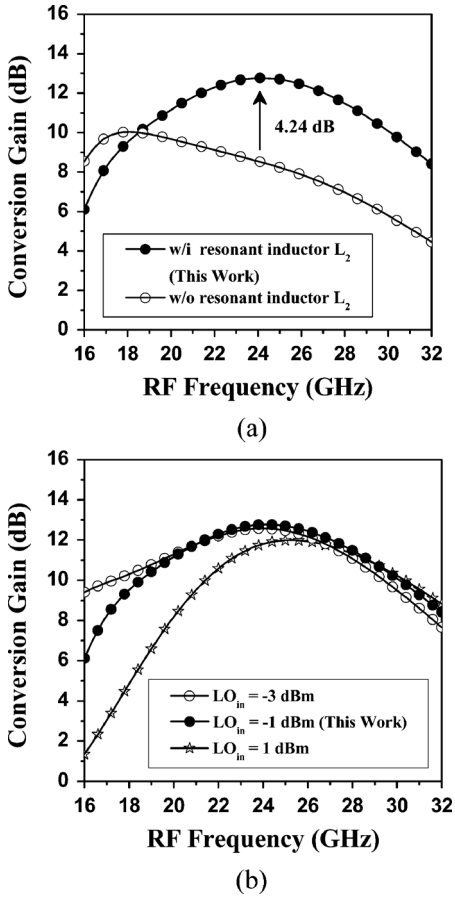


Fig. 15. Simulated CG versus RF frequency characteristics of the mixer: (a) with and without the resonant inductor L_2 and (b) at various LO input power.

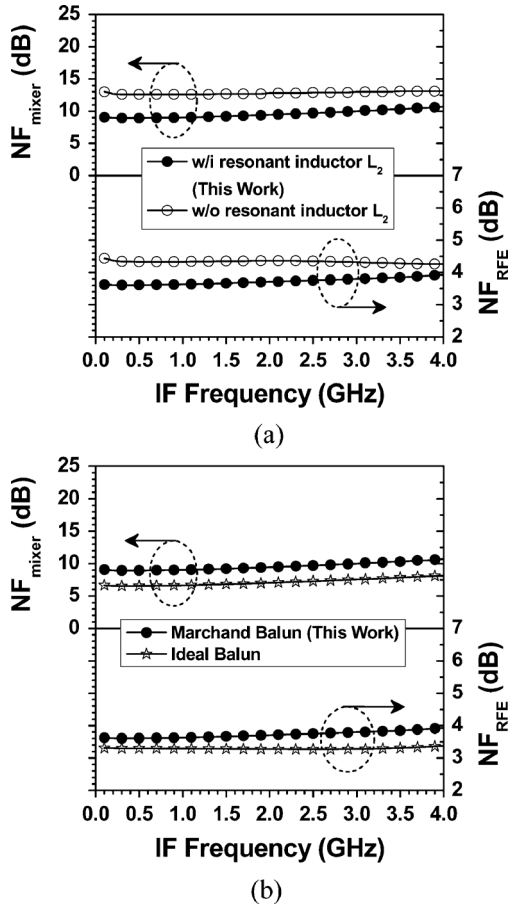


Fig. 16. Simulated $\mathrm{NF}_{\mathrm{mixer}}$ and $\mathrm{NF}_{\mathrm{RF}E}$ versus IF frequency characteristics: (a) with and without the resonant inductor L_2 and (b) by using the designed Marchanrd baluns and by using the ideal baluns.

CG, but also an improvement of NF. Thus, due to the inductive gain peaking caused by L_2, the CG and NF performances of the mixer over the 21–29-GHz band can be enhanced.

Fig. 15(a) shows the simulated CG versus RF frequency characteristics of the mixer with and without the resonant inductor L_2. The IF frequency is fixed at 0.1 GHz. That is, the LO frequency is 0.1 GHz lower than the RF frequency. The mixer achieves flat and high CG of 11.8 $\pm$ 0.97 dB for frequencies 21–29 GHz. In addition, the resonant inductor L_2 can significantly improve the CG. For example, an improvement of 4.25 dB in CG (from 8.52 to 12.77 dB) is achieved at 24 GHz.

Fig. 15(b) shows the simulated CG versus RF frequency (i.e., LO frequency plus 0.1 GHz) characteristics of the mixer at various LO input power $(\mathrm{LO_{in}})$. For frequencies 21–29 GHz, the mixer achieves flat and high CG of 11.45 ± 1.12 dB for $\mathrm{LO_{in}} = -3$ dBm and 10.76 ± 1.23 dB for $\mathrm{LO_{in}} = 1$ dBm, close to that (11.8 ± 0.97 dB) of this work ($\mathrm{LO_{in}} = -1$ dBm). In addition, the mixer achieves $P_{1\ \mathrm{dB}}$ better than -15 dBm and group-delay variation smaller than ± 6 ps for frequencies 21–29 GHz.

Fig. 16(a) shows the simulated single-sideband (SSB) NF of the mixer $(\mathrm{NF_{mixer}})$ and the SSB NF of the receiver front-end $(\mathrm{NF_{RFE}})$ versus IF frequency characteristics with and without the resonant inductor L_2. The LO frequency is fixed at 25 GHz, and the RF frequency is the sum of the LO frequency and the IF frequency. As can be seen, the resonant inductor L_2 can significantly improve NF. For example, an improvement of 3.93 dB in $\mathrm{NF_{mixer}}$ (from 13 to 9.07 dB) is achieved at IF frequency of 0.1 GHz. In addition, the resonant inductor L_2 can significantly improve $\mathrm{NF}_{\mathrm{RF}E}$. For example, an improvement of 0.82 dB in NF (from 4.44 to 3.62 dB) is achieved at IF frequency of 0.1 GHz.

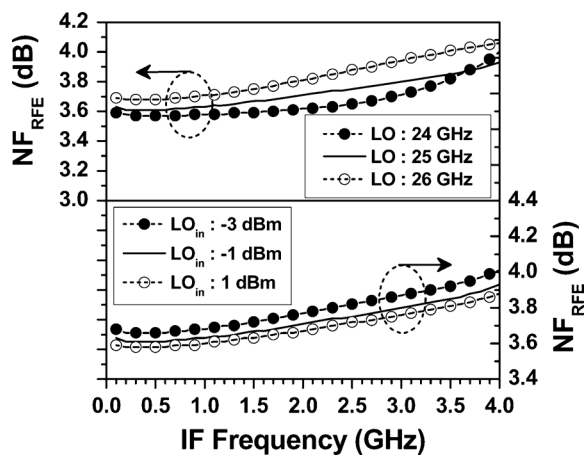
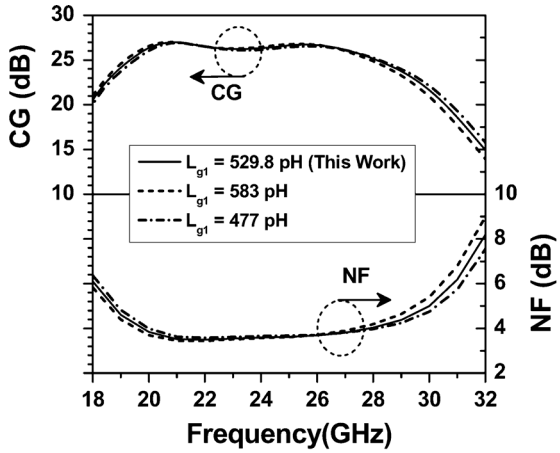
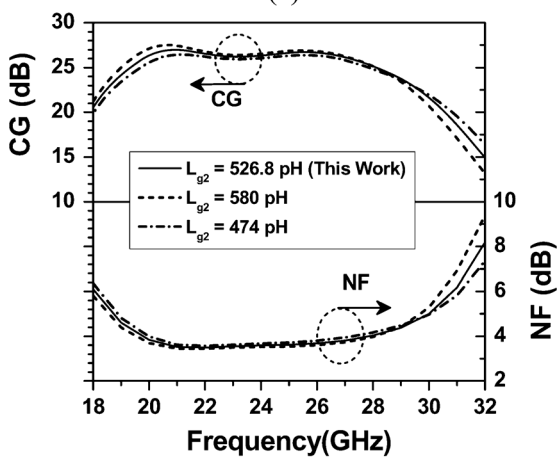


Fig. 17. Simulated $\mathrm{NF}_{\mathrm{RF}E}$ versus IF frequency characteristics at various LO frequencies and LO input power.

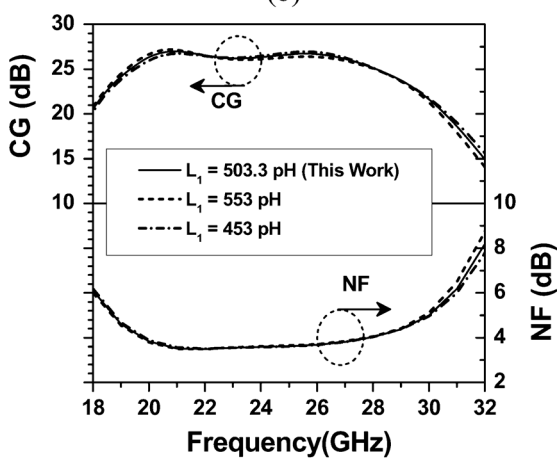
Fig. 16(b) shows the simulated $\mathrm{NF_{mixer}}$ and $\mathrm{NF}_{\mathrm{RF}E}$ versus IF frequency characteristics by using the Marchard baluns and



(a)



(b)



(c)

Fig. 18. Simulated CG and NF versus frequency characteristics of the receiver front-end at various: (a) L_{g1} values, (b) L_{g2} values, and (c) L_1 values.

the ideal baluns. Compared with the case that uses the ideal baluns, though there is a medium degradation in $\mathrm{NF}_{\mathrm{mixer}}$ due to the loss of the Marchand baluns, the degradation in $\mathrm{NF}_{\mathrm{RF}E}$ is slight. For example, at IF frequency of 0.1 GHz, the degradation in $\mathrm{NF}_{\mathrm{mixer}}$ is 2.42 dB (from 6.65 to 9.07 dB), while the degradation in $\mathrm{NF}_{\mathrm{RF}E}$ is only 0.31 dB (from 3.31 to 3.62 dB). This is mainly attributed to the high gain of the LNA.

Fig. 17 shows the simulated $\mathrm{NF}_{\mathrm{RF}E}$ versus IF frequency characteristics at various LO frequencies. The RF frequency is

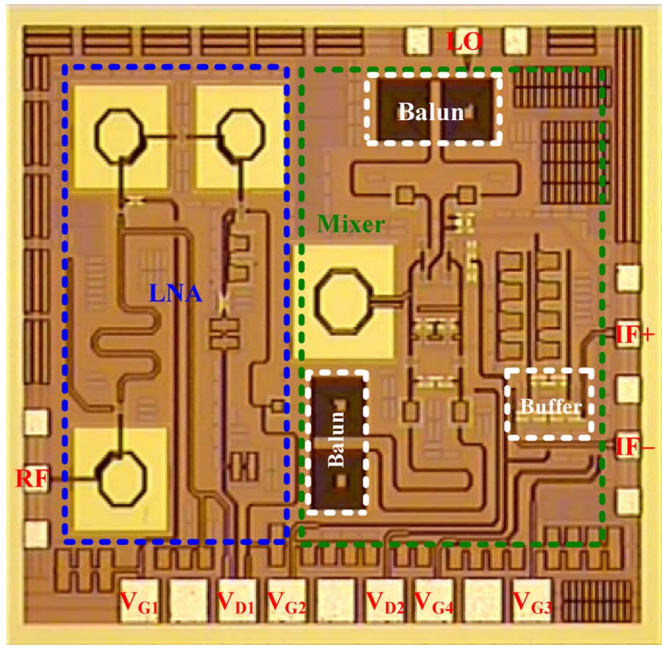


Fig. 19. Chip micrograph of the implemented receiver front-end.

the sum of the LO frequency and the IF frequency. The variation of LO frequency only slightly changes $\mathrm{NF}_{\mathrm{RF}E}$ performance. For example, at IF frequency of 0.1 GHz, the simulated $\mathrm{NF}_{\mathrm{mixer}}$ is 3.59 dB and 3.6 dB at LO frequency of 24 and 26 GHz, respectively, close to that (3.63 dB) at 25 GHz. What is also shown in Fig. 17 is the simulated $\mathrm{NF}_{\mathrm{RF}E}$ versus IF frequency characteristics at various LO input power. The variation of LO input power only slightly changes $\mathrm{NF}_{\mathrm{RF}E}$ performance. For example, at IF frequency of 0.1 GHz, the simulated $\mathrm{NF}_{\mathrm{RF}E}$ is 3.68 and 3.59 dB at LO input power of -3 and 1 dBm, respectively, close to that (3.63 dB) at 25 GHz.

Fig. 18(a) shows the simulated CG and NF versus frequency characteristics of the receiver front-end at various L_{g1} values, i.e., typical value (529.8 pH), typical value plus 10% (583 pH), and typical value minus 10% (477 pH). The simulated CG of the receiver front-end is 25.12 ± 1.86 dB for $L_{g1} = 583$ pH and 25.44 ± 1.46 dB for $L_{g1} = 477$ pH, close to that (25.35 ± 1.61 dB) for $L_{g1} = 529.8$ pH. In addition, the simulated NF of the receiver front-end is 4.04 ± 0.41 dB for $L_{g1} = 583$ pH and 3.94 ± 0.31 dB for $L_{g1} = 477$ pH, close to that (3.93 ± 0.44 dB) for $L_{g1} = 529.8$ pH.

Fig. 18(b) shows the simulated CG and NF versus frequency characteristics of the receiver front-end at various L_{g2} values, i.e., typical value (526.8 pH), typical value plus 10% (580 pH), and typical value minus 10% (474 pH). The simulated CG of the receiver front-end is 25.42 ± 2.02 dB for $L_{g2} = 580$ pH and 25.01 ± 1.44 dB for $L_{g2} = 474$ pH, close to that (25.35 ± 1.61 dB) for $L_{g2} = 526.8$ pH. In addition, the simulated NF of the receiver front-end is 3.93 ± 0.49 dB for $L_{g2} = 580$ pH and 4.02 ± 0.46 dB for $L_{g2} = 474$ pH, close to that (3.93 ± 0.44 dB) for $L_{g2} = 526.8$ pH.

Fig. 18(c) shows the simulated CG and NF versus frequency characteristics of the receiver front-end at various L_1 values, i.e., typical value (503.3 pH), typical value plus 10% (553 pH),

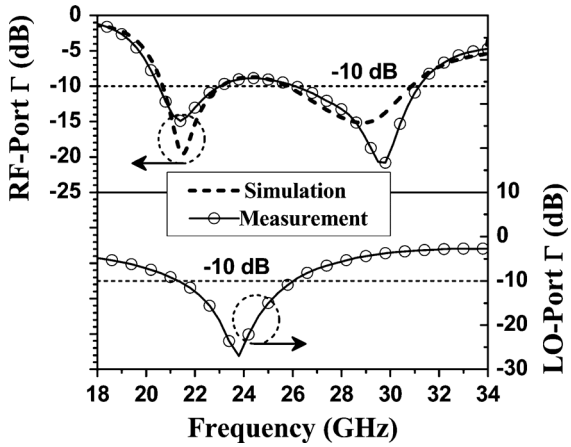


Fig. 20. Measured and simulated RF-port reflection coefficient and measured LO-port reflection coefficient versus frequency characteristics of the receiver front-end.

and typical value minus 10% (453 pH). The simulated CG of the receiver front-end is 25.39 ± 1.75 dB for $L_1 = 580$ pH and 25.22 ± 1.52 dB for $L_1 = 474$ pH, close to that (25.35 ± 1.61 dB) for $L_1 = 526.8$ pH. In addition, the simulated NF of the receiver front-end is 3.95 ± 0.46 dB for $L_1 = 553$ pH and 3.95 ± 0.44 dB for $L_1 = 453$ pH, close to that (3.93 ± 0.44 dB) for $L_1 = 503.3$ pH.

In addition, two-tone intermodulation simulation was performed at RF frequencies of 24 and 24.001 GHz, fixed LO frequency of 23.9 GHz, and fixed LO input power of -1 dBm. The receiver front-end shows $P_{1\,\mathrm{dB}}$ of -29 dBm, input second-order intercept point (IIP2) of 40 dBm, and input third-order intercept point (IIP3) of -19 dBm (not shown here).

IV. Measurement Results and Discussions

The chip micrograph of the finished receiver front-end is shown in Fig. 19. The chip area is only 1.25×1.06 mm^2, including the test pads. On-wafer measurement was performed by using an Agilent's 50-GHz RFIC measurement system, including an Agilent E8254A (250 kHz–40 GHz) PSG analog signal generator for generation of LO input signals, an Agilent E4448A (3 Hz–50 GHz) PSA series spectrum analyzer for IF spectrum measurement, and an Agilent HP8510C vector network analyzer (VNA) for return- and insertion-loss measurements. The gate bias of the RF input transistors and the gate bias of the LO switching quad is 0.7 and 1.1 V, respectively. The LNA consumes a current of 7.21 mA from a 1.8-V supply. The mixer (includes the IF amplifier) consumes a current of 17.5 mA from a 1.5-V supply. That is to say, the receiver front-end consumes 39.2 mW power in total.

Fig. 20 shows the measured and simulated RF-port reflection coefficient versus frequency characteristics of the receiver front-end. The measured result conforms well to the simulated one. The measured RF-port reflection coefficient is below -10 dB for frequency from 20.5 to 31.2 GHz (except for a small range from 23 to 26.1 GHz, which is below 9 dB), indicating a very broadband input matching characteristic. What is also shown in Fig. 20 is the measured LO-port reflection coefficient versus frequency characteristics of the receiver front-end. The measured LO-port reflection coefficient is below -10 dB for frequencies 21.3–26.1 GHz.

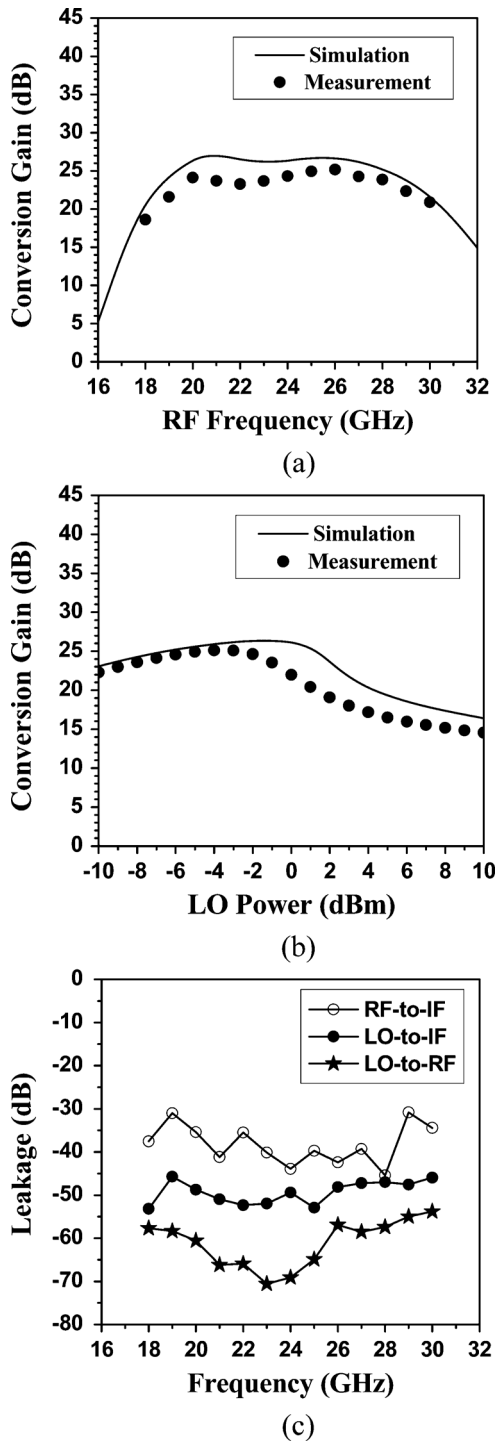


Fig. 21. (a) Measured and simulated CG versus RF frequency characteristics, (b) measured and simulated CG versus LO input power characteristics, and (c) measured RF-IF, LO-IF, and LO-RF isolation versus frequency characteristics of the receiver front-end.

Fig. 21(a) shows the measured and simulated CG versus RF frequency characteristics of the receiver front-end at IF frequency of 0.1 GHz. That is, the LO frequency is 0.1 GHz lower than the RF frequency. The measured result conforms well to the simulated one. The receiver front-end achieves flat and high CG of 23.7 ± 1.4 dB over the 21–29-GHz band.

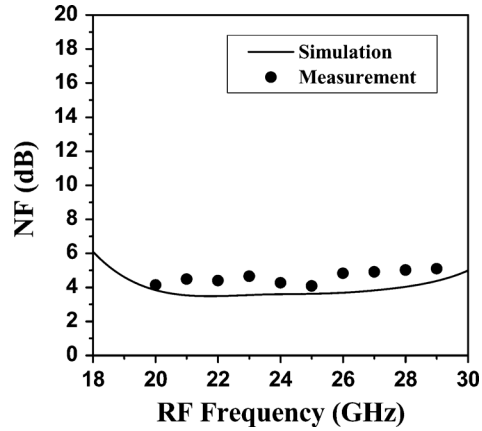


Fig. 22. Measured and simulated NF versus frequency characteristics of the receiver front-end.

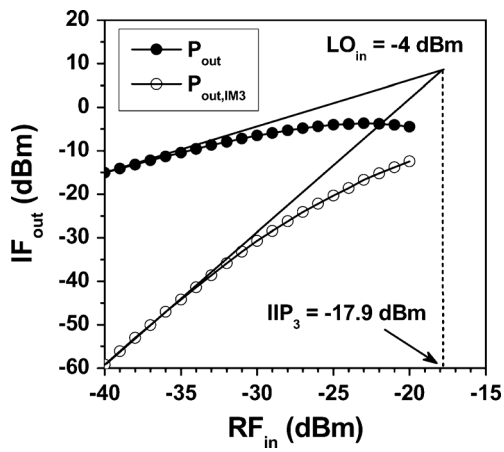


Fig. 23. Measured IIP3 of the receiver front-end at 24 GHz.

Fig. 21(b) shows the measured and simulated CG versus LO input power characteristics at RF frequency of 24 GHz, IF frequency of 0.1 GHz, and RF input power of -40 dBm. The measured result conforms well to the simulated one. Due to the excellent LO-port input matching (-26 dB at 23.9 GHz), the receiver front-end achieves maximum CG of 25.1 dB at a relatively lower LO input power of -4 dBm. Note that a sufficiently large LO input power will push the RF input transistors to the triode region due to the large voltage drop of the load resistors R_7/R_8, which, in turn, results in a degradation of g_m of the RF input transistors. This explains why the CG exhibits a maximum of 25.1 dB at LO input power of -4 dBm, then drops at higher LO power levels.

Fig. 21(c) shows the measured LO-IF, LO-RF, and RF-IF isolation versus frequency characteristics of the receiver front-end. The receiver front-end achieves excellent LO-IF isolation smaller than -47 dB, LO-RF isolation smaller than -55 dB, and RF-IF isolation smaller than -35.5 dB over the 21–29-GHz band.

Fig. 22 shows the measured and simulated NF versus RF frequency characteristics of the receiver front-end. The measured result conforms well to the simulated one. The receiver front-end achieves excellent flat and low NF of 4.6 ± 0.5 dB over the 21–29-GHz band.

TABLE I
SUMMARY OF THE IMPLEMENTED 21–29-GHz CMOS RECEIVER FRONT-END, AND RECENTLY REPORTED STATE-OF-THE-ART 21–29-GHz BAND CMOS RECEIVER FRONT-ENDS

	This Work	[3] 2004-JSSC	[4] 2008-ISCAS (simulation)	[10] 2009-TMTT
CMOS Technology (μm)	0.18	0.18	0.18	0.18
RF frequency (GHz)	21 ~ 29	21.8	24	22 ~ 29
LO frequency (GHz)	25	16.9	23.9	25.5
IF frequency (GHz)	0~ 4	4.9	0.1	0~ 3.5
S_{11} (dB)	-8.8 ~ -16.8	-21	-12.2	<-14.5
LO-IF Leakage (dB)	-47 ~ -52.3	--	-20.9	<-23
LO-RF Leakage (dB)	-55 ~ -70.5	--	--	<-30
RF-IF Leakage (dB)	-35.5 ~ -45.4	--	-38.5	<-45
Conversion Gain (dB)	23.7 ± 1.4	27.5	23.36	36.55 ± 1.55
NF (dB)	4.6 ± 0.5	7.7	5.32	6.45 ± 0.95
IIP3 (dBm)	-17.9	--	-17.4	-9
P_{1dB} (dBm)	-28	-23	-27	-20.3
BW(GHz)	9	--	--	8.7
Power Consumption (mW)	39.2	64.5	31.65	50.94

In addition, two-tone intermodulation measurement was performed at RF frequencies of 24 and 24.001 GHz, fixed LO frequency of 23.9 GHz, and fixed LO input power of -4 dBm. Fig. 23 shows the measured fundamental and third-order intermodulation (IM3) output power versus input power characteristics of the receiver front-end. The corresponding $P_{1\ \mathrm{dB}}$ and IIP3 are -28 dBm and -17.9 dBm, respectively.

Table I is a summary of the implemented 21–29-GHz CMOS receiver front-end, and recently reported state-of-the-art 21–29-GHz band CMOS receiver front-ends [3], [4], [10]. As can be seen, our receiver front-end exhibits the lowest NF, low power, and excellent port-to-port isolations. Overall, the results indicate that this receiver front-end is suitable for 21–29-GHz UWB automotive radar systems.

V. CONCLUSION

In this paper, we have presented the design and analysis of a 21–29-GHz CMOS receiver front-end in a standard 0.18-μm CMOS process for UWB automotive radar systems. The performances of the mixer are improved with the current-bleeding technique and a parallel resonant inductor in the differential outputs of the RF transconductance stage. The wideband Marchand baluns can convert the single RF and LO signals to nearly perfect differential signals over the 21–29-GHz band. The receiver front-end dissipates 39.2 mW, and exhibits excellent CG of 23.7 ± 1.4 dB and NF of 4.6 ± 0.5 dB over the 21–29-GHz band. In addition, LO-IF isolation smaller than -47 dB, LO-RF isolation smaller than -55 dB, and RF-IF isolation smaller than -35.5 dB are achieved over the 21–29-GHz band. The results highlight the potential application of the proposed architecture in 21–29-GHz band communication systems.

ACKNOWLEDGMENT

The authors are very grateful for the support of the National Chip Implementation Center (CIC), Hsinchu, Taiwan, for chip

fabrication, and the National Nano-Device Laboratory (NDL), Hsinchu, Taiwan, for measurements.

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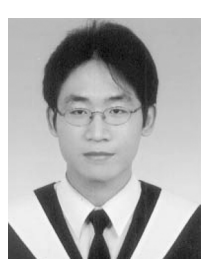

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