Analysis and Design of a CMOS Bidirectional Passive Vector-Modulated Phase Shifter

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***Abstract*— This paper presents a passive vector-modulated phase shifter (VMPS). The passive X-type attenuator consisting of digitally controlled transistor-array units is employed to perform the phase-invertible gain tuning, and thus enables phase shift in all four quadrants. The Wilkinson-like power combiner is utilized to sum up the quadrature signals and avoid impedance mismatches. Analysis proves that the proposed passive VMPS can provide consistent phase-shift performance for bidirectional operation. The proof-of-concept VMPS is implemented in 40-nm CMOS technology and occupies a core chip area of 0.15 mm^2. Measured results prove that it can provide consistent bidirectional 6-bit phase-shift operation, with accurate phase tuning (i.e., RMS phase error $< 2.4°$) and low gain error (i.e., $\pm$ 0.6 dB) over the whole 70–90 GHz band.**

***Index Terms*— CMOS, E band, gain tuning, millimeter-wave (mm-Wave), phase shifter, phased array, vector-modulated phase shifter, X-type attenuator.**

I. Introduction

THE increasing demand for high-data-rate wireless links has driven the development of the millimeter-wave (mm-Wave) communications in E band, such as the high-density fixed wireless services [1] and the satellite communications [2]. To simultaneously enable high-speed link, flexible signal coverage and interference tolerance, high-performance phased-array transceivers are required [3], [4].

In each element of a phased-array system, the phase shifter is employed for performing beamforming and spatial filtering. Both the active and passive phase shifters have been used to accomplish phase tuning in the phased-array systems [5]–[11]. The switched-type phase shifter (STPS) and reflective-type phase shifter (RTPS) are the most commonly used passive phase shifter topologies. As shown in Fig. 1(a), the STPS usually consists of cascaded phase shifting units, in order to cover a large phase-shift range with high resolution [12]–[14]. However, too many cascaded transistors in signal path will introduce high loss. Besides, the loss variation among the phase-shifting states has to be carefully compensated. For instance, the variable gain amplifier (VGA) is used to compensate for the gain variations in [15]. Compared with the multi-bit high-resolution STPS, the RTPS has relatively low loss while ensuring high phase-shift resolution. As depicted in Fig. 1(b), the RTPS consists of a 3dB quadrature coupler and two tunable reflective loads to perform phase tuning, and its phase-shift range depends on the impedance tuning range of the reflective loads. To achieve full 360° phase-shift range, multi-resonance loads are required. The dual-resonated loads enabling high phase-shift range for RTPS are reported in [16], [17]. In [18], the transformer-based multi-resonance loads are adopted, contributing to over 360° phase-shift range. However, the impedance of a multi-resonance load is highly dependent on the operation frequency, which leads to inherently narrow band nature of the RTPS. The dual-voltage control method can be employed to enhance the operation bandwidth, but with the penalty of high control complexity [18], [19].

As shown in Fig. 1(c), the vector-modulated phase shifter (VMPS) consists of a 3dB quadrature coupler, two gain tuning blocks and a combining network to sum up the in-phase (I) and quadrature (Q) signals. By employing phase-invertible gain tuning blocks, the VMPS can provide fully 360° phase-shift range, covering all four quadrants. The active VMPS employing the VGA as the gain tuning block can provide power gain and thus compensate for the loss introduced by the passive components [20]–[25], but at the penalty of DC power consumption. The linearity of the active VMPS is limited by the linear output of the VGA, and the overall linear output power suffers from an inherent 3 dB loss from the combiner. In contrast, the passive VMPS has the advantage of zero DC power. Although the passive loss is relatively high, it can be compensated by a single amplifier, which would consume less DC power than the two VGAs. Also, unlike the VGA in the active VMPS, the linear output power of the compensation amplifier following the passive VMPS will not be affected. The passive VMPSs with different gain tuning structures have been investigated. In [26], [27], the reflective-type attenuator (RTA) is employed to achieve the phase-invertible gain tuning for the VMPS. However, the coupler-based RTA usually occupies large area, leading to bulky chip size. In addition, the analog control method of the RTA is inconvenient for the digitally-controlled beamforming of the phased-array systems. In [28], [29], the T-/PI-type attenuators are utilized for gain tuning, and the phase inverting operation is performed by an extra sign-select combining amplifier, which introduces extra DC power consumption. Recently, the switch-based X-type attenuator enabling both digital gain control and phase inverting operation is adopted for the design of VMPS in [30], [31]. Although they can provide accurate phase shift in the target

Manuscript received October 31, 2020; revised December 15, 2020; accepted December 30, 2020. Date of publication January 14, 2021; date of current version March 8, 2021. This work was supported in part by the National Key Research and Development Program of China under Grant 2019YFB1803000. This article was recommended by Associate Editor P. Rombouts. *(Corresponding author: Dixian Zhao.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2020.3048816.

Digital Object Identifier 10.1109/TCSI.2020.3048816

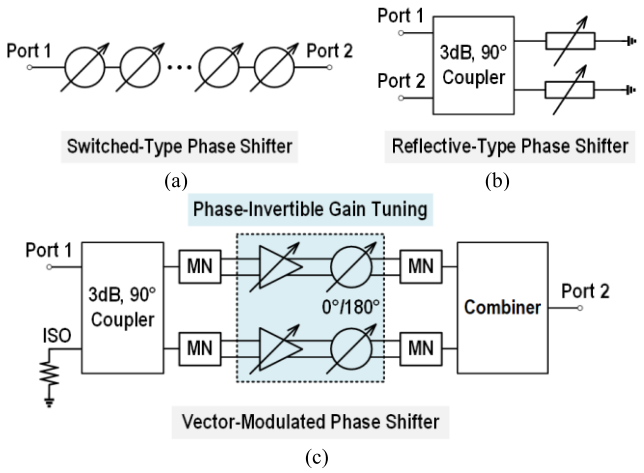


Fig. 1. Block diagrams of (a) the switched-type phase shifter (STPS), (b) the reflective-type phase shifter (RTPS) and (c) the vector-modulated phase shifter (VMPS).

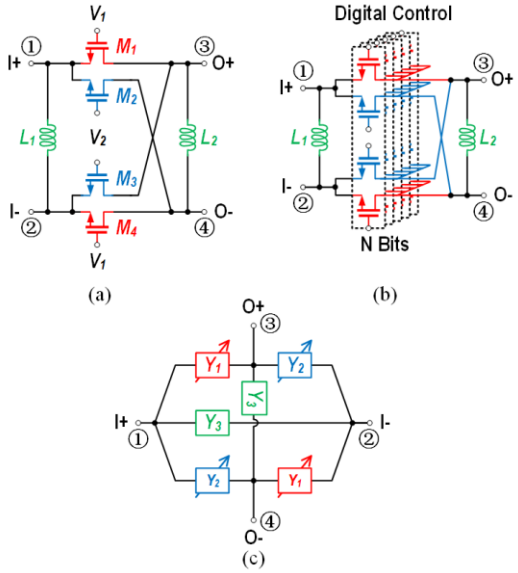


Fig. 2. (a) Schematic of the X-type attenuator utilizing analog-controlled transistors. (b) Schematic of the X-type attenuator using transistor array for direct-digital control. (c) Equivalent model of the X-type attenuator.

bands, the control codes have to be optimized for different frequencies in their bands, which increases control complexity. Besides, for the design of the VMPS employing the X-type attenuator, only a qualitative, first-order description has been addressed. And, the two commonly used combining topologies, including the current combining and the power combining topologies, which have different combining behaviors, are not discussed.

In this paper, an in-depth, thorough analysis of the passive VMPS utilizing the X-type attenuator is presented. For the X-type attenuator, the derivations of its transmission and reflection behaviors, and the modeling of gain errors across process, voltage and temperature (PVT) variations are carried out, guiding the optimizations of the gain tuning block. For the combining block, the behaviors of both the current and power combining topologies are analyzed and compared, in order to determine a suitable combining topology for the passive VMPS. The forward and backward phase shifting modes are discussed, indicating that the proposed passive VMPS can provide consistent phase-shift performance for bidirectional operation. The proof-of-concept VMPS is implemented in 40-nm CMOS technology. Measured results prove that it can achieve ultra-broadband (i.e., 70–90 GHz) bidirectional 6-bit phase shift, with low RMS phase error (i.e., $< 2.4°$) and low gain error (i.e., $\pm$ 0.6 dB). Besides, the control codes are consistent over the whole 70–90 GHz band, without the need of frequency-dependent compensations or look-up tables.

This paper is organized as follows. Section II presents the thorough analysis of the X-type attenuator. Section III compares the current and power combining topologies and demonstrates the bidirectional operation of the passive VMPS. In Section IV, the design details of the passive VMPS are presented, where the 2-bit control method are proposed, with extra degree of freedom to control the VMPS. Finally, the measured results are depicted and discussed, in Section V.

II. Gain Tuning Block

The bidirectional passive VMPS requires a passive gain tuning block to weight both the I and Q signals, and provide phase inverting operation so as to support full 360° phase shift.

A. X-Type Attenuator

As shown in Fig. 2(a), the X-type attenuator commonly consists of cross-connected transistors M_{1-4}, with the same size. These transistors operate in the deep triode region and can provide tunable resistance by changing the gate control voltage [32]. To enable a balanced differential signal, M_1 and M_4 share the same gate control voltage V_1, and M_2 and M_3 share the same gate control voltage V_2. The unwanted parasitic capacitance of the transistors may affect the gain tuning performance. In fact, by simply adding the two shunt inductors L_1 and L_2 (shown in Fig. 2a), the transistor parasitic capacitance can be resonated out. To enable direct-digital control for the X-type attenuator, the multi-unit transistor array with digital control can be adopted (see Fig. 2b).

Fig. 2(c) depicts the equivalent circuit model of the X-type attenuator for investigating the transmission and reflection behaviors. The Y_1, Y_2 and Y_3 representing the admittances of the devices are adopted for a universal and concise analysis. For the four-port circuit shown in Fig. 2(c), the Y-parameter matrix is

$$Y_{4P} = \begin{bmatrix} Y_1+Y_2+Y_3 & -Y_3 & -Y_1 & -Y_2 \\ -Y_3 & Y_1+Y_2+Y_3 & -Y_2 & -Y_1 \\ -Y_1 & -Y_2 & Y_1+Y_2+Y_3 & -Y_3 \\ -Y_2 & -Y_1 & -Y_3 & Y_1+Y_2+Y_3 \end{bmatrix} \quad (1)$$

In Fig. 3(a) and 3(b), the four-port and two-port models of the X-type attenuator are shown. The voltage and current settings of each port are marked. Consider the relationships of the voltage, current and Y-parameter matrix between the four-port

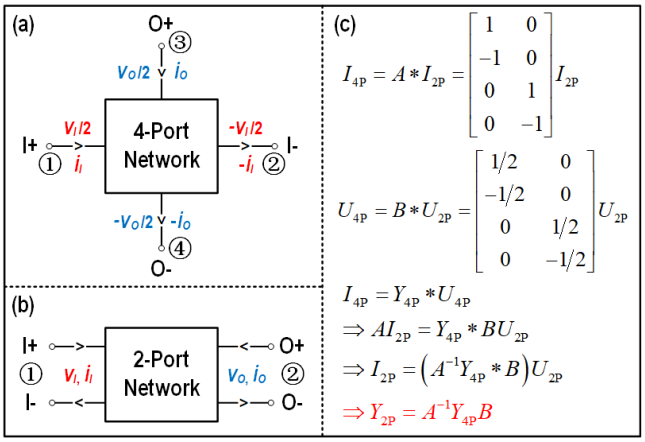


Fig. 3. (a) 4-port network model and the voltage and current settings. (b) 2-port network model and the voltage and current settings. (c) Relationships of the voltage, current and the Y-parameter matrix between the 4-port and 2-port networks.

and two-port networks, as shown in Fig. 3(c), the Y-parameters of the two-port model can be calculated

$$Y_{2P} = \begin{bmatrix} \frac{1}{2}(Y_1 + Y_2 + 2Y_3) & \frac{1}{2}(-Y_1 + Y_2) \\ \frac{1}{2}(-Y_1 + Y_2) & \frac{1}{2}(Y_1 + Y_2 + 2Y_3) \end{bmatrix} \tag{2}$$

Further, the S-parameters of the attenuator can be calculated by using the transformation from Y-parameters to S-parameters

$$S = \frac{1}{[1 + (Y_1 + Y_3) Z_L][1 + (Y_2 + Y_3) Z_L]} \times \begin{bmatrix} 1 - (Y_1 + Y_3)(Y_2 + Y_3) Z_L{}^2 & (Y_1 - Y_2) Z_L \\ (Y_1 - Y_2) Z_L & 1 - (Y_1 + Y_3)(Y_2 + Y_3) Z_L{}^2 \end{bmatrix} \tag{3}$$

where Z_L represents the load impedance of the attenuator. Consider the simplified model of the transistors and inductors, then the admittance Y_1, Y_2 and Y_3 can be simply calculated by

$$\begin{aligned} Y_1 &= 1/R_1 + j\omega C_{\text{par}} \\ Y_2 &= 1/R_2 + j\omega C_{\text{par}} \\ Y_3 &= -j/\omega L \end{aligned} \tag{4}$$

where R_1 and R_2 represent the tunable resistance of the transistors and C_{par} is the parasitic capacitance. For simplicity, we assume that the parasitic capacitance is the same for Y_1 and Y_2, and its value is invariant when the resistance is tuned. Considering (3) and (4), the frequency-dependent S-parameters can be calculated

$$\begin{aligned} S_{21} = S_{12} &= \frac{Z_L (1/R_1 - 1/R_2)}{[1 + Z_L/R_1 + j\text{f}(\omega)][1 + Z_L/R_2 + j\text{f}(\omega)]} \\ S_{11} = S_{22} &= \frac{1 - [Z_L/R_1 + j\text{f}(\omega)][Z_L/R_2 + j\text{f}(\omega)]}{[1 + Z_L/R_1 + j\text{f}(\omega)][1 + Z_L/R_2 + j\text{f}(\omega)]} \end{aligned} \tag{5}$$

where

$$\text{f}(\omega) = Z_L\left(\omega C_{\text{par}} - 1/\omega L\right) \tag{6}$$

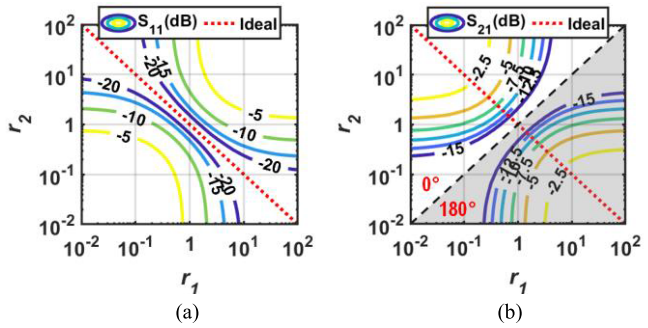


Fig. 4. Calculated contour lines of (a) S_{11} and (b) S_{21} when r_1 and r_2 are varied.

The imaginary part f(ω) causes variant S-parameters versus frequency. Consider the resonance at the center frequency ω_0

$$L = 1/\omega_0^2 C_{\text{par}} \tag{7}$$

then (6) can be rewritten

$$\text{f}(\omega) = Z_L C_{\text{par}}\left(\omega - \omega_0^2/\omega\right) \tag{8}$$

In fact, based on the S_{21} in (5), the fluctuation of gain versus frequency is negligible when f(ω) $<<$ 1, which can usually be satisfied over a wide band. Besides, according to (8), a low C_{par} leads to a flat f(ω) around 0, which means the bandwidth can be enhanced if C_{par} (mainly decided by the technology) is reduced.

Then, consider the S-parameters at the center frequency

$$\begin{aligned} S_{21} = S_{12} &= \frac{Z_L (1/R_1 - 1/R_2)}{(1 + Z_L/R_1)(1 + Z_L/R_2)} \\ S_{11} = S_{22} &= \frac{1 - (Z_L/R_1)(Z_L/R_2)}{(1 + Z_L/R_1)(1 + Z_L/R_2)} \end{aligned} \tag{9}$$

To ensure impedance matching, S_{11} and S_{22} should be zero, leading to

$$R_1 R_2 = Z_L^2 \tag{10}$$

For calculation convenience, R_1 and R_2 are normalized to Z_L, which is defined as

$$\begin{aligned} r_1 &= R_1/Z_L \\ r_2 &= R_2/Z_L \end{aligned} \tag{11}$$

Then the S-parameters in (9) can be simplified

$$\begin{aligned} S_{11} = S_{22} &= \frac{r_1 r_2 - 1}{(1 + r_1)(1 + r_2)} \\ S_{21} = S_{12} &= \frac{r_2 - r_1}{(1 + r_1)(1 + r_2)} \end{aligned} \tag{12}$$

Fig. 4(a) and 4(b) depict the calculated contour lines of the S_{11} and S_{21} (in decibel) using (12), so as to clearly present the transmission and reflection behaviors when r_1 and r_2 are tuned. As shown in Fig. 4(b), the attenuation level increases when r_1 and r_2 get close, and the maximum attenuation is achieved when $r_1 = r_2$. The phase of S_{21} is 0° when $r_1 < r_2$ and is inverted (i.e., 180°) when $r_1 > r_2$. In Fig. 4(a), it can be found that perfect impedance matching can be achieved when $r_1 r_2 = 1$ (i.e., the ideal case marked by the dotted line), even

the attenuation level is variant. Therefore, in practical design, r_1 and r_2 should be tuned to satisfy $r_1 r_2 = 1$, in order to achieve phase-invertible gain tuning and impedance matching simultaneously. For the VMPS to achieve a phase shift θ with linear tuning step, the corresponding attenuation of the I- and Q-path attenuators should be independently tuned to satisfy

$$\begin{aligned} G_I &= G_0 + 20\log_{10}\ (\cos\theta) \\ G_Q &= G_0 + 20\log_{10}\ (\sin\theta) \end{aligned} \tag{13}$$

where G_0 represents the insertion loss of the X-type attenuator. Considering (12) and (13), the target r_1 and r_2 for both the I- and Q-path attenuators can be worked out for each phase state.

B. Modeling and Optimization of Gain Variation

The PVT variations will affect the transistor parameters and thus deteriorate the gain tuning performance. To provide robust and consistent gain and phase shifting performance for the passive VMPS, the X-type attenuator should have the least gain variation across different corners. Therefore, it is necessary to investigate the gain variation behavior of the X-type attenuator.

For the impact of the corner variations on the transistor, consider both the resistance and capacitance variations will lead to an accurate model. The error factors ε and ε_C are introduced, and the parameters with corner variations are now given by

$$\begin{aligned} R_{1,\mathrm{err}} &= (1+\varepsilon)\, R_1 \\ R_{2,\mathrm{err}} &= (1+\varepsilon)\, R_2 \\ C_{\mathrm{par,err}} &= (1+\varepsilon_C)\, C_{\mathrm{par}} \end{aligned} \tag{14}$$

Note that the error factors could be negative or positive. In (14), the two resistors share the same error factor, considering that the transistors are usually close to each other in the design and they will exhibit similar variation behaviors. Besides, for simplicity, the Z_L is assumed to remain the same under different corners. Consider (5), (6), (11) and (14), then the S_{21} with errors is given by (15), as shown at the bottom of the page,

$$\mathrm{f}_e = \varepsilon_C \omega_0 C_{\mathrm{par}} Z_L \tag{16}$$

Dependent on the used technology, ε_C is typically less than 0.1 and $\omega_0 C_{\mathrm{par}} Z_L$ is usually < 1, thus $\mathrm{f}_e << 1$ can be satisfied and the imaginary part in (15) can be ignored, leading to

$$S_{21,err} = \frac{(1+\varepsilon)\,(r_2 - r_1)}{[1+(1+\varepsilon)\,r_1]\,[1+(1+\varepsilon)\,r_2]} \tag{17}$$

Then, the gain variation can be calculated and simplified as

$$\Delta S_{21} = \frac{S_{21,err}}{S_{21}} = 1 \Big/ \left[1 + \frac{\varepsilon r_1 r_2 - \varepsilon/(1+\varepsilon)}{(1+r_1)\,(1+r_2)}\right] \tag{18}$$

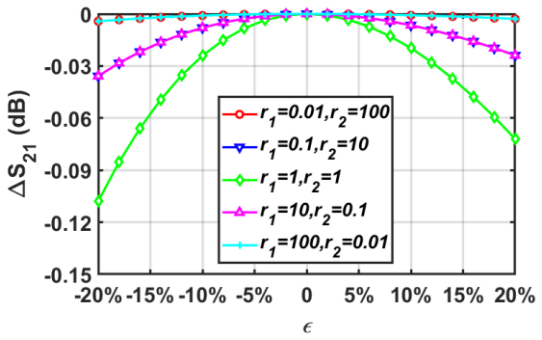


Fig. 5. Calculated ΔS_{21} versus the error factor ε, when $r_1 r_2 = 1$ is satisfied.

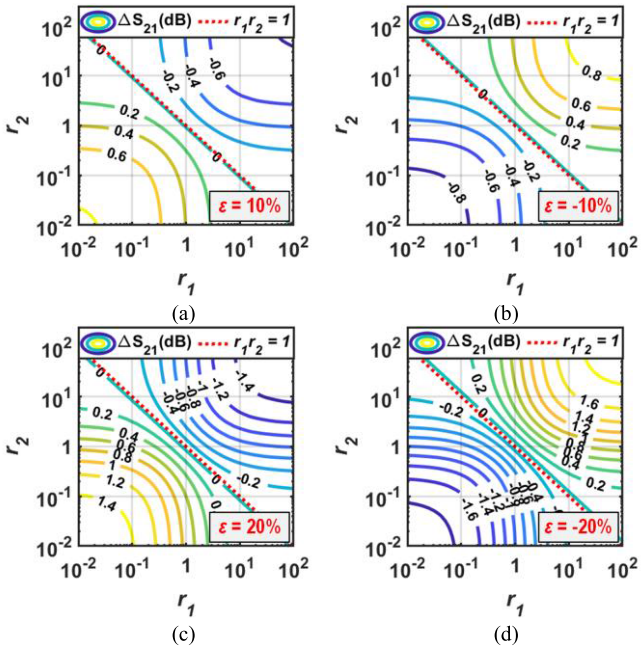


Fig. 6. Calculated contour lines of ΔS_{21} for (a) $\varepsilon = 10\%$, (b) $\varepsilon = -10\%$, (c) $\varepsilon = 20\%$ and (d) $\varepsilon = -20\%$, respectively.

As indicated by (18), the gain variation depends on ε, r_1 and r_2. To achieve zero gain error, (18) should be 1, leading to

$$r_1 r_2 = 1/(1+\varepsilon) \tag{19}$$

Thus, the product of r_1 and r_2 has to change when ε varies, in order to ensure zero gain variation. Although it is hard to achieve zero gain variation with a variant ε (e.g., variant operation temperature), the gain variation could be sufficiently small if the values of r_1 and r_2 are properly set. Fig. 5 shows the calculated ΔS_{21} when $r_1 r_2 = 1$ is satisfied. The gain variation has the maximum value when $r_1 = r_2 = 1$, and it remains less than 0.11 dB even the error factor ε reaches $\pm$ 20%, indicating robust gain tuning performance. In practice, the condition $r_1 r_2 = 1$ is not always satisfied and it is necessary to further evaluate the gain error when $r_1 r_2 \neq 1$.

$$S_{21,err} = \frac{(1+\varepsilon)\,(r_2 - r_1)}{[1+(1+\varepsilon)\,r_1 + j\mathrm{f}_e\,(1+\varepsilon)\,r_1]\,[1+(1+\varepsilon)\,r_2 + j\mathrm{f}_e\,(1+\varepsilon)\,r_2]} \tag{15}$$

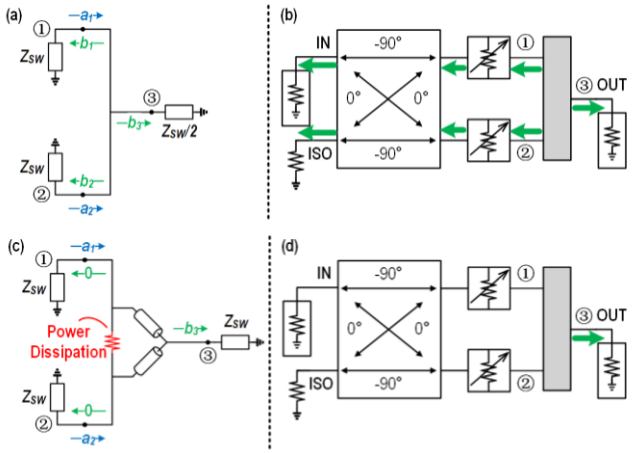


Fig. 7. Equivalent circuit of the current combining topology and (b) the reflected voltage waves. (c) Equivalent circuit of the power combining topology and (d) the reflected voltage waves.

Fig. 6(a)–(d) depict the calculated contour lines of ΔS_{21}, when r_1 and r_2 are varied from 0.01 to 100, and ε is set to 10%, −10%, 20% and −20%, respectively. As expected, the contour lines will become dense when the absolute value of ε gets large, implying that high resistance variation leads to large gain error. Besides, it can be observed that a low gain error can be ensured as long as $r_1 r_2$ is close to 1.

The above analysis suggests that in order to ensure impedance matching and minimize gain error while tuning the gain, $r_1 r_2 = 1$ should be satisfied. In consequence, for the digitally-controlled transistor array, an accurate and flexible resistance tuning is in demand to ensure $r_1 r_2 = 1$.

III. Combining Block

The VMPS requires a combining block to sum up the I and Q signals, so as to achieve a desired phase shift after combining. Two combining topologies are commonly used, which are the current and the power combining topologies, as shown in Fig 7. Since the two topologies exhibit different characteristics, they should be carefully selected when designing the VMPS.

A. Current Combining Vs. Power Combining

Fig. 7(a) shows the simplified model of the current combining topology. This topology directly connects the I- and Q-path outputs, and generates the combining output at the center tap. Assume the output impedances of the I and Q paths are identical and equal to Z_{SW}(assumed as a pure real value). The load impedance ensuring maximum power transmission is $Z_{SW}/2$. For this three-port network, the S-parameter matrix can be calculated [33]

$$S_C = \begin{bmatrix} -1/2 & 1/2 & 1/\sqrt{2} \\ 1/2 & -1/2 & 1/\sqrt{2} \\ 1/\sqrt{2} & 1/\sqrt{2} & 0 \end{bmatrix} \tag{20}$$

To investigate the behavior of the current combining network when it is adopted for the VMPS, excitations with quadrature phases are applied at port 1 and 2. Assume that a_1 and a_2 are the incident voltage waves of the two ports, and b_1, b_2 and b_3 represent the reflected voltage waves, as shown in Fig.7(a). The phase difference between a_1 and a_2 is 90°. Then, define the ratio of the two waves as

$$j\gamma = a_2/a_1 \tag{21}$$

where γ is a pure real value. Considering (20) and (21), the reflected voltage waves can be calculated

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = S_C \begin{bmatrix} a_1 \\ a_2 \\ 0 \end{bmatrix} = \begin{bmatrix} (-a_1 + a_2)/2 \\ (a_1 - a_2)/2 \\ (a_1 + a_2)/\sqrt{2} \end{bmatrix} = \begin{bmatrix} (-1 + j\gamma)\, a_1/2 \\ (1 - j\gamma)\, a_1/2 \\ (1 + j\gamma)\, a_1/\sqrt{2} \end{bmatrix} \tag{22}$$

For b_3 at the output port, define the combining gain

$$G_C = 10\lg \frac{|b_3|^2}{|a_1|^2} = 10\lg\left(1 + \gamma^2\right) - 3 \tag{23}$$

Also, define the ideal lossless combining gain

$$G_{Ideal} = 10\lg \frac{|a_1|^2 + |a_2|^2}{|a_1|^2} = 10\lg\left(1 + \gamma^2\right) \tag{24}$$

Comparing (23) and (24), it can be found that the current combining topology suffers from an inherent 3 dB loss, which means only half of the input power is delivered to the output port. The other half of power is reflected by the network, with a quarter of the power to port 1 and a quarter to port 2, which is predicted by (22) (i.e., b_1 and b_2). Fig. 7(b) demonstrates the reflected voltage waves in detail. The reflected voltage wave to port 3 is the desired phase shifting output, and the reflected voltage waves to port 1 and 2 will continue their transmission through the attenuators and the coupler, and finally reach the input and isolated ports of the coupler. Thus, for the phase shifter in Fig. 7(b), when excitation is applied at the coupler input, reflection will be observed there, indicating input impedance mismatch. For example, the S_{11} at the input port is −6 dB (i.e., a quarter of the input power reflected) when the blocks in Fig. 7(b) are lossless. Further, when the I-/Q-path attenuation is tuned, the reflected voltage wave at the coupler input (or equivalently, S_{11}) will have variant amplitude and phase, which makes the input impedance dependent on the gain settings and thus phase settings. This would cause degradation of phase shift accuracy, since the impedance matching performance is inconsistent in different phase states.

Fig. 7(c) shows the simplified model of the power combining topology, where the I and Q signals are summed up by a Wilkinson power combiner. For this combining network, the S-parameter matrix is [33]

$$S_P = \begin{bmatrix} 0 & 0 & -j/\sqrt{2} \\ 0 & 0 & -j/\sqrt{2} \\ -j/\sqrt{2} & -j/\sqrt{2} & 0 \end{bmatrix} \tag{25}$$

Similarly, excitations with quadrature phases are applied at port 1 and 2, and the reflected voltage waves can be calculated

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = S_P \begin{bmatrix} a_1 \\ a_2 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ -j\,(a_1 + a_2)/\sqrt{2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ -ja_1\,(1 + j\gamma)/\sqrt{2} \end{bmatrix} \tag{26}$$

For b_3 at the output port, the combining gain (in decibel) is

$$G_P = 10\lg\frac{|b_3|^2}{|a_1|^2} = 10\lg\left(1+\gamma^2\right) - 3 \tag{27}$$

which is same as (23). Thus, the power combining topology only delivers half the input power to the output port as well, with the other half dissipated on the isolation resistor. Besides, as indicated by (26), the reflected voltage waves at the two input ports remain zero, thanks to the perfect impedance matching and the ideal isolation. In consequence, for the phase shifter in Fig. 7(d), no reflection will be observed at the input port, and thus the input impedance is invariant when the I-/Q-path attenuation is tuned.

Based on the above analysis, conclusions can be drawn when the two combining topologies are adopted for the VMPS. (1) The two topologies both inherently introduce 3 dB loss after combining; (2) The current combining topology suffers from impedance mismatch at the two combiner input ports, which causes variant input impedance for the passive VMPS. In practice, the current combining topology is attractive due to its compact area and low loss. It is commonly adopted in the design of active VMPSs, since the VGAs can provide sufficient reverse isolation and thus the reflected voltage waves have negligible impact on former circuit stages. In this work, to avoid the impedance variance at the phase shifter input and thus enhance the phase shift accuracy, the power combining topology is preferred.

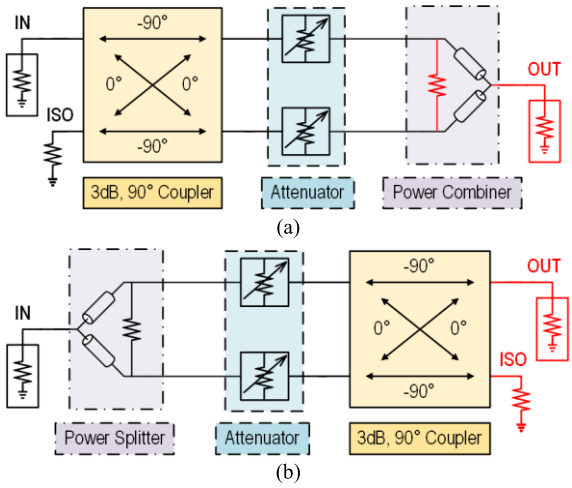


Fig. 8. Block diagrams of the bidirectional VMPS operating in (a) the forward phase shifting mode and (b) the backward phase shifting mode.

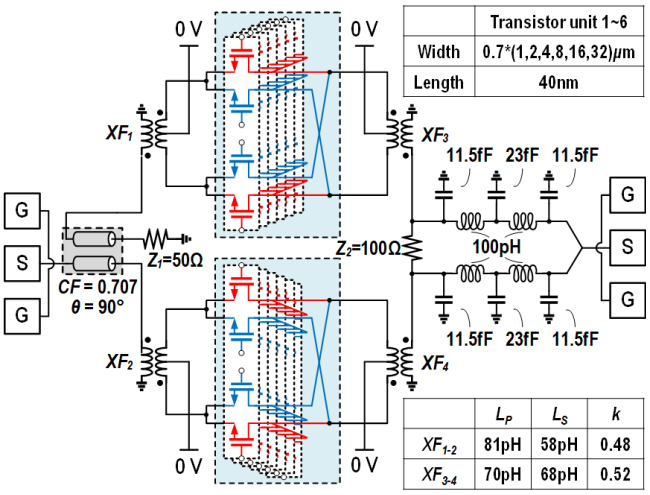


Fig. 9. Schematic of the proposed passive VMPS.

B. Bidirectional Phase Shifting

The passive VMPS can provide bidirectional phase-shift operations, as shown in Fig 8. Note that in this work, the phase-shift operation with the input at the coupler and the output at the combiner (see Fig. 8(a)) is referred to as forward phase shifting mode, and the backward phase shifting mode has a reverse signal flowing direction (see Fig. 8(b)).

For the forward phase shifting mode, the input signal is split to the I and Q signals by the coupler. Then, the I/Q signal is weighted by the digitally controlled attenuator and final summed up by the power combiner. By tuning the attenuation of the I/Q attenuator, the desired phase shift can be generated at the output port. According to the analysis in Section III-A, the forward phase shifting mode will introduce an inherent 3dB loss, with the power dissipated on the isolation resistor in the combiner, as shown in Fig. 8(a).

The backward phase shifting mode is shown in Fig. 8(b). The input signal is split into two identical signals by the power combiner (splitter), and then weighted by the passive attenuators. The 3dB quadrature coupler sums up the two signals and generates the desired phase shift at the output port. Phase tuning is achieved by changing the amplitude ratio of I and Q signals, similar as the forward operation mode. Caused by the coupler-performed combining, the backward operation mode will also introduce an inherent 3dB loss, with the power dissipated on the isolation resistor in the coupler (see Fig. 8(b)). Thus, it can be concluded that the proposed passive VMPS can provide consistent bidirectional phase-shift operation.

IV. Circuit Implementation

The schematic of the proposed passive VMPS is shown in Fig. 9. The couple-line coupler is employed to generate the quadrature signals. It is implemented by vertically coupled microstrip lines using the top two metal layers to reduce loss. The coupling factor (CF) between the two microstrip lines is carefully adjusted to about 0.707, so as to generate broadband quadrature signals. According to the ADS momentum simulation, the stand-alone coupler introduces approximately 0.8 dB insertion loss at 80 GHz for the quadrature signals, and

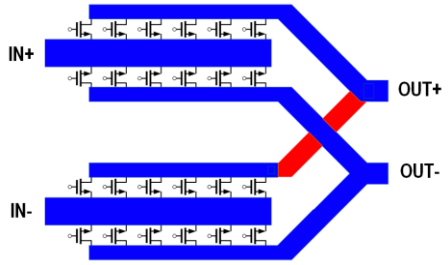


Fig. 10. Floorplan of the transistor array.

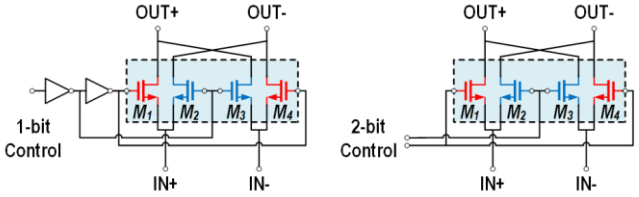


Fig. 11. Schematic of a transistor-array unit with (a) the conventional 1-bit control and (b) the proposed 2-bit control.

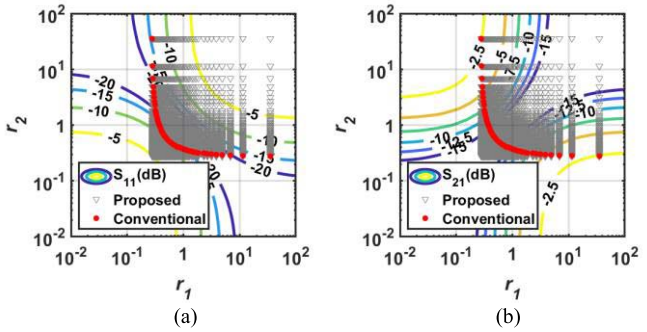


Fig. 12. Simulated gain tuning states presenting in the contour charts of (a) S_{11} and (b) S_{21}, with the conventional and the proposed control methods.

exhibits 50 Ω characteristic impedance. The amplitude and phase errors between the I and Q signals are less than 0.2 dB and 2° across 70–90 GHz, indicating broadband amplitude and phase balance. Following the coupler, two transformer-based baluns XF_1 and XF_2 are utilized for impedance matching and also for the single-ended to differential signal conversions. The simulated insertion loss is 1.2 dB at 80 GHz.

For the design of the digitally controlled X-type attenuator, the total transistor width is first determined. Under the circumstance that Z_L equals to 50 Ω, the total width is tuned to achieve good impedance matching and also ensure low parasitic capacitance. The total width is divided among 6 transistors, with the minimum width of 0.7 μm, as shown in Fig. 9. Note that more transistor units can provide better tuning accuracy, and the number of transistor unit is limited by the minimum transistor size of the technology. The floorplan of the transistor array is shown in Fig. 10. The transistors are placed close to each other and are set to have the same width per finger, so that they will experience similar PVT variations, which is beneficial for ensuring low gain error. Also, the interconnects are implemented by the top two metal lines to reduce loss. The simulated loss of the switch array is 3.8 dB at 80 GHz and drops when frequency increases. The design of the two resonating inductors are absorbed in the former and latter matching transformers.

At the outputs of the I- and Q-path attenuators, the XF_3 and XF_4 are utilized to accomplish impedance matching and perform differential to single-ended signal conversions. A simulated 1.2 dB loss is introduced at 80 GHz. The single-ended I- and Q-path outputs are summed-up by the Wilkinson-like power combiner. As shown in Fig. 9, the two $\lambda/4$ transmission lines in the combiner are accomplished by the lumped capacitors and inductors, based on the lumped model of the transmission line, so as to reduce area. The loss of the combiner is about 0.5 dB at 80 GHz.

In Fig. 11, two control methods of the transistor unit are shown, including the conventional 1-bit control and the proposed 2-bit control. The conventional method utilizes only 1-bit digital signal to control the unit, with one pair of transistors (e.g., M_1 and M_4) turned on and the other (e.g., M_2 and M_3) turned off. Then, the 6 units are controlled by 6 bits and generate 32 phase-invertible gain tuning states (i.e., a total of 64 states). In this case, r_1 and r_2 are dependent on each other and cannot always satisfy $r_1 r_2 = 1$ in different attenuation levels, leading to variant impedance matching. To deal with this issue, the 2-bit control method is proposed, as shown in Fig. 11(b), which provides independent control for the two pairs of transistors. Thus, a more flexible resistance tuning can be achieved by the 6-unit transistor array. Fig. 12 depicts the simulated gain states in the S_{11} and S_{21} contour charts, with the 2-bit control method. A total of 4096 (i.e., 2^{12}) states are available, and by properly setting the 12-bit control codes, it is possible to achieve the target attenuation level while ensuring $r_1 r_2$ close to 1. For each of the 64 phase states, the target attenuation level of the I/Q attenuator is determined by (13), and the related control codes (each 12 bits for I and Q paths) are decided. Therefore, a total of 24 bits are utilized to control the proposed VMPS, with 64 states selected for a 6-bit phase-shift resolution. Note that due to the limited resistance tuning accuracy and flexibility of the transistor array, $r_1 r_2$ close to 1 instead of $r_1 r_2 = 1$ is implemented, causing degradation in phase shift accuracy, but the accuracy is sufficiently high for the 6-bit phase shifter. In Fig. 13, the simulated S_{21} and S_{11} using the conventional 12-bit and the proposed 24-bit control methods are compared. The conventional 12-bit control provides 4096 possible states, and a sub-selection of the states can support accurate 6-bit phase shift, but with relatively high gain variation (i.e., 1 dB) and variant matching performance among the phase states. With the 24-b control, the gain variation can be reduced to only 0.3 dB and a relatively consistent input matching is achieved, thanks to the flexible resistance tuning.

To evaluate the impact of PVT variations, the phase shifter performance versus frequency is simulated under different corners, as shown in Fig. 14. The RMS phase error remains less than 2.7° and the maximum gain error is less than 1.1 dB across 70–90 GHz, implying robust phase shifting performance. Besides, to investigate the performance variation

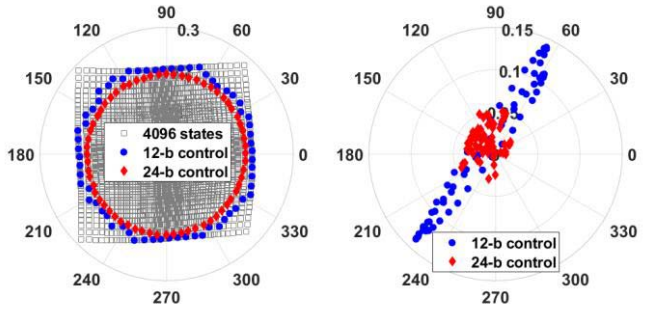


Fig. 13. Simulated (a) S_{21} and (b) S_{11} at 80 GHz, using the conventional and the proposed control methods.

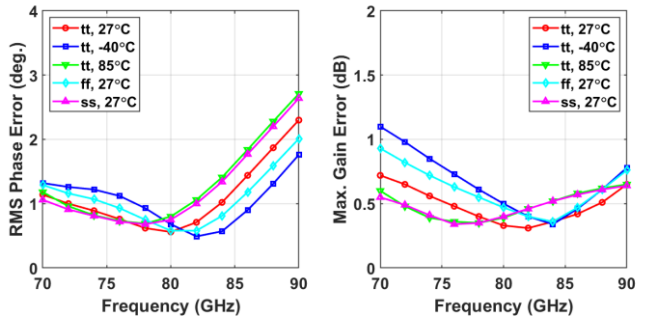


Fig. 14. Simulated (a) RMS phase error and (b) maximum gain error under different corners.

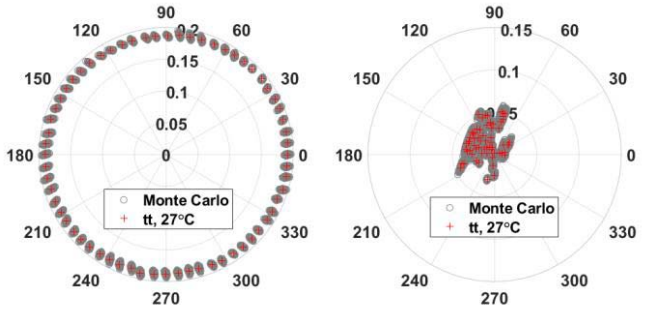


Fig. 15. Monte Carlo results of (a) S_{21} and (b) S_{11} at 80 GHz for all the 64 phase shifting states, each with 200 samples.

in the presence of random variation (including both process and mismatch statistical variations), Monte Carlo simulation is performed for all the 64 phase shifting states at 80 GHz, each with 200 samples. The simulated S_{21} in polar chart are shown in Fig. 15(a). For each state, the gain/phase variation among the samples is less than ± 0.32dB/ $\pm$ 1.35°, which is sufficiently low and tolerable for the proposed 6-bit phase shifter. In Fig. 15(b), S_{11} has negligible variation in the presence of random variation, indicating robust impedance matching.

V. Measurement Results

The passive VMPS prototype is implemented in 40-nm CMOS technology. The micrograph of the chip is shown

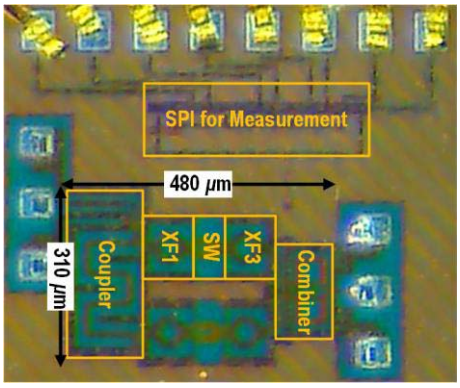


Fig. 16. Microphoto of the passive VMPS (core area: 0.15 mm^2).

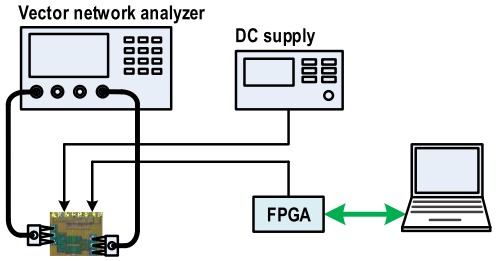


Fig. 17. Block diagram of the measurement setup.

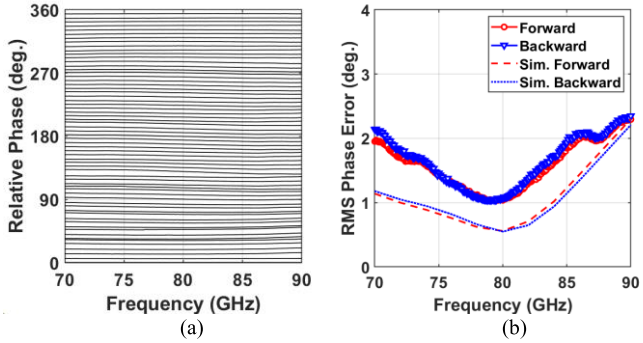


Fig. 18. Measured (a) relative phase (forward mode shown) and (b) RMS phase error of the 64 phase-shift states.

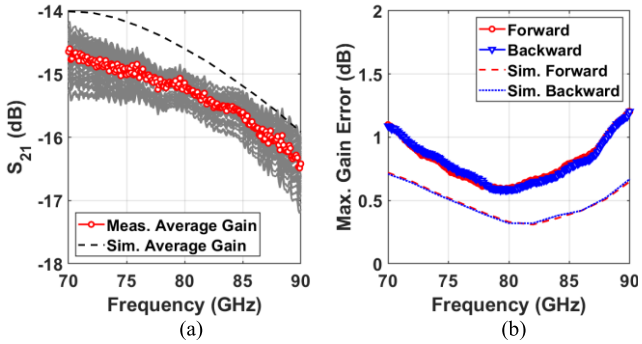
in Fig. 16, with a core chip area of 0.15 mm^2. The chip has been measured on a high-frequency probe station. The measurement setup is shown in Fig. 17. The vector network analyzer and probes operating up to 90 GHz are utilized to measure the S-parameters. Probe-tip calibration is performed by using the short-open-load-through (SOLT) calibration method. The phase state of the chip is automatically controlled by a computer, with the aid of a field-programmable gate array (FPGA).

In Fig. 18(a), the relative phases of the 64 phase-shift states are shown, covering the whole 360° phase-shift range with approximately 5.625° phase-shift step. The RMS phase errors for both the forward and backward operation modes are shown in Fig. 18(b). As depicted, the RMS phase error has a maximum value of 2.4° over the measured 70–90 GHz band, implying broadband and accurate phase-shift operation.

TABLE I
COMPARISON OF THE PRIOR-ART VECTOR-MODULATED PHASE SHIFTERS

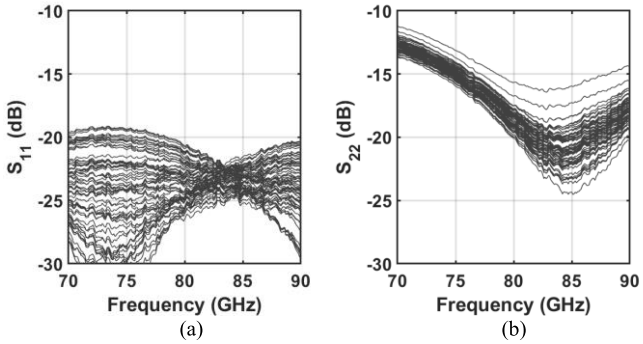
Reference	**This work**	[31]	[30]	[26]	[29]	[34]	[35]	[36]	[20]
Technology	**40-nm CMOS**	65-nm CMOS	40-nm CMOS	0.18-μm CMOS	55-nm BiCMOS	65-nm CMOS	130-nm BiCMOS	130-nm BiCOMS	28-nm CMOS
Gain tuning topology	**X-type attenuator**	X-type attenuator	X-type attenuator	RTA	STA + sign-select	VGA	VGA	VGA	VGA
Combining topology	**Power combining**	Current combining	Power combining	Power combining	Current combining	Current combining	Current combining	Current combining	Current combining
Frequency (GHz)	**70-90**	21-30	57-66	22-26	71-76	2-20	26-28	76-95	80.2-96.8 *
Phase step (°)	**5.625**	0.8	5.625	22.5	5.625	22.5	11.25	11.25	22.5
RMS phase error (°)	**< 2.4**	~ 0.88	N/A	< 1.5	< 2.1	< 1.22	< 4	< 11	< 11.9
Average gain at f_0 (dB)	**-15.1**	12.2**	-11	-15.3	-1	-4.25	-0.5	-4 ***	0.83
Gain variation (dB)	**± 0.6**	± 0.5	± 1.5	± 0.8	± 0.8 ***	± 0.75	± 0.5 ***	± 2.5 ***	± 2.3 ***
Frequency -independent control	**Yes**	No	No	Yes	Yes	Yes	Yes	Yes	Yes
P_{DC} (mW)	**0**	0	0	0	12.8	92	23	28	21.6
Core chip area (mm^2)	**0.15**	N/A	N/A	0.31	0.38	2.16 ****	0.48	N/A	0.06

* 3dB bandwidth. **Including amplifier gain. *** Estimated from figures. **** Chip area including pads.



(a) (b)

Fig. 19. Measured (a) S_{21} (forward mode shown) and (b) maximum gain error of the 64 phase-shift states.



(a) (b)

Fig. 20. Measured (a) S_{11} and (b) S_{22} of the 64 phase-shift states.

Besides, the RMS phase errors are similar for both the forward and backward operation modes, ensuring relatively consistent performance for bidirectional operation. It is worth noting that the control codes for the depicted 64 states are consistent over the measured band. Any frequency-dependent compensations or look-up tables are not necessary.

Fig. 19(a) shows the measured S_{21} of the 64 phase-shift states. The average insertion loss is 15.1 dB at 80 GHz. The amplitude response is relatively flat with an average slope of 0.1 dB/GHz, and thus the phase shifter can be adopted for various applications in the 70–90 GHz band. In Fig. 19(b), the maximum gain errors among the 64 phase-shift states for both the forward and backward operation modes are shown. As revealed, the maximum gain error remains less than ± 0.6 dB across the 70–90 GHz band, which can greatly ease the phase and amplitude calibrations of the phased-array system.

In Fig. 20, the measured S_{11} and S_{22} for all the 64 states are depicted, with a maximum value of −19 dB and −11 dB across the 70–90 GHz band, respectively.

The polar chart in Fig. 21 depicts the measured S_{21} of the 64 phase-shift states at 70/80/90 GHz. The phase of S_{21} in the polar chart has been normalized, in order to present the results more clearly. As indicated, the proposed VMPS can provide relatively consistent phase-shift performance over the whole 70–90 GHz band, using frequency-independent control codes.

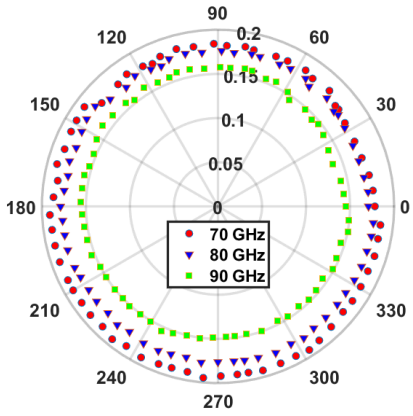


Fig. 21. Measured S_{21} of the 64 states in polar chart at 70/80/90 GHz.

In Table I, the performance of the proposed passive VMPS is summarized and compared with the prior-art VMPSs, including passive and active designs. The insertion loss of this VMPS is relatively high, due to the use of all-passive building

blocks and the high operation frequency. Nevertheless, the zero DC power consumption makes this VMPS attractive for large-scaled low-power phased-array systems, compared with the active VMPSs utilizing two VGAs for gain tuning and amplification. Benefiting from the proposed 2-bit control method, this VMPS supports accurate phase tuning with 5.625° phase step and only introduces low gain error, over the whole 70–90 GHz band. Moreover, the frequency-independent control codes can be directly applied at different frequencies in this band, without the need of frequency-dependent compensations or look-up tables.

VI. Conclusion

In this paper, the analysis and design of the bidirectional passive VMPS are presented. For the gain tuning block, the derivations of its transmission and reflection behaviors, and the modeling of gain variations are carried out, guiding the optimizations. The current and power combining topologies are compared, implying that the power combining topology is more suitable for the passive VMPS. The analysis of the forward and backward phase-shift modes proves that the passive VMPS is capable of providing consistent bidirectional phase-shift operation. The proposed passive VMPS is fabricated in 40-nm CMOS technology. It achieves 6-bit phase-shift resolution with low RMS phase error (i.e., $< 2.4°$) and low gain error (i.e., $\pm$ 0.6 dB) across the whole 70–90 GHz band.

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