A 300-GHz Transmitter Front End With −4.1-dBm Peak Output Power for Sub-THz Communication Using 130-nm SiGe BiCMOS Technology

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***Abstract*— This article presents a compact 300-GHz transmitter front end manufactured in a 130-nm SiGe BiCMOS process. The transmitter consists of a 240-GHz amplifier multiplier chain (AMC) and a modified 300-GHz Gilbert mixer. Limited by the space between top two thick metal layers of the SiGe process, the coupling coefficient between the coils, which form a transformer-based balun, is usually small at subterahertz (THz). Therefore, the vertical or horizontal coupling single-turn transformer-based balun will exhibit large insertion loss at around 300 GHz. In this work, a self-shielded Marchand balun (SSMB) with an enhancement to the coupling coefficient is proposed, which is realized by a novel multilayer metal topology with self-shielded coupling (SSC). The AMC is composed of a 120-GHz frequency doubler, a 120-GHz two-stage power amplifier (PA), and a two-way power synthesis balanced frequency doubler. This AMC exhibits a measured peak output power of 5.5 dBm at 252 GHz, with 48-GHz 3-dB bandwidth from 212 to 260 GHz. The transmitter chip achieves a maximum output power of −4.1 dBm at 300 GHz and delivers an output power better than −10 dBm from 270 to 315 GHz. Over the 30-GHz 3-dB bandwidth from 280 to 310 GHz, the transmitter shows a maximum OP_{1dB} of −6.5 dBm at 296 GHz, a peak conversion gain of −11.2 dB at 298 GHz, and a local oscillator (LO)-to-RF leakage rejection better than 40 dB, with only 300-mW dc power consumption. Compared with other state of the arts, the transmitter exhibits a comparable output power among silicon-based transmitters near 300 GHz.**

***Index Terms*— Amplifier multiplier chain (AMC), power combining, self-shielded Marchand balun (SSMB), subterahertz (THz) transmitter, 300 GHz.**

I. Introduction

As WIRELESS technology advances, wireless communication is facing a new data rate challenge in the level of terabytes. Compared to microwave and millimeter-wave (mm-wave) communication, terahertz (THz) communication has a larger transmission bandwidth and transmission rate because of a higher carrier frequency and richer spectrum resources. Besides, the IEEE 802.15.3d standard reported in October 2017 defines 32 2.16-GHz-wide channels between 252 and 325 GHz (300-GHz band) for up to 100-Gb/s data rate [1]. III–V group compound semiconductor technology has traditionally been adopted for THz communication, but recent advances in silicon-based technologies have resulted in SiGe heterojunction bipolar transistors (HBTs) with cutoff frequency f_T approaching 300 GHz [2]. This has made silicon-based process a good low-cost alternative for III–V semiconductors [3], [4]. However, due to the limited maximum oscillation frequency (f_{max}) of transistors and low efficiency of passive components, the generation of a milliwatt-level local oscillator (LO) signal based on existing silicon processes for sub-THz communication system [5] remains a challenge. Studies on silicon-based amplifiers at frequencies above 200 GHz have shown remarkable advancement in the past few years [6]–[11]. At present, the reported maximum output power of sub-THz silicon-based power amplifier (PA) is 13.5 dBm at 240 GHz (above 200 GHz) [11]. However, it is still a challenge to deliver milliwatt-level output power using silicon-based processes at the 300-GHz band.

At sub-THz, the RF ground plane would introduce seriously parasitic inductance, which will deteriorate the stability of the transmitter. Besides, the connection of bypass decoupling capacitors would introduce extra parasitic signal paths to the ground, which will decrease the power-handling capability besides stability issues. Thus, the differential topology is usually adopted for sub-THz circuit design to take advantage of the virtual ground [11], [12]. For sub-THz differential circuits, the single-ended-to-differential conversion is an extremely critical component due to the limited active gain. In the microwave and mm-wave bands, the integrated single-turn transformer-based balun is a compact and low-loss solution. However, at the sub-THz band, the size of the transformer is relatively small, which will lead to self-resonance and large insertion loss.

The topology of transmitters at sub-THz frequency band can be broadly divided into two categories, which are directly mixing structure and subharmonic mixing architecture.

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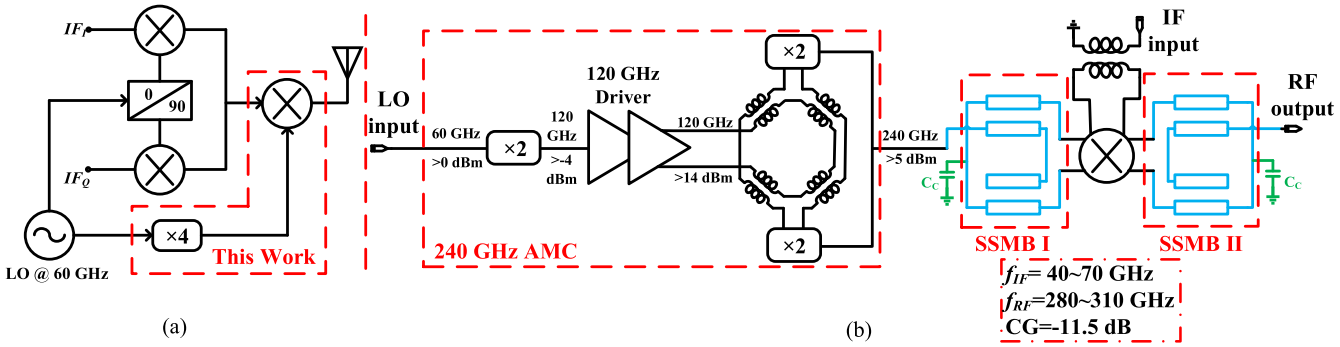

Fig. 1. (a) Block diagram of sliding-IF architecture and (b) proposed 300-GHz transmitter front end.

Between them, the transmitters of the reported direct modulation scheme often adopt a heterodyne [12]–[14] or zero-intermediate frequency (IF) system architecture [15]–[21]. A 0.8-dBm saturated output power over 200 GHz is achieved in [19]. Rodríguez-Vázquez *et al.* [20], [21] reported a 1-m LO-tunable wireless link with a set of fundamentally operated and fully packaged Tx/Rx direct-conversion IQ RF front-end modules. For the direct frequency modulation systems, high LO drive power and dc power consumption are usually required. There have been several demonstrations of frequency multiplier chains (FMCs) above 200 GHz reported in the literature [22]–[26]. An alternative solution is to adopt the subharmonic mixing architecture [27], [28]. As the THz signal generation block is the most power-hungry portion of most THz transceivers, a sliding-IF architecture is an effective solution to ease the difficulty of LO generation. The sliding-IF architecture is a heterodyne architecture, where the LO frequencies track each other, so that they can be generated from the same source, as shown in Fig. 1. In this article, we target at mixing the signal up to 300 GHz by using a lower LO frequency. For this purpose, we set the LO frequency at 60 GHz, and the baseband is first modulated up to 60 GHz with an IQ-mixer. Then it is further upconverted to 300 GHz by effectively multiplied with a 240-GHz LO signal. With this frequency allocation, the image signal is located at 0.5–0.7 times the RF frequency and can be easily rejected by the band-selection filter or on-chip antenna.

In this work, we present a 300-GHz SiGe THz front end targeted at channels 14–26 (280.8–308.88 GHz) of the IEEE 802.15.3d standard. The proposed integrated 300-GHz transmitter front end is comprised of a 240-GHz amplifier multiplier chain (AMC) and a modified 300-GHz Gilbert mixer. The 240-GHz AMC achieves a measured peak output power of 5.5 dBm at 248 and 48-GHz 3-dB bandwidth from 212 to 260 GHz, which is sufficient to drive the succeeding 300-GHz modified Gilbert mixer. Besides, a stacked Marchand balun with a novel multilayer metal self-shielded coupling (SSC) structure is proposed for single-ended-to-differential conversion at sub-THz band. The transmitter demonstrates a measured peak output power of -4.1 dBm at 300 GHz, a maximum $\mathrm{OP}_{1\,\mathrm{dB}}$ of -6.5 dBm at 296 GHz, a conversion gain of -11.2 dB at 298 GHz, and an LO-to-RF leakage rejection better than 40 dB. The proposed system has the potential to be used in the BPSK modulation communication system. It can also act as a front end and can be integrated with a V-band transmitter to form a 300-GHz heterodyne architecture communication system.

This article is organized as follows. Section II discusses the adopted 130-nm SiGe BiCMOS technology briefly. Section III introduces the proposed architecture of this 300-GHz transmitter. Section IV analyzes the proposed Marchand balun based on coupled lines and the proposed multilayer metal SSC method. Section V discusses the circuit details, including a 240-GHz AMC and a modified 300-GHz Gilbert mixer. Section VI presents the measurement method and the measurement results. Section VII draws conclusions and makes comparisons with state-of-the-art integrated transmitters at the sub-THz band.

II. 130-nm SiGe BiCMOS Technology

The THz transmitter developed in this work is based on IHP's 130-nm SiGe BiCMOS technology. The adopted technology provides high-performance HBTs that exhibit $f_t/f_{\max}$ of 300/500 GHz and breakdown voltages of $\mathrm{BV_{CEO}} = 1.7$ V and $\mathrm{BV_{CBO}} = 4.8$ V, respectively. Considering the parasitic of transistor's peripheral connection, the simulated $f_{\max}$ of a single transistor with the size of $8 \times 0.07 \times 0.9\ \mu\mathrm{m}^2$ is around 320 GHz. The process provides seven metal layers that include two low-loss thick metal layers and five thin metal layers. The metal layers enable the customized realization of high-quality inductors, metal–oxide–metal (MOM) capacitors, and transmission lines, such as microstrip and coplanar lines. The lower metal layers can be utilized as ground planes, dc feed lines, and metal interconnects. In addition, the process offers polysilicon resistors and high-quality-factor metal–insulator–metal (MIM) capacitors.

The MIM capacitor provided by this process has a low Q-factor in the sub-THz frequency band and its self-resonance frequency is close to 200 GHz. Therefore, customized MOM capacitors that composed of multilayer metals and oxide are devised and utilized as dc blocks in the matching networks (see Fig. 2). The MOM capacitors have a higher resonant frequency and relatively lower insertion loss compared with MIM capacitors at around 300 GHz.

III. Transmitter Architecture

The block diagram of this 300-GHz transmitter designed for 300-GHz wireless links is shown in Fig. 1. For this transmitter,

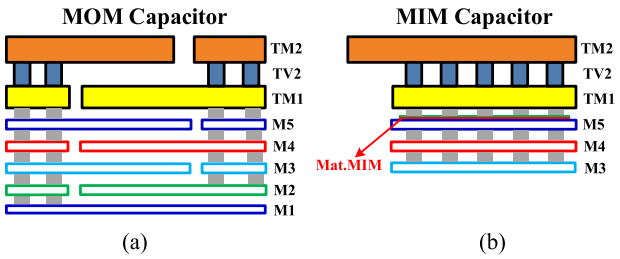

Fig. 2. Layout of (a) MOM capacitor and (b) MIM capacitor.

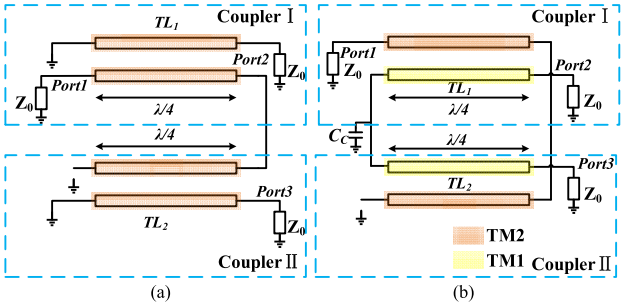

Fig. 3. Equivalent schematic of (a) ideal Marchand balun and (b) modified Marchand balun with C_C.

the IF (f_{IF}) is from 40 to 70 GHz, and the output sub-THz signal's frequency range is from 280 to 310 GHz (f_{RF}). The ×4 multiplier chain consists of a 120-GHz doubler, a 120-GHz driver, and a 240-GHz doubler. To enhance LO driving power, the output stage of the LO chain adopts a power-combining structure with two doubler cells. The two-stage 120-GHz gain-boosting driver can supply sufficient output power to drive the 240-GHz doubler. The upconversion mixer is based on the Gilbert cell, but the differential pair at the IF input end is abandoned and replaced by a transformer-based balun. The LO input termination and RF output termination are both matched with the proposed self-shielded Marchand balun (SSMB).

IV. Analysis of the SSMB

A. Marchand Balun Analysis

Transformer-based baluns are widely used for single-ended-to-differential conversion due to its capability of achieving impedance matching with moderate chip size. However, the dimension of the balun decreases rapidly as the targeted frequency increases, which makes the fabrication extremely difficult. Meanwhile, the decreasing mutual coupling factor of the transformer will increase its insertion loss at the sub-THz frequency band. Fortunately, the Marchand balun is a better substitute at the sub-THz band. Several works have been proposed to realize the Marchand balun at mm-wave and sub-THz band [29]–[32].

For an ideal model of a compact backward-wave coupler, the electrical length of the coupled line is $\lambda/4$, and the scattering matrix of the four-port couplers with infinite directivity and coupling factor k is given by (1) according to [29].

Fig. 3(a) shows the structure of a traditional Marchand balun, which is composed of two cascaded backward-wave couplers. The S matrix of the Marchand balun as shown in Fig. 3(a) can be calculated by considering the S matrix of the two identical backward-wave couplers and can be expressed as follows [29], [30]:

$$[S]_{\mathrm{coupler}} = \begin{bmatrix} 0 & -j\sqrt{1-k^2} & k & 0 \\ -j\sqrt{1-k^2} & 0 & 0 & k \\ k & 0 & 0 & -j\sqrt{1-k^2} \\ 0 & k & -j\sqrt{1-k^2} & 0 \end{bmatrix} \tag{1}$$

$$[S]_M = \begin{bmatrix} \frac{1-3k^2}{1+k^2} & j\frac{2k\sqrt{1-k^2}}{1+k^2} & -j\frac{2k\sqrt{1-k^2}}{1+k^2} \\ j\frac{2k\sqrt{1-k^2}}{1+k^2} & \frac{1-k^2}{1+k^2} & \frac{2k^2}{1+k^2} \\ -j\frac{2k\sqrt{1-k^2}}{1+k^2} & \frac{2k^2}{1+k^2} & \frac{1-k^2}{1+k^2} \end{bmatrix}. \tag{2}$$

Due to the multilayer metal characteristics of the silicon-based process, the Marchand balun can also be realized by the vertical coupling of the top two thick metal layers. For the stacked balun made of the top two thick metal layers, the short end of the two couplers in Fig. 3(a) can be connected together and RF-grounded by a capacitor C_C [see in Fig. 3(b)]. The balance performance of the Marchand balun can be improved by the capacitor C_C, and the supply voltage can be fed at this common node, which will also result in a compact layout design.

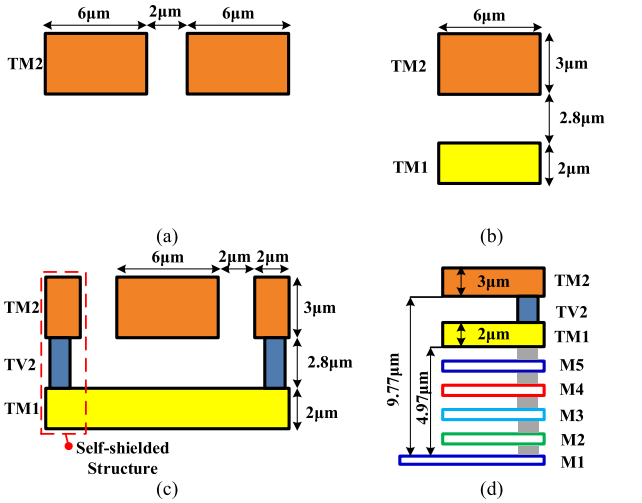

Fig. 4. Cross-sectional of (a) coplaner coupled line, (b) stacked coupled line, (c) proposed stacked coupled line with self-shielded structure, and (d) metal layer of the process.

B. Coupled Line Analysis

For the Marchand balun, it is important to design a reliable coupling transmission line with high performance. The cross-sectional view of different quarter-wavelength coupled lines is shown in Fig. 4. From the above analysis, a coupling factor of −4.8 dB is required for an ideal Marchand balun composed of $\lambda/4$ coupled lines. Actually, the required coupling factor

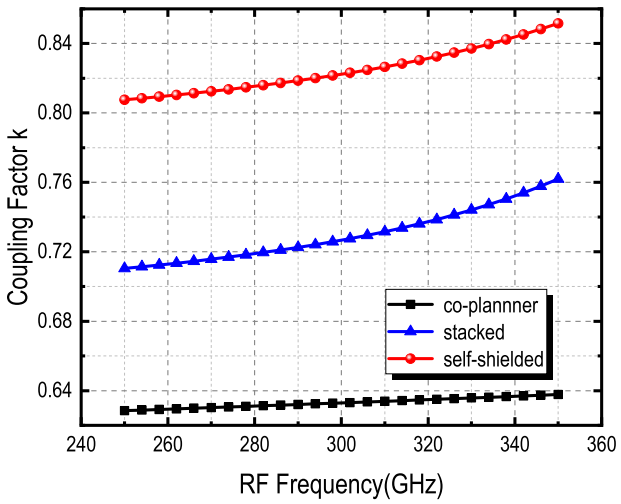

Fig. 5. Simulated coupling factor of the three types of $\lambda/4$ coupled lines.

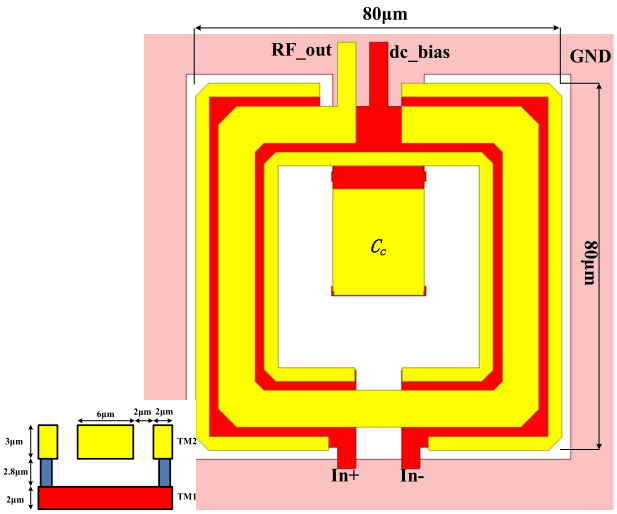

Fig. 6. Layout top view of the proposed SSMB II at RF port of the mixer.

is also concerned about load terminations and the electrical length of coupled line. When the balun's load terminations changes from Z_0 to Z_L, the transmission parameter S_{21} of an ideal Marchand balun composed of $\lambda/4$ coupled lines can be changed to [29]

$$S_{21} = S_{31} = j\frac{2k\sqrt{1-k^2}\sqrt{\frac{Z_L}{Z_0}}}{1+k^2\left(2\frac{Z_L}{Z_0}-1\right)}. \tag{3}$$

To achieve optimum power transfer of -3 dB at each port, the needed coupling factor can be estimated by

$$k = \frac{1}{\sqrt{2\frac{Z_L}{Z_0}+1}}. \tag{4}$$

Considering the impedance matching, for example, the differential output impedance at mixer RF port is $(14.2-j\times 21.67)\ \Omega$ and the load impedance is 50 Ω, a coupling factor of 0.86 is required. In Fig. 5, the coupling factor of three types of $\lambda/4$ coupled lines is compared. According to the simulation results, the proposed self-shielded coupled line (SSCL) shows a better coupling factor. For the coplanar coupled line, the low coupling factor of 0.62 will cause 3-dB extra insertion loss without other matching networks.

Apart from the coupling factor, the transmission mode of the coupled line should be concerned. The scattering matrix in (1) is based on a TEM-type backward-wave coupler. Considering a quasi-TEM type coupler such as a microstrip line-based coupler, the phase velocities of even and odd modes are unequal ($\beta_e \neq \beta_o$). Also, some of the electronic field components will occur in the propagation direction, which means that transmission power leaks into medium. An effective solution to compensate for this difference is to design coupled line with different widths.

In this work, the SSCL is proposed, as shown in Fig. 4(c). This self-shielded structure makes broadside coupling and edge coupling existing at the same time compared with other coupled lines, which increases the total coupling factor dramatically, as shown in Fig. 5. Finally, the proposed SSCL achieves a coupling factor of over 0.8 and makes the low output impedance easily matched to the 50-Ω load. Besides, the proposed structure also compensates for the difference of phase velocities and degrades the electronic field component in the propagation direction. Compared with the stacked coupled line, the insertion loss is decreased by using the proposed SSC structure.

C. Self-Shielded Marchand Balun Design

In this design, a compact stacked Marchand balun based on the SSCL is proposed for LO and RF matching in the mixer block. The top view of SSMB II at RF port in the mixer is shown in Fig. 6. The coupling factor of the coupled line is 0.83 and it is close to the demand of output impedance matching $[(14.2-j\times 21.67)\ \Omega]$ from the previous analysis. $\lambda/4$ is about 125 μm at the working frequency in this medium and a balun with a dimension of 80 μm × 80 μm can well match the output impedance to 50 Ω. A high-quality-factor MOM capacitor C_C is introduced at the common node of the secondary coil to improve the phase and amplitude balance performance of the Marchand balun. Also, the dc voltage can be fed through the virtual ground node. To ensure RF grounding, the capacitance should be over 150 fF. However, if the capacitance of C_C is too large, it will take a large area and make the realization of layout difficult. Finally, an optimized C_C of 200 fF is selected, which achieves an amplitude imbalance of less than 1 dB and a phase imbalance of less than 4° from 250 to 330 GHz, as the simulated results shown in Fig. 7. The electromagnetic (EM) simulation results show that the output balun matches the differential output impedance of $(14.2-j\times 21.67)\ \Omega$ to the single-end 50 Ω load with about 1.5 dB insertion loss. The input balun SSMB I can be designed in a similar method, of which the insertion loss is about 1.4 dB. This is a much better performance compared with the Marchand balun based on coupled lines in Fig. 4(a) and (b). Compared with other matching networks realized by stacked or coplaner balun at 300 GHz, the insertion loss is improved by more than 1.2 dB, as shown in Fig. 8.

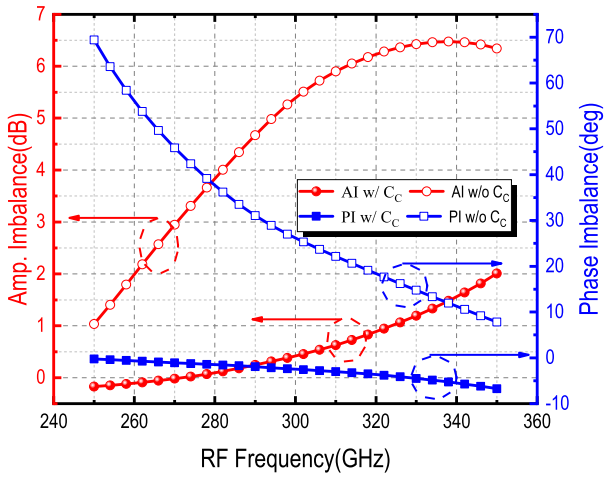

Fig. 7. Amplitude and phase imbalance of the SSMB with and without capacitor C_C.

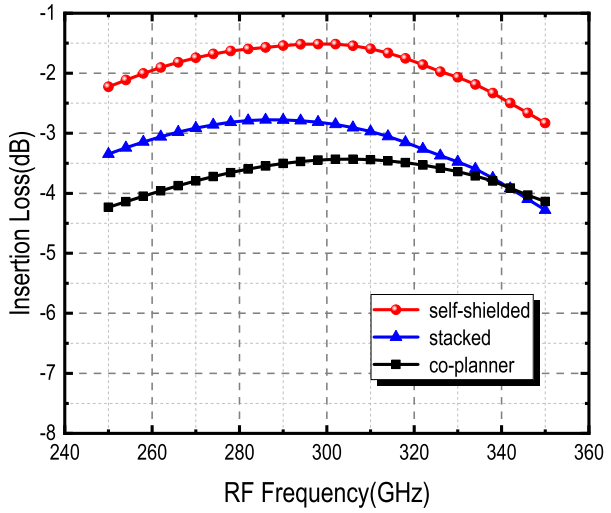

Fig. 8. Simulated insertion loss of Marchand baluns based on three types of coupled lines.

V. Circuit Design

In this 300-GHz transmitter, the mixer's output power determines the wireless link distance, and LO-to-RF isolation limits the transmitter functionality. Besides, the AMC's driving ability limits the transmitter's conversion gain.

A. Mixer Design

The schematic of the 300-GHz mixer based on modified Gilbert topology is shown in Fig. 9. Because of insufficient maximum available gain of the active devices and high insertion loss of the passive components, it is a challenge to design a 300-GHz PA with sufficient output power and wide bandwidth. Therefore, the 300-GHz transmitter is designed without a PA at the output. As the operating frequency is close to the transistor's cutoff frequency, the differential pair transistors below the Gilbert core in the traditional structure become lossy and limit the linearity of the mixer. As a result, a modified Gilbert topology without the g_m stage is adopted,

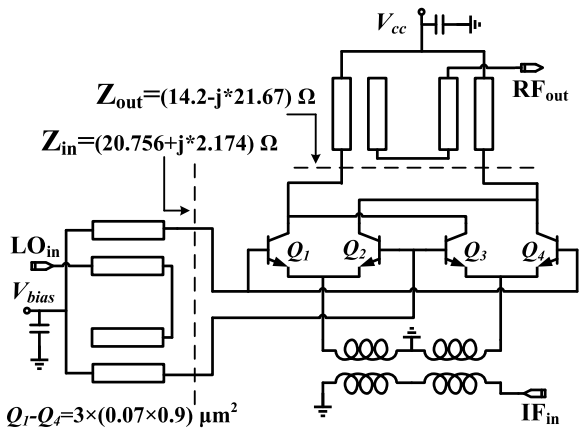

Fig. 9. Schematic of the 300-GHz modified Gilbert mixer.

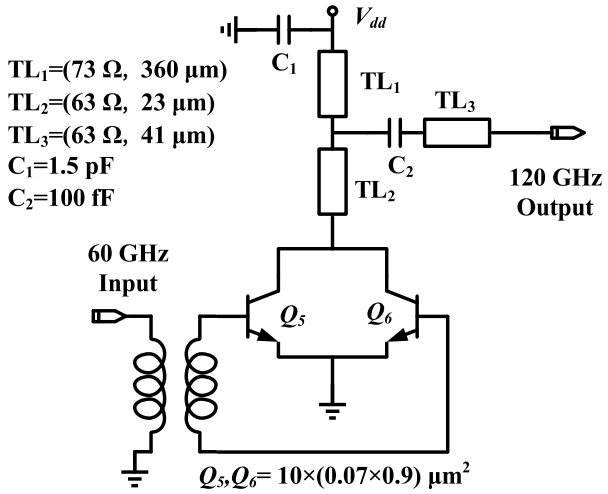

Fig. 10. Schematic of the 120-GHz doubler.

as shown in Fig. 9. In the modified mixer, the g_m stage is replaced by a transformer-based balun, and the balun also acts as the matching network for the single-ended 60-GHz IF input port. The LO input and RF output network utilize the proposed SSMB for impedance matching, which realizes a single-ended-to-differential conversion with about 1.4- and 1.5-dB insertion loss, respectively. Benefiting from the proposed SSMB, the conversion gain of the mixer has increased by more than 2 dB compared with the matching network realized by the traditional vertical or horizontal coupling Marchand balun.

The size of the transistors (Q_1–Q_4) used in the mixing core has been optimized to make a tradeoff between conversion gain and linearity. Transistors of smaller size will obtain higher conversion gain with lower LO-drive power requirement, while it will lead to a lower $OP_{1\,dB}$. To minimize the LO power generation requirements (which is limited by the output power of the AMC), the transistors with the size of $Ae = 3 \times (0.07 \times 0.9)\ \mu m^2$ were selected to achieve better output power and also keep the 5-dBm LO input drive power satisfying the requirements for measurement.

The mixer achieves a simulated conversion gain of −10.5 dB at 300 GHz. The saturated output power is simulated

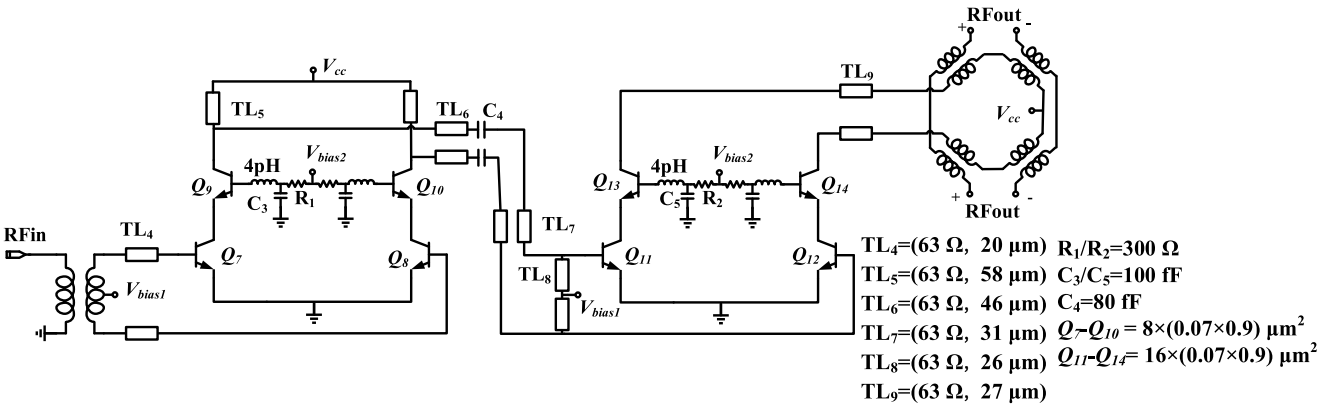

Fig. 11. Schematic of the 120-GHz driver.

to be −3.5 dBm, and the $OP_{1\,dB}$ is simulated to be −5.3 dBm at 300 GHz.

B. 240-GHz LO Chain

The 240-GHz LO chain adopts the power-combining architecture and consists of a 120-GHz doubler, a 120-GHz driver, and a 240-GHz doubler, as shown in Fig. 1. The 120-GHz driver is designed based on a fully differential cascode topology. It is designed to deliver over 14-dBm output power to drive the succeeding 240-GHz doubler cores. The 240-GHz doubler consists of two doubler cells. A one-to-two-way differential power splitter is introduced between the 120-GHz driver amplifier and the 240-GHz doublers to deliver RF power to two doubler cells, which also plays the role of impedance matching.

1) 120-GHz Doubler Design: The 120-GHz doubler is designed using two common-emitter transistors, as shown in Fig. 10. It is a common way to use input second-harmonic reflectors to form the reflector at the base, which can obtain a higher second-harmonic power in push–push topology doubler. However, the resonator will restrain the 3-dB bandwidth. Besides, the output power of the 120-GHz doubler without second-harmonic reflector is sufficient to drive the succeeding 120-GHz driver amplifier. Thus, the input resonator is abandoned in this design. The input signal is applied through a symmetrical single-coil transformer using the top two thick metal layers. The output impedance is matched by a high-pass network, which consists of transmission lines TL_1, TL_2, and TL_3 and capacitor C_2. The 120-GHz doubler delivers about −4-dBm output power with 0-dBm input power.

2) 120-GHz Driver Design: The 120-GHz driver employs the cascode topology due to its higher gain and better isolation, as shown in Fig. 11. The driver is introduced between the two doublers to provide sufficient drive power and suppress the spurious signals simultaneously. A transformer-based balun with a bypass MIM capacitor grounded at the center tap of the secondary coil is introduced for input impedance matching. The interstage match network consists of transmission lines TL_6, TL_7, and TL_8 and capacitor C_4. A small inductance is carefully designed at the base of the common base stage and is used to provide a gain boost under the premise of ensuring

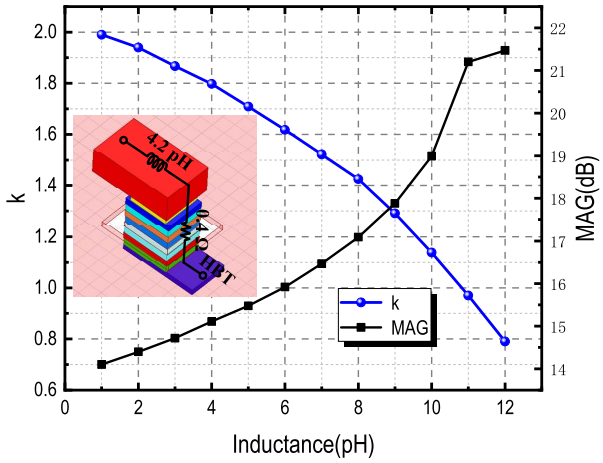

Fig. 12. 3-D model of the via transition designed for the amplifying gm-boosting inductor.

absolute stability of the driver [34]. To verify the effect of this base inductor, the maximum available gain and the stability factor of one-stage cascode amplifier are simulated at 120 GHz as the introduced inductance changes. The base inductance is chosen to be about 4 pH and the simulated small gain increases about 1 dB. The realization of the inductor is obtained by a transition from M1 to TM2, as shown in Fig. 12. This tiny inductor is designed using a metal-vias connection array between M1 and TM2 with a series resistance of 0.4 Ω. The matching network between the 120-GHz drive amplifier and the 240-GHz doubler is a transformer-based two-way power splitter, as shown in Fig. 13. The center tap of the secondary coil is grounded using an MOM capacitor formed by the lower metal layers M1–M5. The insertion loss of the power divider is only 2 dB with each path delivering about 9-dBm output power to the succeeding 240-GHz doubler.

3) 240-GHz Doubler Design: The 240-GHz doubler employs a current-combining configuration to enhance the output power, as shown in Fig. 14. Each doubler cell adopts a common-emitter topology with second-harmonic resonators at $2f_0$. Shopov *et al.* [5] and Wu *et al.* [23] have proved that the harmonic components of collector current are a function of conduction angle and determined by the input power level

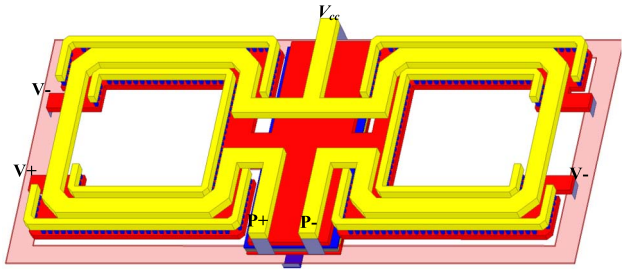

Fig. 13. 3-D model of the transformer-based power splitter.

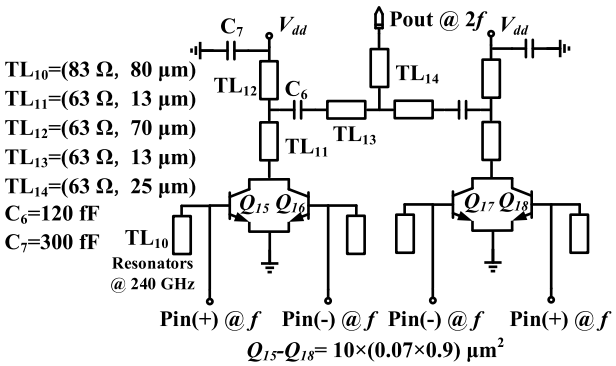

Fig. 14. Schematic of the 240-GHz doubler.

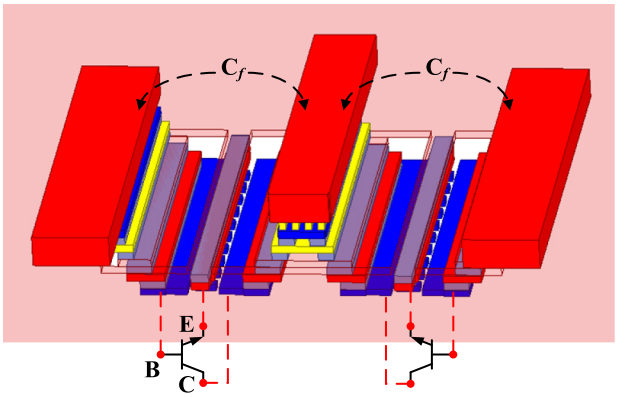

Fig. 15. Proposed optimal transistor layout with stair-like interconnection utilized.

and base bias point. Based on the available fundamental drive power (9 dBm) and harmonic-balance simulation of the doubler, the device size of Ae = 10 × (0.07 × 0.9) μm^2 is chosen for higher output power with a base bias voltage of 0.6 V and a supply voltage of 1.6 V. The layout of the doubler core is also optimized for better performance at the sub-THz band. The interconnection metal vias are required to connect the top thick metal layer TM2 to the transistor's output interface (metal layer M1). However, two parallel vertical metal vias (M1 to TM2) will suffer from serious coupling at the sub-THz frequency band, which is expressed by a feedback capacitance C_f, as shown in Fig. 15. The Miller effect caused by C_f will deteriorate the output power (see in Fig. 15). In this design, a stair-like interconnection [35] is utilized, as shown in Fig. 15. With this method, the coupling capacitance C_f is

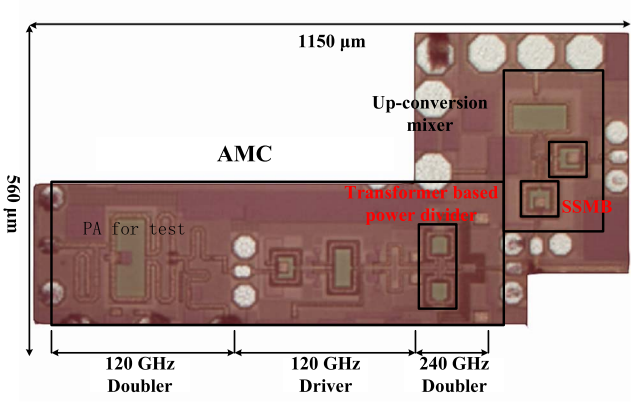

Fig. 16. Die photograph of the proposed transmitter.

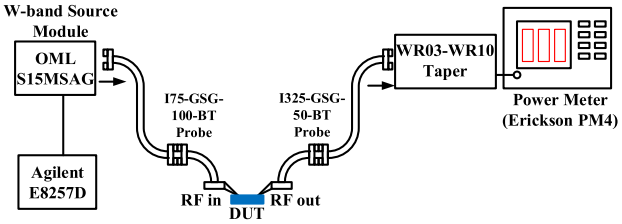

Fig. 17. Measurement setup of the LO chain.

reduced from 13.6 to 8.1 fF at 300 GHz when compared to the traditional straight-up layout.

For a compact layout design, an open stub rather than a short stub is used as the second-harmonic reflector to enhance the second-harmonic's output power. With the $\lambda/4$ open stub, the output power of the second harmonic drops fast when the working frequency is higher than the frequency point corresponding to the maximum second-harmonic output power [23]. The electrical length of the open stub is optimized to make a tradeoff between peak output power and bandwidth. Through EM simulation, the electrical length of the reflector is set to be 65° in this design. In order to make the layout more compact, lower metal layers M1–M5 are used to implement the reflectors. The output is combined and matched to a 50-Ω impedance shown in Fig. 14. The output network is composed of transmission lines TL_{11}, TL_{12}, TL_{13}, and TL_{14} and capacitor C_6 enabling a high-pass characteristic for better fundamental frequency suppression. Since the low quality factor of the MIM capacitor will lead to self-resonance at the sub-THz band, the bypass capacitor C_7 adopts an MOM capacitor as an alternative.

The multiplier chain achieves a simulated peak output power of 6.5 dBm at 238- and 55-GHz 3-dB bandwidth from 211 to 266 GHz.

VI. Measurement Results

The transmitter system is fabricated in the IHP 130-nm SiGe BiCMOS process. This technology provides seven metal layers for routing, where the top two thick metal layers can be used for the low-loss transmission lines. The die micrograph of the 300-GHz transmitter is shown in Fig. 16. RF pads are inserted

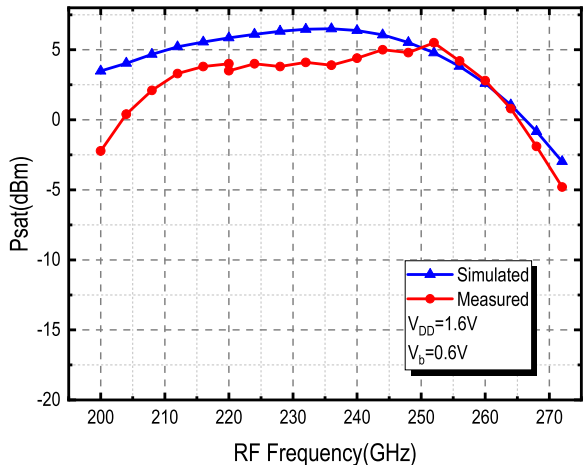

Fig. 18. Simulated and measured output power versus frequency of the multiplier chain.

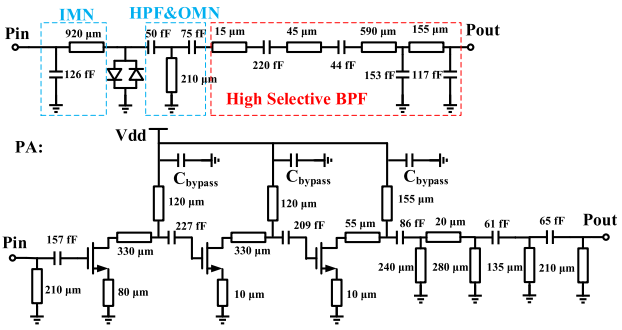

Fig. 19. Schematic of the 60-GHz frequency tripler and the following PA.

between every two blocks for the performance demonstration of each block. For instance, if we want to measure the output power of the 240-GHz multiplier chain, we use the New Wave Ezlaze II laser to cut off the output of the previous 240-GHz doubler stage and the input of the next 300-GHz mixer stage, and then, we can measure the performance of the 240-GHz multiplier chain easily. The chip is on-wafer measured with wires bonded to dc pads for dc supply.

A. Measurement of the 240-GHz AMC

For the 240-GHz multiplier chain test, the measurement setup is shown in Fig. 17. The input power was generated by an Agilent E8257D signal generator and a *W*-band OML S15MS-AG multiplier by a six-source module. Due to the lack of wideband probes and waveguides that cover the frequency band from 200 to 300 GHz, the output power was measured by the Erickson PM4 power meter in the frequency band 140–220 and 220–325 GHz, respectively. In the output path, the loss of WR03 (WR05) Infinity probe and tapers can be obtained from the datasheet, and the loss of WR03 (WR05) the S-bend waveguide is measured by the Keysight vector network analyzer with extenders. The deembedded output power versus input frequency is shown in Fig. 18. The multiplier chain achieves a measured peak output power of 5.5 dBm at 252 GHz with a 3-dB bandwidth of 48 GHz from 212 to 260 GHz. Compared with other state of the arts shown in Table I, the proposed AMC demonstrates good output power and operating bandwidth performance.

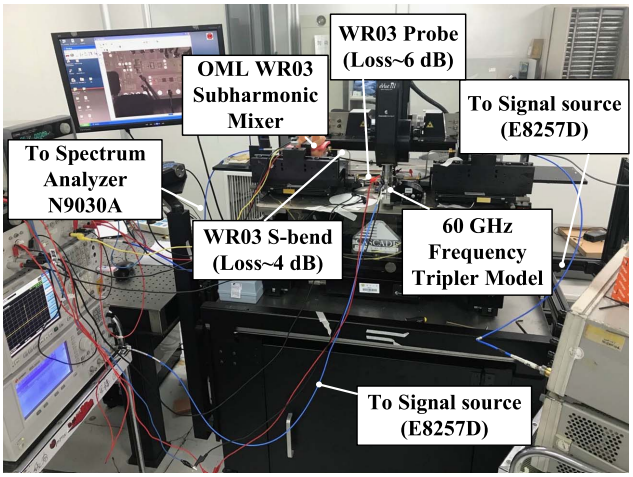

Fig. 20. Measurement setup of the proposed transmitter.

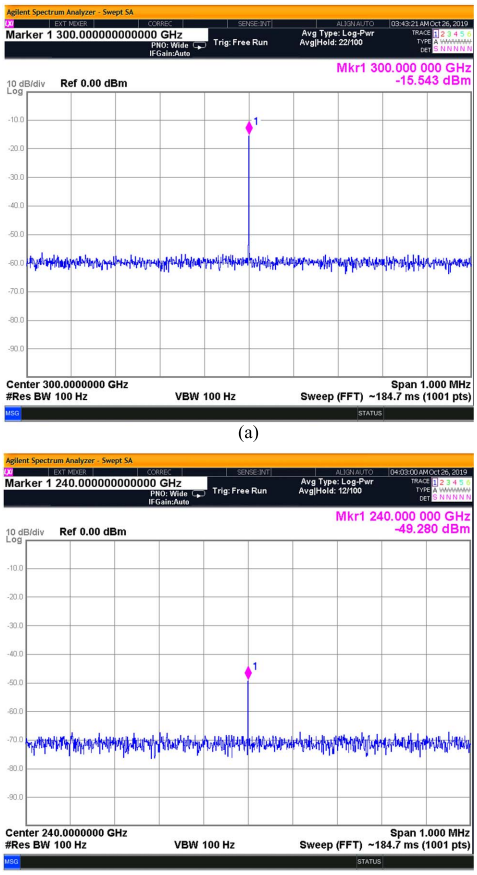

Fig. 21. Measured spectrum of (a) RF power in 1-dB compression point for $f_{IF} = 60$ GHz, $f_{LO} = 240$ GHz, and $P_{IF,TX} = 3$ dBm. (b) LO leakage for $f_{LO} = 240$ GHz.

B. 60-GHz Frequency Tripler for Measurement Setup

This integrated 300-GHz transmitter's input IF signal is 60 GHz. A 60-GHz tripler chip based on GaAs technology was added as an IF signal generator, as shown

TABLE I
COMPARISON OF WITH STATE-OF-THE-ART AMC AROUND 300 GHz

Freq. (GHz)	Tech	Topology	P_{sat} (dBm)	3-dB BW (GHz)	Relative BW (%)	DC-to-RF Efficiency (%)	Area (mm^2)	Ref.
300	130-nm SiGe	×4 Multi. + PA + Doub	2.3	223-350	44.3	0.3	1	[22]
204	130-nm SiGe	2-way PA + Doub	6.5	170-220	25.6	1.13	NA	[23]
284	130-nm SiGe	Doub + PA + Doub	2.5	280-314	11.4	0.46	0.652	[24]
215	90-nm SiGe	4-way Comb. PA + Doub	8	200-230	14	0.23	3.63	[25]
280	130-nm SiGe	×27 Multi.	8.5*	272-288	5.7	0.72	2.8	[26]
252	**130-nm SiGe**	**Doub + PA + 2-way Doub**	**5.5**	**212-260**	**20.3**	**1.4**	**0.29**	**This work**

*Radiated Power

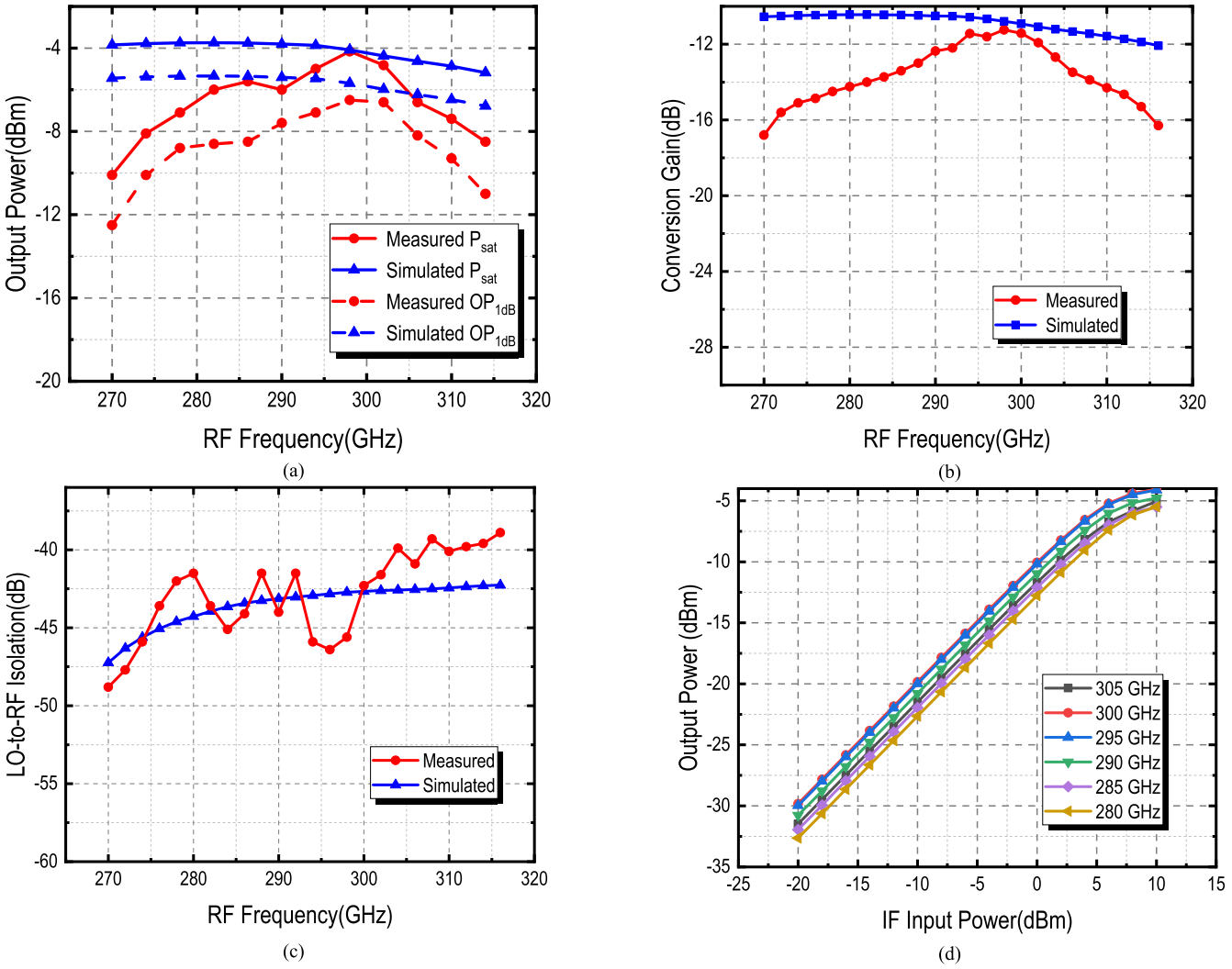

Fig. 22. Transmitter characterization results. (a) Measured and simulated saturated output power/$OP_{1\,dB}$. (b) Conversion gain at LO frequency of 240 GHz. (c) Measured and simulated LO-to-RF isolation of the transmitter. (d) Measured RF power as a function of IF input power.

in Fig. 19. This tripler model is comprised of a tripler and a three-stage common-source PA similar to our previous work [36]. The tripler consists of an antiparallel diode pair and a bandpass filter (BPF). A fifth-order high pass filter (HPF) is employed after the amplifier for fundamental and second-harmonic rejection. The saturated output power of the tripler model varies from 17 to 18.8 dBm and is sufficient for test requirements.

Considering the waveguide probe for the measurement, the tripler is integrated into a WR-12 waveguide packaging. The transition includes the RF GSG-pad-to-microstrip-line bonding wire and microstrip-line-to-waveguide transition. The insertion loss of the transition varies from −0.3 to −0.8 dB. In this way, the IF input frequency of the whole system is around 20 GHz and can be supplied by an Agilent E8257D signal generator.

TABLE II
COMPARISON OF MONOLITHICALLY INTEGRATED SUB-THZ TRANSMITTERS

Reference	[12]	[18]	[19]	[37]	[38]	[39]	[40]	**This work**
Process	0.25 μm InP DHBT	130 nm SiGe	130 nm SiGe	40 nm CMOS	40 nm CMOS	28nm CMOS	40nm CMOS	**130 nm SiGe**
f_T/f_{max} (GHz)	370/650	300/500	300/500	<300	NA	NA	-/280	**300/500**
3 dB BW (GHz)	297.6-318.1	230-250	220-255	255-275(2)	289-311	390(16)	275-305	**280-310**
Conversion Gain (dB)	25	16	10.5	-2(2)	-8(2)	NA	-10(2)	**-11.2**
P_{sat}/OP_{1dB} (dBm)	-2.3/-5	-6/-10	-0.8/-1.5(1)	-1.6/-3(2)	-5.5/-	-16/-	-14.5/-	**-4.1/-6.5**
f_{LO}/P_{LO} (GHz/dBm)	298.1/-1.8	240/0	240/0	133/NA	145/5.5	115/-	97/-	**240/5**
P_{DC} (mW)	452	1033	375	890	1400	1100	1400	**300**
Chip size (mm^2)	1.32	1.695	1.25	11.07	5.2	2	6	**0.65**
LO Arch	Fund Oscillator	Frequency multiplier (×16)	Frequency multiplier (×8)	Frequency multiplier (×3)	Frequency multiplier (×3)	External	External	**Frequency multiplier (×4)**
Architecture	Fund Mixer Amplifier	Fund Mixer Amplifier	Amplifier, Mixer, LO	Square Mixer	Square Mixer	Fund Mixer Tripler	Cubic Mixer	**Fund Mixer**

(1) Compensated for output pad
(2) Estimated from the figures.

C. Measurement of the 300-GHz Transmitter

For the measurement of the 300-GHz transmitter, the LO power is supplied by the 240-GHz multiplier chain. The OML WR03 harmonic mixer followed by the Keysight spectrum analyzer N9030A is used for the output frequency and LO signal leakage detecting, as shown in Fig. 20. The image frequency signal and other spurious signals are difficult to be filtered, so the output power of the transmitter is measured by the spectrum analyzer, and the insertion loss of the OML WR03 subharmonic mixer is calibrated using the OML calibration table. The transmitter characterization, including conversion gain and saturated output power $OP_{1\,dB}$, and the LO-to-RF isolation are summarized in Figs. 21 and 22. Fig. 21 shows the measured output spectrum at 300 GHz and the measured LO leakage spectrum at 240 GHz with a 60-GHz IF signal. Fig. 22(a) shows the measured P_{sat} and $OP_{1\,dB}$ of the transmitter front end when the IF frequency is swept and the LO frequency is fixed at 240 GHz. Fig. 22(b) shows the conversion gain of the transmitter as a function of the RF frequency swept from 275 to 315 GHz with a fixed LO frequency of 240 GHz. Fig. 22(c) shows the LO-to-RF isolation as a function of the RF frequency swept from 275 to 315 GHz with a fixed IF frequency of 60 GHz. Fig. 22(d) shows P_{RF} as a function of P_{IF}.

Across the 30-GHz 3-dB bandwidth from 280 to 310 GHz, the transmitter achieves a maximum conversion gain of −11.2 dB at 298 GHz and over −40-dB LO-to-RF isolation. The transmitter consumes 300 mW in total with 3.3-V supply, where the multiplier chain consumes 270 mW, and the upconversion mixer consumes only 30 mW.

VII. CONCLUSION

A 300-GHz monolithic integrated transmitter chipset has been demonstrated in a commercial 130-nm SiGe HBT technology. This 300-GHz transmitter consists of a 240-GHz AMC and a 300-GHz upconversion mixer. In the sub-THz band, the most critical issues are the limited transistor performance, in terms of gain and output power. In this article, the LO AMC achieves a saturated output power of 5.5 dBm, which is sufficient to drive a 300-GHz modified Gilbert mixer. High-performance balun is also a key component in the sub-THz circuit. In this work, an SSMB with coupling coefficient enhancement is proposed, which achieves the lowest insertion loss with a compact layout at around 300 GHz, to the author's best knowledge. Over the 280–310-GHz bandwidth, the output power of the transmitter is higher than −7 dBm with the maximum output power of −4.1 dBm at 300 GHz. Furthermore, this transmitter exhibits a conversion gain of −11.2 dB with $OP_{1\,dB}$ of −6.5 dBm. Compared with other state of the arts shown in Table II, the transmitter exhibits a comparable performance among silicon-based transmitters near 300 GHz with limited dc power consumption. The implemented transmitter can be used in sliding-IF or other heterodyne architecture, where IF signals [V-band (60 GHz)] are moved to the 300-GHz band for future communication systems. Besides, the presented chipset can be adapted to a number of sub-THz band imaging, radar, and sensing applications.

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REFERENCES

[1] *IEEE Standard for High Data Rate Wireless Multi-Media Networks—Amendment 2: 100 Gb/s Wireless Switched Point-to-Point Physical Layer*, IEEE Standard 802.15.3d-2017, 2017.
[2] H. Rucker, B. Heinemann, and A. Fox, "Half-terahertz SiGe BiCMOS technology," in *Proc. IEEE 12th Topical Meeting Silicon Monolithic Integr. Circuits RF Syst.*, Jan. 2012, pp. 133–136.

[3] J. J. Pekarik *et al.*, "A 90 nm SiGe BiCMOS technology for mm-wave and high-performance analog applications," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Sep. 2014, pp. 3.9.1–3.9.3.

[4] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_T/370 GHz f_{MAX} HBT and high-Q millimeter-wave passives," in *IEDM Tech. Dig.*, Dec. 2014, pp. 3.9.1–3.9.3.

[5] S. Shopov, A. Balteanu, J. Hasch, P. Chevalier, A. Cathelin, and S. P. Voinigescu, "A 234–261-GHz 55-nm SiGe BiCMOS signal source with 5.4–7.2 dBm output power, 1.3% DC-to-RF efficiency, and 1-GHz divided-down output," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2054–2065, Sep. 2016.

[6] S. Moghadami, F. Hajilou, P. Agrawal, and S. Ardalan, "A 210 GHz fully-integrated OOK transceiver for short-range wireless chip-to-chip communication in 40 nm CMOS technology," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 5, pp. 737–741, Sep. 2015.

[7] S. Moghadami, J. Isaac, and S. Ardalan, "A 0.2–0.3 THz CMOS amplifier with tunable neutralization technique," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 6, pp. 1088–1093, Nov. 2015.

[8] H. Bameri and O. Momeni, "A high-gain mm-wave amplifier design: An analytical approach to power gain boosting," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 357–370, Feb. 2017.

[9] D. Park *et al.*, "A 230–260-GHz wideband and high-gain amplifier in 65-nm CMOS based on dual-peak G_{max}-core," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1613–1623, Sep. 2019.

[10] K. Tokgoz *et al.*, "A 273–301-GHz amplifier with 21-dB peak gain in 65-nm standard bulk CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 5, pp. 342–344, Apr. 2019.

[11] M. H. Eissa and D. Kissinger, "4.5 A 13.5 dBm fully integrated 200-to-255 GHz power amplifier with a 4-way power combiner in SiGe:C BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 82–84.

[12] S. Kim *et al.*, "300 GHz integrated heterodyne receiver and transmitter with on-chip fundamental local oscillator and mixers," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 1, pp. 92–101, Jan. 2015.

[13] H. Hamada *et al.*, "300-GHz. 100-Gb/s InP-HEMT wireless transceiver using a 300-GHz fundamental mixer," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 1480–1483.

[14] D. del Rio *et al.*, "A wideband and high-linearity E-B and transmitter integrated in a 55-nm SiGe technology for backhaul point-to-point 10-Gb/s links," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 8, pp. 2990–3001, Aug. 2017.

[15] C. J. Lee *et al.*, "A 120 GHz I/Q transmitter front-end in a 40 nm CMOS for wireless chip to chip communication," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 192–195.

[16] E. Öjefors, F. Pourchon, P. Chevalier, and U. R. Pfeiffer, "A 160-GHz low-noise downconverter in a SiGe HBT technology," in *Proc. 40th Eur. Microw. Conf.*, Sep. 2010, pp. 521–524.

[17] U. R. Pfeiffer, E. Ojefors, and Y. Zhao, "A SiGe quadrature transmitter and receiver chipset for emerging high-frequency applications at 160 GHz," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 416–417.

[18] N. Sarmah *et al.*, "A fully integrated 240-GHz direct-conversion quadrature transmitter and receiver chipset in SiGe technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 562–574, Feb. 2016.

[19] M. H. Eissa *et al.*, "Wideband 240-GHz transmitter and receiver in BiCMOS technology with 25-Gbit/s data rate," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2532–2542, Sep. 2018.

[20] P. Rodríguez-Vázquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "A 16-QAM 100-Gb/s 1-M wireless link with an EVM of 17% at 230 GHz in an SiGe technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 4, pp. 297–299, Apr. 2019.

[21] P. Rodriguez-Vazquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "A QPSK 110-Gb/s polarization-diversity MIMO wireless link with a 220–255 GHz tunable LO in a SiGe HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 9, pp. 3834–3851, Sep. 2020.

[22] A. Ali *et al.*, "220–360-GHz broadband frequency multiplier chains (x8) in 130-nm BiCMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2701–2714, Jul. 2020.

[23] K. Wu, S. Muralidharan, and M. M. Hella, "A wideband SiGe BiCMOS frequency doubler with 6.5-dBm peak output power for millimeter-wave signal sources," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 1, pp. 187–200, Jan. 2018.

[24] P. Zhou, J. Chen, P. Yan, Z. Chen, D. Hou, and W. Hong, "A 280-325 GHz frequency multiplier chain with 2.5 dBm peak output power," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2019, pp. 1–4.

[25] H.-C. Lin and G. M. Rebeiz, "A SiGe multiplier array with output power of 5-8 dBm at 200-230 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2050–2058, Jul. 2016.

[26] N. Buadana *et al.*, "A 280-GHz digitally controlled four port chip-scale dielectric resonator antenna transmitter with DiCAD true time delay," *IEEE Solid-State Circuits Lett.*, vol. 3, no. 7, pp. 2050–2058, Jul. 2016.

[27] E. Ojefors, B. Heinemann, and U. R. Pfeiffer, "Subharmonic 220- and 320-GHz SiGe HBT receiver front-ends," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1397–1404, May 2012.

[28] Y. Zhao, E. Ojefors, K. Aufinger, T. F. Meister, and U. R. Pfeiffer, "A 160-GHz subharmonic transmitter and receiver chipset in an SiGe HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3286–3299, Oct. 2012.

[29] K. S. Ang and I. D. Robertson, "Analysis and design of impedance-transforming planar Marchand baluns," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 2, pp. 402–406, Feb. 2001.

[30] F. Ahmed, M. Furqan, and A. Stelzer, "A 200–325-GHz wideband, low-loss modified Marchand balun in SiGe BiCMOS technology," in *Proc. Eur. Microw. Conf. (EuMC)*, Sep. 2015, pp. 40–43.

[31] S. Malz, P. Hillger, B. Heinemann, and U. R. Pfeiffer, "A 275 GHz amplifier in 0A3 μm SiGe," in *Proc. 11th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Oct. 2016, pp. 185–188.

[32] L. Xu, H. Sjoland, M. Tormanen, T. Tired, T. Pan, and X. Bai, "A miniaturized Marchand balun in CMOS with improved balance for millimeter-wave applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 1, pp. 53–55, Jan. 2014.

[33] R. Mongia, I. Bahl, and P. Bhartia, *RF and Microwave Coupled-Line Circuits*. Norwood, MA, USA: Artech House, 1999.

[34] P. Zhou *et al.*, "A 150-GHz transmitter with 12-dBm peak output power using 130-nm SiGe:C BiCMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 5, pp. 342–344, Jul. 2020.

[35] H. Li *et al.*, "A 250-GHz differential SiGe amplifier with 21.5-dB gain for sub-THz transmitters," *IEEE Trans. THz Sci. Technol.*, vol. 10, no. 6, pp. 624–633, Nov. 2020.

[36] C. Wang *et al.*, "E-band transceiver MMIC in waveguide package for millimeter-wave radio channel emulation applications," *Sci. China Inf. Sci.*, to be published.

[37] S. Lee *et al.*, "An 80-Gb/s 300-GHz-band single-chip CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3577–3588, Dec. 2019.

[38] K. Takano *et al.*, "A 105 Gb/s 300 GHz CMOS transmitter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 308–309.

[39] A. Standaert and P. Reynaert, "A 390-GHz outphasing transmitter in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2703–2713, Oct. 2020.

[40] K. Katayama *et al.*, "A 300 GHz CMOS transmitter with 32-QAM 17.5 Gb/s/ch capability over six channels," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3037–3048, Dec. 2016.

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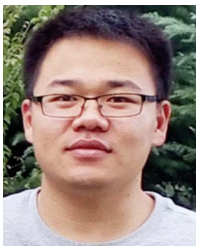

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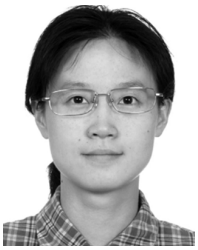

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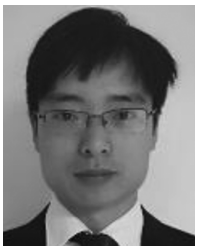
Since 2000, she has been with the State Key Laboratory of Millimeter Waves, Southeast University, where she is currently an Associate Professor with the School of Information Science and Engineering. Her current research interests include microwave and millimeter-wave circuit design and monolithic microwave integrated circuit (MMIC) design.



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