A New Compact CMOS Distributed Digital Attenuator

Kwangwon Park, Seungjong Lee, and Sanggeun Jeon, *Member, IEEE*

***Abstract*— This article presents a new millimeter-wave (mm-wave) distributed digital attenuator with a compact size and high linearity. To overcome the large area consumption of conventional distributed attenuators, multiple unit attenuation cells are combined at a single node, forming a multistate cell. By distributing the multistate cells along transmission lines (T-lines), the number of T-lines is reduced, leading to a compact chip size at a given attenuation range and step. The linearity is improved by stacking multiple FET varistors in each unit attenuation cell. An analytical analysis confirms that the proposed distributed attenuator topology maintains a low phase error comparable to that of the conventional counterpart. To experimentally verify the proposed topology, two different mm-wave digital attenuators are designed and implemented using a 65-nm CMOS technology. The first attenuator (Att1) uses a regular nFET as varistor of the attenuation cell, whereas the other attenuator (Att2_TW) uses a triple-well nFET to reduce the insertion loss. The maximum attenuation range of both attenuators is 14 dB with a step of 1 dB. The measured insertion losses of Att1 and Att2_TW are 4.8 and 4.1 dB at 35 GHz, respectively. The insertion losses are no more than 6.2 dB over 10–50 GHz and 4.3 dB over 15–43 GHz, respectively. The input 1-dB compression powers are 15 and 14 dBm, respectively, at 35 GHz. The chip sizes, excluding probing pads, are as small as 0.19 and 0.29 mm^2.**

***Index Terms*— CMOS varistors, digital attenuator, distributed attenuator, millimeter wave (mm-wave), multistate cell, triple-well nFET.**

I. Introduction

VARIABLE attenuators are widely used in many RF and millimeter-wave (mm-wave) applications, such as wireless communication and radar systems [1]–[4]. In phased-array systems, the amplitude control is needed for several purposes, including the signal calibration among different array channels (or chips) and beam tapering for sidelobe suppression. Typical specifications required for a variable attenuator are the attenuation range, step, bandwidth, insertion loss, and amplitude/phase errors. In addition, low dc-power and small chip-area consumption are demanded particularly if the attenuator is employed in a large-scale phased-array system. Furthermore, high linearity would be needed to maintain high dynamic range of the system with a strong desired or interference signal presented.

Conventionally, T- or Π-attenuators with switching transistors have been widely designed to provide precise step attenuation by digitally controlling the switches [5]–[11]. These attenuators in general offer a large attenuation range with compact chip area, but may suffer from relatively large phase error due to the parasitics of a series-connected switch [8]. Moreover, the attenuator performance, such as insertion loss, isolation, and bandwidth, are strongly affected by the switch device performance. Therefore, the T- or Π-attenuators are preferred in the GaAs technologies that have superior device performance than the silicon technologies at mm-wave frequencies.

A distributed attenuator, on the other hand, does not require such high switch device performance and thus is appropriate in the silicon technologies [11]–[13]. It offers an advantage of relatively low insertion loss and phase error because no series switch is used in the RF signal path. However, a distributed attenuator usually suffers from a limited attenuation range and large chip area consumption. This is because more varistors and transmission lines (T-lines) are demanded for achieving a higher attenuation range, which inevitably increases the chip area.

In this article, a new topology for compact distributed digital attenuator is proposed and demonstrated in a 65-nm CMOS technology. By combining multiple unit attenuation cells at a single node along T-lines, the attenuation range and the number of states can be increased with small increment of chip area. Moreover, the linearity of the attenuator is improved by using a stacked-FET structure. This article is organized as follows. In Section II, the operation principle of the proposed distributed attenuator is described and compared with that of the conventional attenuator. In Section III, two different versions of CMOS distributed digital attenuators are designed using the proposed topology. The measurement results are presented in Section IV, followed by the conclusion in Section V.

II. Operation Principle

A. Proposed Compact Distributed Attenuator

A typical schematic of the conventional distributed attenuator with N-attenuation states is shown in Fig. 1(a). It consists

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Kwangwon Park was with the School of Electrical Engineering, Korea University, Seoul 02841, South Korea. He is now with the Electronics and Communication Engineering, Republic of Korea Air Force Academy, Chungcheongbuk-do 28187, South Korea.

Seungjong Lee and Sanggeun Jeon are with the School of Electrical Engineering, Korea University, Seoul 02841, South Korea (e-mail: sgjeon@korea.ac.kr).

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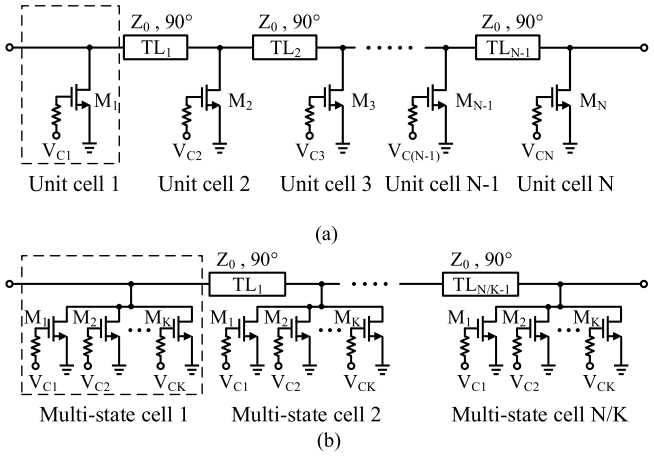

Fig. 1. Structure of the distributed digital attenuator with N-attenuation states. (a) Conventional. (b) Proposed.

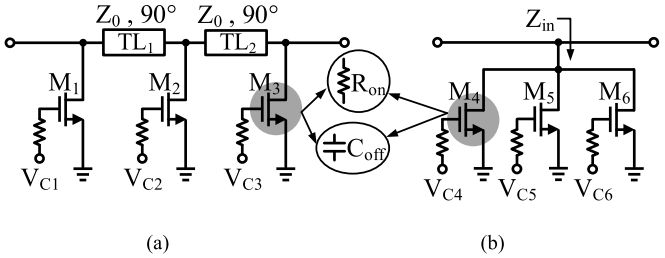

Fig. 2. Exemplary 3-dB attenuator with 1-dB step. (a) Conventional. (b) Proposed.

TABLE I
TRANSISTOR PARAMETERS REQUIRED FOR 3-dB ATTENUATION WITH 1-dB STEP OF FIG. 2

		Transistor	R_{on}	C_{off}
Conventional		M_1, M_2, M_3	$4Z_0$	C_o
Proposed	Config. I	M_4	$4Z_0$	C_o
		M_5	$1.9Z_0$	$2.1C_o$
		M_6	$1.2Z_0$	$3.3C_o$
	Config. II	M_4	$4Z_0$	C_o
		M_5	$3.6Z_0$	$1.1C_o$
		M_6	$3.2Z_0$	$1.3C_o$

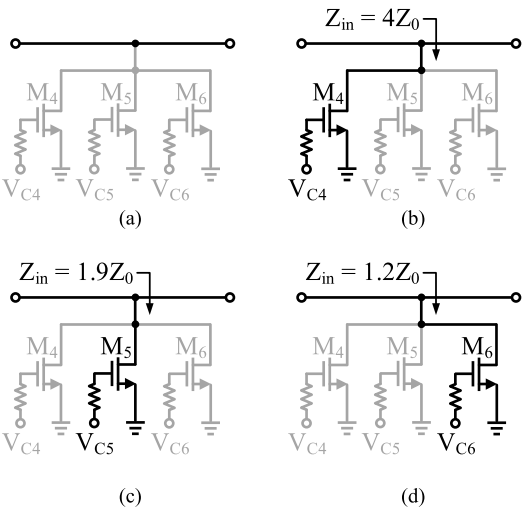

Fig. 3. Transistor configurations I (config. I) for implementing the attenuation state of (a) 0 dB (reference state), (b) 1, (c) 2, and (d) 3 dB.

of N shunt transistors (M_1–M_N) and $N-1$ quarter-wave T-lines (TL_1–TL_{N-1}). Each transistor operates as a varistor by switching it ON or OFF with the control voltage (V_{C1}–V_{CN}). The quarter-wave T-lines convert the impedance of varistors to achieve proper impedance matching at the input and output ports. Since no series switch is used, the distributed attenuator generally presents low insertion loss and phase error, especially in silicon transistor technologies, compared with T- or Π-attenuators. However, in case that a high attenuation range with more steps is required, the number of shunt transistors should be increased. This accordingly increases the number of quarter-wave T-lines, thus resulting in large chip area consumption. Although the electrical length of T-lines can be reduced below 90° at the expense of compromised impedance matching [11], [12], the number of T-lines is still proportional to the number of attenuation states.

To resolve the large chip area consumption demanded for a high attenuation range, a new compact distributed attenuator is proposed, as shown in Fig. 1(b). Multiple unit attenuation cells are combined at a single node along the T-lines, forming a multistate attenuation cell. If K unit cells are combined together, K-different attenuation states are implemented at once by the single multistate cell at a single node. It should be compared with the conventional distributed attenuator where only a single unit cell is connected to each node, as shown in Fig. 1(a). Therefore, in the proposed attenuator, the number of attenuation cells connected to T-lines is reduced from N to N/K (N/K is assumed to be a natural number) for achieving N-attenuation states. This accordingly decreases the number of T-lines to $N/K-1$, thus reducing the chip area consumption.

An exemplary comparison between the conventional and proposed distributed attenuators is shown in Fig. 2. The attenuation range and step are assumed to be 3 and 1 dB, respectively, for both attenuators. In the conventional attenuator shown in Fig. 2(a), three transistors (M_1–M_3), operating as varistors, are distributed along two quarter-wave T-lines. Each transistor is modeled by an ON-resistance (R_{ON}) and OFF-capacitance (C_{OFF}) when the transistor is switched ON and OFF, respectively. To implement 3-dB attenuation with 1-dB step, R_{ON} of each transistor should be $4Z_0$, as given in Table I. On the other hand, the proposed attenuator shown in Fig. 2(b) requires only three transistors (M_4–M_6) with no need of T-lines in principle. The three transistors form a three-state attenuation cell at once. To achieve 1-, 2-, and 3-dB attenuation, the input impedance looking into the three-state cell (Z_{in}) should be equal to $4Z_0$, $1.9Z_0$, and $1.2Z_0$, respectively.

There are two different configurations of transistors that implement Z_{in} required for the three attenuation states. The first configuration (config. I) is shown in Fig. 3. Each attenuation state is realized by turning on one of M_4–M_6 in turn,

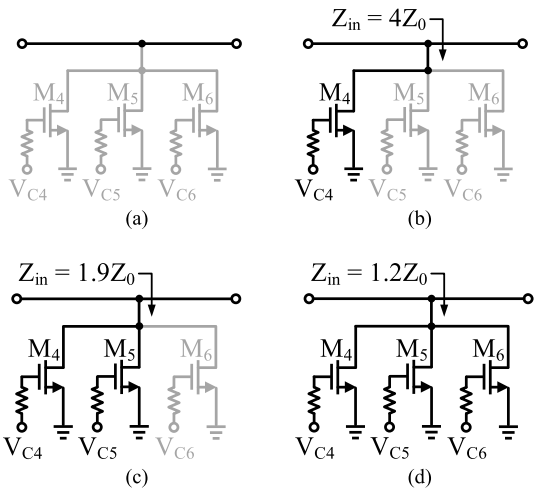

Fig. 4. Transistor configurations II (config. II) for implementing the attenuation state of (a) 0 (reference state), (b) 1, (c) 2, and (d) 3 dB.

while the other two are turned off. Therefore, the dimension of transistors should be determined such that $R_{\rm ON}$ of M_4–M_6 becomes $4Z_0$, $1.9Z_0$, and $1.2Z_0$, respectively, as given in Table I. The second configuration (config. II) is shown in Fig. 4. The ON-resistance of a newly turned-on transistor is added in shunt to those of previously turned-on transistors. For 1-dB attenuation, only M_4 is turned on. However, for 2-dB attenuation, both M_4 and M_5 are turned on, leading to $Z_{\rm in} = 1.9Z_0$. For 3-dB attenuation, all of M_4–M_6 are turned on, leading to $Z_{\rm in} = 1.2Z_0$. Therefore, the transistors should be designed such that $R_{\rm ON}$ of M_4–M_6 are $4Z_0$, $3.6Z_0$, and $3.2Z_0$, respectively, as summarized in Table I.

Config. II demands smaller transistor sizes due to higher $R_{\rm ON}$ than config. I. This allows for less transistor parasitics, e.g., less $C_{\rm OFF}$. In Table I, $C_{\rm OFF}$ of each transistor is calculated under the first-order assumption that $R_{\rm ON} \times C_{\rm OFF}$ is constant, which will be used in the phase-error analysis in Section II-B.

It is also noted that the number of transistors (K) in each multistate cell can be further extended to increase the attenuation range and step. However, as the attenuation range achieved by each multistate cell increases, the input impedance of the cell ($Z_{\rm in}$) must be reduced accordingly, thus degrading the port-matching performance. Therefore, the attenuation range, step, and K of each multistate cell should be carefully determined considering the tradeoff between the chip area consumption and impedance matching.

B. Phase-Error Analysis

In the digital attenuators, the insertion phase should be ideally constant over different attenuation states to avoid adverse signal distortion. The phase error ($\Delta\varphi$) is defined by an insertion phase difference between the reference state and the maximum attenuation state. In this section, the phase error of the proposed attenuator is analyzed and compared with that of the conventional attenuator.

First, the phase error of the conventional 3-dB distributed attenuator of Fig. 2(a) is calculated as follows. By using the *ABCD* matrices of the transistors and T-lines, S_{21} of the conventional attenuator operating in the reference and 3-dB attenuation states is derived as

$$S_{21,\rm ref}^{\rm conv} = \frac{2}{2[(\omega C_{\rm OFF} Z_0)^2 - 1] + j[(\omega C_{\rm OFF} Z_0)^3 - 3\omega C_{\rm OFF} Z_0]} \tag{1}$$

and

$$S_{21,3\,\rm dB}^{\rm conv} = -\frac{2R_{\rm ON}^3}{2R_{\rm ON}^3 + 3R_{\rm ON}^2 Z_0 + 2R_{\rm ON} Z_0^2 + Z_0^3} \tag{2}$$

respectively. Note that all three transistors are modeled by $C_{\rm OFF}$ in the reference state and by $R_{\rm ON}$ in the 3-dB state. From (1) and (2), the phase error of the conventional 3-dB distributed attenuator is calculated as

$$\Delta\phi_{\rm 3dB}^{\rm conv} = \tan^{-1}\left[\frac{\omega C_o Z_0}{2}\frac{3 - (\omega C_o Z_0)^2}{1 - (\omega C_o Z_0)^2}\right] \tag{3}$$

where $C_{\rm OFF}$ is replaced by C_o, as given in Table I. Assuming that $\omega C_o Z_0 \ll 1$, (3) is approximated to be

$$\Delta\phi_{\rm 3dB}^{\rm conv} \simeq \tan^{-1}\left[\frac{3\omega C_o Z_0}{2}\right] \simeq 1.50\omega C_o Z_0. \tag{4}$$

The phase error of the proposed 3-dB distributed attenuator of Fig. 2(b) is calculated in a similar way. First, config. I is assumed for the transistor operation. In the reference state, all transistors are turned off as shown in Fig. 3(a), so that S_{21} is written as

$$S_{21,\rm ref}^{\rm prop(1)} = \frac{2}{2 + j\omega(C_{{\rm OFF},M4} + C_{{\rm OFF},M5} + C_{{\rm OFF},M6})Z_0} \tag{5}$$

where $C_{{\rm OFF},Mk}$ ($k = 4, 5, 6$) is the OFF-capacitance of M_k. S_{21} in the 3-dB attenuation state shown in Fig. 3(d) is derived as

$$S_{21,3\rm dB}^{\rm prop(1)} = \frac{2R_{{\rm ON},M6}}{(2R_{{\rm ON},M6} + Z_0) + j\omega(C_{{\rm OFF},M4} + C_{{\rm OFF},M5})Z_0 R_{{\rm ON},M6}} \tag{6}$$

where $R_{{\rm ON},Mk}$ ($k = 4, 5, 6$) is the ON-resistance of M_k. By inserting the values of $R_{\rm ON}$ and $C_{\rm OFF}$ given in Table I into (5) and (6), the phase error of the proposed 3-dB attenuator with config. I is derived as

$$\phi_{\rm 3dB}^{\rm prop(1)} \simeq 2.11\omega C_o Z_0. \tag{7}$$

Finally, S_{21} of the proposed distributed attenuator with config. II operating in the reference and 3-dB attenuation states is calculated as

$$S_{21,\rm ref}^{\rm prop(2)} = \frac{2}{2 + j\omega(C_{{\rm OFF},M4} + C_{{\rm OFF},M5} + C_{{\rm OFF},M6})Z_0} \tag{8}$$

and

$$S_{21,3\rm dB}^{\rm prop(2)} = \frac{2}{2 + \frac{Z_0}{R_{{\rm ON},M4} \| R_{{\rm ON},M5} \| R_{{\rm ON},M6}}} \tag{9}$$

respectively. Therefore, the phase error of the proposed 3-dB attenuator with config. II is calculated as

$$\Delta\phi_{\rm 3dB}^{\rm prop(2)} \simeq 1.70\omega C_o Z_0. \tag{10}$$

Comparing (7) and (10), config. II exhibits a less phase error than config. I. This is because the size of transistors required for config. II is smaller than that for config. I. Furthermore, comparing (10) with (4), the proposed attenuator presents a similar phase error to the conventional one, not disrupting a benefit of the distributed attenuator, i.e., low phase error.

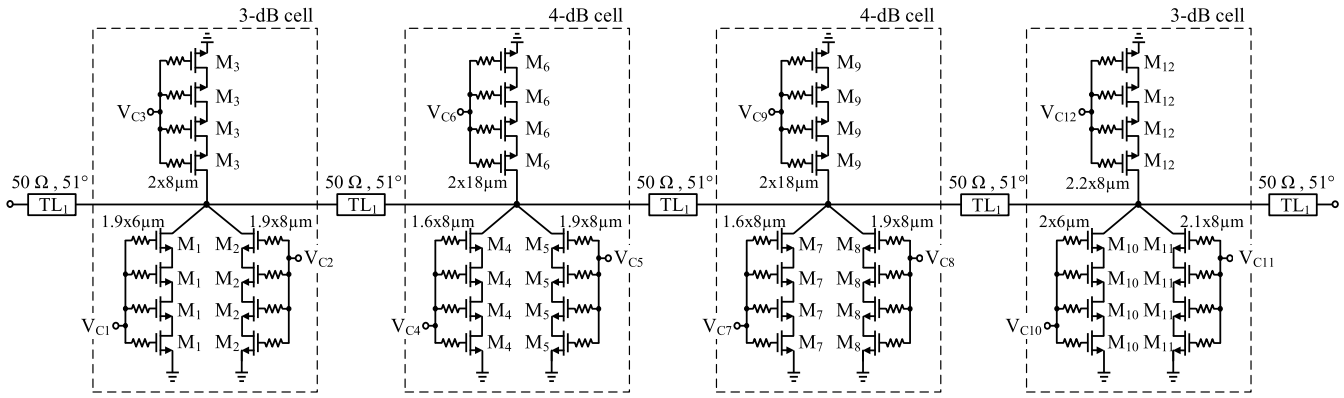

Fig. 5. Schematic of the proposed compact 14-dB distributed attenuator with regular nFETs (Att1). The electrical lengths of T-lines are defined at 35 GHz.

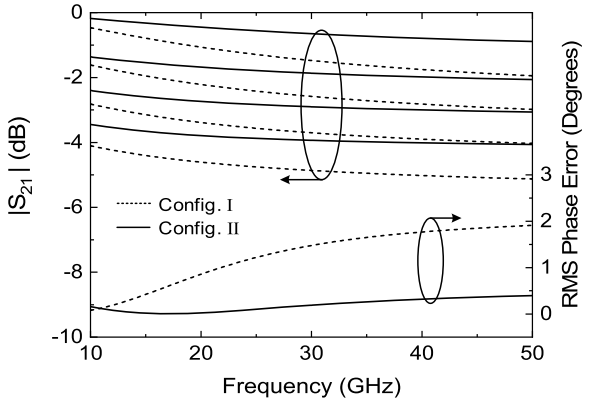

Fig. 6. Simulated insertion loss and RMS phase error of the 3-dB cell with config. I and config. II.

III. Design of Proposed Distributed Attenuators

Two mm-wave CMOS digital attenuators are designed using the proposed compact distributed topology. The first attenuator (Att1) uses a regular nFET as a varistor, whereas the second (Att2_TW) uses a triple-well nFET to reduce the insertion loss. The attenuation range and step are aimed to be 14 and 1 dB, respectively.

A. Mm-Wave Distributed Attenuator With Regular nFETs (Att1)

A schematic of the proposed CMOS distributed attenuator (Att1) is shown in Fig. 5. To implement the 14-dB attenuation range, Att1 consists of two 3-dB cells and two 4-dB cells, which are distributed along T-lines. A 3-dB cell is composed of three different transistors (M_1-M_2-M_3 and M_{10}-M_{11}-M_{12}) connected together in shunt, as proposed in Fig. 2(b). Among the two different transistor configurations of the attenuation cell discussed in Section II-A, config. II is chosen for low parasitic capacitance and phase error as well. In Fig. 6, the simulated insertion loss and rms phase error of the 3-dB cell are compared between config. I and config. II. As expected, config. II presents less insertion loss and less phase error than config. I. This is due to the smaller parasitic capacitance of transistors used in config. II.

TABLE II
Transistor Operation of 3-dB Attenuation Cell (*O*: On and -: Off)

	M_1 (M_{10})	M_2 (M_{11})	M_3 (M_{12})
Reference	—	—	—
1 dB	O	—	—
2 dB	O	O	—
3 dB	O	O	O

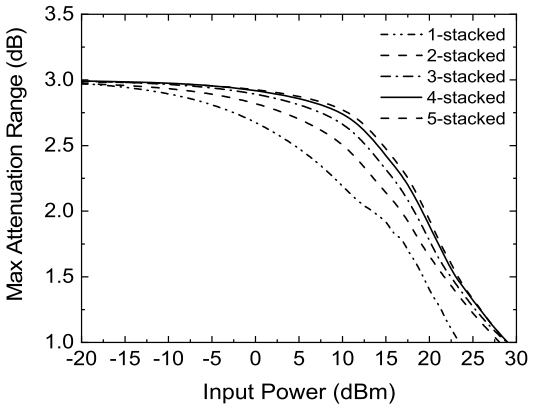

Fig. 7. Simulated linearity of the 3-dB cell at 35 GHz according to the number of stacked transistors.

The operation of each transistor in the 3-dB cell is given in Table II. The 1-, 2-, and 3-dB attenuations are realized by turning on $M_1(M_{10})$ only, turning on M_1 and $M_2(M_{10}$ and $M_{11})$ only, and turning on all of M_1–M_3 (M_{10}–M_{12}), respectively. The transistor dimension is determined by the ON-resistance required for each attenuation value, i.e., $4Z_0$, $3.6Z_0$, and $3.2Z_0$, as given in Table I.

To improve the linearity, a stacked-FET structure is employed for the implementation of each ON-resistance. In Fig. 7, the linearity of the 3-dB cell at 35 GHz is compared when the number of stacked transistors is varied from one to five. The input 1-dB compression power ($P_{\text{in,1 dB}}$) increases from 13.5 to 19.6 dBm as the stacked number increases from one to four. Further increase of the stacked number over four results in little improvement of $P_{\text{in,1 dB}}$. Therefore,

TABLE III
TRANSISTOR OPERATION OF 4-dB ATTENUATION CELL (*O*: ON AND -: OFF)

	M_4 (M_7)	M_5 (M_8)	M_6 (M_9)
Reference	–	–	–
1 dB	O	–	–
2 dB	O	O	–
4 dB	O	O	O

four transistors are chosen to be stacked together to realize each ON-resistance. The dimension of each transistor is shown in Fig. 5. The control voltage (V_{Ck}, $k = 1, 2, \ldots, 12$) of 1 or 0 V is applied through a 20-kΩ resistor to turn on or off the transistor. An additional in-house modeling is performed to the original transistor model for improving the simulation accuracy at the mm-wave frequency [14].

A 4-dB cell is designed in a similar manner as the 3-dB cell. In Table III, the operation of M_4-M_5-M_6 (or M_7-M_8-M_9) is given to realize 1-, 2-, and 4-dB attenuation in addition to the reference state. The dimensions of M_4 and M_5 (M_7 and M_8) are determined such that the ON-resistances become $4Z_0$ and $3.6Z_0$, respectively, which are the same as those of a 3-dB cell. On the other hand, the dimension of M_6 (M_9) is determined to have an ON-resistance of $0.85Z_0$, which realizes 4-dB attenuation. The 4-dB cell is also implemented using a four-FET-stacked structure for high linearity.

Two 3-dB cells and two 4-dB cells are distributed along T-lines. In principle, the electrical length between two adjacent attenuation cells should be 90° for the best return loss [15]. However, the length can be reduced to save the chip area at the expense of compromised return loss [12]. It is found from the simulation that an electrical length of 51° at 35 GHz is enough to keep the return loss below 10 dB from 16 to 62 GHz.

The placement order of the four individual attenuation cells is carefully determined in such a way to maintain decent return loss. A 4-dB cell demands a larger transistor with less ON-resistance than a 3-dB cell. Thus, the 4-dB cell would disrupt the impedance matching more significantly at the input and output ports. Therefore, two 4-dB cells are placed in the middle, whereas two 3-dB cells are placed at each end close to the input or output port.

The ON/OFF operation of each transistor for realizing 14-dB attenuation with 1-dB step is summarized in Table IV. It is noted that there exist multiple ON/OFF combinations of the transistors to realize a specific attenuation state. For example, the 1-dB attenuation can be realized by turning on M_1 or M_4 or M_7 or M_{10}. However, the closer the ON-resistance is placed to the port, the more the return loss is degraded. Therefore, it would be better to turn on either M_4 or M_7 for 1-dB attenuation for greater return loss. In this work, M_4 is chosen to be turned on, as shown in Table IV. In the same perspective of return loss, to achieve the first six attenuation states (up to 6-dB attenuation), two 4-dB cells placed in the middle are first used without turning on the 3-dB cells. For the attenuation of 7 dB and above, the 3-dB cells begin to be used because such high attenuation states cannot be realized only with 4-dB cells. Finally, the maximum attenuation of 14 dB is realized by turning on all transistors.

TABLE IV
TRANSISTOR OPERATION FOR ALL 15 ATTENUATION STATES (*O*: ON AND -: OFF)

Atten (dB)	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}	M_{11}	M_{12}
0	–	–	–	–	–	–	–	–	–	–	–	–
1	–	–	–	O	–	–	–	–	–	–	–	–
2	–	–	–	O	–	–	O	–	–	–	–	–
3	–	–	–	O	O	–	O	–	–	–	–	–
4	–	–	–	O	O	–	O	O	–	–	–	–
5	–	–	–	O	O	O	O	–	–	–	–	–
6	–	–	–	O	O	O	O	O	–	–	–	–
7	O	–	–	O	O	O	O	O	–	–	–	–
8	–	–	–	O	O	O	O	O	O	–	–	–
9	O	–	–	O	O	O	O	O	O	–	–	–
10	O	O	–	O	O	O	O	O	O	–	–	–
11	O	O	O	O	O	O	O	O	O	–	–	–
12	O	O	O	O	O	O	O	O	O	O	–	–
13	O	O	O	O	O	O	O	O	O	O	O	–
14	O	O	O	O	O	O	O	O	O	O	O	O

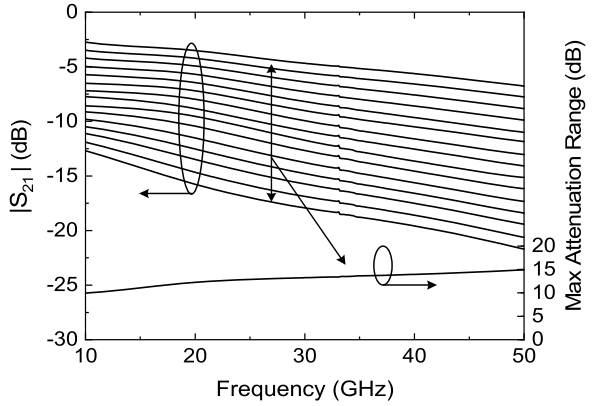

Fig. 8. Simulated attenuation and the maximum attenuation range of Att1.

It is noted that the ON/OFF operation of transistors is not symmetric along the middle of the circuit except for the attenuation states of 2, 4, 8, and 14 dB. In order to offset the adverse effect of the asymmetry on realizing each designated attenuation state, the transistor dimension is subtly tuned and adjusted. As a result, the transistor dimensions of two 3-dB cells are slightly different from each other, as shown in Fig. 5. The simulated attenuation and the maximum attenuation range of Att1 with regular nFETs are shown in Fig. 8.

B. Mm-Wave Distributed Attenuator With Triple-Well nFETs (Att2_TW)

The second CMOS distributed attenuator (Att2_TW) is designed in the same manner to Att1 except that a triple-well nFET with the body-floating technique is used to improve the insertion loss [16], [17]. The schematic of Att2_TW is shown in Fig. 9. Since the isolated p-well of the

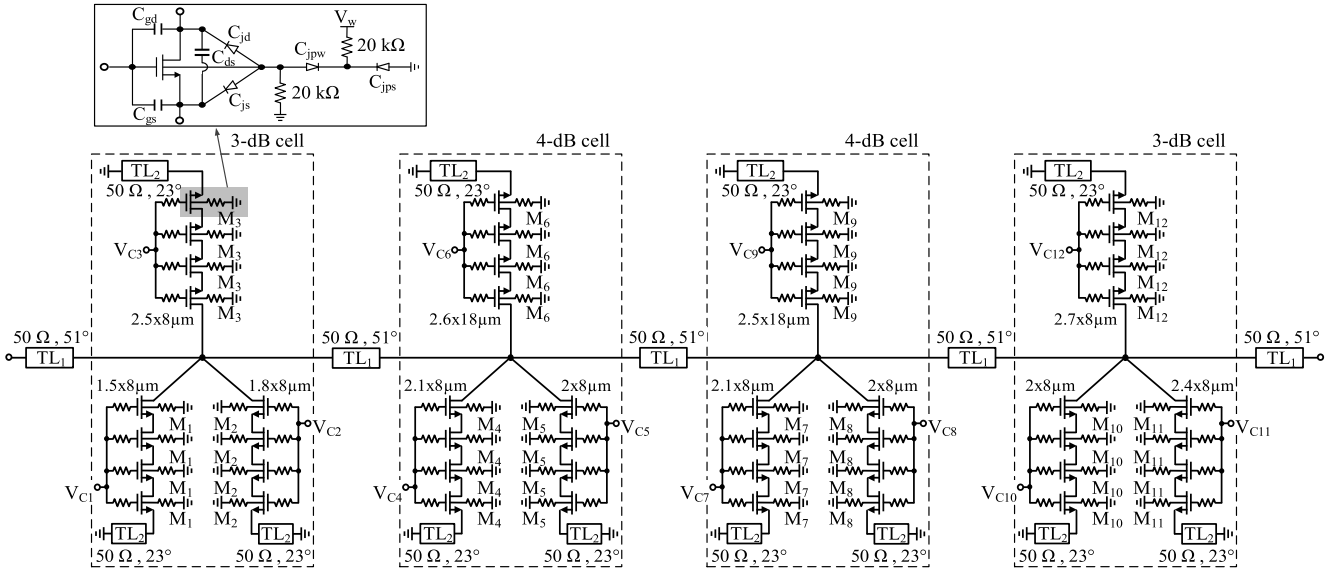

Fig. 9. Schematic of the proposed compact 14-dB distributed attenuator with triple-well nFETs (Att2_TW). The electrical lengths of T-lines are defined at 35 GHz.

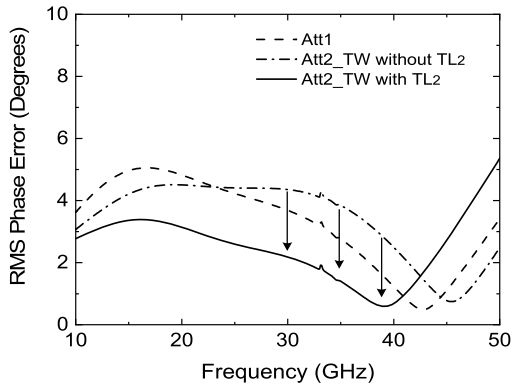

Fig. 10. Simulated rms phase error of Att1 and Att2_TW with and without the phase-compensating T-lines.

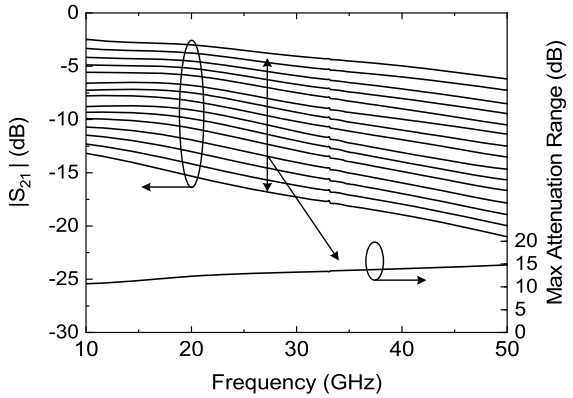

Fig. 11. Simulated attenuation and the maximum attenuation range of Att2_TW.

triple-well nFET is grounded through a 20-kΩ resistor, the transistor body is floated in the RF sense. This reduces the OFF-capacitance contributed by the parasitic junction capacitances, thus improving the insertion loss. The triple-well nFETs are stacked together to increase the linearity. The ON/OFF operation of the transistors for achieving 14-dB attenuation is identical to that shown in Table IV.

Although improving the insertion loss, the triple-well nFET presents more various junction capacitances among the isolated p-well, deep n-well, and p-substrate than a regular nFET. This would increase the phase error of the attenuator. As shown in Fig. 10, the rms phase error of Att2_TW over the entire 14 attenuation states is larger than that of Att1 from 23 to 44 GHz.

To reduce the phase error, additional grounded T-lines (TL_2) are inserted in series to the transistors [12]. The T-lines resonate out the parasitic capacitances of transistors and thus compensate for the phase error. The characteristic impedance and electrical length of TL_2 are 50 Ω and 23°, respectively, and each TL_2 occupies an area of 0.014 mm^2. It can be seen from Fig. 10 that the rms phase error is reduced by the use of the phase-compensating T-lines.

The simulated attenuation and the maximum attenuation range of Att2_TW are shown in Fig. 11. Compared to Att1, the insertion loss in the reference state is improved by 0.3–0.7 dB over the frequency of 10–50 GHz (see Fig. 12), whereas the chip area increases a little due to the additional T-lines for phase compensation.

IV. Measurement Results

The proposed distributed attenuators (Att1 and Att2_TW) are fabricated in a 65-nm CMOS technology. The chip photographs are shown in Figs. 13 and 14. The chip areas are 980 $\times$ 210 μm^2 and 980 $\times$ 300 μm^2, respectively, excluding the probing pads.

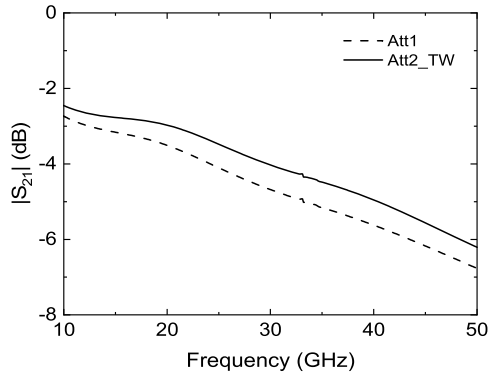

Fig. 12. Comparison of insertion loss in the reference state between Att1 and Att2_TW.

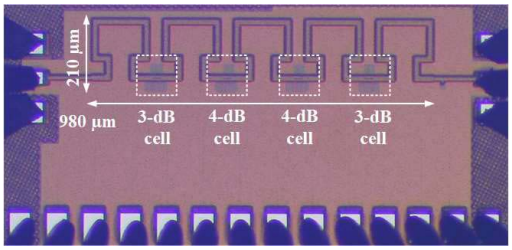

Fig. 13. Chip photograph of Att1.

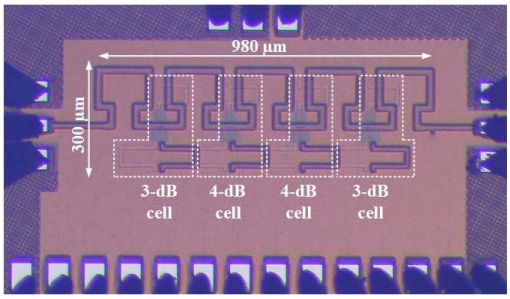

Fig. 14. Chip photograph of Att2_TW.

A. Mm-Wave Distributed Attenuator With Regular nFETs (Att1)

The measured attenuation at all 15 attenuation states (one reference and 14 attenuation states) is shown in Fig. 15. The insertion loss at the reference state is 4.8 dB at 35 GHz and varies from 2.6 to 6.2 dB over the frequency of 10–50 GHz. The maximum attenuation range is on average 14 dB with a step of 1 dB. As shown in Fig. 16, the input and output return losses of all attenuation states are higher than 8.7 dB at 10–50 GHz.

Fig. 17 shows the measured attenuation range at different input powers at 35 GHz. As the input power increases, the insertion-loss curve compresses at the low attenuation states, while the curve expands at the high attenuation states. The 1-dB compression point is defined as the point where the maximum attenuation range decreases by 1 dB. The input power at the 1-dB compression point ($P_{\text{in,1 dB}}$) is measured to be 15 dBm at 35 GHz.

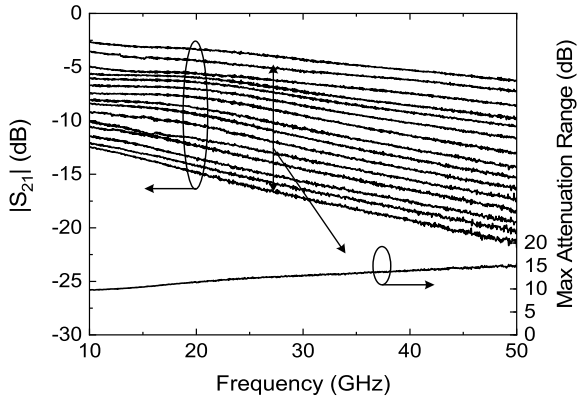

Fig. 15. Measured attenuation and the maximum attenuation range of Att1.

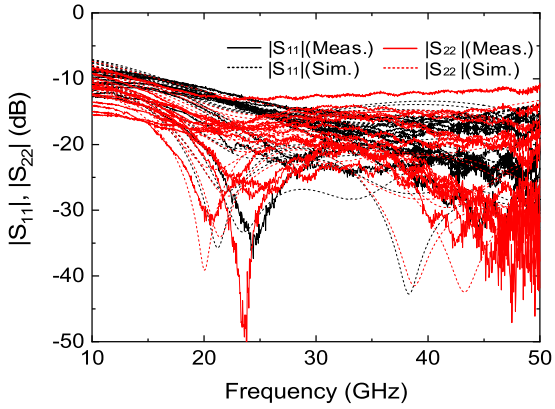

Fig. 16. Measured input and output return loss of Att1.

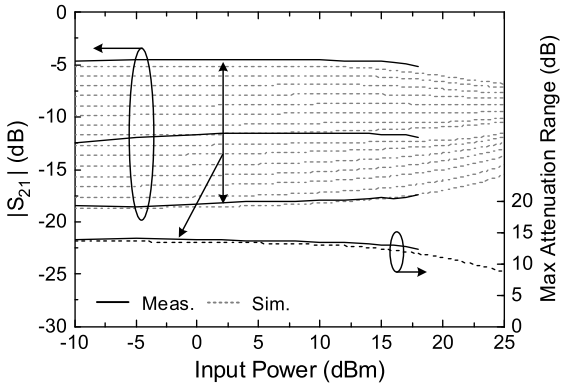

Fig. 17. Measured attenuation range versus input power at 35 GHz of Att1.

Fig. 18 shows the measured rms amplitude and phase errors. The rms amplitude error is 0.3–2.2 dB over the frequency of 10–50 GHz. The rms phase error varies from 0.8° to 4.5° over the frequency of 10–50 GHz.

B. Mm-Wave Distributed Attenuator With Triple-Well nFETs (Att2_TW)

The measured attenuation at 15 states is shown in Fig. 19. The insertion loss at the reference state is 4.1 dB at 35 GHz and varies from 2.9 to 4.3 dB over the frequency of 15–43 GHz. Compared to Att1, the insertion loss is improved

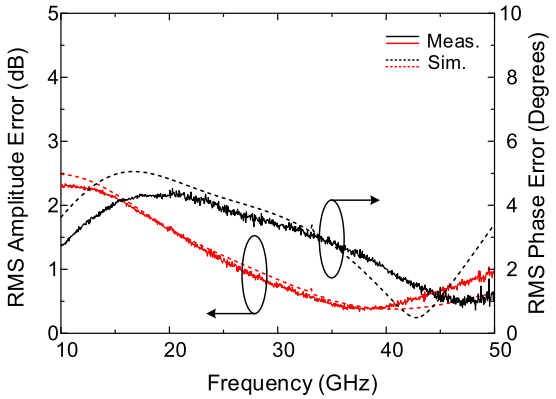

Fig. 18. Measured RMS phase error and RMS amplitude error of Att1.

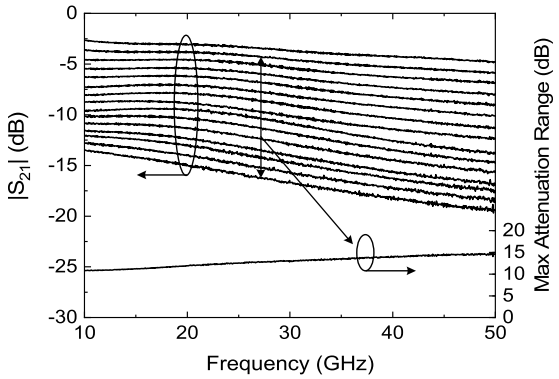

Fig. 19. Measured attenuation and the maximum attenuation range of Att2_TW.

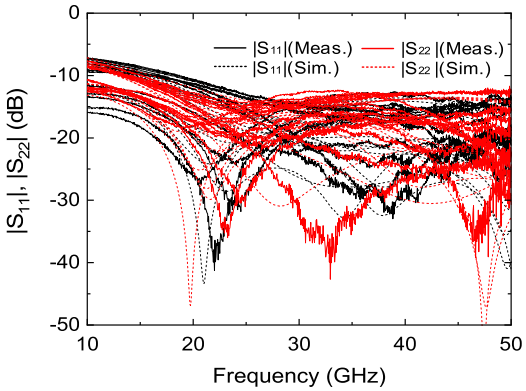

Fig. 20. Measured input and output return loss of Att2_TW.

due to the use of triple-well nFETs with the body floated. The input and output return losses are higher than 8.8 dB at all attenuation states over 15–43 GHz, as shown in Fig. 20. The linearity measurement is shown in Fig. 21, indicating $P_{\text{in,1 dB}}$ of 14 dBm at 35 GHz.

Fig. 22 shows the measured rms amplitude and phase errors. The rms amplitude error and phase error vary from 0.3 to 1.7 dB and from 1 to 6°, respectively, over the frequency of 15–43 GHz. Although the rms phase error was originally designed to have the minimum at around 40 GHz, the frequency is shifted down to 25 GHz in the measurement. This

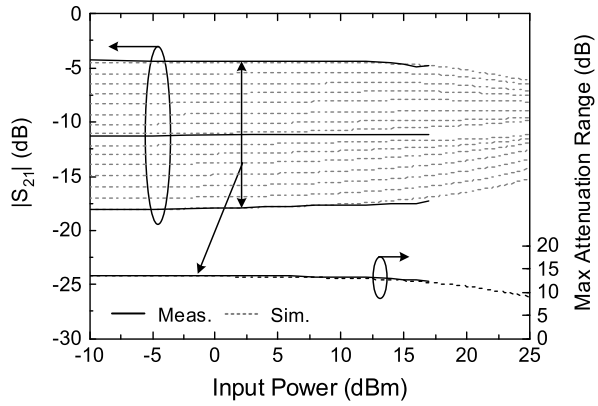

Fig. 21. Measured attenuation range versus input power at 35 GHz of Att2_TW.

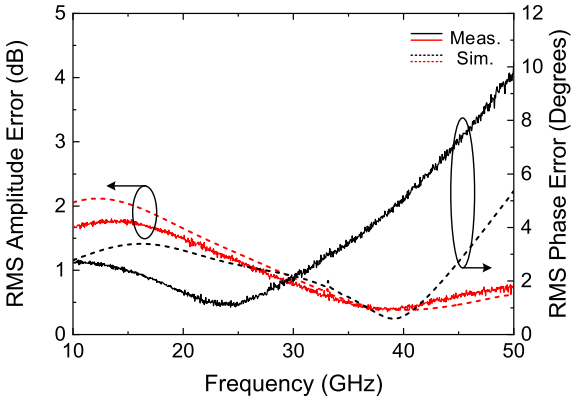

Fig. 22. Measured RMS phase error and RMS amplitude error of Att2_TW.

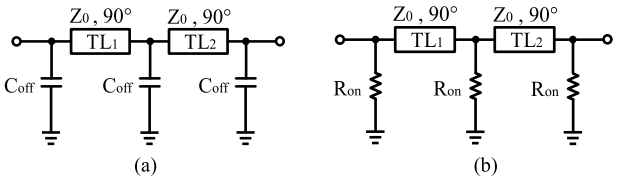

Fig. 23. Equivalent circuits of conventional distributed attenuator in (a) reference state and (b) 3-dB attenuation state.

results in a rapid increase in phase error as the frequency increases above 30 GHz. This unfortunately limits the operating bandwidth of Att2_TW up to 43 GHz. The reason for the frequency shift is believed in part that the coupling between TL_1 and TL_2 (Fig. 9) that are close to each other in the layout was not considered in the simulation during the design stage.

C. Performance Comparison

The performance of the proposed distributed digital attenuators is summarized and compared with those of the state of the arts in Table V. Compared with most other attenuators, this work achieves lower insertion loss, wider bandwidth, and compact chip size by adopting the proposed distributed topology. Compared with other compact attenuators [9], [12], [13], this work presents a larger attenuation range with a smaller or at least similar chip size.

TABLE V
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART DIGITAL ATTENUATORS

Ref.	Technology	Topology	BW (GHz)	Atten. Range / Step (dB)	Insertion Loss (dB)	$P_{in,1dB}$ (dBm)	Return Loss (dB)	RMS Phase Error (deg)	RMS Amp. Error (dB)	Size* (mm^2)
[5]	0.15-μm GaAs	Switched T	DC-40	23 / 1	4-10	n/a	14	n/a	n/a	4.48
[6]	0.15-μm GaAs	Switched Pi	40-50	31.5 / 0.5	6.5-8	n/a	9	n/a	0.5-0.9	1.89
[7]	0.15-μm GaAs	Switched path	40-50	30 / 2.5	8	n/a	14.5	< 7	n/a	n/a
[9]	0.18-μm BiCMOS	Switched T/Pi	36-52	8 / 1	4.4-5.9	20 @44GHz	9.7	1.9-6.7	0.8-1.4	0.22
[10]	0.18-μm BiCMOS	Switched T/Pi	22-29 57-64	16 / 1	5.4-7.9 10.5-11.1	14 @24GHz 11 @60GHz	10 10	1-4.7 2.3-3.6	0.49-0.51 0.93-1.5	0.94
[11]	0.18-μm BiCMOS	Switched T/Pi /Distributed	10-67	40 / 3	8.4-15.2	15 @35GHz	8.7	n/a	n/a	0.77
[12]	0.12-μm BiCMOS	Distributed	10-50	11 / 1	2-3	4 @ 35GHz	9	0.9-3	n/a	0.15
[13]	65-nm CMOS	Distributed	50-110	10 / 0.75	5.6-11.2	17 @ 80GHz	15	1.4	n/a	0.38
This work	**65-nm CMOS (Att1)**	**Distributed**	**10-50**	**14 / 1**	**2.6-6.2**	**15 @35GHz**	**8.7**	**0.8-4.5**	**0.3-2.2**	**0.19**
This work	**65-nm CMOS (Att2_TW)**	**Distributed**	**15-43**	**14 / 1**	**2.9-4.3**	**14 @35GHz**	**8.8**	**1-6**	**0.3-1.7**	**0.29**

*The probing pads are excluded.

V. CONCLUSION

A new compact distributed digital attenuator is proposed and demonstrated. By combining multiple attenuation unit cells at a single node along T-lines, a large attenuation range is achieved with a compact chip size compared with conventional distributed attenuators. A stacked-FET structure is employed to increase the linearity. To validate the proposed topology, two mm-wave 14-dB digital attenuators are demonstrated using a 65-nm CMOS technology. The first attenuator using regular nFETs exhibits 6.2 dB over 10–50 GHz with the input 1-dB compression power of 15 dBm at 35 GHz. The other attenuator using triple-well nFETs exhibits a lower insertion loss of 2.9–4.3 dB over 15–43 GHz at the expense of more chip area consumption. The input 1-dB compression power at 35 GHz is 14 dB. Both attenuators occupy a compact chip area as small as 0.19 and 0.29 mm^2, respectively. The measured result confirms that the proposed topology efficiently mitigates a well-known traditional tradeoff between the attenuation range and the chip area consumption of the conventional distributed attenuators.

APPENDIX

Equations (1) and (2) are derived as follows. The conventional attenuator of Fig. 2(a) reduces to the equivalent circuits of Fig. 23(a) and (b) in the reference and 3-dB attenuation states. The *ABCD* matrices of each equivalent circuit $A_{\text{ref}}^{\text{conv}}$ and $A_{\text{3dB}}^{\text{conv}}$ are calculated as

$$\begin{aligned} A_{\text{ref}}^{\text{conv}} &= \begin{bmatrix} 1 & 0 \\ j\omega C_{\text{OFF}} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_0 \\ \dfrac{j}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{\text{OFF}} & 1 \end{bmatrix} \\ &\quad \times \begin{bmatrix} 0 & jZ_0 \\ \dfrac{j}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{\text{OFF}} & 1 \end{bmatrix} \\ &= \begin{bmatrix} \omega^2 C_{\text{OFF}}^2 Z_0^2 - 1 & -j\omega C_{\text{OFF}} Z_0^2 \\ j(\omega^3 C_{\text{OFF}}^3 Z_0^2 - 2\omega C_{\text{OFF}}) & \omega^2 C_{\text{OFF}}^2 Z_0^2 - 1 \end{bmatrix} \end{aligned} \tag{11}$$

$$\begin{aligned} A_{\text{3dB}}^{\text{conv}} &= \begin{bmatrix} 1 & 0 \\ \dfrac{1}{R_{\text{ON}}} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_0 \\ \dfrac{j}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \dfrac{1}{R_{\text{ON}}} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_0 \\ \dfrac{j}{Z_0} & 0 \end{bmatrix} \\ &\quad \times \begin{bmatrix} 1 & 0 \\ \dfrac{1}{R_{\text{ON}}} & 1 \end{bmatrix} \\ &= \begin{bmatrix} -\dfrac{R_{\text{ON}}^2 + Z_0^2}{R_{\text{ON}}^2} & -\dfrac{Z_0^2}{R_{\text{ON}}} \\ -\dfrac{2R_{\text{ON}}^2 + Z_0^2}{R_{\text{ON}}^3} & -\dfrac{R_{\text{ON}}^2 + Z_0^2}{R_{\text{ON}}^2} \end{bmatrix}. \end{aligned} \tag{12}$$

Then, (1) is obtained by converting (11) into S-matrix and taking S_{21}. Equation (2) is obtained from (12) in the same manner.

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Kwangwon Park received the B.S. and M.S. degrees from the School of Electrical Engineering, Korea University, Seoul, South Korea, in 2018 and 2020, respectively.

Since 2020, he has been a full-time Instructor in electronics engineering with the Korea Air Force Academy, Cheongwon, South Korea. His research interests include microwave and millimeter-wave integrated circuits and systems.

Seungjong Lee is currently pursuing the B.S. degree in electrical engineering at Korea University, Seoul, South Korea.

His research interests include millimeter-wave and terahertz integrated circuits.

Sanggeun Jeon (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2004 and 2006, respectively.

From 1999 to 2002, he was a full-time Instructor in electronics engineering with the Korea Air Force Academy, Cheongwon, South Korea. From 2006 to 2008, he was a Research Engineer with the Caltech High-Speed Integrated Circuits Group, where he was involved with CMOS phased-array receiver design. Since 2008, he has been with the School of Electrical Engineering, Korea University, Seoul, where he is currently a Professor. His research interests include integrated circuits and systems at microwave, millimeter-wave, and terahertz bands for high-speed wireless communication and high-resolution imaging applications.