A 6 Bit Vector-Sum Phase Shifter With a Decoder Based Control Circuit for X-Band Phased-Arrays

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***Abstract*—This letter presents a 6 bit vector-sum phase shifter with a novel control circuitry for X-band phased-arrays using a 0.25 μm SiGe BiCMOS technology. A balanced active balun and highly accurate I/Q network are employed to generate the reference in-phase and quadrature vectors. The desired phase is synthesized by modulating and summing the generated reference vectors using current steering VGAs that are controlled by a decoder based control circuit. The phase shifter resulted in a measured RMS phase error $<2.8^\circ$ between 9.6–11.7 GHz and $<5.6^\circ$ between 8.2–12 GHz, achieving 6 bit phase resolution. The chip size is 1.87 $\times$ 0.88 mm^2, excluding pads. To the best of authors' knowledge, this is the first demonstration of a digitally controlled 6 bit vector-sum phase shifter for X-band.**

***Index Terms*—Phased-arrays, vector-sum phase shifters, X-band.**

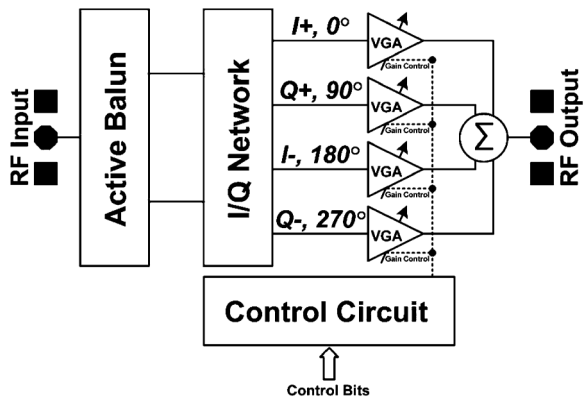

Fig. 1. Block diagram of the vector-sum phase shifter.

I. Introduction

PHASE shifters are the most essential elements in phased-arrays since they provide fast beam-steering to the systems and control the scanning phase of each T/R module. The scanning resolution and sidelobe levels of phased-arrays are directly related to the number of different phase states that can be generated by the phase shifters. In order to achieve high resolution scanning and avoid complex system level calibrations, phase shifters that will be implemented in phased-arrays should have high phase resolution.

A variety of fully integrated phase shifter topologies that are based on passive networks such as high-pass/low-pass switched-type circuits have been demonstrated [1]–[3]. Even though the passive phase shifter topologies can maintain excellent large signal capabilities, they lack high phase resolution, bring large insertion loss to the systems and occupy large chip areas. Therefore, passive phase shifters are not always suitable to be implemented in phased-arrays.

Compared to passive phase shifters, vector-sum architectures can provide exceptional phase resolution and gain in smaller chip areas [4]–[7]. Thus, vector-sum architecture is a prime candidate to be implemented in next-generation phased-arrays. However, performance of the control circuits can be a bottleneck for the phase resolution performance of vector-sum phase shifters. This work focuses on important design considerations and a novel approach to achieve a robust and high phase resolution vector-sum phase shifter by implementing a decoder based control circuit.

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II. Circuit Design

Fig. 1 presents the block diagram of the implemented phase shifter. Vector-sum method is selected as the topology since this method offers higher number of phase states in a smaller chip area with respect to the passive phase shifter topologies [1]–[3]. In order to achieve high phase resolution over a wide bandwidth such as in this work, both phase and amplitude performances of the balun and I/Q network as well as the performances of the VGAs becomes critical. Phase resolution bandwidth in this vector-sum topology depends mainly on the accuracy of the generated in-phase and quadrature reference vectors. Therefore, selection of the balun and I/Q network topologies are crucial. Another key point is designing identical VGAs in order to minimize effects of parasitics in the summation operation.

The active balun is based on the common-base common-emitter (CB-CE) pair type topology to provide a quality differential input signal to the I/Q network as presented in Fig. 2. Amplitude balance and desired phase imbalance (180°) between the outputs of the balun needs to be preserved in the operation bandwidth to ensure the desired performance of the I/Q network. The input signal enters the CB pair from the emitter and arrives at the collector. Simultaneously, the input signal enters the base of the CE pair and arrives at the collector with 180° phase shift relative to output of the CB pair. Thus, the differential input signal necessary for the I/Q network is generated. We observed at a simulation level that the undesired amplitude and phase imbalances between the outputs of the balun are <0.1 dB and $<0.1^\circ$.

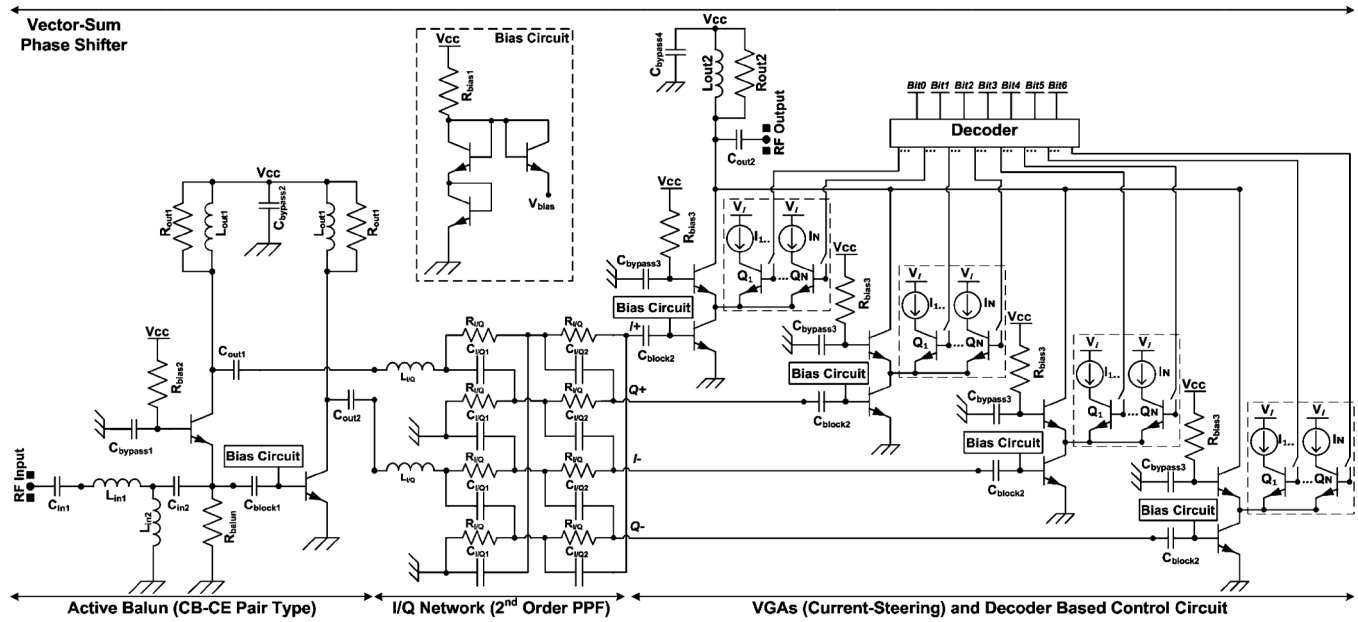

Fig. 2. Detailed schematic of the vector-sum phase shifter.

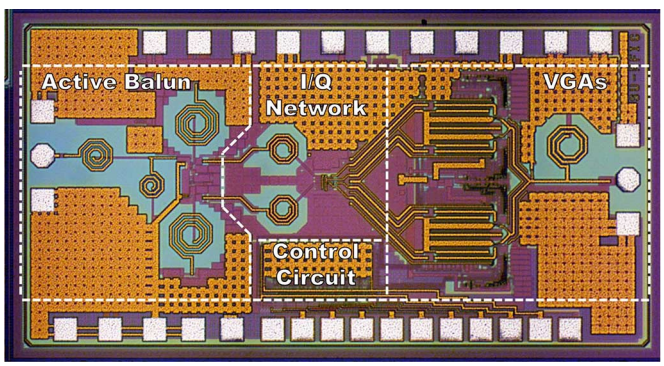

Fig. 3. Die photo of the vector-sum phase shifter.

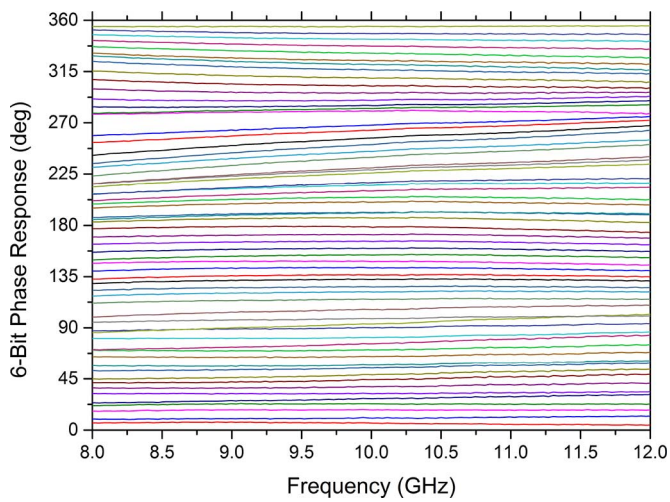

Fig. 4. Measured relative phase response of the vector-sum phase shifter.

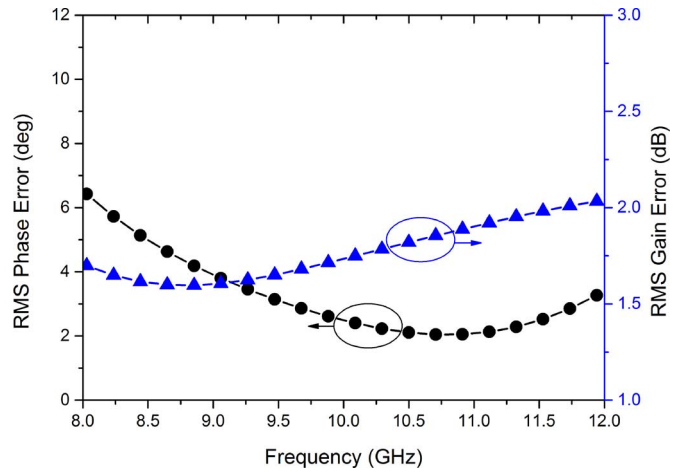

Fig. 5. Measured RMS phase/gain error of the vector-sum phase shifter.

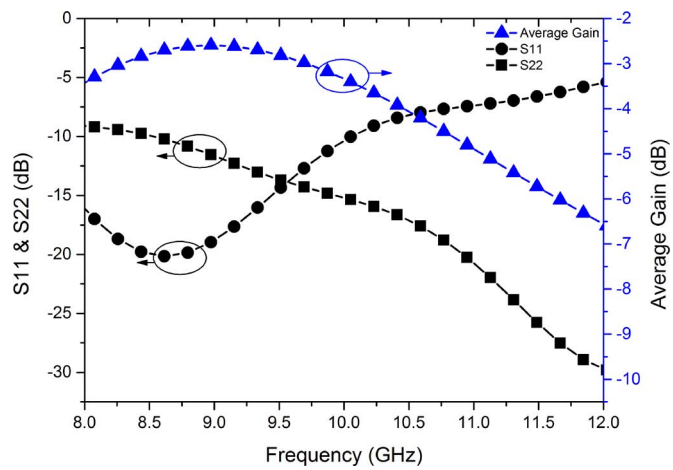

Fig. 6. Measured input/output return losses and average gain of the vector-sum phase shifter.

I/Q network is used to generate the reference in-phase and quadrature reference vectors. Considering that the accuracy of the synthesized phase is sensitive to any unexpected amplitude and phase error between the reference vectors, I/Q network topology should be selected and designed with great caution. An ideal I/Q network should maintain the desired amplitude and phase relationships between it's outputs over the bandwidth of operation. To achieve robustness against different corners and generate the reference vectors accurately over a wide frequency range, a constant-phase second order polyphase filter

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

	[1]	[2]	[5]	This work
Technology	0.18-μm SOI	0.13-μm BiCMOS	0.18-μm BiCMOS	0.25-μm BiCMOS
Method	Switched Type	Switched Type	Vector Sum	Vector Sum
Frequency (GHz)	8-12	8-12	6-18	8-12
Number of bits	5	5	5	6
Phase range (deg)	360 /11.25	360 /11.25	360 /11.25	360 /5.625
Gain (dB)	<-11	<-20	<19.5	<-2.5
RMS gain error (dB)	<0.5	-	<1.1	<2
RMS phase error (deg)	<6.5	<9.1	<5.6	<6.4
Input P1dB (dBm)	10	-	-40	-11
Power consumption (mW)	0	<1	61	110
Size (mm^2)	1.14 ×0.78	1.8×2.7	1.2×0.75	1.87×0.88

(PPF) is implemented as shown in Fig. 2. Phase difference between the outputs will be 90° at all frequencies as desired and amplitude balance between the outputs will be achieved at the pole frequencies of the each stage at the expense of high signal loss. We observed at a simulation level that the undesired amplitude imbalance between the outputs of the I/Q network are <0.17 dB

$$\theta_{\text{desired}} = \angle \tan^{-1}(Q_{o\pm}/I_{o\pm}),$$
$$K = \sqrt{{A_{I_{o\pm}}}^2 + {A_{Q_{o\pm}}}^2}. \quad (1)$$

Last stage of the vector-sum phase shifter consists of four identical VGAs and a novel decoder based conrol circuit as shown in Fig. 2 to generate the desired phase state. In order to have control over the amplitude weighting of each reference vector, cascode amplifiers with current steering transistors are implemented as VGAs. $I_1, \ldots, I_N$ are different amounts of currents mirrored from a current source over the collectors of the $Q_1, \ldots, Q_N$ HBTs that are acting as switches for the current steering operation. The switching of the HBTs are controlled by the outputs of the decoder circuit. When VDD state is applied to the base of a current-switch HBT, the amount of mirrored current to it's collector is steered from the cascode. Thus, variable gain operation is achieved. When 0 V state is applied to a base of a current-switch HBT, no current is steered from that cascode and the gain stays unchanged. Unlike popular VGA topologies used in vector-sum phase shifters such as Gilbert-Cell type VGAs, total current consumed by the transistors seen by the outputs of the PPF stays the same with the current steering VGAs. Thus, undesired asymmetry between the outputs of the polyphase filter that could corrupt the reference vector generation is minimized. $I_1, \ldots, I_N$ currents and output states of the decoder are calculated and optimized using the equations in (1) and the simulation results so that the vector summation operation between the $I_\pm$ and $Q_\pm$ cascodes results in the desired phase and relationship between the output phase and control bit sequence is linear. K is the selected constant amplitude for the vector summation output, $A_{I_{o\pm}}$ and $A_{Q_{o\pm}}$ are the amplitudes of the selected reference vectors as a function of the steered current from the VGAs. Finally, vector summation is done in the current domain by connecting the outputs of the VGAs to a common load. When summing two reference vectors, remaining reference vectors' VGAs are turned off by steering all of their currents, in order to cancel out their undesired effects in the summation operation.

III. MEASUREMENT RESULTS

The vector-sum phase shifter is realized in IHP SG25H3 0.25 μm SiGe BiCMOS technology. The chip size is 1.87×0.88 mm^2, excluding pads. Fig. 4 shows the measured 6 bit phase response of the vector-sum phase shifter. The measured RMS phase and RMS gain errors are shown in Fig. 5. The measured RMS phase error is $< \text{LSB}/2$ (2.8°) between 9.6–11.7 GHz and $<$ LSB (5.6°) between 8.2–12 GHz, achieving 6 bit phase resolution. The measured RMS gain error is $\leq$2 dB between 8–12 GHz. Fig. 6 shows the input and output return losses and the average gain of the phase shifter. Total current consumption of the active balun is 20 mA from 2.5 and 3 V supplies for the CB and CE pair respectively. Each VGA consumes 5.5 mA from a 2.5 V supply. The phase shifter has a total power consumption of 110 mW.

IV. CONCLUSION

This letter has demonstrated a novel approach to achieve a high phase resolution vector-sum phase shifter by implementing a decoder based control circuit. The proposed control method results in additional power consumption compared to other vector-sum phase shifter designs. However, high phase resolution and low RMS phase error over a wide bandwidth is achieved. Measured results prove that the demonstrated architecture is suitable to be implemented in next-generation high performance phased-arrays.

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