Design and Analysis of a Low Loss, Wideband Digital Step Attenuator With Minimized Amplitude and Phase Variations

Ickhyun Song, *Member, IEEE*, Moon-Kyu Cho, *Member, IEEE*, and John D. Cressler, *Fellow, IEEE*

***Abstract*— A compact, low loss, wideband digital step attenuator (DSA) is presented. The proposed DSA utilizes amplitude/phase-compensated T-type attenuator cells, in which the locations of poles and zeros are manipulated for minimizing variations in attenuation and phase. In addition, the reduced T-type attenuator cells that eliminate series switch transistors are used to achieve low insertion loss (IL). These techniques provide wideband (dc-20 GHz) operation for the DSA, with significantly decreased attenuation/phase errors and reduced IL. The DSA was implemented in a 130-nm silicon-germanium (SiGe) BiCMOS platform. The full attenuator circuit has binary-coded 6-bit digital control inputs with a least significant bit of 0.5-dB attenuation. It has a root-mean-square (rms) attenuation error of 0.37 dB and an rms phase error of 4°, both at 20 GHz. The IL and the input 1-dB compression point at 10 GHz are 4 dB and 10 dBm, respectively. The active core layout area is 0.14 mm^2 (1.0 mm × 0.14 mm).**

***Index Terms*— Attenuation/phase error compensation, attenuator, digital step attenuator (DSA), insertion loss (IL), modified switched T-type, passive, reduced switched T-type, silicon-germanium (SiGe) BiCMOS, wideband.**

I. Introduction

ATTENUATORS are one of the key building blocks in many RF communications, radar, and measurement systems. The primary function of attenuators is to provide amplitude control for various purposes such as linearity adjustment and damage protection [1], [2]. With regard to phased array applications, attenuators should provide an accurate control for sidelobes in antenna radiation patterns [3]. While as a gain control element variable-gain amplifiers (VGAs) perform a similar function, they typically exhibit one or more limitations, consisting of: large amplitude/phase variation, narrow bandwidth, limited linearity, unidirectional operation, and large power consumption, complex system configuration (due to RF chokes or biasing) [4]–[9] compared to passive-type attenuators, all of which can be detrimental to the realization of wideband large-scale phased array systems. From this perspective, passive digital step attenuators (DSAs) are more attractive, since they can provide most of the following advantages, including wide bandwidth, fine amplitude control, high linearity, bidirectional operation, reduced amplitude and phase variations, and simple system configurations [10]–[13].

In passive DSAs, three topologies have been investigated in the literature: distributed, switched-path, and switched π-/T-type attenuators [11], [13]–[18]. First, distributed step attenuators provide wide bandwidth and low insertion loss (IL) among passive DSAs. However, they exhibit low values of maximum attenuation (e.g., <10–15 dB), large chip size due to the use of transmission lines, and performance degradation in a low gigahertz region [13], [14]. Second, switched-path step attenuators have advantages of low amplitude and phase variations (e.g., <0.5 dB, 5°, respectively), but they often suffer from high IL and large chip size due to the use of many series switches and lumped inductors, respectively [15], [16]. Finally, switched π-/T-type step attenuators show low IL, high maximum attenuation (e.g., >30 dB), and compact size, which are attractive features in large phased array systems. However, they still have the drawbacks of relatively high attenuation variation (2–3 dB) that potentially limit a fine amplitude control (e.g., attenuation variations <1 dB) in wideband applications [11], [17], [18].

Recently, several techniques for compensating amplitude and phase variations of switched π-/T-type step attenuators have been proposed [3], [19]–[21]. Either the inductive or the capacitive amplitude/phase compensation techniques is able to reduce such variations, but capacitive compensation is better suited for large-scale wideband phased array systems [3], [20], [21] than the inductive compensation due to the size increase associated with the inductors [19]. While the compensation solution proposed in [3] is very simple and effective in the minimization of amplitude/phase variations, only a qualitative, first-order description of the approach has been addressed in the literature [3], [22], which over simplified the detailed physics and behavior associated within such structures.

In this paper, we present an in-depth, thorough investigation of the amplitude/phase compensation technique, based on pole-zero analysis. By developing the analytic equations for the conventional and the modified T-type attenuator cells, the locations of poles and zeros can be found, and then the mechanisms of the reduction in amplitude/phase variations can be explained. As an example of the application of this analysis, the design and the characterization of a 6-bit DSA in a silicon-germanium (SiGe) BiCMOS platform is demonstrated. The

Manuscript received September 15, 2017; revised February 13, 2018 and April 5, 2018; accepted April 9, 2018. Date of publication May 4, 2018; date of current version July 20, 2018. This paper was approved by Associate Editor Woogeun Rhee. *(Corresponding author: Moon-Kyu Cho.)*

The authors are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA (e-mail: ihsong@gatech.edu; mcho79@mail.gatech.edu; cressler@ece.gatech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2018.2827934

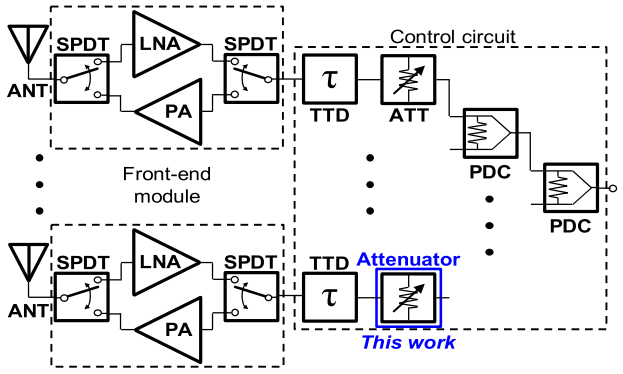


Fig. 1. Configuration of a wideband phased array transceiver chipset. It includes switchable front-end modules and bi-directional control circuit block. ANT: antenna. SPDT: single-pole double-throw. LNA: low-noise amplifier. PA: power amplifier. TTD: true-time delay. ATT: attenuator. PDC: power divider/combiner).

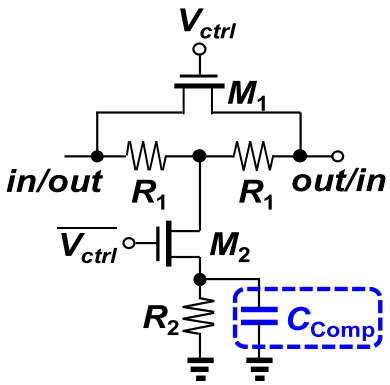


Fig. 2. Schematic of a switched T-type attenuator cell. The conventional attenuator topology includes all components except C_{Comp}, while the modified schematic utilizes C_{Comp} for compensating attenuation and phase errors. Large bias resistors at the transistor gate terminals are not shown.

DSA is intended for a multi-channel wideband phased array transceiver (T/R) system, which consists of antennas, front-end modules, and bidirectional control circuits, as shown in Fig. 1. The designed DSA employs not only the capacitive compensation technique but also the loss minimization scheme [23]–[25] for maximized performance over the entire bandwidth (from dc to 20 GHz). For comparison purposes, the performance of the conventional T-type DSA without the amplitude/phase compensation is also presented. Section II describes the detailed analysis of the amplitude/phase compensation technique compared with a conventional T-type attenuator cell. In addition, the effects of the loss minimization technique will be investigated. In Section III, the measured results will be shown, followed by discussion, and Section IV will summarize this paper.

II. DSA With Modified T-Type Attenuation Cells

A. Limitations of Conventional T-Type Switched Attenuators

The schematic of a switched T-type attenuator cell is shown in Fig. 2. The conventional design includes T-type resistors (R_1 and R_2) for attenuation, and series/shunt transistors (M_1 and M_2) for mode switching [19], whereas the modified attenuator cell utilizes an additional capacitor C_{Comp}

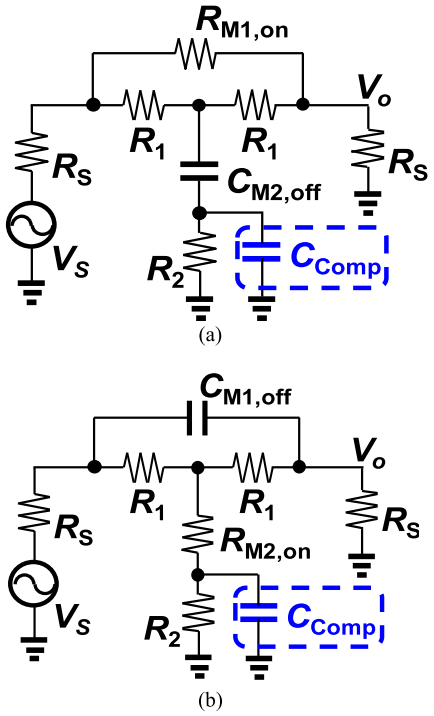


Fig. 3. Simplified small-signal equivalent circuits for (a) reference state and (b) attenuation state.

(the dashed box in Fig. 2). Under a reference (no attenuation) state, the large series transistor (M_1) provides a low-loss path from the input to the output. Under an attenuation state, M_1 is OFF and the two resistors, R_1 and R_2, and together with the fully turned-ON shunt transistor M_2 form a T-type network. Given the required attenuation A (in decibel) and the characteristic impedance Z_0, ideal values of R_1 and R_2 can be calculated using the following equations [26]:

$$R_1 = Z_0 \cdot \left(\frac{10^{A/20} - 1}{10^{A/20} + 1} \right) \tag{1}$$

$$R_2 = 2 \cdot Z_0 \cdot \left(\frac{10^{A/20}}{10^{A/10} - 1} \right) - R_{M2,\mathrm{ON}}. \tag{2}$$

In (2), $R_{M2,\mathrm{ON}}$ is the ON-state resistance of the shunt transistor M_2. While the conventional T-type cells offer a simple structure and accurate attenuation, they often suffer from two limitations: 1) large amplitude/phase variations and 2) high IL in a high-frequency region, which prohibits wideband operation. The former is mainly attributed to the change in parasitic capacitance when the transistors are either turned ON or OFF, while the latter is mainly associated with the ON-state resistance of the series transistor.

First, the amplitude and the phase variations associated with attenuator cells can be analyzed from their small-signal equivalent circuits. In Fig. 3, the equivalent circuits are shown, depending on the operational states. For simplicity, a switch transistor (M_1, M_2) is modeled as either a resistor for an ON-state ($R_{M1,\mathrm{on}}$ and $R_{M2,\mathrm{on}}$) or a capacitor ($C_{M1,\mathrm{off}}$ and $C_{M2,\mathrm{off}}$) for an OFF-state. The resistor and the capacitor represent the channel resistance and the combined capacitance

TABLE I
PARAMETER VALUES FOR AN 8-DB ATTENUATOR CELL

R_1	22.5 Ω	R_2	37.6 Ω
$R_{M1,on}$	4.3 Ω	$C_{M1,off}$	74.5 fF
$R_{M2,on}$	10.3 Ω	$C_{M2,off}$	33.7 fF

in the oxide, junction, and substrate regions of the transistor, respectively. While this first-order approximation does not reflect the complex response of the attenuator cells at high frequencies, due to the omission of many parasitic components, we can more easily understand their frequency behavior from a dominant pole-zero analysis for the band of interest, thus providing useful insight. In order to find the locations of poles and zeros, the transfer functions of the conventional attenuator cells under a reference state and an attenuation state are derived, as shown in equations (3) and (4), at the bottom of this page.

As an example, we present the frequency response of an 8-dB attenuation cell, since three identical 8-dB cells will be used in the final DSA schematic. Inspecting (3) and (4), we expect the attenuator cell has one pole and one zero in both states, and their corresponding poles and zeros are obtained from the following equations:

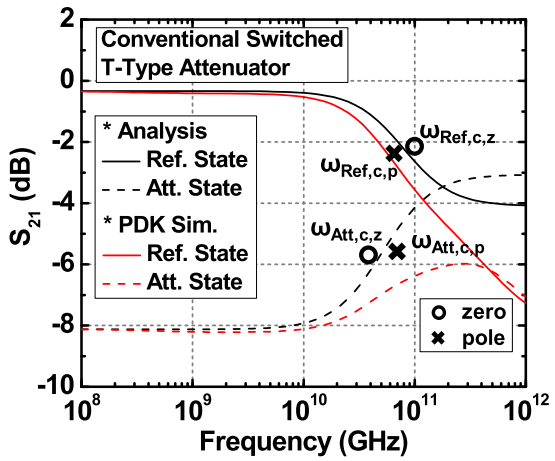
$$f_{\text{Conv,Ref},z} = \frac{2R_1 + R_{M1,\text{ON}}}{2\pi C_{M2,\text{OFF}}\left(R_1^2 + 2R_1R_2 + R_2R_{M1,\text{ON}}t\right)} \tag{5}$$

$$f_{\text{Conv,Ref},p} = \frac{1}{\pi C_{M2,\text{OFF}}(R_1 + 2R_2 + R_S)} \tag{6}$$

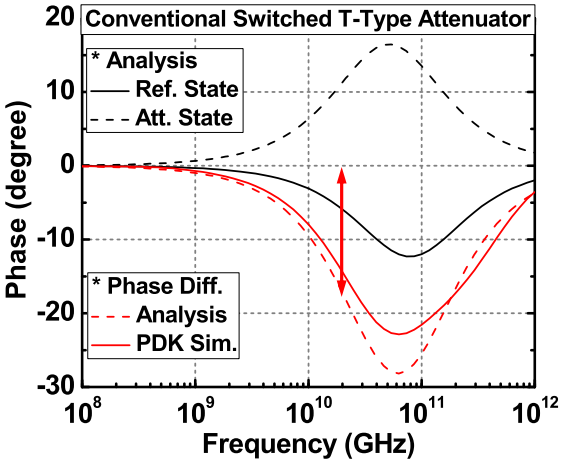
$$f_{\text{Conv,Att},z} = \frac{R_2 + R_{M2,\text{ON}}}{2\pi C_{M1,\text{OFF}}\left(R_1^2 + 2R_1R_2 + 2R_1R_{M2,\text{ON}}\right)} \tag{7}$$

$$f_{\text{Conv,Att},p} = \frac{R_1 + R_S}{4\pi C_{M1,\text{OFF}}R_1R_S}. \tag{8}$$

Using the values from Table I, which summarizes reasonably optimized values for the 8-dB attenuation, we see that the pole ($\omega_{\text{Ref},c,p}$) first appears at 60 GHz, and a zero ($\omega_{\text{Ref},c,z}$) is at 100 GHz in the reference state, as shown in Fig. 4(a). On the other hand, in the attenuation state, a zero ($\omega_{\text{Att},c,z}$) is located at 40 GHz and a pole ($\omega_{\text{Att},c,p}$) comes next at 70 GHz. Since the changes in S_{21} slope and phase for a pole and a zero are opposite from each other, the resulting amplitude variations become worse as frequency increases, thereby limiting the operational bandwidth of the attenuator cell. In Fig. 4(b), the phase response of both the ON- and OFF-states is shown. As expected from the amplitude response in Fig. 4(a), the phase variation monotonically increases until 60 GHz. It should be noted that the simulation results were made using a process design kit (PDK), and show a different frequency behavior at high frequencies. This is expected, since



(a)



(b)

Fig. 4. (a) Frequency response of a conventional T-type 8-dB attenuator cell. The parameters in Table I are used for the pole-zero calculation in (5)–(8). For simulation results, a PDK was used. (b) Phase response of the same 8-dB attenuator cell.

the accurate PDK model includes numerous poles and zeros which are not revealed at low frequencies.

Second, the conventional switched T-type attenuator inevitably exhibits finite IL since the ON-state resistance of a series transistor cannot be zero. While a large-sized series transistor can reduce the ON resistance, an excessive increase in parasitic capacitance moves a pole and a zero to lower frequencies, as implied from (3) and (4). In Fig. 5, the simulated IL and bandwidth of the conventional switched T-type 8-dB attenuator cell are presented. In this simulation, the bandwidth is defined as the frequency at which the amplitude variation equals to 0.5 dB. It is shown that lower IL can be achieved at the cost of the substantial reduction in the operational

$$T(s)_{\text{Conv,Ref}} = \frac{R_S\left[2R_1 + R_{M1,\text{ON}} + C_{M2,\text{OFF}}\left(R_1^2 + 2R_1R_2 + R_2R_{M1,\text{ON}}\right)s\right]}{(R_1R_{M1,\text{ON}} + 2R_1R_S + R_{M1,\text{ON}}R_S)[2 + C_{M2,\text{OFF}}(R_1 + 2R_2 + R_S)s]} \tag{3}$$

$$T(s)_{\text{Conv,Att}} = \frac{R_S\left[R_2 + R_{M2,\text{ON}} + C_{M1,\text{OFF}}\left(R_1^2 + 2R_1R_2 + 2R_1R_{M2,\text{ON}}\right)s\right]}{(R_1 + 2R_2 + 2R_{M2,\text{ON}} + R_S)(R_1 + R_S + 2C_{M1,\text{OFF}}R_1R_S \cdot s)}. \tag{4}$$

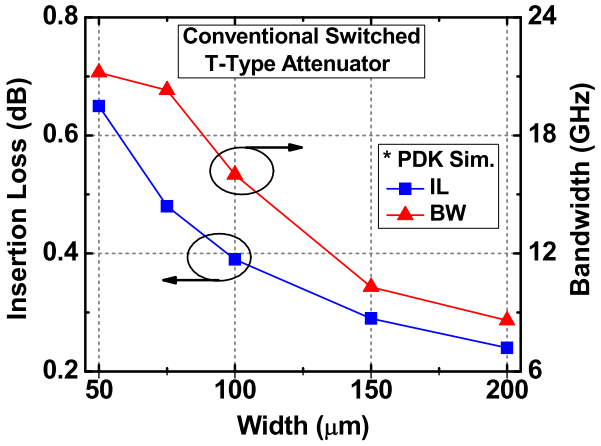


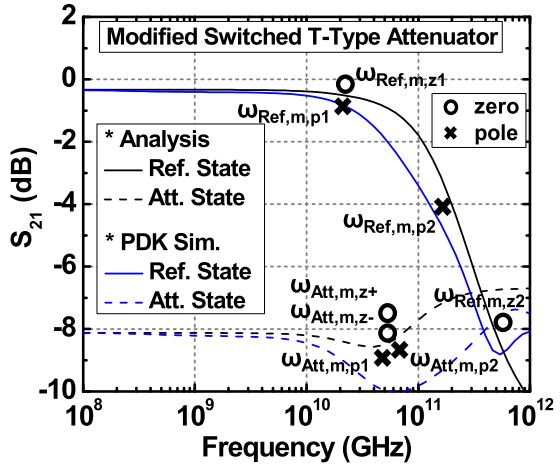
Fig. 5. Simulated IL and bandwidth of the conventional T-type 8-dB attenuator cell versus the width of the series transistor.

bandwidth of the attenuator cell. Therefore, it is important to eliminate series transistors as much as possible in order to avoid the tradeoff relationship.

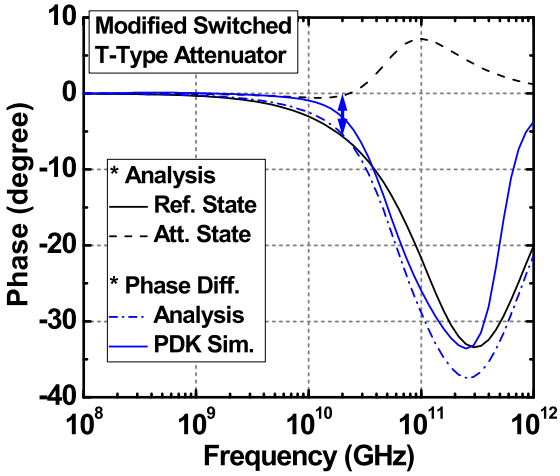
B. Amplitude/Phase-Compensated T-Type Attenuator Cell

The modified attenuator cell schematic, which includes an amplitude- and phase-compensation capacitor C_{Comp} [3], is shown in Fig. 2. The addition of C_{Comp} changes the attenuator cell (in Fig. 3) to become a two-pole, two-zero system (the denominators and the numerators are now in quadratic forms), as analytically derived in the following equations. The explanation in [3] and [22] briefly states that the inclusion of C_{Comp} extends the operational bandwidth due to the phase lagging associated with an additional pole or the introduction of a low-pass filter network under an attenuation state. However, closely located poles and zeros may affect the frequency behavior of an attenuator cell. In addition, under a reference state, the hidden pole-zero cancellation plays an important role in bandwidth extension.

With a careful selection of the C_{Comp} capacitance, the resulting frequency response an 8-dB attenuator cell is presented in Fig. 6(a). For the reference state, since both the first pole ($\omega_{\text{Ref},m,p1}$) and the first zero ($\omega_{\text{Ref},m,z1}$) appear at about 20 GHz, they effectively cancel each other, while the second pole ($\omega_{\text{Ref},m,p2}$) at 160 GHz becomes dominant. Hence, the flat-response bandwidth is extended compared with a conventional attenuator cell [Fig. 4(a)]. On the other hand, in the attenuation state, now a pole ($\omega_{\text{Att},m,p1}$) first appears at 47 GHz, shaping the S_{21} response similar to the reference state beyond 10 GHz. Two co-located zeros ($\omega_{\text{Att},m,z+}$ and $\omega_{\text{Att},m,z-}$) at 53 GHz raise the S_{21} slope to be positive, which is eventually compensated by the second pole ($\omega_{\text{Att},m,p2}$) at 70 GHz. This implies that the C_{Comp} capacitance can favorably modify the frequency response by adjusting the pole and zero locations so that the maximized operational bandwidth and the minimized attenuation and phase variations are achieved. The phase response of the modified attenuation cell is presented in Fig. 6(b). Compared with Fig. 4(b), the phase difference at



(a)



(b)

Fig. 6. (a) Frequency response of the modified T-type 8-dB attenuator cell. The parameters in Table I are used for the pole-zero calculation in (9) and (10). For simulation results, a PDK was used. (b) Phase response of the same 8-dB attenuator cell.

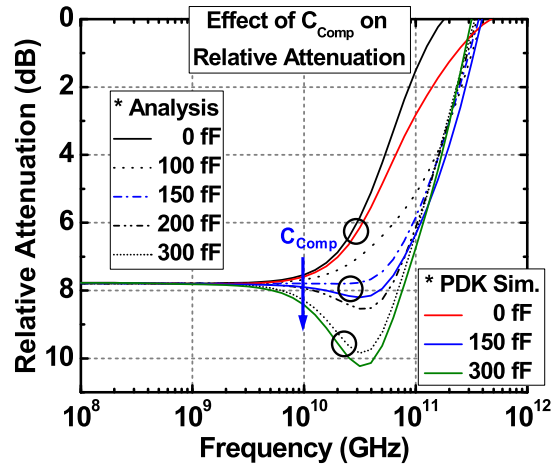
20 GHz is reduced from 18° to 6°

$$\omega_{\text{Att},m,p} = \frac{R_1 + 2R_2 + 2R_{M2,\text{ON}} + R_S}{C_{\text{Comp,init}}(R_1R_2 + 2R_2R_{M2,\text{ON}} + R_2R_S)} \tag{11}$$

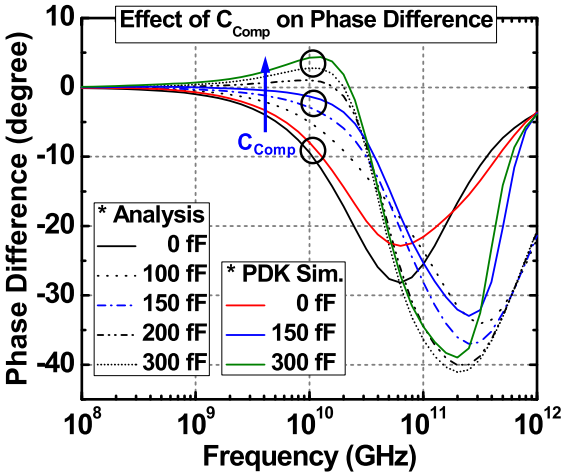
$$\omega_{\text{Att},m,z} = \left(\frac{R_2 + R_{M2,\text{ON}}}{C_{\text{Comp,init}}\left[C_{M1,\text{OFF}}\left(R_1^2R_2 + 2R_1R_2R_{M2,\text{ON}}\right)\right]}\right)^{1/2} \tag{12}$$

$$C_{\text{comp,init}} = \frac{C_{M1,\text{OFF}}R_1\left(R_1 + 2R_{M2,\text{ON}}\right)}{R_2\left(R_2 + R_{M2,\text{ON}}\right)} \times \left(\frac{R_1 + 2R_2 + 2R_{M2,\text{ON}} + R_S}{R_1 + 2R_{M2,\text{ON}} + R_S}\right)^2. \tag{13}$$

The calculation of the full analytical optimal capacitance of C_{Comp} for obtaining maximum bandwidth is cumbersome. However, finding a reasonable C_{Comp} capacitance is relatively simple, and this can be used for an initial value as a starting point. Since in the proposed circuit an additional dominant



(a)



(b)

Fig. 7. Effect of the compensation capacitor C_{Comp} on the frequency response of (a) relative attenuation and (b) phase difference. The direction of the arrows indicates the increasing capacitance. For comparison, a few PDK simulation results are added.

pole needs to appear earlier than the zeros in an attenuation state, we can find $C_{\mathrm{Comp,init}}$ when the lowest pole and the lowest zero locations are at the same frequency. Therefore, by equating (11) and (12), $C_{\mathrm{Comp,init}}$ can be calculated as (13). Using the parameter values in Table I, it shows a $C_{\mathrm{Comp,init}}$ of about 130 fF. For the maximized bandwidth, the optimal C_{Comp} should be slightly larger than $C_{\mathrm{Comp,init}}$ due to the co-located zeroes, so that the falling slope of S_{21} increases similar to the reference state response, as shown in Fig. 6(a).

TABLE II
THEORETICAL RESISTANCE FOR T-TYPE ATTENUATION

Attenuation (dB)	4	2	1	0.5
R_1 (Ω)	11.3	5.7	2.9	1.4
R_2 (Ω)	104.8	215.2	433.3	868.1

The optimal value of C_{Comp} is determined by graphically analyzing the relative attenuation and phase difference from (9) and (10), as shown at the bottom of this page. In Fig. 7(a), the relative attenuation with varying C_{Comp} is shown. When there is no compensation capacitance ($C_{\mathrm{Comp}} = 0$ fF), the relative attenuation decreases as the frequency increases at values higher than about 9 GHz, as expected from Fig. 4(a). The optimum C_{Comp} lies at around 150 fF, with which the maximum flat amplitude response is obtained. The similar result is observed in the phase difference plot, as shown in Fig. 7(b). In this case, C_{Comp} of 200 fF is optimal for the maximally flat phase difference between a reference state and an attenuation state. Therefore, a compensation capacitance between 150 and 200 fF should be chosen for the final design depending on the DSA specifications. In the present design, PDK-based simulations predict the optimal capacitance of about 155 fF, which minimized the phase variations under other design constraints such as impedance matching and attenuation errors.

C. Reduced T-Type Attenuator Cell

The dominant IL of the conventional attenuator cell is associated with the ON-state resistance of a series transistor. While this finite series resistance is inevitable in the switched T-type attenuator topology, however, there are certain cases in which the series transistor can be removed without loss of functionality. When the required attenuation for a given cell is as low as 0.5 or 1.0 dB, the theoretical resistances of R_1 and R_2 become smaller and larger, respectively. Table II summarizes the ideal values of R_1 and R_2 for different attenuations. For low attenuation cells, the role of the series resistance is much less significant than the shunt resistance in the overall response. This implies that the series resistance R_1 can be eliminated in the T-type network and the remaining series transistor is now redundant. The resulting reduced attenuator

$$T(s)_{\mathrm{Mod,Ref}} = \frac{R_S\left[2R_1 + R_{M1,\mathrm{ON}} + C_{M2,\mathrm{OFF}}\left(R_1^2 + 2R_1R_2 + R_2R_{M1,\mathrm{ON}}\right)s + C_{\mathrm{Comp}}(2R_1R_2 + R_2R_{M1,\mathrm{ON}})s + C_{M2,\mathrm{OFF}}C_{\mathrm{Comp}}R_1R_2 \cdot s^2\right]}{(R_1R_{M1,\mathrm{ON}} + 2R_1R_S + R_{M1,\mathrm{ON}}R_S)[2 + C_{M2,\mathrm{OFF}}(R_1 + 2R_2 + R_S) \cdot s + 2C_{\mathrm{Comp}}R_2s + C_{M2,\mathrm{OFF}}C_{\mathrm{Comp}}(R_1R_2 + R_2R_S)s^2]} \quad (9)$$

$$T(s)_{\mathrm{Mod,Att}} = \frac{R_S\left[R_2 + R_{M2,\mathrm{ON}} + C_{M1,\mathrm{OFF}}\left(R_1^2 + 2R_1R_2 + 2R_1R_{M2,\mathrm{ON}}\right)s + C_{\mathrm{Comp}}R_2R_{M2,\mathrm{ON}} \cdot s + C_{M1,\mathrm{OFF}}C_{\mathrm{Comp}}\left(R_1^2R_2 + 2R_1R_2R_{M2,\mathrm{ON}}\right)s^2\right]}{[R_1 + 2R_2 + 2R_{M2,\mathrm{ON}} + R_S + C_{\mathrm{Comp}}(R_1R_2 + 2R_2R_{M2,\mathrm{ON}} + R_2R_S)s](R_1 + R_S + 2C_{M1,\mathrm{OFF}}R_1R_S \cdot s)} \quad (10)$$

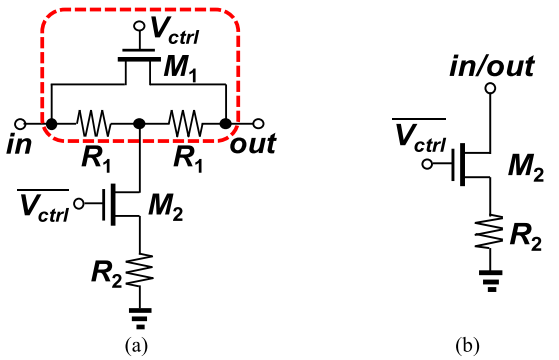


Fig. 8. (a) Schematic of the conventional T-type attenuator cell. (b) Schematic of the reduced T-type attenuator cell.

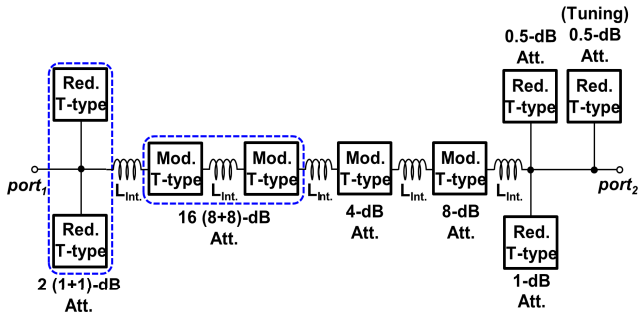


Fig. 10. Full schematic of the 6-bit digital-step attenuator. It consists of the modified and the reduced T-type attenuator cells. For 2-dB attenuation, two 1-dB cells are parallel-combined, while for 16-dB attenuation, two 8-dB cells are series connected.

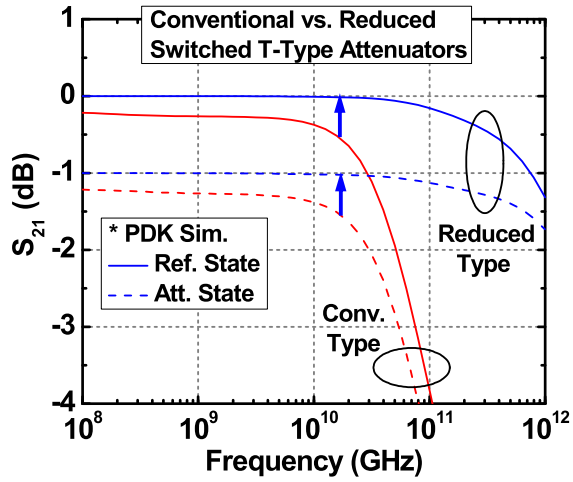


Fig. 9. (a) Simulated S_{21} under attenuation and reference states for both the conventional and the reduced cells. (b) Comparison of phase difference between attenuation and reference states for both attenuators. Matching results of the reduced attenuator is presented as well.

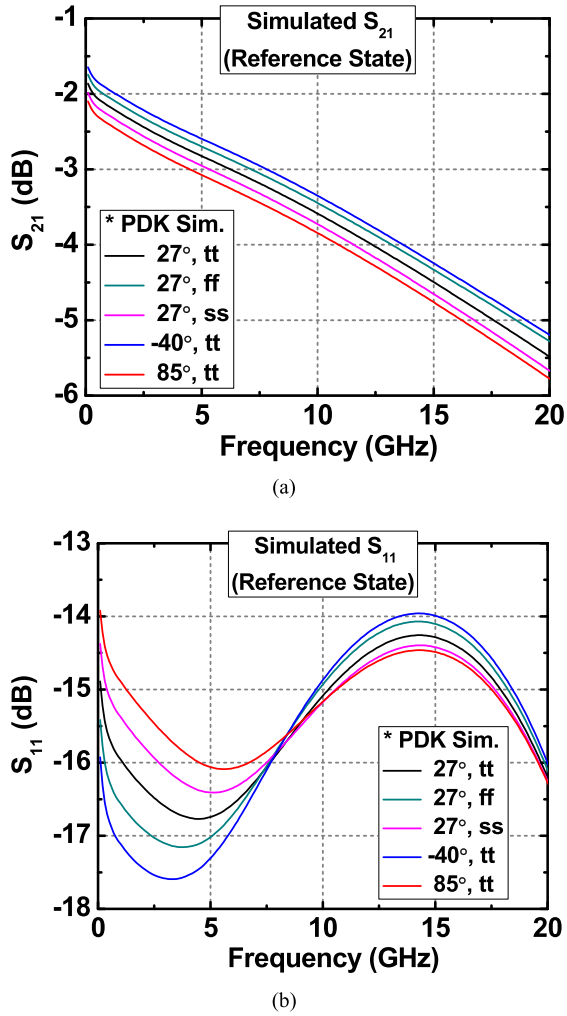


Fig. 11. Simulated performance variations of (a) S_{21} and (b) S_{11} under different process and temperature corners for the reference state.

cell schematic is shown in Fig. 8. From the conventional schematic in Fig. 8(a), R_1 and M_1 are removed and the required attenuation is achieved by adjusting R_2 and M_2 only [Fig. 8(b)] [23], [25].

In Fig. 9, the S-parameter response of the reduced T-type attenuator cell is presented. As an example, a 1-dB attenuator cell is selected for the comparison with the conventional design. The simulated S_{21} results of both the conventional and the reduced attenuator cells are shown in Fig. 9(a). While in both case, the required 1-dB attenuation is achieved,

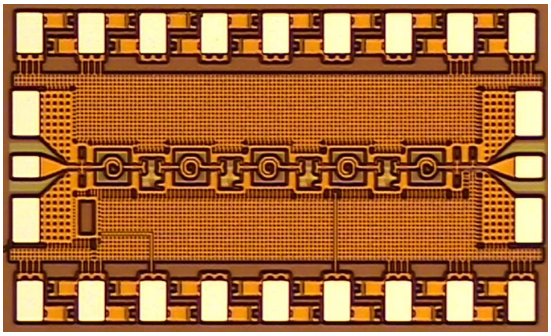
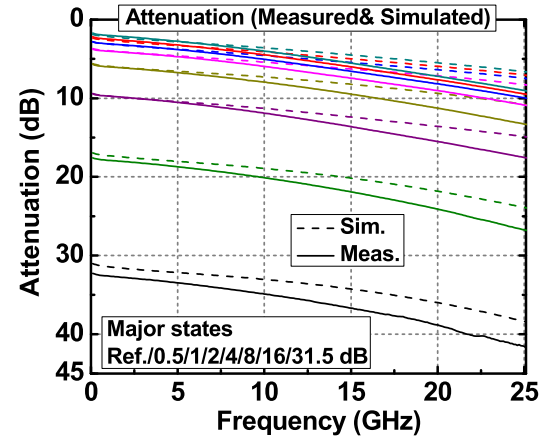
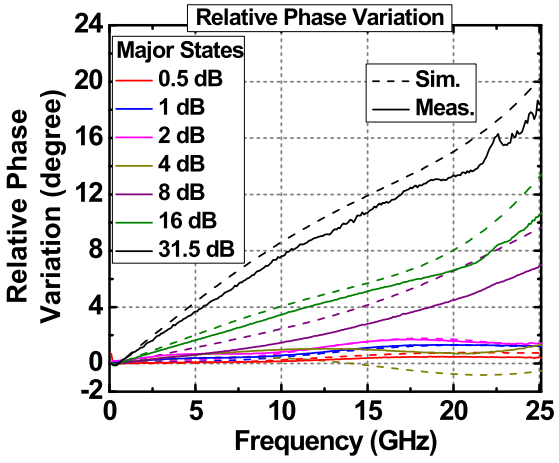


Fig. 12. Chip micrograph of the proposed 6-bit DSA. The total chip size is 0.98 mm^2 (1.3 mm x 0.75 mm).

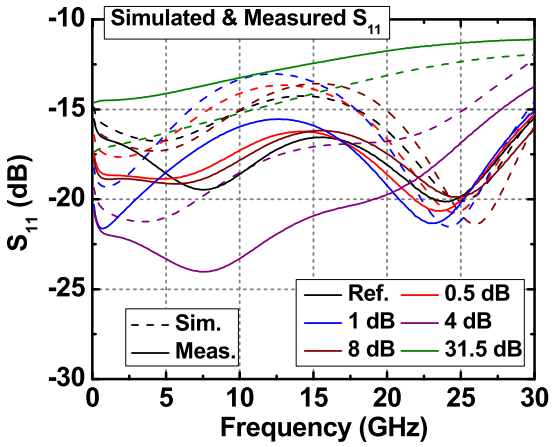


(a)

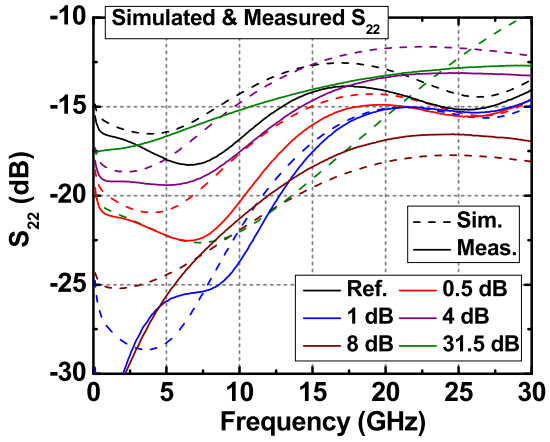


(b)

Fig. 13. Measured and simulated (a) attenuation response and (b) relative phase variations for major states.



(a)



(b)

Fig. 14. Simulated and measured (a) S_{11} and (b) S_{22} for major states.

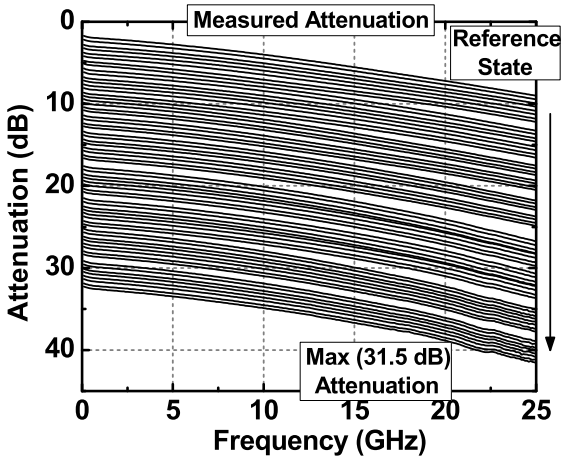
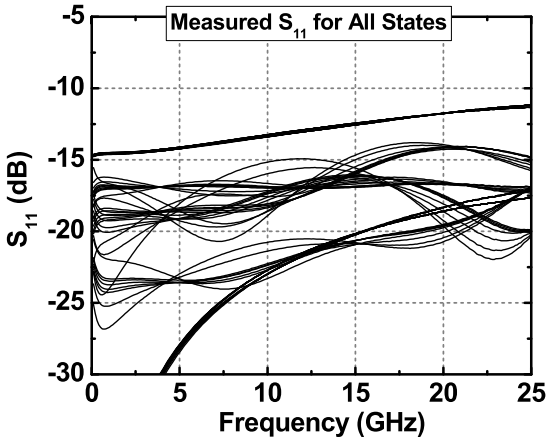


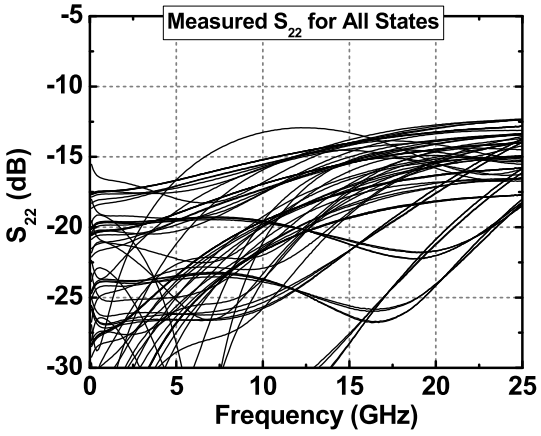
Fig. 15. Measured attenuation over frequency for all states.

the reduced cell provides almost negligible IL (<0.1 dB) below 30 GHz. In addition, since the dominant pole appears at much higher frequency (60 GHz) than the operational bandwidth (due to their smaller parasitic capacitance), it does not impose any bandwidth limitations when combined with the other modified T-type attenuator cells discussed in Section II-A.

In Fig. 9(b), the phase difference between a reference state and an attenuation state is shown for both the conventional and the reduced T-type attenuator cells. The reduced attenuation cell presents a low phase variation of 0.2° at 20 GHz, which is more than 60% reduction from the conventional design. On the other hand, when it comes to the matching response, the reduced cell cannot present an ideal 50-Ω-matched condition due to the omission of the series resistors R_1 from

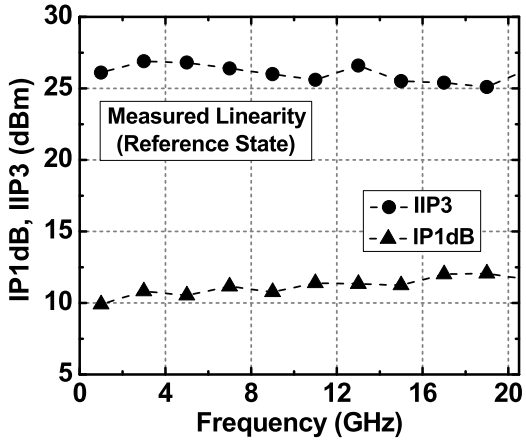


(a)

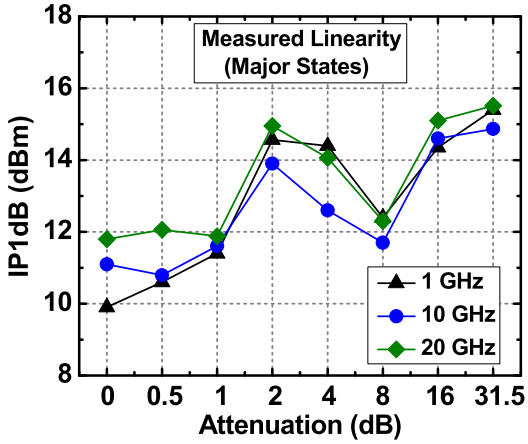


(b)

Fig. 16. Measured (a) S_{11} and (b) S_{22} versus frequency for all attenuation states.



(a)



(b)

Fig. 17. (a) Measured IP1dB compression point and IIP3 under the reference state. (b) Measured IP1dB for the major states.

the original T-type network. The simulated matching (S_{11} or S_{22}) results are shown in Fig. 9(b) for the reduced T-type 1-dB attenuator cell. The worst case is the attenuation state, but S_{11} remains lower than -18 dB below 100 GHz. From a practical point of view, since the reduced attenuator cells present reasonable matching response, they can replace the conventional designs in the case of low attenuation such as 0.5, 1.0, or 2.0 dB, effectively minimizing the loss associated with the series transistors.

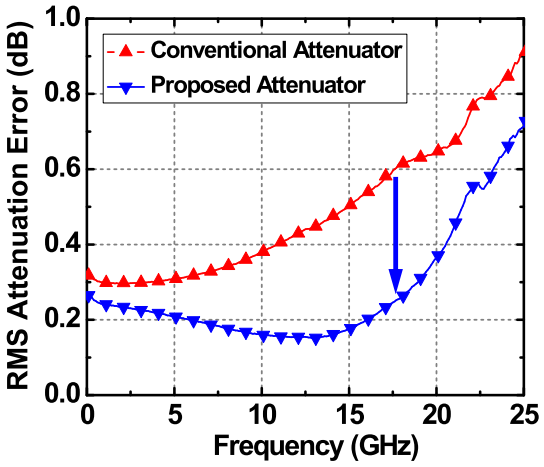
D. Full DSA Design

The full schematic of the proposed wideband low-loss DSA is shown in Fig. 10. It has six digital bit inputs, which provide an independent control of binary-coded attenuation levels (0.5, 1, 2, 4, 8, and 16 dB). The high-attenuation cells, including 4, 8, and 16 dB, use the modified switched T-type cells, while the low-attenuation cells (0.5, 1, and 2 dB) use the reduced T-type cells. The 16-dB cell consists of two identical 8-dB cells to minimize amplitude errors and phase variations. Similarly, the 2-dB cell is composed of two 1-dB cells for better impedance matching response. For system optimization, an additional 0.5-dB attenuator cell is included for performance tuning. Since the parasitic capacitance associated with the transistors and the interconnection structures presents a negative imaginary impedance, this shifts S_{11} and S_{22} down along the 50-Ω circle on the Smith chart. Inserting series inductors between stages improves the matching characteristics, thereby maximizing operational bandwidth.

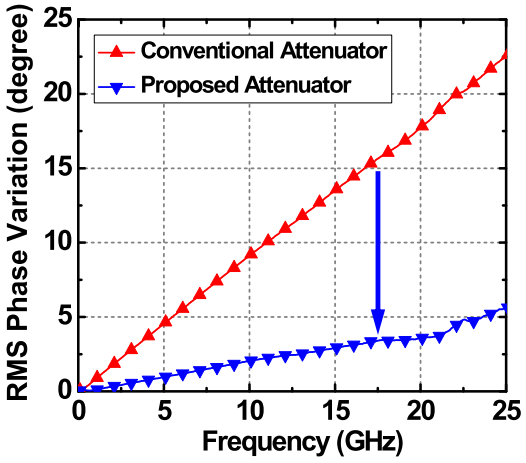
The series and the shunt transistors in the modified T-type attenuator cells have dimensions of 19 fingers of 5 μm $\times$ 120 nm and 8 fingers of 5 μm $\times$ 120 nm, respectively, whereas the shunt transistors in the reduced cells have a dimension of 1 finger of 4 μm $\times$ 120 nm. In addition, each series and shunt switch transistor employed a body/N-well-floating technique for minimizing signal leakage through substrate junctions [27]. Parasitic components such as interconnections, pads, and signal line structures were modeled with an electromagnetic (EM) simulation tool (SONNET) [28]. The proposed attenuator used coplanar waveguide (CPWG) lines with ground plane for interconnect signal lines. The series inductors have an inductance of about 300 pH, and the IL of an inductor is 0.5–0.7 dB at 20 GHz. Overall, the simulated IL of the DSA is about 5.5 dB at 20 GHz, considering five series inductors and four series attenuation cells.

E. Process and Temperature Effects

Process and temperature variations affect the performance of attenuators, as they change both the active and the passive

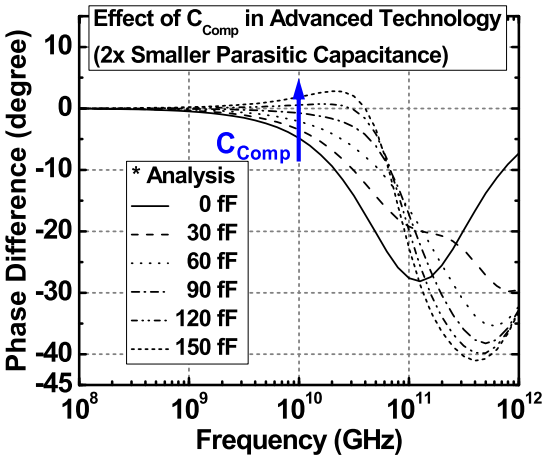


(a)

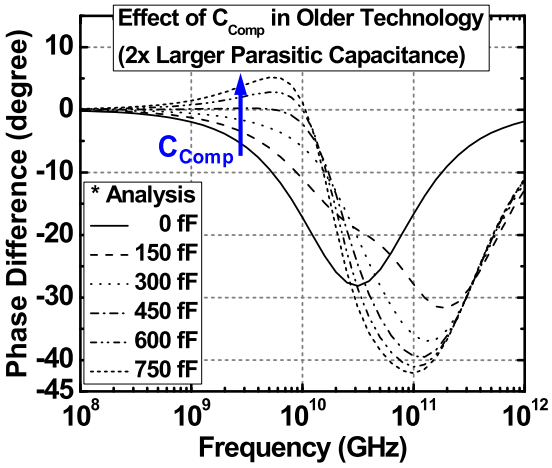


(b)

Fig. 18. (a) Measured rms attenuation error.(b) Measured rms phase variation for both the conventional and the proposed attenuators.



(a)



(b)

Fig. 19. Phase difference between a reference state and an attenuation state for (a) advanced technology platform which has 2× smaller parasitic capacitance and (b) older platform which has 2× larger parasitic capacitance. The values in Table I is used as a reference.

device parameters. In addition, since passive DSAs have no signal gain, they are likely to be more sensitive to parameter variations. The simulated S_{21} and S_{11} under different corners for the reference state are shown in Fig. 11(a) and (b), respectively. For low temperature and fast process corners, IL decreases due to reduced resistances, whereas IL increases for high temperatures and slow process corners. Capacitance also changes according to process and temperature corners, modifying the matching characteristics [Fig. 11(b)]. If the system requires constant performance (e.g., IL) across different corners, adaptive bias circuitry may be necessary to adjust gate control voltages, using internal or external process and temperature sensors.

III. Measured Results and Discussion

The proposed wideband DSA was fabricated in GlobalFoundries 130-nm 8HP SiGe BiCMOS technology platform, which provided triple-well RF nFETs with a unity-gain frequency (f_T) of about 90 GHz [29]. Since advanced SiGe BiCMOS platforms provide high-performance SiGe heterojunction bipoloar transistors (HBTs), they are suitable for the realization of full wideband T/R chipsets as shown in Fig. 1. Power supplies of 2.5 and 1.2 V were used for N-well biasing and digital control blocks, respectively. A chip micrograph is shown in Fig. 12. The core layout area without measurement pads and non-active space was 0.14 mm^2 (1.00 mm × 0.14 mm), while the total chip size was 0.98 mm^2 (1.30 mm × 0.75 mm). For the S-parameter characterization, a network analyzer (Agilent PNA E8364B) was used, whereas analog signal generators (Agilent PSG E8257D) and a signal analyzer (Agilent PXA N9030A) were used for linearity measurements.

In Fig. 13(a), the measured and simulated attenuation results for the major states (a reference state and 0.5/1/2/4/8/16/31.5-dB attenuation states) are shown. The measured attenuation exhibited higher loss due to an increase in parasitics associated with custom inductors and interconnect structures. Each inductor adds an additional 100–150 fF of shunt capacitance, and the interconnection presents about 5–7 Ω of series resistance from the circuit layout. The measured and the simulated relative phase variations are shown in Fig. 13(b). While the overall trend is similar, the measurement results have about 1° degradation for high attenuation states (8, 16, and 31.5 dB). The measured and simulated S_{11} and S_{22} are presented under major attenuation

TABLE III
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART DIGITAL-STEP ATTENUATORS

Reference	[24]	[30]	[31]	[19]	[16]	[20]	**This work**	
Process technology	GaAs FET	0.18 μm GaAs PHEMT	InGaAs pin diode	0.18 μm bulk CMOS	0.18 μm SOI CMOS	0.25 μm SiGe BiCMOS	**0.13 μm SiGe BiCMOS**	
Topology	Distributed T-type	N/A	Switched π-type w. pin diode	Switched T-/π-type w. inductive correction	Switched path w. DPDT	Switched T-/π-type w. iNMOS	**Conventional Switched T-type**	**Switched T-type w. capacitive compensation**
Bandwidth (GHz)	DC-20	1-15	7-40	DC-14	DC-20	6-12.5	**DC-20**	
Attenuation range (dB)	22.5 (4 bit) (LSB=1.5)	31.5 (6 bit) (LSB=0.5)	31 (5 bit) (LSB=1)	31.5 (6 bit) (LSB=0.5)	31 (5 bit) (LSB=1)	16.51 (7 bit) (LSB=0.26)	**31.5 (6 bit) (LSB=0.5 dB)**	
Insertion loss (dB)	3.1-4.8	3.0-6.2	7-11.5	3.7-10	3.1-7.6	12.7	**1.7-7.4**	**1.7-7.2**
Return loss (dB)	>13	>12	>8.0	>9	>12	13	**>12**	**>12**
RMS amplitude error (dB)	0.5	0.4	2.3	0.5	0.5	0.26	**0.65**	**0.37**
RMS phase variation (°)	N/A	7.5	N/A	4.2	2.5	3.5	**16**	**4.0**
IP1dB (dBm)	24	20	N/A	15	10	12.5	**10**	**10**
OIP3 (dBm)	N/A	N/A	N/A	29	N/A	N/A	**26**	**25**
Chip area (mm^2)	4.2 (2.6 x 1.6)	3.1 (2.6 x 1.2)	1.3 (1.6 x 0.8)	0.5 (1.25 x 0.4)*	0.63 (0.93 x 0.68)	0.29	**0.98 (1.30 x 0.75) 0.14 (1.00 x 0.14)***	

* Core circuit area without pads and non-active space

states in Fig. 14(a) and (b), respectively. Since 2- and 16-dB attenuation states consist of two identical 1- and 8-dB cells, for simplicity, they are not included.

The measured attenuation results over frequency for all states from 0 to 31.5 dB are shown in Fig. 15. While the overall gaps between attenuation states are relatively constant, a few overlaps are still observed between some states from 10 to 20 GHz. The measured impedance matching results for all states are presented in Fig 16. The input matching [S_{11} in Fig. 16(a)] and the output matching [S_{22} in Fig. 16(b)] were better than -12 and -13 dB for the entire bandwidth, respectively. The measured linearity of the proposed DSA is shown in Fig. 17(a). The input 1-dB-compression point (IP1dB) under a reference state is about 10–12 dBm across the operational bandwidth. The measured input third-order-intercept point (IIP3) under a reference state is about 25–27 dBm from 1 to 20 GHz. In Fig. 17(b), the measured IP1dB for the major states are presented. While IP1dB under the maximum attenuation (31.5 dB) state is about 15 dBm, the IP1dB response shows some fluctuations depending on the DSA state chosen.

The performance of the proposed wideband DSA is summarized in Table III and compared with the literature. The DSA exhibits the lowest IL among the state-of-the-art attenuators in silicon-based platforms, and the overall IL result is comparable to the best attenuators implemented in III–V technologies. In addition, the proposed DSA provides low root-mean-square (rms) amplitude/phase errors and good impedance matching for wideband operation. Regarding the attenuation roll-off in the proposed DSA, attenuators based on compound semiconductor technologies or silicon-on-insulator CMOS typically exhibit gradual roll-off due to their low parasitics. However, attenuators in bulk silicon technology suffer from steeper roll-off due to its inherently lossy substrate, which degrades the high-frequency performance of the active devices and the passive components. In order to minimize this roll-off, smaller devices can be used for obtaining smaller parasitics at the cost of higher IL. At the system level, additional loss compensation amplifiers with an equalization function can be used for achieving flat in-band performance. Compared with other published designs, the proposed DSA also occupies the smallest core chip area, since it employs a small number of on-chip inductors and avoids the use of transmission lines as matching elements. While the linearity of the proposed DSA is somewhat limited, several high power-handling switch techniques, including stacked transistors, feed-forward capacitors, and negative bulk bias, can be applied for future design optimization, as required [32]. Table III also includes the performance of the uncompensated DSA as a reference circuit. It employs conventional switched T-type cells and the loss-minimized reduced T-type attenuator cells. While the matching and linearity results of both the reference and the proposed attenuators are similar, the amplitude and the phase variations are significantly improved in the proposed DSA. The measured rms amplitude errors and phase variations over frequency are shown in Fig. 18. The proposed attenuator exhibits a reduction of 45% and 75% in the amplitude and the phase variations at 20 GHz, respectively.

It should be noted that the amplitude/phase compensation technique is applicable to other technology platforms in general. As a conceptual verification, the phase difference of an 8-dB attenuator cell is simulated for increased and reduced capacitance with respect to Table I, in order to reflect the use of both more advanced and older technology platforms, respectively. When the capacitance of transistors is reduced by 50% [Fig. 19(a)], C_{Comp} of about 120 fF shows the flat response up to 30 GHz. On the other hand, when the capacitance is doubled [Fig. 19(b)], C_{Comp} of about 450 fF is the optimal for the maximum bandwidth of 6 GHz. In both extreme cases, the usable bandwidth is extended by more than a decade. Hence, the amplitude/phase-compensation technique investigated in this paper can be used in practical DSA designs as a simple, yet effective performance optimization method.

IV. Conclusion

In this paper, the design and the analysis of a wideband low-loss DSA with minimized amplitude/phase variations are presented. The DSA based on the combination of amplitude/phase-compensated switched T-type cells and loss-minimized T-type attenuator cells was implemented in a 130-nm SiGe BiCMOS technology platform. The fabricated DSA achieves low IL, minimized variations, matching characteristics, moderate linearity, and compact size.

Acknowledgment

The authors would like to thank Georgia Tech Research Institute (GTRI) and the silicon-germanium (SiGe) team of GlobalFoundries for their invaluable support, especially D. Harame, N. Cahoon, and A. Joseph.

References

[1] H. Dogan and R. G. Meyer, "Intermodulation distortion in CMOS attenuators and switches," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 529–539, Mar. 2007.

[2] J. Nehring *et al.*, "Highly integrated 4–32-GHz two-port vector network analyzers for instrumentation and biomedical applications," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 1, pp. 229–244, Jan. 2017.

[3] S. Sim, L. Jeon, and J.-G. Kim, "A compact X-band bi-directional phased-array T/R chipset in 0.13 μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 562–569, Jan. 2013.

[4] H. Liu *et al.*, "A wideband analog-controlled variable-gain amplifier with dB-linear characteristic for high-frequency applications," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 533–540, Feb. 2016.

[5] Y. Wang, B. Afshar, L. Ye, V. C. Gaudet, and A. M. Niknejad, "Design of a low power, inductorless wideband variable-gain amplifier for high-speed receiver systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 696–707, Apr. 2012.

[6] Y.-Y. Huang, W. Woo, H. Jeon, C.-H. Lee, and J. S. Kenney, "Compact wideband linear CMOS variable gain amplifier for analog-predistortion power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 68–76, Jan. 2012.

[7] U. Mayer, F. Ellinger, and R. Eickhoff, "Analysis and reduction of phase variations of variable gain amplifiers verified by CMOS implementation at C-band," *IET Circuits, Devices Syst.*, vol. 4, no. 5, pp. 433–439, Sep. 2010.

[8] J.-W. Lai, Y.-J. Chuang, K. Cimino, and M. Feng, "Design of variable gain amplifier with gain-bandwidth product up to 354 GHz implemented in InP-InGaAs DHBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 2, pp. 599–607, Feb. 2006.

[9] B. Sewiolo, G. Fischer, and R. Weigel, "A 30 GHz variable gain amplifier with high output voltage swing for ultra-wideband radar," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 9, pp. 590–592, Sep. 2009.

[10] J. Bae, J. Lee, and C. Nguyen, "A 10–67-GHz CMOS dual-function switching attenuator with improved flatness and large attenuation range," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4118–4129, Dec. 2013.

[11] W. Cheng, M. S. O. Alink, A. J. Annema, G. J. M. Wienk, and B. Nauta, "A wideband IM3 cancellation technique for CMOS II- and T-attenuators," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 358–368, Feb. 2013.

[12] J. Bae and C. Nguyen, "A novel concurrent 22–29/57–64-GHz dual-band CMOS step attenuator with low phase variations," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 6, pp. 1867–1875, Jun. 2016.

[13] K. Kim and B.-W. Min, "V-W band CMOS distributed step attenuator with low phase imbalance," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 8, pp. 548–550, Aug. 2014.

[14] B.-W. Min and G. M. Rebeiz, "A 10–50-GHz CMOS distributed step attenuator with low loss and low phase imbalance," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2547–2554, Nov. 2007.

[15] L. Sjogren, D. Ingram, M. Biedenbender, R. Lai, B. Allen, and K. Hubbard, "A low phase-error 44-GHz HEMT attenuator," *IEEE Microw. Guided Wave Lett.*, vol. 8, no. 5, pp. 194–195, May 1998.

[16] M.-K. Cho, J.-G. Kim, and D. Baek, "A broadband digital step attenuator with low phase error and low insertion loss in 0.18-μm SOI CMOS technology," *Electron. Telecommun. Res. Inst. J.*, vol. 35, no. 4, pp. 638–643, Aug. 2013.

[17] H. Dogan, R. G. Meyer, and A. M. Niknejad, "Analysis and design of RF CMOS attenuators," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2269–2283, Oct. 2008.

[18] Y.-Y. Huang, W. Woo, Y. Yoon, and C.-H. Lee, "Highly linear RF CMOS variable attenuators with adaptive body biasing," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1023–1033, May 2011.

[19] B.-H. Ku and S. Hong, "6-bit CMOS digital attenuators with low phase variations for *X*-band phased-array systems," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 7, pp. 1651–1663, Jul. 2010.

[20] M. Davulcu, C. Caliskan, I. Kalyoncu, M. Kaynak, and Y. Gurbuz, "7-bit SiGe-BiCMOS step attenuator for X-band phased-array radar applications," *IEEE Microw. Compon. Lett.*, vol. 26, no. 8, pp. 598–600, Aug. 2016.

[21] W. Ciccognani, F. Giannini, E. Limiti, and P. E. Longhi, "Compensating for parasitic phase shift in microwave digitally controlled attenuators," *Electron. Lett.*, vol. 44, no. 12, pp. 743–744, Jun. 2008.

[22] P. Sun, "Analysis of phase variation of CMOS digital attenuator," *Electron. Lett.*, vol. 50, no. 25, pp. 1912–1914, 2014.

[23] M.-K. Cho, J.-H. Han, J.-H. Kim, and J.-G. Kim, "An X/Ku-band bi-directional true time delay T/R chipset in 0.13 μm CMOS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–3.

[24] B. Khabbaz, A. Pospishil, and H. P. Singh, "DC-to-20-GHz MMIC multibit digital attenuators with on-chip TTL control," *IEEE J. Solid-State Circuits*, vol. 27, no. 10, pp. 1457–1462, Oct. 1992.

[25] M.-K. Cho, I. Song, and J. D. Cressler, "A true time delay-based SiGe bi-directional T/R chipset for large-scale wideband timed array antennas," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2018.

[26] M. E. V. Valkenburg and W. M. Middleton, *Reference Data for Engineers: Radio, Electronics, Computers and Communications*, 9th ed. Woburn, MA, USA: Newnes, 2001.

[27] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 31–39, Jan. 2006.

[28] Sonnet Software Inc. *Sonnet Suites*. Accessed: Jan. 9, 2017. [Online]. Available: http://www.sonnetsoftware.com/products/sonnet-suites

[29] B. A. Orner *et al.*, "A 0.13 μm BiCMOS technology featuring a 200/280 GHz (f_T/f_{max}) SiGe HBT," in *Proc. Bipolar/BiCMOS Circuits Technol. Meeting*, Sep. 2003, pp. 203–206.

[30] OMMIC, Limeil-Brvannes, France. *6-bit 1-15 GHz Attenuator Datasheet CGY2171XBUH*. Accessed: Jan. 8, 2017. [Online]. Available: http://www.ommic.fr/produits/w2171b-39

[31] J. G. Yang and K. Yang, "Broadband compact InGaAs pin 5-bit digital attenuator using π-type resistive network," *Electron. Lett.*, vol. 48, no. 12, pp. 702–704, Jun. 2012.

[32] J. Rascher, A. Zohny, S. Glock, G. Fischer, R. Weigel, and T. Ussmueller, "A comparative overview of high power handling CMOS switches and their recent applications in RF front ends," in *Proc. IEEE Wireless Microw. Technol. Conf. (WAMICON)*, Apr. 2013, pp. 1–5.

Ickhyun Song (M'17) received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2006 and 2008, respectively, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2016.

From 2008 to 2012, he was a Design Engineer with Samsung Electronics Company, Hwasung, South Korea, where he has contributed to the development of analog circuits for next-generation memory products. Since 2017, he has been with the School of Electrical and Computer Engineering, Georgia Institute of Technology, where he is currently a Research Engineer. His current research interests include radio frequency and analog circuits and systems, radiation-hardened space electronics design, and CMOS/SiGe heterojunction bipoloar transistors (HBT) device physics.

Dr. Song was a recipient of the 2007–2008 Samsung Semiconductor Scholarship, the Silver Paper Award at the 2007 IEEE Seoul Section Student Paper Contest, the Gold Prize at the 2008 Samsung HumanTech Paper Award, the 2012–2013 Fulbright Graduate Study Award, and the 2016 Georgia Electronic Design Center (GEDC) Best Poster Award.

Moon-Kyu Cho (M'13) received the B.S., M.S., and Ph.D. degrees in electronic engineering from Kwangwoon University, Seoul, South Korea, in 2009, 2011, and 2014, respectively.

In 2014, he joined the Georgia Electronic Design Center (GEDC), Institute for Electronics and Nanotechnology (IEN), Georgia Institute of Technology, Atlanta, GA, USA, as a Research Engineer. His current research interests include wideband/narrowband phased-array antenna systems, integrated radio and radar systems in silicon technologies for wireless communications, wireless sensing and detection, and imaging applications at RF, microwave, millimeter-wave, and sub-millimeter-wave regimes.

Dr. Cho was a recipient of the 2011 and 2012 Best Paper Award of the IEEE Electron Device Society, Seoul Chapter, the 2013 Best Paper Award of the IEEE Solid-State Circuits Society, Seoul Chapter, and the2012 and 2013 Best Poster Award and Best Demo Award of the International SoC Design Conference. He was the co-recipient of the 2016 Georgia Electronic Design Center (GEDC) Best Poster Award.

John D. Cressler (F'01) received the B.S. degree from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 1984, and the Ph.D. degree from Columbia University, New York, NY, USA, in 1990.

From 1984 to 1992, he was a Research Staff with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA. From 1992 to 2002, he served on the Faculty at Auburn University, Auburn, AL, USA. In 2002, he joined the Faculty at Georgia Tech, where he is currently the Schlumberger Chair Professor in electronics with the School of Electrical and Computer Engineering. The basic thrust of Cressler's research is to develop novel micro/nanoelectronic devices, circuits and systems for next-generation applications within the global electronics infrastructure. He and his team attempt to break the business-as-usual mold in this field and re-imagine the way electronics in the 21st century can and should be practiced. His current research interests include Si-based (SiGe/strained-Si) heterostructure devices and technology, mixed-signal (analog, digital, RF-sub-millimeter-wave) circuits built from these devices, radiation effects, cryogenic electronics, device-to-circuit interactions, noise and reliability physics, device-level simulation, and compact circuit modeling. He and his students authored or co-authored over 700 scientific papers in this field and he has graduated 49 Ph.D. students during his academic career.

Dr. Cressler was elected as a Fellow of the IEEE in 2001 for his research contributions. He was a recipient of the 2010 Class of 1940 W. Howard Ector Outstanding Teacher Award (Georgia Tech's top teaching award), the 2011 IEEE Leon Kirchmayer Graduate Teaching Award (the IEEE's Top Graduate Teaching Award), and the Class of 1934 Distinguished Professor Award (the highest honor Georgia Tech bestows on its faculty). His books include: *Silicon-Germanium Heterojunction Bipolar Transistors*, *Silicon Heterostructure Handbook*, *Silicon Earth: Introduction to the Microelectronics and Nanotechnology Revolution*, and *Extreme Environment Electronics*.