Chapter 10
Stability and Frequency Compensation

中科大微电子学院

黄 鲁

教材:模拟CMOS集成电路设计

Behzad Razavi

10.1 General considerations

Negative feedback finds wide application in the processing of analog signals.

suppressing variations of the open-loop characteristics.

Feedback systems suffer from potential instability, they may oscillate.

the closed-loop transfer function

$$\frac{Y}{X}(s) = \frac{H(s)}{1+\beta H(s)}$$

may oscillate at frequency ω_1

$$|\beta H(j\omega_1)| = 1$$

$$\angle\beta H(j\omega_1) = -180^\circ$$

设某个频率时，负反馈能变成正反馈！

"Barkhausen's Criteria." 巴克豪森判据

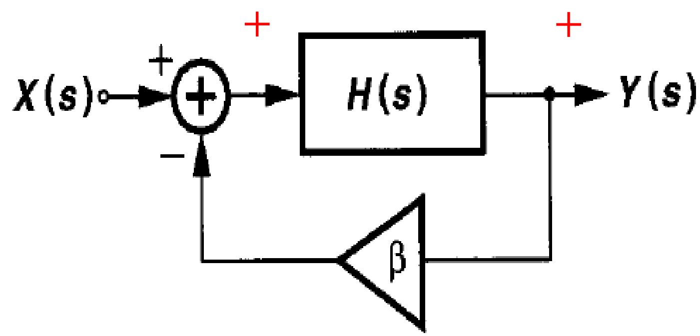


Figure 10.1 Basic negative-feedback system.

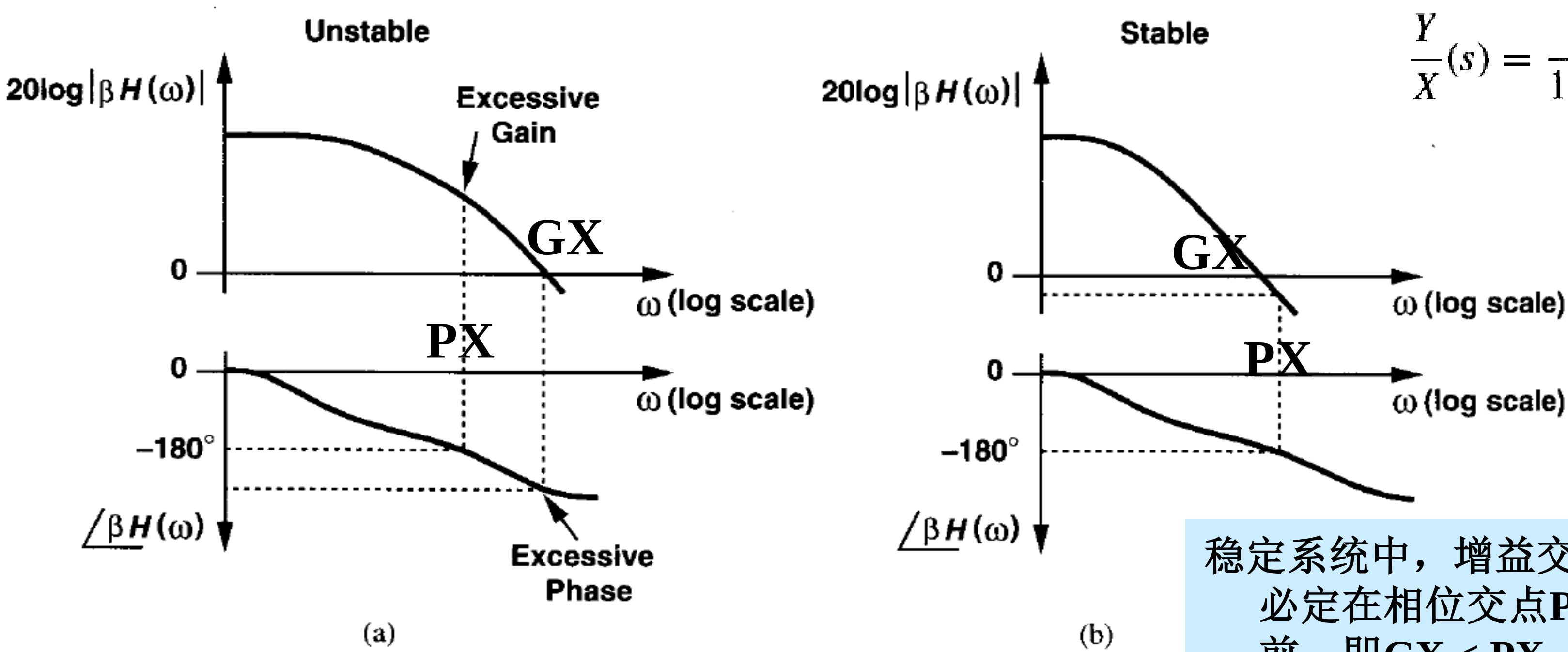
设反馈网络与频率无关,且 $\beta \le 1$

$$Y(S) = H(S)(X(S) - \beta Y(S))$$

当正反馈(某个频率）环路增益>=1时发生自激振荡

Stability criteria(判据)

$$\frac{Y}{X}(s) = \frac{H(s)}{1+\beta H(s)}$$



稳定系统中，增益交点GX必定在相位交点PX之前，即GX < PX。

Figure 10.2 Bode plots of loop gain for unstable and stable systems.

gain crossover point (增益交点GX)：环路增益=1的频率，比单位增益带宽小

phase crossover point (相位交点PX)：环路相位= -180的频率

if β is reduced (less feedback), then the magnitude plots are shifted down, thereby moving the gain crossover closer to the origin and making the feedback system more stable.

worst-case stability corresponds to $\beta = 1$, i.e, unity-gain feedback. For this reason, we often analyze the magnitude and phase plots for $\beta H = H$.

10.2 Multi-Pole Systems

- 大多数实用运放是多极点的。一般而言，信号通路上的每个MOS管至少会产生一个极点。
- 若反馈减弱即 β（设与频率无关)减小，则环路幅频曲线下移，相位曲线不变；因此，增益交点GX向原点移动，$\angle\beta H(j\omega_{GX})$相移减小，系统更稳定。
- 结论：弱反馈有利于系统稳定。

稳定系统中，增益交点GX频率必定在相位交点PX频率之前，即GX < PX。

每个极点导致在很高频率时相位滞后90°；
每个极点频率处，幅频下降3dB，波特图上以-20dB/10倍频程下降；
每个零点频率处，幅频上升3dB，波特图上以20dB/10倍频程上升。

(if $0.1\omega_{p2} > 10\omega_{p1}$)

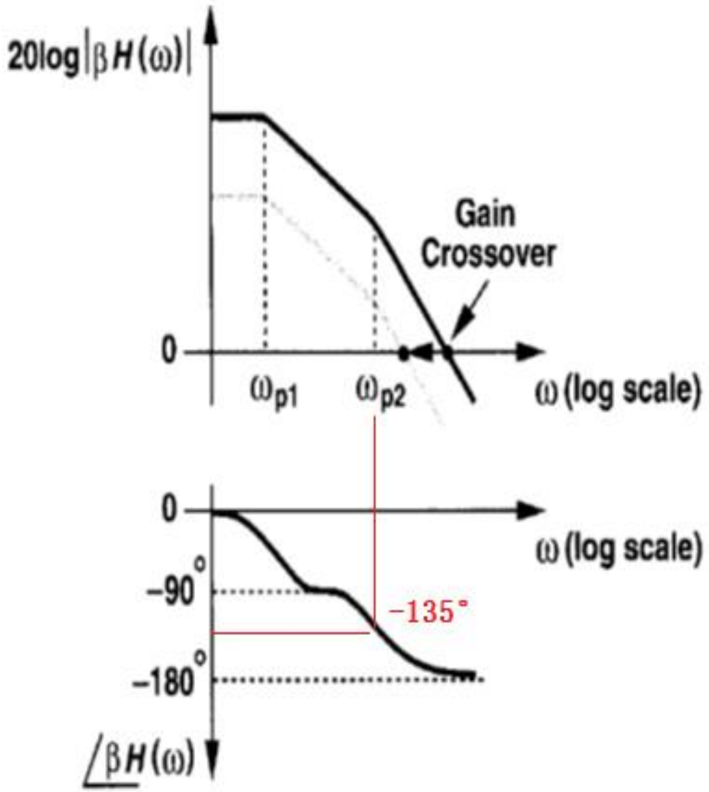


Figure 10.6 Bode plots of loop gain for a two-pole system.

二阶系统负反馈是稳定的

高阶系统

三阶以上系统，必然存在某个频率点：ω_1

$$\angle \beta H(j\omega_1) = -180^0$$

若此频率点的环路增益幅值>1，则

反馈电路产生振荡！

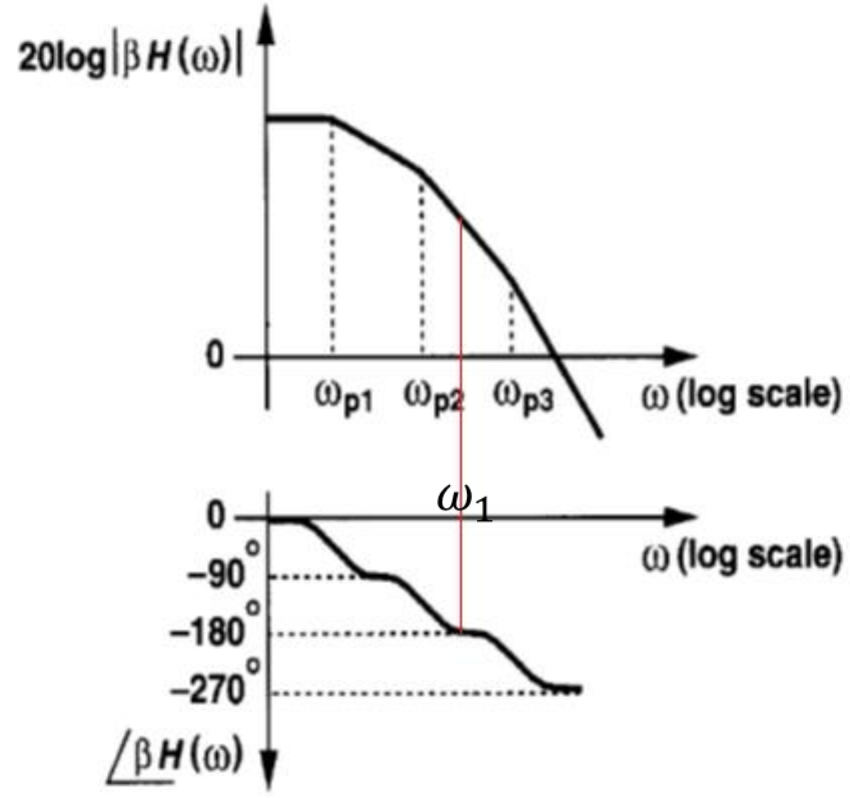


Figure 10.8 Bode plots of loop gain for a three-pole system.

10.3 Phase Margin相位裕度（量）

- GX与PX的关系:

稳定系统的环路增益 $|\beta H(j\omega)|$必须在 $\angle \beta H(j\omega)$ 达到 -180^0之前下降到 1 （0dB)。
即GX<PX。GX应离PX多远？

- 在增益交点GX处 $\beta H(j\omega_{GX}) = 1 \times \exp^{j\angle\beta H(j\omega_{GX})}$

- 本例(a)处于边缘稳定，$\angle \beta H(j\omega_{GX}) = -175^\circ$

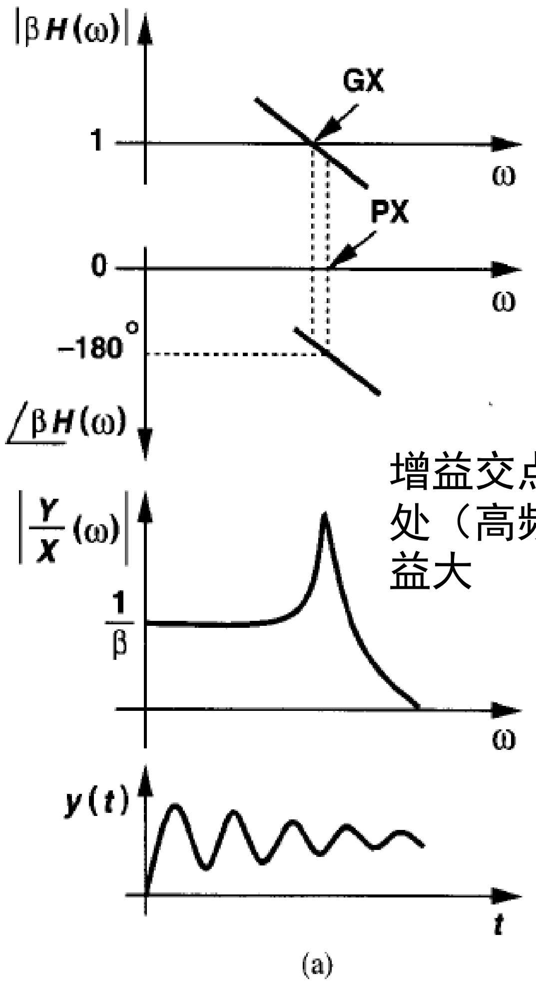
记ω_{GX}为ω_1

$$\frac{Y}{X}(j\omega_1) = \frac{H(j\omega_1)}{1+\beta H(j\omega_1)}$$

$$= \frac{\frac{1}{\beta}\exp(-j175^\circ)}{1+\exp(-j175^\circ)}$$

$$= \frac{1}{\beta}\cdot\frac{-0.9962 - j0.0872}{0.0038 - j0.0872}$$

$$\left|\frac{Y}{X}(j\omega_1)\right| = \frac{1}{\beta}\cdot\frac{1}{0.0872} \approx \frac{11.5}{\beta}$$



增益交点频率处（高频）增益大

Figure 10.9

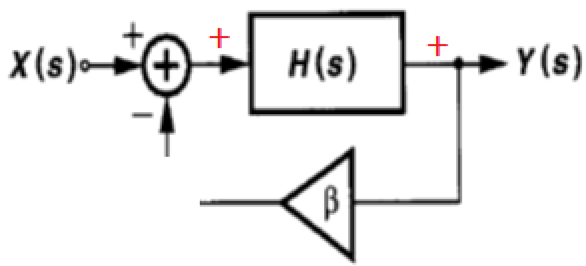
second-order system may suffer from ringing although it is stable

- 注意：增益交点GX是环路概念，
不是闭环增益。

PM相位裕度 (量)

- GX距离PX较远（GX<PX）,则闭环系统稳定性好。
- 相位裕度PM：

$$PM = 180^0 + \angle \beta H(\omega_{GX})$$



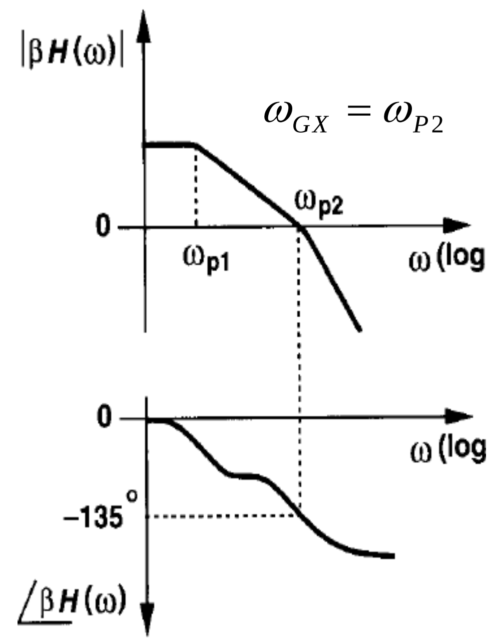


Figure 10.10

- Example 10.3

一个两极点系统被设计成 $|\beta H(j\omega_{P2})| = 1$

且 $\omega_{P1} << \omega_{P2}$ ，PM= ?

$$\because \quad \angle \beta H(j\omega_{P2}) = -135^\circ$$

$$\therefore \quad PM = 45^0$$

How much phase margin is adequate?

For $PM = 45°$.

$$\angle \beta H(j\omega_{GX}) = -135^o$$
$$|\beta H(j\omega_{GX})| = 1$$

$$\left|\frac{Y}{X}(j\omega_{GX})\right| = \left|\frac{H(j\omega_{GX})}{1+\beta H(j\omega_{GX})}\right|$$

$$= \left|\frac{\frac{1}{\beta}\exp^{-j135^o}}{1+\exp^{-j135^o}}\right| \approx \frac{1.3}{\beta} > \frac{1}{\beta}$$

当$PM = 60^0$

$$\left|\frac{Y}{X}(j\omega_{GX})\right| = \left|\frac{H(j\omega_{GX})}{1+\beta H(j\omega_{GX})}\right| = \left|\frac{\frac{1}{\beta}\exp^{-j120^o}}{1+\exp^{-j120^o}}\right|$$

$$= \frac{1}{\beta\left|1+(-\frac{1}{2}-j\frac{\sqrt{3}}{2})\right|} = \frac{1}{\beta}$$

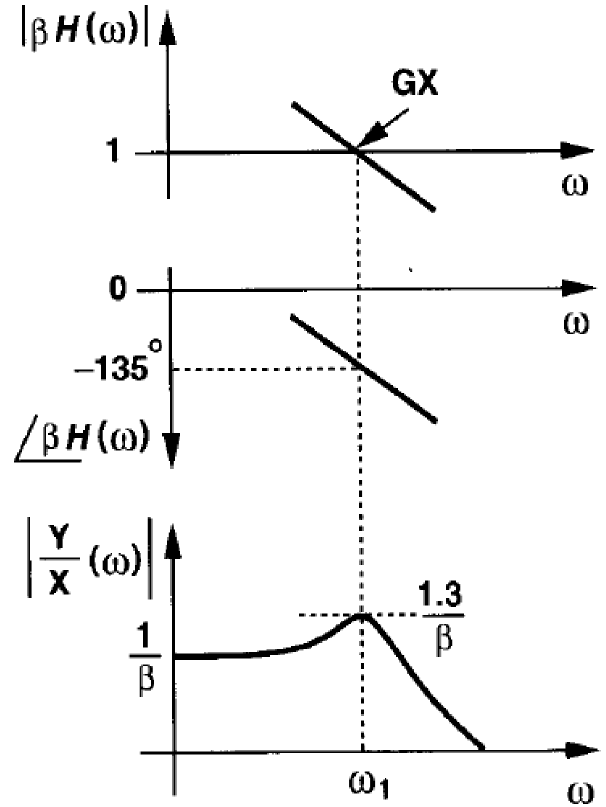


Figure 10.11 Closed-loop frequency response for 45° phase margin.

How much phase margin is adequate? (cont.)

- 对于更大的PM(GX离PX更远，更小)，系统更加稳定，但时间响应减慢（例如减小开环主极点）。

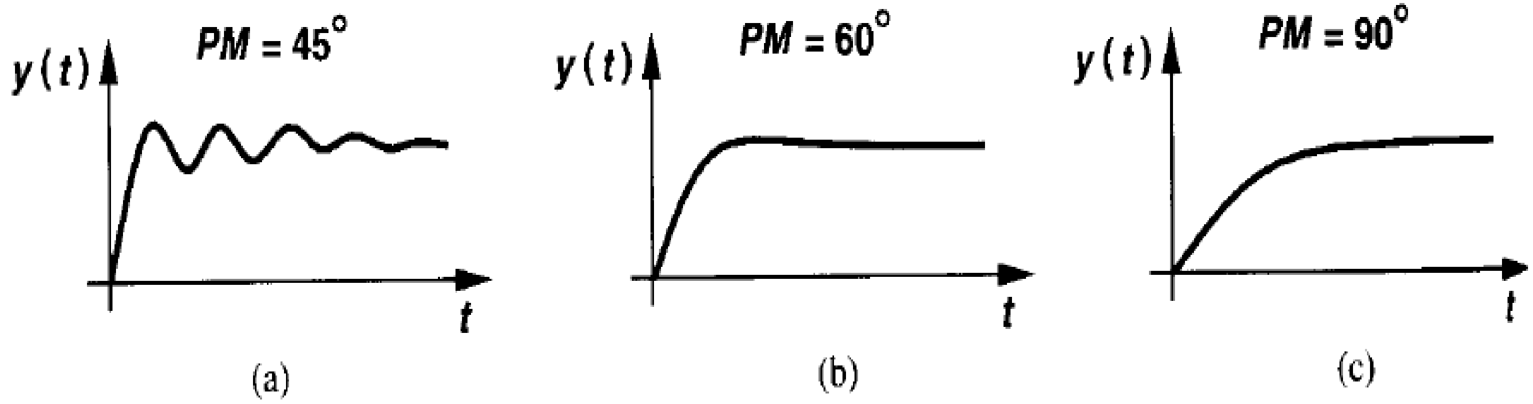
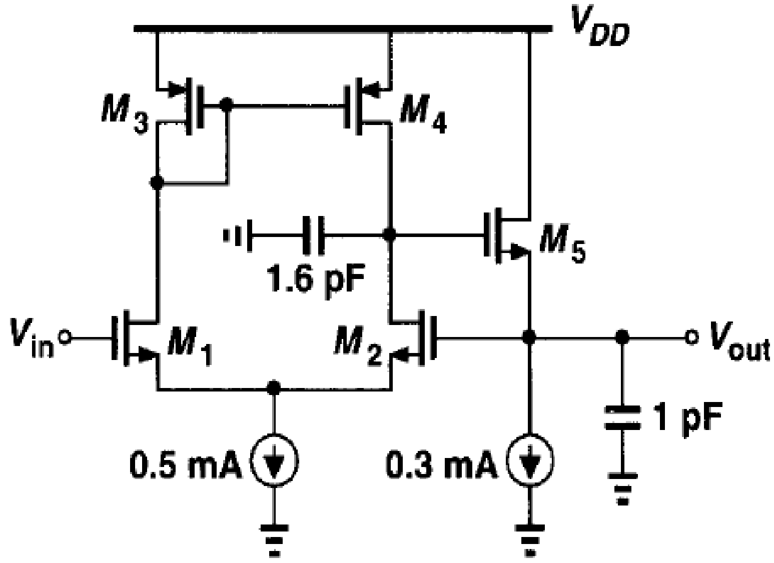
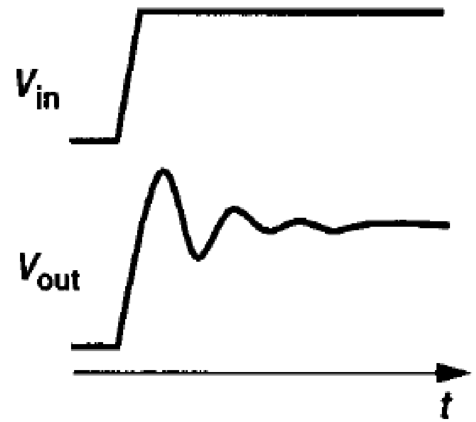


Figure 10.12 Closed-loop time response for 45°, 60°, and 90° phase margins

- 一般取 $PM = 60^0$
  - 注意：相位裕量的概念（环路频域计算）适合处理小幅度信号电路的设计。
  - 大信号阶跃响应与图10.12不符合。原因是：偏置电压和偏置电流的较大偏离所导致的非线性，以及在瞬态过程引起极点频率和零点频率变化（RC与工作点有关），导致复杂的 时间响应。
  - 对于大信号应用，采用闭环系统的时域仿真计算更合适，即瞬态仿真；
  - 手工计算时用转换速率或压摆率估算上升时间。

Example:单位增益缓冲器





大信号

Figure 10.13 Unity-gain buffer.

- 设所有晶体管: $\frac{W}{L} = \frac{50\mu m}{0.6\mu m}$
- SPICE模拟得到： 相位裕度为 65^0
- 单位增益频率（GX点）为150MHz。
- Vout波动说明虽然单位增益放大器相位裕量很好,但大信号稳定性不好.

系统稳定的方法

- 常用运放都是多极点系统，当有3个以上极点时，若有反馈应用，须检查是否需要进行相位补偿，即修正开环传输函数（相当于反馈系数=1时的环路增益），确保闭环电路稳定。
- 使运放系统稳定的方法：

（1）减小环路增益总相移，使相位交点PX向外推，如图10.14（a），但电路设计上比较难实现（例如减小次极点节点的寄生电容）。

（2）降低增益，使增益交点GX向内推，如图10.14（b）。

稳定：GX<PX

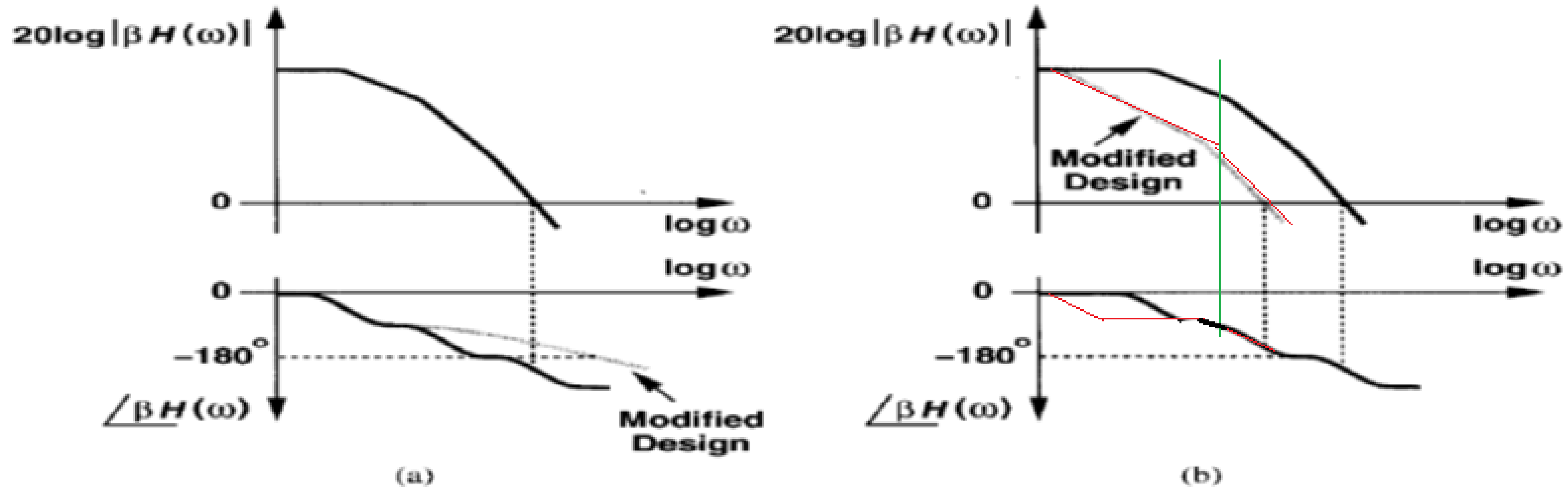


Figure 10.14 Frequency compensation by (a) moving PX out, (b) pushing GX in.

系统稳定的方法（cont.）

- 减小相移的设计方法：
  选择使极点数减至最少的电路结构。由于每级放大至少增加一个极点，因此开环H级数应减至最少。前提是H能达到适当的电压增益带宽积和输出摆幅。
- 使增益交点内移的设计方法：
  在保证开环H增益带宽积>>反馈（闭环）运算放大器带宽前提下，降低开环H带宽，即将增益交点向原点内推，具体方法称为频率（或相位）补偿。

- 例：

path 1 contains a high-frequency pole at the source of M_3, a mirror pole at node A, another high-frequency pole at the source of M_7,

path 2 contains a high-frequency pole at the source of M_4.

The two paths share a pole at the output.

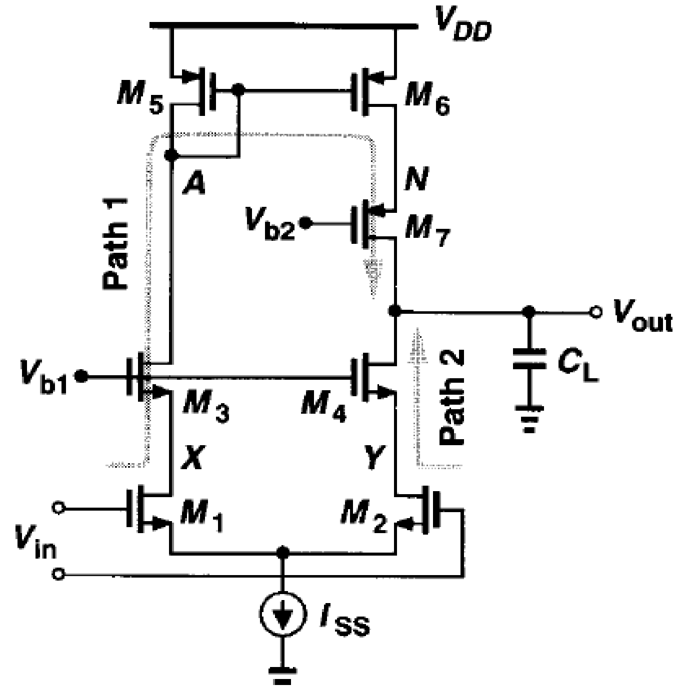


Figure 10.15 Telescopic op amp with single-ended output.

- 极点估算：

因cascode结构输出电阻很大，比其它节点小信号电阻高很多，因此输出极点 $\omega_{p,out}$ 值最小(靠近原点)，称为主极点，“dominant pole,”通常确定开环3DB带宽。

极点估算(续)：

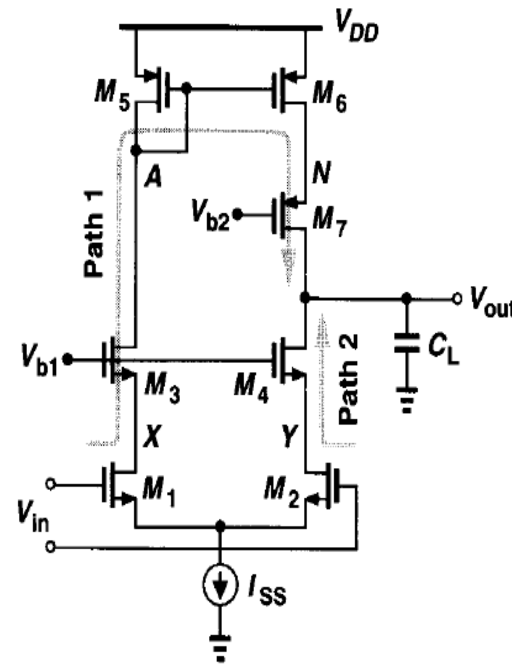
We also surmise 推测 that the first "nondominant pole," arises at node A. the total capacitance is relatively large.

Which node yields the next nondominant pole: N or X (and Y)?

since $g_m = 2I_D/|V_{GS} - V_{TH}|$,

transistors are designed to have the same overdrive,

nodes N and X (or Y) see roughly equal small-signal resistances to ground but node N suffers from much more capacitance.



- 节点X和Y的二个极点相等，通路1和通路2传输函数相加，因此它们是一个极点。
- 镜像极点A影响相位裕量(次极点频率上总移相-135°，假设主极点频率<<次极点频率)。

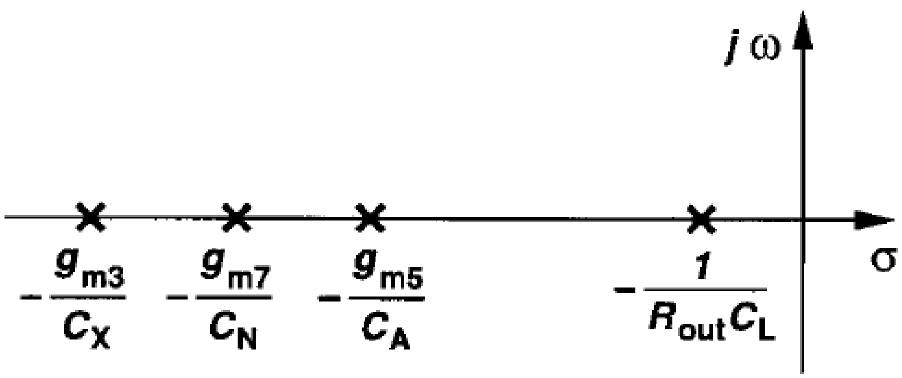


Figure 10.16 Pole locations for the op amp of Fig. 10.15.

How do compensating?

assume that the number and location of the nondominant poles and hence the phase plot at frequencies higher than roughly $10\omega_{p,out}$ remain constant.

Thus, we must force the loop gain to drop such that the gain crossover point moves toward the origin.

To accomplish this, we simply lower the frequency of the dominant pole by increasing the load capacitance.

translating the dominant pole toward the origin affects the magnitude plot but not the critical part of the phase plot.

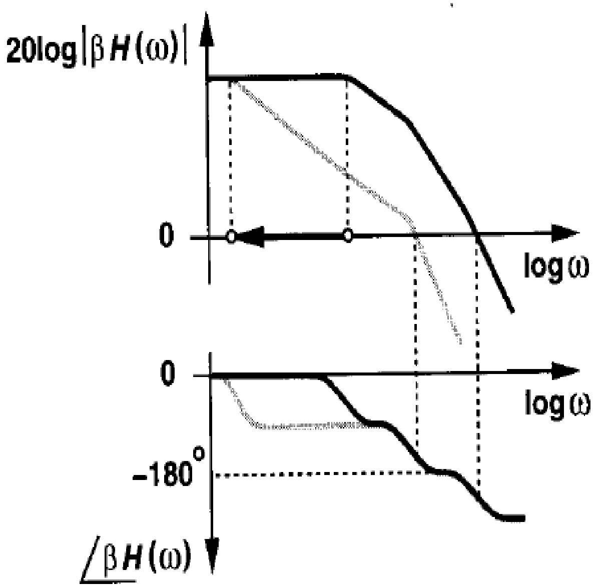


Figure 10.18 Translating the dominant pole toward origin.

设主次极点距离很远 $\omega_{p2} > 10\omega_{p1}$，无零点时，次极点的总移相为-135°，若次极点（频率）处的环路增益幅度>0dB, 则表明相位裕量<45°，**在最大负反馈应用** $\beta = 1$ **情况下**，要求在补偿后，开环H放大器（最大负反馈时的环路增益）的**单位增益带宽**小于H的次极点频率 ω_{p2} 即PM>45°

Increasing Rout does not compensate

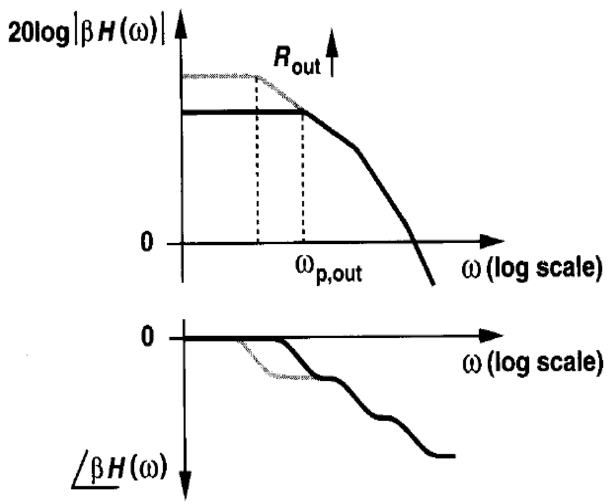


Figure 10.20

although $\omega_{p,out} = (R_{out}C_L)^{-1}$

a higher R_{out} does not improve the phase margin.

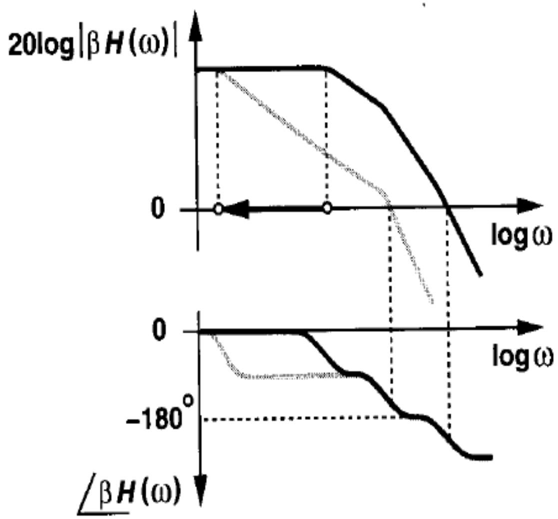
只能增加主极点关联节点的电容，会增加功耗！

频率补偿后，次极点与增益交点（环路增益=1）频率的合理关系：
设相位裕量=60°，主极点和次极点足够远。

设可近似为2极点系统：$\beta H(s) = \beta \dfrac{A_o}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}$

在增益交点ω_{GX}上：$\angle\beta H(\omega_{GX}) = -\angle(1+j\frac{\omega_{GX}}{\omega_{p1}}) - \angle(1+j\frac{\omega_{GX}}{\omega_{p2}})$

$\approx -(90° + 30°) = -120°$（相位裕量60°）



$\arctan(1 + j\frac{\omega_{GX}}{\omega_{p2}}) = 30°$，得到 $\frac{\omega_{GX}}{\omega_{p2}} = \frac{\sqrt{3}}{3}$，即 $\omega_{p2} = \sqrt{3}\omega_{GX} \approx 2\omega_{GX}$

低频环路增益*主极点频率=？

增益交点（单位增益）频率=（0.5~0.6）*第1次极点频率ω_{p2}

Fully differential telescopic cascode

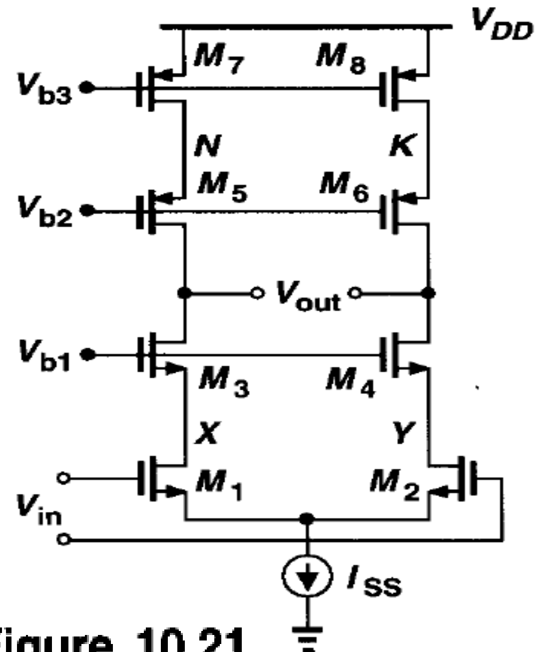


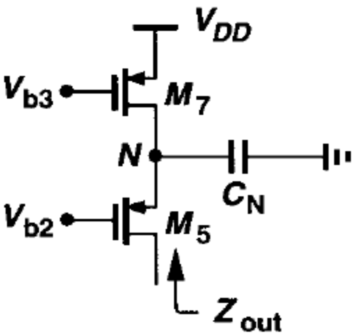
Figure 10.21

Fully differential telescopic op amp

this topology avoids the mirror pole exhibiting stable behavior for a greater bandwidth.

one dominant pole at each output node

how about the pole at node N?



$$C_N = C_{GS5} + C_{SB5} + C_{GD7} + C_{DB7},$$

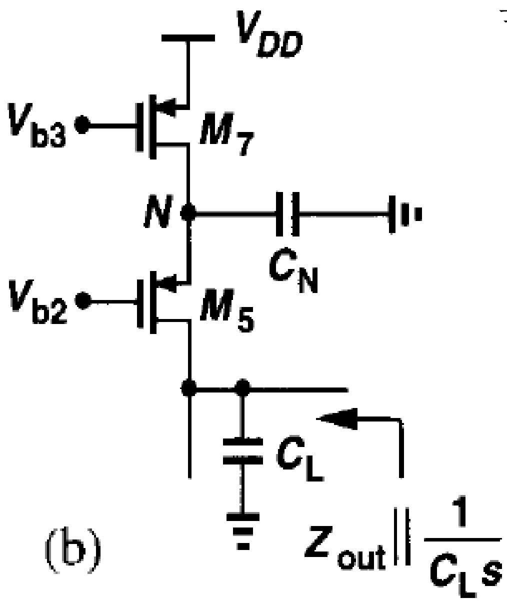
$$Z_N = r_{O7} || (C_N s)^{-1}$$

assume body effect is neglected

$$Z_{out} = (1 + g_{m5} r_{O5}) Z_N + r_{O5}, \qquad (10.19)$$

$$\approx (1 + g_{m5} r_{O5}) \frac{r_{O7}}{r_{O7} C_N s + 1}.$$

Fully differential telescopic cascode (cont.)



(b)

Figure 10.22

节点关联的独立电容数决定了节点对应的极点数

take the output load capacitance into account:

$$Z_{out}||\frac{1}{C_L s} = \frac{(1+g_{m5}r_{O5})\dfrac{r_{O7}}{r_{O7}C_N s+1}\cdot\dfrac{1}{C_L s}}{(1+g_{m5}r_{O5})\dfrac{r_{O7}}{r_{O7}C_N s+1}+\dfrac{1}{C_L s}}$$

$$= \frac{(1+g_{m5}r_{O5})r_{O7}}{[(1+g_{m5}r_{O5})r_{O7}C_L + r_{O7}C_N]s+1}.$$

the overall time constant equals the "output" time constant plus $r_{O7}C_N$.

The key point is that the pole in the PMOS cascode is *merged* with the output pole,

It merely lowers the dominant pole by a slight amount.

the circuit contains only one nondominant pole located at relatively high frequencies owing to the high transconductance of the NMOS

负载管M5~M8不会增加新极点！但会稍微降低输出极点频率值。

10.5 Compensation of two-stage op amps

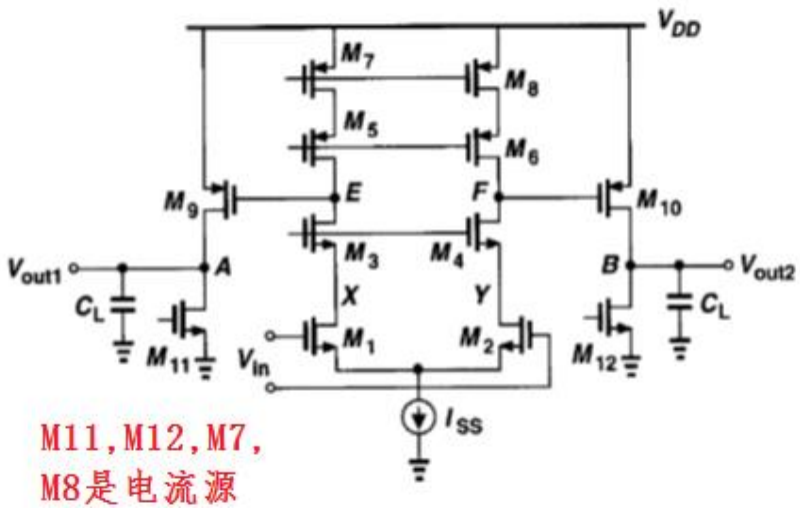
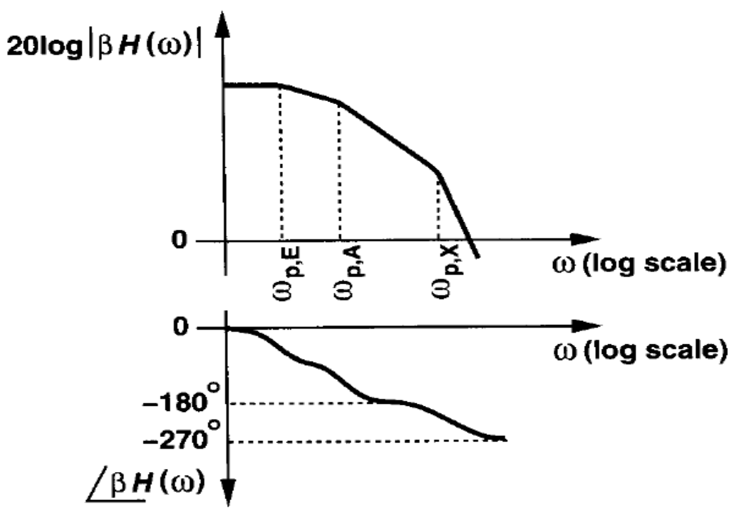


Figure 10.23 Two-stage op amp.



if the output voltage swing must be maximized.

We identify three poles: a pole at X (or Y), another at E (or F), and a third at A (or B).

the pole at X lies at relatively high frequencies.

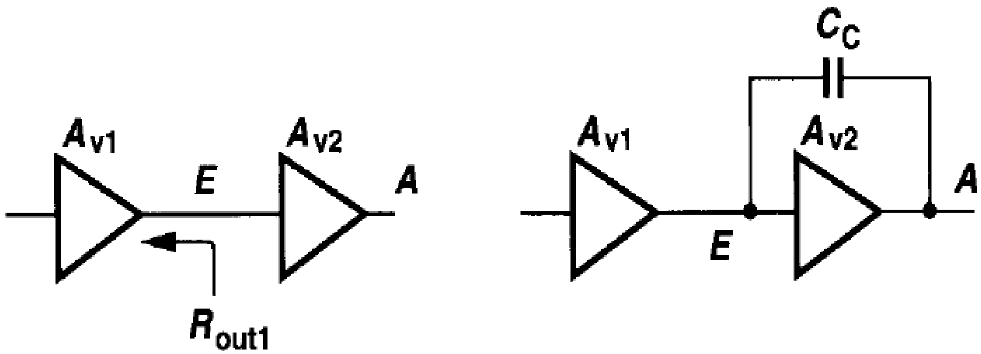
the circuit exhibits *two* dominant poles.

one of the dominant poles must be moved toward the origin so as to place the gain crossover well below the phase crossover.

the unity-gain bandwidth after compensation cannot exceed the frequency of the second pole of the open loop system.

bandwidth is limited to approximately $\omega_{p,A}$

Miller compensation



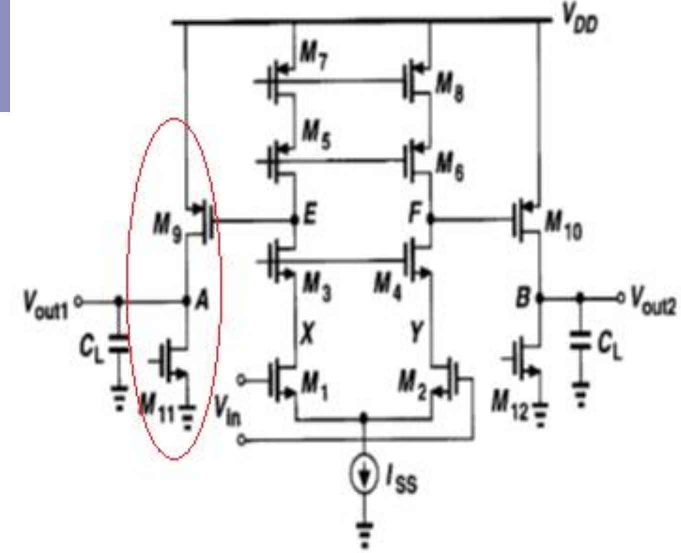


Figure 10.25 Miller compensation of a two-stage op amp.

the idea is to create a large capacitance at node E, equal to $(1+A_{v2})C_C$,

the corresponding pole to $R_{out1}^{-1}[C_E + (1 + A_{v2})C_C]^{-1}$,

Av2反向放大器

In addition to lowering the required capacitor value, Miller compensation entails a very important property: it moves the *output* pole *away* from the origin.

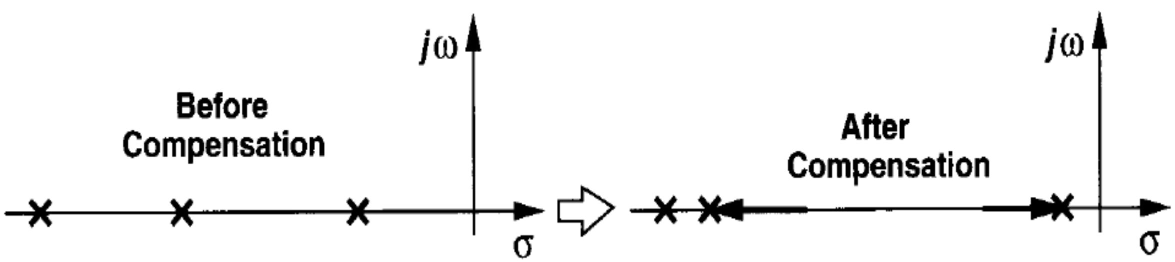
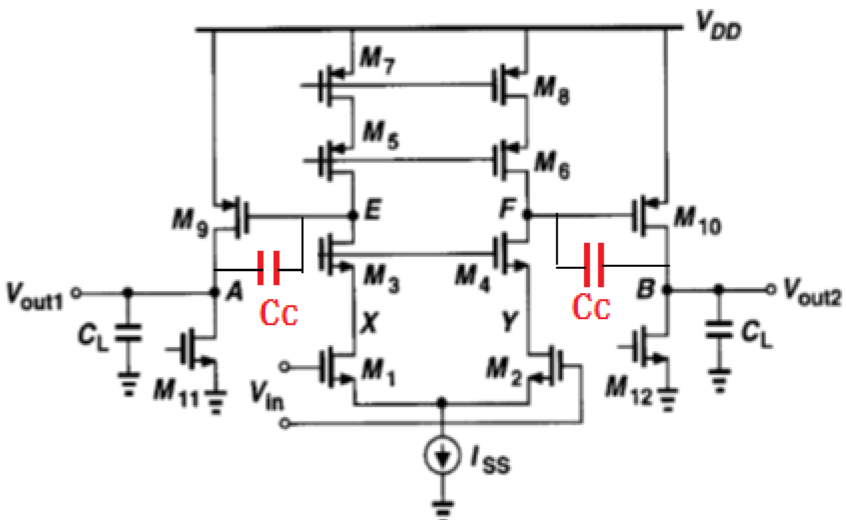
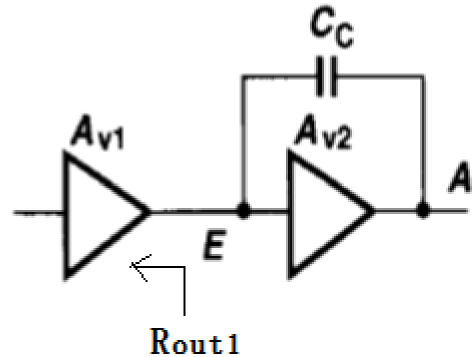


Figure 10.26 Pole splitting as a result of Miller compensation.

单位增益频率估算





第一级： $A_{v1}=g_{m1}[R_{out1}||1/(A_{v2}SC_C)]$

总增益： $A_v=A_{v1}A_{v2}$

高频时：

$$A_v\,(s) \approx g_{m1}\frac{1}{A_{v2}SC_C}\times A_{v2}=\frac{g_{m1}}{SC_C}$$

单位增益频率ω_u, 则$|A_V(\omega_u)|=1$, 即 $\dfrac{g_{m1}}{\omega_u C_C}=1, \therefore\ \omega_u\approx\dfrac{g_{m1}}{C_C}$

单位增益频率一般是（0.5~0.6）*第1次极点频率 ω_{p2}（PM=60°）

稳定系统必小于第2次极点频率 ω_{p3}　　若$\omega_{p2}=\omega_u$，$PM\approx45^{o}$

Miller compensation (cont.)

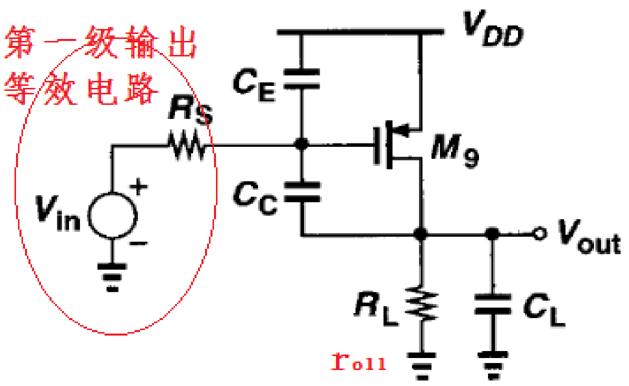


Figure 10.27 Simplified circuit of a two-stage op amp.

simplify the output stage of Fig. 10.23 as in Fig. 10.27, where R_S denotes the output resistance of the first stage and $R_L = r_{O9} \| r_{O11}$.

From fig. 6.10 , equation (6.26) and (6.32):

$$\omega_{p1} \approx \frac{1}{R_S[(1 + g_{m9}R_L)(C_C + C_{GD9}) + C_E] + R_L(C_C + C_{GD9} + C_L)} \qquad (10.23)$$

$$\omega_{p2} \approx \frac{R_S[(1 + g_{m9}R_L)(C_C + C_{GD9}) + C_E] + R_L(C_C + C_{GD9} + C_L)}{R_S R_L[(C_C + C_{GD9})C_E + (C_C + C_{GD9})C_L + C_E C_L)]}. \qquad (10.24)$$

These expressions are based on the assumption $|\omega_{p1}| \ll |\omega_{p2}|$.

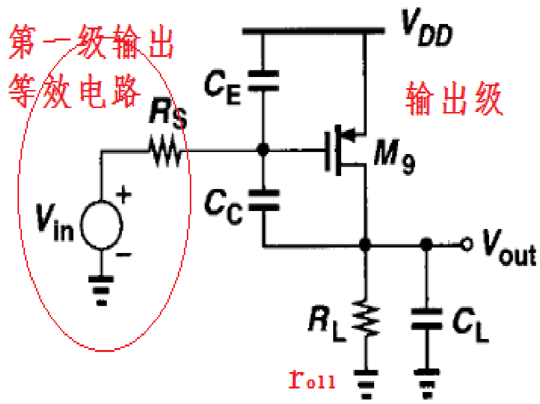
Before compensation, however, ω_{p1} and ω_{p2} are of the same order of magnitude.

Comparing wp2 before and after compensation

For $C_C = 0$ and relatively large C_L, the output pole

$$\omega_{p2} \approx 1/(R_L C_L).$$

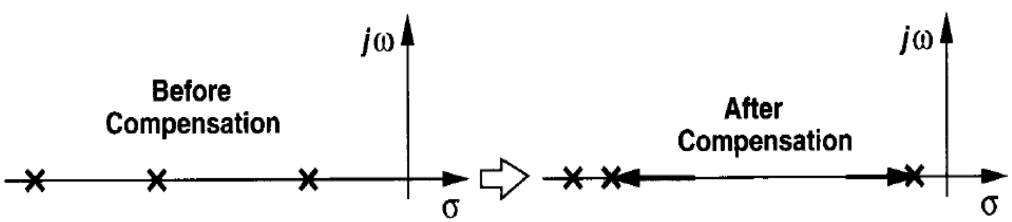
未补偿时开环第1次极点>
补偿后的单位增益带宽



$$\omega_{p2} \approx \frac{R_S[(1+g_{m9}R_L)(C_C+C_{GD9})+C_E]+R_L(C_C+C_{GD9}+C_L)}{R_S R_L[(C_C+C_{GD9})C_E+(C_C+C_{GD9})C_L+C_E C_L)]}$$

typically $C_C + C_{GD9} \gg C_E$, $\omega_{p2} \approx g_{m9}/(C_E + C_L)$. $= g_{m9}/C_L$ $C_E \ll C_L$ 近似估算

Miller compensation increases the magnitude of the output pole by roughly a factor of $g_{m9}R_L$



$$\text{补偿后次极点改变} = \frac{g_{m9}/C_L}{1/R_L C_L} = g_{m9}R_L = g_{m9}(r_{o11} \,||\, r_{o9})$$

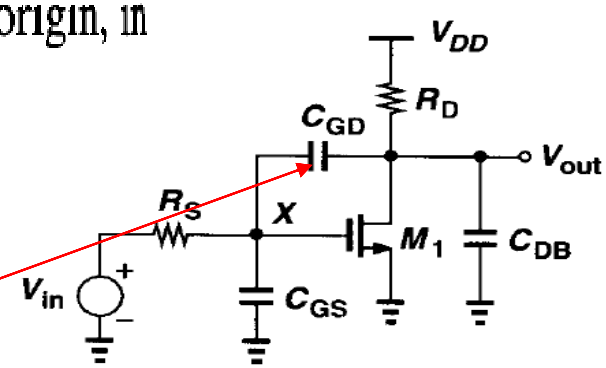
PM增大

C_C provides a low impedance between the gate and drain of M_9, reducing the resistance seen by C_L from R_L to roughly $R_S || g_{m9}^{-1} || R_L \approx g_{m9}^{-1}$.

Miller compensation allowing a much greater bandwidth than that obtained by merely connecting the compensation capacitor from one node to ground.

Effect of zero of transfer function

While in cascode topologies, the zeros are quite far from the origin, in two-stage op amps incorporating Miller compensation, a nearby zero appears in the circuit.



Recall from (6.23)

$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + [R_S(1+g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD}+C_{DB})]s + 1}$$

Figure 6.10

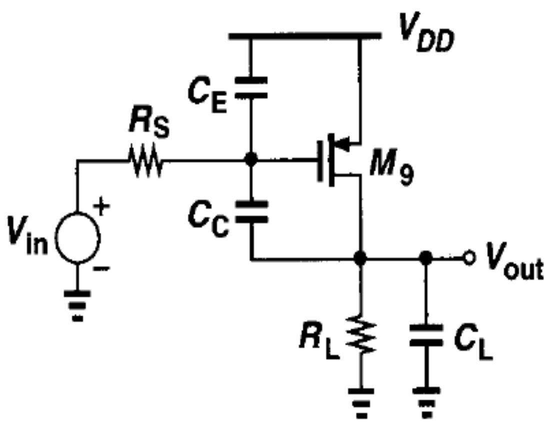


Figure 10.27

$\omega_z = g_{m9}/(C_C + C_{GD9})$. 右半平面是坏的正零点！

$(1 - s/\omega_z)$, yielding a phase of $-\tan^{-1}(\omega/\omega_z)$,

a zero in the right half plane contributes more phase shift, moving the phase crossover toward the origin. Furthermore, the zero slows down the drop of the magnitude, thereby pushing the gain crossover away from the origin.

As a result, the stability degrades considerably.

Effect of zero of transfer function (cont.)

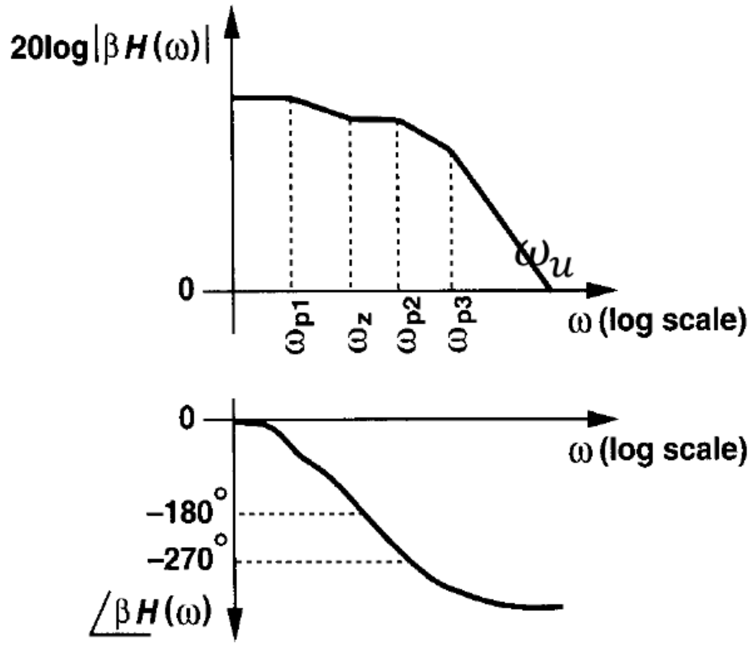


Figure 10.28 Effect of right half plane zero.

a third- order system

a zero in the right half plane ω_z.

单独C_C补偿后$\omega_{p2} \approx g_{m9}/C_L$,

$\omega_z \approx g_{m9}/C_C$

单位增益频率$\omega_u \approx \dfrac{g_{m1}}{C_C}$,

从稳定性上考虑，零点ω_Z应 $> \omega_u$

$g_{m1} < g_{m9}$

Modify zero

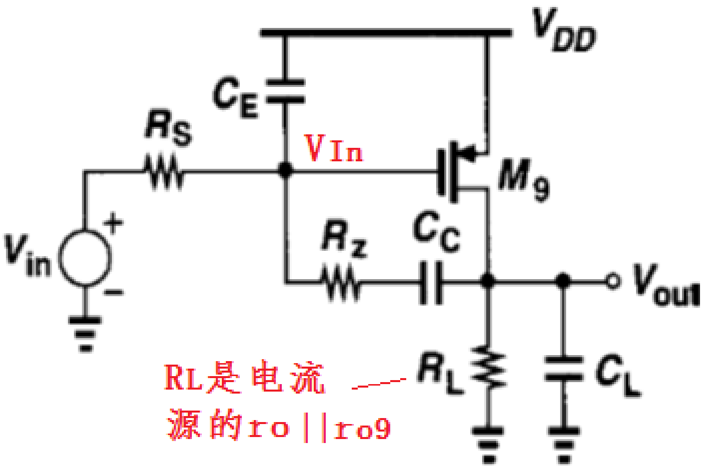


Figure 10.29 Addition of R_z to move the right half plane zero.

The output stage now exhibits *three* poles,

At the zero, Vout = 0. and

$$\frac{V_{In}}{R_z+\frac{1}{S_z C_c}} = g_{m9} V_{in}$$

$$\left(\frac{1}{g_{m9}} - R_z\right)^{-1} = S_z C_c$$

$$\therefore S_z = \frac{1}{C_c(g_{m9}^{-1}-R_z)}$$

叠加定律:
2路电流形成Vout
Vout=短路电流
*输出阻抗

$$\omega_z \approx \frac{1}{C_C\left(g_{m9}^{-1} - R_z\right)}.$$

使Rz>g_{m9}^{-1}，零点<0，在s左半平面

Thus, if $R_z \geq g_{m9}^{-1}$, then $\omega_z \leq 0$. While $R_z = g_{m9}^{-1}$ seems a natural choice, in practice we may even move the zero well into the left half plane so as to cancel the first nondominant pole. This occurs if

$$\frac{1}{C_C\left(g_{m9}^{-1} - R_z\right)} = \frac{-g_{m9}}{C_L + C_E} = -\omega_{p2}$$

使负零点与次极点相消，极点均在s左半平面

that is,

$$R_z = \frac{C_L + C_E + C_C}{g_{m9} C_C} \approx \frac{C_L + C_C}{g_{m9} C_C}, \qquad (10.28)$$

→Rz可用线性区电阻替代而真实电阻会受温度影响

Difficulties in Modifying zero

抵消ω_{p2}： $R_z = \dfrac{C_L + C_C}{g_{m9}C_C}$ 前提是C_E远小于$C_L + C_C$

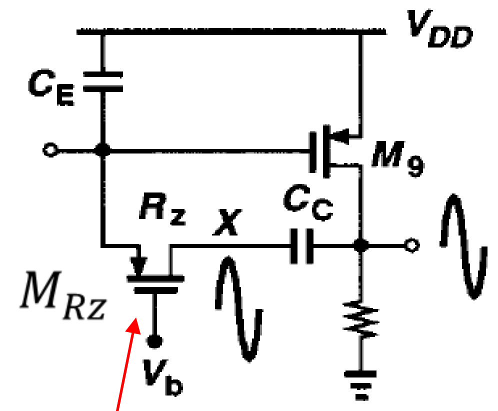


Figure 10.30

Effect of large output swings on R_Z.

if C_L is unknown or variable.

For example, in switched-capacitor circuits.

零极点抵消法需要C_L恒定，因此不适合开关电容电路

R_z changes substantially as output voltage excursions are coupled through C_C to node X, thereby degrading the large-signal settling response.

Vb使MRz的$|V_{GS}|>|V_{TH}|$，则PMOS自动工作在线性区！输出变化很大时，M_{Rz}导通电阻变化大，不好。

频率补偿是降低主极点，米勒效应（反馈）产生了零点，不是为了抵消极点而制造零点。米勒电容目的是降低电容值，并非必须使用。

Generation of Vb

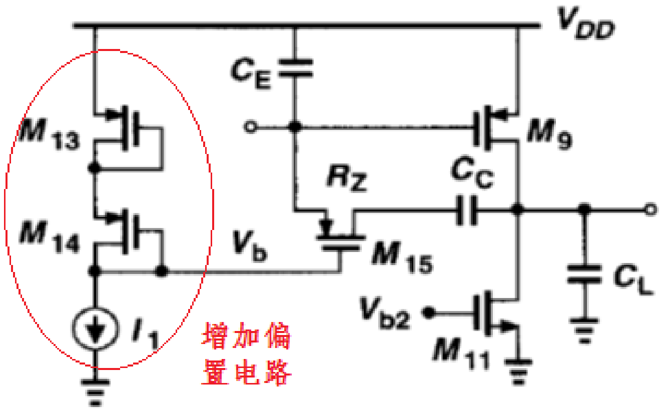


Figure 10.31 Generation of V_b for proper temperature and process tracking.

ω_Z抵消ω_{p2}, 则$R_z = \dfrac{C_L + C_C}{g_{m9} C_C}$

I_1 is chosen with respect to I_{D9} such that $V_{GS13} = V_{GS9}$, then $V_{GS15} = V_{GS14}$. Since

$$R_{on15} = [\mu_p C_{ox}(W/L)_{15}(V_{GS15} - V_{TH15})]^{-1}$$

$$g_{m14} = \mu_p C_{ox}(W/L)_{14}(V_{GS14} - V_{TH14})$$

we have $R_{on15} = g_{m14}^{-1}(W/L)_{14}/(W/L)_{15}$.

$$R_{on15} = g_{m14}^{-1}\frac{(W/L)_{14}}{(W/L)_{15}} = g_{m9}^{-1}\left(1 + \frac{C_L}{C_C}\right) \qquad (10.29)$$

and hence

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}$$

$$(W/L)_{15} = \sqrt{(W/L)_{14}(W/L)_9}\sqrt{\frac{I_{D9}}{I_{D14}}\frac{C_C}{C_C + C_L}} \qquad (10.30)$$

$$I_{D14} = I_1$$

不同零点的讨论

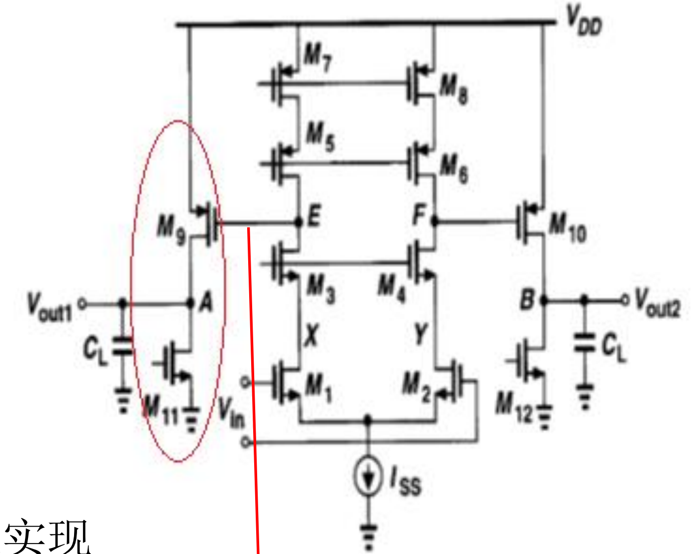
当$C_C + C_{GD9} >> C_E$时：$\omega_{p2} \approx \dfrac{g_{m9}}{C_L + C_E} \approx \dfrac{g_{m9}}{C_L}$

左半平面零点$1 + \dfrac{s}{\omega_Z}$，这里$\omega_Z \approx \dfrac{1}{C_C(R_z - 1/g_{m9})}$

零点设计方案*1.*

使ω_Z很大：$R_Z = \dfrac{1}{g_{m9}}$

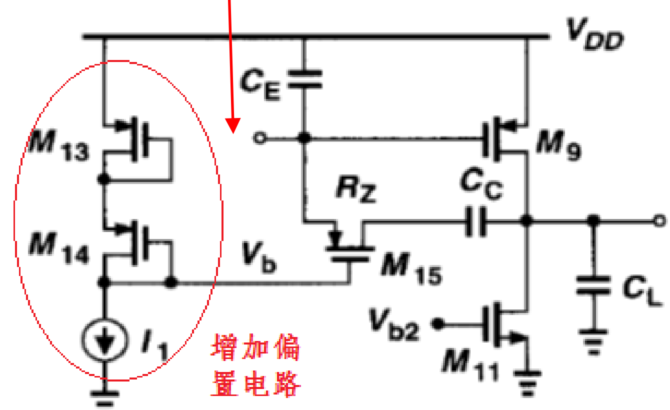
若零点很大，则无论正负，均视为无影响



零点设计方案2. MOS管做为电阻，

使ω_Z抵消ω_{p2}：$R_z = \dfrac{C_L + C_C}{g_{m9}C_C}$，$C_L$不变时可用$M_{RZ}$较精确地实现

验证：$\omega_Z \approx \dfrac{1}{C_C(R_z - 1/g_{m9})} = \dfrac{1}{C_C\left(\dfrac{C_L + C_C}{g_{m9}C_C} - 1/g_{m9}\right)} = \dfrac{g_{m9}}{C_L}$



零点设计方案*3.* 用较大电阻R_Z，近似抵消ω_{p2}。

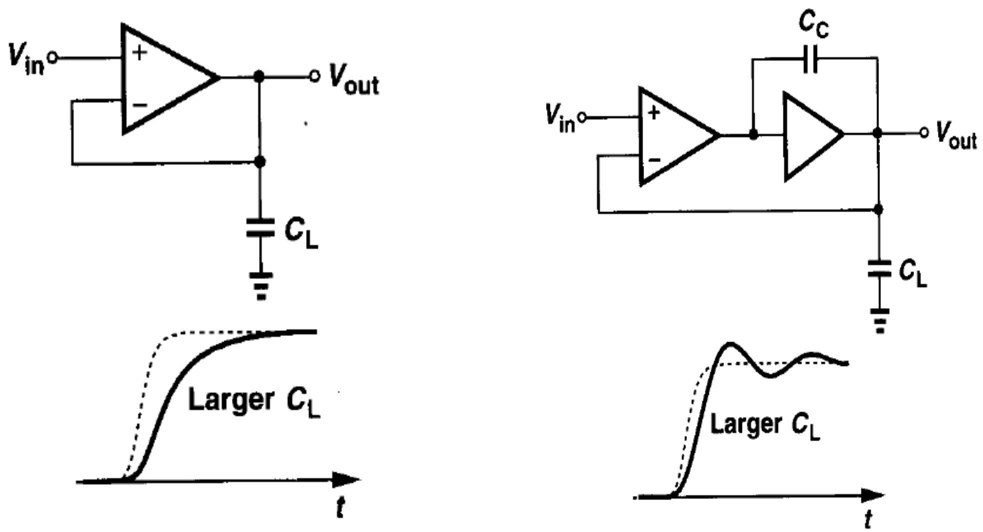
例如：取$R_Z = \dfrac{5}{g_{m9}}$，则$Cc = C\,L/4$

好处是可使C_c较小（$C_c >> C_E$），缺点是可能补偿不够。

$\omega_u \approx \dfrac{g_{m1}}{C_C}$，$C_C$小则$\omega_u$大，一般$\omega_u < \omega_{p2}(PM > 45^o)$

两级运放对负载电容敏感

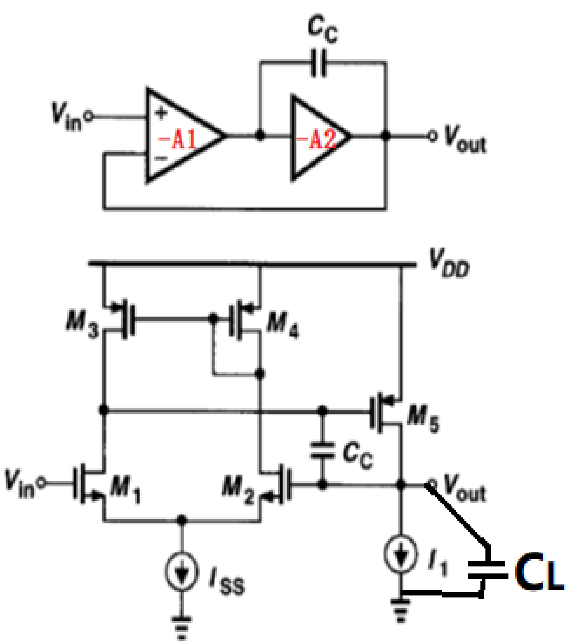
An attribute of two-stage op amps that makes them inferior to "one-stage" op amps is the susceptibility to the load capacitance. Since Miller compensation establishes the dominant pole at the output of the first stage, a higher load capacitance presented to the second stage moves the second pole toward the origin, degrading the phase margin. By contrast, in one-stage op amps, a higher load capacitance brings the *dominant* pole closer to the origin, *improving* the phase margin (albeit making the feedback system more overdamped).



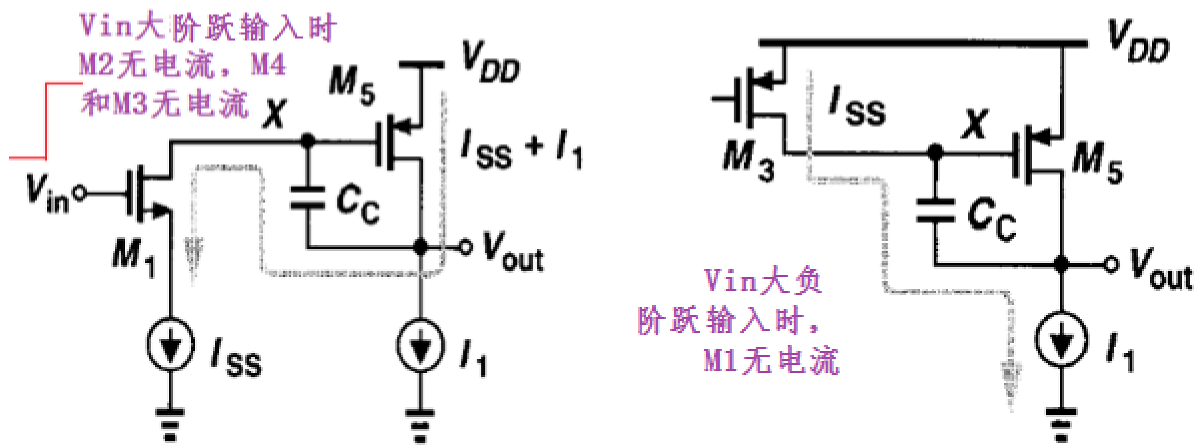
一级运放的负载电容，使主极点向低频移动，有利于稳定性。
两级运放的负载电容，使次极点向低频移动，不利于稳定性。

Figure 10.33 Effect of increased load capacitance on step response of one- and two-stage op amps.

Slewing in two-stage op amps



(a)



(b) (c)

Figure 10.34 (a) Simple two-stage op amp, (b) simplified circuit during positive slewing, (c) simplified circuit during negative slewing.

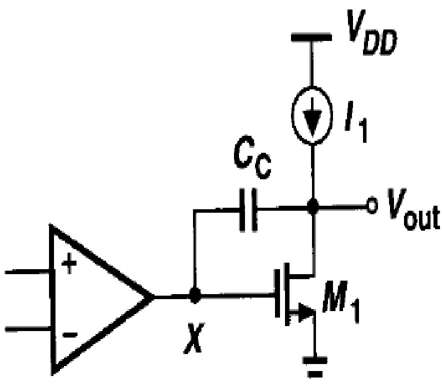
Suppose V_{in} experiences a large positive step at $t = 0$, turning off M_2, M_4, and M_3. The circuit can then be simplified to that in Fig. 10.34(b),

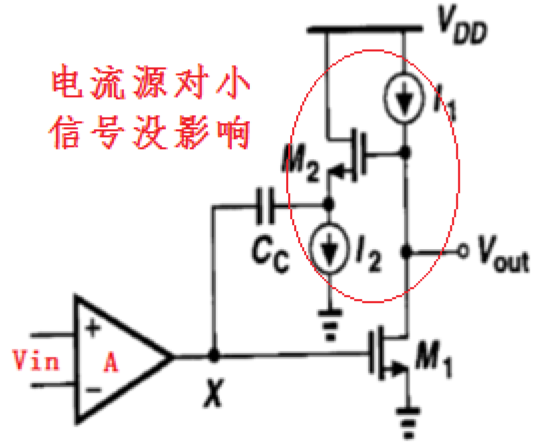
Recognizing that the gain of the output stage makes node X a virtual ground, $V_{out} \approx I_{SS} t / C_C$. $I_1 > I_{SS}$. 实际设计中要考虑C_L输出摆率（负载C_L放电）

If M_5 is not wide enough to sustain $I_{SS} + I_1$ in saturation, then V_X drops significantly, in Fig. 10.34(c). I_1 must support both I_{SS} and I_{D5}. Cc影响转换速率，Cc大则Iss大

10.6 other compensation techniques

The difficulty in compensating two-stage CMOS op amps arises from the feedforward path formed by the compensation capacitor [Fig. 10.35(a)]. If C_C could conduct current from the output node to node X but not vice versa, then the zero would move to a very high frequency.





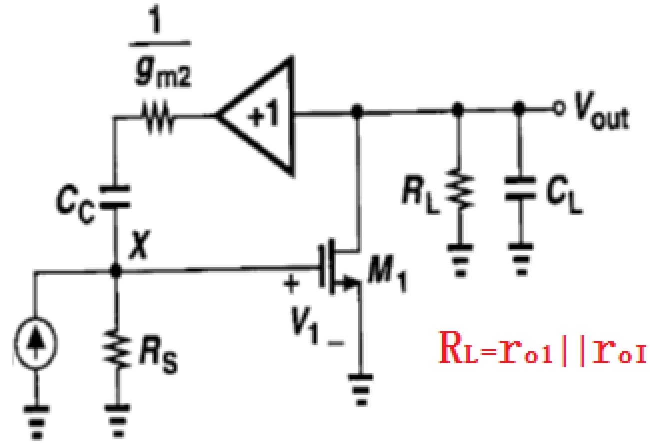


Figure 10.36

Figure 10.35 (a) M2可能会限制Vout (b)

(a) Two-stage op amp with right half plane zero due to C_C, (b) addition of a source follower to remove the zero.

令Vx=V1

$$-g_{m1}V_1 = V_{out}(R_L^{-1} + C_L s)$$

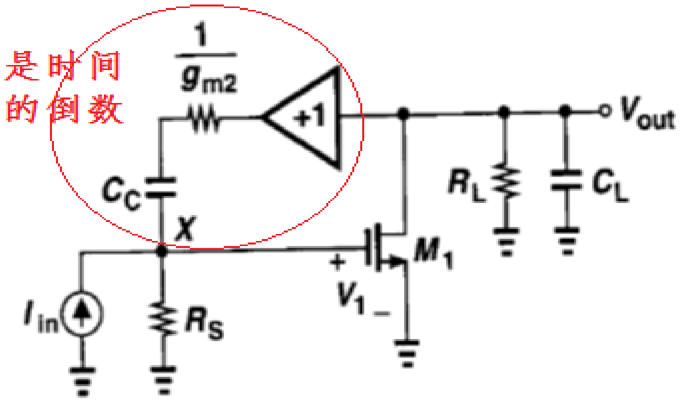
输出级为电压电流负反馈，R_S 为A内的输出阻抗，$I_{in}=A*V_{in}/R_S$

hence

$$V_1 = \frac{-V_{out}}{g_{m1}R_L}(1 + R_L C_L s). \qquad (10.31)$$

阻断补偿电容的前馈通路

$$\frac{V_{out}-V_1}{\frac{1}{g_{m2}}+\frac{1}{C_C s}}+I_{in}=\frac{V_1}{R_S}.$$



Substituting for V_1 from (10.31) yields:

$$\frac{V_{out}}{I_{in}}=\frac{-g_{m1}R_L R_S(g_{m2}+C_C s)}{R_L C_L C_C(1+g_{m2}R_S)s^2+[(1+g_{m1}g_{m2}R_L R_S)C_C+g_{m2}R_L C_L]s+g_{m2}}. \quad (10.33)$$

Thus, the circuit contains a zero in the *left* half plane, which can be chosen to cancel one of the poles.

Since typically $1+g_{m2}R_S \gg 1$ and $(1+g_{m1}g_{m2}R_L R_S)C_C \gg g_{m2}R_L C_L$, we have

$$\omega_{p1}\approx\frac{g_{m2}}{g_{m1}g_{m2}R_L R_S C_C}\approx\frac{1}{g_{m1}R_L R_S C_C}, \quad (10.35)$$

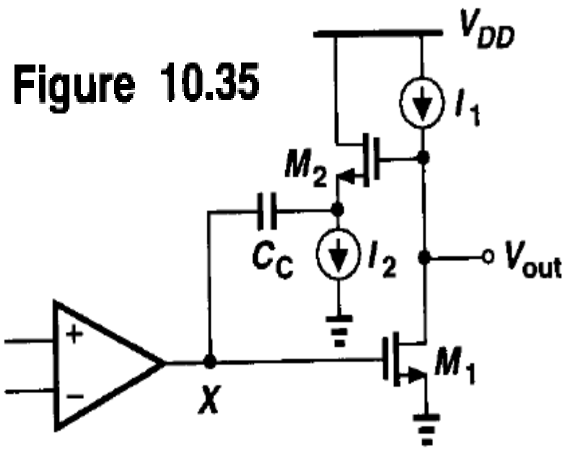
米勒效应进行极点近似估计

$$\omega_{p2}\approx\frac{g_{m1}g_{m2}R_L R_S C_C}{R_L C_L C_C g_{m2}R_S}\approx\frac{g_{m1}}{C_L}.$$

the output pole has moved from $(R_L C_L)^{-1}$ to g_{m1}/C_L.

环路增益$g_{m1}R_L$

Figure 10.35



M2可能会限制Vout

The primary issue in the circuit of Fig. 10.35(b) is that the source follower limits the lower end of the output voltage to $V_{GS2} + V_{I2}$,

utilize the compensation capacitor to isolate the dc levels in the active feedback stage from that at the output.

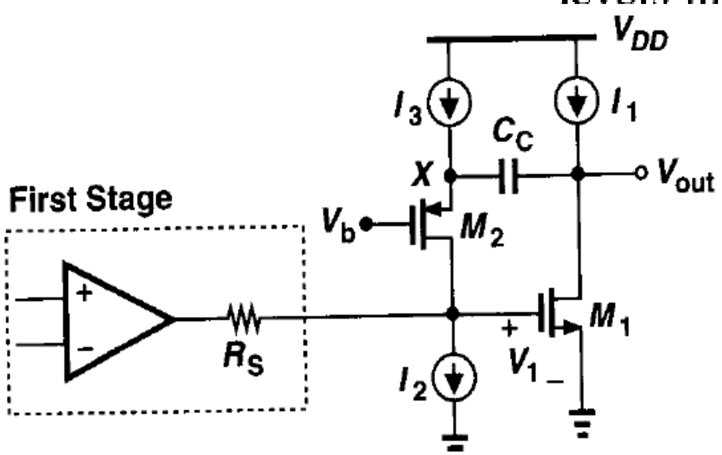
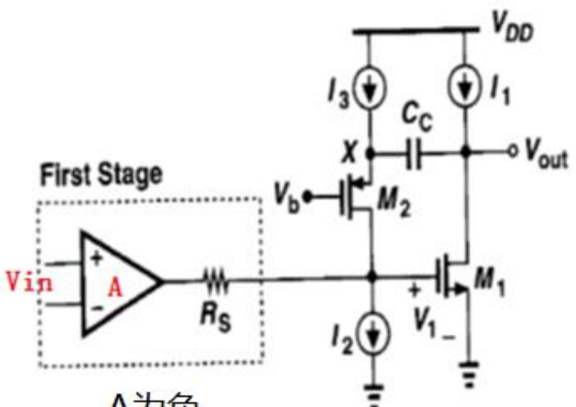


Figure 10.37 Compensation technique using a common-gate stage.

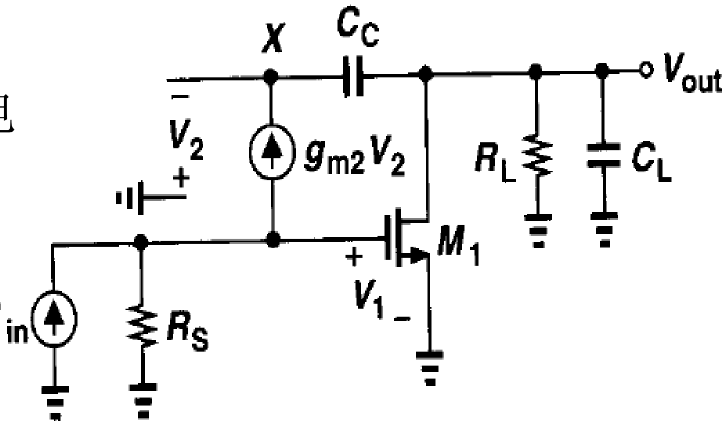
If V_1 changes by ΔV and V_{out} by $A_v \Delta V$, then the current through the capacitor is nearly equal to $A_v \Delta V C_C s$ because $1/g_{m2}$ can be relatively small.

providing a capacitor multiplication factor equal to A_v.

电路跨阻计算



A为负



电 压 电
流负反馈

Figure 10.37

Assuming $\lambda = \gamma = 0$

Figure 10.38 Simplified equivalent circuit of Fig. 10.37.

$$V_{out} + \frac{g_{m2}V_2}{C_C s} = -V_2 \rightarrow V_2 = -V_{out}\frac{C_C s}{C_C s + g_{m2}}.$$

主极点近似估计（米勒效应）

$$g_{m1}V_1 + V_{out}\left(\frac{1}{R_L} + C_L s\right) = g_{m2}V_2$$

$$I_{in} = V_1/R_S + g_{m2}V_2.$$

$I_{in}=A*V_{in}/R_S$

$$\rightarrow \frac{V_{out}}{I_{in}} = \frac{-g_{m1}R_S R_L(g_{m2} + C_C s)}{R_L C_L C_C s^2 + [(1 + g_{m1}R_S)g_{m2}R_L C_C + C_C + g_{m2}R_L C_L]s + g_{m2}} \quad (10.41)$$

极点近似值与直观估计

低频主极点 $$\omega_{p1} \approx \frac{1}{g_{m1} R_L R_S C_C} \quad (10.42)$$

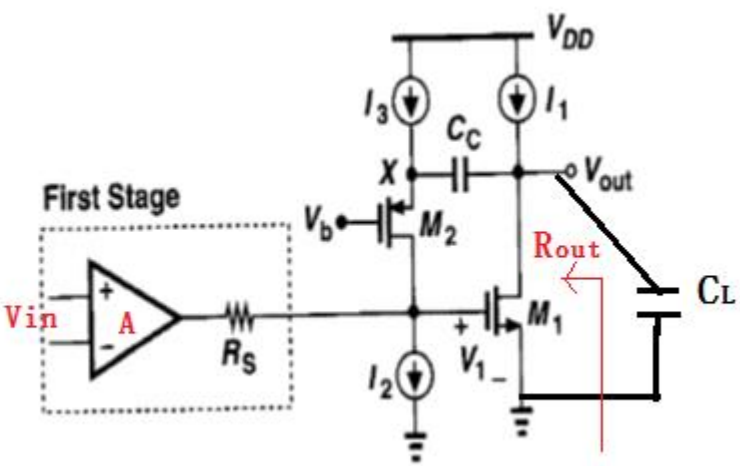
高频次极点 $$\omega_{p2} \approx \frac{g_{m2} R_s g_{m1}}{C_L}. \quad (10.43)$$

次极点增大

the second pole has considerably risen in magnitude — by a factor of $g_{m2} R_S$

Figure 10.35

$$\omega_{p2} \approx \frac{g_{m1}}{C_L} \quad (10.37)$$

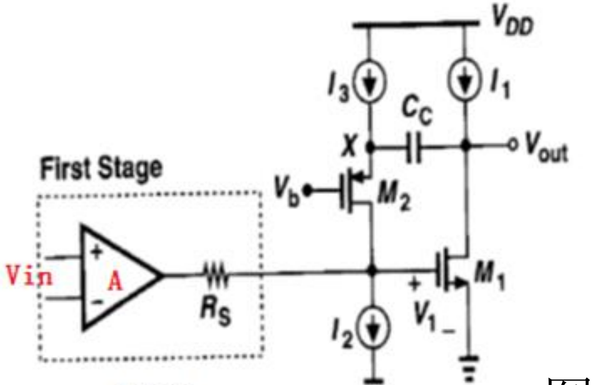


次极点近似估计：电压电流负反馈减小输出阻抗

环路增益：$g_{m1}R_{out}*g_{m2}R_S$
(可合理的近似看作C_C对于交变小信号短路）
输出阻抗=1/（$g_{m1}g_{m2}R_S$）

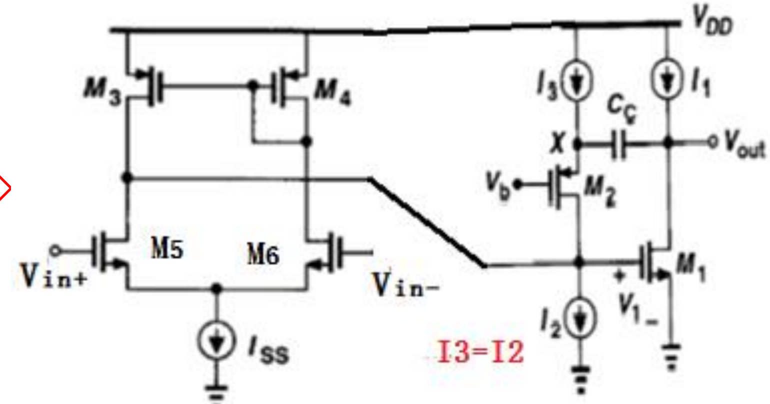
输出节点关联的极点$\omega_{p2} = 2\pi f_{p2} = \dfrac{g_{m1} g_{m2} R_S}{C_L}$

转换速率：对补偿电路电流源的要求

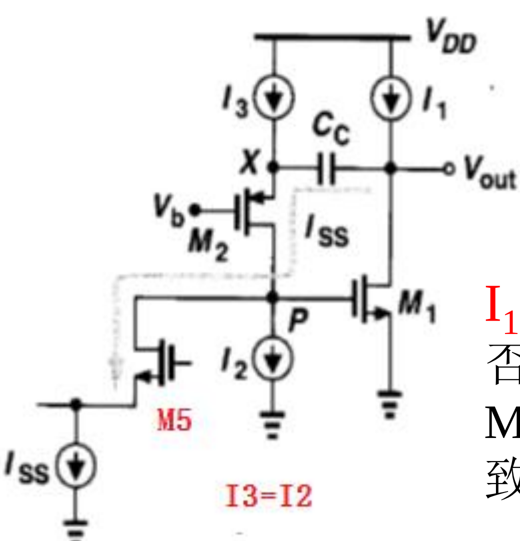


A为负

图10.37

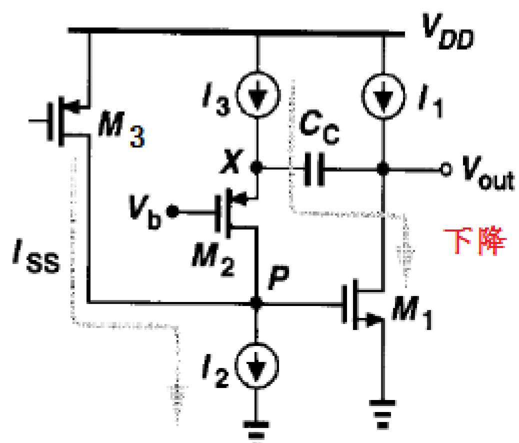


Vin有大的正阶跃输入时：



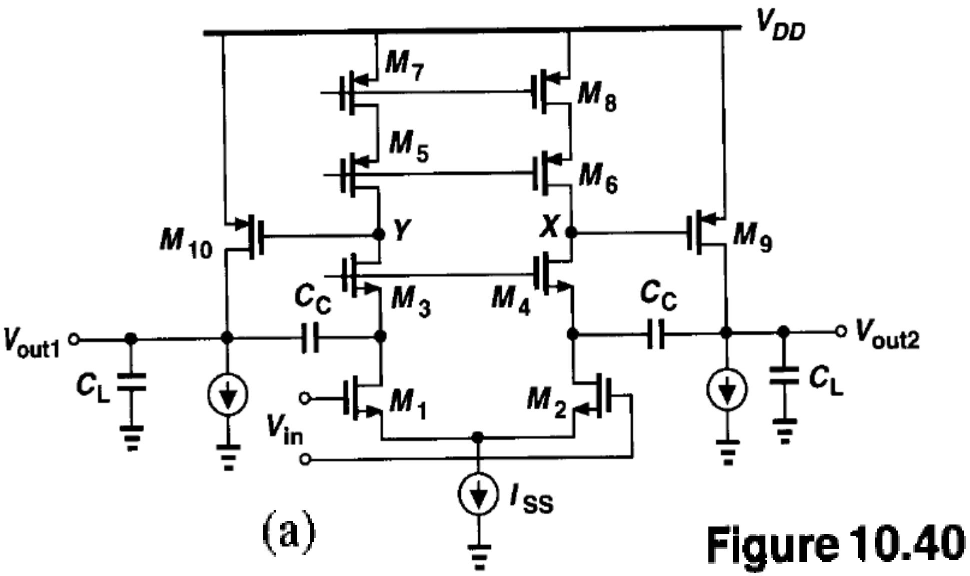
$I_1=I_{SS}+I_{D1}$
否则VP下降使M1电流减少，导致M1关断

Vin有大的负阶跃输入时

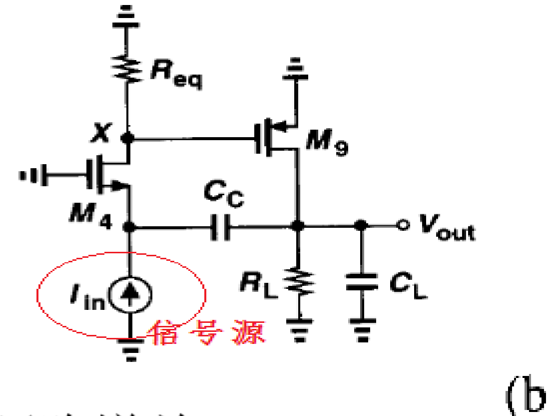


$I_2=I_{SS}+I_{D2}$
$I_{D1}=I_1+I_{SS}$
W1大（P可看作虚地）

针对cascode 2级OP的相位补偿



$$R_{eq} = g_{m6}r_{o6}r_{o8} \,||\, g_{m4}r_{o4}r_{o2}$$



环路增益$g_{m9}R_L g_{m4}R_{eq}$

(a) Alternative method of compensating two-stage op amps, (b) simplified equivalent circuit of (a).

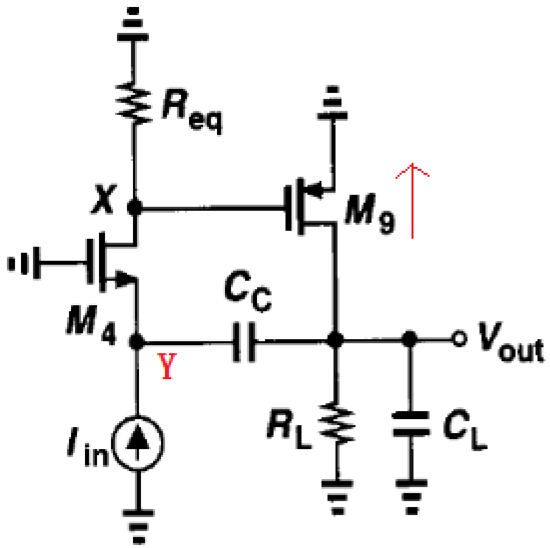
the dominant pole is located at approximately $(R_{eq}g_{m9}R_LC_C)^{-1}$, 主极点X，式10.42

the first nondominant pole is given by $g_{m4}g_{m9}R_{eq}/C_L$, 极点与输入无关，估算次极点为高频，Cc视作短路，环路增益 $= g_{m4}R_{eq}g_{m9}R_L$

can prove that the zero appears at $(g_{m4}R_{eq})(g_{m9}/C_C)$, 零点(信号通路上有2条与频率相关的支路)

In reality, the capacitance at X may not be negligible

计算零点



V_{out} 节点：

$$g_{m9}V_X + V_{out}(R_L^{-1} + SC_L) + (V_{out} - V_Y)SC_C = 0$$

Y节点：

$$I_{in} - g_{m4}V_Y + (V_{out} - V_Y)SC_C = 0$$

X节点：

$$\frac{V_X}{R_{eq}} - g_{m4}V_Y = 0$$

$$\frac{V_{out}}{I_{in}} = \frac{-(g_{m4}g_{m9}R_{eq} - SC_C)}{C_C C_L S^2 + (g_{m4}g_{m9}R_{eq} + R_L^{-1})SC_C + g_{m4}S\,(C_C + C_L) + R_L^{-1}g_{m4}} \approx -R_{eq}g_{m9}R_L \times \frac{1 - \dfrac{S}{g_{m4}g_{m9}R_{eq}/C_C}}{g_{m4}^{-1}R_L C_C C_L S^2 + R_{eq}g_{m9}R_L C_C S + 1}$$

$$= -R_{eq}g_{m9}R_L \times \frac{1 - \dfrac{S}{\omega_Z}}{\dfrac{S^2}{\omega_{p1}\omega_{p2}} + \dfrac{S}{\omega_{p1}} + 1}\text{由此得到}\omega_{p1} = \frac{1}{R_{eq}g_{m9}R_L C_C}, \omega_{p2} = g_{m4}g_{m9}R_{eq}/C_L$$

电路如何改造为s左半平面负零点？

对照图10 .37进行改进

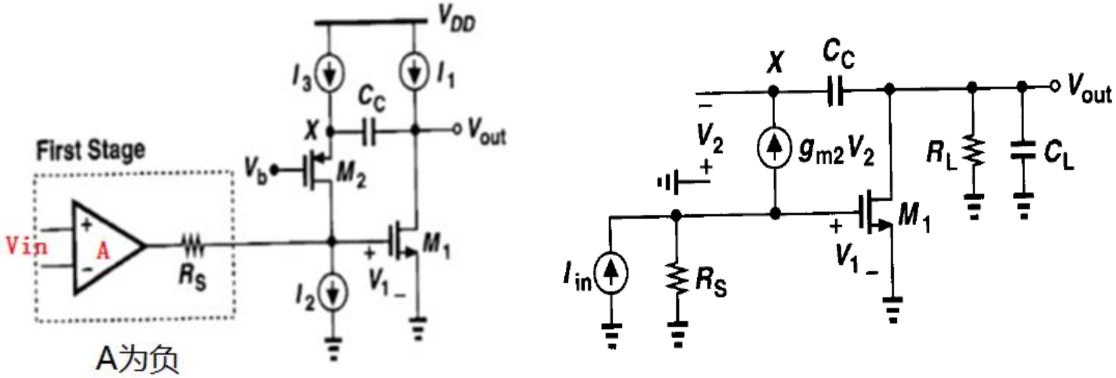


Figure 10.37

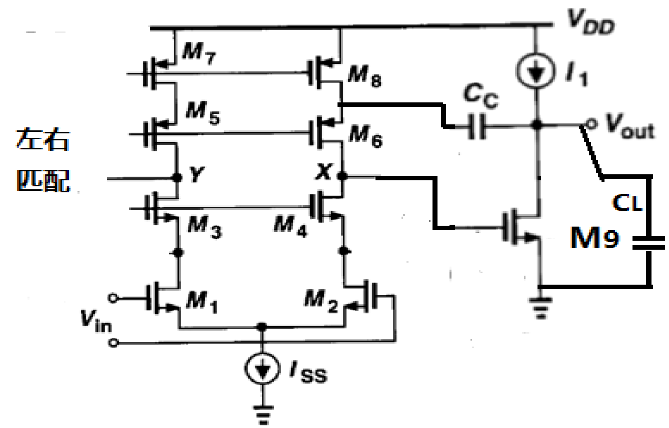


图10.99

$$\frac{V_{out}}{I_{in}}=\frac{-g_{m9}R_SR_Lg_{m6}\left(1+\frac{s}{g_{m6}/C_C}\right)}{R_LC_CC_Ls^2+[(1+g_{m9}R_S)g_{m6}R_LC_C+C_C+g_{m6}R_LC_L]s+g_{m6}}$$

$$\approx\frac{-R_S\,g_{m9}R_L\left(1+\frac{s}{g_{m6}/C_C}\right)}{R_Lg_{m6}^{-1}C_CC_Ls^2+R_Sg_{m9}R_LC_Cs+1}\qquad \omega_{p1}=\frac{1}{R_Sg_{m9}R_LC_C}$$

$$I_{in}=\frac{V_{in}A}{R_S}=V_{in}g_{m2}\qquad R_S\approx g_{m4}r_{o4}r_{o2}||g_{m6}r_{o6}r_{o8}\qquad \omega_{p2}=\frac{R_Sg_{m6}g_{m9}}{C_L}$$