S- and C-Band Ultra-Compact Phase Shifters Based on All-Pass Networks

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***Abstract*—Ultra-compact phase shifters are presented. The proposed phase-shifting circuits utilize the lumped element all-pass networks. The transition frequency of the all-pass network, which determines the size of the circuit, is set to be much higher than the operating frequency. This results in a significantly small chip size of the phase shifter. To verify this methodology, 5-bit phase shifters have been fabricated in the S- and C-band. The S-band phase shifter, with a chip size of 1.87 mm $\times$ 0.87 mm (1.63 mm^2), has achieved an insertion loss of 6.1 dB $\pm$ 0.6 dB and rms phase-shift error of less than 2.8° in 10% bandwidth. The C-band phase shifter, with a chip size of 1.72 mm $\times$ 0.81 mm (1.37 mm^2), has demonstrated an insertion loss of 5.7 dB $\pm$ 0.8 dB and rms phase-shift error of less than 2.3° in 10% bandwidth.**

***Index Terms*—All-pass network, compact size, monolithic microwave integrated circuit (MMIC), phase shifter.**

I. Introduction

PHASE shifters have been widely used in active phased array antennas (APAAs) for electronic beam steering [1]; phase shifters can be analog or digital. Analog phase shifters provide a continuously variable phase shift and demonstrate lower insertion loss when compared to digital [2]. Digital phase shifters provide a discrete set of phase shifts and are employed in many phased array applications. This is because they are more immune to their control voltage noise and temperature variation. Recently, compact monolithic microwave integrated circuit (MMIC) digital phase shifters have been developed for low-cost microwave applications [3]–[6].

The conventional digital phase shifters reported here are based on the high-pass filter [4], [5]. Theoretically, the cutoff frequency of the high-pass filter, determining the size of the phase shifters, is much lower than the operating frequency. Over the Ku-band, these phase shifters are quite easy to fabricate in MMICs because the circuit elements are reasonably small enough [4], [5]. In a low-frequency S- or C-band, however, the phase shifters need a relatively large chip area, as the cutoff frequency of the high-pass filter is much lower than the S- or C-band. It does not seem an effective solution, therefore, to employ the conventional circuit in the view of cost reduction resulting from the size of the MMIC.

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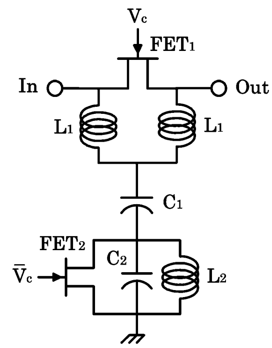

Fig. 1. Proposed phase-shifting circuit based on all-pass network.

To resolve this problem, phase-shifting circuits, based on an all-pass network, have been reported [7], [8]; these are suitable for microwave applications used in lower frequency bands. The transition frequency of the all-pass network, which determines the size of the circuit elements, can be set to be much higher than the operation frequency [8]. The phase-shifting circuit, though, inevitably has amplitude error and unwanted resonance near the operating frequency for a large phase shift in principle.

This paper describes phase-shifting circuits based on an all-pass network, which have low amplitude error performance and can avoid unwanted resonance. The low amplitude error is achieved by employing a parallel resonance circuit comprised of a field-effect transistor (FET) and capacitor rather than a single capacitor. Further, an improved configuration which utilizes an FET in place of a fixed capacitor constructing all-pass network for avoiding unwanted resonance at the reference state is proposed. The design equations for circuit elements are derived and the fabricated results in the S- and C-band are presented.

II. Circuit Configuration and Design Equations

Fig. 1 shows the proposed phase-shifting circuit based on an all-pass network. For the reference state shown in Fig. 2(a), FET_1 is turned on and the FET_2 is pinched off. To obtain low amplitude error, the capacitor of the parallel resonance circuit is realized by C_2 and $C_{\mathrm{off}2}$. The reflection coefficient S_{11r} and the transmission coefficient S_{21r} at the reference state are expressed as

$$S_{11r} = 1 - \frac{1}{1+\frac{1}{Z_0}\left(\frac{\varpi L_1 R_{\mathrm{on}1}}{2\varpi L_1 - jR_{\mathrm{on}1}}\right)} - \frac{1}{1+j\frac{1}{Z_0}\left(\varpi L_1 - \frac{2}{\varpi C_1} + \frac{2\varpi L_2}{1-\varpi^2 L_2 C_p}\right)} \quad (1)$$

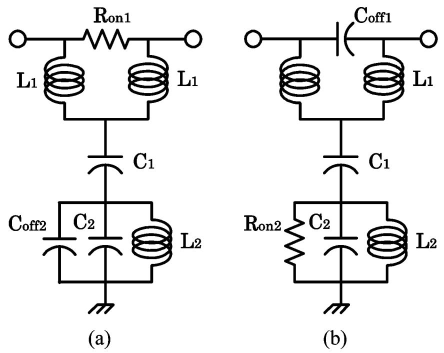

Fig. 2. Equivalent circuits of the proposed phase-shifting circuit. (a) Reference state. (b) Phase-shift state.

$$S_{21r} = \frac{1}{1+\frac{1}{Z_0}\left(\frac{\varpi L_1 R_{\mathbf{on1}}}{2\varpi L_1 - jR_{\mathbf{on1}}}\right)} - \frac{1}{1+j\frac{1}{Z_0}\left(\varpi L_1 - \frac{2}{\varpi C_1} + \frac{2}{1-\varpi^2 L_2 C_p}\right)} \tag{2}$$

where Z_0 is the system impedance and R_{on1} is the on-state resistance of FET_1 and C_p is the total capacitance of C_{off2} and C_2. To achieve impedance matching, the inductor L_2 is set to have parallel resonance with C_p at the operating frequency ϖ_0, expressed in the following equation:

$$L_2 = \frac{1}{\varpi_0^2 C_p}. \tag{3}$$

When R_{on1} is much smaller than the reactance of L_1, the circuit depicted in Fig. 2(a) can be considered as a single series resistor, having effectively zero phase response and the insertion loss due to R_{on1}. At operating frequency ϖ_0, (1) can be simplified using (3)

$$S_{11r}\big|_{\varpi=\varpi_0} \approx 1 - \frac{1}{1+R_{\mathbf{on1}}/2Z_0} \approx 0 \tag{4}$$

where it is assumed $R_{\mathrm{on1}} \ll \varpi_0 L_1,\ Z_0$. Likewise, (2) can be simplified as

$$S_{21r} \approx \frac{1}{1+j\frac{\varpi_0 C_p Z_0(\varpi/\varpi_0 - \varpi_0/\varpi)}{2} - \frac{1}{Z_0}\left(\varpi L_1 - \frac{2}{\varpi C_1}\right)}. \tag{5}$$

From (5), the phase response ϕ_r at the reference state can be calculated as

$$\begin{aligned}\phi_r &\equiv \angle S_{21r}\\ &\approx -\tan^{-1}\left(\frac{1}{\frac{2}{\varpi_0 C_p Z_0(\varpi/\varpi_0 - \varpi_0/\varpi)} - \frac{1}{Z_0}\left(\varpi L_1 - \frac{2}{\varpi C_1}\right)}\right).\end{aligned} \tag{6}$$

For the phase-shift state shown in Fig. 2(b), FET_1 is pinched off and FET_2 is turned on. The reflection coefficient S_{11p} and transmission coefficient S_{21p} at the phase-shift state are expressed as

$$\begin{aligned}S_{11p} &= 1 - \frac{1}{1+j\frac{1}{Z_0}\left(\frac{\varpi L_1}{1-2\varpi^2 L_1 C_{\mathbf{off1}}}\right)}\\ &\quad - \frac{1}{1+j\frac{1}{Z_0}\left(\varpi L_1 - \frac{2}{\varpi C_1}\right) + \frac{1}{Z_0}\left(\frac{2\varpi L_2 R_{\mathbf{on2}}}{\varpi L_2 - jR_{\mathbf{on2}}(1-\varpi^2 L_2 C_2)}\right)}\end{aligned} \tag{7}$$

$$\begin{aligned}S_{21p} &= \frac{1}{1+j\frac{1}{Z_0}\left(\frac{\varpi L_1}{1-2\varpi^2 L_1 C_{\mathbf{off1}}}\right)}\\ &\quad - \frac{1}{1+j\frac{1}{Z_0}\left(\varpi L_1 - \frac{2}{\varpi C_1}\right) + \frac{1}{Z_0}\left(\frac{2\varpi L_2 R_{\mathbf{on2}}}{\varpi L_2 - jR_{\mathbf{on2}}(1-\varpi^2 L_2 C_2)}\right)}\end{aligned} \tag{8}$$

where R_{on2} is the on-state resistance of FET_2 and C_{off1} is the off-state capacitance of FET_1. The circuit depicted in Fig. 2(b) can be considered as the lumped-element all-pass network composed of the off-state capacitor C_{off1}, two inductors L_1, and capacitor C_1, as long as R_{on2} is quite small. The impedance matching conditions are given as follows:

$$C_{\mathrm{off1}} = C/2 \quad C_1 = 2C \quad C = L_1/Z_0^2. \tag{9}$$

Here, we define the transition frequency ϖ_t as

$$\varpi_t \equiv 1/\sqrt{L_1 C}. \tag{10}$$

Using (9) and (10), (8) can be simplified as

$$S_{21p} \approx \frac{-1+j(\varpi/\varpi_t - \varpi_t/\varpi)}{1+j(\varpi/\varpi_t - \varpi_t/\varpi)}. \tag{11}$$

From (11), the phase response ϕ_p at the reference state can be calculated as

$$\begin{aligned}\phi_p &\equiv \angle S_{21p}\\ &\approx -\pi - 2\tan^{-1}(\varpi/\varpi_t - \varpi_t/\varpi).\end{aligned} \tag{12}$$

The phase shift $\phi = \phi_r - \phi_p$ can be calculated using (6), (9), and (12) in the following:

$$\begin{aligned}\phi &\approx -\pi - 2\tan^{-1}(\varpi/\varpi_t - \varpi_t/\varpi)\\ &\quad - \tan^{-1}\left(\frac{1}{\frac{2}{\varpi_0 C_p Z_0(\varpi/\varpi_0 - \varpi_0/\varpi)} - (\varpi/\varpi_t - \varpi_t/\varpi)}\right).\end{aligned} \tag{13}$$

Setting ϕ_0 as the desired phase shift at ϖ_0, ϖ_t can be expressed by ϖ_0 and ϕ_0 from (13) in the following:

$$\varpi_t = p\varpi_0 \quad p = \frac{1}{\frac{1}{2\tan(\phi_0/2)} + \sqrt{1+\frac{1}{4\tan^2(\phi_0/2)}}} \tag{14}$$

where p is determined according to only ϕ_0. The value of p increases as ϕ_0 decreases.

Using (9), (10), and (14), C_{off1}, C_1, and L_1 can be designed from the following equations:

$$C_{\text{off1}} = \frac{1}{2p\varpi_0 Z_0} \quad C_1 = \frac{2}{p\varpi_0 Z_0} \quad L_1 = \frac{Z_0}{p\varpi_0}. \tag{15}$$

Next, we derive the design equations for C_p and L_2. To obtain broadband phase-shift characteristics, it is required to satisfy the following condition:

$$\left.\frac{\partial \phi}{\partial \varpi}\right|_{\varpi=\varpi_0} = 0. \tag{16}$$

Substituting (10), (13), and (14) into (3) and (16), we obtain the following equation:

$$C_p = \frac{1}{\varpi_0 Z_0}\frac{2(p+1/p)}{1+(p-1/p)^2} \tag{17}$$

$$L_2 = \frac{Z_0}{\varpi_0}\frac{1+(p-1/p)^2}{2(p+1/p)}. \tag{18}$$

Finally, the design equations for C_2 and C_{off2} are derived. To yield low amplitude error, it is required that the transmission amplitudes at the reference state and phase-shift state are identical

$$|S_{21r}|_{\varpi=\varpi_0} = |S_{21p}|_{\varpi=\varpi_0}. \tag{19}$$

Substituting (5), (8), (15), (17), and (18) into (19), we obtain

$$R_{\text{on2}} = \frac{(1+P^2)\left(-A+\sqrt{A-(A-1)^2P^2}\right)}{2A[1+(A-1)P^2]}Z_0 \tag{20}$$

where

$$A = \frac{1+(1/Kp^2\varpi_0)^2}{1+\frac{1}{p^2}(1+1/Kp\varpi_0)^2}$$

$$P = p - \frac{1}{p}$$

$$K = R_{\text{on1}}C_{\text{off1}} = R_{\text{on2}}C_{\text{off2}}$$

where it is assumed $R_{\text{on2}} \ll \varpi_0 L_2$, and K is constant, which depends on the fabrication process. From (17) and (20), the following equations can be obtained:

$$C_{\text{off2}} = \frac{2AK[1+(A-1)P^2]}{Z_0(1+P^2)\left(-A+\sqrt{A-(A-1)^2P^2}\right)} \tag{21}$$

$$\begin{aligned} C_2 &= C_p - C_{\text{off2}} \\ &= \frac{1}{\varpi_0 Z_0}\frac{2(p+1/p)}{1+(p-1/p)^2} \\ &\quad - \frac{2AK[1+(A-1)P^2]}{Z_0(1+P^2)\left(-A+\sqrt{A-(A-1)^2P^2}\right)}. \end{aligned} \tag{22}$$

From (16)–(18), (21), and (22), all circuit elements can be designed. For example, in the case of $\varpi_0 = 2\pi \cdot 5$ GHz, $\phi_0 = 45^\circ, Z_0 = 50\ \Omega$ and $K = 0.4$ pF $\cdot\ \Omega$, it is obtained that $L_1 = 0.57$ nH, $L_2 = 1.7$ nH, $C_1 = 0.46$ pF, $C_{\text{off1}} = 0.11$ pF, $C_{\text{off2}} = 0.06$ pF, and $C_2 = 0.53$ pF. The transition frequency ($\varpi_t = 2\pi \cdot 13.9$ GHz) is much higher than ϖ_0 so the values of the circuit elements are reasonably small. Therefore, employing the proposed circuit is effective in view of cost reduction resulting from the size of the MMIC. Fig. 3 shows the calculation results for $\phi_0 = 45^\circ$. All of the circuit elements' constants are obtained from the above equations. It is shown that the impedance matching and equal transmission amplitude conditions are obtained at the center frequency. Further, the flatness of phase shift at ϖ_0 can be realized. Unwanted resonance occurs at $\varpi \cong 0.75\varpi_0$, though, for the reference state. This is due to the capacitor C_1 and inductor L_1, L_2. The resonant frequency is close to ϖ_0 as ϕ_0 increases. Fig. 4 shows the relationship between the unwanted resonance frequency and the phase shift ϕ_0. The limitation of the proposed circuit's bandwidth can be found by using this chart. For the large phase shift ($\phi_0 \cong 90^\circ$), some improvement for avoiding the unwanted resonance is required.

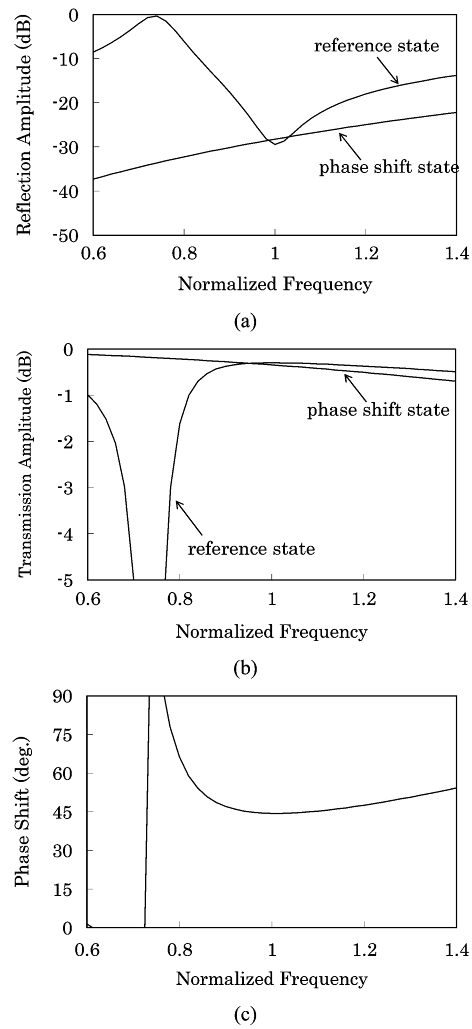

Fig. 3. Calculation results of the design example in the case of $\phi_0 = 45^\circ, Z_0 = 50\ \Omega$, and $K = 0.4$ pF $\cdot\ \Omega$. (a) Reflection amplitude. (b) Transmission amplitude. (c) Phase shift.

III. Improved Circuit for Large Phase Shift

At the reference state, the proposed circuit, based on the all-pass network in Fig. 1, has unwanted resonance due to the fixed capacitor C_1 and inductor L_1, L_2, as mentioned above. This resonance has a serious effect when large phase shifts are required ($\phi_0 \cong 90^\circ$). To solve this problem, an improved phase-shifting

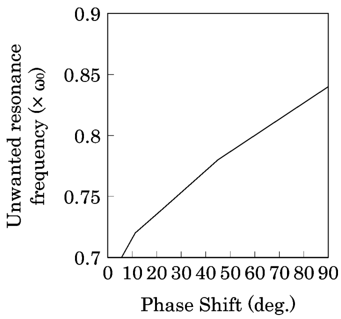

Fig. 4. Relationship between unwanted resonance frequency and phase shift ϕ_0.

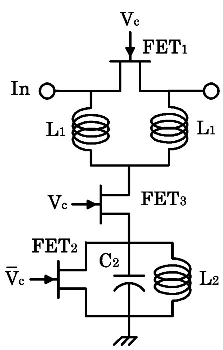

Fig. 5. Improved phase-shifting circuit based on all-pass network.

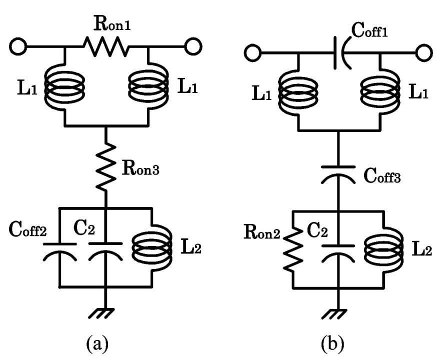

Fig. 6. Equivalent circuits of the improved phase-shifting circuit. (a) Reference state. (b) Phase-shift state.

circuit is proposed in Fig. 5. The difference between the circuit in Figs. 1 and 5 is that FET_3 is employed rather than the fixed capacitor C_1. For the reference state shown in Fig. 6(a), FET_1 and FET_3 are turned on and FET_2 is pinched off. If it is assumed $R_{\mathrm{on}1} \ll \varpi_0 L_1, R_{\mathrm{on}3}$, which is the on-state resistance of FET_3, does not affect electric property. The reflection and transmission coefficient are then expressed as (4) and (5).

For the phase-shift state shown in Fig. 6(b), FET_1 and FET_3 are pinched off and FET_2 is turned on. The reflection and transmission coefficient are equivalent, except that C_1 switches positions with $C_{\mathrm{off}3}$, which is the off-state capacitance of FET_3. $C_{\mathrm{off}3}$ can then be designed from the following equation:

$$C_{\mathrm{off}3} = \frac{2}{p\varpi_0 Z_0}. \tag{23}$$

Fig. 7 shows the calculation results for the design example in the case of $\phi_0 = 45°, Z_0 = 50\ \Omega$ and $K = 0.4\ \mathrm{pF} \cdot \Omega$. As shown in this figure, the improved circuit is useful in making the unwanted resonance disappear.

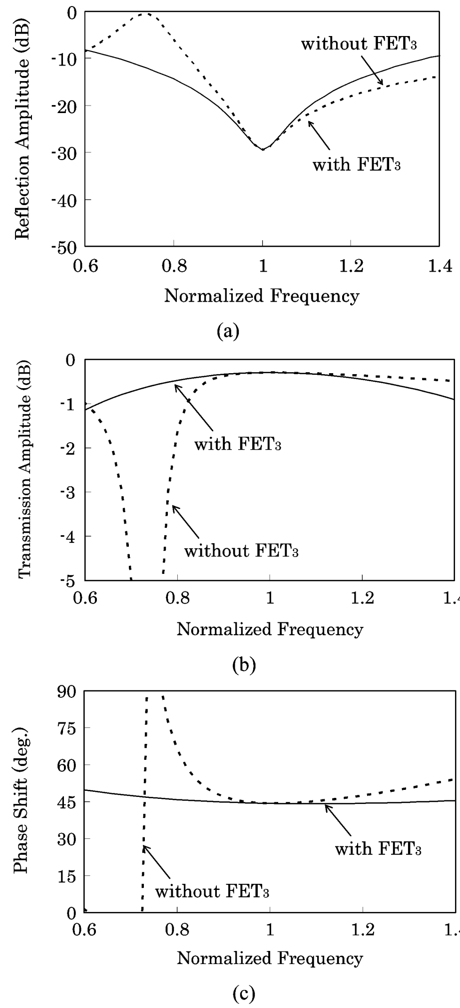

Fig. 7. Calculation results of design example in case of $\phi_0 = 45°, Z_0 = 50\ \Omega$, and $K = 0.4\ \mathrm{pF} \cdot \Omega$. (a) Reflection amplitude at the reference state. (b) Transmission amplitude at the reference state. (c) Phase shift. The dotted line is without FET_3. The solid line is with FET_3 (improved circuit).

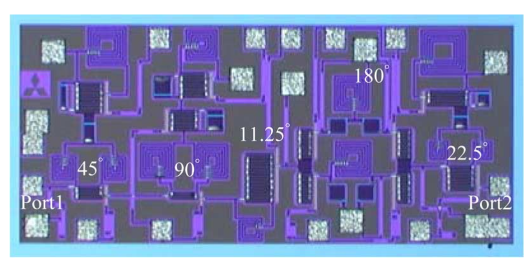

Fig. 8. Photograph of the S-band 5-bit MMIC phase shifter.

Generally, the capacitance value per unit area of the metal–insulator–metal (MIM) capacitor is much higher than that of the FET's off-state capacitance. The improved circuit should be employed for the large phase-shift circuit ($\phi_0 \cong 90°$) in the view of size reduction.

IV. Measurement Results

S- and C-band ultra-compact MMIC phase shifters are shown. The integrated circuits are fabricated by using 0.5-μm pseudomorphic HEMT (pHEMT) technology with a 0.1-mm-thick GaAs substrate and high-Q inductors ($Q = 15$–20). Simulation data shown here are obtained

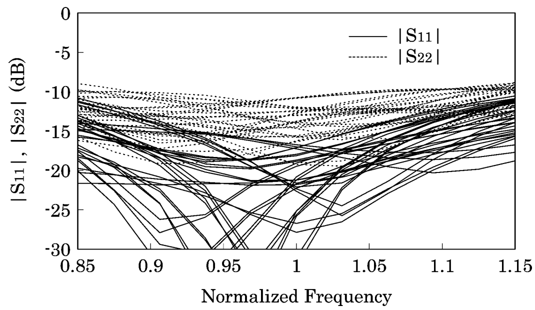

Fig. 9. Measured input and output reflection amplitude in all 32 phase states.

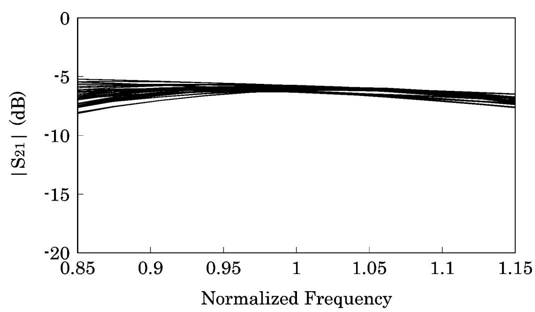

Fig. 10. Measured transmission amplitude in all 32 phase states.

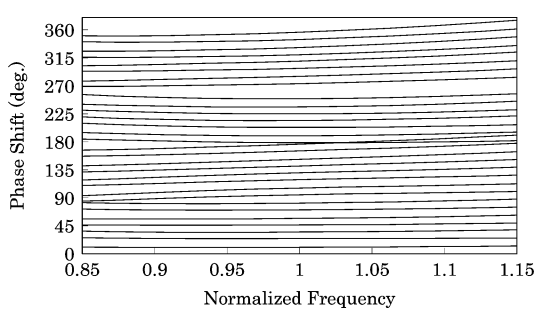

Fig. 11. Measured phase shift in all 32 phase states.

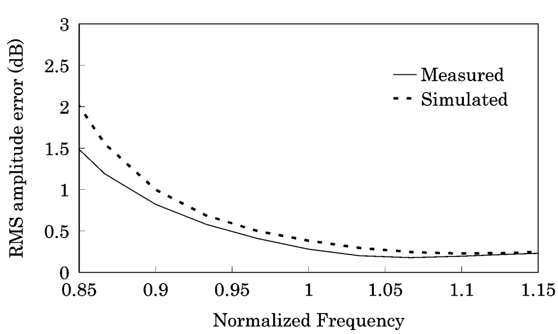

Fig. 12. RMS amplitude error.

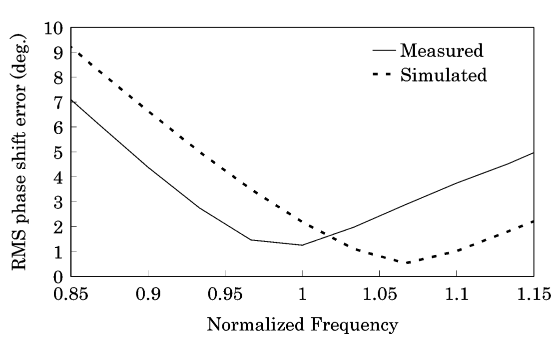

Fig. 13. RMS phase shift error.

TABLE I
SUMMARY OF THE MEASURED RESULTS OF THE S-BAND 5-bit MMIC PHASE SHIFTER

Parameter	Value
Frequency	S-band
Fractional Bandwidth	10%
Max. Input Return Loss	13.8dB
Max. Output Return Loss	10dB
Max. Insertion Loss	6.7dB
Average Insertion Loss	6.1dB
RMS Amplitude Error	0.58dB
RMS Phase Error	2.8°
Chip Size	1.63mm^2

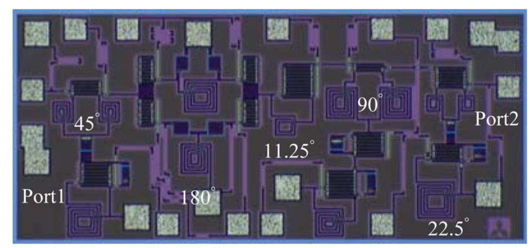

Fig. 14. Photograph of the C-band 5-bit MMIC phase shifter.

by using commercial simulation tools. FETs are modeled by the lumped-element equivalent circuit, while the peripheries employed in the phase shifters are 0.2-1 mm.

A. S-Band Ultra-Compact 5-bit Phase Shifter

Fig. 8 shows a photograph of the fabricated S-band 5-bit GaAs MMIC phase shifter. The chip size is 1.87 mm $\times$ 0.87 mm (1.63 mm^2). The 90° bit employs the proposed improved phase-shifting circuit based on the all-pass network, while the 45° and 25° bits employ the proposed circuit based on the all-pass network. The 180° bit is constructed using the switched high-pass/low-pass topology [1] and the 11.25° bit is realized by the matched embedded FET phase-shifting circuit [9]. The measured characteristics of the phase shifter in all 32 phase states are shown in Figs. 9–11 with a control voltage of -5 V. The measured input and output return losses were 13.8 and 10 dB in the worst case, respectively, over a fractional bandwidth of 10% in the S-band. The insertion loss was 6.1 dB $\pm$ 0.6 dB over the same frequency range. The rms amplitude error was 0.58 dB and the rms phase error was 2.8° in the operating frequency, as shown in Figs. 12 and 13. Table I shows the typical measured results of the S-band 5-bit MMIC phase shifter.

B. C-Band Ultra-Compact 5-bit Phase Shifter

Fig. 14 shows a photograph of the fabricated C-band 5-bit GaAs MMIC phase shifter [8]. The chip size is 1.72 mm $\times$ 0.81 mm (1.37 mm^2). The 90° bit employs the proposed improved phase-shifting circuit based on the all-pass network, while the 45° and 25° bits employ the proposed circuit based on the all-pass network. The 180° bit is constructed using the switched high-pass/low-pass topology [1]; the 11.25° bit is realized by the matched embedded FET phase-shifting circuit [9]. The measured characteristics of the phase shifter in all 32 phase states are shown in Figs. 15–17 with a control voltage of -5 V. The measured input and output return losses

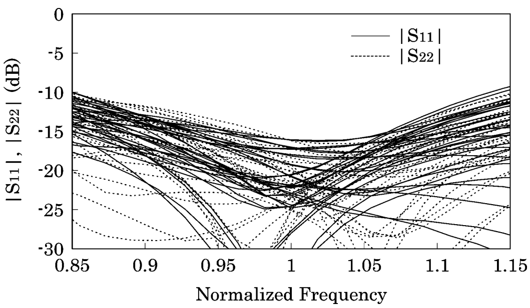

Fig. 15. Measured input and output reflection amplitude in all 32 phase states.

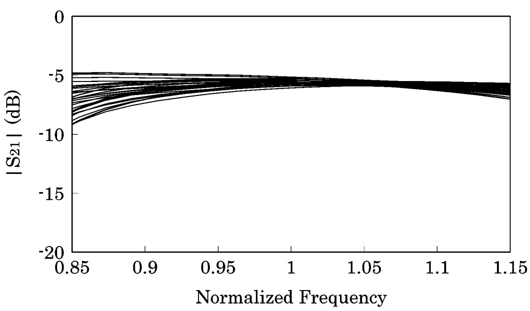

Fig. 16. Measured transmission amplitude in all 32 phase states.

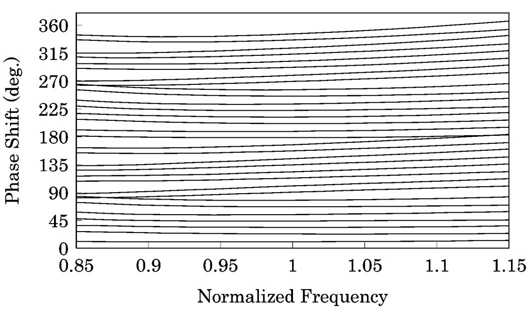

Fig. 17. Measured phase shift in all 32 phase states.

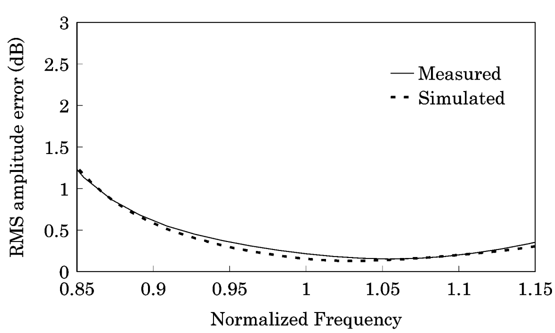

Fig. 18. RMS amplitude error.

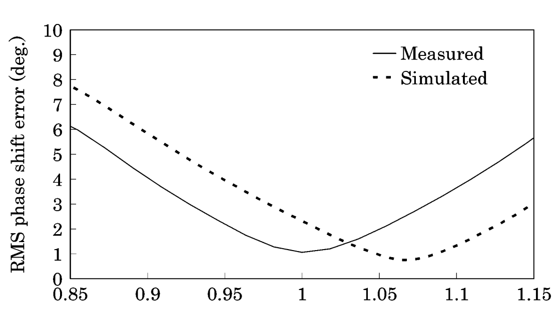

Fig. 19. RMS phase-shift error.

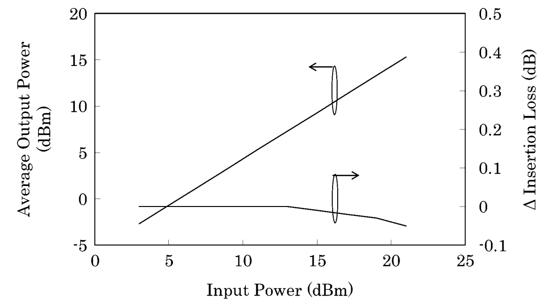

Fig. 20. Measured average output power and variation of insertion loss against input power in all 32 phase states.

TABLE II
SUMMARY OF THE MEASURED RESULTS OF THE C-BAND 5-bit MMIC PHASE SHIFTER

Parameter	Value
Frequency	C-band
Fractional Bandwidth	10%
Max. Input Return Loss	14.5dB
Max. Output Return Loss	13.5dB
Max. Insertion Loss	6.5dB
Average Insertion Loss	5.7dB
RMS Amplitude Error	0.37dB
RMS Phase Error	2.3°
1-dB Compression Level	> 21dBm
Chip Size	1.37mm^2

TABLE III
COMPARISON OF COMPACT MMIC PHASE SHIFTERS

Ref.	Number of Bits	Frequency Band	Band width	RMS Phase Error	Chip Size
[3]	4	X	8%		1.3mm^2
[4]	5	K	21%	< 3°	1.3mm^2
[5]	5	Ku	16%	< 3.7°	1.25mm^2
[6]	4	L	53%	< 3°	2.6mm^2
[6]	4	S	50%	< 3°	2.6mm^2
This	5	S	10%	< 2.8°	1.63mm^2
Work	5	C	10%	< 2.3°	1.37mm^2

were 14.5 and 13.5 dB in the worst case, respectively, over a fractional bandwidth of 10% in the C-band. The insertion loss was 5.7 dB $\pm$ 0.8 dB over the same frequency range. The rms amplitude error was 0.37 dB and the rms phase error was 2.3° in the operating frequency, as shown in Figs. 18 and 19. The average output power in all 32 phase states is shown in Fig. 20. The 1-dB compression level (P1 dB) was much greater than 21 dBm. It is assumed then that the third-order input intercept point (IIP3) is greater than 31 dBm [10]. Table II shows the typical measured results of the C-band 5-bit MMIC phase shifter.

Table III shows a comparison of compact MMIC phase shifters. This study achieved a comparable small chip size with [3]–[5] in spite of lower frequency operation.

V. CONCLUSION

The design techniques of ultra-compact phase-shifting circuits utilizing an all-pass network topology have been developed. The circuit topology can achieve low amplitude error and elimination of unwanted resonance in a conventional circuit.

It has shown that the all-pass network enables us to design the phase shifter with small size by the fact that the transition frequency of the all-pass network can be higher than the operating frequency. The excellent performance of the fabricated MMIC phase shifters for S- and C-band, with a chip size of 1.87 mm $\times$ 0.87 mm (1.63 mm^2) and 1.72 mm $\times$ 0.81 mm (1.37 mm^2), respectively, have shown that the proposed design techniques are useful for low-cost phased-array applications.

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