Switchless Class-G Power Amplifiers: Generic Theory and Design Methodology Using Packaged Transistors

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***Abstract*—This paper develops a complete theory of the Switchless Class-G (SLCG) PA and proposes a new design method that allows for operating commercial packaged transistors in high-efficiency SLCG mode over a wide frequency band. It starts with a comprehensive analysis that investigates the impact of various transistor and circuit parameters on the SLCG PA's key performances. Then, design equations are derived to produce SLCG prototypes with optimal back-off efficiency and gain flatness. Moreover, to overcome the difficulty of applying classical SLCG circuits to packaged devices, a new SLCG output combining network is developed to absorb various transistors and package parasitic while maintaining the load conditions that enable the wideband SLCG operation. This expands the applicable scope of the SLCG technique and yields packaged-transistor-based, wideband, and high-efficiency SLCG PAs. For validation, a 1-3GHz SLCG PA is designed using the proposed method with commercial packaged transistors. Measurements under continuous-wave excitations reveal that, over 1-3GHz, the proposed SLCG PA can provide saturation output power (P_{sat}) of 36.5-38.7dBm and deliver drain efficiency (DE) of 39.2-49.1%, 45.4-51.2%, and 47.8-57.7% at power levels that are 7.5dB, 6dB and 0dB back-off from P_{sat}, respectively. Moreover, when excited by a 40MHz 64-QAM modulated signal over 1-3 GHz, the PA realizes an average DE of 39-49.2% at an average output power of 28.8-31.6dBm, and maintains an error vector magnitude of about 1.2% and adjacent channel power ratio of below -46dBc after digital pre-distortion.**

***Index Terms*—Broadband, switchless class-G power amplifier, GaN, high efficiency, packaged transistor.**

I. INTRODUCTION

The endless pursuit of high-speed wireless data rate drives modern communication systems to employ new standards with spectrum-efficient modulation schemes at various continuous or non-contiguous frequency bands [1]-[2]. This requires the base station power amplifier (PA) to support efficient amplification of signals with high peak-to-average power ratio (PAPR) over broad frequency bands [3].

As traditional Class-AB PAs can only maintain high efficiency around peak powers, it is compulsory for the base station PAs to adopt back-off efficiency enhancement (BEE) techniques which boost the average PA efficiency under high PAPR signals [4]. As the most adopted BEE technique, the Doherty power amplifier (DPA) [5]-[8] is popular due to its various merits, such as simple circuitry, RF-in-RF-out feature, excellent 6dB back-off efficiency, and moderate linearity. However, to achieve proper load modulation between the two sub-PAs, the DPA involves the quarter-wave transmission line (TL) which intrinsically limits its bandwidth. Although many attempts have been made to mitigate this problem by innovating the DPA's output combiner network or its input driving conditions [9]-[13], these techniques are still bound by the narrowband nature of the impedance inversion. Especially when dealing with signals of high PAPR of >6dB, the DPA needs to apply an enlarged impedance inversion ratio, which further reduces the available PA bandwidth [14]. Recently, new BEE techniques, such as Distributed Efficient Power Amplifier (DEPA) [15]-[16] and Load Modulated Balanced Amplifier (LMBA) [17]-[19] have been developed to boost back-off efficiency over wide operation bandwidth. However, both techniques require the corporation of more than two sub-PAs and additional combining networks, such as couplers or multi-stage distributed networks. This necessitates the phase and amplitude alignments among multi-path over wideband as well as bulky combiners with enlarged size and loss, which undoubtedly leads to higher design complexity compared to the 2-way PAs.

The switchless Class-G (SLCG) PA is a recently developed BEE technique [20]. Similar to the DPA, it adopts a very simple 2-way structure that utilizes a Class-AB biased main PA and a Class-C biased auxiliary PA. Different from the DPA, these two sub-PAs are biased under very distinctive DC drain supply voltages. This allows the main transistor to be gradually modulated from the 1st quadrant to the 3rd quadrant when the auxiliary transistor current increases from 0 (e.g. at cut-off state) in the low-power region (LPR) to large levels in the high-power region (HPR). This two-quadrant-modulation (TQM) [20] brings the following advantages: firstly, the 3rd-quadrant-operated main transistor behaves more like a load impedance instead of an active device, as it no longer delivers current to the outside but draws current inside. Therefore, the TQM helps to softly switch the power source from the main transistor to the auxiliary one when the PA operates through LPR to HPR without involving a hardware switch. This avoids the linearity issue in the conventional Class-G PA [21]-[22] due to the abrupt changes in

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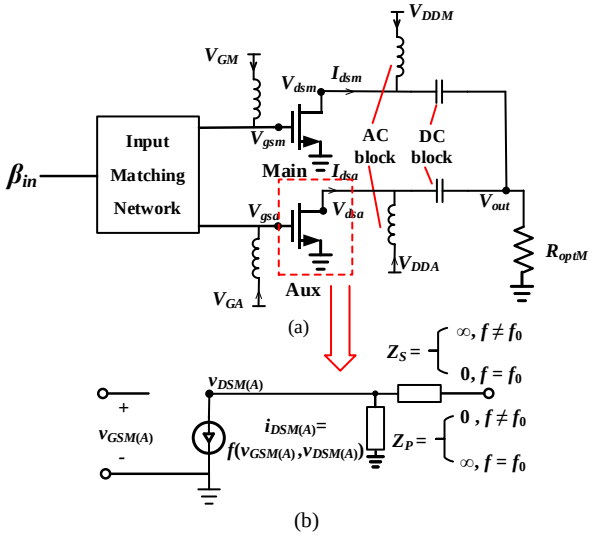


Fig. 1. Diagrams of (a) the classic SLCG circuit; and (b) transistor modeling with all harmonic impedances shorted

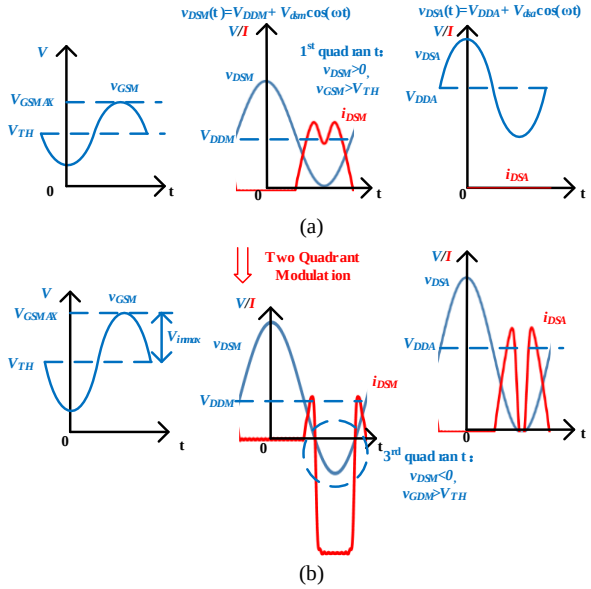


Fig. 2. Voltage and current waveforms of the main and auxiliary transistors and illustration of TQM: (a) OBO; (b) Saturation.

gain and efficiency characteristics brought by the hard switching. Secondly, since the output power (P_{out}) delivered by SLCG PA in the HPR is entirely contributed by the auxiliary PA, henceforth the load modulation of the main transistor is no longer the top factor limiting the PA back-off efficiency and bandwidth.

The above benefits make the SLCG PA an attractive solution for realizing enhanced back-off efficiency over wideband. However, ref. [20] mainly focuses on discussing the concept of TQM, e.g. the variation of transistor characteristics during the shift from the 1st quadrant to the 3rd quadrant, and lacks the analysis of the overall SLCG circuit model. Moreover, the SLCG circuit reported in [20] requires the internal current source (CS) plane drain nodes of the main and auxiliary transistors to be AC-connected. This is difficult to fulfill for commercial packaged transistors, as such transistors usually exhibit non-negligible package parasitic inductance and capacitance which at RF frequency make the drain voltage at the external package plane significantly different from the transistor internal plane. This issue limits the applicable range of the SLCG PA proposed in [20].

This paper contributes in the following aspects: firstly, it presents a generic theory of the SLCG PA. A comprehensive analysis is given to systematically explain how the various SLCG design parameters, such as bias voltage, device periphery, load impedance, and input driving conditions, affect the key performances of the SLCG PA, e.g. the Output Back-off (OBO), efficiency, P_{out}, and gain. Through this analysis, design equations are derived to yield SLCG prototypes with optimal AM-AM characteristics. Secondly, to make the SLCG technique applicable to commercial packaged devices, this paper proposes a new SLCG output combining network (OCN) that uses 0° impedance transformers to perform impedance transformation as well as absorb the various transistor and package parasitic parameters, consequently enabling packaged-device-based, wideband and high-efficiency SLCG PAs. For validation, the proposed method is applied to design a 1-3GHz wideband SLCG PA using commercial packaged transistors CGH40006P and CG2H40010F from the Wolfspeed Inc. Measurements under Continuous Wave (CW) excitation reveals that, over 1-3GHz, the proposed SLCG PA can deliver saturation P_{out} (P_{sat}) of 36.5-38.7 dBm and maintains drain efficiency (DE) of 39.2-49.1%, 45.4-51.2% and 47.8-57.7% at 7.5dB, 6dB and 0dB back-off from P_{sat}. Moreover, when excited with a 40MHz 64-QAM signal with a PAPR of 7.5dB, the proposed PA achieves an average DE of 39-49.2% at an average P_{out} of 28.8-31.6 dBm, and maintains an error vector magnitude (EVM) of about 1.2% and an adjacent channel power ratio (ACPR) of <-46dBc after applying digital pre-distortion (DPD).

II. Theory And Proposed Design Method Of SLCG PA

A. SLCG Basis and the Transistor and Input Condition Modeling

Fig. 1(a) shows the classic SLCG circuit reported in [20], where a DC block capacitor is used to connect the main and auxiliary transistors so that these two transistors can be biased at different DC supply voltages (V_{DDM} and V_{DDA}, $V_{DDM}<V_{DDA}$), while their drain voltage AC components can be considered exactly identical ($v_{dsm}=v_{dsa}$). It is worth noting that, for the variable nomenclature, this analysis uses symbols of uppercase letters with uppercase subscripts to denote DC variables, lowercase letters with lowercase subscripts for AC variables, lowercase letters with uppercase subscripts for the superposed DC and AC variables, uppercase letters and lowercase subscripts for frequency domain components obtained from Fourier transform. For instance, as depicted in Fig. 2, the time-domain main transistor drain voltage is denoted as v_{DSM}, which exhibits a DC, AC, and fundamental component of V_{DDM}, v_{dsm}, and V_{dsm}, respectively.

The SLCG PA and DPA operation is partially similar in the LPR, where the auxiliary transistor is turned off and only the main transistor is conducting. Henceforth, the value of the load impedance in Fig. 1(a) is set to the optimal load (R_{optM}) of the main transistor, so that an efficiency peak is attained at a certain OBO power for average efficiency enhancement [Fig. 2(a)].

The SLCG PA behaves very differently from DPA when the auxiliary transistor turns on in the HPR. As v_{dsm} is forced identical to v_{dsa}, the increase of v_{dsa} can yield v_{dsm} with

amplitude higher than V_{DDM}, thus the drain voltage of the main transistor will swing below 0. This pushes the main transistor to be modulated from the 1st quadrant ($v_{DSM}>0$, $v_{GSM}>V_{TH}$) to the 3rd quadrant ($v_{DSM}<0$, $v_{GDM}>V_{TH}$), which is also known as TQM. This phenomenon is shown in Fig. 2(b). Due to the large signal nature of TQM, when analyzing the SLCG PA, the main transistor cannot be considered an ideal voltage-controlled CS, and it is compulsory to consider the effects of both gate and drain voltages. In this analysis, the equations used in [20] are applied to model the transistors:

$$i_{DS}(v_{GS},v_{DS})=\begin{cases} I_{MAXM(A)}\psi(v_{GS})\tanh(0.74\cdot\frac{v_{DS}}{V_{KNEE}}), v_{DS}\geq 0 \\ I_{MAXM(A)}\psi(v_{GS}-v_{DS})\tanh(0.74\cdot\frac{v_{DS}}{V_{KNEE}}), v_{DS}\leq 0 \end{cases} \quad (1)$$

$$\psi(x)=\begin{cases} 1, x>1 \\ x, 0\leq x\leq 1 \\ 0, x<0 \end{cases} \quad (2)$$

Where I_{MAXM} and I_{MAXA} stand for the maximum drain currents of the main and auxiliary transistors, respectively, and V_{KNEE} is the knee voltage. Note that this model can be viewed as the multiplication of two factors: (i) the hyperbolic tangent function which models the effect of v_{DS} on i_{DS} [23]; and (ii) the step function $\varphi(x)$ which describes the effect of gate voltage on i_{DS} and eventually enables the analysis of transistor operation over both the 1st and 3rd quadrants.

To form a proper TQM, it is required that the input signals of the main and auxiliary paths are judiciously synchronized. This is very similar to the input requirements in DPA, so it is natural to borrow input models that are commonly used in DPA analysis. These models include the AB-C model [24] and the dual Class-B model [25]. Compared with the AB-C model, the dual Class-B model is relatively simple as it eliminates the cumbersome conduction angle analysis. This allows for a quick evaluation of key circuit performances. Therefore, in this theoretical study, both transistors are assumed to be operated in Class-B mode, and their fundamental gate voltages (V_{gsm} and V_{gsa}) are expressed as:

$$V_{gsm}=\beta_{in}\cdot V_{in\max} \qquad 0\leq\beta_{in}\leq 1 \quad (3)$$

$$V_{gsa}=\begin{cases} 0 & 0\leq\beta_{in}\leq\beta \\ \frac{\beta_{in}-\beta}{1-\beta}e^{j\theta_{\Delta}}V_{in\max} & \beta\leq\beta_{in}\leq 1 \end{cases} \quad (4)$$

Where V_{inmax} denotes the maximum fundamental input voltage of the transistor, and β_{in} is a unitless normalized input parameter that is between [0,1], and β is the value of β_{in} when the auxiliary transistor is turned on, and θ_{Δ} is the phase difference between the main and auxiliary input voltage. For the classical SLCG circuit, θ_{Δ} is equal to 0.

B. The Analysis of the Classical SLCG PA

In this part, a comprehensive analysis of the classical SLCG circuit is performed to obtain the relationship between the SLCG circuit parameters and its key performances. A set of design equations yielding the optimal gain flatness is then derived and verified.

This analysis starts with discussing the characteristics of the main transistor in the LPR, where its drain voltage is usually much higher than V_{KNEE} ($v_{DS}>>V_{KNEE}$). Therefore, the hyperbolic tangent function in (1) is approximately equal to 1, and equation (1) can be degenerated to a basic voltage-controlled current-source relationship. Consequently, under the Class-B bias assumption, the fundamental drain current of the main transistor (I_{dsm}) can be expressed as a linear function of the input voltage:

$$I_{dsm}=\frac{1}{2}\beta_{in}\cdot I_{MAXM} \quad (5)$$

The output voltage of the SLCG PA (V_{out}) can then be expressed as:

$$V_{out}=V_{dsm}=\frac{1}{2}\beta_{in}\cdot I_{MAXM}\cdot R_{optM} \quad (6)$$

The amplifier gain ($\mathrm{Gain_{OBO}}$) at OBO can be viewed as the ratio between V_{out} and V_{gsm}. Based on (5)-(6), $\mathrm{Gain_{OBO}}$ and the value of I_{dsm} at the OBO ($\beta_{in}=\beta$) takes the following form:

$$Gain_{OBO}=\left.\frac{V_{out}}{V_{gsm}}\right|_{OBO}=\frac{1}{2}\frac{I_{MAXM}\cdot R_{optM}}{V_{in\max}} \quad (7)$$

$$I_{dsm,obo}=\frac{1}{2}\beta\cdot I_{MAXM} \quad (8)$$

For the main transistor to achieve an efficiency peak at the OBO power, its fundamental drain voltage should reach V_{DDM}-V_{KNEE} which is considered as the maximum swing allowed without compressing the device. Therefore, the main transistor current and voltage and the SLCG $\mathrm{P_{out}}$ ($\mathrm{P_{obo}}$) at OBO should satisfy:

$$V_{DDM}-V_{KNEE}=R_{optM}\cdot\frac{1}{2}\beta\cdot I_{MAXM} \quad (9)$$

$$P_{obo}=\frac{1}{2}\frac{(V_{DDM}-V_{KNEE})^2}{R_{optM}} \quad (10)$$

At the saturation power, the auxiliary transistor is fully turned on. Consequently, as identified in Fig. 2(b), the main transistor is forced to operate in the 3rd quadrant for a considerable portion of a cycle. This generates a large amount of current flowing into the main transistor. Therefore, the main transistor absorbs fundamental power instead of delivering it to the outside, and consequently, it can be equivalent to a load impedance at the fundamental frequency. Denote this impedance as $Z_{LM,sat}$, and consequently, the auxiliary transistor sees an impedance of $Z_{LM,sat}//R_{optM}$. Meanwhile, according to (1) and (2), the fundamental drain current (I_{dsa}) of the auxiliary transistor is equal to $I_{MAXA}/2$ at saturation. Therefore, the auxiliary transistor drain voltage at saturation ($V_{dsa,sat}$), which is also the saturation SLCG output voltage, can be written as:

$$V_{out}\big|_{SAT}=V_{dsa,sat}=(Z_{LM,sat}//R_{optM})\cdot\frac{1}{2}I_{MAXA} \quad (11)$$

To maximize the $\mathrm{P_{out}}$ and efficiency of the auxiliary PA while avoiding compression, this voltage should meet the following conditions:

$$V_{dsa,sat}=V_{DDA}-V_{KNEE} \quad (12)$$

According to (11) and (12), the auxiliary transistor optimal load and the SLCG $\mathrm{P_{sat}}$ can be expressed as:

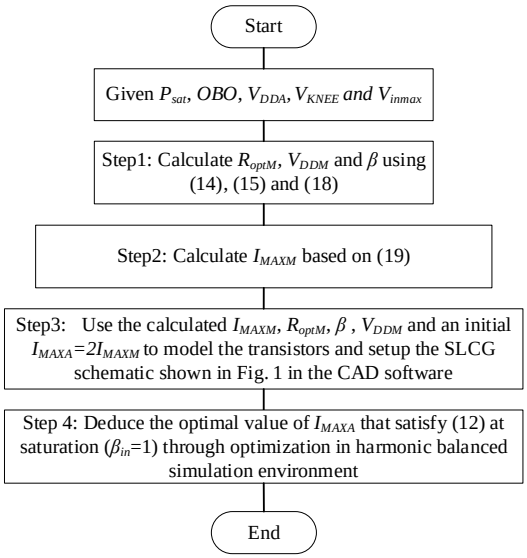


Fig. 3. Flow chart to solve the value of I_{MAXA} that maximizes the auxiliary transistor power and efficiency at saturation.

$$R_{optA} = 2\frac{(V_{DDA} - V_{KNEE})}{I_{MAXA}} = Z_{LM,sat} // R_{optM} \tag{13}$$

$$P_{sat} = \frac{1}{2}\frac{(V_{DDA} - V_{KNEE})^2}{R_{optM}} \tag{14}$$

Combining (10)-(11) and (13)-(14), the realized OBO and saturation gain of the SLCG PA can be written as:

$$\text{OBO} = \frac{P_{sat}}{P_{obo}} = \frac{(V_{DDA} - V_{KNEE})^2}{(V_{DDM} - V_{KNEE})^2} \tag{15}$$

$$Gain_{SAT} = \left.\frac{V_{out}}{V_{gsm}}\right|_{SAT} = \frac{1}{2}\frac{I_{MAXA}R_{optA}}{V_{in\max}} \tag{16}$$

Note that the OBO calculated from (15) is in the linear scale. An additional logarithm operator is required to transform it into the dB scale. Defining AM-AM$_{obo}$ as the ratio of Gain$_{OBO}$ to Gain$_{SAT}$. According to (7) and (16), we have:

$$AM - AM_{obo} = \frac{Gain_{OBO}}{Gain_{SAT}} = \frac{I_{MAXM}\cdot R_{optM}}{I_{MAXA}\cdot R_{optA}} = \frac{V_{DDM} - V_{KNEE}}{\beta(V_{DDA} - V_{KNEE})} \tag{17}$$

To reduce the SLCG gain variation in the HPR, we expect AM-AM$_{obo}$ = 1. Combined with equations (15) and (17), this asks β to satisfy the below equation:

$$\beta = \frac{V_{DDM} - V_{KNEE}}{V_{DDA} - V_{KNEE}} = \sqrt{\frac{1}{OBO}} \tag{18}$$

Furthermore, substitute (18) into (9), I_{MAXM} can be expressed as (19). This equation identifies the value of I_{MAXM} for optimal gain flatness and maximized P$_{sat}$. Note that this value is determined by V_{DDA} (not V_{DDM}), and is independent of OBO.

$$I_{MAXM} = \frac{2(V_{DDA} - V_{KNEE})}{R_{optM}} \tag{19}$$

Up to now, various design parameters have been obtained by targeting optimal PA power efficiency and gain flatness. However, it is worth noting that equations (13)-(19) are derived by assuming that the auxiliary transistor delivers optimal power and efficiency at saturation. This requires the satisfaction of (12) which further demands a proper $Z_{LM,sat}$ to be presented by the 3rd-quadrant-operated main transistor. According to [20], the value of $Z_{LM,sat}$ is greatly dependent on the injection current from the auxiliary transistor. This makes it possible to obtain optimal auxiliary transistor power efficiency by properly selecting the value of I_{MAXA} which affects the injection current and eventually controls $Z_{LM,sat}$. However, due to the nonlinear characteristic of the 3rd-quadrant-operated main transistor, the optimal I_{MAXA} that yields the satisfaction of (12) must be determined from large-signal simulations.

TABLE I
SLCG PARAMETERS UNDER VARIOUS OBO

Circuit parameters					
OBO(dB)	β	V_{DDM}(V)	R_{optM}(Ω)	I_{maxM}(A)	I_{maxA}(A)
6	0.50	14.78	55.65	0.95	2.10
7	0.45	13.34	55.65	0.95	2.18
8	0.40	12.05	55.65	0.95	2.22

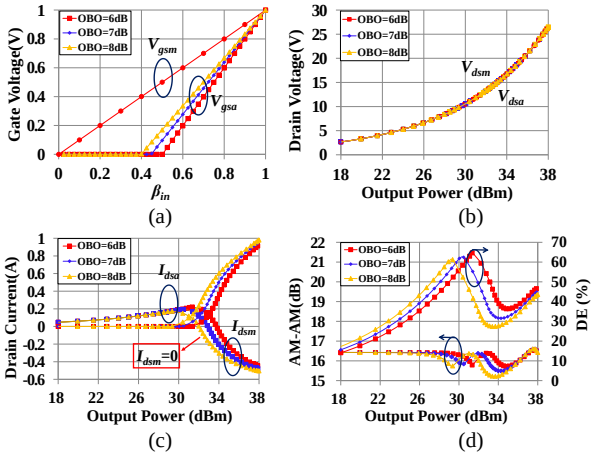


Fig. 4. HB simulation results under different OBO: (a) gate voltages; (b) drain voltages; (c) drain currents; (d) DE and AM-AM.

Fig. 3 shows the flow chart utilized to solve the optimal I_{MAXA}. Based on Fig. 3, for a given set of OBO, P$_{sat}$, V_{DDA}, V_{KNEE}, and V_{inmax} using (14), (15), and (18), R_{optM}, V_{DDM}, and β can be obtained, and subsequently, I_{MAXM} is calculated using (19). Then, using these parameters and setting an initial I_{MAXA} to twice I_{MAXM}, the main and auxiliary transistor can be built using (1)-(2), and subsequently the SLCG PA circuit shown in Fig. 1(a) is established and simulated with a harmonic balance (HB) simulator. In the next, the value of I_{MAXA} is optimized so that the maximum output power condition shown in (12) is satisfied at β_{in}=1. This produces the correct value of I_{MAXA}.

Moreover, non-zero harmonic components complicate the analysis. Therefore, as shown in Fig. 1(b), when modeling the transistors, an L-shape network is involved to short-circuit all harmonic drain voltages. For this purpose, its parallel/series impedance is defined as equal to $\infty/0$ and $0/\infty$ at the fundamental and harmonic frequencies, respectively. Henceforth, all the harmonic components of transistor drain

voltages are set to zero, and only the DC and fundamental ones are retained. This helps with a quick evaluation of the theoretical performance of the SLCG PA.

Table I shows the circuit parameters (β, V_{DDM}, R_{optM}, I_{MAXM}, I_{MAXA}) obtained by applying Fig. 3 under various OBO values while setting P_{sat}, V_{DDA}, V_{KNEE}, V_{inmax}, and θ_Δ to 38dBm, 28V, 1.5V, 1V and 0°, respectively. Fig. 4 shows the HB simulation results of various SLCG circuits built using the parameters summarized in Table I.

According to Fig. 4(a), different values of OBO require V_{gsa} to increase at different rates, but in general, this rate difference is not significant. In addition, it can be seen from Table I that both I_{MAXM} and I_{MAXA} vary little with OBO. This means that the SLCG PA can present different OBO characteristics simply by adjusting V_{DDM} and β (bias conditions) without changing transistors and other circuit parameters. This reconfigurable feature improves the robustness of the SLCG PA to the inaccuracy issues of the transistor's large-signal model in predicting its 3rd quadrant behavior. According to Fig. 4(b), V_{dsm} and V_{dsa} remain identical for all OBO and reach V_{DDA}-V_{KNEE} (26.5V) at saturation. This verifies the maximization of the auxiliary transistor power efficiency at P_{sat}. Moreover, Fig. 4(c) shows that the variation of target OBO has a strong effect on the current profiles. For instance, the increase of OBO yields the decrease of β, and thus forces the auxiliary transistor to turn on at lower β_{in}, and causes the main transistor to quickly behave as a load impedance, i.e., lower β_{in} for I_{dsm}<0 [see Fig. 4(c)]. As shown in Fig. 4(d), this brings more power consumption and leads to lower efficiency in the HPR region under large OBO. Meanwhile, for all OBO cases, the gain value at the OBO and saturation power are identical.

Finally, it is worth noting that the optimal gain flatness condition revealed in (18) is derived under dual Class-B and zero-transistor-parasitic assumptions. Therefore, it is merely used to simplify the prototype design and point out the possibility of realizing high-performance SLCG PAs. In the practical design, due to the input parasitic of the transistor, it is necessary to take into account various parameters, such as the transistor input impedance, the input matching network design, power divider selection, and bias conditions, to enhance the efficiency and gain characteristic of the real SLCG PAs.

C. The Proposed SLCG PA Enabling the Packaged-transistor-based Implementation

The classic SLCG circuit requires the internal AC drain voltages of the two transistors to be identical. This is difficult to achieve for commercial packaged transistors as these transistors usually exhibit substantial parasitic inductance and capacitance which make the package plane drain voltage significantly different from the internal one. As a result, even if the devices are directly connected, their internal voltages differ from each other greatly. Therefore, it is difficult to apply the classic SLCG technique to commercial packaged transistors.

To mitigate this problem, this work proposes a new SLCG output combining network (OCN) which adopts matching networks (OMN_M and OMN_A) in both main and auxiliary branches [see Fig. 5(a)]. These matching networks are deliberately constructed based on the following criterion:

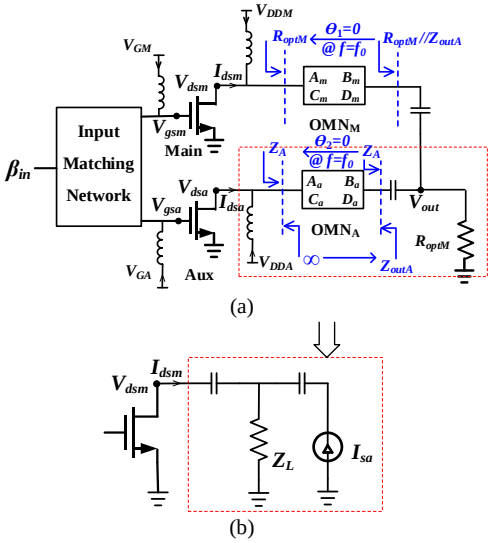


Fig. 5. Diagrams of: (a) the proposed SLCG PA and (b) its equivalent circuit in the HPR.

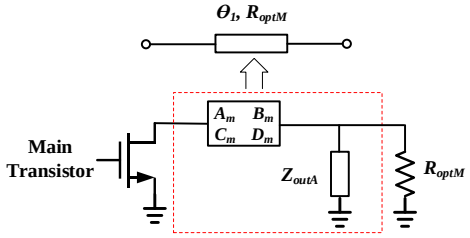


Fig. 6. Equivalent circuit of the proposed SLCG PA in the LPR.

firstly, both networks are wideband impedance transformers that fulfill specific load transformation targets required in Fig. 5(a), and at the center frequency (f_0) they are equivalent to ideal voltage transformers with a phase shift of 0° and a voltage ratio of 1:1, so that the entire network is equivalent to the classical SLCG circuit at f_0. Therefore, the method given in the previous part for device selection and circuit parameter computation can be directly applied. Secondly, these networks are assumed to exhibit positive group delays, so that transistor and package parasitic parameters can be absorbed as part of the networks.

Using the above criterion, the OMN_A is firstly modeled as an artificial TL with a characteristic impedance of Z_A, an electrical length of θ_2, a constant group delay of τ_A, and its ABCD-Parameter takes the following form:

$$\begin{bmatrix} A_a & B_a \\ C_a & D_a \end{bmatrix} = \begin{bmatrix} \cos\theta_2 & jZ_A\sin\theta_2 \\ j\dfrac{1}{Z_A}\sin\theta_2 & \cos\theta_2 \end{bmatrix} \tag{20}$$

$$\theta_2 = (f - f_0)\tau_A \tag{21}$$

Define γ as the normalized characteristic impedance of OMN_A with respect to R_{optA}:

$$\gamma = \frac{Z_A}{R_{optA}} \tag{22}$$

In the LPR, the auxiliary transistor is turned off, so that the proposed SLCG circuit can be simplified to the one shown in Fig. 6, where Z_{outA} is the output impedance of the auxiliary branch. Using (20), Z_{outA} can be expressed as:

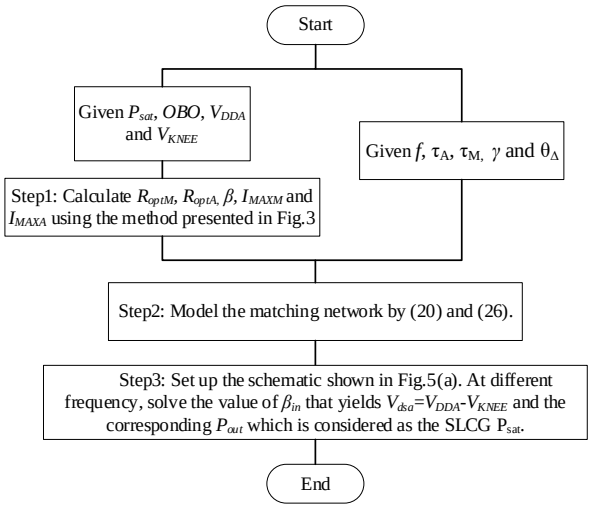


Fig. 7. Simulation flowchart used to determine the saturation input voltage and output power at various frequency points.

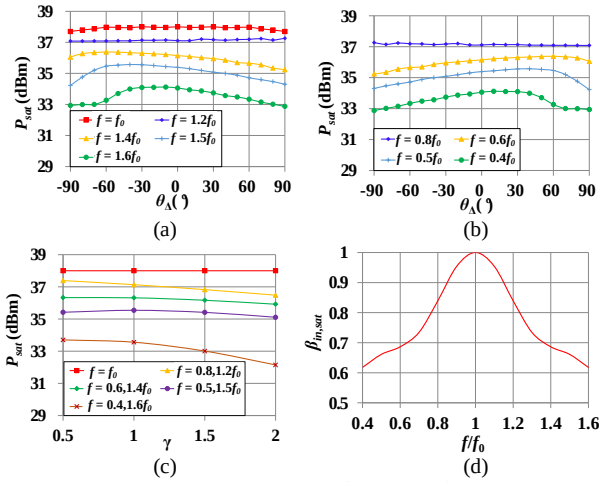


Fig. 8. HB simulation results using the flowchart of Fig. 7: (a)-(b) P_{sat} vs. θ_Δ for various frequencies and γ=1; (c) P_{sat} vs. γ for various frequencies under $\theta_\Delta=\theta_2-\theta_1$. (d) $\beta_{in,sat}$ vs. freq. under $\theta_\Delta=\theta_2-\theta_1$ and γ=1.

$$Z_{outA} = jZ_A \tan\theta_2 \tag{23}$$

To maintain good back-off efficiency over wideband, the main transistor should see R_{optM} over a broad frequency range in the LPR. Therefore, as shown in Fig. 6, the combination of OMN_M and the parallel Z_{outA} should be equivalent to another artificial TL with a characteristic impedance of R_{optM}, an electrical length of θ_1, and a group delay of τ_M. Using the network theory, this equivalence can be expressed as:

$$\begin{bmatrix} \cos\theta_1 & jR_{opt}\sin\theta_1 \\ j\dfrac{1}{R_{opt}}\sin\theta_1 & \cos\theta_1 \end{bmatrix} = \begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 1/Z_{outA} & 1 \end{bmatrix} \tag{24}$$

$$\theta_1 = (f - f_0)\tau_M \tag{25}$$

Note that both θ_1 and θ_2 from (25) and (21) are modeled to exhibit constant group delay and their value is equal to 0 at f_0. Subsequently, the ABCD-Parameters of OMN_M can be solved from (24) and expressed as follows:

$$\begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix} = \begin{bmatrix} \cos\theta_1 - j\dfrac{R_{optM}}{Z_{outA}}\sin\theta_1 & jR_{optM}\sin\theta_1 \\ j\dfrac{\sin\theta_1}{R_{optM}} - \dfrac{\cos\theta_1}{Z_{outA}} & \cos\theta_1 \end{bmatrix} \tag{26}$$

The application of (20) and (26) finishes the construction of the proposed SLCG PA. Before examining its characteristics, a brief discussion is given below to explain the relationship between the proposed SLCG circuit and the classic one. Using (20) and (26), and by treating the proposed SLCG network as a lossy two-port network, its Z-parameters can be derived:

$$\begin{bmatrix} V_{dsm} \\ V_{dsa} \end{bmatrix} = \begin{bmatrix} R_{optM} & \dfrac{e^{-j\theta_1}R_{optM}}{\cos\theta_2} \\ \dfrac{e^{-j\theta_1}R_{optM}}{\cos\theta_2} & \dfrac{R_{optM}\left(1+\tan^2\theta_2\right)}{j\tan\theta_1+1} + j\tan\theta_2 Z_A \end{bmatrix}\begin{bmatrix} I_{dsm} \\ I_{dsa} \end{bmatrix} \tag{27}$$

Moreover, it is worth noting that the auxiliary transistor does not enter the 3rd quadrant throughout the whole SLCG operation. Therefore, its behavior can be simplified as a linear voltage-controlled CS, and consequently, Norton equivalence can be performed to deduce an equivalent circuit of the components inside the red box of Fig. 5(a). Fig. 5(b) depicts the resulting circuit after Norton equivalence, where Z_L and I_{sa} denote the equivalent output impedance and short-circuit CS. Based on (27), Z_L and I_{sa} can be solved as:

$$Z_L = Z_{11} = R_{optM} \tag{28}$$

$$I_{sa} = \frac{e^{-j\theta_1}}{\cos\theta_2} I_{dsa} = \frac{|I_{dsa}|}{\cos\theta_2} e^{j(\theta_\Delta - \theta_2)} \tag{29}$$

Comparing the circuit of Fig. 5(b) and the classic SLCG in Fig. 1(a), one can find that these two are very similar, except that an equivalent CS is used as the auxiliary transistor in Fig. 5(b). Therefore, it is still possible to modulate the main transistor to the 3rd quadrant and consequently maintain wideband SLCG operation with the help of the equivalent CS. However, this CS does not stand for the real auxiliary transistor, and the real drain voltage of the auxiliary transistor must be derived backward from (27) and (29). This leads to the following expression:

$$V_{dsa,sat} = |I_{sa,sat}|e^{j(\theta_\Delta-\theta_1)}\left[\frac{R_{optM}}{\cos\theta_2}\left(\frac{Z_{LM,sat}\cos\theta_1 + jR_{optM}\sin\theta_1}{Z_{LM,sat}+R_{optM}}\right) + j\sin\theta_2 Z_A e^{j\theta_1}\right] \tag{30}$$

At f_0, θ_1, θ_2, and θ_Δ are all equal to 0, and one can find that the value of $V_{dsa,sat}$ is equal to $I_{dsa,sat}(R_{optM}$ //$Z_{LM,sat})$, which is the same as (11) reported in the previous part. When frequency deviates from f_0, θ_1 and θ_2 deviate from 0 for a real network. Thereby, $V_{dsa,sat}$ is a function of frequency, $Z_{LM,sat}$, θ_Δ, and Z_A, and consequently, the evaluation of the proposed SLCG PA relies on large signal HB simulations.

Fig. 7 shows the flow chart used in evaluating the proposed SLCG PA. Firstly, various design parameters are calculated according to the method presented in the previous part for given P_{sat}, OBO, V_{DDA}, V_{KNEE}, V_{inmax}, and f_0. Then, the proposed SLCG OCN of Fig. 5(a) was established using (20) and (26), and the whole circuit was simulated using the HB simulator to solve the value of V_{dsa} and the SLCG P_{out} at a specified β_{in} under the given τ_A, τ_M, γ, θ_Δ, and frequency. To avoid the compression of the auxiliary transistor, in the simulation, the

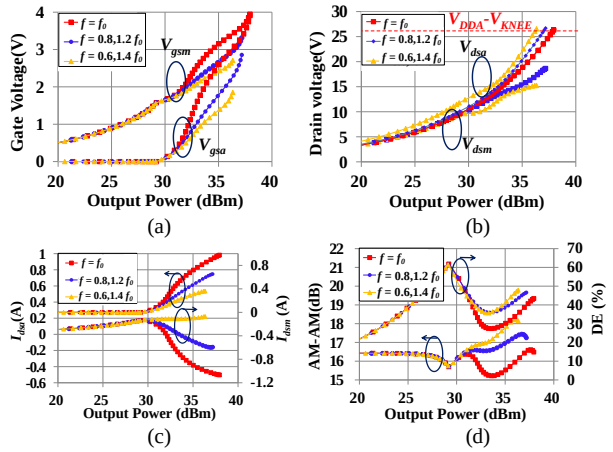


Fig. 9. HB simulation results of the proposed SLCG PA at different frequency points: (a) gate voltages; (b) drain voltages; (c) drain currents; (d) DE and AM-AM.

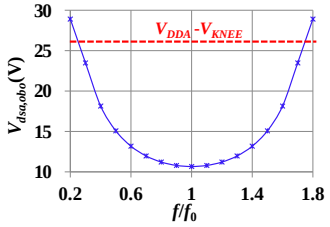


Fig. 10. Calculated $V_{dsa,obo}$ vs. frequency.

β_{in} value that yields V_{dsa} equal to V_{DDA}-V_{KNEE} is recorded and marked as the saturation input voltage $\beta_{in,sat}$, and the corresponding P_{out} is treated as the P_{sat}. Meanwhile, the values of group delay also have an important impact on the circuit bandwidth. Considering that the TL network in the main branch is the combination of OMN_M and the shunt Z_{outA}, τ_M should be higher than τ_A. Therefore, τ_M is set to twice τ_A in this analysis, and τ_A is set equal to $\pi/2f_0$, which is the group delay value of 90° TL. These settings make the analysis more realistic.

Using the above settings and flow chart shown in Fig. 7, the value of $\beta_{in,sat}$ and P_{sat} is solved at various frequencies for different γ and θ_Δ combinations under targe OBO of 8dB, P_{sat} of 38dBm, V_{DDA} of 28V, V_{KNEE} of 1.5V and V_{inmax} of 1V. Fig. 8(a)-(b) shows the computed P_{sat} vs. θ_Δ at various frequencies under γ=1. It can be found that the available SLCG P_{sat} decreases as the frequency deviates from f_0. When the frequency is lower than $0.5f_0$, or higher than $1.5f_0$, P_{sat} degrades by more than 2.5dB compared to the maximum P_{sat} at f_0. However, this degradation is lower than 1.6dB in the range of $0.6f_0 \le f \le 1.4f_0$. Therefore, it is reasonable to state that the SLCG PA functions normally in [$0.6f_0$, $1.4f_0$]. Secondly, the effect of θ_Δ on the available P_{sat} manifests at edge frequencies, such as at $0.6f_0$ and $1.4f_0$. Since the implementation of θ_Δ depends on the design of the input matching network (IMN), and the relative phase between the two paths of a real IMN is usually approximately linear with frequency, thereby θ_Δ is chosen equal to θ_2-θ_1 for preliminary analysis.

Fig. 8(c) shows calculated P_{sat} vs. γ at various frequencies under θ_Δ=θ_2-θ_1. It can be found that P_{sat} decreases with the increase of γ, but the overall variation is not large, thereby γ=1 can be used as the initial choice for prototyping. Fig. 8(d) shows the calculated $\beta_{in,sat}$ vs. frequency under θ_Δ=θ_2-θ_1 and γ=1. It is obvious that the auxiliary transistor enters saturation at lower β_{in} when the frequency is offset from f_0.

Using the above observations, the proposed SLCG PA of Fig. 5(a) is simulated with the HB simulator at various frequencies while setting the range of β_{in} to [0, $\beta_{in,sat}$] and selecting γ and θ_Δ as 1 and θ_2-θ_1, respectively. Fig. 9 shows the obtained large signal simulation results. As the frequency deviates from f_0, the saturation value of the V_{gsa} and V_{gsm} decreases [see Fig. 9(a)] due to the reduction of the $\beta_{in,sat}$ [see Fig. 8(d)], and the value of V_{dsa} in Fig. 9(b) reaches V_{DDA}-V_{KNEE} at lower P_{out}. Moreover, the main transistor gradually changes from behaving as a load impedance to behaving as an active device in the HPR. For instance, as shown in Fig. 9(c), when the frequency is equal to $0.8f_0$ or $1.2f_0$, although the transistor still operates with I_{dsm}<0 in part of the P_{out} range, but this range is less than the one at f=f_0. Moreover, at f=$0.6f_0$ or $1.4f_0$, I_{dsm} is maintained higher than 0 for all power levels. This translates into better efficiency in the HPR at edge frequencies [see Fig. 9(d)].

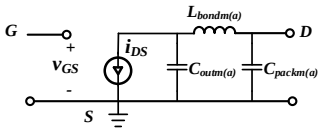
Finally, if the frequency greatly deviates from f_0 (e.g., f=0.4, $1.6f_0$), one can find from Fig. 8(a)-(c) that the choice of θ_Δ and γ help little in raising the P_{sat}. This limitation is related to the value of auxiliary drain voltage ($V_{dsa,obo}$) at the OBO power, which can be derived from (27) and expressed as follows:

$$V_{dsa,obo} = \frac{e^{-j\theta_1}\left(V_{DDM} - V_{KNEE}\right)}{\cos\theta_2} \tag{31}$$

According to (31), it is obvious that $V_{dsa,obo}$ is a function of θ_2 and consequently strongly dependent on the frequency. Fig. 10 plots the $V_{dsa,obo}$ vs. frequency. One can find that, for f <$0.4f_0$ or f >$1.6f_0$, the resulted $V_{dsa,obo}$ amplitude is already very close to V_{DDA}-V_{KNEE}, thereby the further driving of the auxiliary transistor leads to its compression and contributes little to the overall P_{out}. For the frequency inside [$0.6f_0$,$1.4f_0$], which corresponds to a θ_2 range of [-36°, 36°], the amplitude of $V_{dsa,obo}$ is relatively small. This implies that there is still enough voltage margin for the auxiliary transistor to generate substantial output power. Therefore, in the practical design, it is extremely important to keep τ_A as small as possible, so that the variation of θ_2 is low enough to maintain sufficient output power.

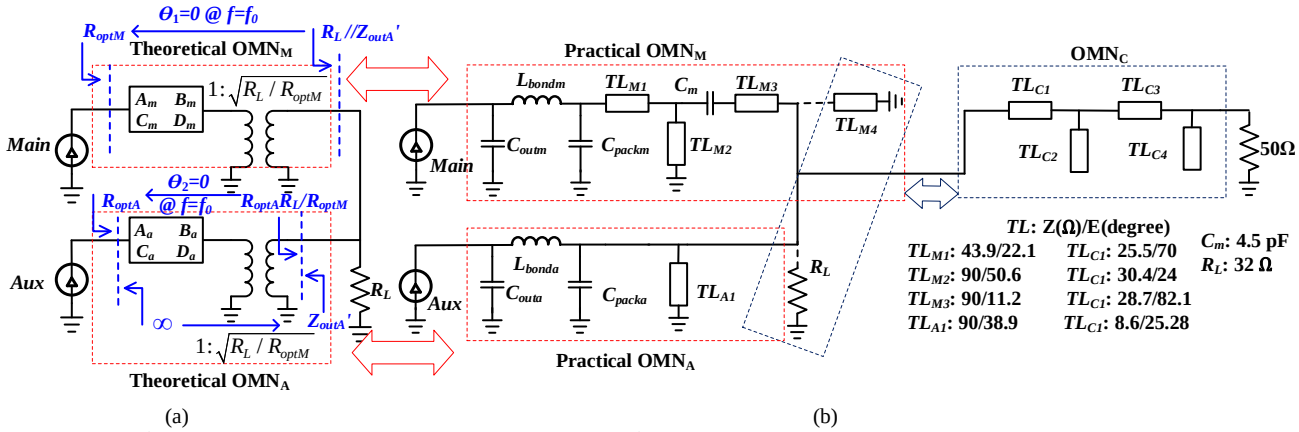
TABLE II
THEORETICAL PARAMETERS OF THE SLCG PROTOTYPE

Circuit parameters				
V_{DDM}	R_{optA}	R_{optM}	I_{maxM}	I_{maxA}
12.7V	24.1Ω	55.65Ω	0.95A	2.2A



C_{outm}	L_{bondm}	C_{packm}
0.92pF	0.62nH	0.21pF
C_{outa}	L_{bonda}	C_{packa}
1.8pF	0.62nH	0.38pF

Fig. 11. Transistor parasitic model and its extracted parameter values.



(a) (b)

Fig. 12. Design of the proposed OCN: (a) theoretical OCN with ideal transformer inserted; (b) practical OCN with transistor parasitic absorbed and OMN_C added.

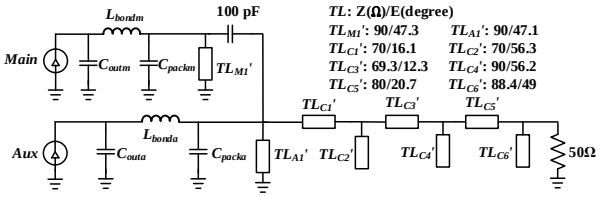


Fig. 13. Diagram of the classical OCN

III. Circuit Design And Simulation

A. The Design of the Proposed OCN

This chapter applies the proposed theory to design a 1-3 GHz high-efficiency SLCG PA with a target P_{sat} of 38dBm and OBO of 7.5dB. Using these targets and Fig. 3, various SLCG parameters can be calculated while setting V_{DDA} and V_{KNEE} to 28V and 1.5V, respectively. Table II summarizes the calculation results, where the obtained I_{MAXM} and I_{MAXA} are used as references to determine the main and auxiliary transistors. As there is no flexibility to adjust the maximum drain current of a packaged transistor, one can only pick up the closest. After careful selection, Wolfspeed transistors CGH40006P and CG2H40010P are utilized as the main and auxiliary active devices, respectively. The maximum drain currents of these two transistors at V_{DD}=3V and V_G=0.5V are 1.06A and 1.96A, which are close to the theoretical values in Table II.

In addition, to improve efficiency at the back-off, the drain supply voltage (V_{DDM}) of the main amplifier is slightly reduced to 12V. Furthermore, by load-pulling the main and auxiliary transistors at the back-off power and saturation power, their optimal impedances, R_{optM} and R_{optA}, are determined as 57Ω and 28 Ω, respectively, which are also close to the theoretical ones in Table II. The transistors' parasitic parameters are also extracted and summarized in Fig. 11. These parasitic parameters include the transistor output parasitic capacitance $C_{outm(a)}$, the package inductance $L_{bondm(a),}$ and the package capacitor $C_{packm(a)}$.

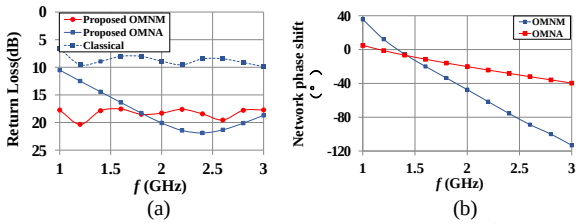
With the above parameters obtained, the impedance transformation targets required for the theoretical OCN in Fig. 5(a) can be clearly identified. However, when implementing Fig. 5(a), it is possible to add ideal transformers with the same voltage ratio to both main and auxiliary branches. This is shown in Fig. 12(a). Note that this operation does not vary the network parameters seen by the two transistors and consequently does not affect the SLCG PA large signal performance. Meanwhile, it brings an additional degree of freedom, i.e. the combining load of the OCN (R_L) does not have to be fixed to R_{optM}, but can be freely selected to boost the SLCG bandwidth. Henceforth, the practical OCN is developed based on the theoretical prototype shown in Fig. 12(a) instead of Fig. 5(a). Such a design strategy has been widely adopted in many broadband Doherty PAs [11], [14].

Applying the above design strategy, the practical OMN_M and OMN_A now need to absorb the corresponding transistor parasitic parameters and fulfill the impedance and phase transformation targets marked in Fig. 12(a). Note that these targets are essentially obtained by cascading the requirements in Fig. 5(a) with the additional transformers in Fig. 12(a). When designing the practical OMN_A, according to Fig. 10, the group delay of this network should be kept as small as possible to avoid the early compression of the auxiliary transistor. Therefore, in this design, only one parallel TL (TL_{A1}) is incorporated in the auxiliary branch to minimize the network group delay. By adjusting the electrical length and characteristic impedance of TL_{A1} and selecting the appropriate R_L, the combination of parasitic parameters and TL_{A1} in Fig. 12(b) is made equivalent to the theoretical OMN_A shown in Fig. 12(a). This realizes wideband impedance matching and the goal of minimal auxiliary phase shift.

After completing the design of OMN_A and obtaining the values of R_L and the output impedance of the auxiliary branch (Z_{outA}'), the high-pass-component-based circuit shown in Fig. 12(b) ($TL_{M1\text{-}4}$, C_m) is applied to realize the practical OMN_M by achieving the parasitic absorption and the target impedance matching and phase transmission highlighted in Fig. 12(a).

Finally, to reduce the complexity of the layout routing around the combining node, a fourth-order ladder network (TL_{C1}-TL_{C4}) is used to realize the parallel combination of R_L and TL_{M4}, so TL_{M4} does not exist in the designed OCN. In other words, the designed OCN only includes the components connected with the solid line in Fig. 12(b).

For comparison purposes, a reference SLCG OCN is designed using the classical method presented in [20]. Fig. 13



(a) (b)

Fig. 14. Simulated matching and phase characteristic of the proposed and classical OCNs: (a) return loss; (b) phase shift.

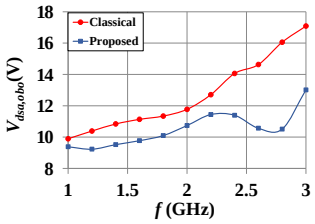


Fig. 15. Simulated $V_{dsa,obo}$.of the proposed and classical OCNs

shows the diagram and circuit parameter of the designed classical OCN, where a 100pF DC-block capacitor is used to directly connect the external drain terminals of the two transistors together, and two short stubs (T_{LM1}' and T_{LA1}') are adopted to provide the drain bias, and a sixth-order ladder network is utilized for post-matching. The circuit parameters of this classical OCN are selected to provide the optimal matching to R_{optM} over 1-3GHz.

Fig. 14 shows the simulated return loss and phase shift of the OMN_M and OMN_A, where the return losses are calculated from the reflection coefficients of the main transistor drain impedance at LPR and the auxiliary drain impedance when OMN_A terminates with the matched load, with reference to their optimal impedances, i.e. R_{optM} and R_{optA}, respectively. Based on Fig. 14(a), over 1-3GHz, the proposed OMN_M can provide good matching to R_{optM} in LPR with a return loss of <-18dB, while the classical OCN can only maintain a return loss of about -10dB. This is mainly due to the direct connection of the main and auxiliary transistors in the classical method. As a result, no matching element can be applied in the main amplifier branch to compensate for the finite OFF-state auxiliary transistor output impedance generated by the significant transistor parasitic parameters, and consequently, the matching capacity of the classical OCN is limited.

Meanwhile, based on Fig.14(b), the proposed OMN_A exhibits a low phase shift within [-40, 8 °]. This low phase variation yields small $V_{dsa,obo}$, which is depicted in Fig. 15 and evaluated as the drain voltage of the OFF-state auxiliary transistor while setting V_{dsm} equal to V_{DDM} -V_{KNEE}. Note that the deduced $V_{dsa,obo}$ is much smaller than V_{DDA} - V_{KNEE} over the entire frequency band, thus the early compression of the auxiliary transistor can be avoided. Moreover, Fig. 15 also illustrates the calculated $V_{dsa,obo}$ of the classical OCN. By comparison, the $V_{dsa,obo}$ in the classical design becomes larger than the proposed one at higher frequencies. This implies early compression of the auxiliary transistor and degradation of P_{sat} in the classical SLCG PA at upper edge frequencies. These comparisons clearly illustrate the effectiveness of the proposed method in the packaged transistor scenario.

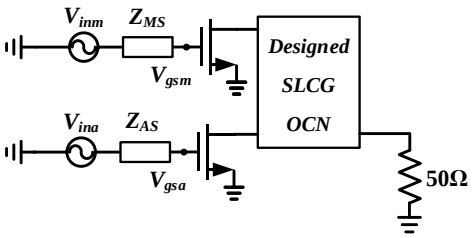


Fig. 16. Dual input circuitry used to extract the target input gate voltages and source impedances.

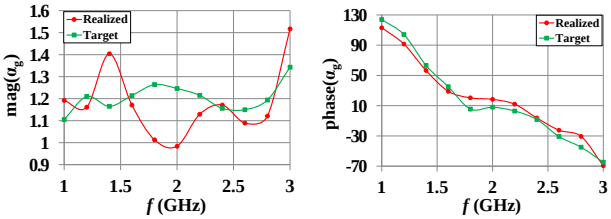


Fig. 17. Comparison of the realized voltage ratio and the target one: (a) magnitude; (b) phase.

The above results imply that sufficient P_{sat} and high back-off efficiency can be obtained over 1-3 GHz, which corresponds to an FBW of 100%. Note that this FBW is slightly higher than the theoretical one (80%) predicted by Fig. 10. This discrepancy is mainly due to the simplicity of the designed OMN_A. For instance, the designed OMN_A only adopts one short stub outside the transistor so that its group delay value is lower than the 90 °TL one which is used as the basis in calculating Fig.10. Therefore, the realized FBW becomes slightly higher than the theoretical prediction.

B. The Design of the IMN and Simulation of the Proposed SLCG PA

Based on the analysis in Section II, the main and auxiliary input signal must exhibit appropriate phase differences to enhance the P_{sat} at the edge frequencies. This is similar to those required in many wideband DPA designs. Therefore, the dual-input method [11], [14] which is commonly used in DPA designs can be applied. Fig. 16 shows the diagram of this method that uses the designed OCN and adjustable input sources to extract the input voltage ratio (α_g=V_{gsa}/V_{gsm}) and the main and auxiliary source impedances (Z_{MS}, Z_{AS}) that yield optimal P_{sat} at various frequency points.

The IMN is then designed to provide the extracted voltage ratios (see Fig. 17) and source impedances. Fig. 18 shows the overall circuit diagram of the designed SLCG PA. With reference to Fig. 18, a third-order Wilkinson Divider is used to achieve equal power distribution from 1-3GHz. The parallel RC pairs are connected in series with the transistor gate to enhance the stability at high frequencies, and the 50Ω resistor is added in the DC gate bias path to enhance the PA stability at the low-frequency band. In addition, band-pass matching networks are used in both the main and auxiliary paths to realize wideband matching between the 50Ω source impedances and the transistor gate impedances. Moreover, a high-pass π-network is used in the auxiliary branch, and 50Ω delay lines are added to both paths. These elements facilitate phase control as well as layout routing. Fig. 17 compares the realized voltage ratio obtained from layout simulations and the target one extracted by using Fig. 16. Based on Fig. 17, it can

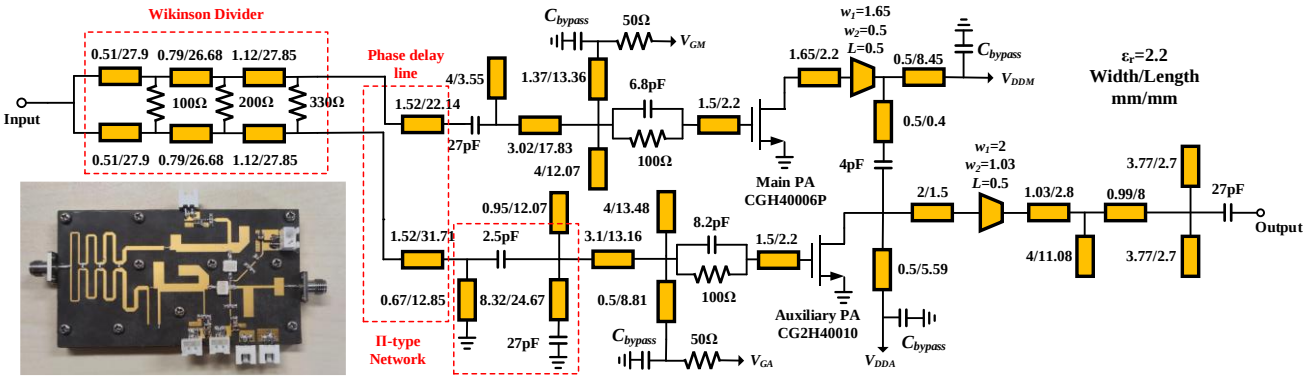


Fig. 18. Schematic diagram of the designed SLCG PA (with junctions and bends omitted) and the photograph of the fabricated one.

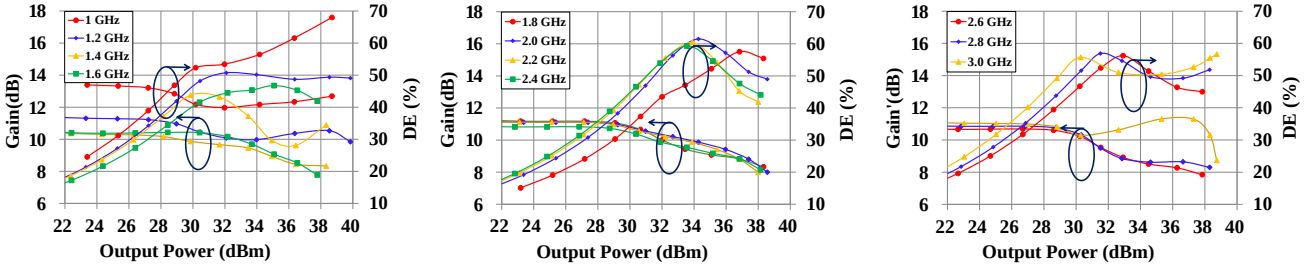


Fig. 19. Simulated DE and gain vs. P_{out} for: (a) 1-1.6GHz (b) 1.8-2.4GHz (c) 2.6-3.0GHz

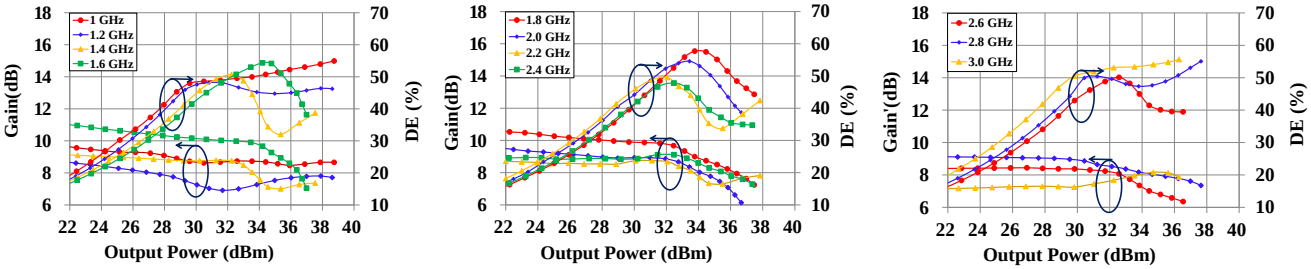


Fig. 20. Measured DE and gain vs. P_{out} for: (a) 1-1.6GHz (b) 1.8-2.4GHz (c) 2.6-3.0GHz.

be found that the designed IMN well fulfills the required phase and amplitude control conditions.

Fig. 19 shows the large-signal simulation results of the designed SLCG PA. Based on Fig. 19, over the frequency range of 1-3GHz, the PA is capable of delivering P_{sat} of 37.8-40 dBm, low power gain of 10.5-13.3dB and DE of 43.5-53%, 40-56.4%, and 43.8-68% at 7.5dB, 6dB and 0dB back-off from P_{sat}, respectively.

IV. Measurement Results

Fig. 18 depicts the photograph of the fabricated PA which occupies an overall PCB area of 9.3×5.2cm^2. In the measurement, the drain supply voltages of the main and auxiliary transistors were 12V and 28V, respectively, and the quiescent drain current of the main transistor and the gate bias voltage of the auxiliary transistor were set to 30mA and -4.8V, respectively.

In the CW-signal measurement, the RS signal generator SMW200A and power meter NRPZ-86 were used to generate input excitation and detect the output, respectively. Fig. 20 shows the measured DE and gain vs. P_{out} of the proposed PA at various frequency points. As can be seen from Fig. 20, the PA can provide a P_{sat} of 36.5-38.7dBm, a low power gain of 8.2-11.2dB. At 7.5dB OBO, 6dB OBO, and saturation power, the PA delivers DE of 39.2-49.1%, 45.4-51.2%, and 47.8-57.7%, respectively, over 1-3GHz. When compared with the simulation results [see Fig. 21(a)], the measured P_{sat} and DE are about 1-2dBm and 5-10% lower. This is mainly due to the large signal model's inaccurate prediction of the transistor behavior in the 3rd quadrant. For instance, the modeling of the 3rd quadrant transistor behavior may partly come from replicating the 1st quadrant one rather than from real testing. This leads to model inaccuracy and yields discrepancies between simulation and measurement as the real GaN HEMT transistor usually does not exhibit symmetry between the drain and source terminals.

In addition, it can be found that both simulated and measured gain characteristics exhibit compressions of about 2-3 dB in the HPR. This deviates from the theoretical results with optimal gain behaviors presented in Section II-B. This is mainly because that the theoretical results in Section II-B are based on the harmonic-short condition which is practically difficult to realize in a broadband design. Therefore, the

TABLE III
COMPARISON TO RECENTLY REPORTED PCB-BASED GAN WIDEBAND AND HIGH BACK-OFF EFFICIENCY PAS

Ref. (Year)	Technique	Transistor type	Freq/FBW GHz/%	Psat (dBm)	Gain (dB)	OBO (dB)	DE@OBO (%)	DE@Psat (%)	Modulation	Center Freq(GHz)	PAPR (dB)	Pavg (dBm)	Average DE(%)	ACPR w. DPD(dBc)	ACPR w/o DPD(dBc)
[12]2018	DPA	Package Device	1.5-3.8 /87	42.3-43.4	10-13.8	6	33-55	42-63	7M WiMAX	2.6	9	34	33	-48	-42
[13]2023	DPA	Package Device	1.4-2.5 /56	43.6-45	12-13.1	6 /7.5	49-58 /43-50[a]	62-71	20M 64QAM	1.4/2/2.5	6.5	37	48/55/51	<-45	<-30
[17]2023	LMBA	Package Device	2.05-3.65 /56.1	45.2-46.8	7.8-10.8	6 /8	51.2-65.8 /50.5-66.2	61.2-79.2	60M /100M LTE	2.25/2.75 /3.25	8	36.2-38.5 /36.1-38.3	50.7-64.7 /49-63.5	-45.2~-59.1 /-40.3~-49.2	-22.3~24.6 /-21.4~24.2
[18]2021	LMBA	Package Device	0.55-2.2 /120	41-43	8-15	6 /7.5	40-60 /45-67[a]	49-82	20M LTE	0.55-2.2	10	31-34	51-62	N/A	-22~-34
[15]2018	DEPA	Bare Die	1.8-3.8 /71.5	44.3-46.5	7.6-10.8	6 /8	35-56[a] /41-51	42-62	20M LTE	1.8-3.8	8	36.5-37.5	38-52	<-50	<-20
[20]2021	SLCG	Bare Die	0.7-2.8 /120	43.1-45	8-12	6 /7.5	45-57.5 /40-53[a]	56-70.3	40M LTE	0.7-2.8	7.7	36.3-37.8	47.8-50	-47~-48.8	N/A
[7]2017	Current Bias	Bare Die	0.8-2.2 /93.3	39.7-40.7	10.5-14.2	6 /7.5	37-45 /36-47[a]	36-48	5M LTE	0.8-2.2	7.2	33.1-34.5	36.9-48.8	-48.1~-54.4	N/A
This Work	**SLCG**	**Package Device**	**1.0-3.0 /100**	**36.5-38.7**	**8.2-11.2**	**6 /7.5**	**45.4-51.2 /39.2-49.1**	**47.8-57.7**	**40M 64QAM**	**1.0-3.0**	**7.5**	**28.8-31.6**	**39-49.2**	**-45.9~-48.4**	**-27~-35.3**

[a] read from graph

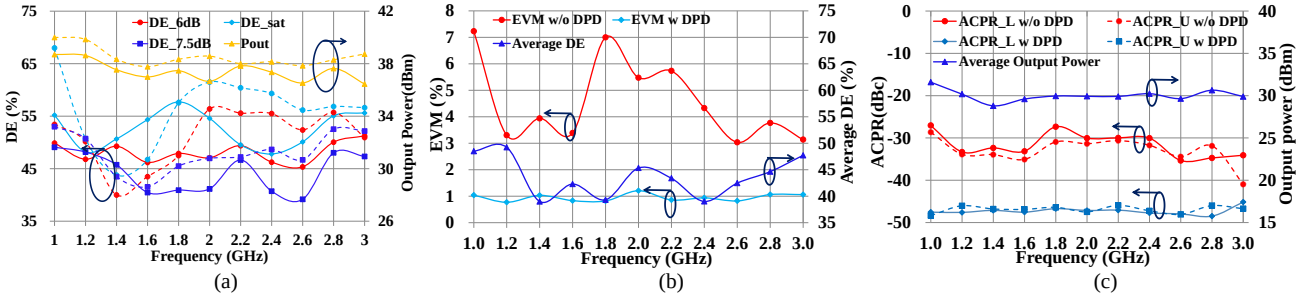


Fig. 21. Summary of measurement results under CW and modulated signals: (a) comparison of the measured (solid line) and simulated (dotted line) large signal CW results; (b) measured average DE and EVM before and after DPD; (c) measured P_{avg} and ACPR before and after DPD

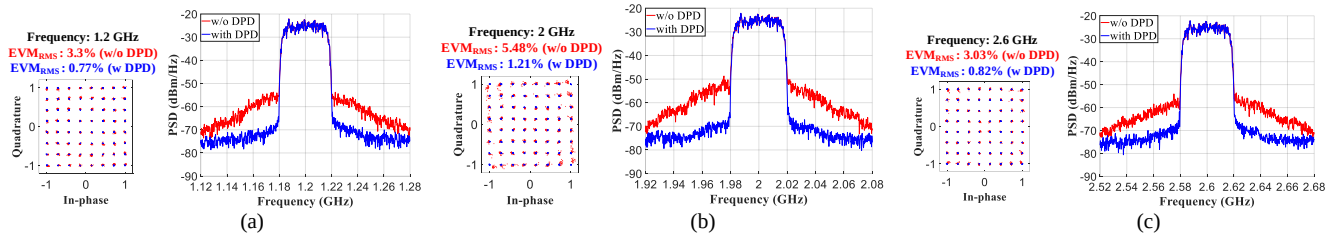


Fig. 22. Measured output spectrum and constellation diagram before and after DPD at: (a) 1.2GHz; (b) 2GHz; (c) 2.6GHz.

non-zero harmonic impedances, especially the 2nd one, may generate additional compression in the HPR and leads to degraded gain characteristics compared to the theoretical ones.

In the modulated signal measurement, the PA is fed with a 64QAM signal with a PAPR of 7.5dB and a modulation bandwidth of 40MHz, and the RS spectrum analyzer FSW43 was used to detect the PA output signal. From 1GHz to 3GHz with a step of 0.2GHz, a complexity-reduced Volterra series based DPD technique [26] is applied to linearize the PA at an average P_{out} (P_{avg}) that is about 7.5dB back-off from P_{sat}. Fig. 21(b)-(c) summarizes the results of this measurement. According to Fig. 21(b)-(c), before DPD, the PA delivers an average DE of 39-49.2% at P_{avg} of 28.8-31.6 dBm while providing an ACPR of -27~-35.3dBc and an EVM of 3.1-7.2%. After DPD, the ACPR and EVM can be improved to -46~-48.4dBc and about 1.2%, respectively, while the same levels of P_{avg} and average DE can be retained.

Fig. 22 shows the measured PA output spectrum and constellation diagram at 1.2/2/2.6 GHz. As can be seen, PA can provide a DE of 49.2/45.3/42.5% at an average P_{out} of 30.2/30/29.7dBm and a center frequency of 1.2/2/2.6GHz. With DPD, ACPR can be improved from -33.5/ -30.8/ -35dBc to -47/-47.3/-48dBc, while EVM is enhanced from 3.3/5.48/3.03% to 0.77/1.21/0.82%. This demonstrates good linearizability.

Table III compares this work with other recently reported PCB-based wideband and high back-off efficiency PAs. It can be found that the proposed SLCG PA can achieve excellent fractional bandwidth (FBW) and back-off efficiency. When compared to the classical SLCG PA [20] that applies bare die devices, the proposed one realizes slightly lower FBW and comparable efficiency using packaged transistors that exhibit better compatibility and reliability. This verifies the capacity of the proposed method in expanding the application range of the SLCG technique.

V. Conclusion

In this paper, a comprehensive theory and a novel design methodology of the SLCG PA are presented. A set of SLCG design equations that can bring optimal gain and back-off efficiency characteristics are derived by studying the relationship between SLCG circuit parameters and its key metrics. A new SLCG OCN that absorbs various transistor parasitic and performs wideband impedance transformation with specific phase shifts is proposed to generalize the SLCG operating mode to the scenarios with commercial packaged transistors. The proposed methodology is then applied to design a wideband SLCG PA operating over 1-3GHz using commercial packaged transistors. The measurement results under both CW and modulated signal stimuli verify the excellent capability of the proposed SLCG PA in delivering high back-off efficiency, wide operation bandwidth, and good linearizability.

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