

# 28–38-GHz 6-bit Compact Passive Phase Shifter in 130-nm CMOS

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**Abstract**—In this letter, a highly compact, bidirectional, wideband 6-bit resolution passive phase shifter (PS) is presented in low-cost 130-nm CMOS technology. A compact Lange differential hybrid is designed in this letter to provide quadrature signals from the input. The compact Lange hybrid is followed by a switching matrix that generates weighted sums of the quadrature signals to cover 360° and additional controlled loss using single pole single throw (SPST) switches. The matrix consists of 12 transistors, each of which is controlled by a three-level gate voltage (0, 0.6, and 1.2 V) providing higher resolution in phase shifts. The chip achieves the state-of-the-art performance with 10-dB insertion loss across 28–38 GHz. The chip also achieves an rms gain error of 0.6 dB and an rms phase error of 3° in the bandwidth, consuming no dc power and only 0.15 mm<sup>2</sup> including baluns.

**Index Terms**—Beamforming, CMOS, coupler, front end, hybrid, passive, phase shifter (PS), switch.

## I. INTRODUCTION

FOR 5G communication systems, antennas need to create multiple independent beams. Low-frequency bands can use a complete digital phase shifter (PS), but the millimeter-wave (mm-wave) bands require precise analog phase shifter for a successful deployment of 5G communication systems. Phase shifters are essential components to build phased array systems. Many types of phase shifters have been proposed, some examples being switched *LC* networks, reflection type, and active vector combining phase shifters [1]–[5]. *LC* networks, reflection, coupled line, and other passive phase shifters are known to have large silicon footprint at *Ka*-band frequencies [6], [7]. These passive phase shifters have high insertion loss but are bidirectional, which reduces the number of phase shifters in the system. Active phase rotors are precise but have high power consumption and are not bidirectional [8], [9].

In this letter, a passive phase shifter with effective 6-bit resolution is presented in low-cost 130-nm CMOS. Section II describes the chip design followed by measurement results in Section III. Finally, Section IV draws the conclusion.

## II. CHIP DESIGN

Each channel in a front-end system consists of phase shifter for beamforming and beam steering, using single-pole double-throws (SPDTs) as proposed in Fig. 1. We can

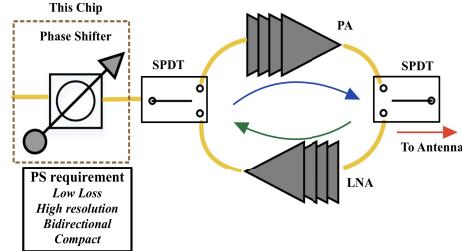


Fig. 1. Block diagram front-end 5G integrated transceiver.

reuse the phase shifter with lower power requirement. The configuration of the proposed phase shifter design is shown in Fig. 3. The circuit comprises an input balun, differential quadrature hybrid followed by the switching matrix, and output balun. The quadrature hybrid provides the signal in four basic quadrants mainly 0, 90, 180, and 270 [2], [10]. These signals are then combined via the CMOS transistor switch matrix, once in-phase and once out of phase. Passive vector combining systems have been proposed in [6], [7], [10], and [11]. In [10], the switching matrix is introduced, with ON-OFF-state switching providing low loss combining but also low resolution. In [6], [7], and [11], a 12-bit passive vector modulated phase shifter (VMPS) is demonstrated by attenuating using a binary-weighted switch system. Higher resolution requires a higher number of switching units, which increases insertion loss and parasitic capacitance requiring high-resonant inductors, leading to increased device size. Our approach of using a simple switching matrix such as [10] but using an additional intermediate control voltage level results in improved resolution without increased complexity of the circuit.

### A. Transistor as a Switch

Fig. 3 shows a simplified model for parasitic losses in a transistor as a switch. In ON-state, losses primarily arise due to channel resistance, which improves with larger size. As the size of the transistor increases, the parasitic capacitance starts to leak signal to the gate and to the substrate, which dominates the loss as size increases [8], [12].

Isolating the bulk of the transistor from the substrate using deep n-well (DNW) transistors and using high resistor to block the leakage improves the performance of the switch. High resistance at the gates avoids the breakdown of the transistor gates and avoids leakage through the gate. The DNW separates the bulk and the substrate minimizing loss to the substrate. Optimizing the n-well area to lower capacitance while providing isolation is essential for performance.

### B. Folded Quadrature Hybrid Coupler

Quadrature hybrids are 3-dB directional couplers with a 90°-phase difference between the through and the coupled

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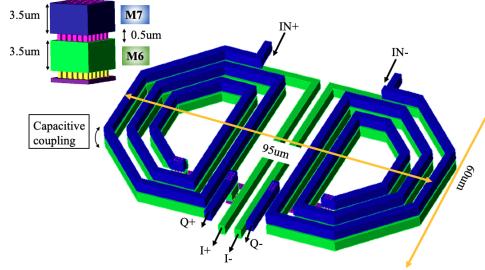


Fig. 2. 3-D layout: compact folded Lange hybrid.

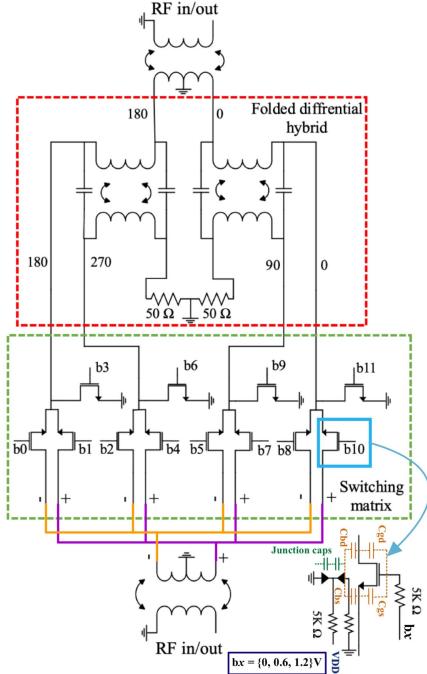


Fig. 3. Schematic phase shifter.

arms. Multiple implementations of such couplers are presented in [1], [4], [6], and [7]. The most common way of achieving 90° phase shifts is using coupled lines as unfolded Lange coupler configuration [4], [15]. The problem with Lange or any coupled line coupler is the size of the component. Multiple-folded couplers are mentioned in the literature using a coplanar design to generate *I/Q* signals [4], [10]. One way of reducing overall size is to fold the line like an inductor and use the bottom layer for additional coupling [6]. Compared to a coplanar design in [10], a 7% reduction in footprint was achieved at half the frequency in the stacked design. The hybrid is designed using 3.5- $\mu$ m-thick top metal and the metal layer below it. The hybrid achieves a simulated insertion loss of 3.5 dB with a phase error between *I/Q* phases of 4° at 35 GHz. Even though the hybrids are placed 10  $\mu$ m from each other, an isolation of 15 dB is achieved between *I*+/*I*- phases. Fig. 2 shows the 3-D layout of the differential hybrid.

### C. Switching Matrix

Once we have the primary signals through the hybrid, we now need to add them and insert minute phase shift/attenuation between them using single pole single throw (SPST) switches [10]. In order to generate all phases, we need to add the vectors either in-phase with each other or out of phase. Fig. 3 shows the schematic of the switching matrix with

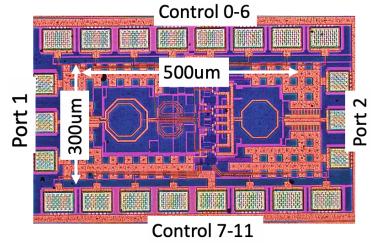


Fig. 4. Chip field image.

a differential load. The gate voltages are treated as control. Each gate voltage is set to have one of three levels 0, 0.6, and 1.2 V. Therefore, we have 12 controls with three levels, amounting to a total of 3<sup>12</sup> possible states. Transistors with control *b*<sub>11</sub>, *b*<sub>9</sub>, *b*<sub>6</sub>, and *b*<sub>3</sub> are used for fine-tuning the phase. The output of the switching matrix is added and is transferred to single ended using a balun. The balun output is matched to 50  $\Omega$  and the best results were obtained when the switching matrix is loaded with 25  $\Omega$ . The output balun is optimized to get the maximum matching for multiple states at the output of the switching matrix. The input-output baluns add 0.5–0.7 dB to the insertion loss. The use of 0.6 V as an intermediate control voltage degrades the power-handling performance of the phase shifter. The simulated IP1 of the phase shifter at 35 GHz is between 12 and 16 dBm for all states. A 5° AM-phase modulation (PM) occurs at 14-dBm input power for a 3-bit PS (45° shift).

All transistors are equal in size (eight fingers of 5  $\mu$ m width each). The gates of the transistors are ac floating with 5-k $\Omega$  resistors, as are the isolated p-well body and DNW. The bulk is connected to the ground and DNW to 1.2 V. This configuration yields the best IP1 and insertion loss in an SPST switch [12], [14]. Fig. 3 shows the basic schematic of the switching matrix.

### III. MEASUREMENT RESULTS

The IC was fabricated in the Tower-Jazz 130-nm seven metal CMOS process (Fig. 4). The *S*-parameters for the chips were measured using the Agilent E8361C vector network analyzer. As every gate control has three levels, thus, 3<sup>12</sup> states were measured. States providing a uniform response with respect to phase resolution and insertion loss were selected.

One of the motivations of our proposed design is achieving a better tradeoff between resolution and insertion loss and error. Using the same topology with binary switching states [0, 1.2 V] yields 4-bit resolution (22.5°), average insertion loss of 10.5 dB, and gain variation of  $\pm 2.5$  dB at 35 GHz. Keeping binary switching and trying to increase resolution would increase insertion loss and variation even more. Using [0.6, 1.2 V] binary switching yields only 3-bit resolution (45°), 10-dB insertion loss, and  $\pm 1.5$ -dB variation. The idea behind this passive phase shifter is to get the maximum possible resolution at minimum loss. Using [0, 0.6 V] binary switching yields only 4-bit resolution (22.5°), 12-dB insertion loss, and  $\pm 1$ -dB variation. However, using our proposed approach of ternary switching [0, 0.6, 1.2 V], we improve the tradeoff on all aspects. We measured an average loss of 10 dB with a variation of 0.5 dB for a maximum resolution of 5.625° (6-bit). Decoding the proper 64 states is a simple digital lookup table.

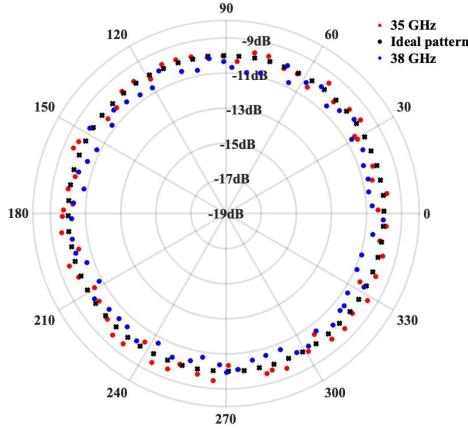


Fig. 5. Polar plot of the optimized control states at 35 GHz.

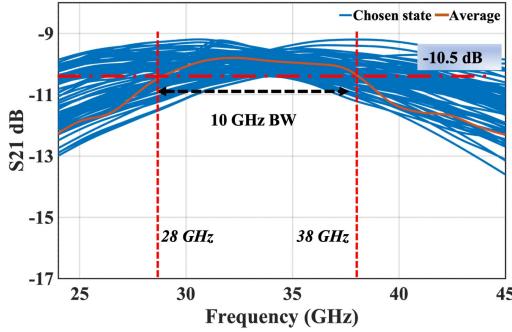


Fig. 6. Insertion versus frequency (64 optimized states).

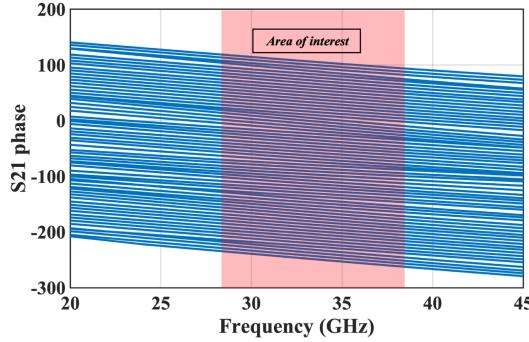


Fig. 7. Phase versus frequency (64 optimized states).

Fig. 5 shows a polar plot of the optimized states at 35 GHz/38 GHz. Fig. 6 shows the insertion loss across frequencies. Fig. 7 shows the phase performance with respect to the frequency. Fig. 8 shows the rms gain and phase error. The rms phase error is better than  $3^\circ$  and the rms gain error is better than 0.6 dB across the bandwidth. Fig. 9 shows the return loss with respect to frequency for chosen states. Gain variation is caused by variation in return loss, and states are optimized to the lower root mean square error (RMSE) gain error. The maximum gain error of  $\pm 1$  dB was measured at 28 and 38 GHz, respectively, with a maximum error of  $\pm 0.5$  dB that was measured at 35 GHz. The maximum phase error of 1 LSB (5.625°) was measured in the bandwidth

$$\text{Phase error} = \sqrt{\frac{1}{N-1} \sum_{n=1}^N (\phi_{n-\text{measured}} - \phi_{n-\text{ideal}})^2} \quad (1)$$

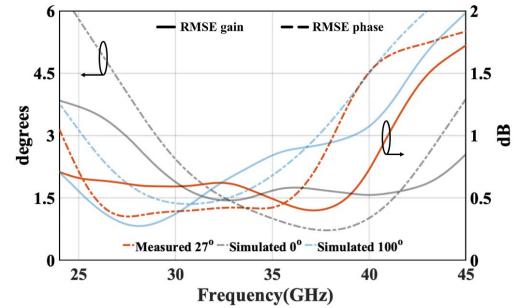
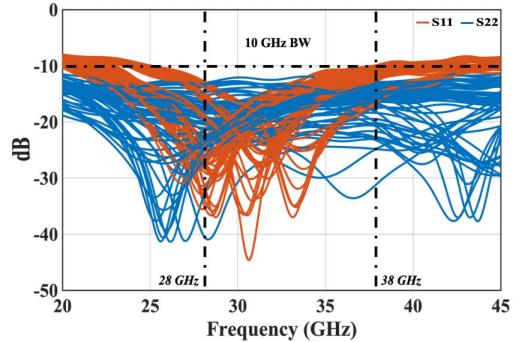


Fig. 8. RMSE phase and gain error versus frequency at three temperatures.

Fig. 9.  $S_{11}$  and  $S_{22}$  versus frequency (64 optimized states).TABLE I  
COMPARISON TO STATE OF ART

| Ref                     | This Work     | MWCL '20[3] | MWCL '17[4] | TCSII '21[5] | SSCL '20[11] |
|-------------------------|---------------|-------------|-------------|--------------|--------------|
| Process                 | 130nm CMOS    | 28nm CMOS   | 65nm CMOS   | 65nm CMOS    | 65nm CMOS    |
| Freq (GHz)              | 28-38         | 29-37       | 27-42       | 37-40        | 27-31        |
| Mean loss(dB)           | 10/10.5       | 12.8        | 12.4        | 9.3          | +4*          |
| Loss Var (dB)           | $\pm 0.5 / 1$ | $\pm 2.5$   | $\pm 1.4$   | $\pm 1$      | $\pm 0.2$    |
| Resolution (deg)        | 5.625         | 22.5        | 11.25       | 11.25        | 5.625        |
| RMSE gain (dB)          | < 0.6         | < 1.1       | < 2.1       | < 0.64       | < 0.1        |
| RMSEphase(deg)          | < 3           | < 8.8       | < 3.8       | < 8          | < 4          |
| Size (mm <sup>2</sup> ) | 0.15          | 0.08        | 0.395       | 0.258        | -            |
| Bi-directional          | ✓             | ✓           | ✓           | ✓            | ✗            |
| DC power (mW)           | 0             | 0           | 0           | 0            | 40           |

\*- Active vector combining

$$\text{Gain error} = \sqrt{\frac{1}{N-1} \sum_{n=0}^N (\text{IL}_{n-\text{measured}} - \text{IL}_{\text{mean}})^2}. \quad (2)$$

## IV. CONCLUSION

In this letter, a 6-bit effective phase shifter is designed for *Ka*-band applications in a cheap 130-nm bulk CMOS process. The 12 gate-controlled low-loss switches are used to attenuate and combine signals. Each “control” has three levels, which provides flexibility in generating multiple states of a similar phase or loss response. Optimizing these states and creating a lookup table leads to lower gain and phase errors improving precision of the phase shifter. This 6-bit phase shifter achieves a mean insertion loss of  $10 \pm 0.5$  dB at 35 GHz with rms phase error lower than  $3^\circ$  and rms gain error lower than 0.6 dB. Compared to the state of the art in Table I, this phase shifter has the minimum rms gain/phase error and resolution compared to the phase bidirectional phase shifters. A higher number of states to choose from increases the resolution of the phase shifter at the cost of complex digital control while keeping the RF complexity down to the minimum.

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