An 18–50-GHz Δ−Σ Modulated Quasi-Continuous Digital Vector-Modulation Phase Shifter With Variable Gain Control

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***Abstract*— This letter presents a high precision wideband active vector-modulating phase shifter with high dynamic range gain control ability. Compared with conventional switching-filter phase shifter and vector-modulation phase shifter, this Δ–Σ modulated vector phase shifter can provide quasi-continuous phase and gain control capability. According to the experimental results, the dynamic range of gain control is greater than 35.5 dB. The output reflection is lower than −10 dB through the 18–50-GHz band, and the input reflection is lower than −10 dB from 18 to 45 GHz. The phase shifter occupies 700 μm × 900 μm on 0.13-μm SiGe bipolar complementary metal-oxide-semiconductor (BiCMOS) technology, and the core size is only 400 μm × 500 μm. After digital calibration, the proposed phase shifter has achieved the highest phase and gain control precision compared with the state-of-the-art digital controlled phase shifters.**

***Index Terms*— Δ–Σ modulation, gain control, high phase precision, millimeter-wave, phased array, phase shifter, wideband.**

I. Introduction

PHASED array system is the main form of millimeter-wave communication and detection system [1]. In phased arrays, the phase shifter is the key block to achieve flexible beam control ability. Conventional phase shifters use switches to select different phase shift networks and combine multiple stages to implement more control bits, which introduces high insertion loss due to the serial connection of multiple networks. The insertion loss of a 4-bit phase shifter is about 12 dB in *Ka*-band as shown in [2] and could be much higher up to a higher frequency band. This high loss leads to designing difficulty in the signal path. In the previous, vector modulating phase shifters often use low bit count current digital-to-analog converters (DACs) or phase select switches as shown in [5] to control the phase of quadrature signal, which limits the phase control resolution and introduced gain error between different control states. To accommodate variable received signal power or adjust transmitted channel power, a variable gain amplifier (VGA) should also be used in the signal path of the transceiver, which makes the design even more complex.

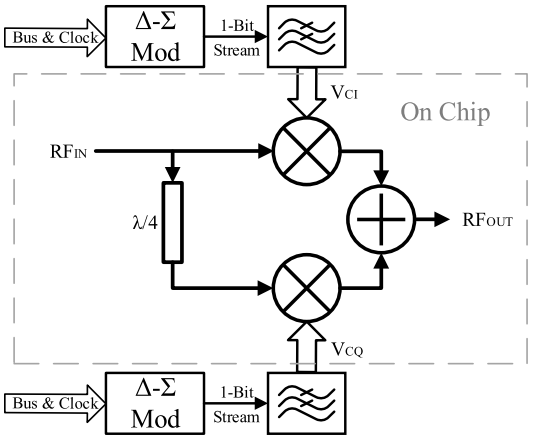

Fig. 1. Overall structure of the phase shifter.

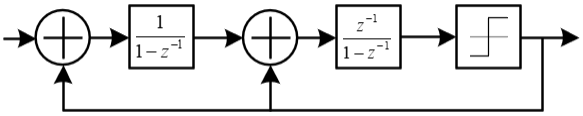

Fig. 2. Structure of the second-order Δ−Σ modulator.

In this letter, an 18–50-GHz Δ−Σ modulated quasi-continuous digital vector-modulation phase shifter with variable gain control ability is presented. The vector modulator architecture can overcome the loss problem and the Δ−Σ modulation technique is used to generate quasi-continuous high-resolution control voltages which greatly improves the phase control resolution and enables digital calibration. The proposed phased shifter uses a vector modulating scheme to provide additional gain control ability by adjusting the control voltage proportionally to avoid using standalone VGA components.

II. Phase Shifter Circuit Design

The architecture of the proposed phase shifter is shown in Fig. 1. This phase shifter includes a 90° transmission line to generate quadrature input signal, two active baluns, and Gilbert cells for control voltage multiplier. Two digital Δ−Σ modulators, which are shown in Fig. 2, are used to generate the I/Q control voltage VCI and VCQ. The Δ−Σ modulation modulates the quantization noise to high frequency and keeps the desired low-frequency signal clean.

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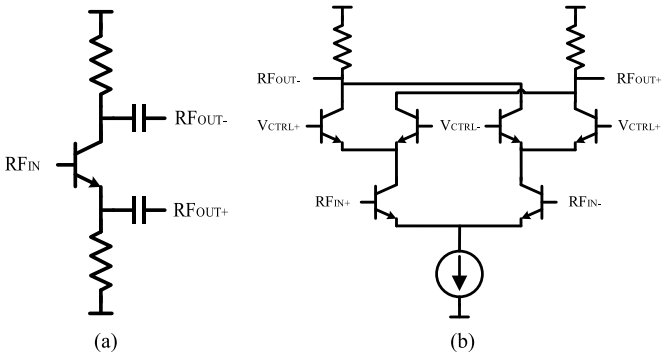

Fig. 3. Simplified schematics of (a) active balun and (b) Gilbert cell multiplier.

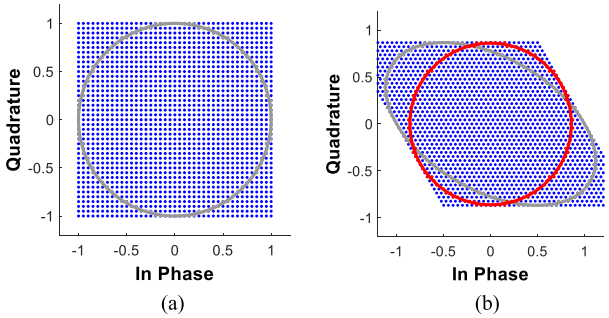

Fig. 4. Gain and phase impairment correction of the proposed phase shifter. (a) Normal 90° phase shift at center frequency. (b) Reselected phase shift state to compensate error at other frequencies.

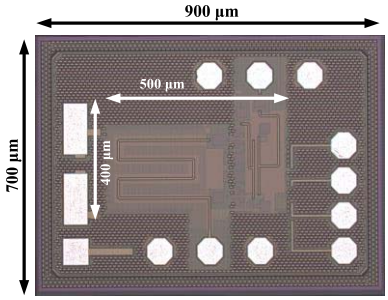

Fig. 5. Photograph of the proposed phase shifter.

Thus, the high-frequency noise can be removed by a low-pass filter (LPF). The Δ–Σ modulator and the passive LPF are implemented on external printed circuit board (PCB) using field-programmable gate array (FPGA) and passive *RC* components. The second-order Δ–Σ modulator provides 16-bit quasi-continuous voltage resolution, and the bandwidth of the passive filter is 10 kHz. The bandwidth of the filter affects both the settling time of control states and the noise level of the phase and gain control voltage, which should be adjusted according to system design requirements. The modulators operate at 50 MHz; thus, the quantization noise level of the filtered signal is −173.8 dB, which could be considered noise-free.

Fig. 3(a) and (b) shows the simplified schematics of the active balun and Gilbert cell multiplier. The active balun converts single-end RF signals into differential signals and then feeds to the Gilbert cell. The Gilbert cells multiply the control voltage with the signals from balun, generating voltage-controlled quadrature signals and combined at the load resistors. To ensure that the insertion loss of the phase shifter is flat and the output reflection is low across 18–50 GHz, resistive loads are used instead of inductors. The differential output is combined and converted into single-ended by absorbing one of the differential signals with a matched resistor.

The vector modulation scheme with high precision control voltages can compensate for the amplitude and phase impairment. Thus, there is no need to implement a 90° coupler or other complex hybrids. A 90° transmission line is enough to cover a 100% relative bandwidth frequency range. The 90° transmission line is located at the thick top metal layer to reduce conductive loss and bent to reduce area, thus maintaining a compact chip size. To compensate for the phase and gain impairment, the control voltage is adjusted to generate a compensated voltage and the error can be canceled. By choosing a closer control state, the phase and gain should match the expected value again, and only the maximum available gain (MAG) shall be compromised. Fig. 4 shows the reselected control state of an impairment state. Fig. 4(a) shows the control states without gain and phase error, and the gray line shows the selected phase shift states at MAG. The gray line in Fig. 4(b) shows that a 30° phase impairment affects the phase and gain control precision. The gray line is directly mapped from Fig. 4(a) and the red line is the reselected control states. After reselection, the gain of control states remains constant, but the MAG suffers from a 1.3-dB loss. The reselection procedure can also select different gain contour to utilize gain control ability.

III. Measurement Results

The die photograph of the proposed phase shifter is shown in Fig. 5. The phase shifter was fabricated with 0.13-μm SiGe bipolar complementary metal-oxide-semiconductor (BiCMOS) technology, and the total chip size is 700 μm × 900 μm including pads and seal ring. The phase shifter was tested using G-S-G probes to feed millimeter-wave signals up to 50 GHz. Off-chip FPGA and second-order passive *RC* filter are used to implement the Δ–Σ modulator and quantization noise filter. The 3.3-V power supply, current bias, control voltage, and ground are connected through bonding wires.

The control states were scanned by an automatic test program and the *S*-parameters were recorded. The program linearly scans the control voltage of the *I* and *Q* channel for 101 points for each, and a total of 10 201 states were scanned. A Keysight N5247A vector network analyzer (VNA) was used to measure the *S*-parameter of each voltage point from 18 to 50 GHz. The scanned control states were used to calibrate the *I*/*Q* control voltage and the performance of the proposed phase shifter was calculated from scanned data. The phase shifter consumes 16.5-mA current including the current mirror reference. The power consumption of the Δ–Σ modulator is negligible if the Δ–Σ modulator is implemented on-chip since it only requires about 200 logic gates and runs at 50 MHz.

The maximum gain and MAG of the phase shifter, along with the rms phase and gain error, are shown in Fig. 6. The group delay variation is less than 4.2 ps for any single

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

	This Work	[3]	[4]	[5]	[6]	[7]	[8]	[9]
Frequency (GHz)	**18-50**	15-35	26-30	36-40	28	27-42	27.5-28.35	12.5-15.7
Type	Vector Modulator	Vector Modulator	Tuned Transmission Line	DiCAD+Vector Selection	Reflection Type	Switch Type	Switch Type	Vector Modulator
Insertion loss (dB)	7.4 to 11.8	-5 to 13.5	9.3	20.2	4	<14.5	5.6 to 7.6	-
Phase resolution (°)	**1.4**	22.5	4.75	22.5	-	11.25	22.5	1.5
RMS gain error (dB)	**<0.1**	1-2.2	0.25 @28GHz	<2.6	0.2 @28GHz	<2.1	-	-
RMS phase error (°)	**<0.7**	4.2-13	0.6 @28GHz	<2.6	1.8 @28GHz	<3.8	<8.98	<1.1
Phase range (°)	360	360	190	360	210	360	360	360
Core size (mm^2)	0.20	0.19	0.18	0.3	0.67	0.395	0.23	0.18
Process	0.13μm BiCMOS	0.18μm BiCMOS	0.13μm BiCMOS	90nm CMOS	0.12μm BiCMOS	65nm CMOS	65nm CMOS	45nm CMOS SOI

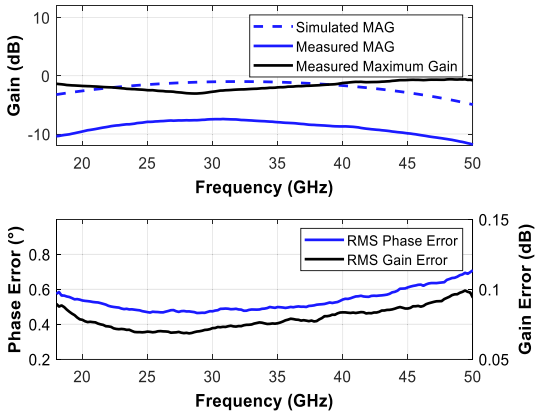

Fig. 6. Measured gain and rms error of the phase shifter.

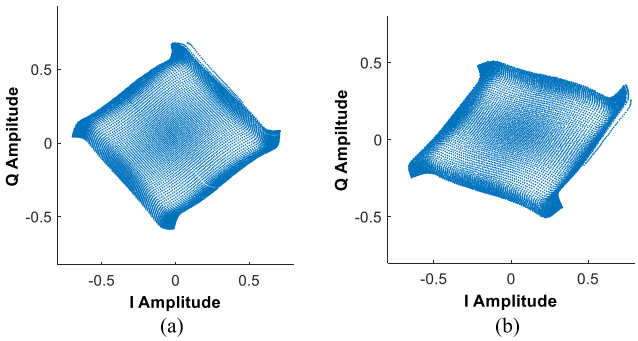

Fig. 7. Scanned phase and gain states at (a) 28 GHz and (b) 38 GHz.

calibration point. The maximum MAG loss of the proposed phase shifter is 4.4 dB, which is acceptable for an 18–50-GHz component. Fig. 7 shows the gain and phase of all 10 201 states at 28 and 38 GHz. The rms phase and gain error are calculated from 256 evenly distributed phases at MAG. Fig. 8 shows the input and output reflection coefficients of different phase and gain states and the average of all states. The output reflection is below −10 dB over the 18–50-GHz frequency range. The input reflection is lower than −10 dB below 45 GHz and still does not exceed −8 dB at 50 GHz. The dynamic range is defined as the difference between MAG and the minimum gain at each frequency, and the minimum dynamic range in 18–50 GHz is 35.5 dB, as shown in Fig. 9.

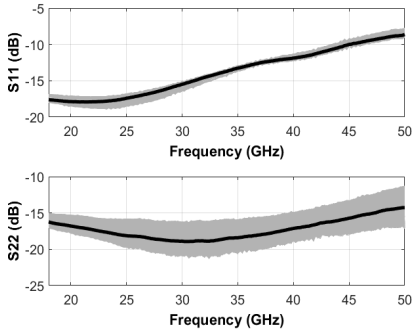

Fig. 8. Measured input and output reflection of the phase shifter.

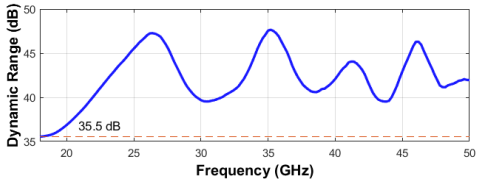

Fig. 9. Measured dynamic range of the phase shifter.

The proposed phase shifter shows excellent phase and gain control precision and low insertion loss compared with switch-type phase shifter and conventional vector-modulating phase shifter, and the area is very compact because a multiple-stage structure is not required. Table I compares the proposed phase shifter to the state-of-the-art phase shifters around 18–50 GHz.

IV. CONCLUSION

This letter presents a Δ−Σ modulated quasi-continuous digital vector-modulation phase shifter with gain control ability. Compared with switched-line phase shifters, vector-modulation phase shifters do not suffer from high insertion loss, and the area is more compact. It covers a broad frequency range of 18–50 GHz with a 7.4–11.8-dB low insertion loss, and its rms phase and gain error are lower than other reported digital controlled phase shifters. With Δ−Σ modulating scheme and digital calibration, high phase and gain control resolution can be easily achieved. The gain control ability with 35.5-dB dynamic range eliminated the VGA in the signal path, which can simplify system design and makes it suitable for system-level phased array front-end chip design.

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