

W-Band 6-Bit Active Phase Shifter Using Differential Lange Coupler in SiGe BiCMOS

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Abstract—This letter presents a W-band vector-modulator-based phase shifter with a 6-bit resolution, implemented in a SiGe:C BiCMOS technology. The phase shifter maintains the RMS amplitude and phase errors lower than 1 dB and 6.6°, respectively, for the frequency range of 86–106 GHz without digital calibration. The maximum average gain is 2.3 dB with the 3-dB bandwidth achieving 31 GHz. The circuit consumes 49 mW of power including the phase control circuitry from a 2.4-V supply voltage, 34 mW of which is used by the Gilbert cell. A novel compact differential Lange coupler is used as an IQ splitter. The core part occupies only 0.027 mm² of the chip area.

Index Terms—Millimeter-wave phase shifters, SiGe, W-band.

I. INTRODUCTION

MODERN mm-wave communication systems use very large phased arrays to achieve high precision for user detection. Analog beamforming remains frequently used nowadays, due to its power efficiency in comparison to digital beamforming. However, this trend imposes strict requirements on a phase shifter that becomes in this case the most crucial component as its performance defines the full beamforming accuracy.

At W-band frequencies, the implementation of a phase shifter becomes considerably challenging. Besides, both passive and active solutions exhibit various limitations thus making the choice between them not obvious. Passive phase shifters become smaller as the frequency increases and provide high linearity, but their losses also increase and require an additional amplification, which in turn limits the linearity compared with a fully passive implementation and increases the overall die size. High linearity is typically important for a receiving chain, since a phase shifter comes after the low-noise amplifier (LNA) and thus receives an amplified (large) signal. Various hybrid implementations and fully active phase shifters become dominant in mm-wave frequencies. Due to limited spacing between antenna elements, phase shifters have to be as compact as possible to be used in large mm-wave arrays.

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That is why in this work we demonstrate a compact solution for an active phase shifter.

In this letter, we present a differential active phase shifter for 86–106-GHz operation with a 6-bit resolution. The circuit is implemented in NXP's SiGe:C BiCMOS technology with a six-layer back end of line [1] and uses a novel differential Lange coupler as an IQ splitter, discussed in detail in Section II-B.

II. CIRCUIT DESIGN

A. Phase Shifter

The vector modulator uses a differential architecture, based on a Gilbert cell topology, formed by Q_1 and Q_2 , as shown in Fig. 1. Transistors Q_3 are used as a common-base (CB) buffer to reduce the load sensitivity of the circuit. This causes an increase in power consumption, but it is an effective solution to minimize phase and amplitude errors over frequency, while maintaining a small chip size. Components L_1 , L_2 , and C_2 form an output matching network. Decoupling capacitors are not shown in schematic but are included at the Vcc and Vb nodes. Besides, available spacing at the silicon between DC pads is used for extra DC decoupling.

The circuit operation is based on a current-steering architecture, where signals with 0°, 90°, 180°, and 270° relative phases, obtained from the differential coupler, are provided at the input. By varying V_{1-4} , one can control current steering between all Q_2 transistors and thus ensure that the required portions of each input signal (for vector summation) reach the output. This approach has the advantage of reduced linearity and amplitude variations between different phase settings in comparison to applying the control signal directly on Q_1 .

The 6-bit phase control is provided by the control circuitry consisting of Q_b , Q_{b1} in a current mirror topology. This bias network provides phase control voltages V_{1-4} and V_{BE} voltages (for Q_1) $V_{5,6}$ that remain constant for all the phase settings. Currents flowing through Q_b transistors satisfy cos and sin functions in a differential way, thus targeting constant amplitude for all the phase states in an ideal case. The control variable theta makes a full 360° circle with a step of 5.625°, reflecting the 6-bit precision.

The linearity of an active phase shifter is potentially worse than a passive variant. In this circuit, the linearity is dominated by the transconductance devices Q_1 , which are dimensioned to improve linearity. Also thanks to the CB output stage, a high simulated average output 1 dB compression point (OP_{1dB}) of 0.6 dBm is achieved at 96 GHz. The circuit exhibits the average simulated noise figure of 12.3 dB at 96 GHz.

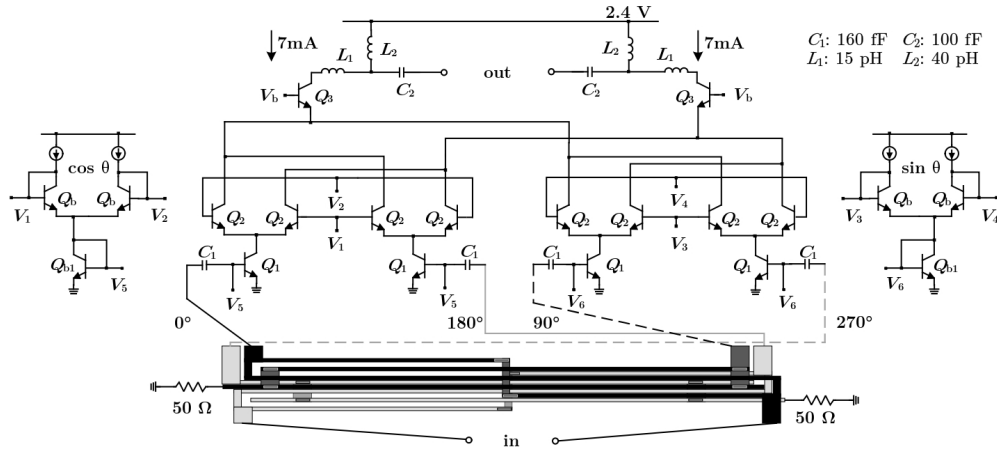


Fig. 1. Simplified schematic.

B. Differential Lange Coupler

An IQ splitter is known to be the bulkiest component of any vector modulator, occupying more than half of the overall chip area in some cases. Therefore, exploring more compact solutions remains crucial. To provide differential I and Q signals to a vector-sum phase shifter, one can use a combination of a coupler and two baluns, as in [2], [3], and [4]. Alternatively, a combination of a balun and a differential coupler can be used, as shown in [5].

This letter presents an area-efficient differential coupler (Fig. 2) built in essence by two conventional Lange couplers due to its good compromise between insertion loss, chip area, and bandwidth. However, instead of placing both the couplers in the same horizontal plane, the second coupler was placed under the first one vertically, resulting in obtaining differential operation on the same footprint. As a first step, couplers 1 and 2 were designed and optimized separately. The linewidth and spacing in coupler 1 are $3\ \mu\text{m}$, following design rules for the m6 layer. Since m1 and m6 thickness is unequal, two stacked thin layers (m1 and m2) are used for coupler 2 to partially compensate for the imbalance in ohmic losses and achieve comparable performance.

As the next design step, two couplers were placed together and optimized as one differential structure. To reduce unwanted interaction between two structures, coupler 2 was horizontally flipped relative to coupler 1, increasing the separation between input lines. In addition, the horizontal offset was introduced to increase further the distance between the lines on m6 and m2. For the same reason, only two layers are used for coupler 2. The simulation results are shown in Fig. 3.

III. EXPERIMENTAL RESULTS

The die microphotograph with radio frequency (RF) and DC pads is shown in Fig. 4. The active circuit core occupies $0.027\ \text{mm}^2$ of the chip area. The small-signal measurements have been carried out using a broadband on-wafer system with Keysight N5290A VNA in a four-port mixed mode configuration. The designed phase shifter consumes 49 mW of power including the control bias circuitry, from which the Gilbert cell itself uses 34 mW from a 2.4-V supply.

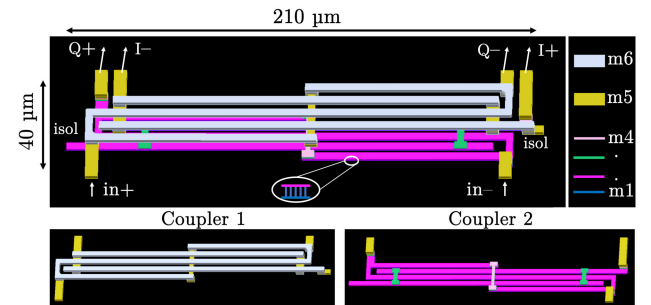


Fig. 2. Differential Lange coupler, its building blocks, and metal layers.

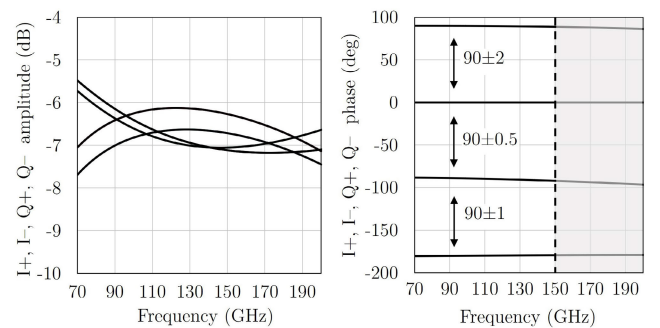


Fig. 3. IQ splitter simulation results.

Fig. 5 presents the measured gain for all the phase states and provides a comparison between the simulated and measured average gains versus frequency. The maximum average gain is 2.3 dB. The average measured gain is in good agreement with the simulated data, especially in the 92–106-GHz span. The relative phase is obtained by normalizing all the 64 measured states to one of the states and is shown in Fig. 6.

The measured frequency behavior of the amplitude RMS error (RMSE) is shown in Fig. 7. The minimum amplitude RMSE is 0.67 dB at 98 GHz, and for the frequency range 86–106 GHz, it remains below 1 dB.

The phase RMSE (Fig. 7) is calculated according to an integral nonlinearity (INL) definition, i.e., the error in comparison to an ideal set of phase values. INL RMS phase error eventually represents full accumulated phase error across all

TABLE I
PERFORMANCE SUMMARY

	Technology	Frequency, GHz	Resolution, bits	Average gain, dB	RMS gain error, dB	RMS phase error, deg	OP_{1dB} , dBm	P_{DC} , mW	Area, mm ²
[6]	130-nm SiGe	92–100	5	9.5	1.8	5	−4	31	0.82 ⁽¹⁾
[3]	130-nm SiGe	72–82	6	7	0.76	3.5	−3	60	0.31
[7]*	28-nm CMOS	80–100	6	−9	0.24	2.2	−10 ⁽²⁾	7.7	0.11
[2]	45nm SOI CMOS	57.7–84.2	5	−6	1.1	10.1	−1	17	0.11
[8]	55-nm SiGe	71–76	6	−2	0.36	2.1	−	12.8	0.38
[9]	SiGe	85–110	4	−5	1	7.5	−9 ⁽³⁾	10 ⁽⁴⁾	−
This work	SiGe	86–106	6	2.3	1	6.6	0.6 ⁽²⁾	49	0.027 ⁽⁵⁾
* calibrated	(¹)including LNA	(²)simulated	(³)calculated from $IP_{1dB} = -3$ dBm	(⁴) w/o DAC	(⁵)differential				

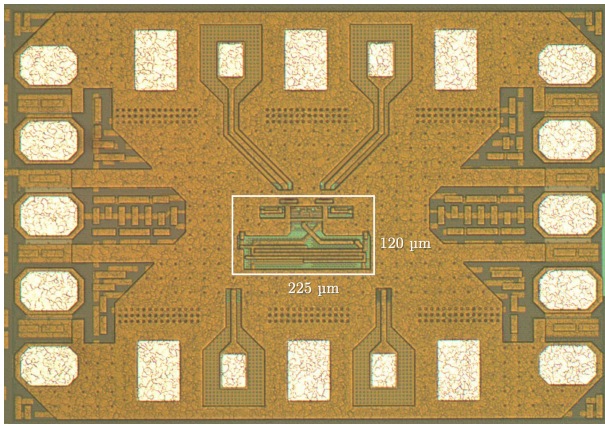


Fig. 4. Chip photograph.

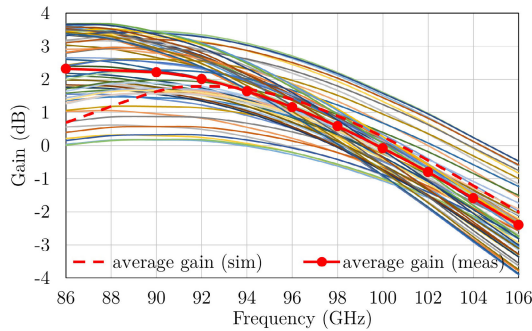


Fig. 5. Measured gain for all the phase settings with overlay of the simulated average gain.

the states and is conventionally used as the phase RMSE definition in the literature. Another definition, namely, differential nonlinearity (DNL) RMS phase error, is calculated as an average error between each state and the previous one and describes the phase shifting monotonicity. Both the metrics belong to the industrial standards in the field of mm-wave 6G systems. The presented phase shifter exhibits 6.4° of INL RMSE and remains below 6.6° at 86–106 GHz. The phase shifter has the minimum DNL RMSE of 0.98° while remaining better than 1.35° across the same frequency range. During the measurement, no additional bits for digital calibration were used, which leaves room for improvement, especially considering the flat frequency response of INL RMS phase error.

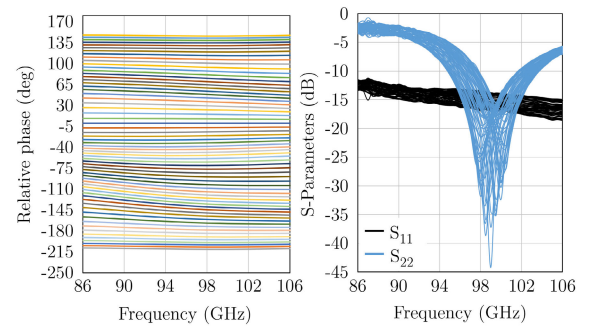


Fig. 6. Measured relative phase and return losses.

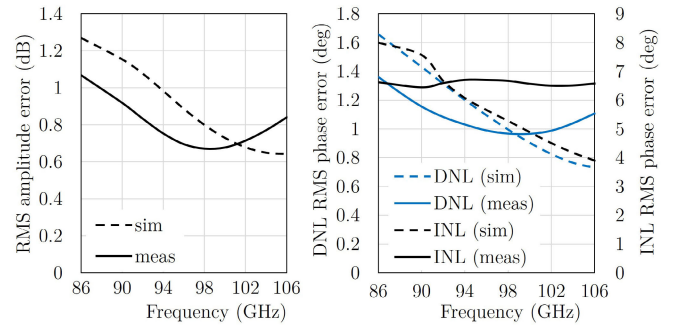


Fig. 7. Measured amplitude and phase RMSE.

IV. CONCLUSION

This letter presents a differential W-band 6-bit active phase shifter. An overview of previously published designs is shown in Table I. The vector sum phase shifter is based on a Gilbert cell topology with a CB buffer stage to reduce the performance variations between different phase settings and a compact differential coupler design to minimize chip area. The achieved RMS gain and phase errors over the wide frequency range, without trimming, are excellent. As a result of the transistors' size optimization, the circuit exhibits higher OP_{1dB} among the works listed, but at the cost of higher power consumption. To our knowledge, the presented vector modulator occupies the smallest chip area among reported W-band 6-bit phase shifters which makes it an attractive candidate for large mm-wave phased arrays.

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