# Design of X-Band GaN Phase Shifters

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***Abstract*—This paper presents two different types of high-power gallium–nitride (GaN) phase shifters designed for X-band (8–12 GHz), but offering good performance over a much wider band. The first is a 22.5° switched-filter phase shifter, which has much wider bandwidth than is typically found with this configuration, while maintaining low insertion loss (<2 dB), good return loss (>11.15 dB), and an amplitude imbalance of less than 1.03 dB across X-band. The 1-dB compression point was higher than laboratory equipment was able to measure (>38 dBm) and the phase shifter monolithic microwave integrated circuit exhibited an input-referred third-order intercept point ($IIP_3$) of 46.2 dBm. The second phase shifter is a novel design, which promises wide bandwidth (in our case, limited by the single-pole double-throw switch we have also designed), but which achieves decent insertion loss (5 dB), good return loss (better than 11 dB), and very low phase variation (1°) across X-band, also with 22.5° phase shift. It offers a 1-dB compression point of 30.1 dBm and an $IIP_3$ of 46.3 dBm. The components for a 45° differential phase shift using the same structure were also fabricated and verified with measurements. The high-power phase shifters have been fabricated in a 0.5-$\mu$m GaN HEMT process and were designed using an accurate customized switch field-effect transistor model.**

***Index Terms*—Gallium–nitride (GaN), high linearity, high power, phase shifter, switch modeling.**

## I. Introduction

PHASE SHIFTERS are important components of many systems, including phased arrays, which are of considerable interest in several key sectors. In addition, research into wide-bandgap semiconductors has progressed significantly in recent times. They now offer very high-power, compact, and low-cost phase shifters. Specifically, gallium–nitride (GaN) devices can be operated at high temperatures ($\sim$ 600 °C), high breakdown voltages ($\sim$100 V), and high current densities ($\sim$1.5 A/mm) [1]. High cutoff frequencies of 300 GHz have also been reported, demonstrating the suitability of this technology to microwave and millimeter-wave circuit design [2]. As a result, GaN is well positioned to dominate in high-power high-reliability high-frequency applications, of which there are an increasing number.

Typically, lumped-element phase shifters offer less bandwidth than distributed phase shifters. For example, bandwidths of around 20%–25% have been reported for 4- and 5-bit switched-filter phase shifters [3], [4], and bandwidths from 40% up to about an octave (67%) are achievable depending on the phase shift and acceptable error for switched high-pass/low-pass phase shifters [5]–[7]. Other examples of lumped-element phase shifters are the modified low-pass/high-pass from Ayasli *et al.* [8] and the embedded field-effect transistor (FET) topology from Bahl and Conway, which is related to the switched-filter phase shifter [9]. However, distributed structures are usually used to achieve wider bandwidths than this. For example, Schiffman phase shifters (and their derivatives) can have up to around 100% bandwidth [10]–[12]. Other distributed topologies include those based on distributed filters or stub-based structures [13]–[16] and broadside coupling of elements [17]. While these circuits offer wideband performance, they tend to be quite large, often incorporating multiple quarter-wavelength transmission lines. This is especially inconvenient when designing monolithic microwave integrated circuits (MMICs) at the lower microwave frequencies (around Ku-band and below). Some microelectromechanical systems (MEMS)-based time-delay circuits have also been presented that offer very low loss, but constant phase over a limited bandwidth [18]–[20]. More recently, broadband MEMS-based phase shifters have been reported [21]–[23], and the high bandwidth, high power handling, and improved lifetimes now available from MEMS-based switches is also very promising [21], [24]. It is worth mentioning that, to our knowledge, aside from the designs we are presenting in this paper and in our corresponding IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS) paper [25], only one other example of a phase shifter in GaN has been published [7].

This paper presents two different types of lumped GaN phase shifters, shown in Fig. 1. The first is based on a switched-filter phase shifter, examples of which are included above, although to our knowledge, none have been realized in GaN. The second is a new type of lumped-element design inspired by a distributed structure based on $\lambda/8$ resonators. The distributed version of the proposed circuit is difficult to implement for low phase shifts, requiring very high impedance transmission lines, but in our lumped-element version, this is not a problem. Furthermore, depending on the tolerance for phase error, its bandwidth may be even higher than that achievable using the distributed structure.

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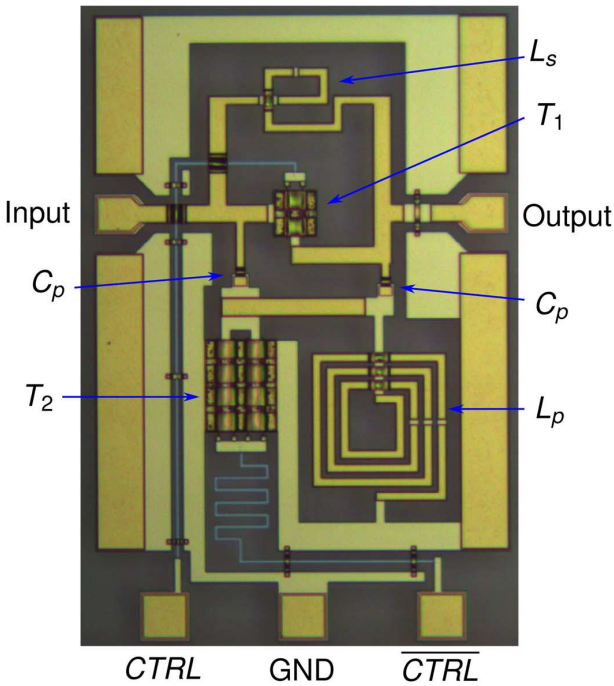
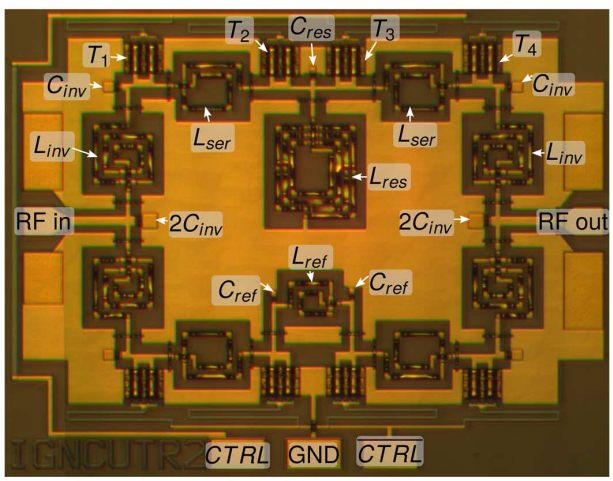



(a)




(b)

Fig. 1. Photographs of the phase-shifter circuits presented in this work. (a) Microphotograph of the $0°/22.5°$ GaN switched-filter phase shifter, also discussed in the corresponding IEEE MTT-S IMS paper [25]. Circuit dimensions are 448 $\mu$m $\times$ 678 $\mu$m (area: 0.304 mm$^2$). (b) Microphotograph of the second $0°/22.5°$ novel broadband GaN phase shifter. Circuit dimensions are 1169 $\mu$m $\times$ 900 $\mu$m (area: 1.05 mm$^2$).

In addition, a linear switch-HEMT model is used to predict the behavior and power performance of the circuits. Despite its simplicity, it has been quite useful for rapid designs. This is important when using a MMIC fabrication process, which is being actively developed.

The GaN HEMT-based designs presented can handle high power levels in a small footprint. Meanwhile, they can achieve wider bandwidth than is typically offered by similar designs, which was accomplished through careful modeling of the switching FETs. Both circuits were intended to cover X-band, although they both manage to cover a significantly larger band: 8–16 GHz for the first switched-filter design, and 7.5–14.5 GHz for the second, which is limited by an integrated single-pole double-throw (SPDT) switch, instead of the phase-shift element. The circuits responsible for producing the phase shift were also manufactured and are presented here (for $0°/22.5°$ and $0°/45°$ phase shifts). All designs are implemented in a commercially available 0.5-$\mu$m GaN process.

This paper is organized as follows. In Section II, the switching HEMT model used to design these circuits is described. In Section III, the analysis and design of the switched-filter phase shift MMIC is presented with measurement results. In Section IV, the novel resonator-based phase-shifter MMIC is detailed, including measurements. Finally, some concluding remarks are given in Section V.

## II. Switching HEMT Model

The circuits presented in this paper were manufactured by the National Research Council Canada (NRC). They operate a foundry where they are developing a 0.5-$\mu$m aluminum–gallium–nitride/gallium–nitride (AlGaN/GaN) HEMT-based MMIC process. The foundry's fabrication process currently offers transistors with an $f_t$ of 27 GHz, which are fabricated on semi-insulating 4H silicon carbide (4H-SiC) substrates. The devices are grown by ammonia molecular beam epitaxy (MBE) and are comprised of a 3-nm aluminum–nitride (AlN) nucleation layer, a 1.1-$\mu$m carbon-doped GaN insulating buffer, a 0.2-$\mu$m undoped GaN layer, a 1.5-nm AlN spacer, and 20-nm AlGaN barrier [26]. Two layers of 1-$\mu$m gold interconnects are present, and the second layer may be used to form either 100-nm metal–insulator–metal (MIM) capacitors or 1-$\mu$m air-bridges. 50-$\Omega/\square$ thin-film nichrome resistors are also available. Spiral inductors in this process typically have a measured quality factor of about 12–18, while capacitors with measured quality factors of at least 50 at X-band are attainable.

Since the foundry does not provide a transistor model suitable for designing switching circuits and our laboratory facilities are not equipped to extract accurate nonlinear models of high-power GaN devices (such as capturing thermal and trapping effects typically present in GaN devices [27], [28]), a linear model of a common-gate switch FET was extracted. The equivalent circuit of the model is shown in Fig. 2.

As with a conventional FET model, several parameters vary with bias: $C_g$, $R_i$, $R_{\rm sw}$, and $C_{\rm sw}$. As might be expected, most of the model parameters scale with FET gate width [29]. While not entirely accurate, the series inductances are modeled as varying with gate width. For large gate widths, moderate coupling between gate and drain is also included, with a coupling factor of 0.3. A comparison of the S-parameters of both the on- and off-states is shown in Fig. 3. As shown, the fit between model and measurements is quite good.

The most common figure-of-merit when evaluating semiconductor processes for switching purposes is the $R_{\rm on}\cdot C_{\rm off}$ product. The on-resistance directly affects the insertion loss, while the off-capacitance affects the isolation. Their product is constant and independent of transistor gate width. A comparison of the figures-of-merit for various technologies, including the GaN process used in this work, is shown in Table I. As shown in the table, this 0.5-$\mu$m GaN process has a relatively poor switching figure-of-merit, but the situation improves for a 0.25-$\mu$m GaN process. Small-signal performance of switches in this 0.5 $\mu$m

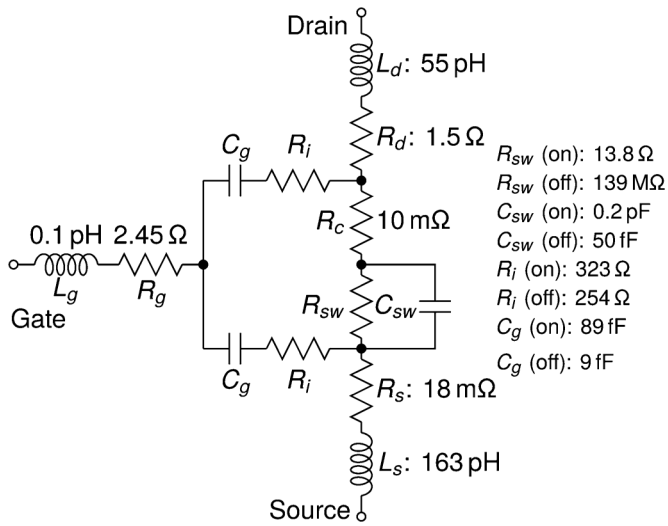



Fig. 2. Linear model used to model the switching GaN HEMT transistors. Parameters correspond to a transistor with total gate width of 160 $\mu$m and scale with gate width. $C_g$, $R_i$, $R_{\rm sw}$, and $C_{\rm sw}$ vary with gate bias as indicated.

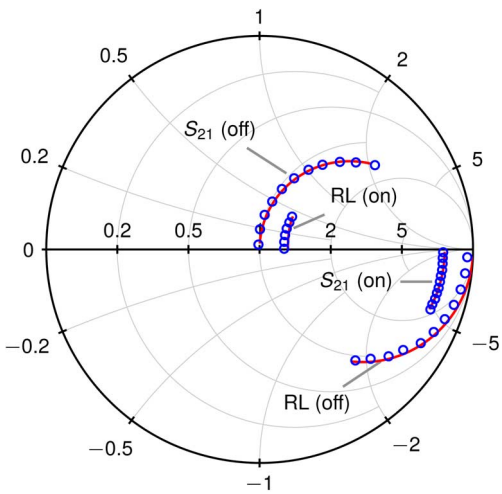



Fig. 3. Measured (lines) and modeled (circles) S-parameters (0–26.5 GHz) for a 4 × 40 $\mu$m common-gate GaN HEMT's on- and off-states.

TABLE I
SWITCHING FIGURE-OF-MERIT FOR DIFFERENT TECHNOLOGIES

| Technology | $R_{on} \cdot C_{off}$ (fs) |
|---|---|
| 0.25 μm GaAs pHEMT [32] | 145 |
| 65 nm CMOS [33] | 300 |
| 0.18 μm CMOS SOI [34] | 250 |
| 0.25 μm GaN [35] | 300 |
| 0.5 μm GaN | 690 |

will likely be worse than for a more modern GaAs or silicon process, but power handling should be significantly better due to increased breakdown voltage and current density. With evolutions in the foundry's process (currently in progress) to reduce contact resistances and gate length, the on-resistance will decrease and the figure-of-merit will improve.

Meanwhile, several factors contribute to an enormous power-handling advantage for GaN switches (and phase shifters) over conventional technologies. The wide bandgap of GaN (3.4 eV) is much larger than silicon (1.12 eV) and gallium arsenide (1.42 eV). Its breakdown field (2 MV/m) is also much greater than those of silicon (0.3 MV/m) and GaAs (0.4 MV/m) so operating voltages can be much higher. Furthermore, since a silicon carbide substrate is used with a very high thermal conductivity, it is easier to avoid overheating problems. As a result, a GaN device may dissipate in excess of 5 W/mm [30], approximately five times higher than GaAs [31] and even more than silicon.

A complete nonlinear model is preferred when designing power circuits, but a simple linear model such as this one can be useful in estimating the power-handling capability of a circuit. The model presented can be easily integrated into the full circuit simulation, and the voltages across the transistor's terminals and the current through the device can be determined using a linear ac analysis available in virtually all simulators. As long as the input RF power does not induce a voltage swing across the transistor's terminals that reaches the transistor's pinch-off voltage or breakdown voltage, the switch-based circuit should function largely as predicted from a linear S-parameter analysis. This type of analysis is performed and illustrated in the following sections.

This simulation does not lend itself well to a quantitative prediction of the 1-dB compression point $(P_{1\ \rm dB})$ or third-order input-referred intercept point $(\rm IIP_3)$. However, it does provide a designer with some useful information on the power-handling capability of the circuit, which can be refined once a large-signal model can be extracted, or when measurements are performed.

## III. SWITCHED-FILTER PHASE SHIFTER

Switched-filter phase shifters have found use when compact circuits are desired [3], [4]. This topology requires less chip area than other phase-shifter circuit topologies, such as switched high-pass/low-pass, switched-line, and distributed (i.e., Schiffman) phase shifters, although bandwidth is typically reduced. An advantage is that the phase performance of the circuit is independent of the loss and phase variations introduced by lossy transmission lines and routing schemes.

The switched-filter phase shifter switches between a filter (typically low pass, although a high-pass filter could also be used), offering the desired phase shift, and a bypass state (i.e., an all-pass network), with ideally zero insertion phase. The circuit schematic, using FETs as switches, is shown in Fig. 4.

It should be noted that in Fig. 4, a low-pass Π topology is adopted. This configuration is advantageous since only one inductor is required. Since inductors typically have higher loss and occupy much more substrate area than capacitors, this topology should be more compact and less lossy than the low-pass T network (which has two inductors). The low-pass Π network also requires smaller inductors than the high-pass T network (also with one inductor).

Performing an analysis similar to that detailed in [5] of the circuit using the low-pass network's $ABCD$ matrix, the insertion phase of the filter is

$$\phi = \tan^{-1}\left(\frac{2B_n + X_n - B_n^2 X_n}{2B_n X_n - 2}\right). \quad (1)$$

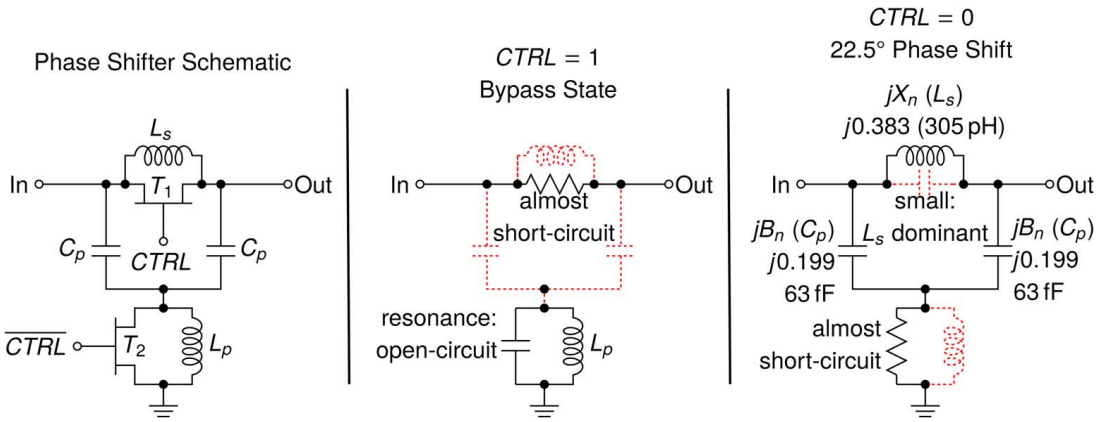



Fig. 4. Schematic of the switched-filter phase shifter and the conceptual equivalent for CTRL $= 1$ ($V_{\mathrm{CTRL}} = 0$ V) and CTRL $= 0$ ($V_{\overline{\mathrm{CTRL}}} = -10$ V). The dotted components have a negligible effect for the given phase state.

For a lossless matched network, $B_n$ and $X_n$ (and therefore, $C$ and $L$) are determined to be

$$B_n = \tan\frac{\phi}{2} \quad \Rightarrow \quad C = \frac{\tan\frac{\phi}{2}}{\omega_0 Z_0} \tag{2}$$

and

$$X_n = \sin\phi \quad \Rightarrow \quad L = \frac{Z_0 \sin\phi}{\omega_0}. \tag{3}$$

To realize the phase shifter, the values of $B_n$ and $X_n$ for a 22.5° phase shifter were found using (2) and (3) and they are shown in Fig. 2. The corresponding values of $C$ and $L$ were then calculated for a 50-Ω system. The circuit was designed for the flattest phase response over a frequency range of 8–12 GHz, a bandwidth of 40%. The circuit was optimized to maintain a return loss better than 10 dB across this frequency range.

Transistor $T_1$ has a total gate width of 80 $\mu$m (two fingers), while $T_2$ has a total gate width of 400 $\mu$m (four fingers). The gate bias resistors were selected to be at least 5 kΩ, although circuit performance is not sensitive to the precise value. A smaller resistor would allow for a faster switching speed at the expense of RF performance.

The phase-shifter circuit was fabricated in the GaN MMIC process developed at NRC, which was described earlier. Fig. 1(a) shows a photograph of the manufactured circuit. The circuit was simulated in Agilent Technologies' Advanced Design System (ADS) and Momentum was used to model the passive circuitry. The circuit was designed to provide 0°/22.5° of phase shift over a frequency range of 8–12 GHz.

Fig. 5 shows the insertion loss of the phase shifter in both phase states (bypass, i.e., no phase shift, and in the phase-shift state) with very good agreement between simulations and measurements. Switching is accomplished by biasing the gates of the two transistors. CTRL $= 0$ is achieved by applying a voltage of $-10$ V. CTRL $= 1$ corresponds to an applied gate voltage of 0 V. Power handling could likely be improved by applying a voltage lower than $-10$ V, but there were concerns about transistor breakdown, which the foundry reported was a problem at lower than expected voltages. Our understanding is that the foundry has identified the source of this problem and it will be corrected in the future.

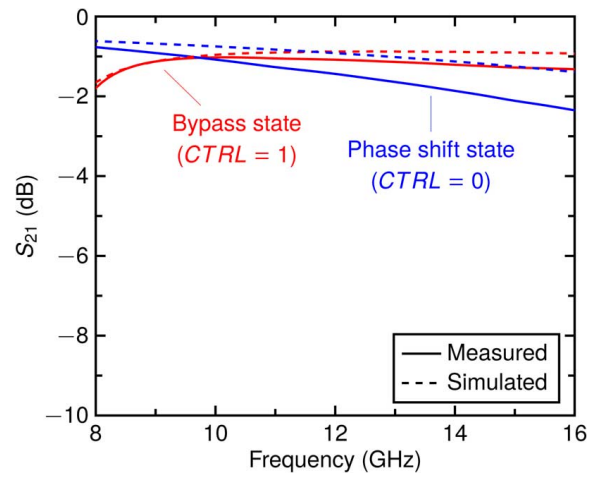



Fig. 5. Measured and simulated insertion loss of the 0°/22.5° phase shifter.

As Fig. 5 shows, the measured insertion loss is better than 2 dB across X-band, and is better than 3 dB across a wider range of 8–16 GHz. The amplitude imbalance between the two states is worst at 8 GHz, and is therefore better than 1.03 dB over the extended band from 8 to 16 GHz.

The return loss for both phase-shift states can seen in Fig. 6. Again, the simulation results and measurements are in good agreement. The measured return loss is better than 11.15 dB across X-band, and is better than 10.2 dB from 8 to 16 GHz. Therefore, an effective compromise between bandwidth, return loss, and insertion loss can be found for this traditionally narrowband (but compact) circuit configuration.

Fig. 7 presents the phase shift obtained from the circuit. Although the measured phase shift is slightly less than simulations predict, the measured phase shift is flat over a large bandwidth. The measured phase response is also flatter than simulations predicted. Since the device model shown in Fig. 3 was scaled from the original gate width of 160 $\mu$m to the actual transistor sizes used in the design (400 and 80 $\mu$m), it is possible the model used in simulation and the final manufactured device are not in perfect agreement. In particular, the parasitic inductances generally do not scale linearly with geometry [29], while in our model, they do. The coupling between gate and drain is also geometry dependent, while in this model, it is fixed.

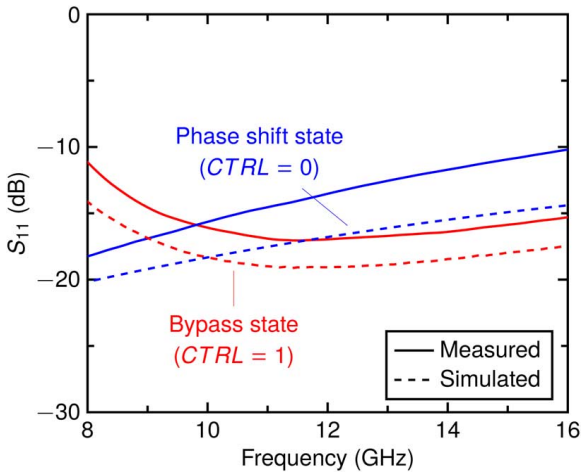



Fig. 6. Measured and simulated return loss for the phase-shifter circuit.

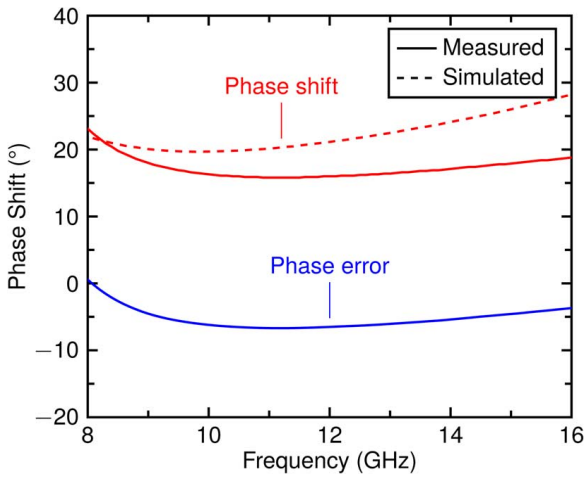



Fig. 7. Measured and simulated phase shift for the 0°/22.5° phase shifter.

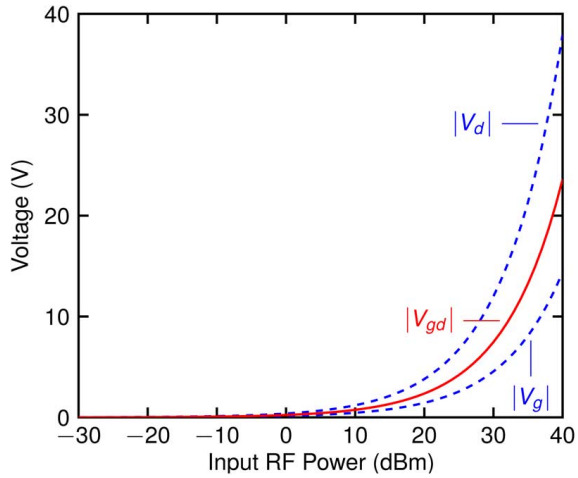



Fig. 8. Simulated voltages on the terminals of the worst case transistor, $T_2$, in the phase-shift state. The source of this transistor is grounded so $V_s$ is not shown.

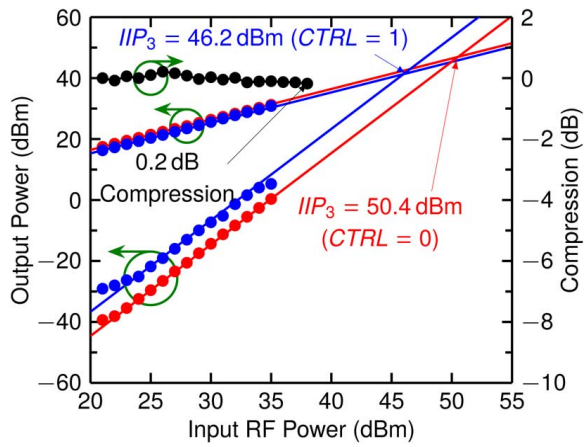



Fig. 9. Linearity measurement (gain compression and third-order intermodulation) results for the phase shifting circuit.

The phase response is also sensitive to the value of $C_p$. A variation of about 20% in this capacitance leads to a 5° decrease in phase shift in simulation. Since these capacitors are quite small ($14\ \mu\text{m} \times 10\ \mu\text{m}$), a variation of $2\ \mu$m in each dimension or a variation in the dielectric thickness could be responsible for the observed phase error. Some small error between the electromagnetic simulation and the realized passives is also expected (particularly inductors). This is likely responsible for the flatter and offset phase response, especially coupled with manufacturing tolerances, which are expected with a new fabrication process under active development. The difference between the measured phase and design target (approximately 5°) could be corrected in a future iteration.

For this circuit, the 5% phase variation bandwidth is found to be 46% (centred around 17°), wide enough to cover X-band. A 10% phase variation definition yields 64% bandwidth, covering 8–16 GHz.

Finally, the linearity and power-handling capability of the circuit were studied. To get an idea of the type of input the circuit can handle, the method described in Section II was used to calculate voltage swing across the terminals of each transistor in both the phase-shift and filter bypass states. The voltages as a function of input power is shown in Fig. 8 for the transistor exhibiting the largest swing, which is $T_2$ in the phase-shift state (i.e., when $T_2$ is off). As shown, the input power level can rise to about 32 dBm before the transistor starts to turn on. The current at this power is below the maximum level the transistor can support.

The measurements results of this study are shown in Fig. 9. Due to the limitations of the laboratory equipment available, these tests were performed at 8 GHz with a 10-W power amplifier. For the purposes of determining the third-order intercept point, a second signal at an offset of 1 MHz was used.

The power-handling capability indicated is better than the linear simulation showed. This could be due in part to the nonlinearities of the transistor providing an advantage. Of course, variations between the model and the fabricated devices could also play a role since the foundry was actively developing their process at the time. Due to space constraints, it was not possible to include extra transistors (for modeling purposes) with this design.

The third-order intercept test was performed for both phase states (0° and 22.5°), as shown. With the 0° (bypass) state, the

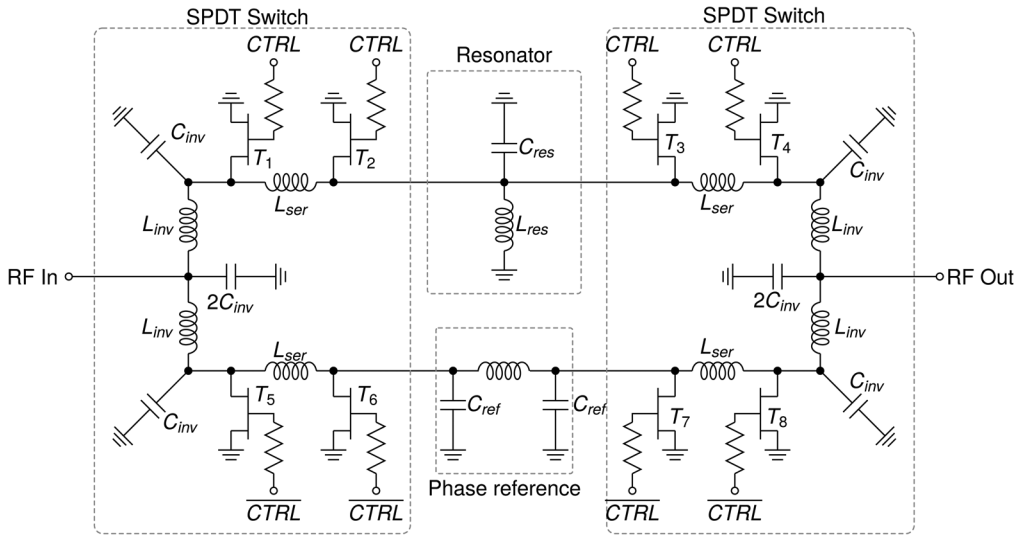



Fig. 10. Schematic of a new type of lumped-element phase shifter.

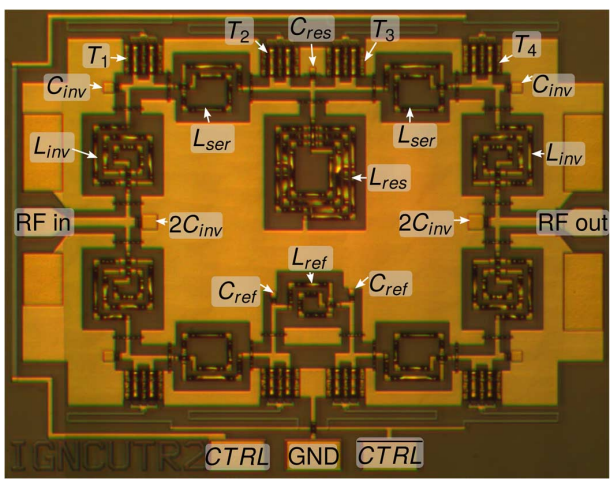



Fig. 11. Microphotograph of the second 0°/22.5° broadband GaN phase shifter. Circuit dimensions are 1169 $\mu$m × 900 $\mu$m (area: 1.05 mm$^2$).

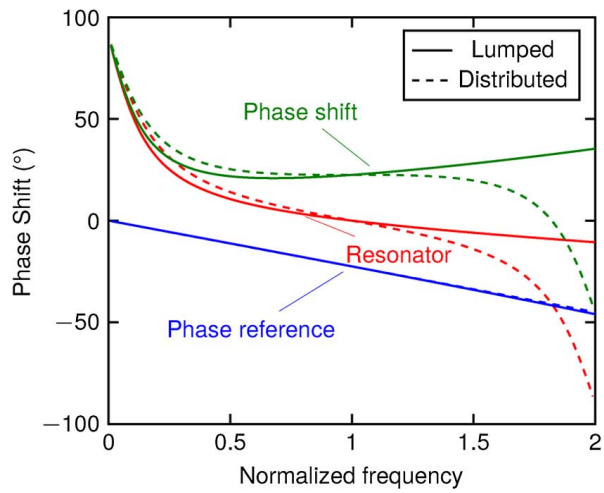



Fig. 12. Comparison of theoretical phase shift versus frequency for the distributed and lumped circuits.

measured IIP$_3$ was 46.2 dBm (determined by extrapolating the 1- and 3-dB/dB curves found from measurements). The 22.5° phase-shift state had a higher IIP$_3$ of 50.4 dBm.

An attempt to determine the 1-dB compression point was made. With the equipment available in the laboratory, it was not possible to observe 1-dB compression, as shown with CTRL = 1 in Fig. 9 (similar compression behavior was observed for CTRL = 1). At 38 dBm of input RF power, only 0.2 dB of gain compression was observed, relative to a reference input power of 21 dBm. It is likely that the 1-dB compression point is a little over 40 dBm.

## IV. Novel Broadband Resonator-Based Phase Shifter

A separate investigation of GaN phase shifters resulted in a novel lumped phase-shifter topology. This circuit is based on a distributed switched-resonator design. This phase shifter offers wide bandwidth, although its power-handling capability is not quite as high. Fig. 10 shows the topology of the phase shifter, while Fig. 11 shows a photograph of the fabricated MMIC.

### A. Phase-Shifter Design

The phase shift is achieved using a shunt *LC* resonator. Its parameters are derived from analyzing two parallel $\lambda/8$ open- and short-end stub resonators. This type of network bears some similarity to that presented in [13], though there are considerable differences in the analysis and the implementation of that design would be challenging for smaller phase shifts, such as 45° or smaller, as will be shown. The combination of parallel short and open $\lambda/8$ resonators yields an equivalent admittance of

$$Y_{eq} = \frac{j(\tan^2\theta - 1)}{z_0 \tan\theta} = \frac{2}{jz_0 \tan 2\theta} \tag{4}$$

which shows their equivalence to a shorted quarter-wave stub with the characteristic impedance halved. The phase shift relative to a phase reference, such as a transmission line, is found by determining the insertion phase ($\angle S_{21}$) of the network and is

$$\Delta\phi = \phi_{\text{ref}} + \tan^{-1}\left(\frac{1}{z_0 \tan 2\theta}\right). \tag{5}$$

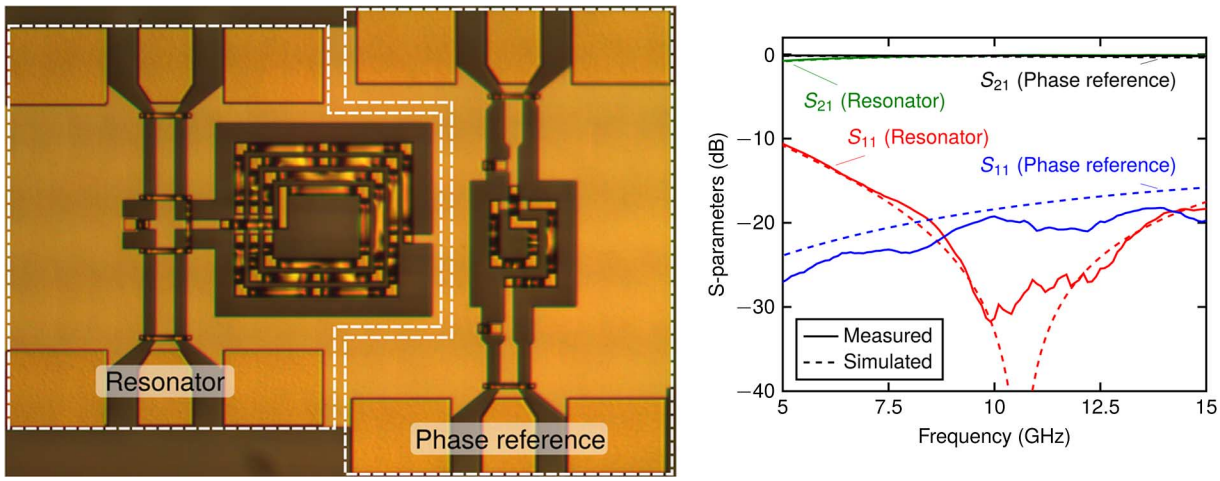



Fig. 13. Measured and simulated S-parameters for the resonator and 22.5° phase reference. (a) Photograph of resonator and phase reference. Dimensions: 436 $\mu$m × 693 $\mu$m. (b) S-parameters of the differential phase shifter.

Since a flat phase shift over frequency is typically desired, the electrical length ($\theta = \pi\omega/4$) of the resonators is substituted. Next, the derivative with respect to frequency is set equal to zero. Solving, the following simple relationship for a normalized frequency $\omega = 1$ is obtained:

$$z_0 = \frac{\pi}{2\phi_{\rm ref}} \tag{6}$$

where $\phi_{\rm ref}$ is the desired phase shift.

Knowing the optimal normalized impedance $z_0$ for a desired phase shift, a parallel $LC$ resonator may be synthesized to achieve an optimal response. At higher frequencies, this relationship would also allow for the distributed resonator(s) to be designed. For completeness, the parallel $LC$ resonator will consist of

$$L_{\rm res} = \frac{Z_0 z_0}{\omega} \tag{7}$$

$$C_{\rm res} = \frac{1}{\omega Z_0 z_0} \tag{8}$$

where $z_0$ is the normalized optimal impedance found using (6) and $Z_0$ is the actual system impedance (e.g., 50 Ω). The desired phase shift only affects the impedance of the resonator, not its electrical length. In this situation, where a 22.5° phase shift is desired, $C_{\rm res} = 80$ fF and $L_{\rm res} = 3.2$ nH.

It must also be noted that for small phase shifts, the characteristic impedance needed for a distributed structure can be quite high. For example, a 22.5° phase shift would require $z_0 = 4$, which requires transmission lines with an impedance of 200 Ω, which are not readily implemented using microstrip or coplanar waveguide. However, a lumped implementation of its equivalent is not particularly challenging at X-band.

The phase reference can be realized as a simple transmission line, or at lower frequencies, as a lumped-element equivalent. For practical purposes and since lumped elements still work well at X-band, we have used a standard Π network, as shown in Fig. 10. A T network would also work, albeit with two inductors, occupying more space and having higher loss. Values for

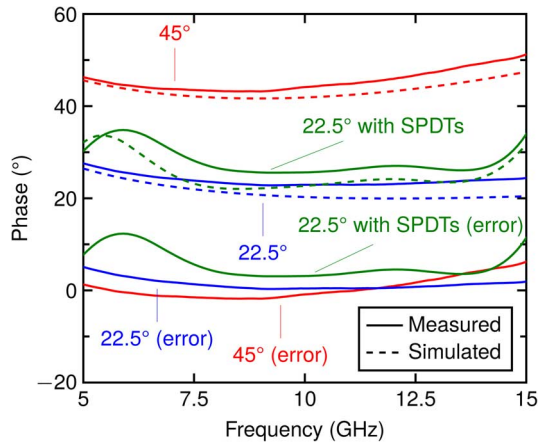



Fig. 14. Phase shift and phase error for the separate 22.5° and 45° phase shifters, as well as for the complete 22.5° phase shifter with SPDT.

the inductor and capacitors are derived from making the equivalence between the $ABCD$ matrix of the lumped network and a transmission line. Again, for completeness, we have used

$$L_{\rm ref} = \frac{Z_0 \sin\phi_{\rm ref}}{\omega} \tag{9}$$

$$C_{\rm ref} = \frac{1 - \cos\phi_{\rm ref}}{\omega Z_0 \sin\phi_{\rm ref}}. \tag{10}$$

The inductance of the reference network is $L_{\rm ref} = 305$ pH and the capacitance is $C_{\rm ref} = 63$ fF.

Since a lumped approach to the implementation of this phase shifter is used, it is also interesting to compare it with the initial idea with $\lambda/8$ short and open stub resonators. Fig. 12 shows this comparison. As shown, the lumped-element version exhibits a similar bandwidth, although its phase shift is not quite as flat at the center frequency. However, depending on the phase error allowed, it may be even more broadband than the distributed network.

Fig. 13 shows the measured and simulated S-parameters of the reference state and $LC$ resonator to achieve a $0°/22.5°$ phase shift, while Fig. 14 shows the phase shift and phase error. As

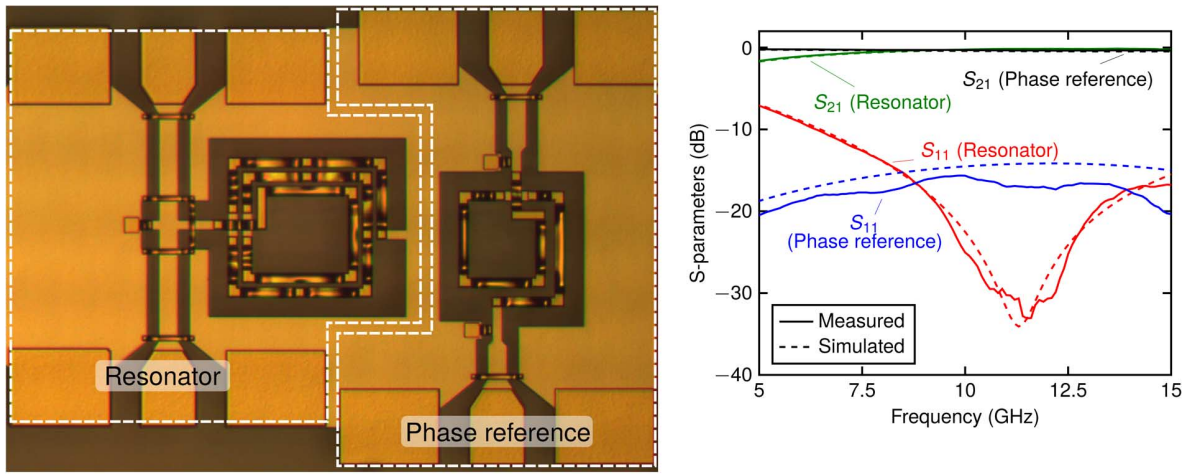



Fig. 15. Measured and simulated S-parameters for the resonator and 45° phase reference. (a) Photograph of resonator and phase reference. Dimensions: 434 $\mu$m × 691 $\mu$m. (b) S-parameters of the differential phase shifter.

shown, the measurements agree quite well with the simulations. The passive circuitry was simulated using Agilent's Momentum solver. Using a standard 5% definition for phase variation and return loss better than 10 dB, the circuits would operate well from 6.3 to 16.2 GHz (88% fractional bandwidth), although the measured phase shift is slightly higher than expected. In fact, the minimum phase shift is 22.5°. The circuit could be tuned to be centered on this desired phase shift.

As a further example, the design technique was also verified with the design of $0^\circ/45^\circ$ phase-shift elements. Fig. 15 shows a photograph of these circuit and the measured S-parameters associated with it and Fig. 14 shows the phase shift and phase error. Due to limited die area, it was not possible to integrate an SPDT switch to alternate between the two phases for this 45° phase shifter. As shown in the figure, measurements are in good agreement with simulations. The bandwidth of the $0^\circ/45^\circ$ differential circuit, bounded by the range where there is less than 5% phase variation and return loss better than 10 dB, is from 6.4 to 13.2 GHz (69% fractional bandwidth).

### B. SPDT Switch Design

Since the desired phase shift is achieved by switching between the resonator and the phase reference, switches are also required. To this end, a lumped SPDT switch is also proposed here. Like the actual phase shift, the switch was inspired by distributed design techniques. Its schematic is shown in Fig. 10.

Two shunt transistors, each 240-$\mu$m wide (four fingers), are used in each arm of the SPDT switch. Their off-capacitances (75 fF each, as calculated from the scalable model in Fig. 3) are absorbed into an artificial transmission line using $L_{\rm ser}$. Real transmission lines have been used in switch designs in the past, as parasitic capacitances are absorbed into the network with limited effect on bandwidth and loss [33], [36], [37]. In this lumped-element circuit, $L_{\rm ser}$ is sized to provide an impedance of 50 Ω to the network, using the usual relationship, $Z_0 = \sqrt{L/C}$. Therefore, $L_{\rm ser}$ is found to be 188 pH. The off-capacitance of each device is proportional to its size, and a capacitance (andtransistor), which is too large, will limit the bandwidth of the switch because the pole of the resulting network is at $\omega = 1/\sqrt{L_{\rm ser}C_{\rm off}}$. On the other hand, a transistor that is too small (which might otherwise be good for achieving a wide bandwidth due to its smaller off-capacitance) will have a higher on-resistance, limiting the isolation of the switch. In this case, the transistors were sized to accommodate the bandwidth of the circuit and no smaller (as mentioned above, the devices used have four fingers, each 60-$\mu$m wide). This ensures a good compromise between bandwidth and isolation. In this circuit as well, gate resistors of at least 5 kΩ were used.

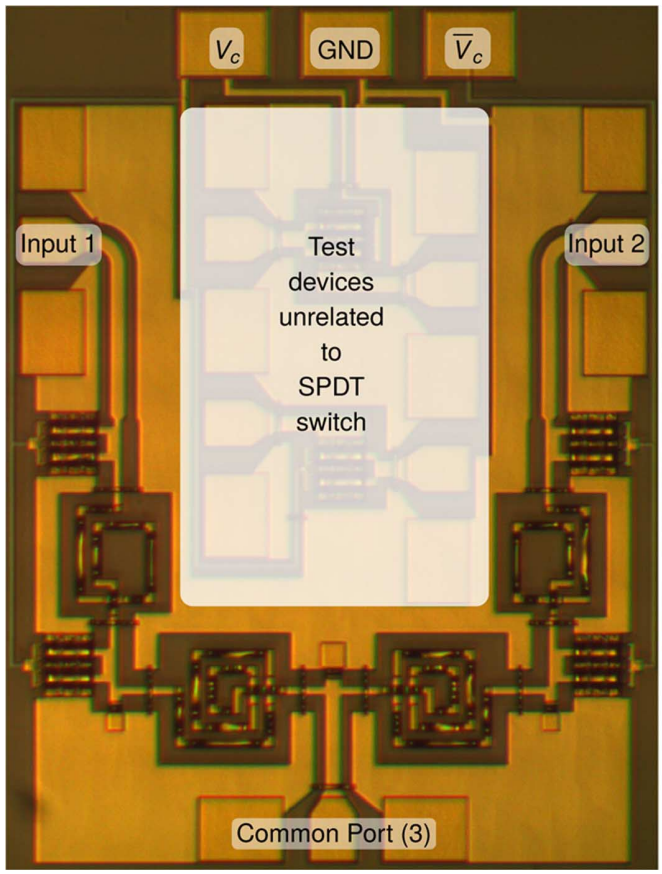
Since these two shunt transistors will provide a short circuit, a lumped impedance inverter is used to rotate the impedance 180° around the Smith chart so that an open circuit is seen at the RF input and output. This impedance inverter is realized in the same manner as the reference line for the phase shifter, where $Z_0 = 50\ \Omega$ and $\phi = \pi/2$ in (9) and (10). The inverter is represented in Fig. 10 by $L_{\rm inv}$ and $C_{\rm inv}$. Here, $L_{\rm inv}$ is calculated to be 798 pH and $C_{\rm inv}$ is 318 fF.

The SPDT switch's isolation, insertion loss, and return loss are shown in Fig. 16. As shown, all three parameters are in good agreement with simulations, with insertion loss better than 2.9 dB (0.5 dB below its peak), return loss better than 10 dB, and isolation better than 22 dB over a frequency range from 6.6 to 13.6 GHz. In this case, the SPDT switch (specifically its return loss) will be the limiting factor in the bandwidth of the phase shifter, but it does allow for X-band to be comfortably covered.

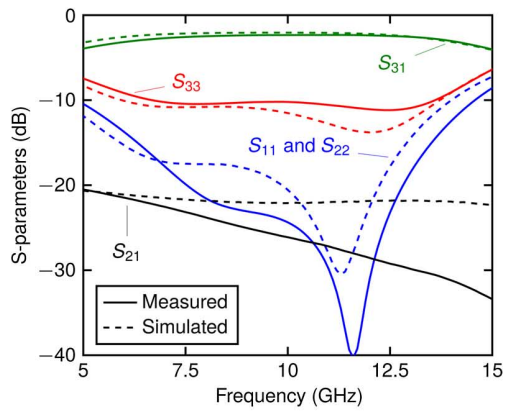
### C. Phase-Shifter Results

A $0^\circ/22.5^\circ$ phase shifter incorporating all elements, including the SPDT switch, was fabricated using the same 0.5-$\mu$m AlGaN/GaN HEMT process, as described earlier. The phase-shift elements (phase reference and resonator) and the SPDT switch were also fabricated separately for verification purposes, which were presented earlier. This completely integrated phase shifter is shown in Fig. 11.

With all components combined, the complete phase-shift circuit was measured. The insertion loss, return loss, and the phase shift achieved by the complete circuit are shown in




(a)




(b)

Fig. 16. Measured and simulated isolation, insertion loss, and return loss for the proposed SPDT switch. (a) Photograph of the SPDT switch. Some test structures, unrelated to the SPDT switch, are in the center. Dimensions (including pads and access lines): 1038 $\mu$m $\times$ 787 $\mu$m. (b) S-parameters of the SPDT switch.

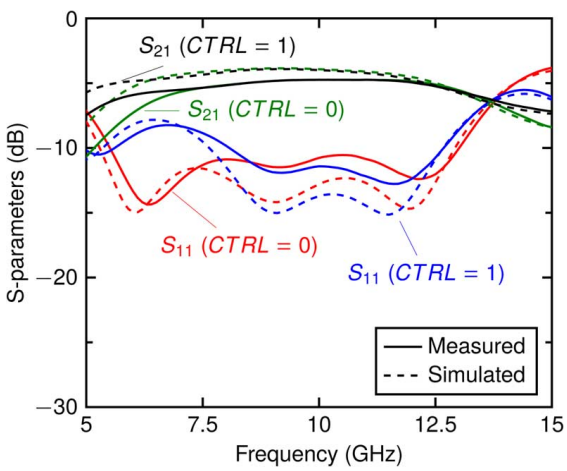



Fig. 17. Insertion loss, return loss, and phase shift for the complete 0°/22.5° phase shifter shown in Fig. 11.

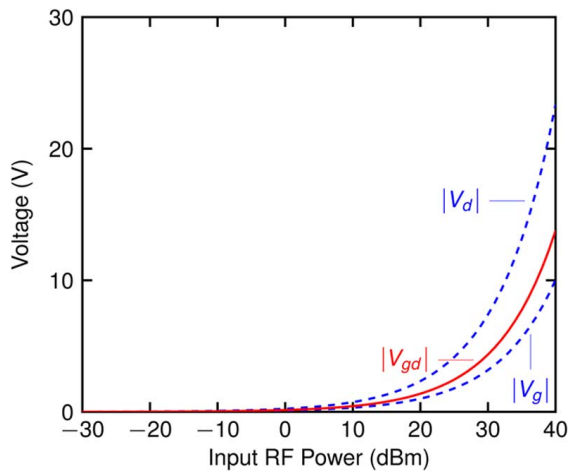



Fig. 18. Simulated voltages on the terminals of the worst case transistor, $T_1$, with CTRL $= 0$. The source of this transistor is grounded so $V_s$ is not shown.

Fig. 17. Again, there is very good agreement between measurement and simulation. The 5%-variation phase-shift bandwidth is 7.5–14.5 GHz, although it is not perfectly aligned with the return loss (better than 10 dB from 5.6 to 13 GHz) and insertion loss. The slight error in phase shift (3°) could be corrected in a future iteration of the design to achieve exactly 22.5° of phase shift.

Over X-band, the phase shifter offers return loss better than 11 dB, insertion loss better than 5 dB, and phase variation of 1° across the band. Since the circuit is nearly symmetrical, these parameters have negligible variation when switched between the reference state and the phase-shift state.

The power-handling analysis discussed earlier was also performed for this circuit. The limiting transistor is $T_1$ when CTRL $= 0$ (or $T_5$ when CTRL $= 1$). This analysis, with data shown in Fig. 18, indicates that the phase shifter ought to be able to handle about 30 dBm, with the maximum current of the transistor not being a factor. The measured results, shown in Fig. 19 confirm this prediction, with an input-referred $P_{1\,\mathrm{dB}}$ of

TABLE II
COMPARISON WITH A SELECTION OF OTHER PHASE SHIFTERS

| Ref. | Type | Bandwidth (GHz / %) | Phase error (°) | Insertion Loss (dB) | Return Loss (dB) | Size ($mm^2$) | Power handling (dBm) |
|---|---|---|---|---|---|---|---|
| [7] | 45° high-pass/low-pass | 8–12 (40 %) | 10 | 2.5 | 10 | 4 | $P_{1\,dB}$: 38 |
| [8] | 2-bit high-pass/low-pass | 2–8 (120 %) | ≈ 30 | 6 | 10 | 8.16 | $P_{1\,dB}$: 30 |
| [9] | 4-bit high-pass/low-pass and switched-filter hybrid | 1.4–2.4 (53 %) | 3 | 3.5 | 10 | 2.6 | $P_{1\,dB}$: 30<br>$IIP_3$: 32 |
| [13] | 45° loaded transmission line | 2–6 (100 %) | 6 | 2.1 | 10 | — | — |
| [15] | 90° loaded transmission line | 2.4–5.6 (82 %) | 6.4 | 0.6 | 10 | — | — |
| [16] | 90° broadside coupling | 3–7 (82 %) | 4 | 2.7 | 12.5 | ≈ 165 | — |
| [17] | 30°/45° broadside coupling | 3.1–10.6 (109 %) | 2.5/2.3 | 1 | 10 | 500 | — |
| [21] | 5-bit MEMS | 8–12 (40 %) | 10 | 4.5 | 10 | 9.2 | — |
| [22] | 4-bit MEMS | 12–18 (40 %) | 7 | 1.7 | 15 | — | — |
| This work | 22.5° switched-filter | 8–16 (67 %) | 5.2 | 2 | 11.15 | 0.304 | $P_{1\,dB}$: ≈ 40<br>$IIP_3$: 46.2 |
| This work | 22.5° LC resonator | 7.5–13 (54 %) | 5.63 | 5 | 11 | 1.05 | $P_{1\,dB}$: 30.1<br>$IIP_3$: 46.3 |
| | | No SPDT: 6.3–16.2 (88 %) | 2.83 | 0.45 | 13.9 | | |
| | 45° LC resonator | No SPDT: 6.4–13.2 (69 %) | 2.86 | 0.9 | 10 | | |

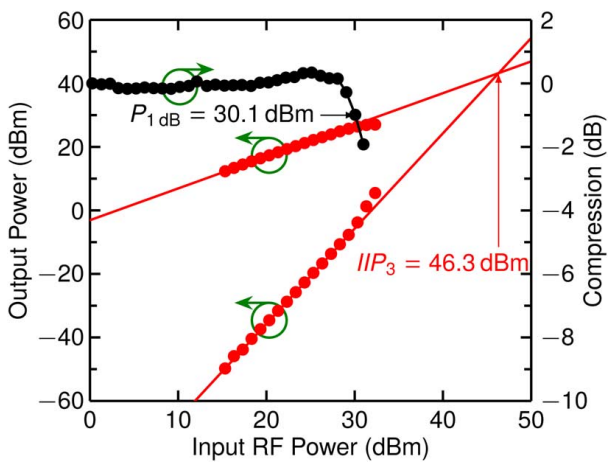



Fig. 19. Measured power handling ($IIP_3$ and compression) of the complete 0°/22.5° phase shifter. The power handling is the same for both states.

30.1 dBm and $IIP_3$ of 46.3 dBm. The separate SPDT switch shows similar performance, with $P_{1\,dB}$ of approximately 31 dBm and $IIP_3$ of 47 dBm when measured. This is expected, as the power handling of the phase shifter is dominated by the power handling of the switch at the input of the phase shifter.

## V. CONCLUSIONS

In this paper, two broadband compact high-power 0°/22.5° phase shifters were presented. One phase shifter is based on a switched-filter topology, while the other new lumped-element design is based on a resonator and phase reference. Both were implemented in a 0.5-$\mu$m AlGaN/GaN process.

The design of both phase shifters has been described, and simulation results agree with measurements, with the first design having insertion loss below 2 dB, return loss better than 11.5 dB, and amplitude imbalance less than 1.03 dB across X-band. The second design offers insertion loss around 5 dB, good return loss (11 dB), decent insertion loss (5 dB), and very low phase variation (1°) across the same band.

Both designs offer good performance over a wider band, with the first operating well over 8–16 GHz and the second over 7.5–13 GHz. The second design is limited by the bandwidth of the SPDT switch, the differential phase shifter alone (excluding the effect of the switch) works over 6.3–16.2 GHz.

We have only presented 0°/22.5° phase shifters and the phase shift circuity for a 0°/45° phase shift in order to demonstrate the design concept and its feasibility. However, the design procedure presented here could be used to design circuits with an arbitrary phase shift and cascaded to obtain full 360° coverage.

Also of particular interest, the power-handling capability of the circuits was shown to be very high. The first design having what we estimate to be a $P_{1\,dB}$ of over 10 W, and the third-order intercept point was determined to be near 50 dBm. The second design has a somewhat lower power-handling capability with a third-order intercept point of 46 dBm and $P_{1\,dB}$ of about 30 dBm.

A comparison of these phase shifters with some others found in the literature is shown in Table II. When reading this table, one should be aware that some authors use different definitions

for bandwidth. The table shows the bandwidth as given in the respective papers. In addition, many studies have not included a way to switch between the reference and phase-shift states (such as SPDT switches). For the first phase shifter presented in this paper, the switch is an integral part and cannot be removed, but for the second phase shifter, the bandwidth without the SPDT switches is included to facilitate more equal comparisons.

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