A K-Band 5-Bit Digital Linear Phase Rotator with Folded Transformer Based Ultra-Compact Quadrature Generation

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***Abstract* — This paper presents a K-band 5-bit vector modulator phase rotator. A fully differential based on a 6-port folded transformer I/Q generation passive network generates the quadrature signals at K-band with low loss, wide bandwidth and high precision, all within an ultra-compact foot-print; this makes the phase rotator design especially suitable for large-scaled high-density phased array systems. Two linear digital VGAs scale the quadrature signals to achieve the desired vector phase interpolation. As a proof-of-concept design, we implement the phase rotator in a SiGe BiCMOS process within a compact chip area of only 310 µm by 380 µm. It achieves -3 dB bandwidth of 6 GHz at the center frequency of 23.5 GHz. The maximum RMS phase error is only 2° for phase interpolation over the full 360° phase span. It consumes 4 mA from 2.5 V and the measured P_{1dB} and IIP_3 are -16 dBm and -5.5 dBm, respectively. Leveraging the dense phase interpolation points to calibrate undesired I/Q mismatch is also demonstrated, which shows the robustness of the design.**

***Index Terms* — K-band, mismatch calibration, phase rotator, quadrature generation, transformer.**

I. Introduction

With the continuous scaling in silicon processes, integrating the entire phased array system on one single silicon chip has gained much interest recently. Such integrated phased array systems offer superior performance over single-element transceivers, including signal to noise ratio (SNR) enhancement, spatial-filtering, beam-steering, and spatial power combining. The phase rotator is one of the most critical blocks in phased array systems, since its phase interpolation performance, i.e., phase precision and interpolation range, governs the beam-forming and beam-steering capability of the array.

Reflective phase shifter is used as a passive approach to achieve phase shifting [1]. However, reflective phase shifters present a fundamental trade-off between insertion loss and phase shifting range, and they also consume excessive chip areas due to the required λ/4 coupler.

Vector modulator based phase rotator is widely used as an active phase interpolation approach [2]. It provides inherent advantages, such as a wide phase shifting range, signal amplification, and a compact chip area. The simplified schematic of a typical vector modulator based phase rotator is depicted in Fig.1. The incoming RF signal is first split into its in-phase and quadrature signals, which are scaled independently by a pair of variable gain amplifiers (VGAs) and then summed together to achieve the desired phase interpolation.

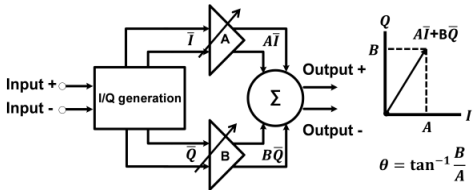

Fig.1. I/Q vector modulator based phase rotator architecture.

The I/Q generation block is a critical part in a vector modulator phase rotator, as its performance largely governs the phase interpolation quality; its key performance aspects include I/Q phase mismatch, I/Q magnitude imbalance, signal loss, and bandwidth. To generate the quadrature signals, RC-CR pair and its poly-phase extension are commonly used. However, they suffer from inherent signal loss and sensitivity to process variations. Structures based on L-C resonance [3] and single-ended transformer [4] are also used for quadrature generations with improved robustness against process variations. But these techniques require excessive chip area particularly in differential configurations, and they are sensitive to the loading effect of the following stages.

To address these challenges, we propose a digital linear phase rotator design with a 6-port folded transformer based ultra-compact passive structure for high-quality quadrature generation. As a proof-of-concept design, a K-band phase rotator implemented and demonstrated.

II. A Folded Transformer Based Differential Ultra-Compact Quadrature Generation

A folded transformer based fully differential ultra-compact quadrature generation scheme is proposed and demonstrated with a 5 GHz design in [5]. We leverage this technique and extend it to achieve K-band operation.

First, two separate transformers (TRF 1 and 2) loaded by C_1 and C_2 are designed to generate a fully differential in-phase and quadrature-phase signals (Fig.2). With a differential mode operation, the current directions in the two transformers are identical, making it feasible to fold the two transformers into one structure within a single inductor footprint (Fig.3). Such folding ensures magnetic enhancement of the two paths without signal cancellation.

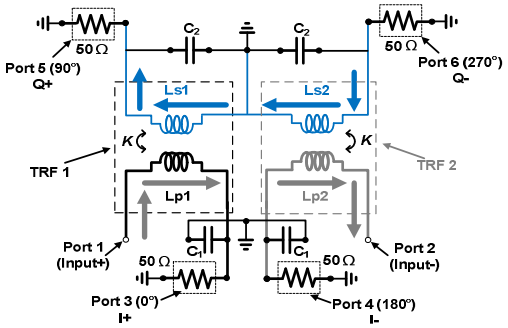

Fig.2. Schematic of a 6-port transformer based I/Q generation network. The common phase delay from the differential input (port 1-2) to the four outputs (port 3-6) is not shown.

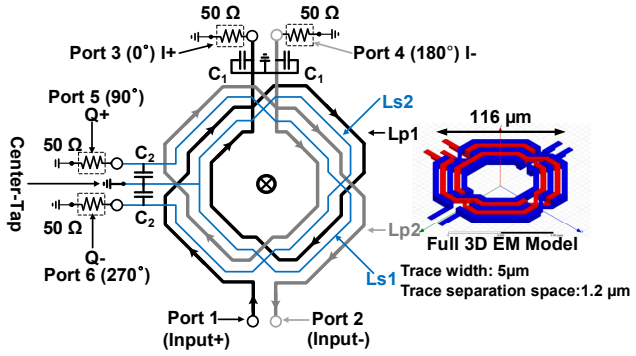

Fig.3. The folded structure of the 6-port transformer based I/Q generation network. The ports and passive components labels correspond to the ones in Fig.2.

By following the design equations and steps in [5], we achieve a K-band differential quadrature generation network as a compact 6-port folded passive network within only one inductor foot-print (D=116 μm) (Fig.3). The black and the grey lines represent the primary coils (L_{p1} and L_{p2}) of the folded structure each with 1.5 turns; the narrow blue lines stand for the two secondary coils (L_{s1} and L_{s2}) each with 1 turn and sharing the ac-ground center-tap (Fig.3). It can be verified that the folded structure in Fig.3 preserves the same current flows in Fig.2 while achieving magnetic enhancement between the two half circuits. The four capacitors represent the VGA parasitic capacitances and are absorbed into the matching.

The simulated behavior of the folded structure based on 3D EM modeling is shown in Fig.4, demonstrating high-performance I/Q generation. By exciting the input ports (port 1 and 2) differentially, the signal magnitudes at the four output ports (port 3-6) are -6.7 dB, indicating an actual 0.7dB passive loss. The magnitude mismatch at 23.5 GHz is within 0.2 dB. The four output phases closely follow the differential quadrature relation with only 2° phase error at 23.5 GHz (Fig.4). This high-performance quadrature generation is achieved with the four output ports loaded by 50 ohm, and the input capacitances of the following stages can be completely absorbed into the matching network. Therefore, this folded structure is robust to the output loading.

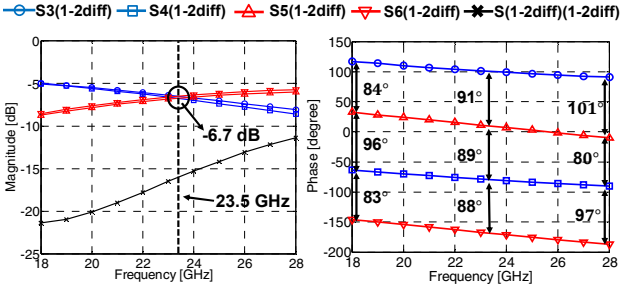

Fig.4. Magnitude and phase response of the I/Q generation circuit. The port numbers follow the definitions in Fig.3. "1-2 diff" means port 1 and 2 are driven differentially as the input.

III. Variable Gain Amplifier Design

The architecture of the phase rotator is shown in Fig.5. The differential I/Q output signals from the 6-port passive quadrature generation network are fed into two variable gain amplifiers (VGAs), with each implemented as 5 binary weighted cells connected in parallel. The weighted currents from I/Q paths are combined at the output inductive load. A differential open drain amplifier buffer is used to facilitate the measurements.

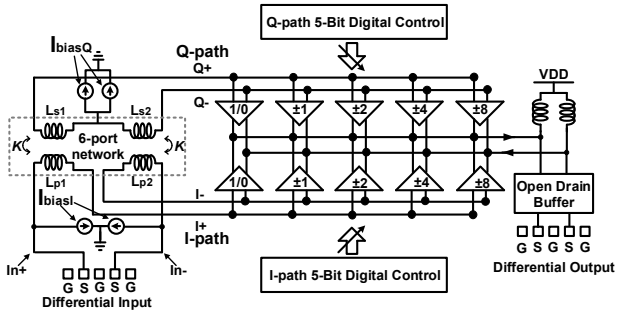

Fig.5. The architecture of the phase rotator.

The binary weighted cells in the VGA are implemented as polarity selectors with common-base differential cascode amplifiers controlled by digital switches (Fig.6). The complementary control signal selects either the left (Q_{L1}-Q_{L4}) or the right (Q_{R1}-Q_{R4}) set of transistors, determining the polarity of the output currents. Taking the ×1 cell as an example, when S is logic high (logic low for $\bar{S}$), the left cascode amplifier (Q_{L1}-Q_{L4}) turns on and produces an output current with "+1" normalized amplitude. A "-1" output current can be generated by the right cascode amplifier enabled by the inverted logic.

In the unit cell (×1), we set each bipolar transistor (Q_{L1}-Q_{L4} and Q_{R1}-Q_{R4}) with an emitter width of 0.7 μm. The other VGA cells are binary weighted by scaling both the emitter size and multiplicity of the transistors. To achieve a normalized weighting range from "-15" to "+15"

including zero weighting, we add a ×1 unit cell to produce "+1" or "0". The outputs of its right cascode amplifiers (Q_{R1}-Q_{R4}) are tied directly to the supply to produce the "0" output weighting.

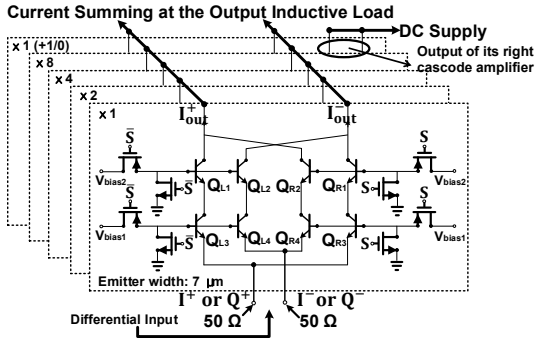

Fig.6. The schematic of the 5 binary weighted cells connected in parallel. A ×1 unit cell is used to generate "1" or "0" weighting.

The common-base topology eases the matching between the VGAs and the passive I/Q generation structure. The transistor size and bias point ensure that the real part of the combined input impedance of the 5-bit VGA cells is 50 ohm, which is the required load of the 6-port I/Q generation structure. The input parasitic capacitances of the VGA cells are absorbed into the I/Q generation network (Fig.3). Since the left (Q_{L1}-Q_{L4}) and right (Q_{R1}-Q_{R4}) set of cascode amplifiers in each weighted cells are identical, the combined input impedance remains constant regardless of the VGA control bits.

In terms of the DC bias currents, the two emitter DC currents of the 5-bit Q-path VGA cells conduct through the secondary coil (L_{s1} and L_{s2}) and sink to the current sources (I_{biasQ}) at the center-tap (Fig.5). The two I-path VGA emitter DC currents flow through the primary coil (L_{p1} and L_{p2}) and sink to the two current sources (I_{biasI}).

IV. Measurement Results

We implement the phase rotator in the IBM9HP SiGe BiCMOS process. The design is highly compact in area (Fig.7), suitable for large-scaled phased array systems. The folded transformer based quadrature generation structure occupies only 116 µm by 116 µm, and the phase rotator is only 310 µm by 380 µm (excluding pad).

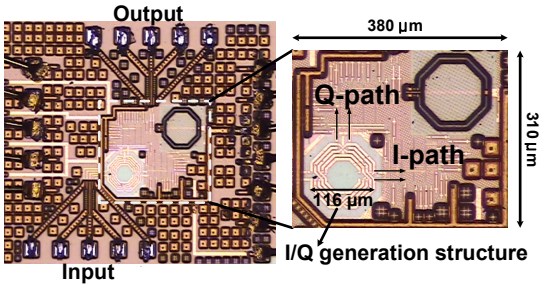

Fig.7. The chip microphotograph of the phase rotator.

The phase rotator consumes 4 mA from 2.5 V. We use external bias-T to provide biasing for the open drain buffer. We use a 4-port vector network analyzer (Agilent PNA-E8364B) for performance characterization (Fig.8). External DAC is used to set the programming bits.

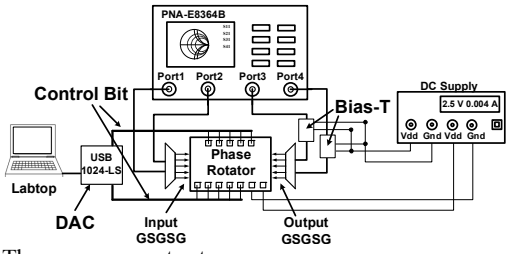

Fig.8. The measurement setup.

The on-chip I/Q VGAs are separately programmed to cover the normalized magnitude span from -15 to +15 (31 settings), yielding total 961 points on the normalized output constellation plane (Fig.10). To preserve symmetry, the gain setting of +16 is not used. If the target phase interpolation is 5° phase step within 1.5dB amplitude variation, the optimum (least square phase error) phase interpolation points are shown for the case at 23.5 GHz (Fig.10a) and 18 GHz (Fig.10b). The measured -3 dB bandwidth is 6 GHz with the 23.5 GHz center frequency, demonstrating a very wide bandwidth of 26% (Fig.11).

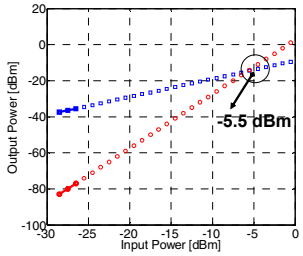

Fig.9. Measured IIP_3 at 23.5 GHz. The loss at the P_{out} due to cables and probes are not de-embedded.

The measured IIP_3 and input P_{1dB} are -5.5 dBm (Fig.9) and -16dBm, demonstrating high-linearity performance.

The digital phase rotator functions as a digital-to-phase convertor. Its discrete interpolated phases lead to quantization phase errors (Fig.13). For a given allowable amplitude variation, the acceptable discrete phase interpolation points on the constellation are determined, and their rms quantization phase error can be calculated. Figure 12a shows the quantization phase error for a full-range (360°) phase interpolation at 23.5 GHz with 1.5 dB amplitude variation. Figure 12b summarizes the measured rms quantization phase errors versus allowable magnitude variations at different frequencies for our phase rotator design. The results demonstrate that a relaxed magnitude variation leads to a smaller rms quantization phase error since more interpolation points can be used.

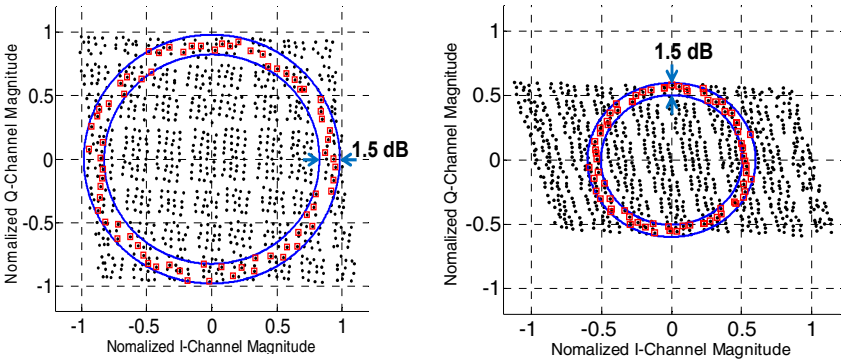

Fig.10. Measured constellation points on the normalized I/Q channel coordinates showing two phase interpolation examples with 5° step and 1.5 magnitude variations at 23.5 GHz (a) and 18 GHz (b). The RMS phase errors are 0.9° and 1.5°, respectively.

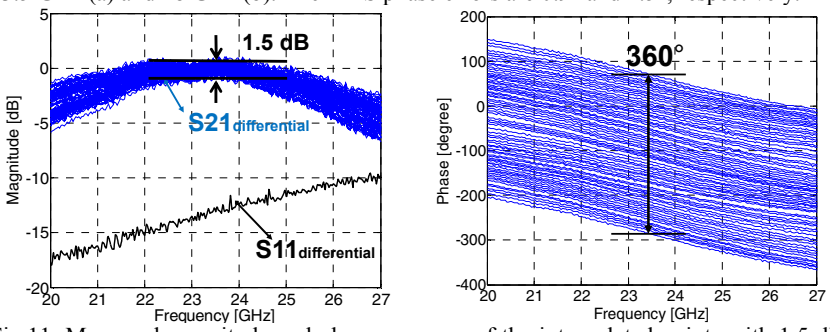

Fig.11. Measured magnitude and phase response of the interpolated points with 1.5 dB magnitude variation and 5° phase step.

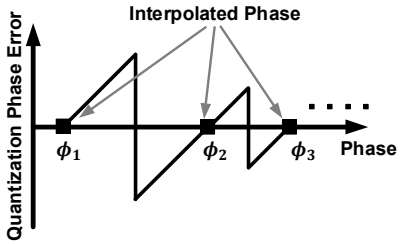

Fig.13. The representation of quantization phase error.

At the edge of the band, e.g., 18 GHz, I/Q generation structure has non-negligible amplitude/phase mismatches (Fig.4), leading to the skewed output constellation plots (Fig.10b). However, the two wideband 5-bit VGAs (I/Q) enable dense interpolation, which can be leveraged to overcome such I/Q mismatches and extend the bandwidth. For example, the current weighting of I path can be scaled to compensate the I/Q mismatch at 18 GHz and still achieve the desired output phases (Fig.10b). Figure 12b also demonstrate that very small rms phase errors can be achieved at the edges of the band with only 1.5° at 21 GHz and 2° at 18 GHz for 1 dB amplitude variation.

V. Conclusion

In this paper, a K-band vector modulator based phase rotator is presented. It employs a folded transformer based differential quadrature generation structure and two 5-bit

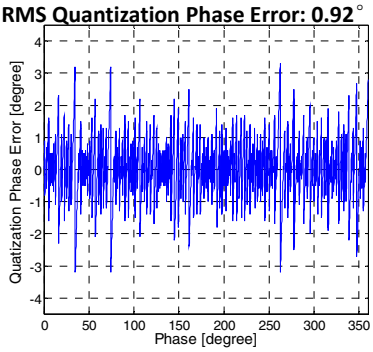

Fig.12 (a). Measured quantization phase error over 360° range with magnitude variations of 1.5 dB at 23.5 GHz.

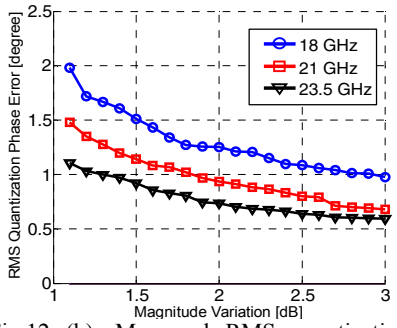

Fig.12 (b). Measured RMS quantization phase error.

wideband VGAs. The measurements on an IBM9HP test chip demonstrate accurate phase interpolation over a broad bandwidth. Compensation capabilities against I/Q magnitude /phase imbalance are presented.

Acknowledgement

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