



GlobalFoundries™

**BiCMOS8HP/8XP**

**Design Kit and Technology Training Book**

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## Introduction to SiGe (BiCMOS) Technologies 5

This section includes an introductory view and comparison of the key aspects of the different GlobalFoundries (GF) SiGe technologies.

## Technology Features, Device Library, Models and ROC (Reliable Operating Conditions) 23

This section consists of the active and passive devices available in the design kit for circuit design. For each device, pertinent performance parameters, its cross-section, layout view and a CDF (Component Description Form) property form are illustrated. This gives designers a quick overview of the device. A brief summary of the technology features, 8HP/8XP process cross-section, available metal stacks is also included. There are unique Millimeter Wave devices in the *bicmos8hp* (*bicmos8xp*) PDK. Information is included about them. *8HP and 8XP are both high performance SiGE technologies, the only difference is in the NPNs. 8XP offers higher performance NPNs. However, the bicmos8hp and bicmos8xp PDKs are kept separate and they can not be inter-changed and/or inter-mixed in the same design.* Modeling information about each device class is also provided in this section. Device reliable operating limits are also included at the end of each class of devices. In addition, some support pcells that are needed to complete the designs e.g., image/chip guard ring, crackstop, bondpad, etc., and that the designers should be familiar with are also described. Information is also provided about which devices can be placed under the pads for compact layouts.

## ESD Library 139

This section includes the available ESD devices in the design kit. ESD protection tutorial is now included in the ESD Reference Guide and therefore omitted from the training book. The ESD device library has both primitive and hierarchical pcells, also referred to as macros. Macros can now be instantiated directly like the primitive pcells. The BiCMOS8HP ESD Reference Guide has detailed information about the ESD devices including the TLP (Transmission Line Pulse) measurement data. Using the ESD Reference Guide in conjunction with the Design Manual is expected to provide the requisite ESD design support for the designers.

## Digital Library, IOs and IP 165

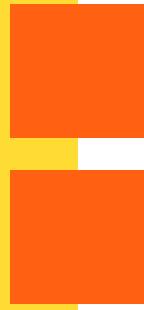
This section gives an overview of the standard cell digital library, IOs and any other IP available.

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<b><a href="#">Simulation</a></b>	<b>188</b>
This section provides an overview of the supported simulators, how to set up simulators and how to account for manufacturing process variations – both Monte Carlo and Fixed/Customer corners in designs. In addition, ‘Fixed’ (digital) corners which are typically employed to analyze delays through digital circuits for timing closure, we provide many “Custom” (fixed analog) corners that a designer can judiciously use for analog circuits thereby reducing the long Monte Carlo simulations. For simulation, Hspice and Spectre modes are supported.	
<b><a href="#">Design Layout Considerations</a></b>	<b>221</b>
This section provides an overview of the BiCMOS8HP Design Manual and BiCMOS8XP Design Manual Addendum and a series of layout topics including the ground rules that may not be obvious, such as, antenna rules and pattern density considerations. We describe floating gate, copper dendrite, the necessity of PCI marks, the techniques for noise minimization, proper use of substrate contacts and latchup prevention, proper layout techniques to achieve optimum device matching, and prevention of electromigration failure and unsatisfactory voltage drops through adequate sizing of conductors. At the end, we also include a few additional layout techniques for compact layouts including yield enhancement.	
<b><a href="#">Design Kit Installation, Documentation and Support</a></b>	<b>292</b>
This section includes the procedure for downloading the BiCMOS8HP/BiCMOS8XP base design kits and “Add-On” components. The base design kit includes only the Assura DRC and LVS decks. All other PDK components, such as, Calibre DRC, LVS decks and the parasitic extraction (PEX) decks - Assura QRC and Calibre XRC etc., are all “Add-On” components. These Add-On components have to be subscribed separately. They are downloaded in the same directory structure as the base design kit. Procedures are illustrated about creating/attaching library properties, version migration, implicit and explicit schematic entry representations, substrate methodology, multicity and some of the utilities provided in the design kit, such as, gds data streaming, parameter checks when migrating to a newer version etc. Designer is advised to go through the cdslib Release Notes. This section is only a small subset of it. Documentation and technical support information is also included.	

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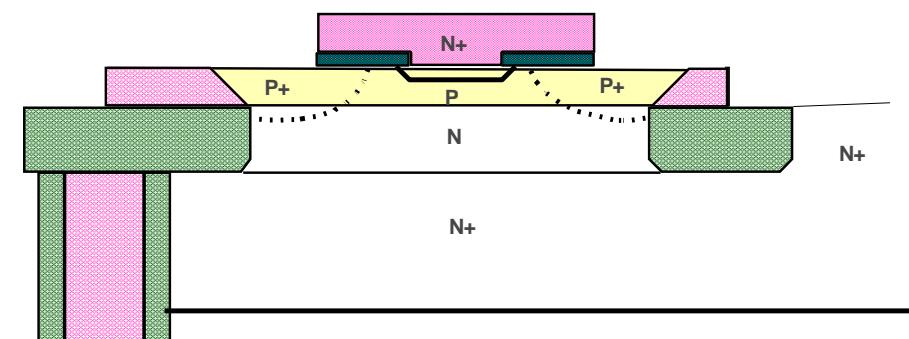
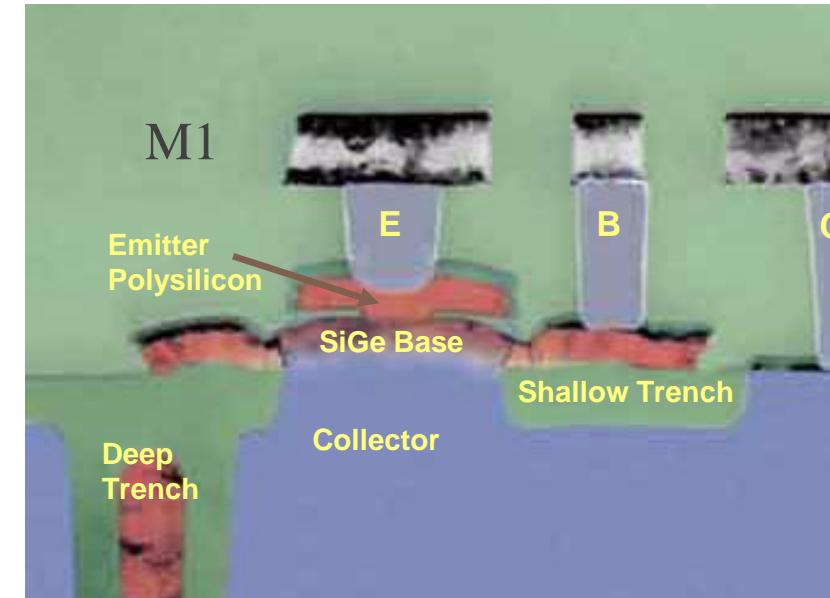
<a href="#"><u>Automotive PDK Notes</u></a>	<a href="#"><u>327</u></a>
This section provides information about using the PDK for Automotive. For automotive, all design rules are level “a” rules and there are some device usage restrictions. AutoPro flow is used for submitting these designs. Its usage details are described.	
<a href="#"><u>ADS Interoperable Design Kit</u></a>	<a href="#"><u>332</u></a>
ADS Standalone Schematic/Layout Kits are available for both BiCMOS8HP and BiCMOS8XP. This section provides a brief overview of what components are available, how to set up ADS and simulation. ADS Release Notes provide additional level of details.	
<a href="#"><u>Design Verification (DRC/LVS) and PEX Flows</u></a>	<a href="#"><u>339</u></a>
This section sections list the supported DRC, LVS and PEX tools. Designers should work with their tool vendors for running them. We only provide sample procedures for running these tools. Documentation in the tool subdirectories have associated Release Notes that list the tool version used to verify them and any known limitations.	
<a href="#"><u>Revision History</u></a>	<a href="#"><u>389</u></a>



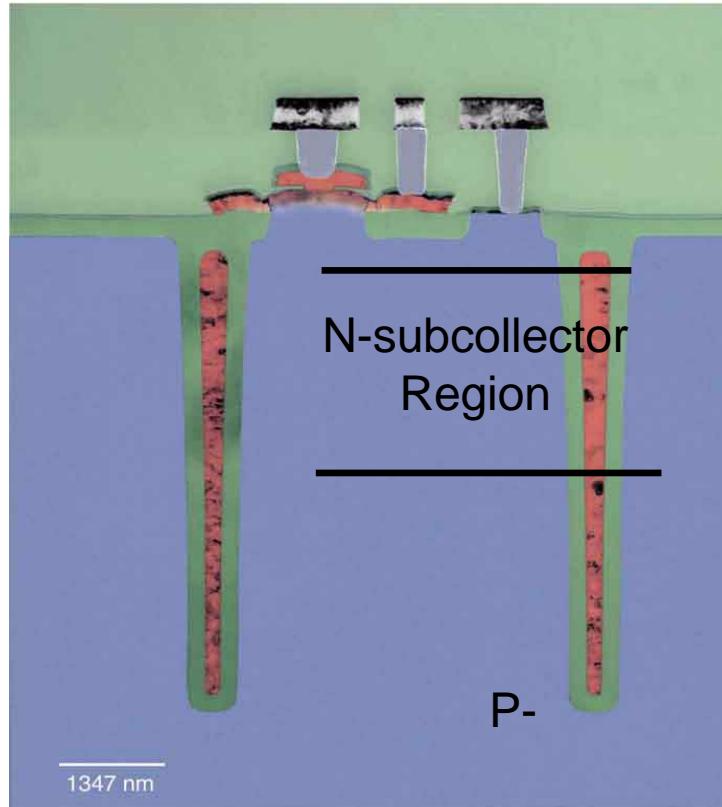
# **Introduction to SiGe (BiCMOS) Technologies**

# High Performance SiGe HBT Structure

- Hetero-junction Bipolar Transistor
- Standard Self-aligned Base
  - Non-selective low-temperature epitaxy
  - Graded Si-Ge base, in situ-doped
  - Self-aligned single-crystal extrinsic base
  - Low resistance, low capacitance base contact
- Patterned Collector Implant
- Low Resistance Sub-collector
- Arsenic Implanted Polysilicon
- Undoped Polysilicon-filled Deep Trench
- CMOS-compatible Shallow-trench
- Readily Scalable, CMOS-compatible
  - SiGe BiCMOS enables RF / Analog circuits with CMOS logic



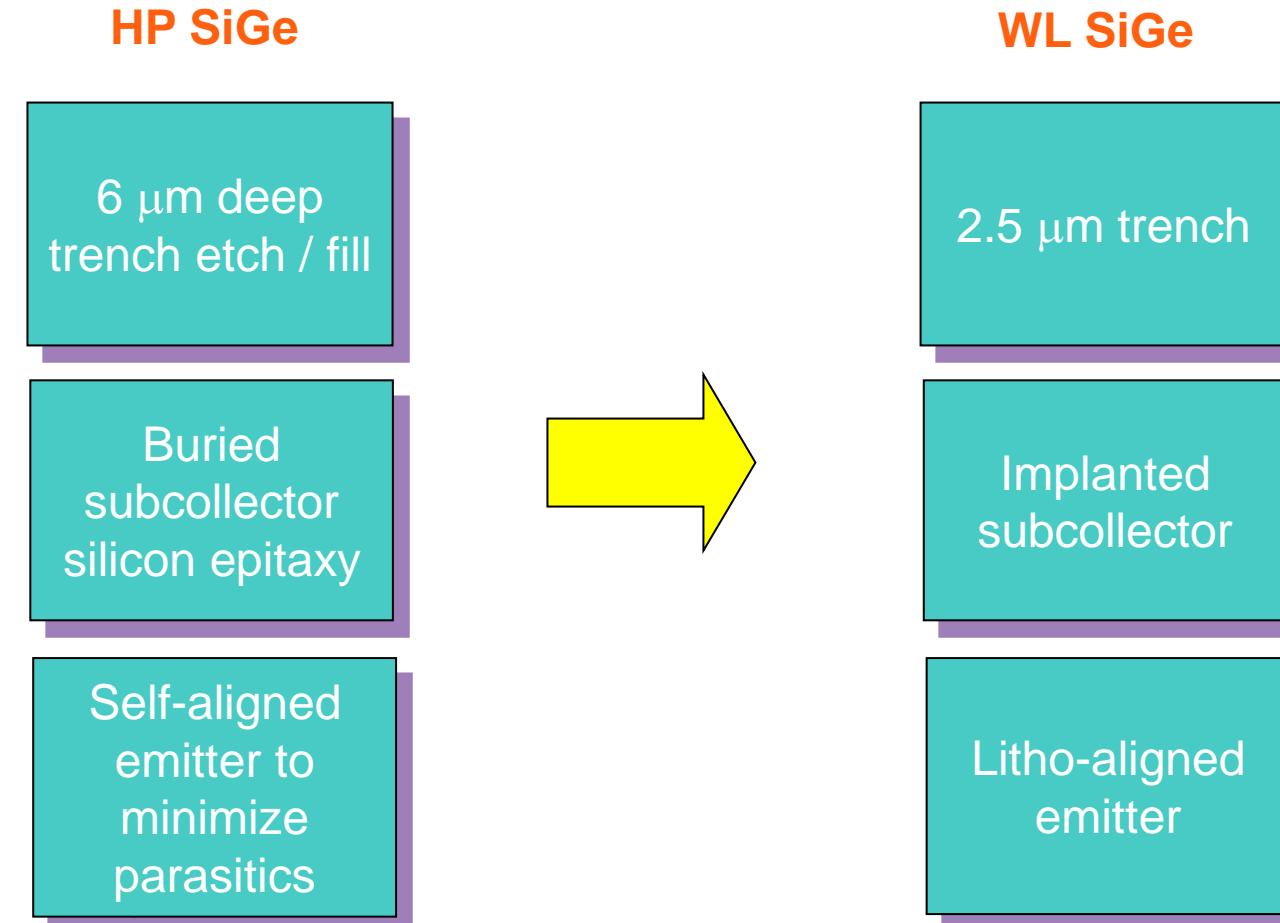
# Deep Trench Isolation



- Highly planar
- Permits a high level of integration, merging RF and Logic functions on a single die (isolation and density)
- Low parasitic (subcollector to substrate)

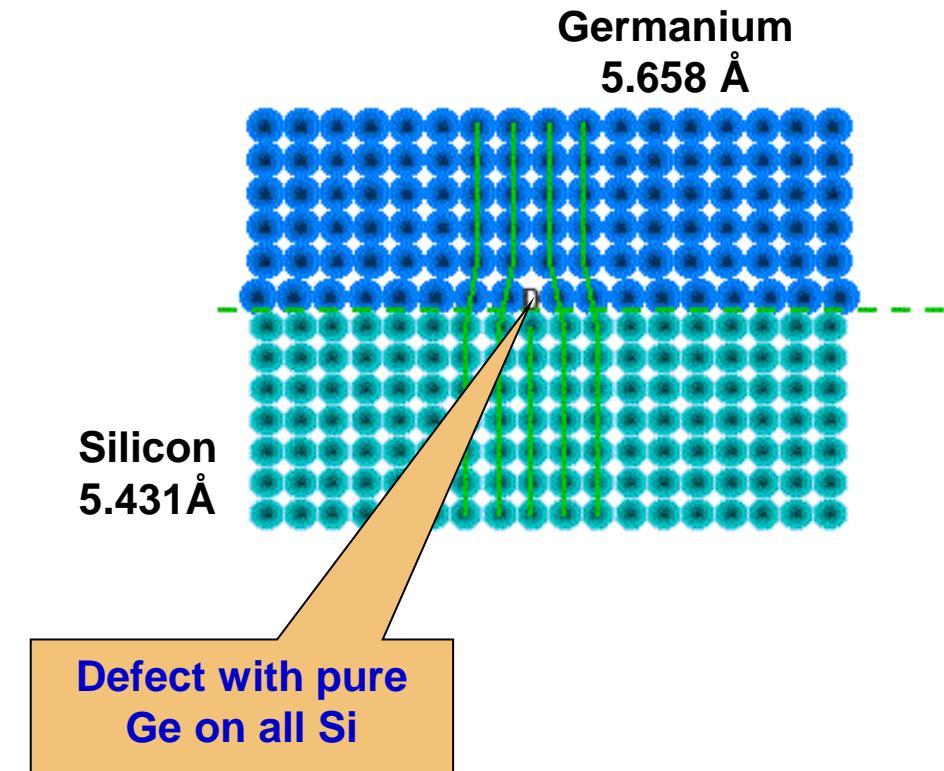
# HP SiGe vs. WL SiGe

- WL SiGe has reduced processing cost / cycle time vs high-performance SiGe HP



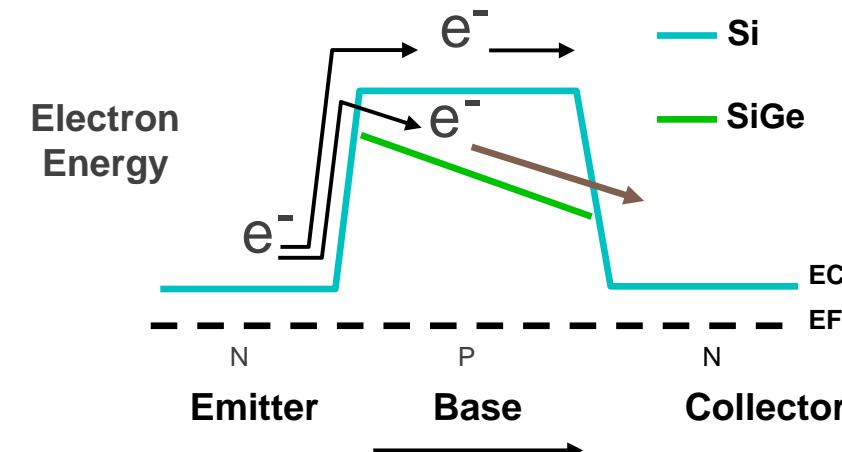
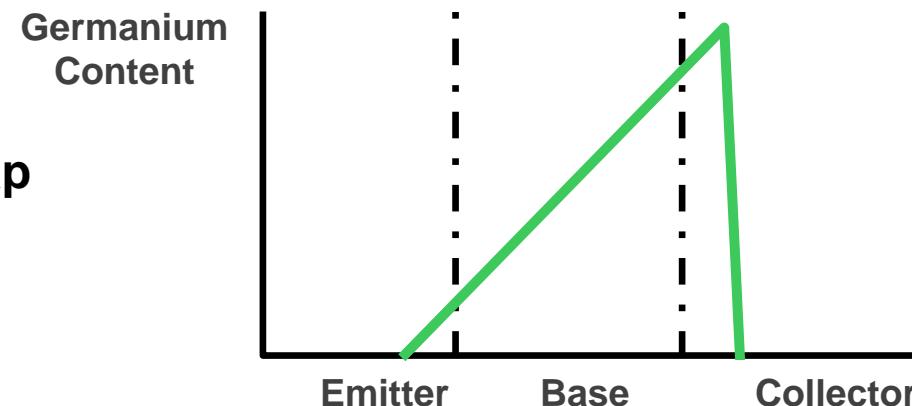
# Graded Base SiGe HBT

- Low temperature epitaxial growth
  - High quality, single crystal  $\text{Si}_x\text{Ge}_{1-x}$
  - In-situ base doping
- "Strained layer" due to lattice mismatch
  - Limits base thickness
  - Limits total Ge content
- Single crystal maintained
  - No crystal defects (dislocations)



# Graded Base SiGe HBT Contd...

- Graded Ge content varies bandgap
  - Built-in drift field
    - Reduces base transit time
    - Increases transition frequency ( $f_T$ )
- Adding Ge grading to the base of a silicon bipolar transistor was suggested as a means to significantly enhance transistor speed as early as 1957-H.  
Kroemer



# **f<sub>T</sub> and f<sub>max</sub>**

- **f<sub>T</sub> : Small-signal unity gain cutoff or transition frequency**

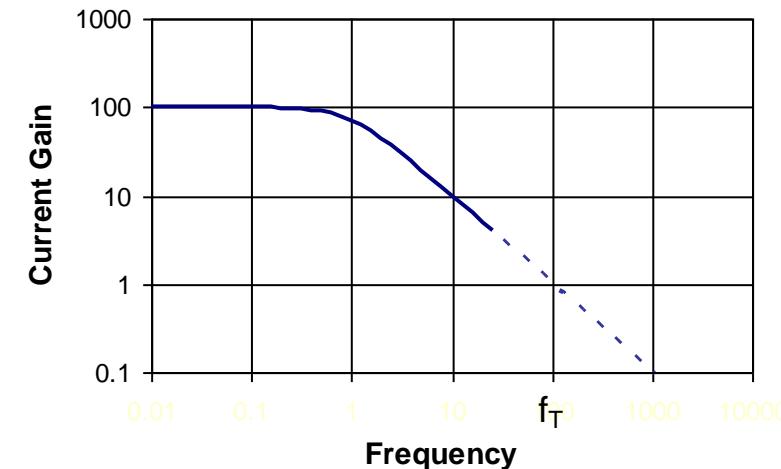
$$\frac{1}{2 \pi f_T} \sim \frac{kT}{q I_c} (C_{je} + C_{jc}) + r_b + r_e + r_c + (R_e + R_c) C_{jc} + R_{ns} C_{sub}$$

- **f<sub>max</sub>: Maximum Oscillation Frequency**

$$f_{max} \sim \sqrt{\frac{f_T}{8 \pi C_{jc} r_b}}$$

**Minimizing base transit time,  $r_b$ , is critical for high  $f_T$  and  $f_{max}$**

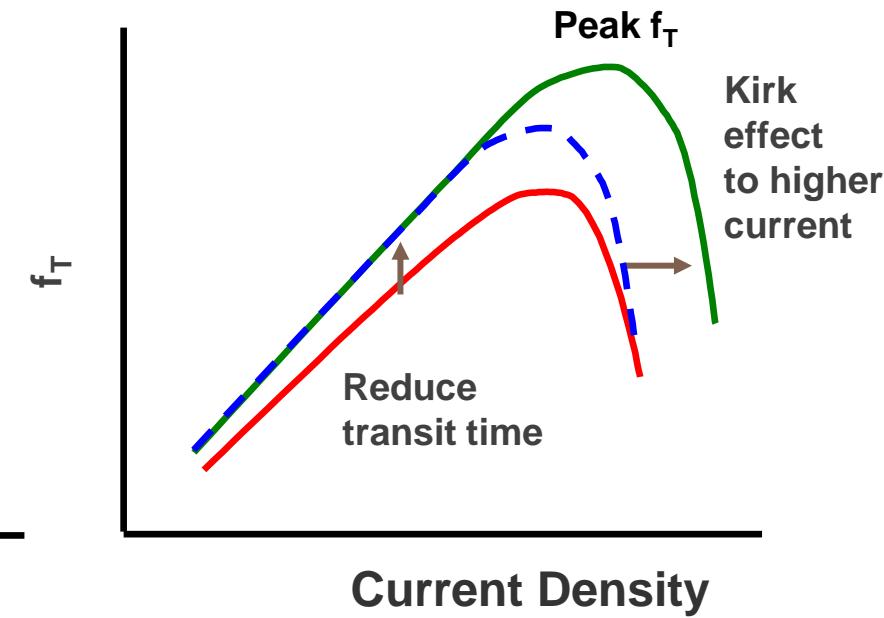
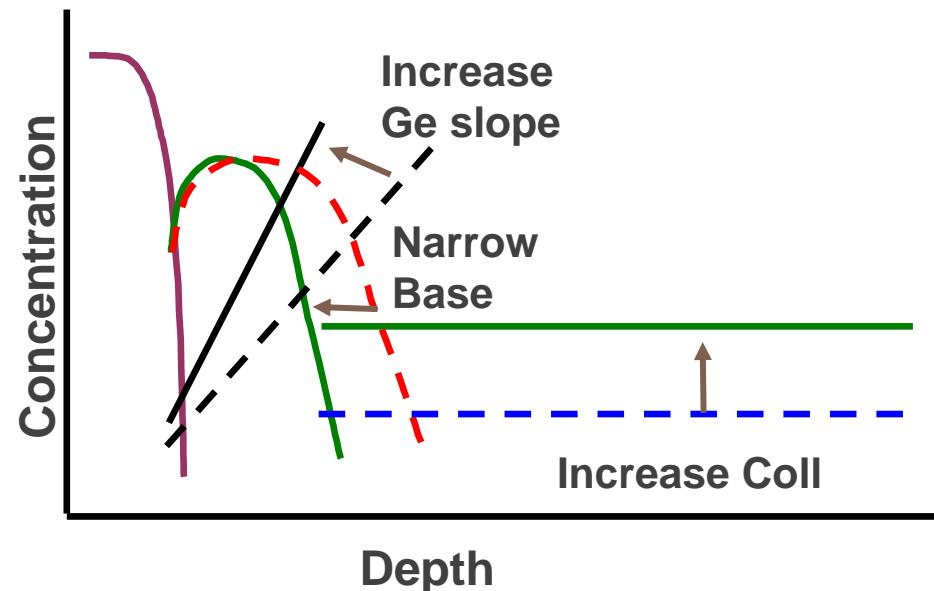
**Low EB and CB depletion capacitances and RC also important**



C<sub>jc</sub> : Collector-Base depletion capacitance; C<sub>je</sub> : Emitter-Base depletion capacitance ; r<sub>b</sub> : Base resistance

# NPN Vertical Scaling for Performance

- Vertical profile determines transit times
  - Base transit time,  $t_b$ , determined by base width and Ge gradient
- Kirk-effect to higher current with higher collector doping
  - Selective collector doping to achieve either
    - Higher Peak  $f_T$
    - Higher Breakdown

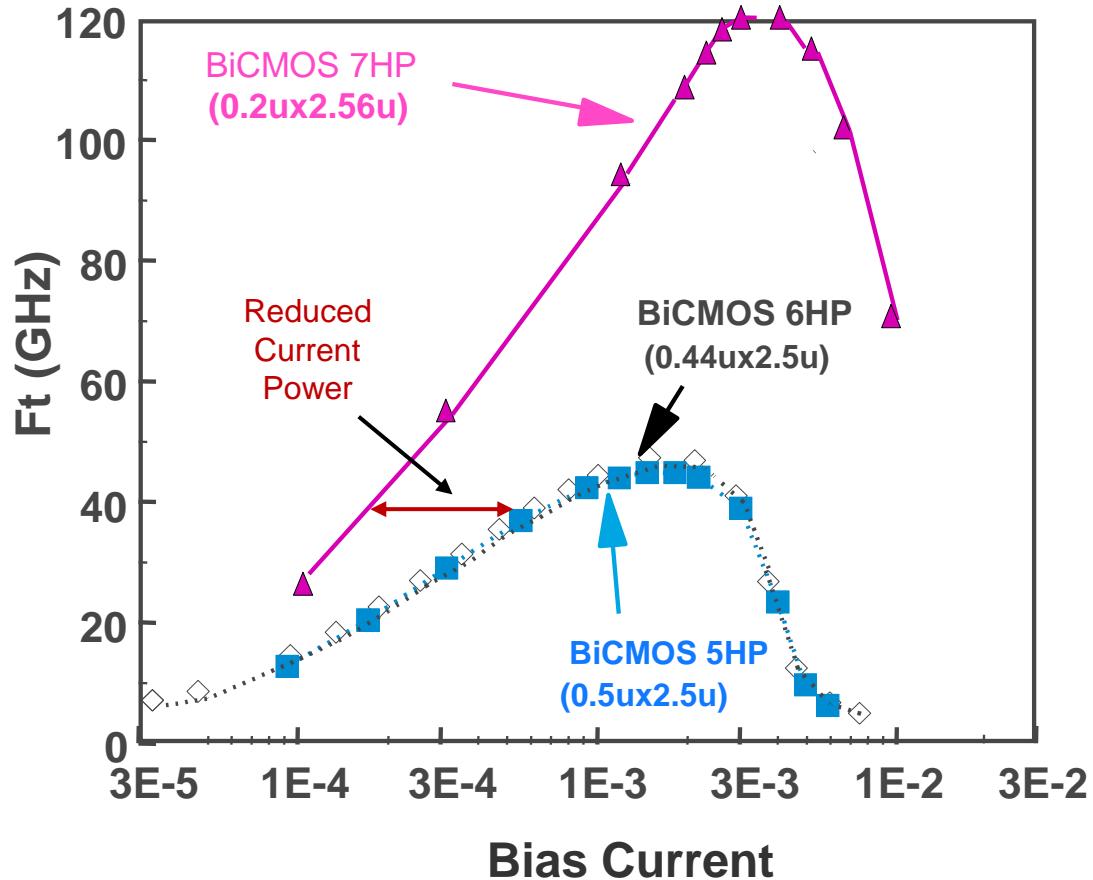


# Other Considerations for Performance

- **Scaling of base width**
  - Addition of Carbon in base to mitigate Boron diffusion during base growth
- **Lateral scaling of transistor dimensions**
  - Reduction in parasitic RC with photo-lithographic scaling
- **Reduction in  $C_{sub}$  with trench versus junction isolation**
  - Process complexity and density implications
- **Re-crystallization of emitter polysilicon**
  - Reduced emitter resistance, and reduced variability of  $R_e$
- **Extrinsic base implant**
  - Trade-offs in emitter-base capacitance versus  $R_b$  and process complexity
- **Raised base integration, for reduced  $R_b$** 
  - Thicker, lower resistance extrinsic base region

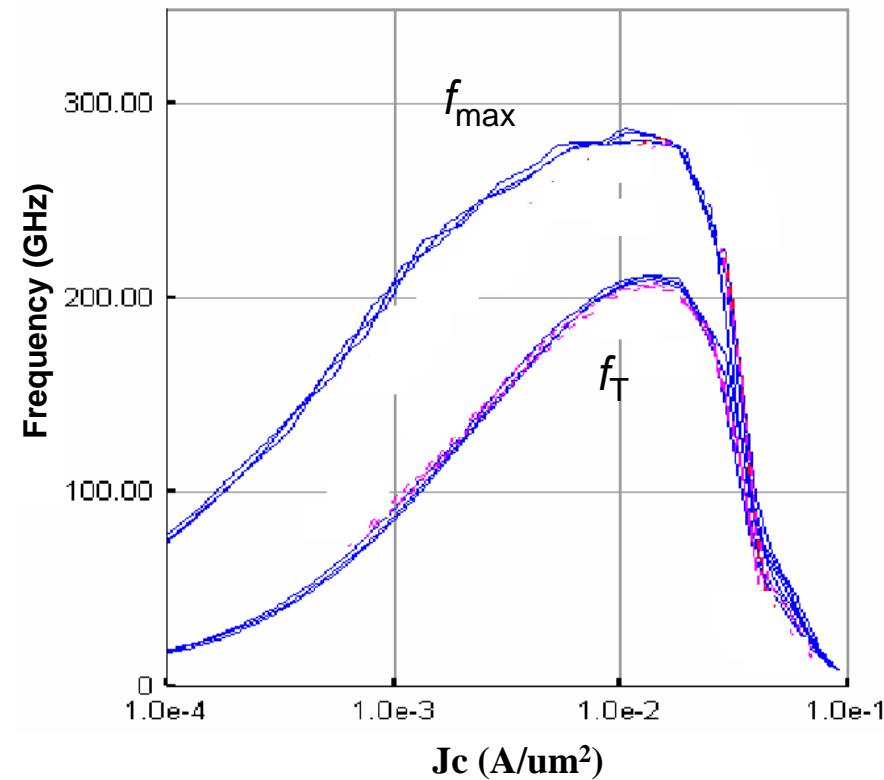
# NPN High $f_T$ / Low Power

Lower power at equivalent speed

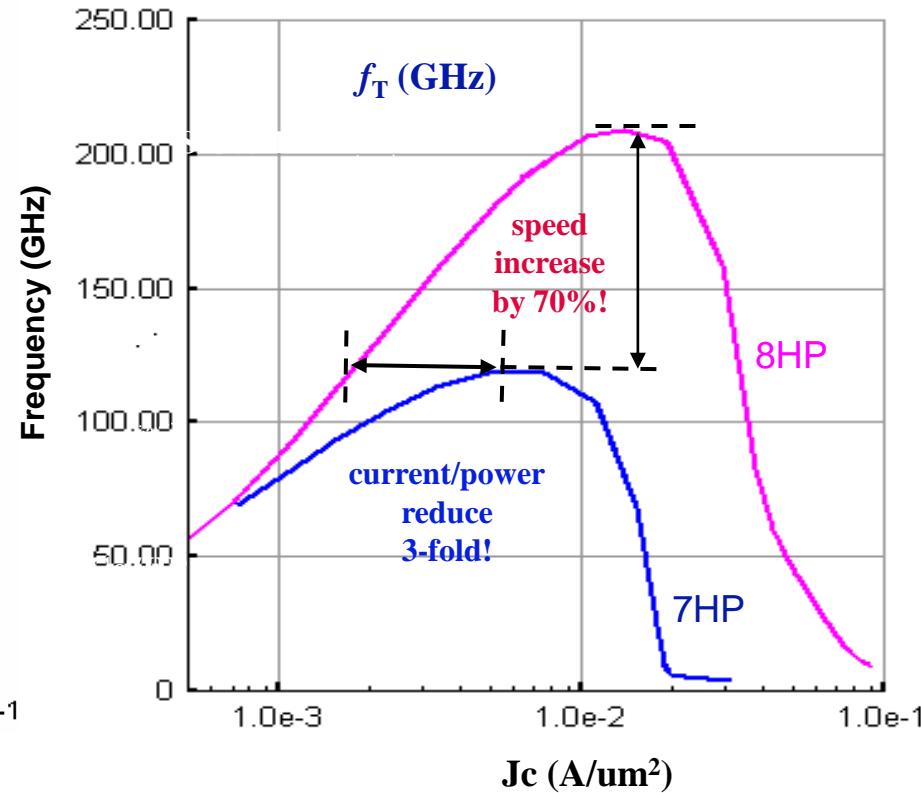


# AC Characterization $f_T$ and $f_{max}$

■ 8HP  $f_T$  and  $f_{max}$  vs.  $I_c$



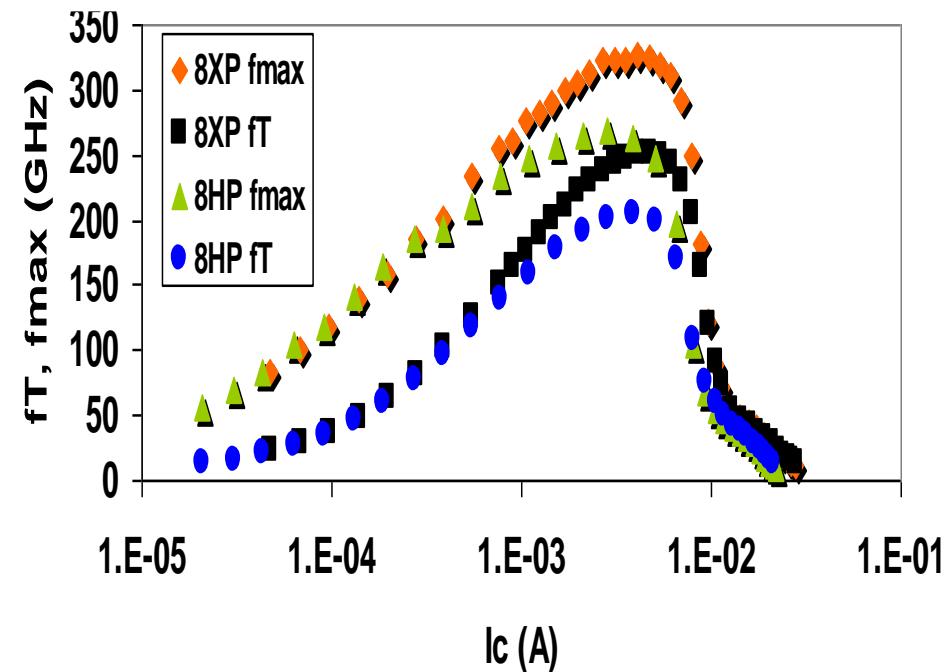
■ 8HP Improvement over 7HP  $f_T$



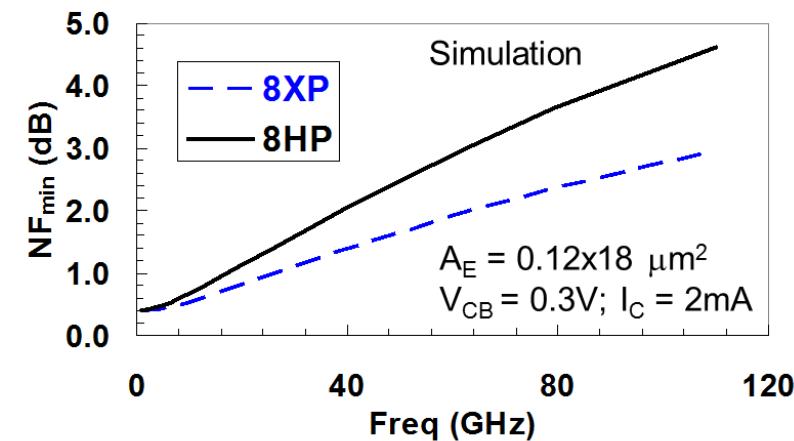
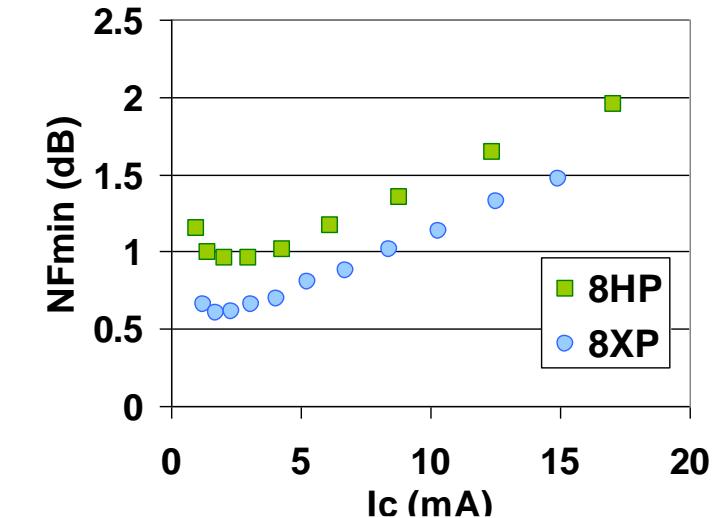
# 8XP vs. 8HP NPN Performance Enhancement (1)

## 8HP vs. 8XP

- Replace HP/HB HBTs with XP/XB
- Add electro-migration robust Cu wiring
- All other 8HP devices and features unchanged
- Existing 8HP non-NPN IP can be re-utilized
- XP NPN pcell has same footprint as HP NPN

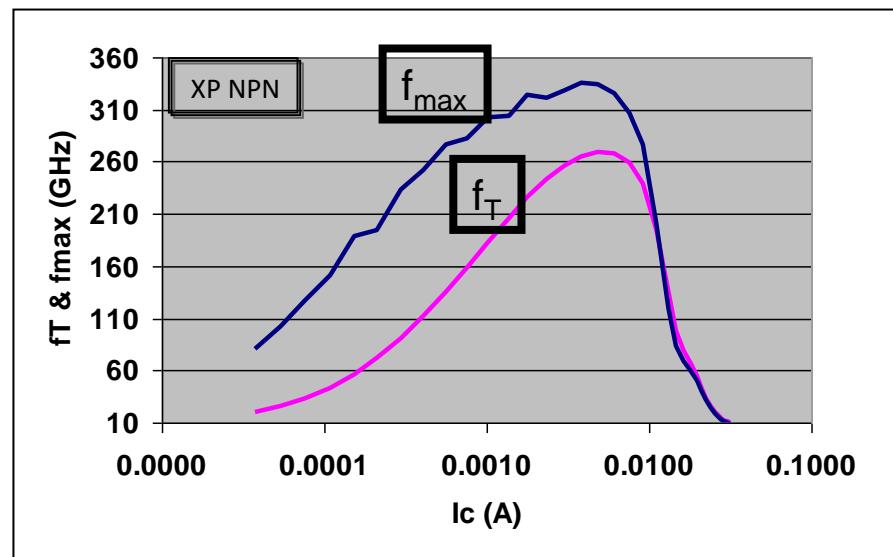


$$F_{\min} \approx 1 + \frac{1}{\beta} + \sqrt{\frac{2I_c}{V_T} (R_B + R_E) \left( \frac{f^2}{f_T^2} + \frac{1}{\beta} \right) + \frac{1}{\beta}}$$

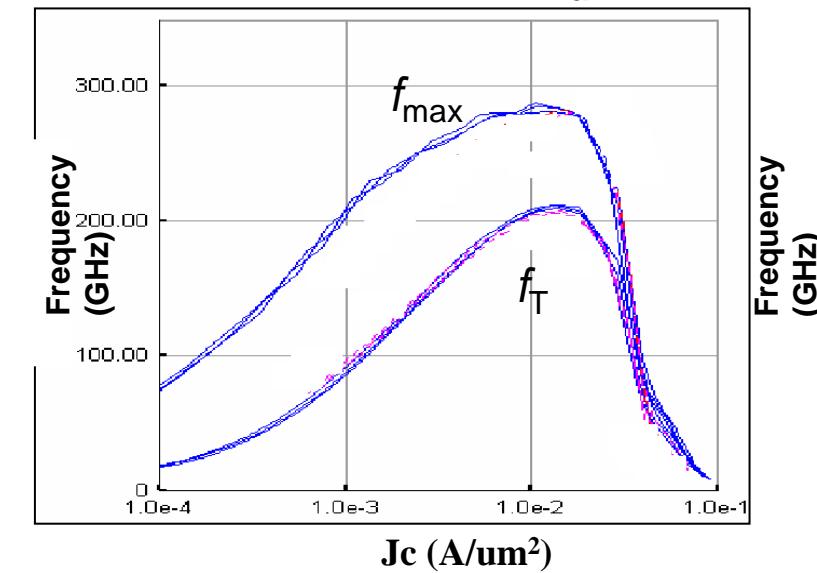


# 8XP vs. 8HP NPN Performance Enhancement (2)

$f_{max}$  and  $f_T$

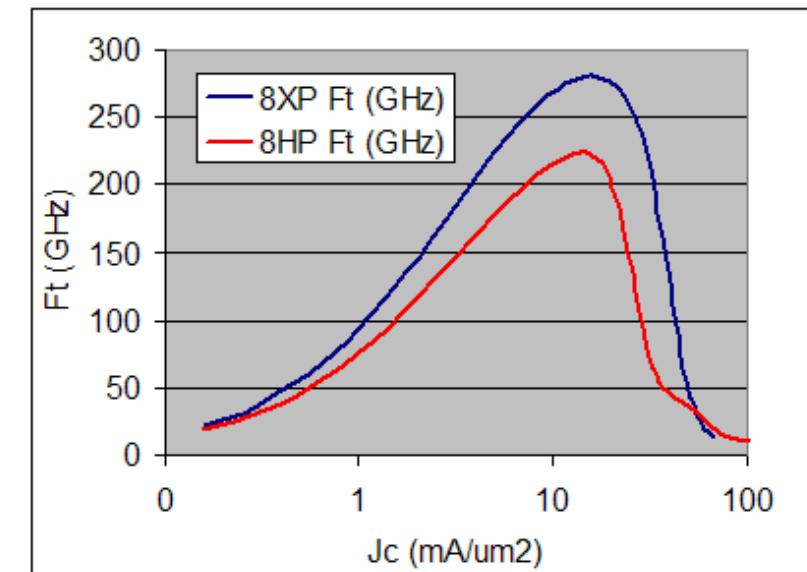
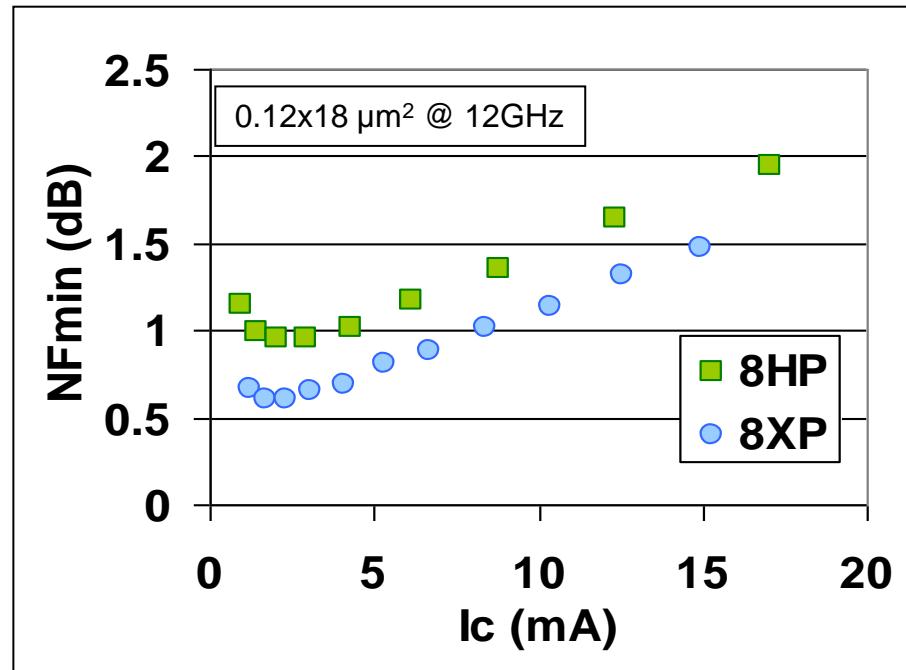


■ 8HP  $f_T$  and  $f_{max}$



# 8XP vs. 8HP NPN Performance Enhancement (3)

NF<sub>min</sub> and F<sub>T</sub>



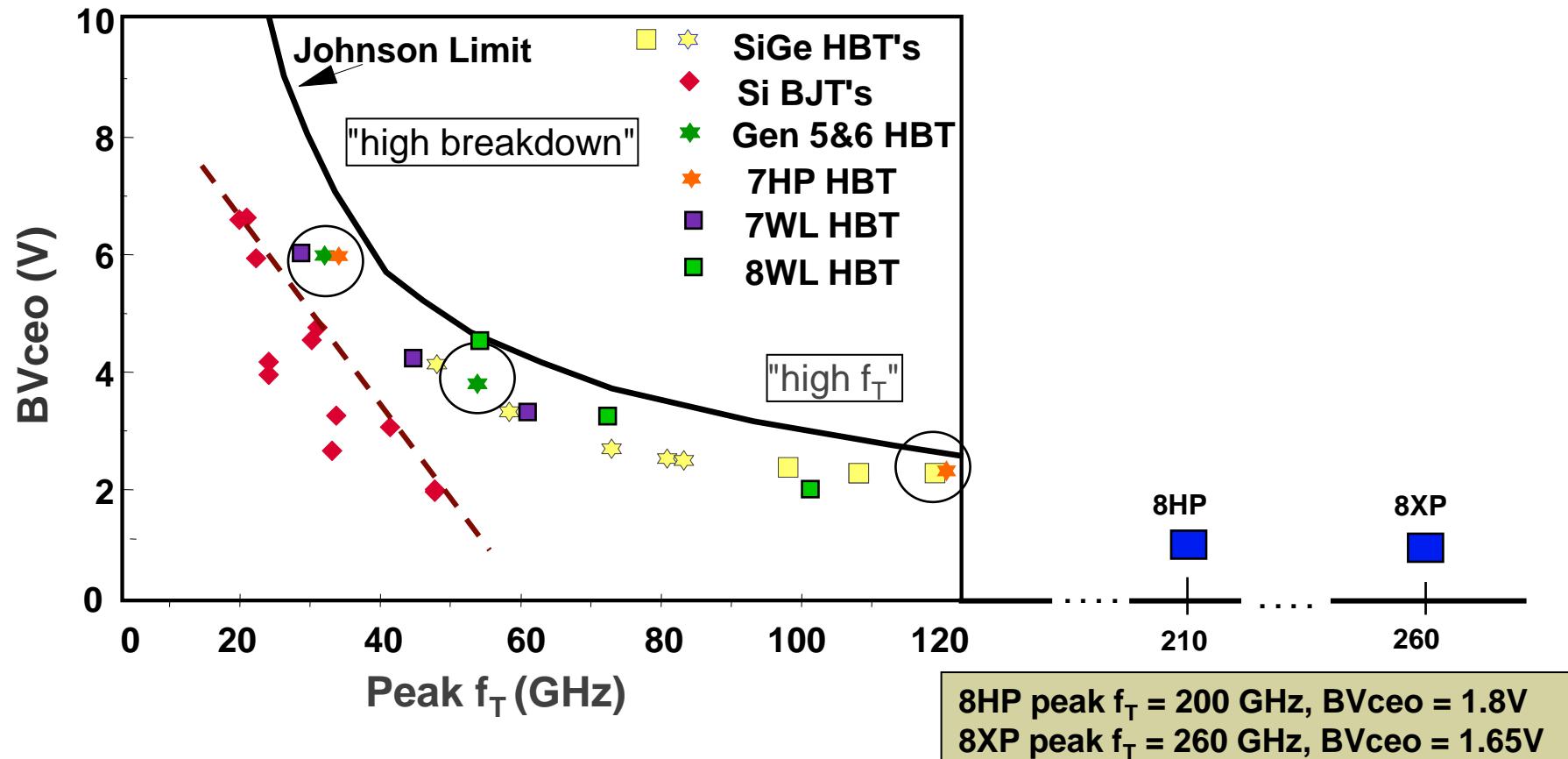
# NPN Breakdown Voltage

- Rapid increase in collector current at high  $V_C$
- Impact ionization at collector depletion region
- Lower breakdown for narrower bandgap materials
  - Si/SiGe will always have lower breakdowns than AlGaAs/GaAs
- Collector bandgap in BC depletion region is determining factor
  - Si versus SiGe base has little impact on BC breakdown
- $BV_{ceo}$  - Collector-emitter breakdown, base open
  - True application limit is  $BV_{cer}$  determined by resistance in base path
  - $BV_{cer}$  bounded by  $BV_{ceo}$  and  $BV_{cbo}$
- Higher breakdown with lower collector doping
  - Fundamental trade-off between  $f_T$  and breakdown voltage

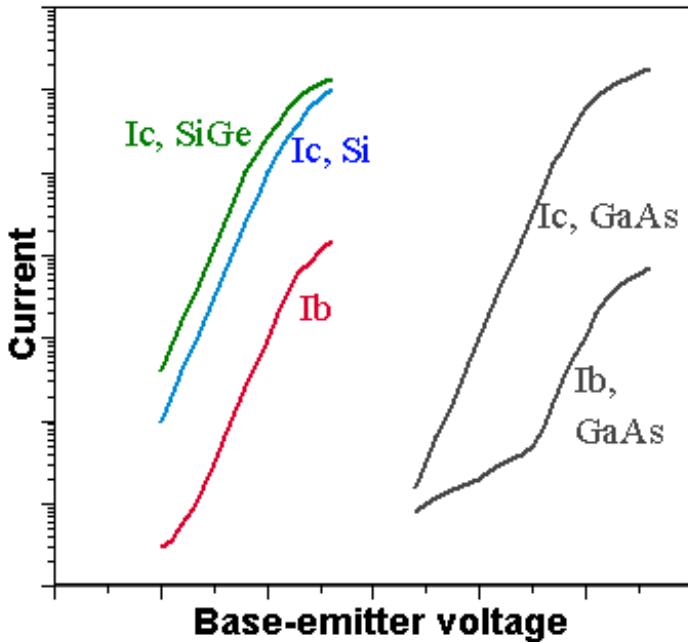
# Peak $f_T$ and Breakdown

First order material limits

Selective collector implant provides flexibility in same technology / design



# Gummel Characteristics



## AlGaAs/GaAs

High turn-on (bandgap)  
High  $\beta \sim \exp(\Delta E_v / kT)$   
 $\Delta E_v$  = Valence band offset at BE  
Recombination at low  $V_{be}$   
(passivation and defects)

## SiGe

High  $\beta$  due to  $\Delta E_{Grade}$

With increasing temperature:

$b_{Si}$  increases

$b_{GaAs}$  decreases

$b_{SiGe}$  ~ constant, depends on details of bandgap grading

$$b_{SiGe} \sim b_{Si} \exp(-\Delta E_v / kT) \frac{\exp(\Delta E_{Grade} / kT)}{1 - \exp(-\Delta E_{Grade} / kT)}$$

# Early Voltage ( $V_A$ )

$V_A$ : A measure of NPN output conductance

Extrapolate  $\partial I_C / \partial V_{CE}$  to negative x-axis interc

High  $V_A \rightarrow$  Flat  $I_C$  vs.  $V_{CE}$

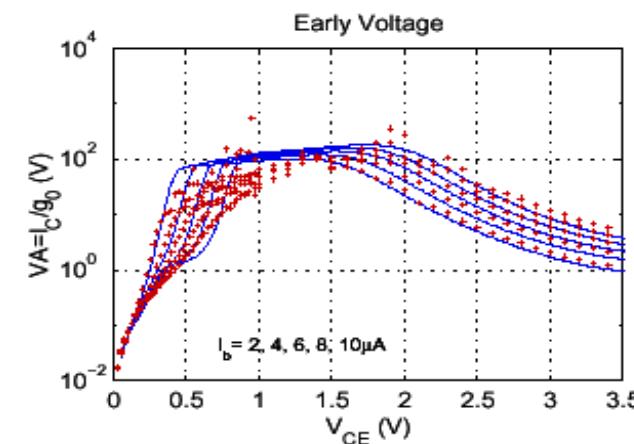
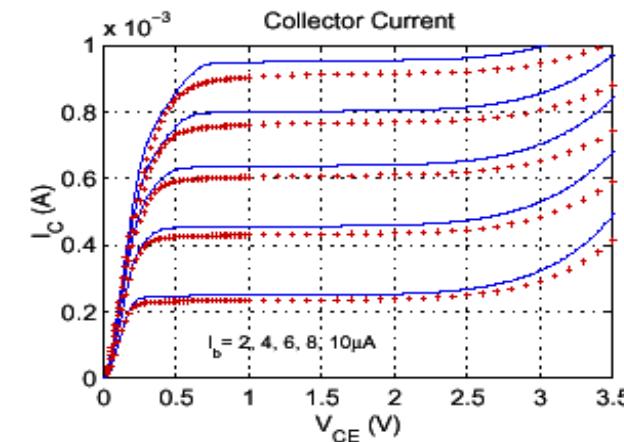
High  $V_{CE}$  depletes base = high beta

## SiGe HBTs

Base doping similar to Si

Higher  $V_A$  due to bandgap engineering

$\partial E_G$  increases  $V_A$





# **Technology Features, Device Library, Models and ROC**

# AutoHP: Introduction - Automotive Design

In addition to the standard foundry offering, an enhanced AutoPro flow has been defined to offer support for the AEC-Q100 standard (Part no.: 01XL074) with the following exceptions to the described commercial flow:

- AUTO:dg marking layer coincident with CHIPEDGE:dg required.
- 100 µm Through Silicon Via (70Y8337) feature prohibited for automotive designs.
- Enhanced crackstop methodology (84Y7710) required.
- Checking additional automotive ground rules, designated by an "A\_" prefix in the rule name.
- No waivers will be granted for severity class a and severity class b rule violations (severity class b rules will appear as class a after running through the parser).
- Severity class c rules should also be followed, and any violations are at the risk of the customer.
- Severity class d rules should be followed wherever space is available.
- Wafer edge exclusion zone will be set at 5 mm.
- The technology is qualified to AEC-Q100 Automotive Temperature Grade 1 standard, and can be used for Automotive Temperature Grade 1-3 products. Automotive Temperature Grade 1 junction temperature range is -40°C to +150°C for 15 years at 10% power on.
- The technology has completed package evaluation to Automotive standard AEC-Q100 Temperature Grade 1 stress conditions. Contact your GLOBALFOUNDRIES Field Application Engineer for packaging option status.

# Technology Features

## Standard Features

- 130 nm Twin-well on non-epi 11-16  $\Omega\text{-cm}$  substrate, low K dielectric
- Shallow (0.35  $\mu\text{m}$ ) and deep (6  $\mu\text{m}$ ) trench isolation
- 1.2/1.5V FETs with 22 $\text{\AA}$  gate oxide
- High Performance SiGe NPN transistors (8HP/8XP)
  - $f_T = 210/250$  GHz, 1.8/1.65V BVceo
- 5 to 8 levels of Cu and Al metal
  - AM: 2 to 4 levels thin 1X Cu, followed by MQ thick 2X Cu, LY Al (1.25  $\mu\text{m}$ ) and AM thick Al (4.0  $\mu\text{m}$ )
  - DM: 2 to 4 levels thin 1X Cu, followed by MQ thick 2X Cu, LY Al (1.25  $\mu\text{m}$ ), E1 Thick Cu (3.0  $\mu\text{m}$ ) and MA thick Al (4.0  $\mu\text{m}$ )
- Forward Bias, PIN and Schottky Barrier Diodes
- n<sup>+</sup> Diffusion, p<sup>+</sup> Poly and NS resistors
- Thin Oxide NMOS Varactor/Decoupling Capacitor
- Single-Layer inductors
- Parallel(high Q) and Series(high density) inductors
- Transmission Lines; RF Interconnect Lines
- Distributed (Microwave/Millimeter Wave) Passives – AM BEOL only
- Electrically Programmable Fuse
- ESD diodes and clamps
- Wire bond, solder bump (C4) terminals & Cu pillar

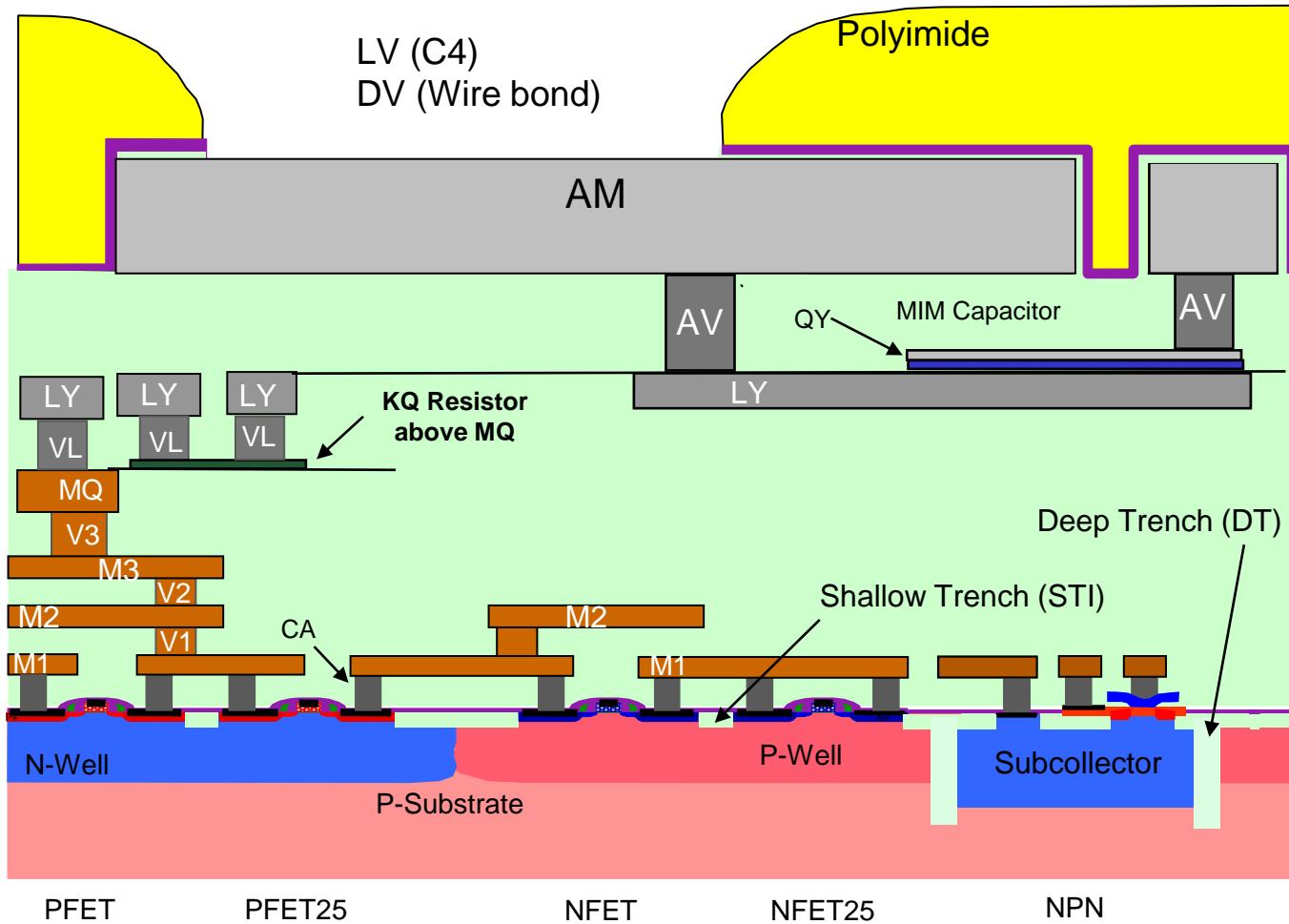
## Optional Features

- High Breakdown SiGe NPN (8HP/8XP)
  - $f_T = 60/67$  GHz, 3.55/3.25V BVceo
- 2.5V/3.3V Thick Oxide FETs; Tox = 52 $\text{\AA}$
- PI Triple-well NFETs
- T3 True Triple-well Isolation
- Vertical PNP\* ( $f_T = 17$  GHz, 8.2V BVceo)
- Thick Oxide NMOS Varactor/Decoupling Capacitor
- Hyper Abrupt (HA) Varactor
- Single and Dual Metal-insulator-metal (MIM) capacitors (1fF/ $\mu\text{m}^2$  & 3.1fF/ $\mu\text{m}^2$ )
- High Resistivity RR Poly resistor
- TaN metal KQ resistor
- Through Silicon Via (TSV2)\*\*
- Enhanced 1x Cu Wiring

\* Not qualified in 8XP

\*\* Not available for AutoHP

# Process Cross-Section\*



\*6 Levels of Metal AM  
Metal Option (wireopt 311) Shown with

3 1X Cu (M1, M2, M3)

1 2X Cu (MQ)

1 Thick 1.25  $\mu\text{m}$  Al (LY)

1 Thick 4.0  $\mu\text{m}$  Al (AM)

- TaN
- Polyimide
- Nitride
- Oxide
- Tungsten
- Aluminum
- Copper
- P-silicon
- N-silicon

# Metallization Options : AM Last Metal

- Number of metal levels: 5, 6, or 7
- 2 to 4 “1X thin” (0.32 µm) Cu layers (M1-M4)
  - M1 and M2 (Cu) required
  - M3 and M4 (Cu) optional
- 1 “2X thick” (0.55 µm) Cu layer (MQ) - Required
- 2 Last analog Al metal layers for high Q inductors (LY and AM) – Required

**M1-M2-M3-M4-MQ-LY-AM**

**(M3-M4 Optional)**

# Levels of Metal	BEOL Wiring Options					
	5	6	7			
Wiring Code	211	311	411			
Last Metal	AM	AM	AM			
LY	LY	LY	LY			
2X Level	MQ	MQ	MQ			
1X Level			M4			
		M3	M3			
	M2	M2	M2			
	M1	M1	M1			

Level	Metallurgy	Pitch (µm)	Thickness (µm)
M1	Cu	0.32	0.29
Mx	Cu	0.40	0.32
Vx	Cu	0.40	0.35
VL	Cu	0.80	0.65
MQ	Cu	0.80	0.55
VY	W	3.24	4.1
LY	Al	3.04	1.25
AV	W	3.24	4.1
AM	Al	2.8	4.0

# Metallization Options : Dual Metal E1/MA Last Metal

- Number of metal levels: 6-8
- 2 to 4 “1X thin” (0.32 µm) Cu layers (M1-M4)
  - M1-M2 Required
  - M3-M4 Optional
- 1 “2X thick” (0.55 µm) Cu layer (MQ) – Required
- 1 Al (1.25 µm) metal layer (LY) – Required
- 1 “Thicker” (3.0 µm) Cu layer (E1) – Required
- 1 Last analog Al (4.0 µm) metal layer (MA) – Required

**M1-M2-M3-M4-MQ-LY-E1-MA**

(M3-M4 Optional)

		BEOL Wiring Options					
# Levels of Metal (LoM)		6	7	8			
Wiring Code		213	313	413			
Last Metal		MA	MA	MA			
E1		E1	E1	E1			
LY		LY	LY	LY			
2X Level		MQ	MQ	MQ			
1X Level				M4			
				M3	M3		
				M2	M2	M2	
				M1	M1	M1	

Level	Metallurgy	Pitch (µm)	Thickness (µm)
M1	Cu	0.32	0.29
M2-M4	Cu	0.40	0.32
Vx (x=1,2,3)	Cu	0.40	0.35
VL	Cu	0.80	0.65
MQ	Cu	0.80	0.55
VY	W	3.24	4.1
LY	Al	3.04	1.25
AV	W	3.24	4.1
E1	Cu	2.50	3.0
F1	Cu	2.00	4.0
MA	Al	2.8	4.0

# BiCMOS8HP/XP Devices

Bipolars	FETs*	Diodes		Varactors	Capacitors	Resistors	Inductors	RF lines	Other Devices
HP npn <b>npn npncbe</b>	1.5V <b>n/pfet</b>	Forward Biased Diode <b>divpnp</b>	Single MIM <b>mim</b>	n+ Diffusion <b>opndres</b>	Single layer <b>ind/symind</b>	Terminals <b>bondpad</b>			
HB npn <b>npn</b>	2.5V/3.3V <b>dgnet/dgpfet</b>	HA Junction Varactor <b>havar</b>	Dual MIM <b>dualmim</b>	n+ Diffusion Subcollector <b>nsres</b>	Dual layer parallel <b>indp symindp</b>	Through Silicon Via <b>tsv2</b>			
Vertical PNP <b>vppn</b>	1.5V PI or T3 Isolated NFET/PFET <b>(nfettw/pfettw)</b>	MOS Varactor (thin oxide) <b>ncap</b>		p+ Poly <b>oppccres</b>	Dual layer Series <b>inds</b>	Electrical Fuse <b>efuse</b>			
	2.5V/3.3V PI or T3 Isolated NFET/PFET <b>(dgnfettw/dgpfettw)</b>	MOS Varactor (thick oxide) <b>dgnkap</b>		OP RR Poly <b>oprrpres</b>	RF Interconnect <b>rflne</b>	Distributed Passive** <b>bend/tee/.../...</b>			
		PIN Diode <b>pin</b>		TaN <b>kqres</b>	transmission line <b>singlewire couplewires</b>				
		Schottky Barrier Diode <b>sbd</b>			Coplanar Waveguide <b>singlecpw coupledcpw</b>				

\*NFET RF pcells (xxx\_rf) also included in the design kit for both thin oxide and thick oxide for standard and triple well configurations

\*\* AM only

# Documentation

- **Design Manual**
  - Device performance specifications, layout ground rules, use restrictions and some basic model equations are contained in the “Electrical Design Rules and Models” section of the Design Manual)
  - Technology and device use conditions, such as maximum voltage or temperature limits, for all of the devices documented here are as specified in the Design Manual
- **Model Reference Guide**
  - Brief overview of the Modeling methodology
  - Model library structure and usage
    - Simulation control switches
  - Description of the statistical process distributions and corner simulation methodology
  - For each device
    - Model features, restrictions, limitations, usage notes
    - Supported instance parameters
    - Model-to-Hardware correlation plots
    - Possible differences between any of the supported simulators (e.g. HSPICE vs SPECTRE)
    - Details on conditions used for device characterization or model extraction
- **ESD Reference Guide**
  - ESD Phenomena, Test Methods and Protection Strategy
  - ESD Device Physics, Data Summary, Relevant Technology Data
  - ESD Design Kit Description, Compact Models, Ground Rule Descriptions, Design Guidelines
- **Release Notes and/or User’s Guides for Each Supported EDA tool.**
- **Individual Model or Rule Deck Files (e.g. nfet.scs, drc.rul)**
  - Syntax, input parameter options and basic topology diagrams are included as comment lines at the top of most individual model or rule deck files

# BiCMOS8HP/8XP Design Manuals

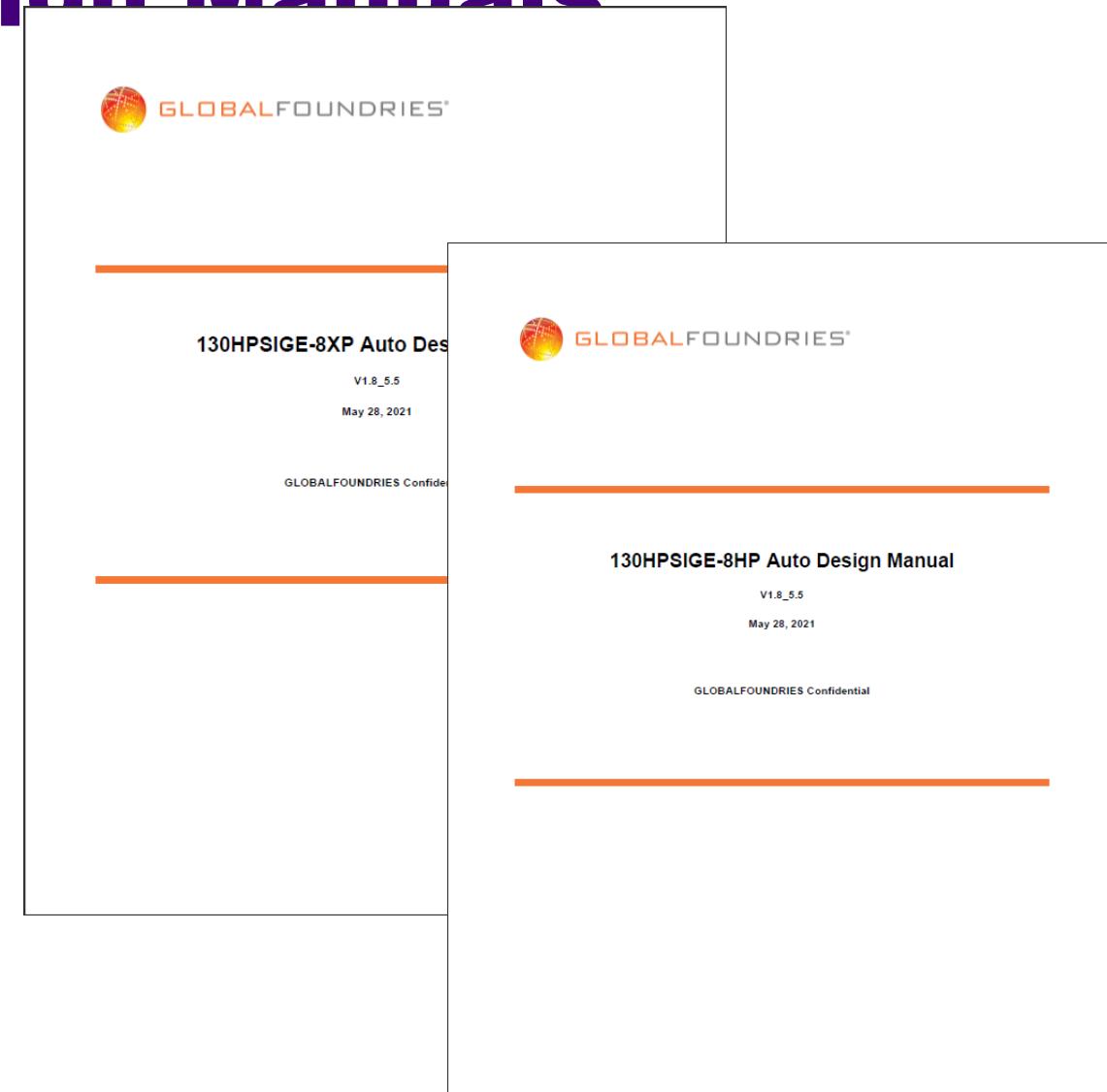
- **Structure consistent across technologies**

- 1: Technology Introduction
- 2: Physical Layout Information
- 3: Physical Design Rules
- 4: Electrical Parameters and Models
- 5: Reliability Design Rules and Models
- 6: Electrostatic Discharge (ESD) Protection
- 7: Design for Manufacturability
- Appendix
  - A: Guideline for Optimal Model-Hardware Correlation
  - B: Total Standby Current (Idd)
  - C: Design Hierarchy Guidelines
  - D: Rule Syntax (Definitions)
  - E: Definitions of Process-Related Terms
  - F: Migration into Future Technologies
  - G: Design preparation
  - H: Pattern Fill Rules
  - I: MxPLANE Information
  - J: NO\_BAT Rules
  - K: Decoupling Capacitor
  - L: Change List

- Design Manual located in **\$GF\_PDK\_HOME/doc**

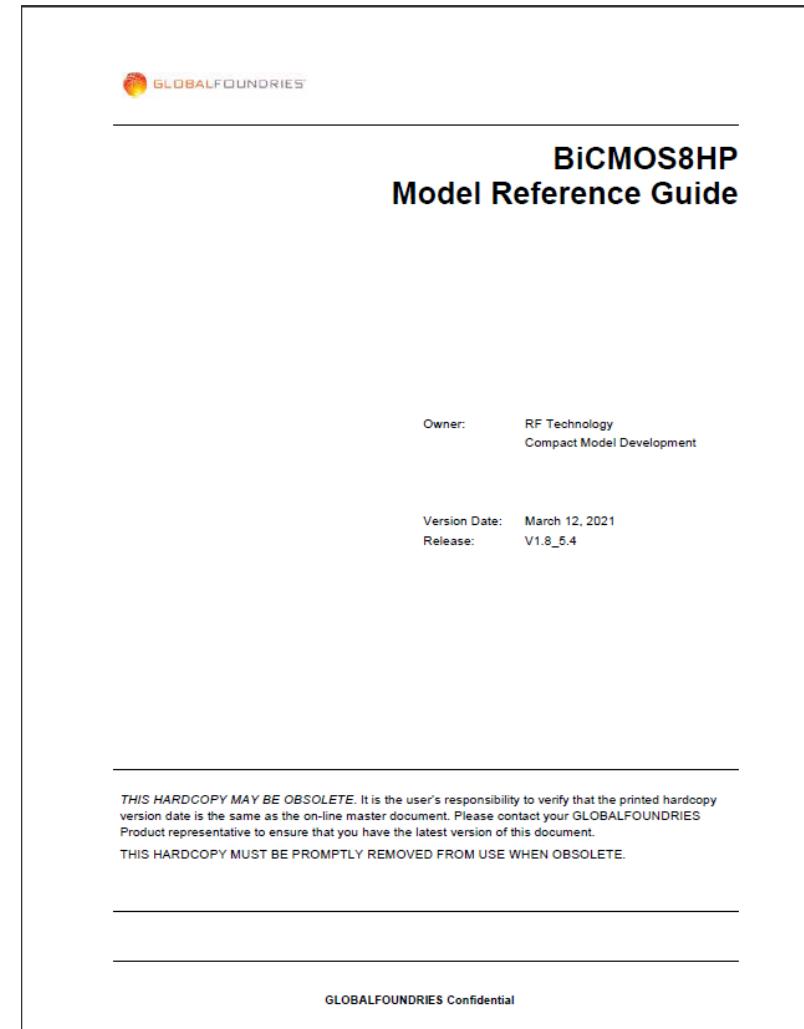
- Doc ID: 8HP DM-000418, 8XP Addendum: DM-000420

- BiCMOS8XP requires both DM-000418 and DM-000420



# BiCMOS8HP Model Reference Guide (MRG)

- Overview of Model Library and Control Switches in MRG
  - Global and local switches
  - Global custom corner parameters
  - Fixed corner model details
  - Device Variation and Mismatch
  - Example simulation settings
- Device Models in MRG
  - Device model features and limitations
  - Model to hardware correlation plots
- MRG located in **\$GF\_PDK\_HOME/doc**



# Models are Process-Based and Scalable

- **Design Flexibility through Scalable models**
  - Single model Applies over the Range of Allowed Device Sizes
  - Simplifies Design Optimization
- **Physics / Process Based Models**
  - Models based on physical structure, dimensions, resistances, etc.
- **Models written as sub-circuits**
  - Network wrapper around base model call (parasitics, distributed elements, etc.)
  - Common file for shared process parameters
    - *process.passive.scs* and *process.soi.scs* (Spectre), *process.lib* (HSPICE)
  - Model include file: *include.scs* (Spectre), *include.lib* (HSPICE)
  - Design file (parameter control): *design.scs* (spectre), *design.lib* (HSPICE)
- **Model Reference Guide contains Model Descriptions, Model-to-Hardware plots, and limitations**

# BiCMOS8HP ESD Reference Guide

- **ESD Reference Guide includes all aspects of ESD design:**
- ESD Phenomena and Test Methods
- ESD Protection Strategy Background
- ESD Device Physics
- ESD Design Kit Description
- ESD Design Kit Data
- ESD Compact Models
- ESD Ground Rule Descriptions and Checking
- ESD Design Review\*
- ESD Design Guidelines

**Other ESD information can also be found in the following sources:**

- Design Manual
- Model Reference Guide
- cdslib User's Guide

130HPSIGE-8HP ESD Reference Guide

## 130HPSIGE-8HP ESD Reference Guide

Date: 07/17/20

### Document History:

Design Manual	Reference Date	ESD Design Kit Version	ESD Reference Guide Date
PLM# DM-000418	07/17/20	V1.8_5.0	07/17/2020

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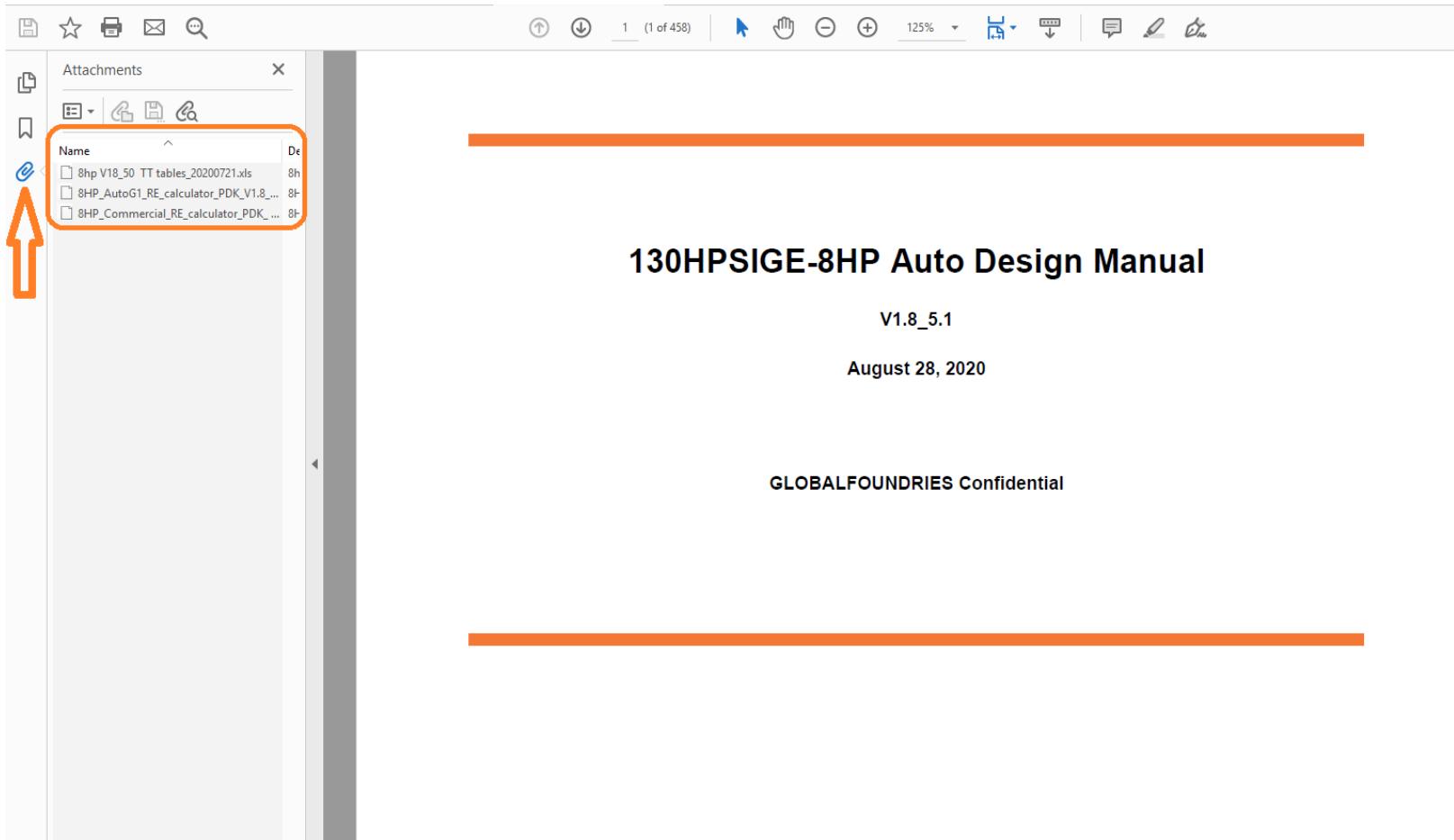
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# Technology Operating and Burn-In Range

- Commercial Operating Temperature Range : -55 to 125<sup>o</sup>C\* (Junction/Silicon Temperature)
- Automotive Temperature Grade 1 junction temperature range is -40<sup>o</sup>C to +150<sup>o</sup>C for 15 years at 10% power on
- Burn-in Temperature: 140<sup>o</sup>C Maximum
- Burn-in Voltage: Vdd = 1.925V for 1.2V circuits, 2.375V for 1.5V circuits, and 3.875V for 2.5V circuits
- See Section 5.2 in Design Manual

# Reliability Calculator

- The SiGe 8HP Reliability Calculator is included as an attachment to this document.



# Junction Diode Breakdown Voltages

## 4.7.1 STI-Bounded Breakdown

Table 4-15. STI-Bounded Junction Breakdown Voltage (V)

P+ / N-Well	N+ / P-Well	N-Well / Substrate
> 10.5	> 10.5	> 10

Table 4-16. Intra-well punch through voltage (V),  $I_L = 1 \text{ nA}/\mu\text{m}$

Diffusion Space	n+ / n+	p+ / p+
0.18 $\mu\text{m}$	> 4	> 7
0.36 $\mu\text{m}$	> 4	> 7

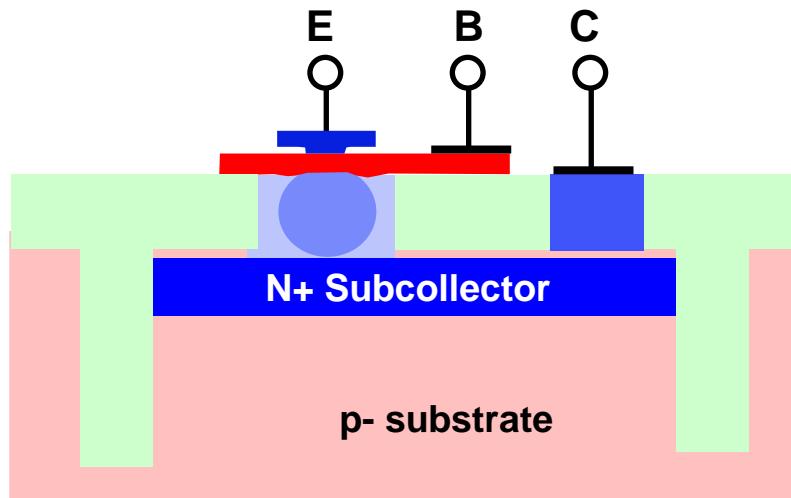
# Current Limit: Metal Lines, Studs and Contacts

- See Electro-migration Rules in Section 5.4, “Back End Of Line (BEOL) Reliability”, in the BiCMOS8HP Design Manual
- General Rules are given for 100°C at 100KPOH
- For other operating conditions, adjustment factors are given in the Design Manual
- There are no design rule checks for electro-migration
  - Cadence Voltus\_FI and Ansys Redhawk\_Totem EMIR tools are supported for EMIR analysis

Metal Level	I <sub>dc</sub> (mA) <sup>1</sup> at 100°C	I <sub>dc</sub> (mA) <sup>2</sup> at 125°C	I <sub>rms</sub> (mA) <sup>1</sup>	I <sub>dc</sub> <sup>1</sup> (mA) min. W at 100°C	I <sub>dc</sub> <sup>1</sup> (mA) min. W at 125°C	I <sub>rms</sub> <sup>1</sup> (mA) min. W
PC <sup>3</sup>	N/A	N/A	$(0.61(W - 0.015)) \sqrt{3.77 + \frac{4.54}{(W - 0.015)}}$	N/A	N/A	0.44
M1 (Cu)	2.80 (W - 0.0625)	0.57 (W - 0.0625)	$(3.58(W - 0.063)) \sqrt{7.47 + \frac{13.63}{(W - 0.0625)}}$	0.273	0.0554	4.24
M2 (Cu)	3.12 (W - 0.07)	0.63 (W - 0.07)	$(2.89(W - 0.07)) \sqrt{6.25 + \frac{18.95}{(W - 0.07)}}$	0.406	0.0824	4.63
M3 (Cu)	3.12 (W - 0.07)	0.63 (W - 0.07)	$(2.5(W - 0.07)) \sqrt{5.50 + \frac{22.09}{(W - 0.07)}}$	0.406	0.0824	4.31
M4 (Cu)	3.12 (W - 0.07)	0.63 (W - 0.07)	$(2.27(W - 0.07)) \sqrt{5.03 + \frac{24.36}{(W - 0.07)}}$	0.406	0.0824	4.09
M1 (Cu+) <sup>4</sup>	Limited by I <sub>max</sub> <sup>5</sup>	2.80 (W - 0.0625)	$(3.58(W - 0.063)) \sqrt{7.47 + \frac{13.63}{(W - 0.0625)}}$	0.568 <sup>5</sup>	0.273	4.24
M2 (Cu+) <sup>4</sup>	Limited by I <sub>max</sub> <sup>6</sup>	3.12 (W - 0.07)	$(2.89(W - 0.07)) \sqrt{6.25 + \frac{18.95}{(W - 0.07)}}$	0.845 <sup>6</sup>	0.406	4.63
M3 (Cu+) <sup>4</sup>	Limited by I <sub>max</sub> <sup>6</sup>	3.12 (W - 0.07)	$(2.5(W - 0.07)) \sqrt{5.50 + \frac{22.09}{(W - 0.07)}}$	0.845 <sup>6</sup>	0.406	4.31
M4 (Cu+) <sup>4</sup>	Limited by I <sub>max</sub> <sup>6</sup>	3.12 (W - 0.07)	$(2.27(W - 0.07)) \sqrt{5.03 + \frac{24.36}{(W - 0.07)}}$	0.845 <sup>6</sup>	0.406	4.09
MQ (Cu)	5.4 (W - 0.075)	1.10 (W - 0.075)	$(2.47(W - 0.075)) \sqrt{5.41 + \frac{34.32}{(W - 0.075)}}$	1.755	0.356	8.45
LY (Al)	1.77 (W - 0.17)	0.706 (W - 0.17)	$(2.59(W - 0.17)) \sqrt{2.78 + \frac{38.96}{(W - 0.17)}}$	2.354	0.939	19.47
AM (Al)	5.625 (W - 0.14)	2.24 (W - 0.14)	$(2.66(W - 0.14)) \sqrt{5.29 + \frac{120.83}{(W - 0.14)}}$	10.463	4.174	41.70
E1 (Cu)	16.02 (W - 0.205)	3.25 (W - 0.205)	$(3.22(W - 0.205)) \sqrt{6.12 + \frac{90.82}{(W - 0.205)}}$	20.746	4.211	36.41
MA (Al)	5.625 (W - 0.14)	2.24 (W - 0.14)	$(2.39(W - 0.14)) \sqrt{4.76 + \frac{131.33}{(W - 0.14)}}$	10.463	4.174	38.89

# NPN Transistors (npn, npncbe\*)

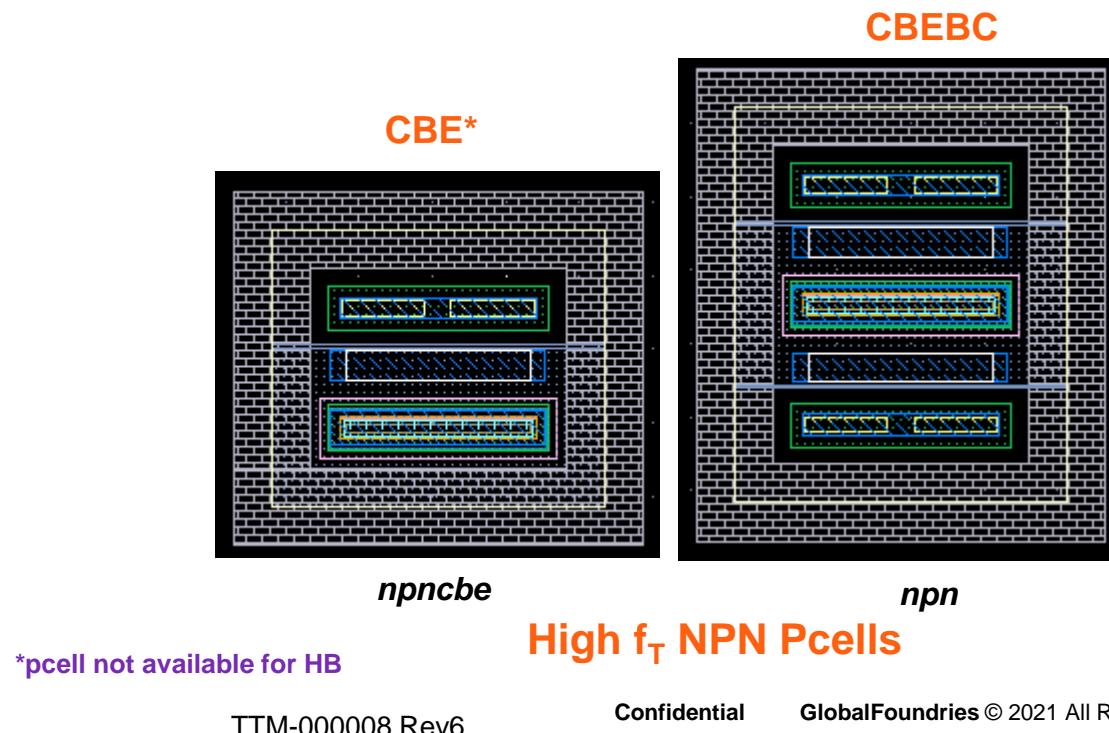
- High  $f_T$  (HP) and High Breakdown (HB)
- Fixed Emitter Width  $W = 0.12 \mu\text{m}$
- Scalable Emitter Lengths  $L = 0.52\text{-}18 \mu\text{m}$
- Single Stripe Emitter only



**The CBEBC is the preferred configuration**

- Very high peak  $f_T$  current density in 8HP NPNs requires careful consideration. CBEBC has improved performance- higher  $f_T$  and  $f_{max}$
- Two collector contacts required to carry  $I_c$  at peak  $f_T$
- Emitter need to be wired from M2

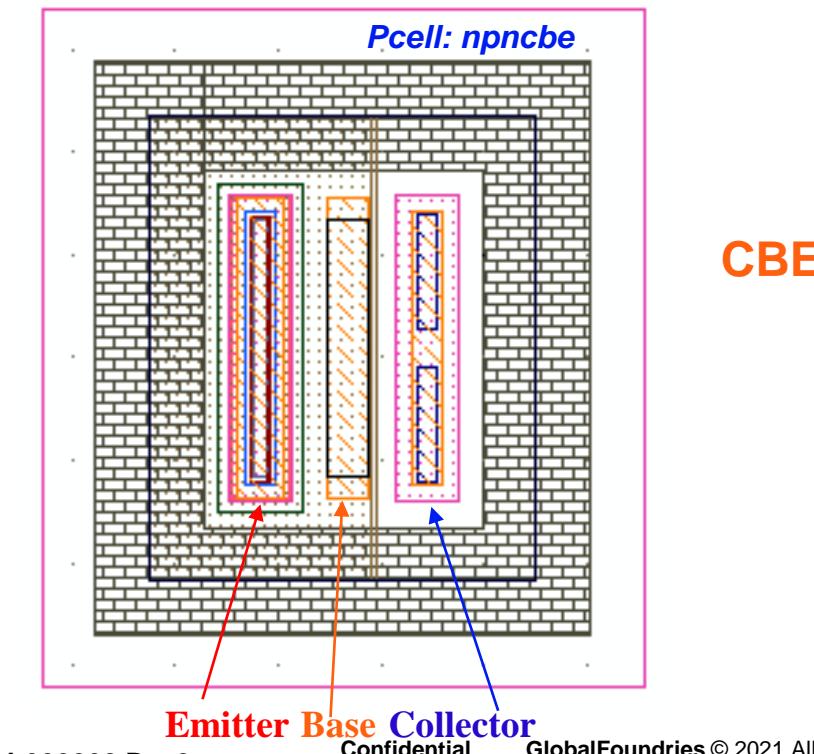
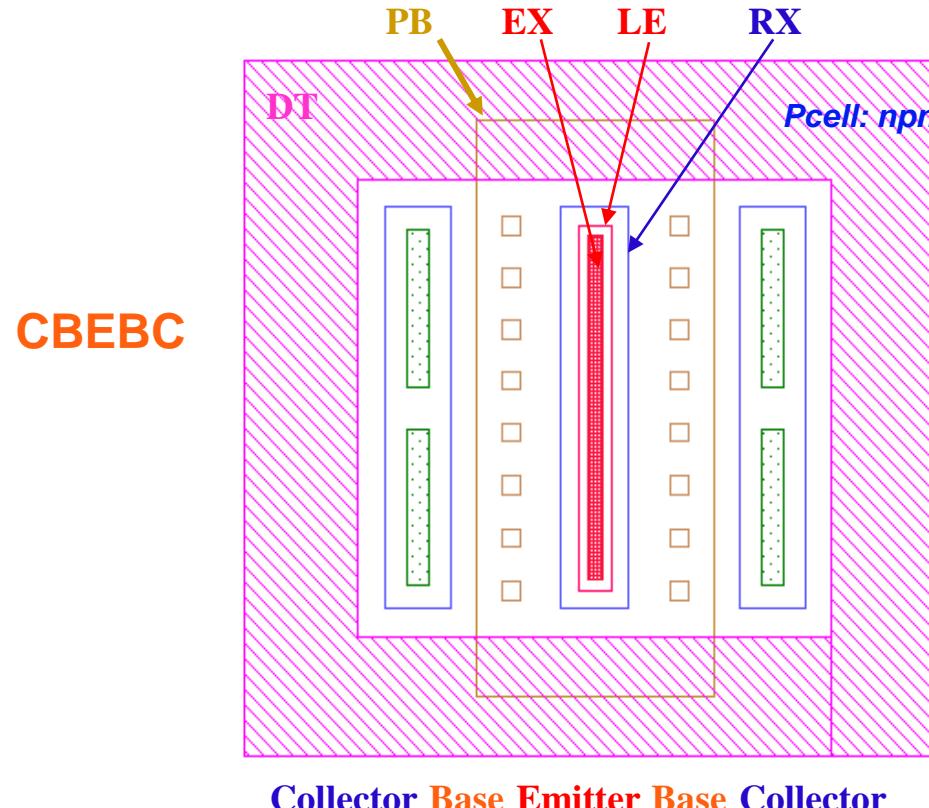
Device	Peak $f_T$ (GHz)	$I_c @ Pk f_T$ (mA/ $\mu\text{m}^2$ )	$\beta$	BV <sub>ceo</sub> (V)	Configurations
High $f_T$ (8HP/8XP)	210/250	12/15	460/450	1.8/1.65	CBE, CBEBC
High Breakdown (8HP/8XP)	60/75	1.4/2.0	400/550	3.55/3.25	CBEBC



\*pcell not available for HB

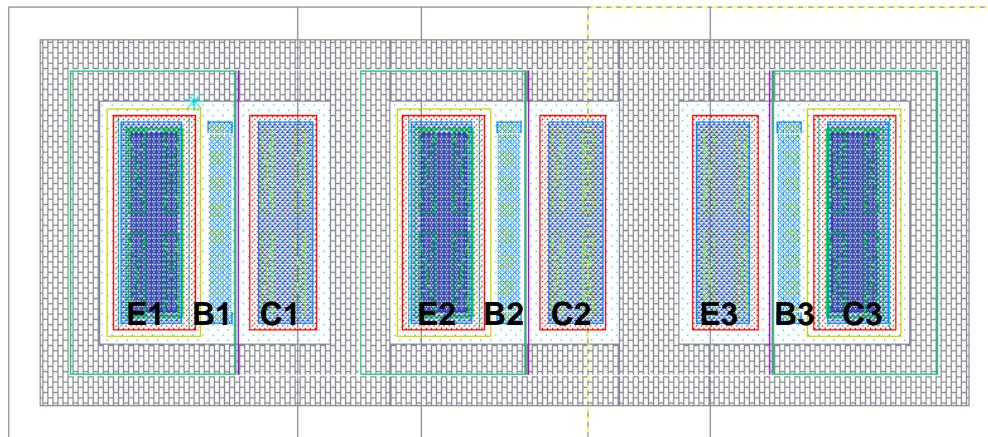
# CBEBC vs. CBE

- 8HP/8XP NPNs have very high peak  $f_T$  current density. Wiring requires careful consideration
- CBEBC configuration has higher  $f_T$  and  $f_{max}$ . It is the recommended configuration from a performance and reliability perspective.
  - Collector contacts from two sides
  - Top-down Emitter-contact from M2 directly to M1, then to CA, to emitter
- Use CBE if the collector current density is low and smaller footprint is needed

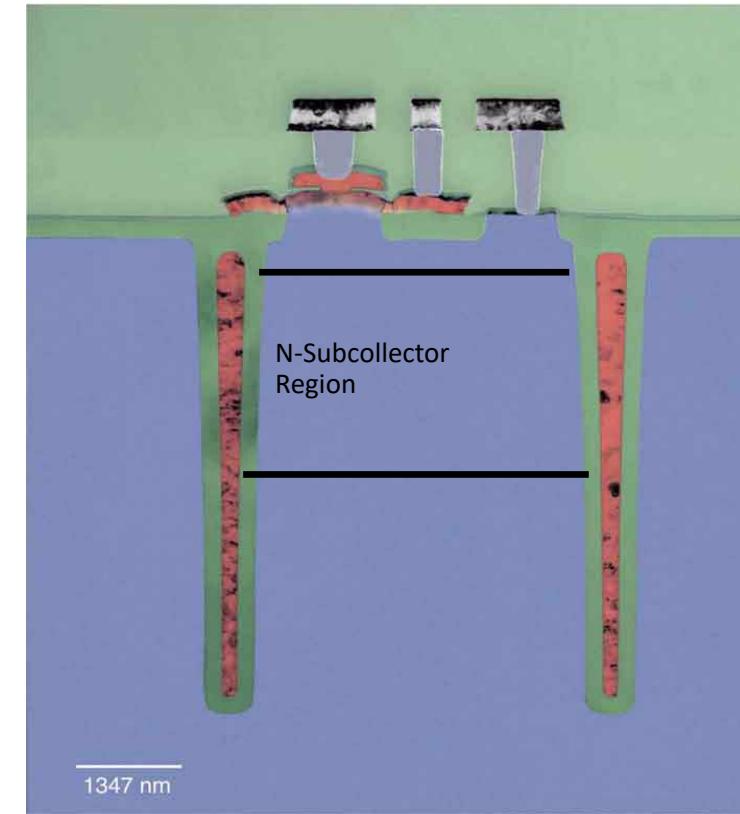


# npn Transistors May Share DT

- Deep trench (DT) isolates adjacent sub-collectors
- Share DT ONLY if density is of utmost priority
  - Model accuracy may be compromised
    - Coupling through DT not modeled
  - Thermal Effects may be significant



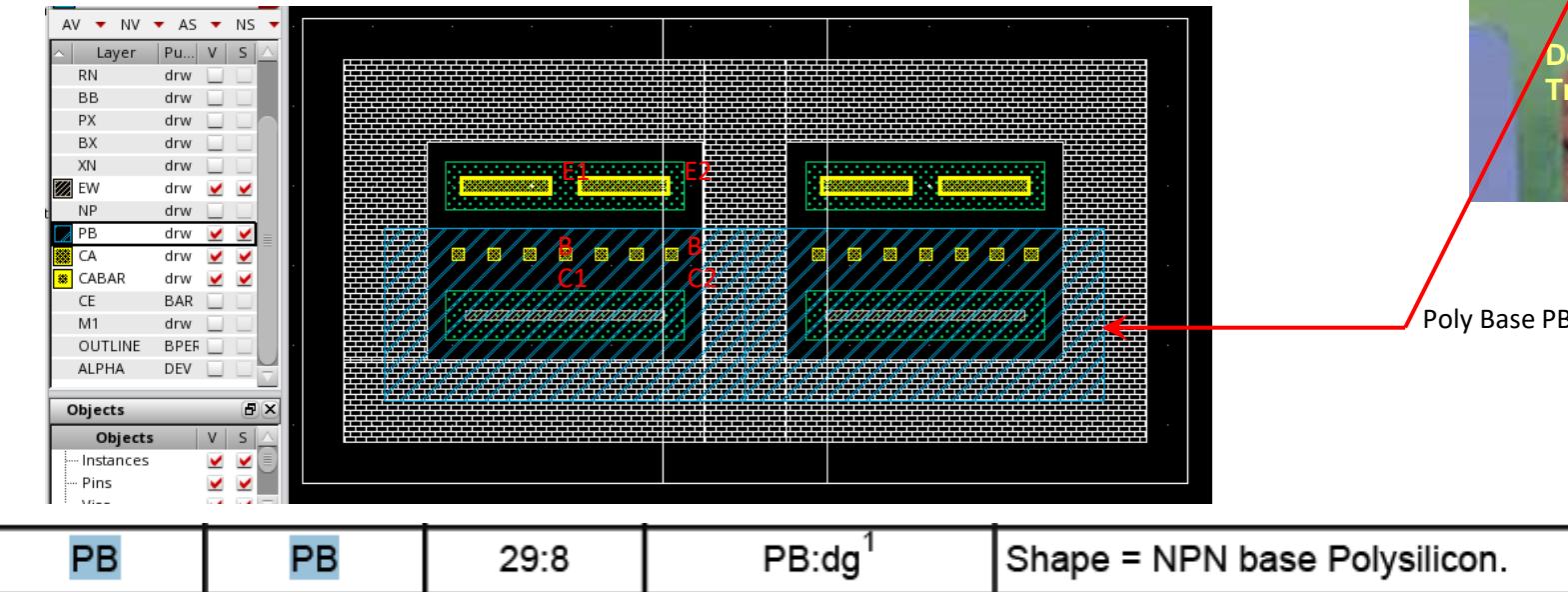
An example of DT sharing with distinct terminals



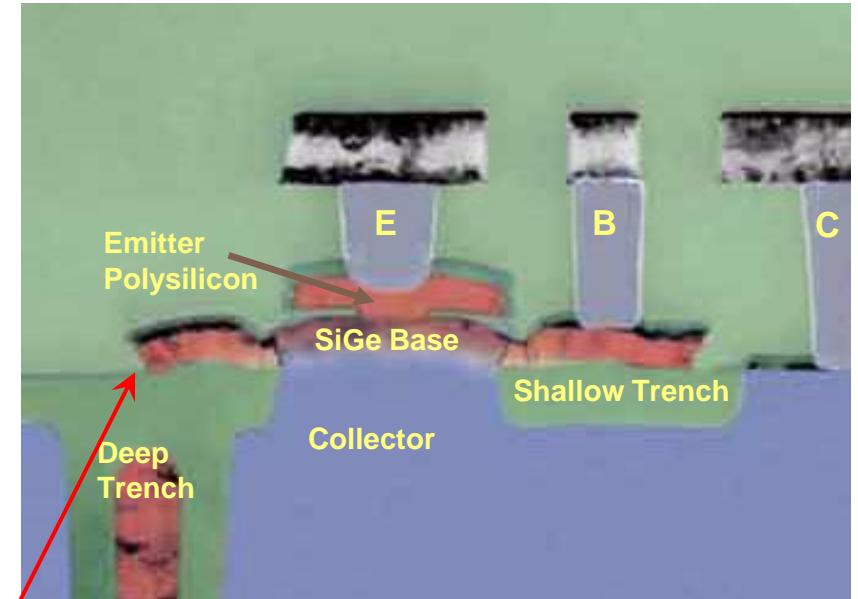
DT is deep enough to cut through each sub-collector region

# Sharing DT with Bases abutted

- Deep trench (DT) isolates adjacent sub-collectors
- If PB (poly base) shapes touch, they will be soft-shorted
- Wire the shared bases in metal as well.



An example of base (PB) touching



# npn Pcell Options (Schematic View)

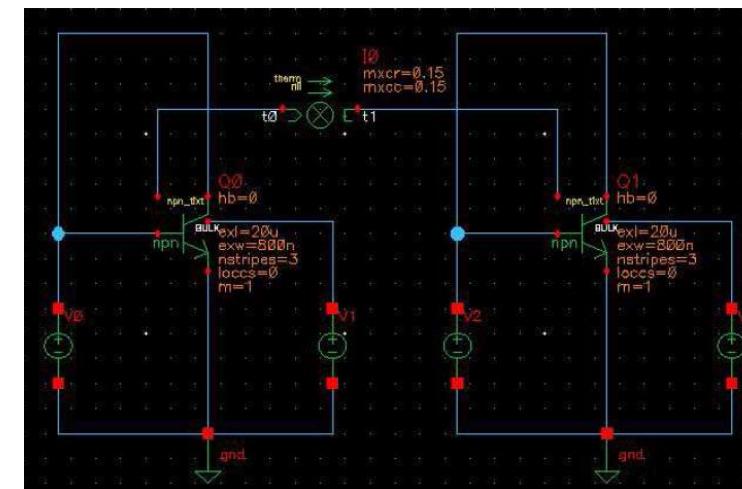
Device Type (High_fT or High_Breakdown)	Performance/Breakdown	High_fT
NPN Size. Emitter Length is fixed.	Emitter Length	2.5 $\mu$ M
Recommended for High Peak current (Wider collector metal width)	Emitter Width	120.0n <input type="button" value="▼"/>
Select to set base metal width to accommodate applications requiring high base current	Reliability Layout?	<input checked="" type="checkbox"/>
Number of Instance copies	Include Base Contacts?	<input checked="" type="checkbox"/>
Override Substrate Resistance? Default Setting recommended. Model includes estimated substrate parameters	Multiplicity	1
Temperature Above Ambient	Sub Resistance	-1 Ohms
Displayed Info for Design Aid	Temperature Delta	0.0 C
Self heating and ion impact were used in model characterization. Leave ON unless non-critical device.	Peak fT current	3.5609m A
Suppress/allow warnings $V_{C-E} > BV_{CEO}$	Use self heating?	<input checked="" type="checkbox"/>
Override Thermal Impedance	Use ion impact?	<input checked="" type="checkbox"/>
	BVceo warnings?	<input checked="" type="checkbox"/>
	Therm Impedance Mult	1.0

# NPN Explicit Thermal Node and Thermal Coupling Structure

- 4-node and 5-node symbols provided, models are identical with the exception of the number of nodes that are netlisted.
  - Float the thermal node of 5-node symbol will give the same simulation result using 4-node symbol
  - Ground the thermal node of 5-node symbol will disable the self-heating effect ( $sh=0$ )
  - Do not tie the thermal nodes of two symbols together which is non-physical.

Model	8HP NPN Process		8XP NPN Process	
	4-node	5-node	4-node	5-node
	npn	npnpt	npnxp	npnxpt

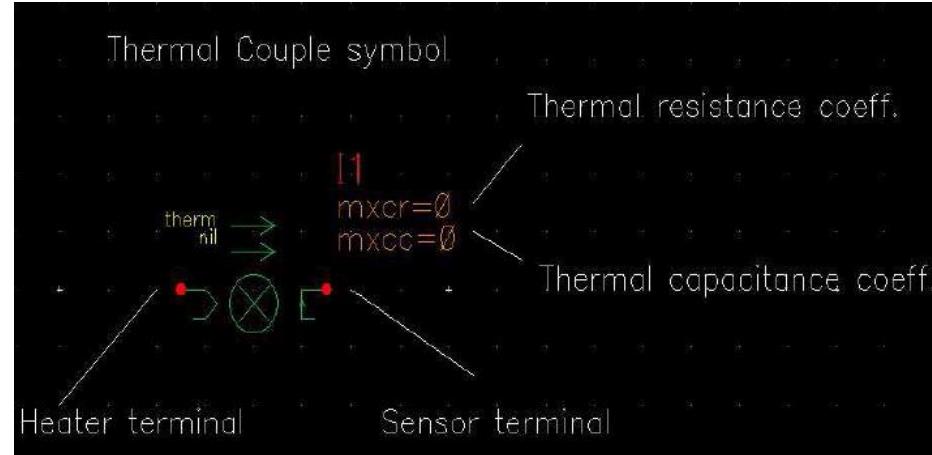
- For general purpose, may use *therm* symbol to simulate thermal coupling between npn devices
  - Need enable the thermal coupling structure switch ( $thcc=1$ ) in CDF of the sensor device(s)
- For limited Use Case which devices are electro-thermally equal in parallel, may override thermal impedance multiplier in Pcell.
  - Model use 1 for thermal impedance multiplier ( $mth=1$ )



Detail usage please see Model Reference Guide Section 3.1.2 “Thermal Coupling Structure”, and cdslib users guide section 5.3 “Bipolar Transistors”

# therm symbol

- **Symbol only, intended to be used only between npn thermal nodes**
- **VerilogA model file ‘thxc.va’**
- **Represent one way coupling of the heater device to the sensor device.**
  - Use more than one for either mutual coupling or multiple coupling
- **Placed only in the same level or higher level of the cellview as the transistor to which it is connected**
- **Separate resistance and capacitance thermal coupling coefficients are provided.**
  - Setting both coefficients to zero will set the thermal coupling effect to zero
  - Suggested values as a function of the relative spacing between device layouts are planned for a future PDK release



# NPN Device Modeling

- HiCUM (High Current Model) model
  - HiCUM allows accurate predictive and statistical modeling
  - Expected to provide better results over a wide range of bias, frequency, temperature, geometries
- Model features include many effects:
  - High current effects including quasi-saturation
  - Distributed high frequency model for the external B-C region
  - Emitter periphery injection and associated charge-storage
  - Emitter current crowding through a bias dependent internal base resistance
  - 2-D and 3-D Collector current spreading
  - Explicit inclusion of all parasitic (extrinsic) B-E and B-C junction and overlap capacitances
  - Vertical non-quasi static effects for transfer current and minority charge
  - Temperature dependence and Self-heating
  - Weak Avalanche multiplication at the B-C junction
  - Tunneling in the B-E junction
  - Parasitic substrate transistor and a substrate network
  - Bandgap difference occurring in HBTs
  - Lateral (geometry) scaling
- Model is optimized with self-heating and impact-ionization switches on. These switches can be turned off to speedup simulation with less accuracy.

# NPN Spectre Operating Region Check

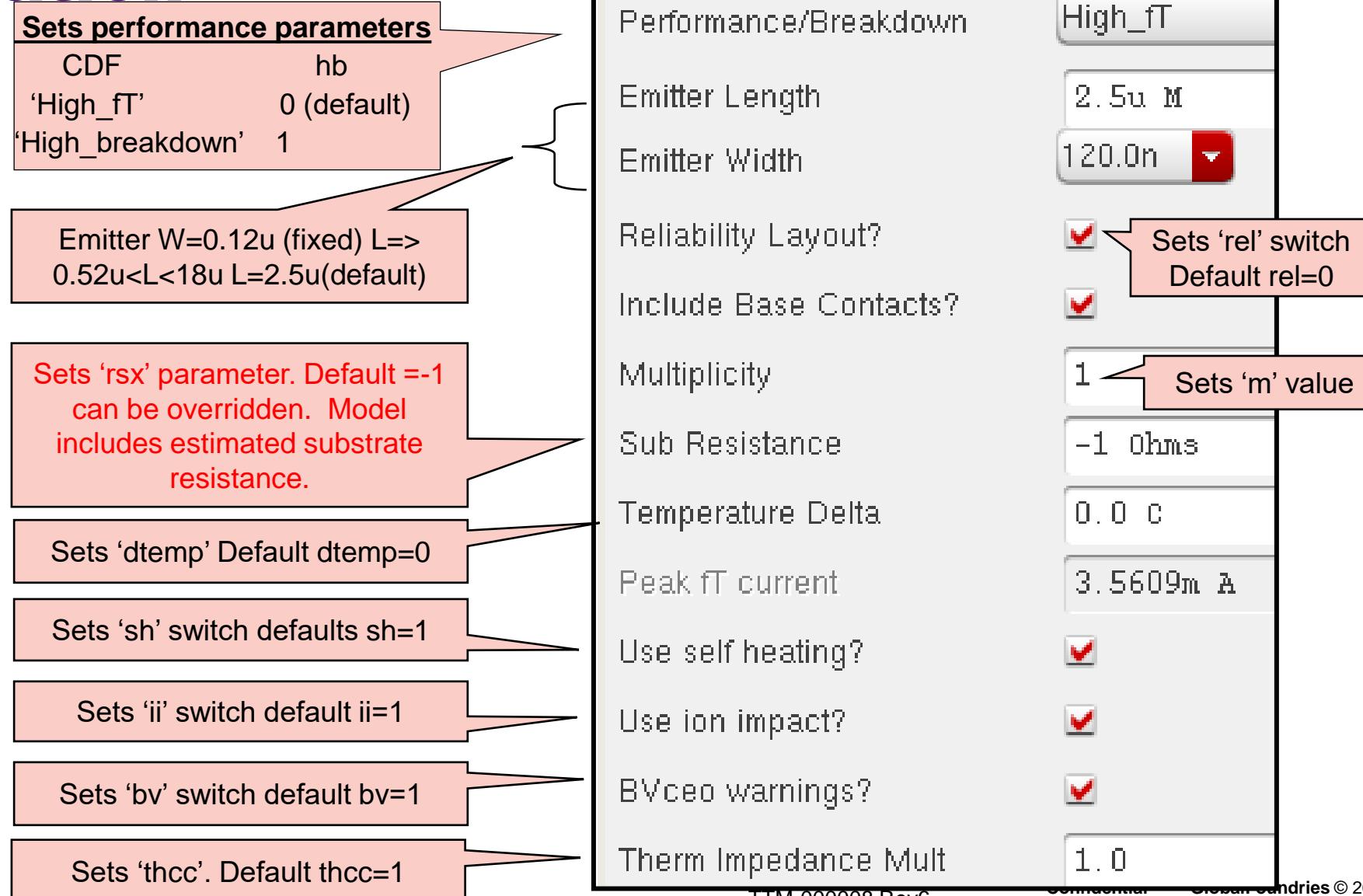
- Spectre NPN model files include "assert" statements which are used to check node voltage limits as documented in the design manual:
  - E-B breakdown voltage - minimum BV<sub>ebo</sub>
  - C-B breakdown voltage - minimum BV<sub>cbo</sub>
  - C-E breakdown voltage - nominal BV<sub>ceo</sub>
    - user may specify V<sub>ce</sub> level at which warning gets issued in design.scs file
      - vcep<sub>d</sub> Specifies C-E voltage to use in breakdown check for HP NPNs.
      - vceb<sub>b</sub> Specifies C-E voltage to use in breakdown check for HB NPNs

***Example of the warning message that will be generated during simulation if any of these voltage limits are exceeded:***

```
Warning from spectre at dc = xx V during DC analysis 'xxx'.
q.bvceo_check, instance xx.q: Collector to Emitter voltage on device terminals exceeds nom BVceo @ 10uA
spec. Expression 'v(c,e)' having value 3.85 V has exceeded its upper bound '3.55'.
```

Simulation results are not affected by these warnings, but designers should review the bias conditions of all devices identified as violating these voltage limits

# Setting Switches/parameters in npn CDF for simulation



# NPN Reliability Limitations

- **Device Group:** NPN
- **Device Names:** npn (High\_fT, High\_Breakdown)
- **See DM Section 5.5.8 Bipolar Reliability**
  - Reverse emitter junction voltage is limited to 1.75 V (see Reverse stress degradation model in RE Calculator)

**The base-collector avalanche operation causes the increase of the base current non-ideality.  
As long you operate the devices with VBC less than 1.5V, degradation is negligible**

# Breakdown Voltage Limits : 8HP High Performance NPN

- Device Group: High Performance NPN
- Device Names: npn (High\_fT)

Table 4-2. Electrical Parameters for Regular High Performance (HP) NPN (0.12 um x 2.5 um)

Parameter	Units	Minimum	Nominal	Maximum	Conditions
$V_{BE}$	Volts	0.703	0.728	0.753	$I_C = 10 \mu A, V_{CB} = 0.2 V$
Beta		100	460	800	$V_{BE} = 0.72 V, V_{CB} = 0 V$
$R_E$ without TSV	Ohms	1	4	8	Roll-over test, $I_E = 5 mA$
$R_E$ with TSV	Ohms	1	6	11	Roll-over test, $I_E = 5 mA$
$f_T$ (peak) <sup>1</sup>	GHz	180	210	240	$V_{CB} = 0.5 V$
$BVEBO$	Volts	1.2	2.3	4.0	$I = 10 \mu A$
$BVCBO$	Volts	5.5	6.0	7.0	$I = 10 \mu A$
$BVCEO$	Volts	1.5	1.8	2.5	$I = 10 \mu A$
$BVCSO$	Volts	20	50		$I = 10 \mu A$

1. With TSV,  $f_T$  decreases correspondingly due to the higher  $R_E$ . For example, an  $R_E$  change from 4 to 6 Ohm, reduces peak  $f_T$  by ~5GHz.

# Breakdown Voltage Limits : 8HP High Breakdown NPN

- Device Group: High Breakdown NPN
- Device Names: npn (High\_Breakdown)

**Table 4-3: Electrical Parameters for Regular High Breakdown (HB) NPN (0.12 μm x 2.5 μm)**

Parameter	Units	Minimum	Nominal	Maximum	Conditions
$V_{BE}$	Volts	0.705	0.730	0.755	$I_C = 10 \mu A, V_{CB} = 0.2V$
Beta	-	90	400	800	$V_{BE} = 0.72V, V_{CB} = 0V$
$f_T(\text{peak})$	GHz	45	60	75	$V_{CB} = 1.0V$
$BVEBO$	Volts	1.2	2.4	4.0	$I = 10 \mu A$
$BVCBO$	Volts	9	12	15	$I = 10 \mu A$
$BVCEO$	Volts	3.1	3.55	4.5	$I = 10 \mu A$
$BVCSO$	Volts	20	50	-	$I = 10 \mu A$

**Note:** In the above tables,  $BV_{CEO}$  is not a voltage limit for biasing unless the NPN is operated under a forced  $I_b$  condition.  $V_{CE}$  greater than  $BV_{CEO}$  is allowed for other bias configurations, lower base impedance leading to higher voltage limits.

# Breakdown Voltage Limits : 8XP High Performance NPN

- Device Group: High Performance NPN
- Device Names: npn (High\_fT)

**Table 4-2: Electrical Parameters for Enhanced High Performance (XP) NPN (0.12 μm x 2.5 μm)**

Parameter	Topology	Units	Minimum	Nominal	Maximum	Conditions
$V_{BE}$	CBE	Volts	0.697	0.717	0.737	$I_C = 10 \mu A, V_{CB} = 0.2$
Beta	CBE	-	150	650	1150	$V_{BE} = 0.72V, V_{CB} = 0$
$R_E$ without TSV	CBE	Ohms	1	5	12	Roll-over test, $I_E = 5 \text{ mA}$
$R_E$ with TSV	CBE	Ohms	2	7	14	Roll-over test, $I_E = 5 \text{ mA}$
$f_T(\text{peak})^1$	CBEBC	GHz	230	260	300	$V_{CB} = 0.3V$
$f_{MAX}(\text{peak})$	CBEBC	GHz	310	350	390	$V_{CB} = 0.3V$
$BVEBO$	CBE	Volts	1.2	2.4	3.8	$I = 10 \mu A$
$BVCBO$	CBE	Volts	5.4	5.8	6.4	$I = 10 \mu A$
$BVCEO$	CBE	Volts	1.45	1.65	2.1	$I = 10 \mu A$
$BVCSO$	CBE	Volts	20	50	-	$I = 10 \mu A$

**Note:**

1. With TSV,  $f_T$  decreases correspondingly due to the higher RE. For example, an  $R_E$  change from 5 to  $7\Omega$ , reduces peak  $f_T$  by ~5GHz.

# Breakdown Voltage Limits : 8XP High Breakdown NPN

- Device Group: High Breakdown NPN
- Device Names: npn (High\_Breakdown)

**Table 4-3: Electrical Parameters for Enhanced High Breakdown (XB) NPN (0.12 μm x 2.5 μm)**

Parameter	Topology	Units	Minimum	Nominal	Maximum	Conditions
$V_{BE}$	CBEBC	Volts	0.694	0.714	0.734	$I_C = 10 \mu A, V_{CB} = 0.2$
Beta	CBEBC	-	150	650	1150	$V_{BE} = 0.72V, V_{CB} = 0$
$f_T(\text{peak})$	CBEBC	GHz	63	78	96	$V_{CB} = 1.0V$
$f_{MAX}(\text{peak})$	CBEBC	GHz	230	265	310	$V_{CB} = 1.0V$
$BVEBO$	CBEBC	Volts	1.2	2.4	3.8	$I = 10 \mu A$
$BVCBO$	CBEBC	Volts	10.7	11.8	12.9	$I = 10 \mu A$
$BVCEO$	CBEBC	Volts	2.7	3.2	3.7	$I = 10 \mu A$
$BVCSO$	CBEBC	Volts	20	50	-	$I = 10 \mu A$

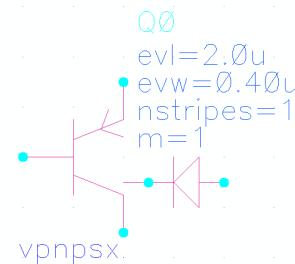
**Note:** In the above tables, BVceo is not a voltage limit for biasing unless the NPN is operated under a forced Ib condition. Vce greater than BVceo is allowed for other bias configurations, lower base impedance leading to higher voltage limits.

# Vertical PNP Transistor\* (vpnpsx)

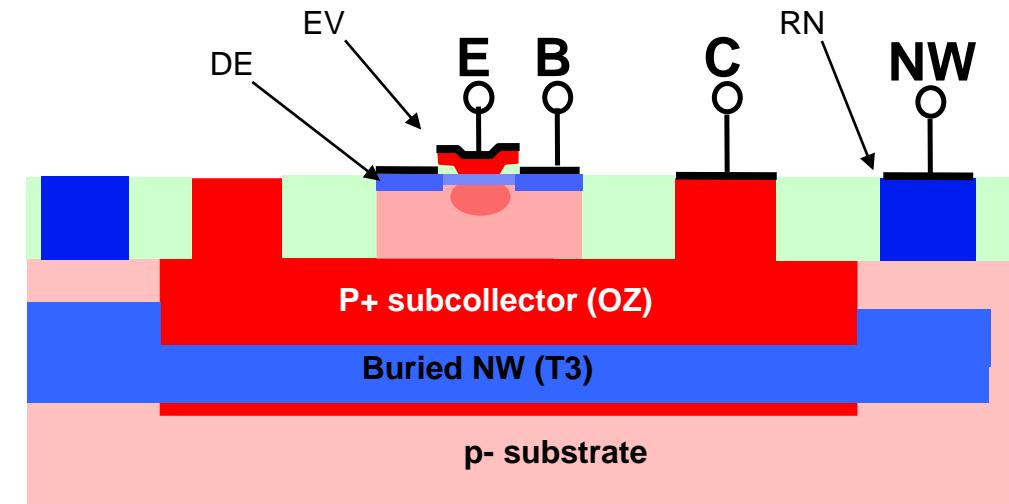
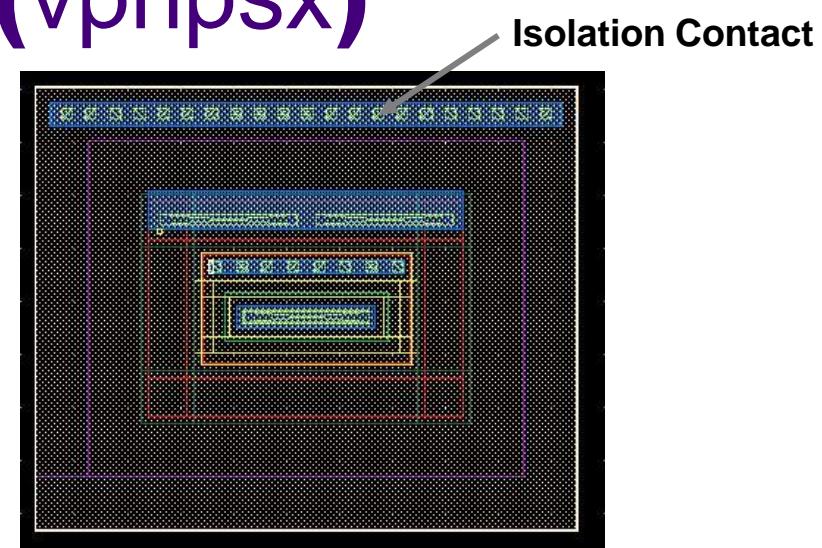
- Optional device: 4 Mask adder (OZ, EV, DE, T3)
- Single and dual striped layouts supported
- 0.4 and 0.8  $\mu\text{m}$  supported emitter (EV) widths and lengths up to 20 $\mu\text{m}$ 
  - Minimum Emitter length 1.2 $\mu\text{m}$  for 0.4 $\mu\text{m}$  width
  - Minimum Emitter length 2.4 $\mu\text{m}$  for 0.8 $\mu\text{m}$  width
- Typical Beta 230 (80 minimum)
- Typical  $f_T$  17 GHz (15 GHz minimum)

## CDF Options:

Emitter configuration [1 or 2 stripes]  
Emitter width [0.4 or 0.8 $\mu\text{m}$ ]  
Emitter length [1.2 or 2.4-20 $\mu\text{m}$ ]  
Base M1 width  
Collector contact rows  
Isolation contact configuration



\*Device not qualified in 8XP



# VPNP Electrical Parameters

Table 4-4: Electrical Parameters for the Vertical PNP (0.4  $\mu\text{m}$  x 2.5  $\mu\text{m}$ , Single Emitter)

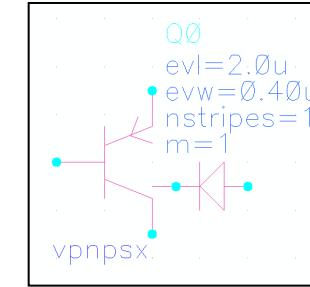
Parameter	Units	Minimum	Nominal	Maximum	Conditions
$V_{BE}$	Volts	-0.775	-0.790	-0.805	$I_C = -10 \mu\text{A}, V_{CB} = 0\text{V}$
Beta	-	80	230	450	$V_{BE} = -0.78\text{V}, V_{CB} = 0\text{V}$
$f_T(\text{peak})$	GHz	15	17	19	$V_{CB} = -3\text{V}, I_C = \sim 0.5 \text{ mA}/\mu\text{m}^2$
$V_{\text{Early}}$	Volts	12	30	60	$V_{BE} = -0.8\text{V}, V_{CE} = -2\text{V} \rightarrow -3.75\text{V}$
BVEBO	Volts	2.4	2.8	20	$I = -10 \mu\text{A}$
BVCBO	Volts	15	18	40	$I = -10 \mu\text{A}$
BVCEO	Volts	6.5	8.2	12	$I = -10 \mu\text{A}$
Maximum Allowed $V_{CE}$ <sup>1</sup>	Volts	-	-	-3.6V	-
$V_{BE}$ Matching <sup>2</sup>	mV	-0.94	0	+0.94	$V_{CB} = 0\text{V}, I_E = -10 \mu\text{A}$ , adjacent vpnpss
Beta Matching <sup>2</sup>	%	-8.1	0	+8.1	$V_{CB} = 0\text{V}, I_E = -10 \mu\text{A}$ , adjacent vpnpss

**Note:**

1. The maximum allowed  $V_{CE}$  to ensure device reliability is set as per [VPNP Bipolar Reliability](#) on page 382. BVCEO is not the limiting factor for reliable device operation.
2. Optimal matching is obtained by having symmetrical layout using the following layout techniques:
  - a. Locating devices as close to each other as possible.
  - b. Same device size and orientation.
  - c. Similar wiring, particularly for VPNP emitters.
  - d. Similar nearest neighbor topology including wiring.

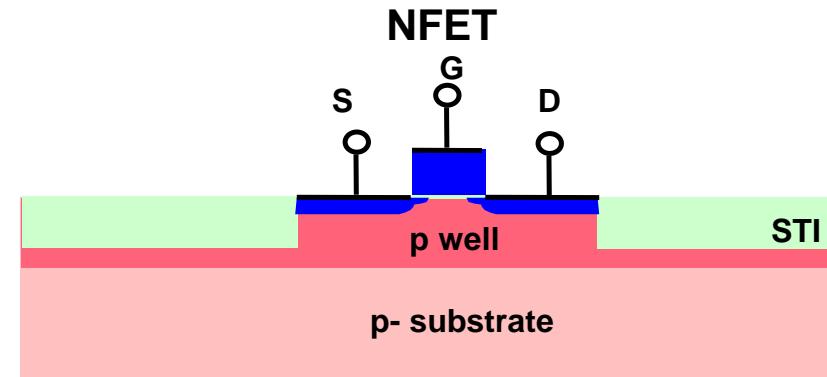
# VPNP Model

- **VBIC Model**
  - VBIC core model for the Vertical PNP
- **Features Supported**
  - Parasitic NPN and isolation diode to substrate
  - Weak avalanche multiplication (impact ionization)
  - Self-heating approximation ( $dVbe/dT$ )
  - Fixed oxide capacitances for the emitter-base and collector-base junctions
  - Quasi-saturation modeling
  - Improved Early effect modeling (as compared to the standard Gummel-Poon model)
- **Option to turn-off the impact ionization effect**
  - Default is ON (gii = 2 global switch for npns and vpnpssx)
  - Model optimized using this feature. If the switch (ii) is not enabled, the output characteristics of the model will not represent hardware measurements as accurately.
  - Turning OFF the switch may help improve simulation time by allowing the designer to de-activate this option for non-critical devices.
- **Model valid for device set layout geometries – See Model Ref Guide Section 6.0 for more details**

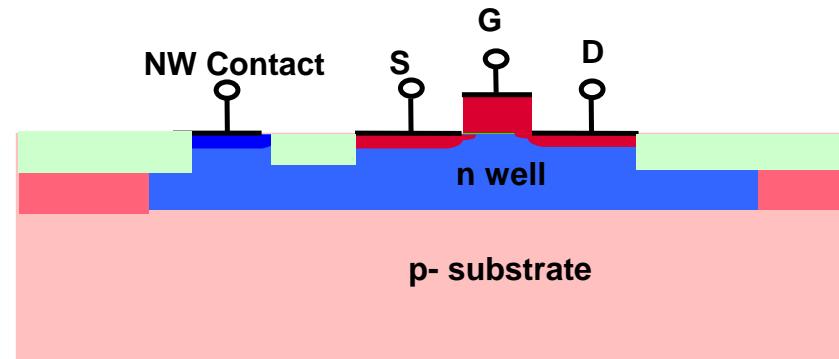


# Regular FETs (nfet/pfet, dgnfet/dgpfet, nfet33/pfet33)

Parameter	Regular FETs* nfet / pfet	Regular I/O FETs Dgnfet / dgpfet, nfet33 / pfet33
Vdd** (V)	1.2V (1.5V)	2.5 / 3.3
Max Supply Voltage** (V)	1.6	2.7 / 3.6
Tox (nm)	2.2	5.2
L <sub>des,min</sub> ( $\mu\text{m}$ )	0.12	0.24 / 0.40
L <sub>eff</sub> *** ( $\mu\text{m}$ )	0.092	0.220/0.220, 0.335 / 0.290
V <sub>tsat</sub> (mV)	355 / -315 (335 / -285)	410/-440, 350 / -300
I <sub>on</sub> ( $\mu\text{A}/\mu\text{m}$ )	525 / -190 (760 / -315 )	660/-260, 790 / -350
I <sub>off</sub> ( $\text{pA}/\mu\text{m}$ )	350 / -300 (500 / -420)	150/-20, 30 / -5



**NFET**



**PFET with Nwell Contact**

P-cell can create layout with or without N-well contact

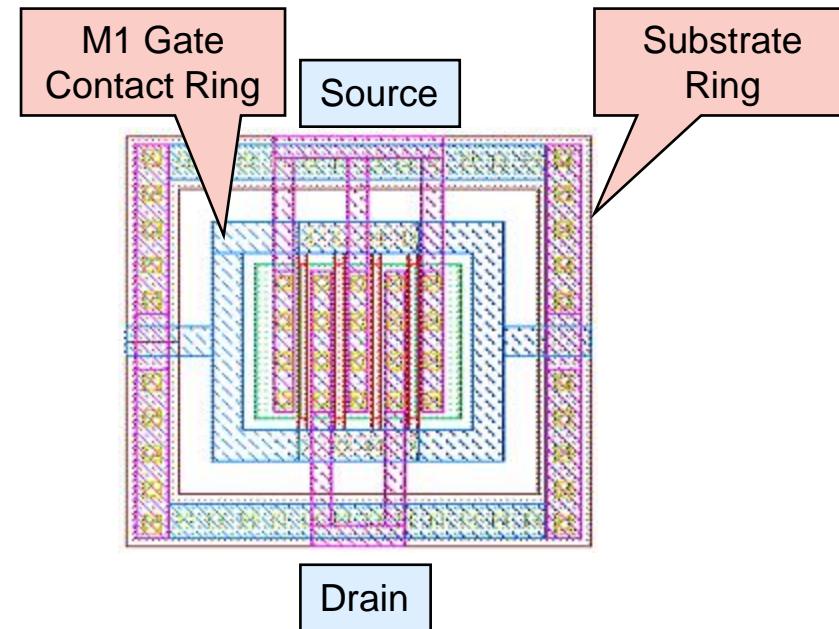
\*Regular FETs are characterized both at 1.2V and 1.5V. 1.5V data shown in the parenthesis in Blue.

\*\*Maximum Voltage across any two terminals between Source, Drain, Gate or Body. \*\*\* $L_{eff} = L_{des,min} - \Delta L$   
TTM-000008 Rev6

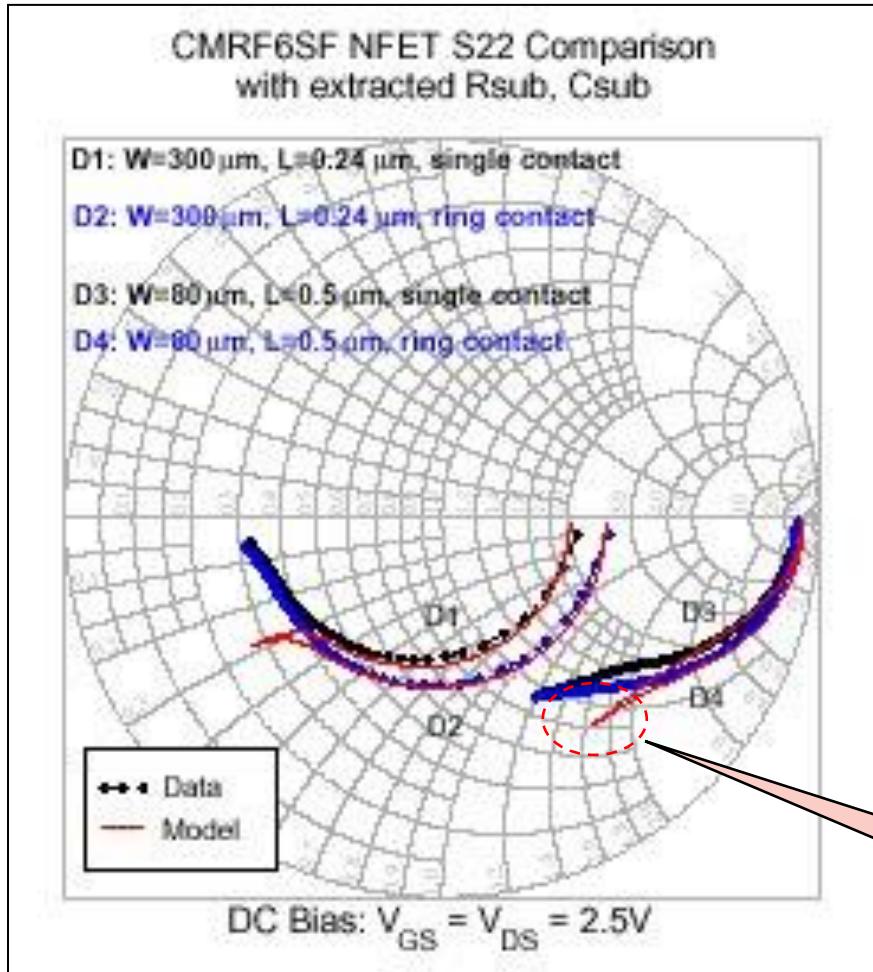
# RF FET Pcells

- Controlled Geometry
- Designated by suffix “\_rf”
- Available for most of the FETs
  - nfet\_rf, nfettw\_rf, dgnfet\_rf, dgnfettw\_rf, nfet33\_rf, nfet33tw\_rf
  - pfet\_rf, dgpfet\_rf, pfet33\_rf

Feature	nfet	nfet_rf
Scalable W, L, nf	Yes	Yes
Flexible wiring	Yes	No
Defined substrate contact	No	Yes
Fixed gate wiring scheme	No	Yes
High accuracy RF model	No	Yes



# S-Parameter Comparison – Substrate Ring



6RF Example Illustrated

- **S22 Comparison**
  - Identical W/L
  - D1 has single substrate contact
  - D2 has substrate contact ring
- **The results show**
  - Large variation in S22 due to substrate contact
  - Accurate model if R<sub>sub</sub> is known
- **Key Points**
  - R<sub>sub</sub> is determined by layout
  - The layout must be fixed for the model to predict S22

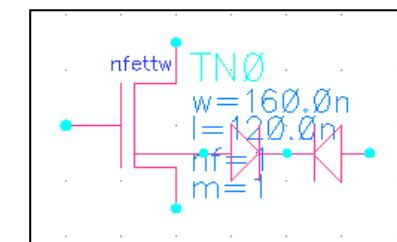
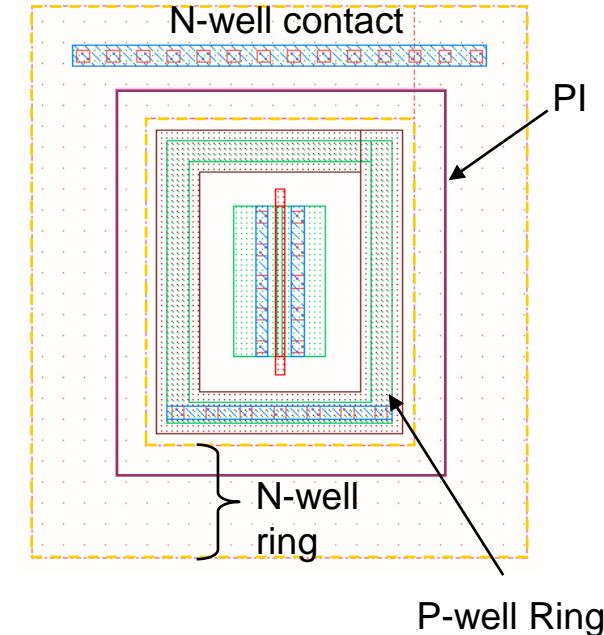
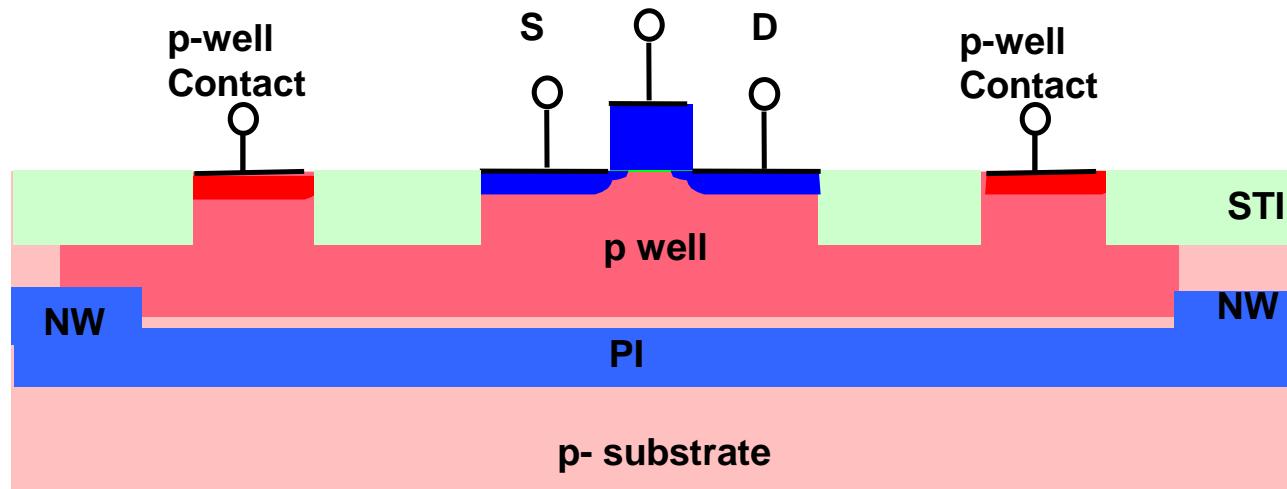
40GHz, past useful frequency range

# PI Triple Well Isolation NFETs (nfettw, dgnfettw)

- Optional devices (additional PI mask)
- Noise/voltage isolation from p- substrate
- Same electrical characteristics as regular NFETs
- Multiple NFETs allowed in a single well
  - Can NOT extend PI under PFET

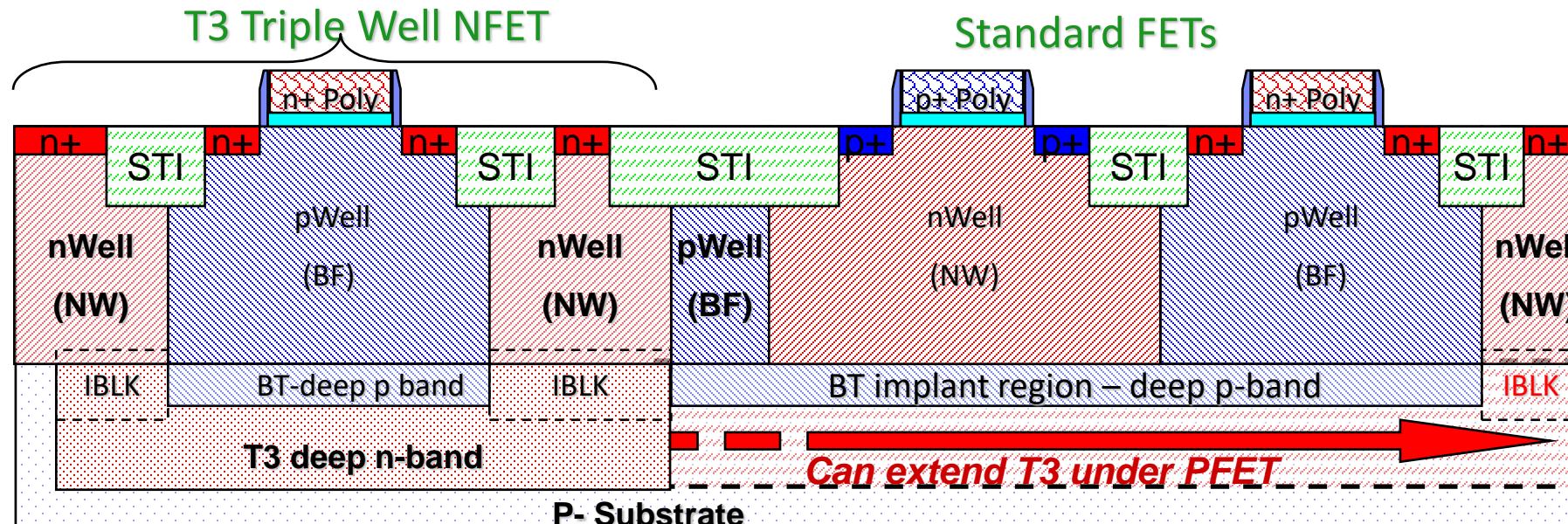
## CDF Options:

p-well and n-well rings (Y/N)  
Place p-well contacts (top, bottom, left, right)  
Place n-well contacts (top, bottom, left, right)  
p-well contact fill %, n-well contact fill %



LVS extracts 6-terminal device

# T3 Triple Well Isolation



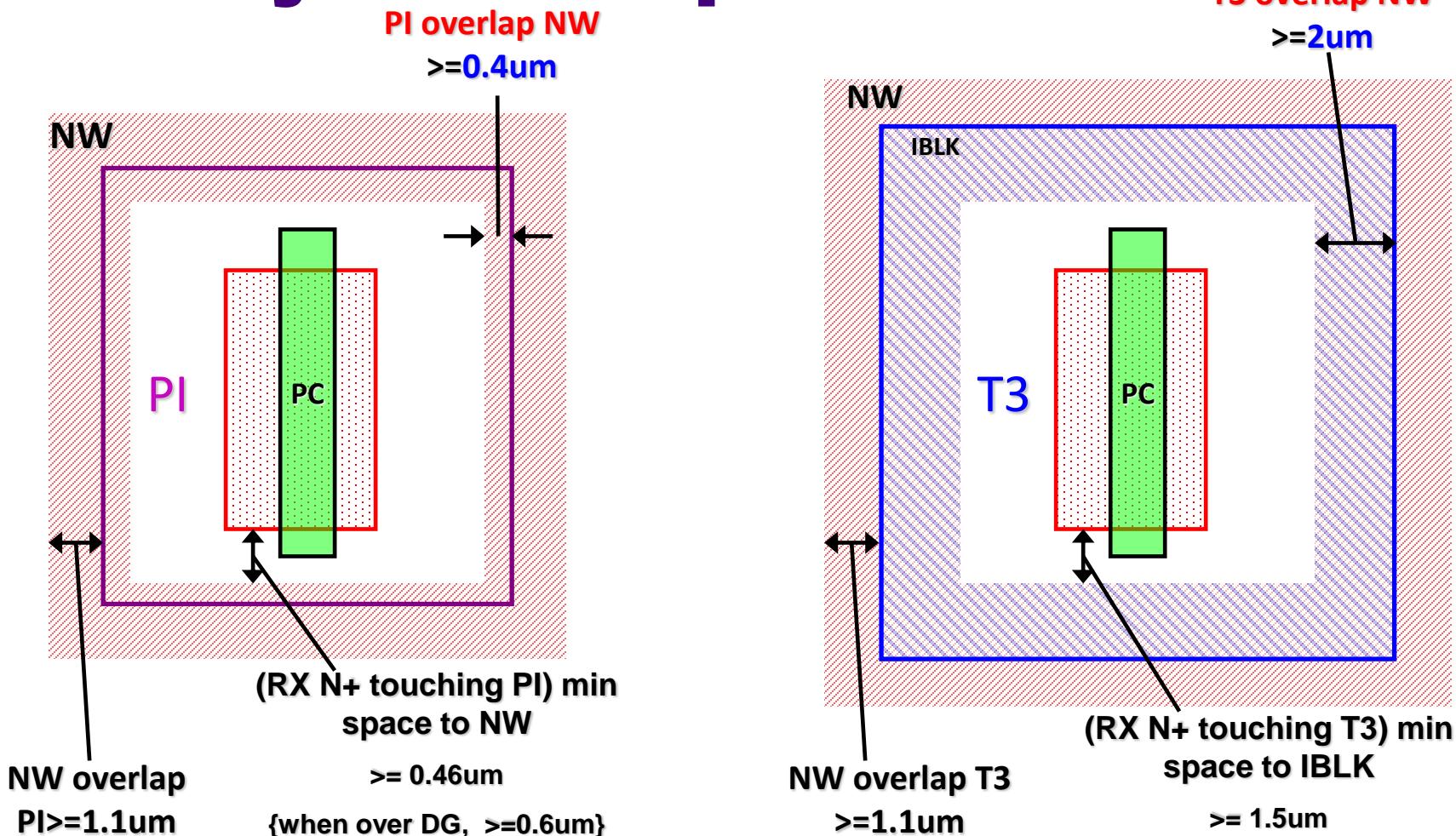
- **T3 isolation mask/process utilizes single deep n-band implant (T3)**

- Increase depth of deep n-band to minimize/eliminate impact on NFET or PFET
  - Maintains an identical pwell (BF mask process) for both isolated and non isolated NFETS
  - Utilize standard NWell to contact down to T3 with IBLK design layer
    - Enabled new design layer “IBLK” to manipulate dataprep to block/remove BT deep p-band to enable NW contact to deep n-band
    - NW regions without IBLK are isolated from deep n-band by BT’s deep p-type region

- **Designer can place both NFETs and PFETs within T3 isolation**

- Enables minimum spaced CMOS digital logic with Triple well to reduce noise.
  - Similar to BULK, N-Well can be biased at different potentials within T3.

# PI & T3 Layout Comparison



- Both PI and T3 are allowed in the same design, however, it is recommended to use either T3 or PI.
- T3 is preferred for performance (allows for nwells isolated from substrate)
- PDK → Misc → Create Guardring for either PI or T3 terminating rings

Typically not an increase/impact if have annular isoPWell contact

Perimeter increase for individual devices is +1.6um

# FET pcell Options (pfet shown)

Physical configuration

Adjusts gate resistance for contact on one or both ends. Sets ngcon parameter in simulation.

Amount of contacts and wire

Add Nwell Contact for pfet

ACLV, ACWV, STI stress and NW Proximity Effects switches for simulations

Add 'VTSENS' shape for DRC checking (gate to well edge distance) for Vt variation due to implant scattering from well edge

Adjusts substrate (body contact) resistance

Device Temperature Rise from Ambient (deg C)

Width Single Finger	160.0n M
Width All Fingers	160.0n M
Length	120.0n M
Number of fingers	1
Multiplicity	1
Interdigitized Layout?	<input type="checkbox"/>
Gate Connection	1 <input type="button" value="▼"/>
Left RX Contact Fill (%)	100
Right RX Contact Fill (%)	100
Add NW contact?	<input checked="" type="checkbox"/> pfet only
Nested / Isolated	Random <input type="button" value="▼"/>
Orientation	Random <input type="button" value="▼"/>
L Matching Proximity	Random <input type="button" value="▼"/>
W Matching Proximity	Random <input type="button" value="▼"/>
switch for STI stress	stress effect <input type="button" value="▼"/>
switch for NW proximity	no proximity effect <input type="button" value="▼"/>
edge sensitivitiy (VTSENS)	<input type="checkbox"/>
Sub Res Multiplier	1
Temperature Delta	0

# FET Models

- PSP core with sub-circuit wrapper
- MOSFET subcircuit features

- Accurate Intrinsic Gate Resistance

- Consists of both the NQS (Non-Quasi Static) channel resistance and the distributed resistance of gates contacted from one or both ends using the instance parameter "ngcon"

- Accurate modeling of the User-defined, layout dependent substrate resistance

- User-defined substrate resistance multiplier ( $rf\_rsub = 1$ ) based on layout (default = 50 ohms) that is used as part of the intrinsic substrate resistance network

- Noise model includes Thermal and 1/f Flicker Noise

- Use of the PSP thermal and 1/f noise equations

- Modeling of impact ionization

- Includes Gate-Drain and Gate-Source Overlap and intrinsic capacitances based on  $capmod = 2$

- Includes Device mis-match as a function of threshold voltage and mobility mis-match

- Components of FET mismatch : Dopant and Geometric (Across Chip Variation)

- Well proximity effect modeled based on PANW1, PANW2, ... , PANW10 instance parameters

- Includes Shallow Trench Isolation (STI) stress effect based on SA, SB and SD instance parameters

- AS/AD/PS/PD must be calculated and netlisted (typically handled by extraction tool)

- Internal estimation of junction area/perimeter not supported

- RF FET Model supports accurate accounting of gate and substrate resistance and junction diode Capacitance

- Junction diode model ( $diodmod = 1$ )
    - RF PCELL models use extrinsic source/drain resistance model ( $rdsmod = 1$ ) to improve the high-frequency S-Parameter and noise performance

# 1/f Flicker and Thermal Noise Model

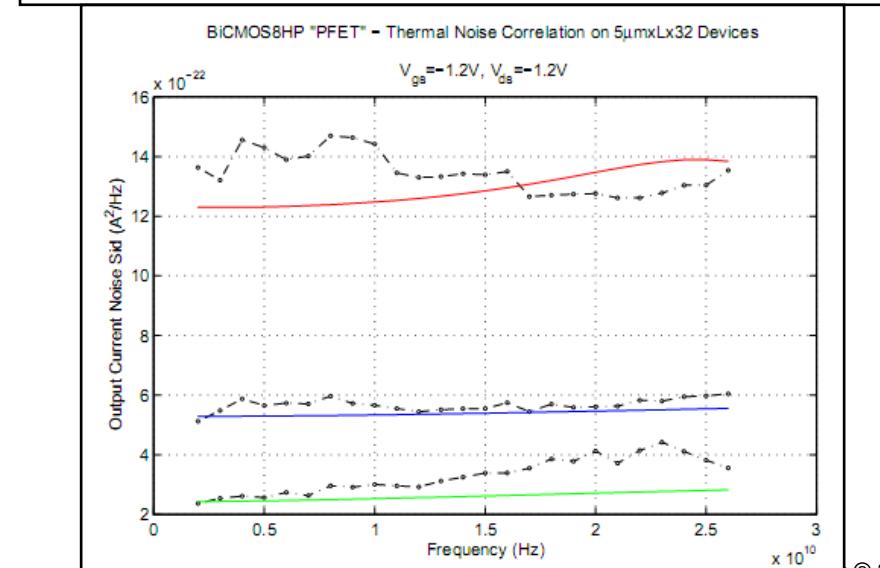
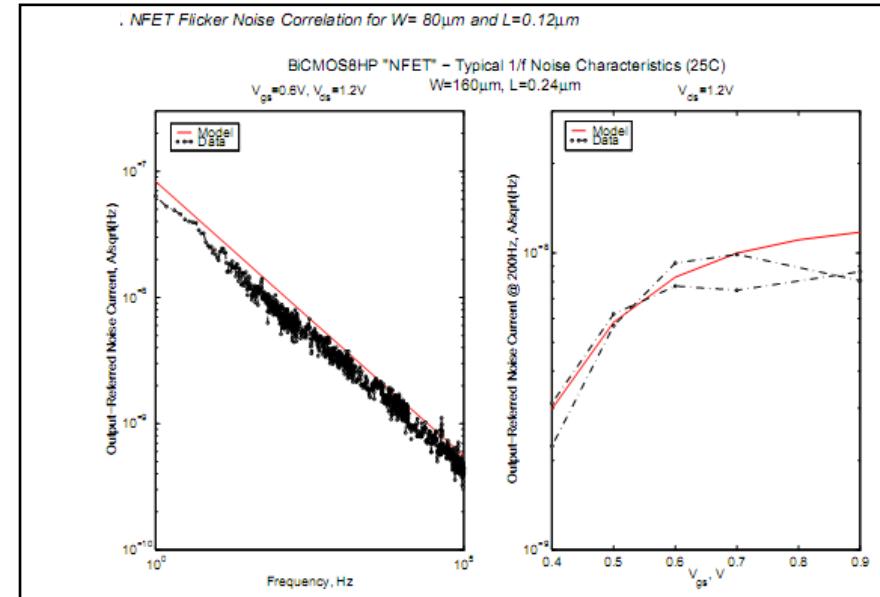
## ▪ PSP Thermal and 1/f (Flicker) Noise models

### ▪ 1/f Flicker Noise Model

- Model predicts low-frequency noise dependence on device area,  $V_{gs}$  and  $V_{ds}$
- Model parameters have been extracted at 25C using a limited sample of device geometry and bias data
- The nominal predictions by the model should be considered as typical not worst case.
- Statistical flicker noise limits based on hardware
- Flicker noise parameters measurements data taken in the frequency range of 1 Hz to 100 kHz

### ▪ Thermal Noise Model

- Model also includes various other noise sources, such as, channel thermal noise, source/drain resistance noise, induced-gate noise, shot noise induced by the source/body and drain/body junctions. These noise sources affect the device's noise performance at high frequencies.



# FET Source and Drain Parasitic

Default values for the Source/Drain (S/D) diffusion geometry parameters AD, PD, AS, PS, NRS and NRD are zero.

With these default values, S/D area and STI bounded perimeter capacitances will not be added to the circuit during simulation.

Gate bounded perimeter component of capacitance is always present, regardless of the value of the geometry parameters.

If the models are called from the Cadence environment, these geometry parameters will be passed as estimated or extracted values for the layout in the Cadence library.

Intrinsic models account for devices with multiple fingers using the instance parameter “NF”.

When  $NF > 1$ , the internal model calculations assume any specified width (W) and source drain geometry parameters (AD, PD, NRD, AS, PS, and NRS) represent the total device values, not per finger values.

Below is an example of the netlist call for a 15 finger thin oxide NFET with each finger 2 $\mu$ m wide and a channel length of 0.12 $\mu$ m:

```
xnf vout vg vsn sub nfet l=0.12u w=30u nf=15 as=6.14p ad=6.14p ps=38.14u +pd=38.14u nrs=0.006 nrd=0.006
```

# STI Proximity Effect : Isolation-Induced Stress

- Shallow trench isolation (STI) edges introduce compressive strain in silicon

- Decreases NFET drain current
- Increases PFET drain current
- Function of width, length, proximity of STI edges

Table 54. Isolation Proximity Effect Example

Device (Geometry)	Bias	Model $\Delta I_{dsat}$	Model $\Delta V_{tsat}$
NFET (2μm x 0.12μm x 1)	$V_{GS} = V_{DS} = 1.2V$	- 11.5 %	+ 16 mV
PFET (2μm x 0.12μm x 1)	$V_{GS} = V_{DS} = 1.2V$	+ 12.6 %	- 11 mV
DGNFET (2μm x 0.24μm x 1)	$V_{GS} = V_{DS} = 2.5V$	- 5.8 %	+ 24 mV
DGPFET (2μm x 0.24μm x 1)	$V_{GS} = V_{DS} = 2.5V$	+ 7.8 %	- 6 mV
NFET33 (2μm x 0.40μm x 1)	$V_{GS} = V_{DS} = 3.3V$	- 8.0 %	+ 9 mV
PFET33 (2μm x 0.40μm x 1)	$V_{GS} = V_{DS} = 3.3V$	+ 8.0 %	- 9 mV

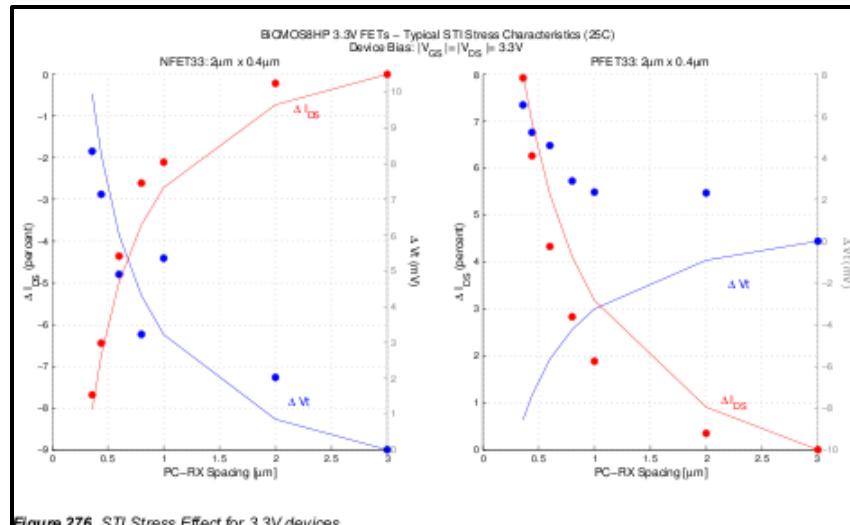


Figure 276. STI Stress Effect for 3.3V devices

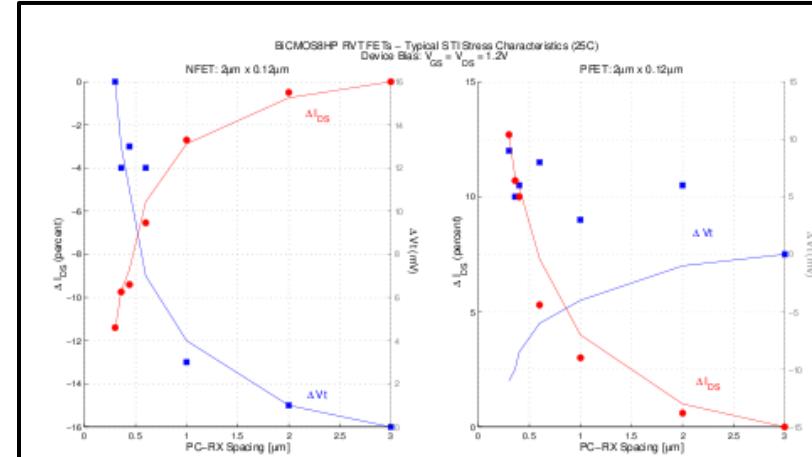


Figure 274. STI Stress Effect for thin oxide devices

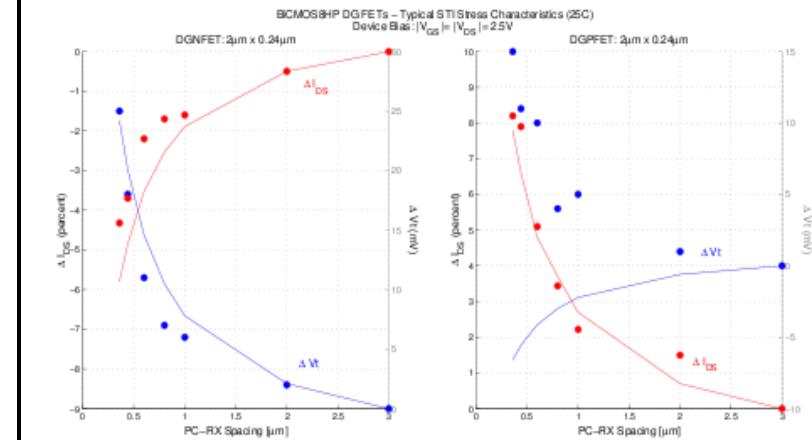
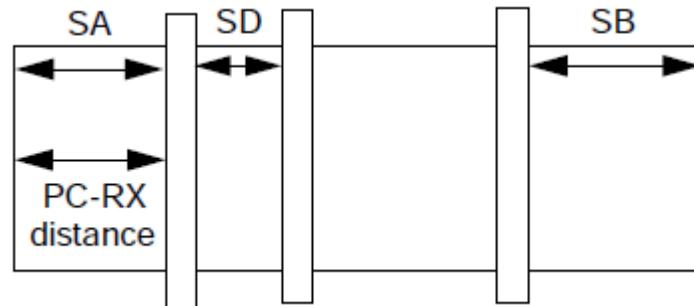


Figure 275. STI Stress Effect for DG devices

# Isolation-Induced Stress Effect –STI Contd..

- Built-in STI stress model is utilized
  - SA, SB, SD replace previous stress model parameters PAM1 and PAM2
  - Models the STI stress effect by adjusting mobility and threshold
  - Supports multi-finger ( $nf > 1$ ) schematic simulation



- Extraction for re-simulation post layout
  - Extract SA/SB for each PC finger individually, no SD
  - SA, SB averaged for non-rectangular layouts
- Global switch “gstis”
  - Default:  $gstis = 2$  (isolation-induced stress effect enabled through non-zero SA/SB/SD)
  - $gstis = 0$  (globally disable isolation-induced stress effect, for analysis purposes)
  - $gstis = 1$  (STI stress effects are enabled on an instance-by-instance basis ( $istis=1$ ))

# Well Proximity Effect

- The root cause for well proximity effect

- High energy well implant -- dopant atom scattering at the photoresist edges changes the effective doping of the adjacent devices
- Increases magnitude of  $V_t$
- NFETs/PFETs closer than ~3um from n-well and triple-well edges are affected

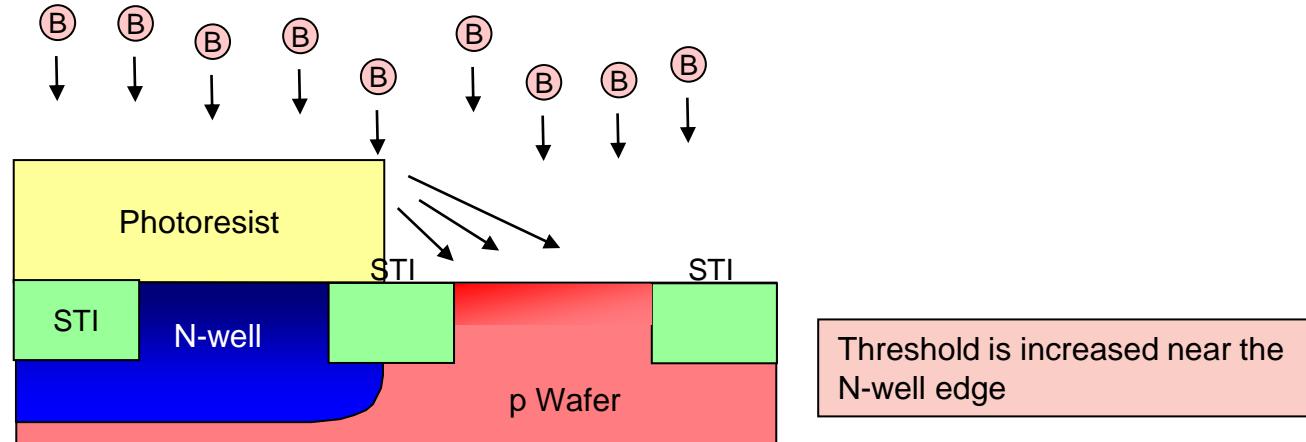
- Option in CDF to add “VTSENS” layer to layout

- DRC will then force gates to be  $\geq 3.0\mu m$  from well edges

- GLOBALFOUNDRIES well proximity effect model calculations dependent on

- Device dimensions, Device type, Device orientation
- Distance of the device gate to the well edge
- Number of proximate well edges

Example: P-well implant  
for the NFET



# Well Proximity Effect

Global switch “gwells” controls well proximity effect

**gwells = 1** If instance parameter lnws=1, the well proximity effect is calculated using the provided instance parameters. (panw1..panw10).

--Useful when instance parameters are available (ie, post-layout extraction)

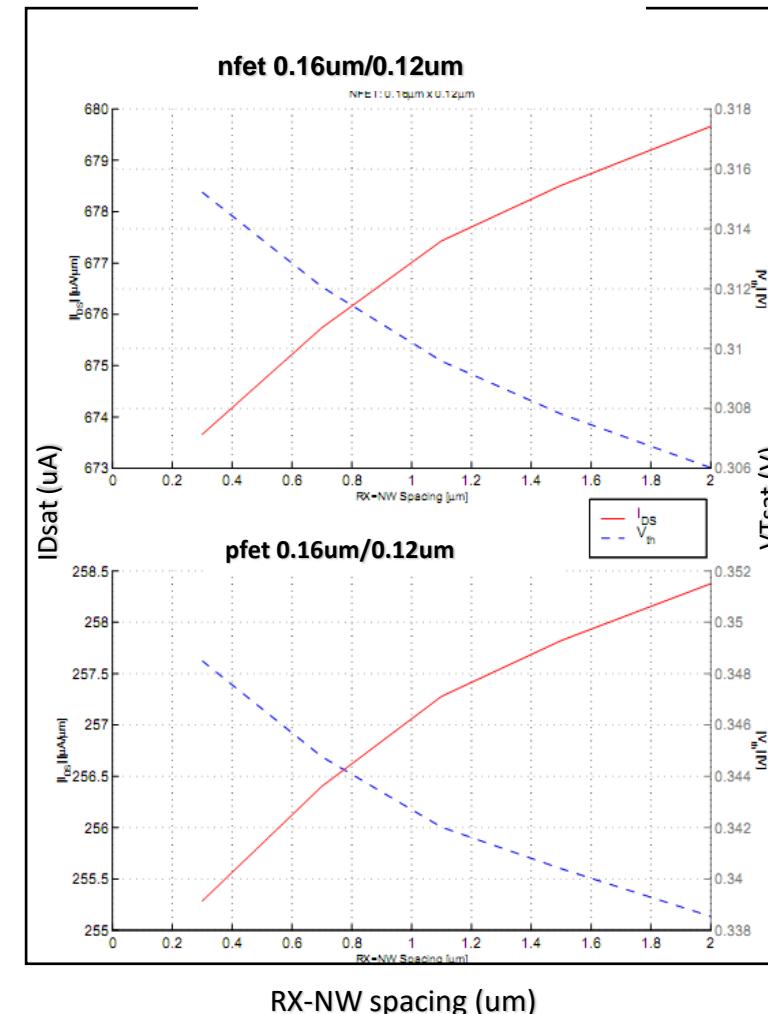
**gwells = 0** Disable the well proximity model, independent of any FET netlist instance parameters.

--Useful for comparison in post-layout simulations

**gwells = 2 (default)** Nwell proximity effect is calculated based on instance parameters provided in each FET netlist.

--Useful in pre-layout analysis to determine sensitivities

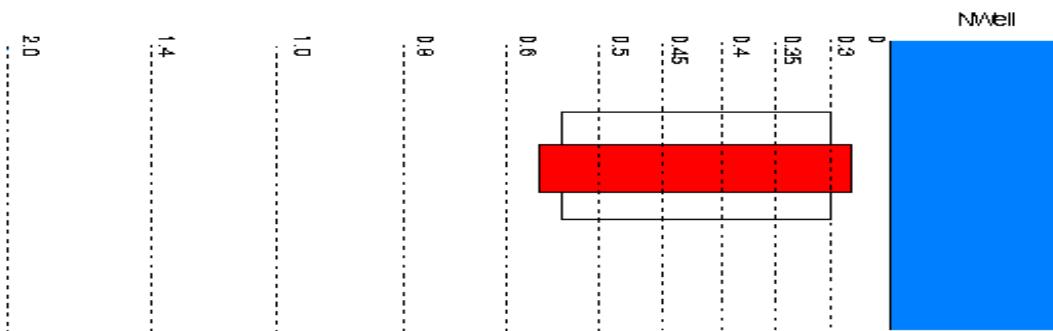
- A method for adjusting the threshold voltage of the device based on the distance to a well edge
- Information about the circuit layout needs to be passed to the model (panw1-10)



# Extracted Layout Information – well proximity

The layout information needs to be passed to the FET models thought the model instance parameters:

- PANW1** – the intersection of PC and RX of the device within **0 to 0.3um** of the nwell edge
- PANW2** – the intersection of PC and RX of the device within **0.3um to 0.35um** of the nwell edge
- PANW3** – the intersection of PC and RX of the device within **0.35um to 0.4um** of the nwell edge
- PANW4** – the intersection of PC and RX of the device within **0.4um to 0.45um** of the nwell edge
- PANW5** – the intersection of PC and RX of the device within **0.45um to 0.5um** of the nwell edge
- PANW6** – the intersection of PC and RX of the device within **0.5um to 0.6um** of the nwell edge
- PANW7** – the intersection of PC and RX of the device within **0.6um to 0.8um** of the nwell edge
- PANW8** – the intersection of PC and RX of the device within **0.8um to 1.0um** of the nwell edge
- PANW9** – the intersection of PC and RX of the device within **1.0um to 1.4um** of the nwell edge
- PANW10** – the intersection of PC and RX of the device within **1.4um to 2.0um** of the nwell edge



# Modeling of Well Proximity Effect

- Vt adjustment comes through body effect parameter k1
- panw# instance parameters based on layout information

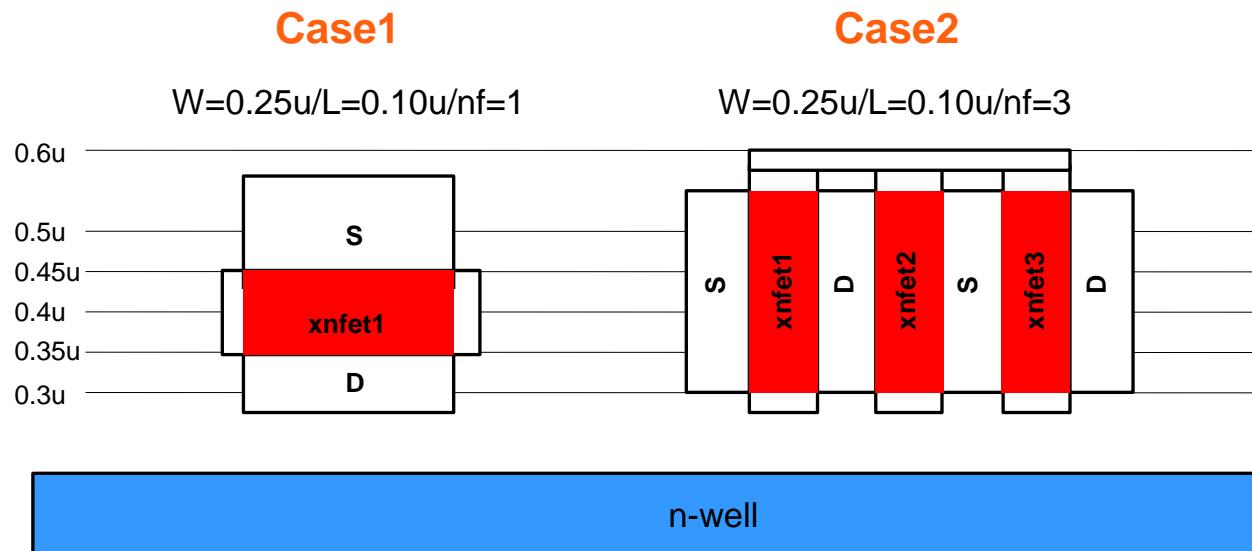
$$k_{1shift} = \left( \frac{A}{l \cdot w} \right) \cdot [panw1/(X1-B) + panw2/(X2-B) + \dots + panw10/(X10-B)]$$

where A and B are fitting parameters

and X1....X10 are midpoint values of each band shown on next page

- Default model parameters “PANW#” set to zero (negligible well proximity)
- Effect is additive for well edges on more than one side of a device
- Model is only an estimation of the effect for a given layout
  - Variation in alignment, on wafer distances, etc not modeled
  - Follow good design practices for sensitive devices
  - Spacing to nwell, identical orientation with respect to well edge
- Well proximity and nf > 1 will not yield the correct results
  - Orientation with respect to well edge unknown for schematic simulation
  - FETs are extracted from layout as individual fingers, nf=1

# Well Proximity Effect: Testcases



**Case1 ➔ xnfet1 vd vg vs vx nfet L=0.10u W=0.25u nf=1**

+ PANW1=0 PANW2=0 PANW3=0.0125p PANW4=0.0125p PANW5=0 PANW6=0

**Case2 ➔ xnfet1 vd vg vs vx nfet L=0.10u W=0.25u nf=1**

+ PANW1=0 PANW2=0.005p PANW3=0.005p PANW4=0.005p PANW5=0.005p PANW6=0.005p

**xnfet2 vd vg vs vx nfet L=0.10u W=0.25u nf=1**

+ PANW1=0 PANW2=0.005p PANW3=0.005p PANW4=0.005p PANW5=0.005p PANW6=0.005p

**xnfet3 vd vg vs vx nfet L=0.10u W=0.25u nf=1**

+ PANW1=0 PANW2=0.005p PANW3=0.005p PANW4=0.005p PANW5=0.005p PANW6=0.005p

# ACV Global Switches and Instance Parameters

Global Switch	Effect and Related Instance Parameters
<code>mc_global</code>	Sets combination of global and matching parameters that will vary randomly in Monte Carlo
<code>fet_dop_mis</code>	Global control for dopant mismatch
<code>fet_geo_mis</code>	Global control for geometric mismatch (ACLV)
<code>pc_nest</code>	Global control for the systematic ACLV component -- Through Pitch
	Instance Parameter <code>plnest</code> : instance is nested, or isolated, or random
<code>pc_orient</code>	Global control for the systematic ACLV component – Orientation
	Instance Parameter <code>plorient</code> : instance is vertical, or horizontal, or random
<code>pc_dist</code>	Global control for the systematic ACLV component -- Distance
	Instance Parameter <code>pld200</code> : instance is within 200um, or not, or random
<code>rx_dist</code>	Global control for the systematic ACWV component -- Distance
	Instance Parameter <code>pwd100</code> : instance is within 100um, or not, or random

`plnest`, `plorient`, `pld200`, and `pwd100` instance parameters are available through the FET CDF

# Voltage Limits: Thin Oxide FETs

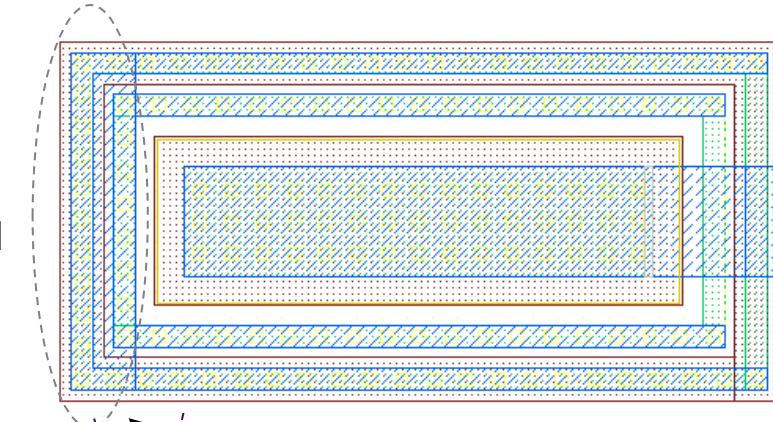
- Device Group: 1.5V Thin Oxide (2.2 nm) FETs
- Device Names: nfet, pfet
- Nominal Operating Voltage: 1.5V (Section 5.1 Design Manual)
- Maximum Vdd : 1.6V (Section 5.1 Design Manual)
- Vmax and Vos (Overshoot Voltage) Equations for gate oxide area, temperature and power on hours for 2.2 nm Gate Dielectrics in Section 4.26.7 Design Manual

# Voltage Limits : Thick Oxide FETs

- Device Group: 2.5V/3.3V Thick Oxide (5.2) FETs
- Device Names: dgnfet, dgpfet; nfet33, pfet33
- Nominal Operating Voltage: 2.5V/3.3V (dgnfet, dgpfet; nfet33, pfet33) - Section 5.1 Design Manual
- Maximum Vdd: 2.7V/3.6V (dgnfet, dgpfet; nfet33, pfet33) - Section 5.1 Design Manual
- Vmax and Vos (Overshoot Voltage) Equations for gate oxide area, temperature and power on hours for 5.2 nm Gate Dielectrics in Design Manual Section 4.26.8

# Forward-bias Diode (divpnp)

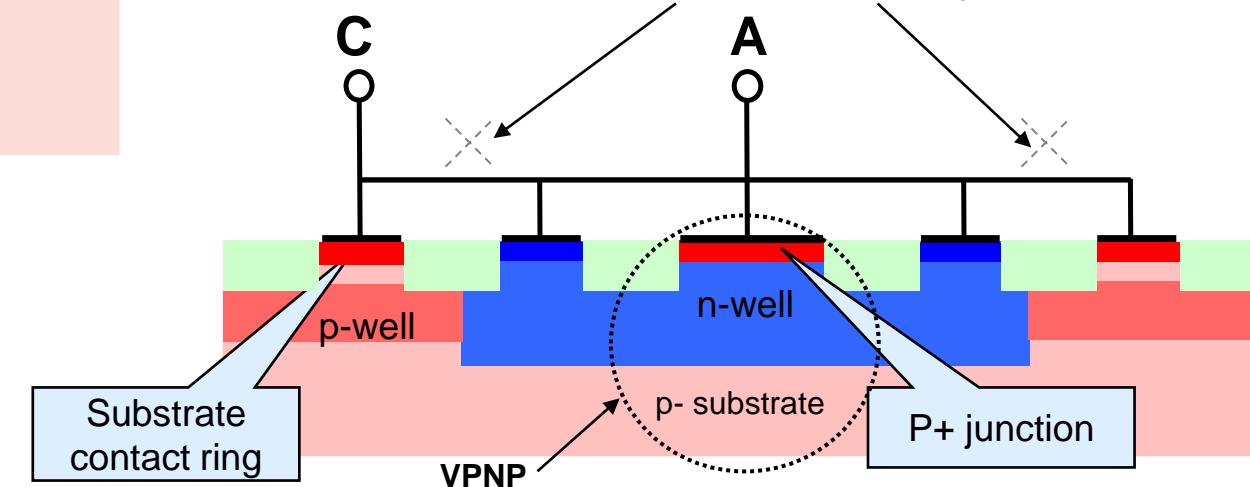
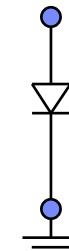
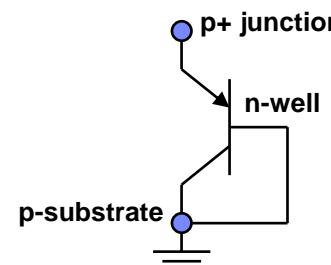
- **P+ in n-well junction**
  - 3 terminal Pcells and models provided
- **Approved only for bandgap reference circuits**
  - Other applications require GLOBALFOUNDRIES approval
- **500 pA/ $\mu\text{m}^2$  to 1 $\mu\text{A}/\mu\text{m}^2$  for accurate model prediction**
- **SX ring should wire to cathode (NW)**
  - Parasitic pnp injects holes into substrate
  - Accidental forward biasing of the NW/SX junction



**divpnp** has three terminals (bjt model) that has separate N-well and substrate ring nodes.

## CDF Options:

Anode width, length,  
Number of anodes



# Forward Bias Diode (divpnp) CDF

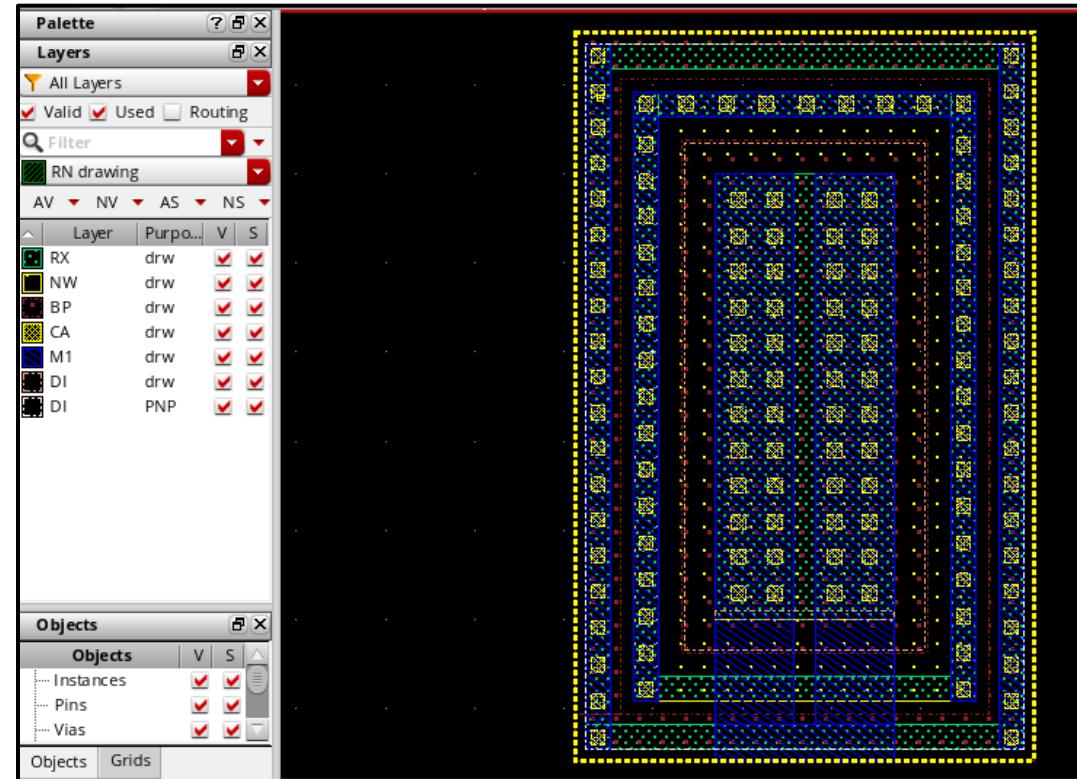
Emitter Length	5u M
Emitter Width	2u M
Number of emitters	1
Multiplicity	1

## CDF Options

Emitter/Anode Length

Emitter/Anode Width

Number of Emitters/Anodes



The forward-bias diode model (divpnp) focuses on the forward bias I-V curves including temperature effects. This is a three node model, and employs the standard Gummel-Poon BJT transistor. The nodes are the emitter (anode), the base (NW), and the collector (SX). Features of this model include:

- Input parameter specification for width, length, and number of fingers.
- Device temperature difference with respect to circuit temperature (dtemp).
- Series resistance based on device geometry is included to describe I-V curve roll-off.
- Device mis-match for adjacent devices.

# PIN (P-Intrinsic-N) Diode (pin)

- Scalable P+/N junction device similar to the extrinsic base-collector junction of the NPN HBT
- DT-isolated
- Ring-shaped N+ reach-through used to provide low-impedance cathode contact
- Low series resistance coupled with relatively low off-capacitance create a device suitable for use as an integrated PiN diode
- Scalable in length, width, and number of parallel anodes

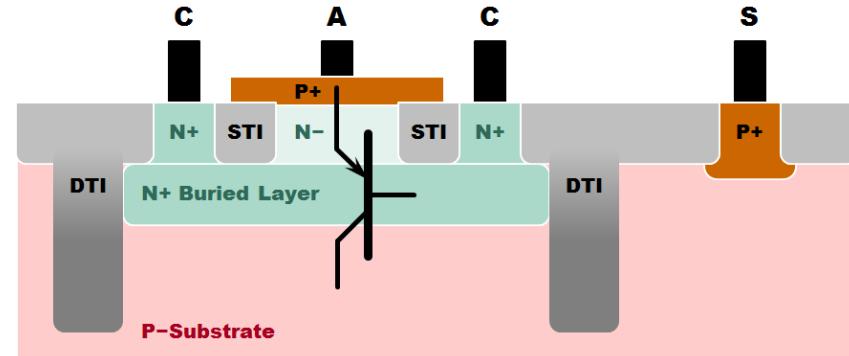
Table 4-33. Electrical Parameters for PIN Diode

Parameter	Units	Minimum	Nominal	Maximum	Conditions
$V_{FWD}$	Volts	0.734	0.749	0.764	$I = 10 \mu A, 5 \mu m \times 5 \mu m$
$V_{BREAKDOWN}$	Volts	5.20	6.20	7.20	$I = 10 \mu A, 5 \mu m \times 5 \mu m$
$C_{J,AREA}$	fF/ $\mu m^2$	1.25	1.79	2.33	$V_{AC} = 0 V$

The minimum allowable width and length dimensions are given in Table 4-34.

Table 4-34. Supported Layout Dimensions for PIN

Anode Dimensions	Width (Min)	Length (Min)
minimum PIN anode	1.0	1.0



Cross section of typical PiN diode, showing physical NPN formation

## Model Features

- Physical 3-terminal topology
- Forward-bias diffusion capacitance (on-capacitance)
- Forward-bias current, including leakage
- Substrate injection due to parasitic PNP
- Depletion & parasitic capacitances
- Series resistance in cathode and substrate
- High-frequency substrate coupling network
- Shot and thermal noise
- Process statistics

# pin CDF

Anode width	2u M
Anode length	8u M
Number of anode fingers	1
<input type="checkbox"/> Connect Anode Terminals?	
Cathode width	620.00n M
<input checked="" type="checkbox"/> Use recommended ground rules?	
Multiplicity	1

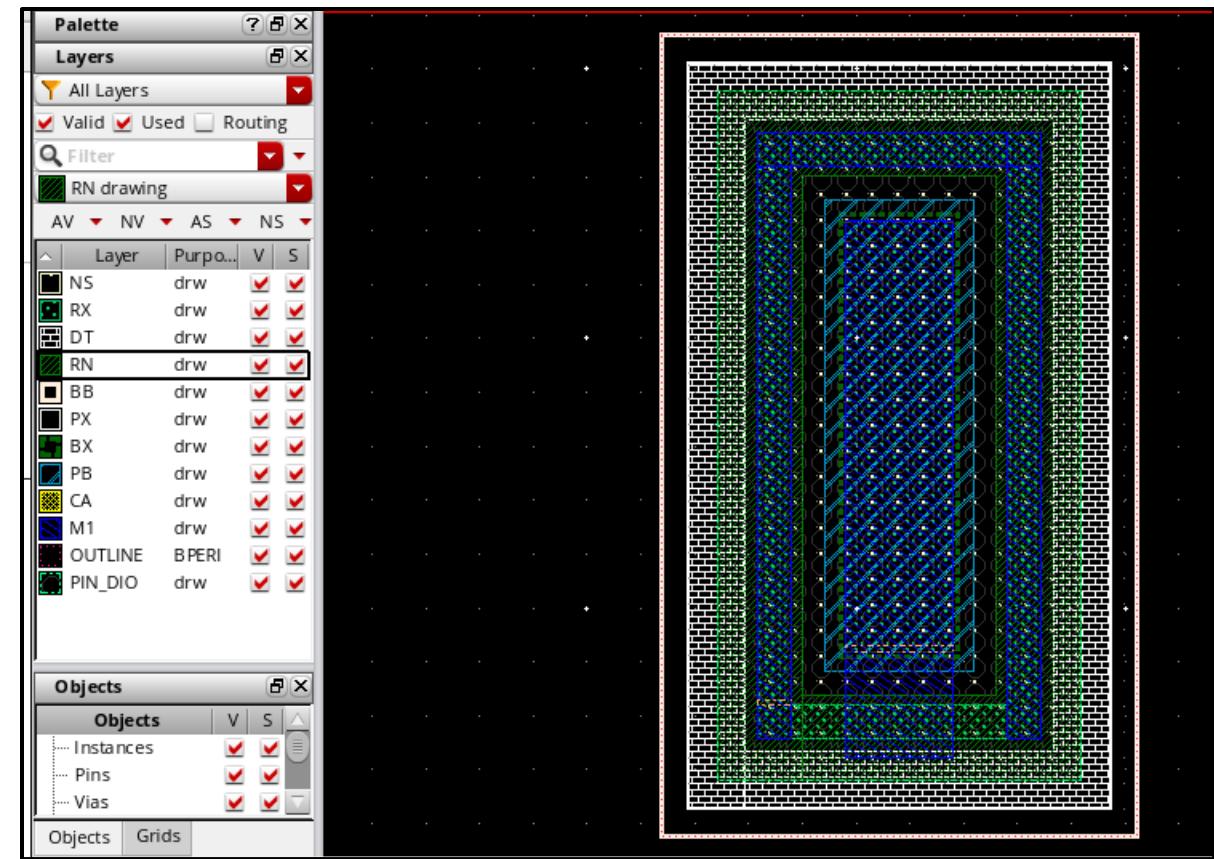
## CDF Options

Length

Width

Number of Fingers

Cathode Width



# Schottky Barrier Diode (sbd)

- Vertical SBD
- p-guardrings reduce leakage
- Silicide forms Schottky on lightly doped n- above NS
- 0.26V diode turn-on voltage
- Cathode (NS), reach-thru (RN) and silicide formation steps are shared with the HBT
- Integrated into the process flow without the addition of any extra mask

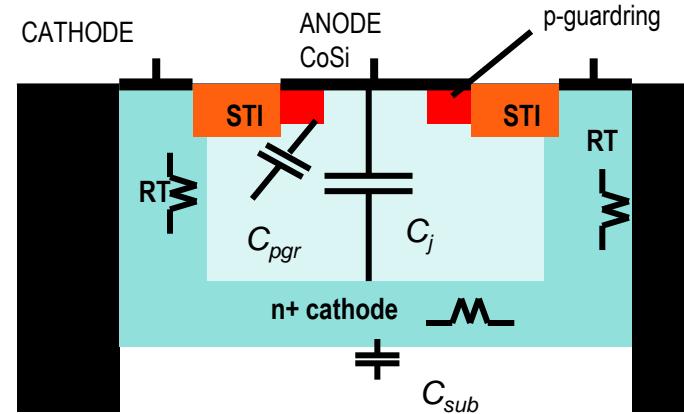
Table 4-31. Electrical Parameters for SBD Diode

Parameter	Units	Minimum	Nominal	Maximum	Conditions
$V_{FWD}$	Volts	0.195	0.260	0.325	$I = 10 \mu A, 5 \mu m \times 5 \mu m$
$V_{REVERSE}$	Volts	2.00	4.00	6.00	$I = 1 mA, 5 \mu m \times 5 \mu m$
$C_{J, AREA}$	fF/ $\mu m^2$	3.12	4.80	6.48	$V_{AC} = 0 V$

The minimum allowable width and length dimensions are given in Table 4-32.

Table 4-32. Supported Layout Dimensions for SBD

Anode Dimensions	Width (Min)	Length (Min)
minimum SBD anode	0.8	1.0



STI = Shallow Trench isolation  
pgr = p-guardring  
RN = Reach-Thru

The SBD model is a fully-scalable, process-based 3-terminal element. It is scalable over anode width, length and number of anode fingers.

The model captures the following physical behaviors:

- Reverse-bias depletion and parasitic fringing capacitances
- Forward-bias diffusion capacitance
- Forward-bias junction current, including low-current leakage
- Series resistance in the cathode
- Temperature dependence and self-heating
- Substrate injection current due to parasitic PNP behavior
- Cathode-substrate depletion capacitance
- Full substrate network scaling (RSU, CSU)
- Shot and thermal noise
- Anode-Cathode reverse leakage and junction breakdown

# sbd CDF

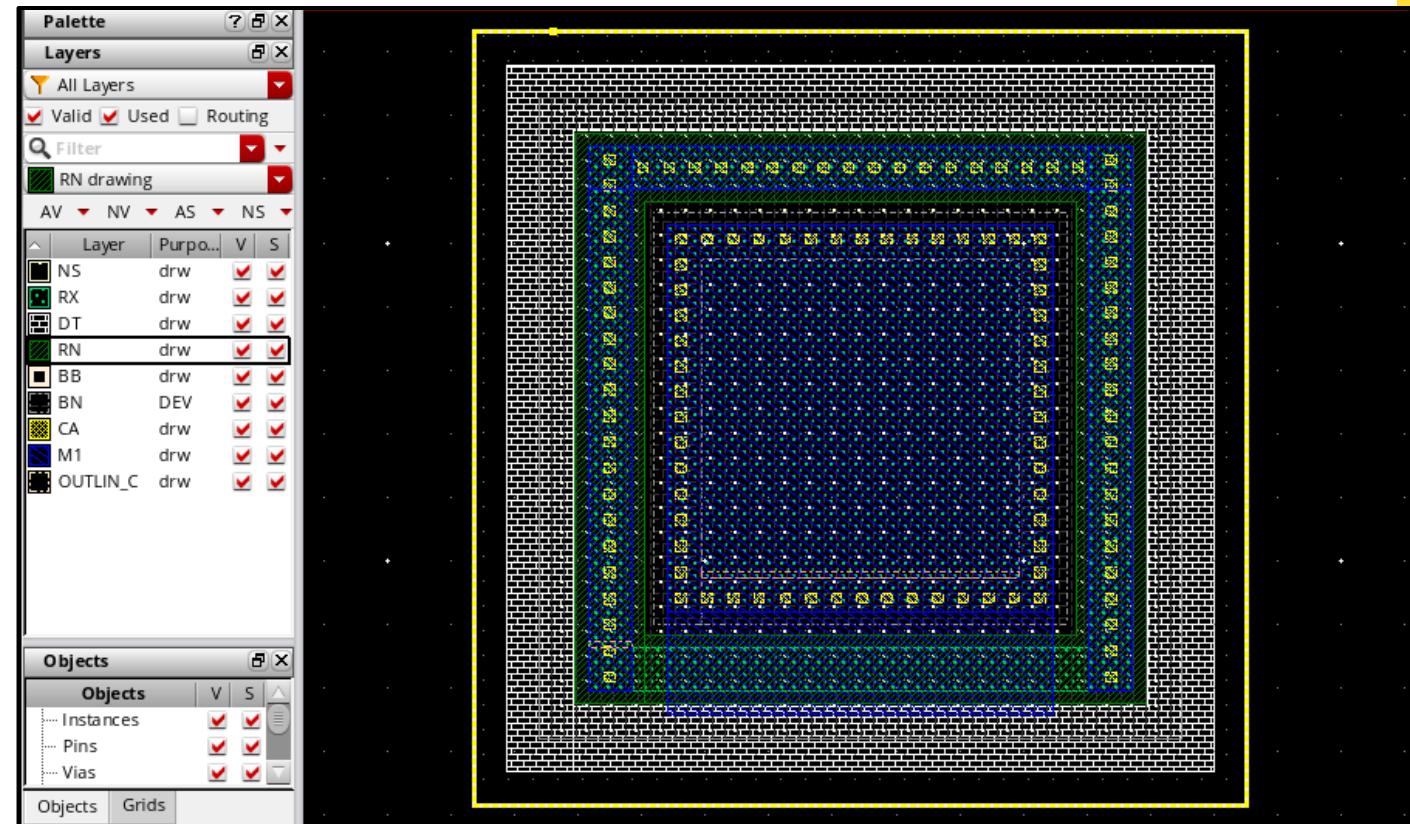
Anode width	5.0u M
Anode length	5.0u M
Number of anode fingers	1
<input type="checkbox"/> Connect anode terminals?	
<input checked="" type="checkbox"/> Use recommended ground rules?	
Multiplicity	1

## CDF Options

Length

Width

Number of Fingers



# Varactors

## ▪MOS Varactors (ncap, dgncap)

- Large tuning range
- May be used as varactors or decoupling capacitors

## ▪HA Junction Varactor (havar)

- Large tuning range and good linearity
- Requires two additional masks (JD,VI)

Device Name	Structure	C <sub>A</sub> : Area Capacitance (fF/ $\mu\text{m}^2$ )	Tuning Voltage Range	Tuning Capacitance Range ***	Typical Q @ 1 GHz ***
ncap*	N+ polysilicon gate over n-well using 2.2 nm gate oxide	11.3 @ 1.2V	- 0.5V to 1.0V	4.8 : 1	78 (0 V)
dgncap	N+ polysilicon gate over n-well using 5.2 nm gate oxide	6.0 @ 1.25V	- 0.5V to 1.0V	2.8 : 1	117 (0 V)
havar**	Implanted junction with an n-type doping spike over implanted subcollector	2.05 @ 0V	-3.6V to 0V	2.7 : 1	216 (0 V)

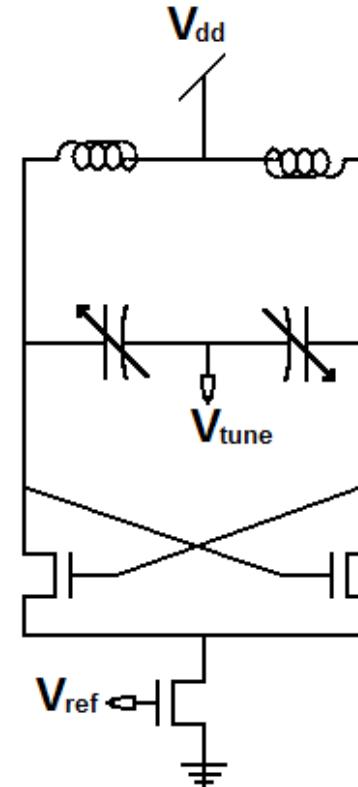
\*diffncap pcell also available for differential circuit applications.

\*\*diffhavar configuration pcell also available.

\*\*\*Q and tuning range dependent on geometry

# Differential Varactors

- **Reduced Chip Area**
  - Reduce Substrate Noise Modulation
- **Inter-digitated fingers for improved Q**
  - Reduce VCO Phase Noise
- **Improved current flow between the devices using same well: no contact between anodes**
  - Improve Symmetry of Circuit
  - Improve Mis-match
- **Decreased Tunability**
  - Due to coupling capacitance
- **Available for *ncap* and *havar***



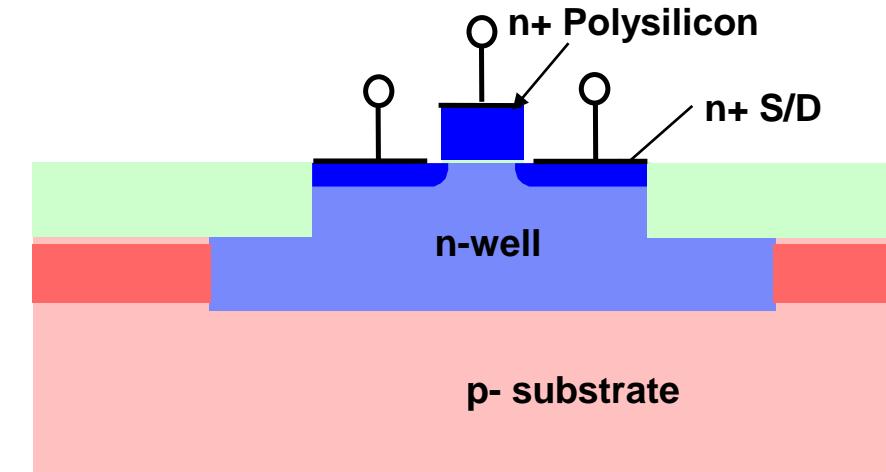
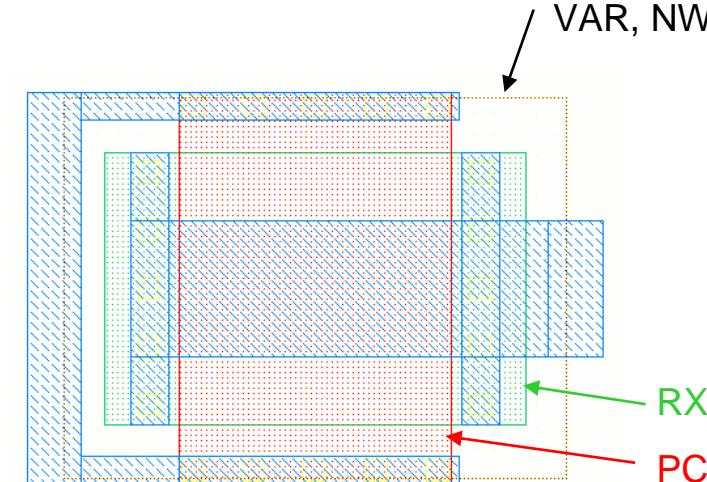
# NMOS Varactors/Decoupling Capacitors (ncap, dgncap)

- N-channel FET in n-well
- Additional **DG** mask required for dgncap
- Used as *varactor* or *decoupling cap*
- VAR device recognition design layer
- Blocks halo/extension implants for improved Q
- Scalable gate width and length
- $C_A = 10.8 / 5.7 \text{ fF} / \mu\text{m}^2$  (ncap / dgncap)
- $V_{g-d, \text{max}} = 1.6 / 3.63\text{V}$  (ncap / dgncap)
- PC area  $\leq 230 \mu\text{m}^2$  per gate\*
- Tie-down required for n-well

## CDF Options:

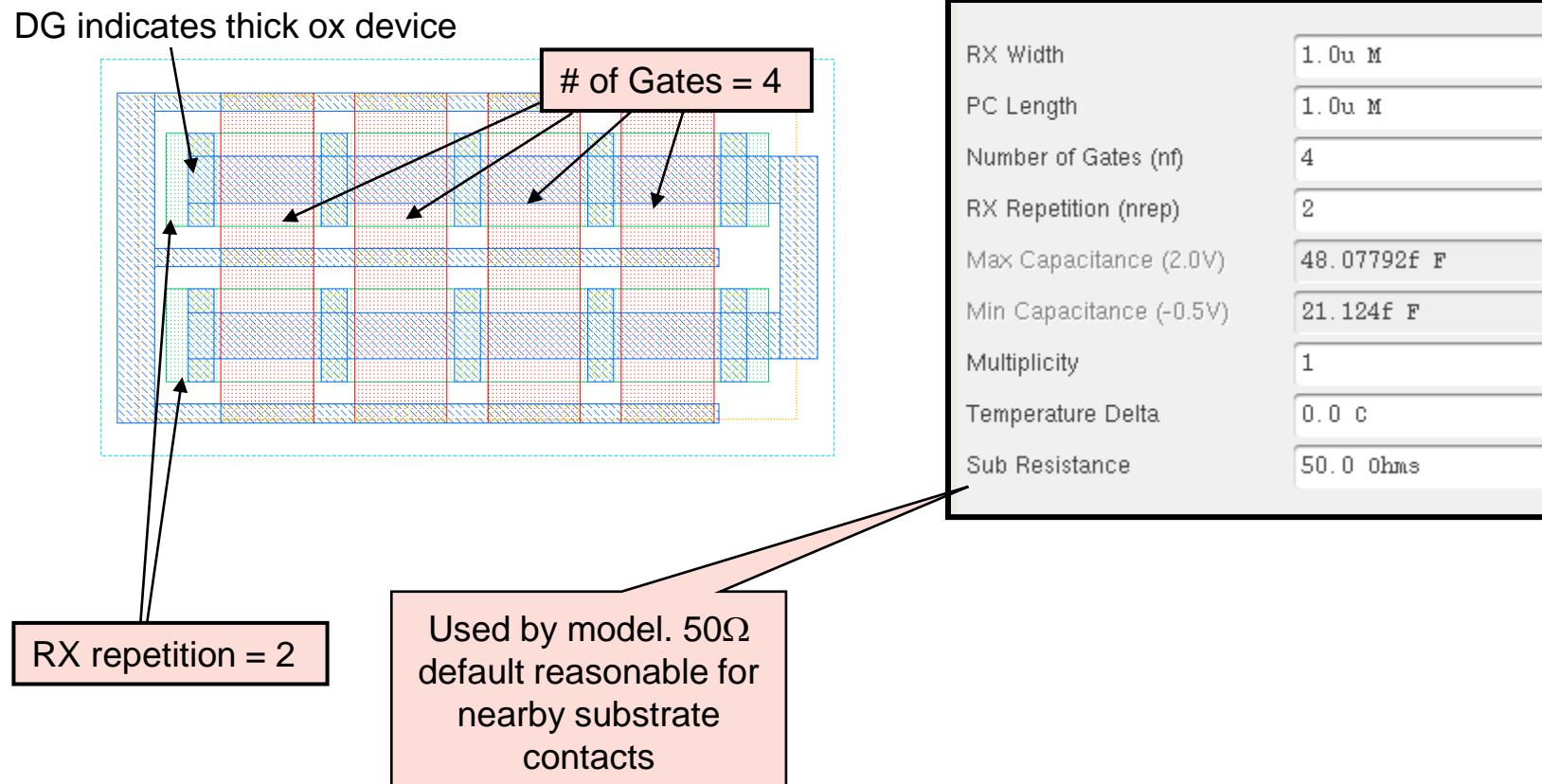
Gate length  
Gate width (RX dimension)  
Number of gates (x)  
RX repetition (y)

\*Recommended 45  $\mu\text{m}^2$



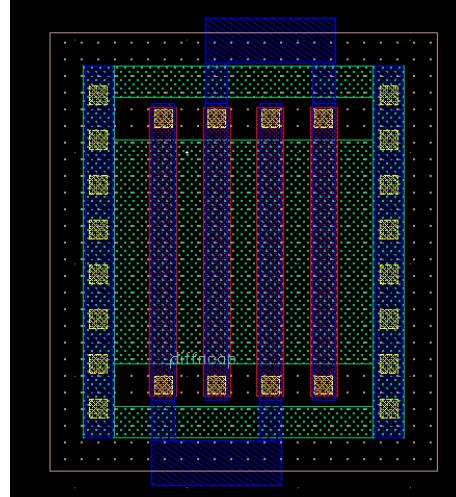
# MOS Varactor/Capacitor Pcell Options (ncap, dgncap)

- Parasitics
  - Model includes wiring, poly and n-well resistances
- Electrical parameters will vary based on form factor choice

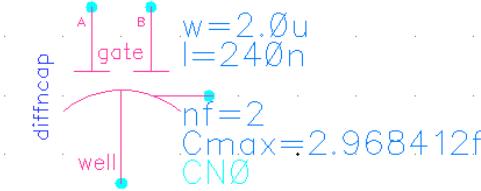


# Differential NMOS Varactor (diffncap)

- Interdigitated fingers for higher Q
  - Improved current flow between the devices
  - Same well: no well contact between gates
- Model includes wiring parasitics
  - 4-terminal device: G, G, NW, sub.
  - Same  $C_{area}$  as ncap
  - $C_{fringe}$  couples between gate terminals
  - Electrical parameters will vary based on form factor choices
- Use for differential excitation only\*



\*Use ncap for single-ended operation



RX Width	2.0μm
PC Length	240nm
Number of Gates	4
Max Capacitance (1V)	6.198324fF
Min Capacitance (-0.5V)	2.53309fF
Multiplicity	1
Sub Resistance	50.0 Ohms

# Voltage Limits : MOSVARs

- Device Group: 1.5V Thin Oxide (2.2 nm) MOSVARs
- Device Name: ncap
- Nominal Operating Voltage: 1.5V
- Maximum V<sub>g-d</sub>: 1.6V
- Vmax and Vos (Overshoot Voltage) Equations for gate oxide area, temperature and power on hours for 2.2 nm Gate Dielectrics
  - See BiCMOS8HP Design Manual Section 4.26.7
- Device Group: 2.5V Thin Oxide (5.2nm) MOSVAR
- Device Name: dgncap
- Nominal Operating Voltage: 2.5V
- Maximum V<sub>g-d</sub>: 3.63V
- Vmax and Vos (Overshoot Voltage) Equations for gate oxide area, temperature and power on hours for 5.2 nm Gate Dielectrics
  - See BiCMOS8HP Design Manual Section 4.26.8

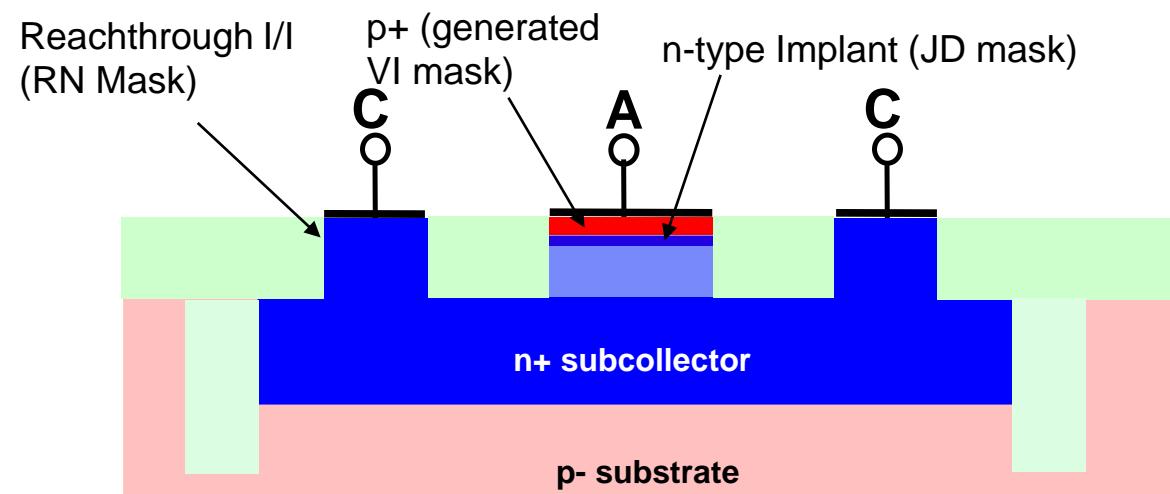
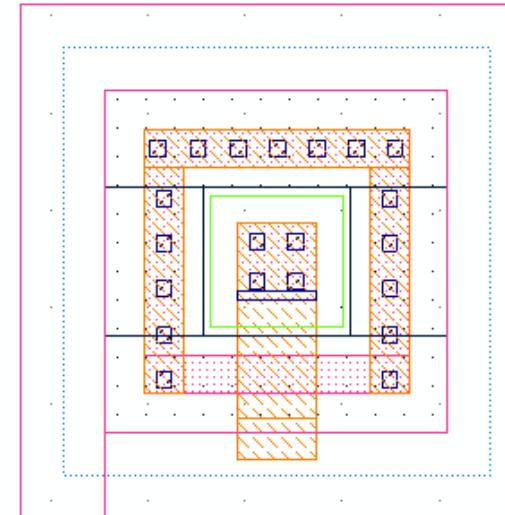
# Hyperabrupt Junction Varactor (havar)

- Optional device (**JD**, **VI** masks)
- Implanted p+ junction with n-type spike
- Scalable anode width and length
- $C_A(0V) = 2.05 \text{ fF} / \mu\text{m}^2$
- Degraded model accuracy past 3.0V
- AC model not characterized for forward biased operation

## CDF Options:

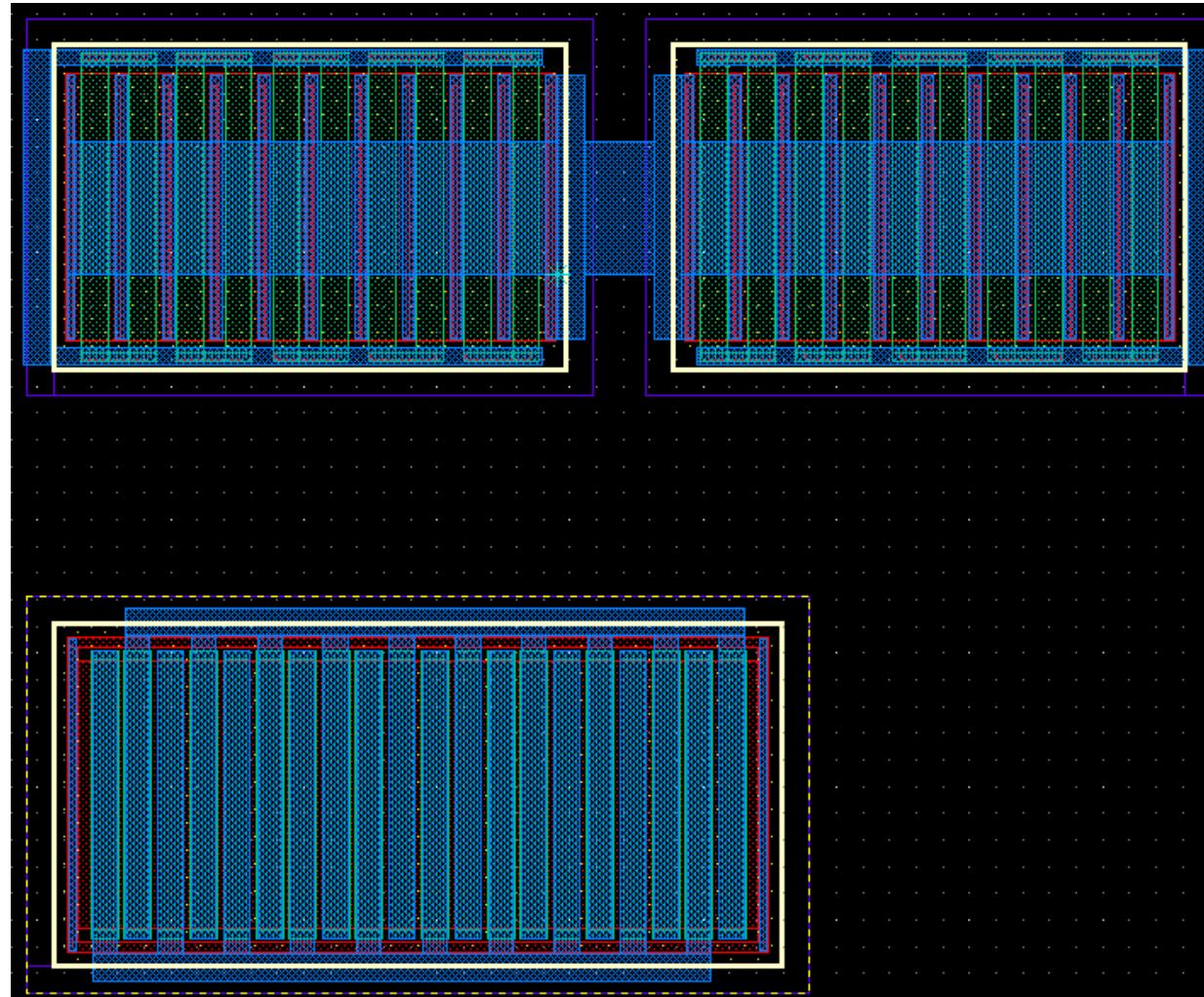
Anode Length  
Anode Width  
Number of Anode Fingers  
**or**  
Anode Width and  
Capacitance (Specify by  
Geometry)

Over-ride model inductance?



# Differential Varactors provide smaller layout area

havar Layout Example – 1 mm X 10 mm x 10



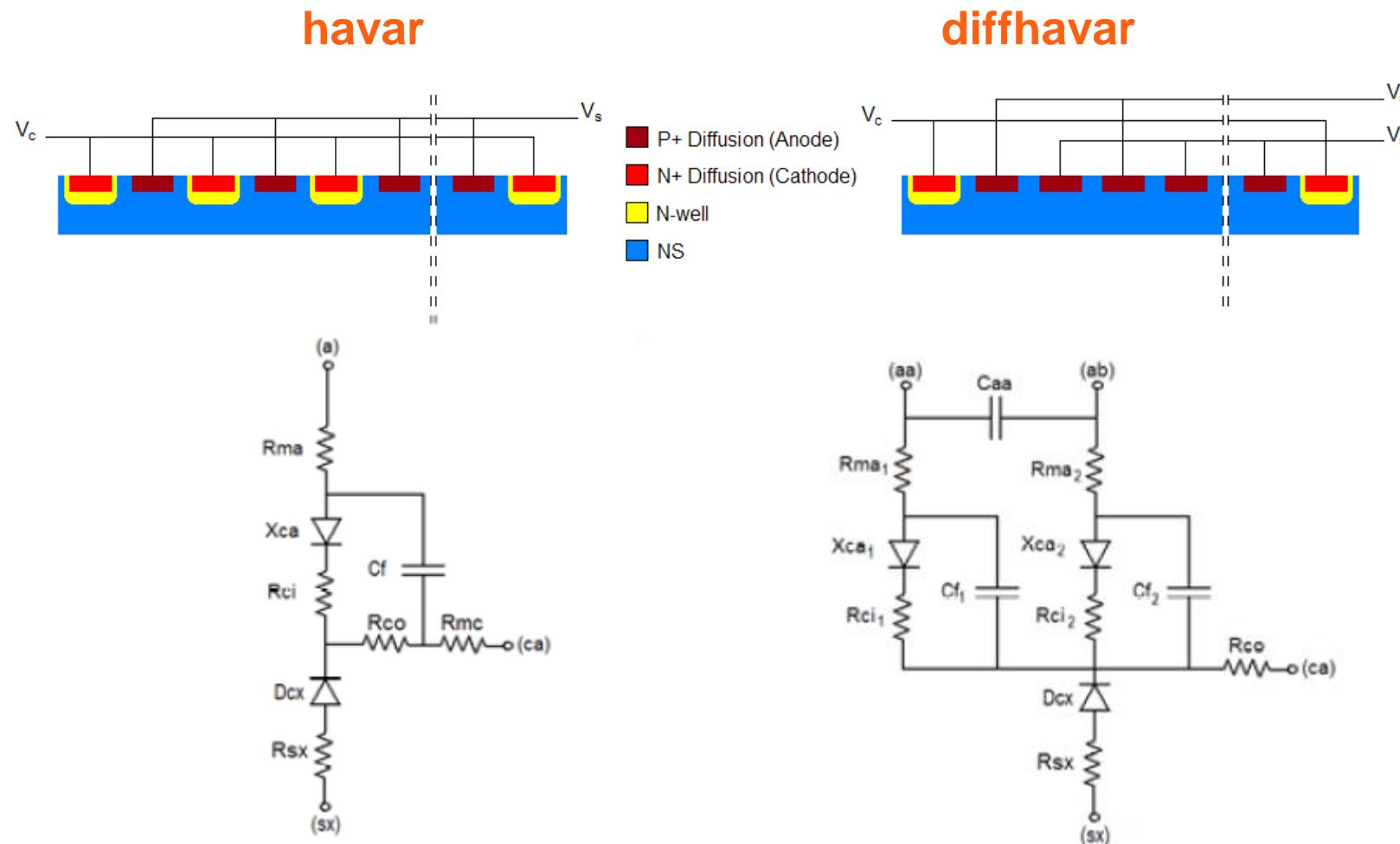
## havar

Two “regular” varactors with wells tied together, that is, wired in differential form. PortA is on left side and PortB is on right side. Well bias is applied to the M1 in the middle.

## diffhavar

Differential varactor layout with PortA on the top side and PortB on the bottom side. Well bias is applied on sides.

# Example: HAVAR Cross Section and Model Schematic

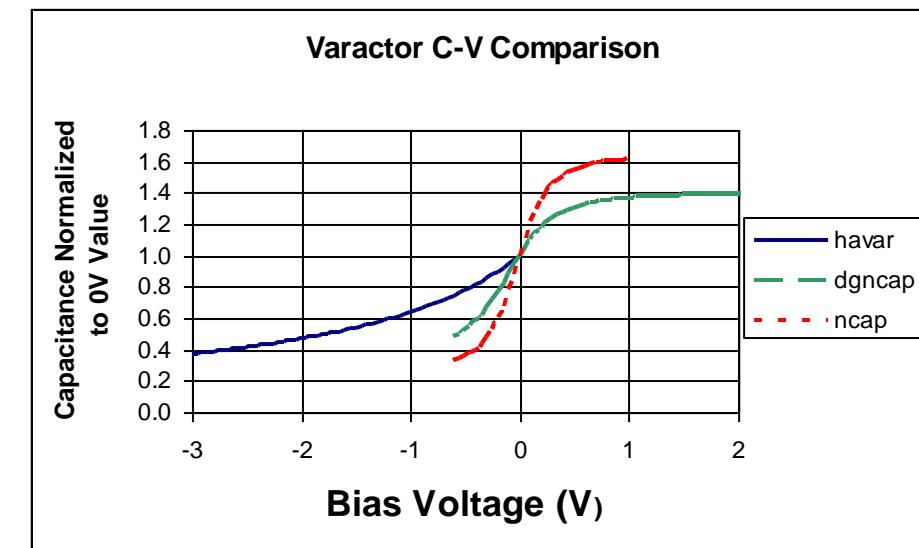
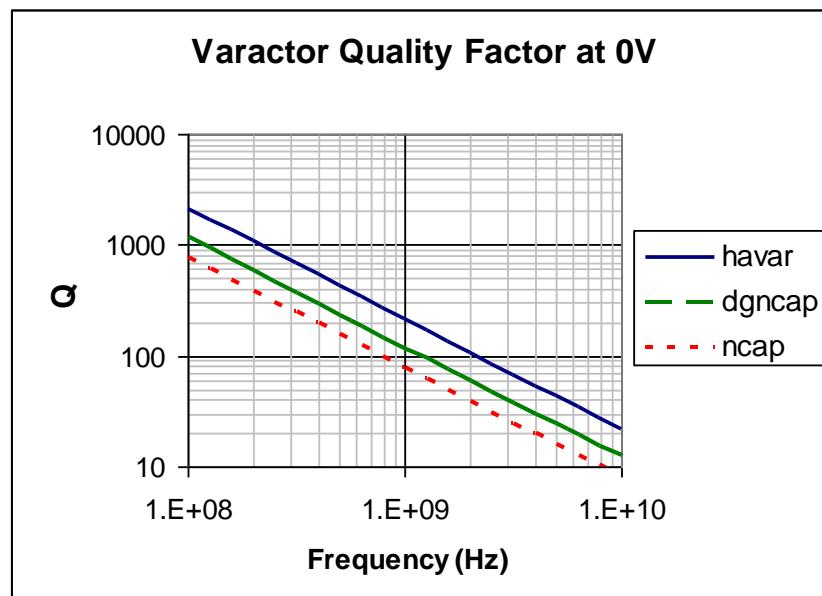


# Varactors: Q and C-V Characteristics

- Simulation Results: Varactor C-V and Q

**havar:**  $2 \times 10 \mu\text{m}$ , anode (p+) driven

**ncap, dgncap:**  $2 \times 2 \mu\text{m}$ , gate driven

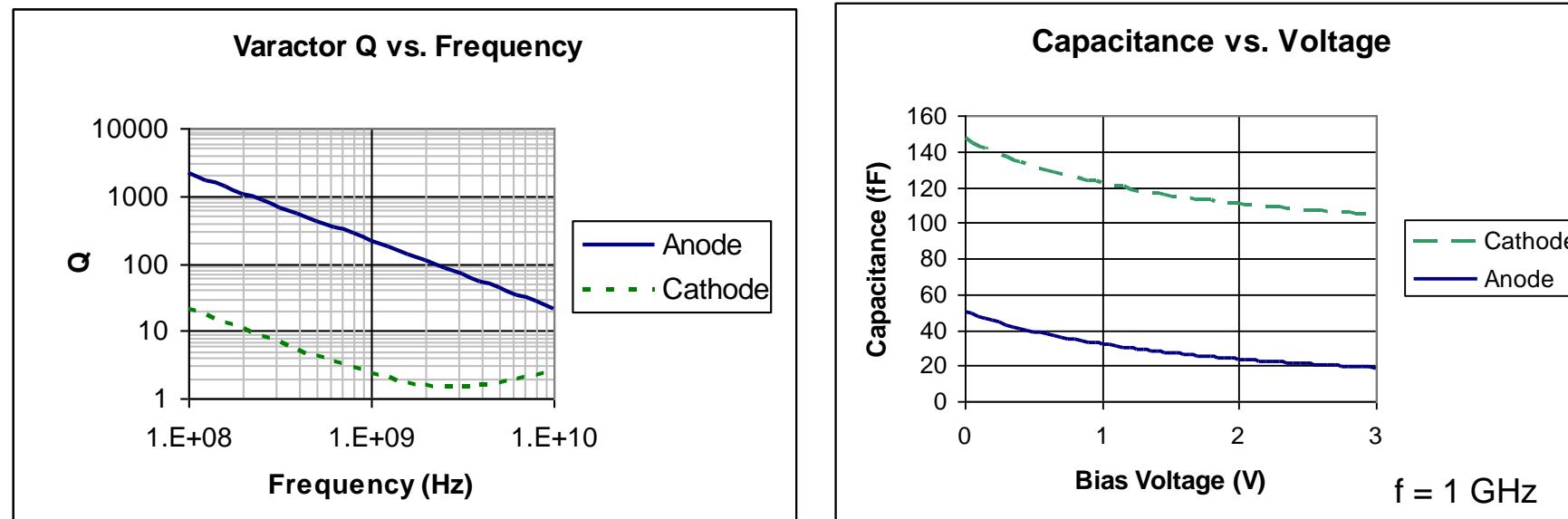


$$f = 1 \text{ GHz}$$

# Varactors: Cathode vs. Anode Excitation

- Q and tuning range are affected by anode vs. cathode RF excitation
- Cathode excitation activates parasitic subcollector-substrate diode

havar, 2 x 20 $\mu$ m



For the **havar**, **anode (p+)** excitation is preferred.

For the **ncap** and **dgncap**, **cathode (gate)** excitation is preferred

# Voltage Limits : HA Varactor

- Device Group: HA Varactor
- Device Name: havar
- Maximum Operating Voltage: 3.6V

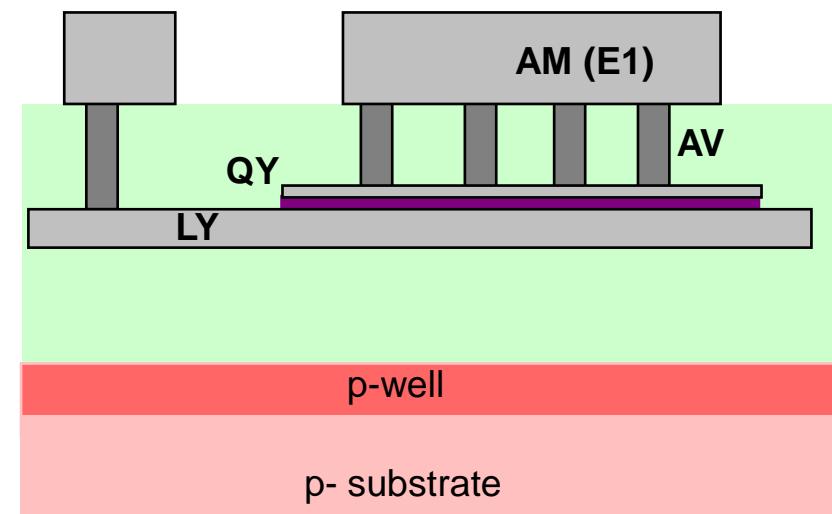
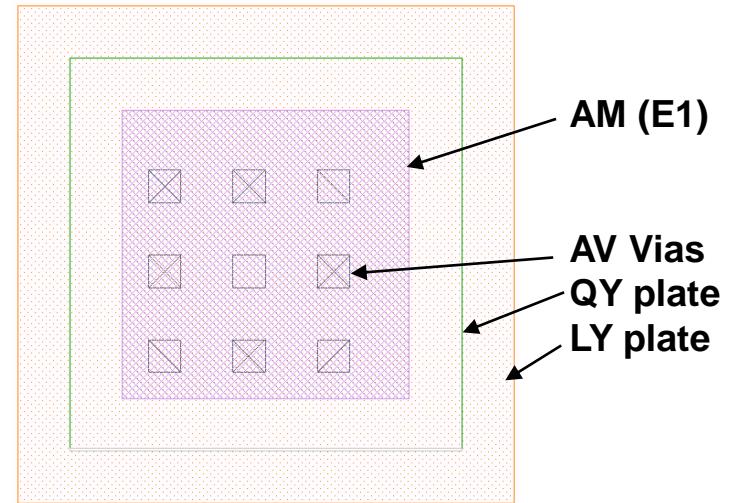
# Single Metal-insulator-metal capacitor (mim)

- Optional device: **QY** mask
- Single Nitride MIM with Al electrodes
- $C_A : 1.00 \text{ fF} / \mu\text{m}^2$
- **Min. size :**  $4 \mu\text{m} \times 4 \mu\text{m}$  ( $\geq 8\mu\text{m}$  preferred)
- **Aspect ratio :**  $1/3 \leq W / L \leq 3$
- **Max. area per MIM :**  $100,000 \mu\text{m}^2$
- **Max. area per chip :**  $2E6 \mu\text{m}^2$
- **MIM always above the LY metal**
- **As protection against charging:**
  - Bottom plate may not wire directly down – both terminals to top metal before other connections
  - Both plates must wire to silicon diffusion

## CDF Options:

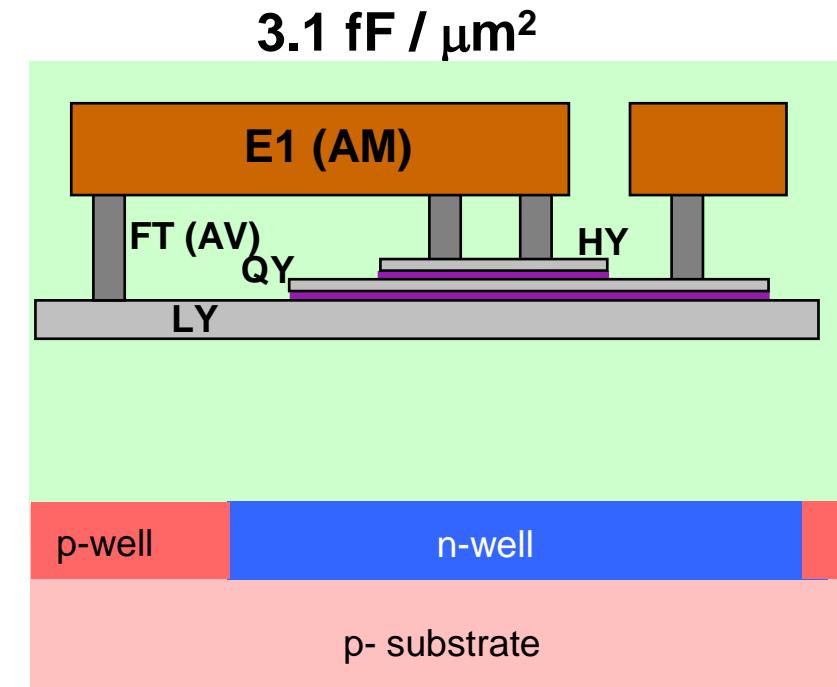
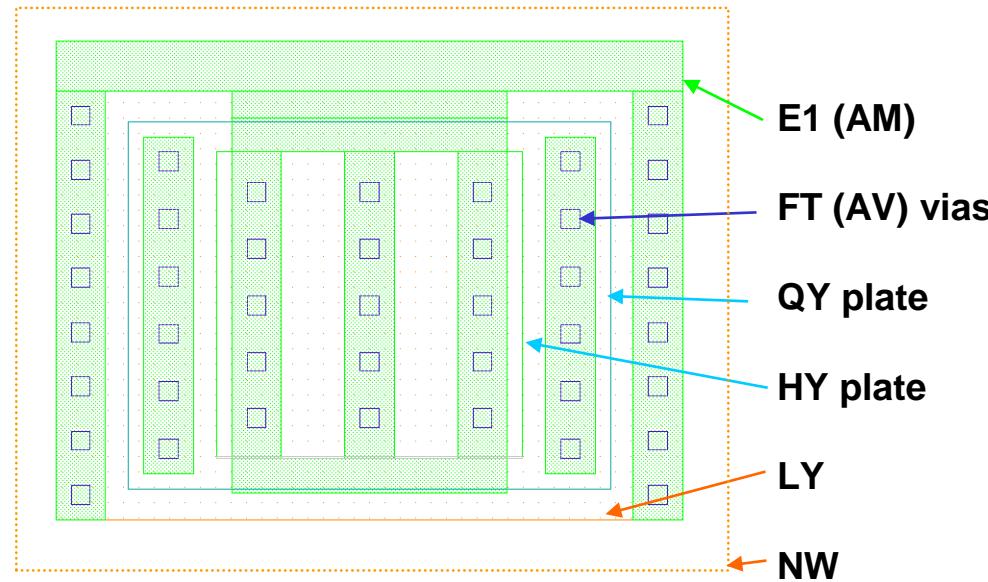
Length and Width  
Backplate (**sub**, NW, PI, BB, NS or DT)  
Override model inductance?

**sub** option allows mim to be placed over other devices



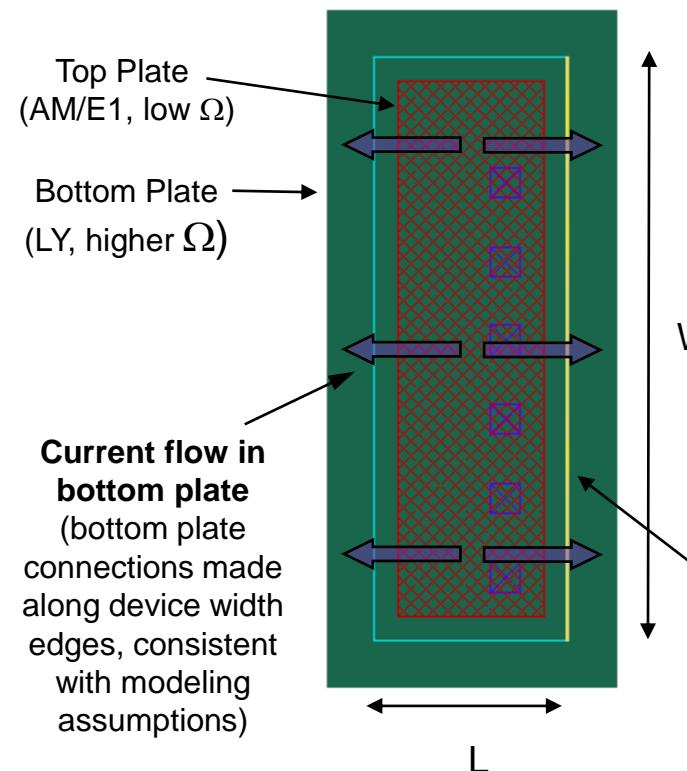
# Dual MIM Capacitor (dualmimcap)

- Optional device
  - Two-mask adder (QY, HY)
  - Consists of two parallel MIMs – one with  $1.0 \text{ fF}/\mu\text{m}^2$  (same as mim on previous chart) and a higher density single  $2.10 \text{ fF}/\mu\text{m}^2$  MIM.

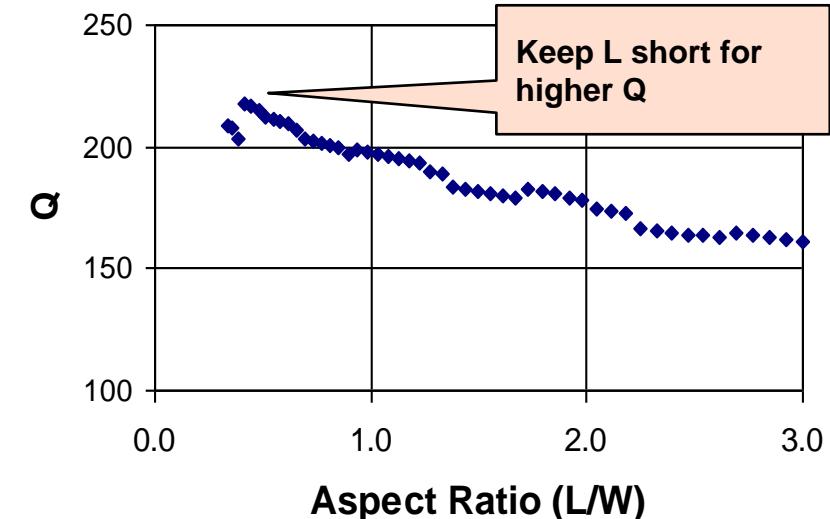


# MIM Quality Factor vs. Aspect Ratio

- LY bottom plate is more resistive than AM/E1 top plate metal
- Device width (W) & length (L) are NOT interchangeable
  - Device width (W) identified with EDGELAYER shape in layout pcell
- For proper model-to-hardware correlation of Q, connect LY bottom plate along width (W) edges
- For best Q, keep L dimension short (minimum L = W/3 =  $\sqrt{\text{Area} / 3}$ )



MIM Q vs. Aspect Ratio (L/W)



EDGELAYER shape (identifies orientation of device width (W))

Note : Presence of shape “edgeLayer” “dg” in the pcell is along the W dimension (non-valid layer by default)

# mim CDF parameters

- Physical configuration:  
Length and Width and  
Multiplicity
- Specify by Geometry or Value

Override modeled  
Self-inductance (-2H)\*

\*Allows user to supply MIM inductance  
calculated from EM simulators in critical  
high frequency (>20GHz) applications.  
Requires user modification of extraction  
decks to preserve override in simulation  
from layout

Schematic simulations include  
estimated bottom plate  
parasitic capacitance (Y/N)

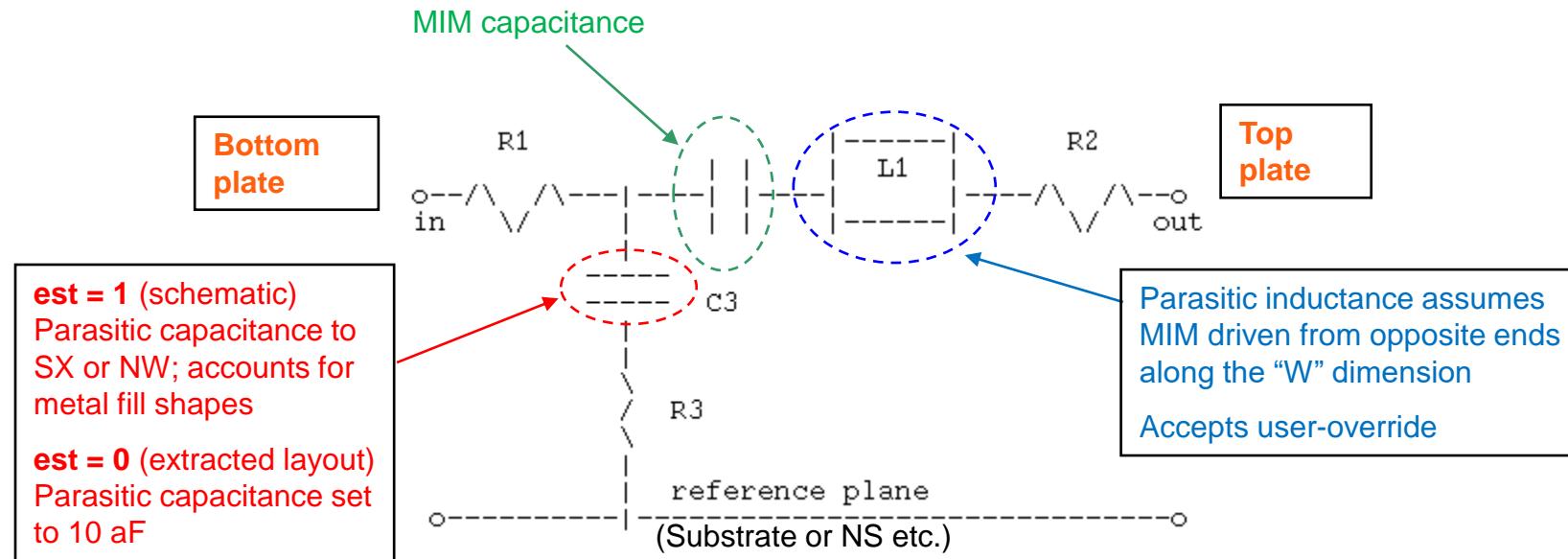
Wireopt	213
Backplate	SUB ▾
Specify cap by geometry?	<input checked="" type="checkbox"/>
Capacitance (effective)	328.536f F
Capacitance	328.536f F
Length	18.0u M
Width	18.0u M
Multiplicity	1
Override model inductance?	<input checked="" type="checkbox"/>
Inductance (H)	-2 H
Include model parasitics?	<input checked="" type="checkbox"/>
Define Sub Resistance	userDefined ▾
Sub Resistance	50.0 Ohms

Wireopt - Set by  
library properties

**SUB:** p-well or mixed  
wells underneath  
**Other options:**  
NW,PI,T3,BB,NS

Used by model.  
50Ω default.

# MIM Capacitor Model



## 16.1 Model Features

The single and dual nitride MIM models include:

- Input parameter specification for length and width or length and capacitance.
- "setind" is the user determined value for the parasitic inductance. The default value of -2, which is used as a switch, forces the model calculated inductance to be used.
- "est" switch includes bottom plate parasitic capacitance (est=1, default) for the case of MIMs without any other devices placed underneath the capacitor. The capacitance is set to a negligible value of 0.01fF (est=0) to support the case of other devices being placed under the MIM where only the layout extraction tool can provide for an accurate calculation of this bottom plate parasitic capacitance.
- "rsx" determines the series resistance (rsx=50, default) from the substrate below the device to the reference node.
- Device temperature difference with respect to circuit temperature (dtemp).

# Voltage Limits : Single MIM and Dual MIM

- Device Group: Single MIM
- Device Name: mim
- Vmax Equation for area, perimeter, temperature and power on hours
  - ~ 17V, See BiCMOS8HP Design Manual Section 4.26.9
- Device Group: Dual MIM
- Device Name: dualmim
- Vmax Equation for area, perimeter, temperature and power on hours
  - ~8V, See BiCMOS8HP Design Manual Section 4.26.10

# Resistors

- Rectangular only - no “dogbone”, bends, or center taps
- Best matched layouts: duplicate resistor & nearby wires (including potentials)

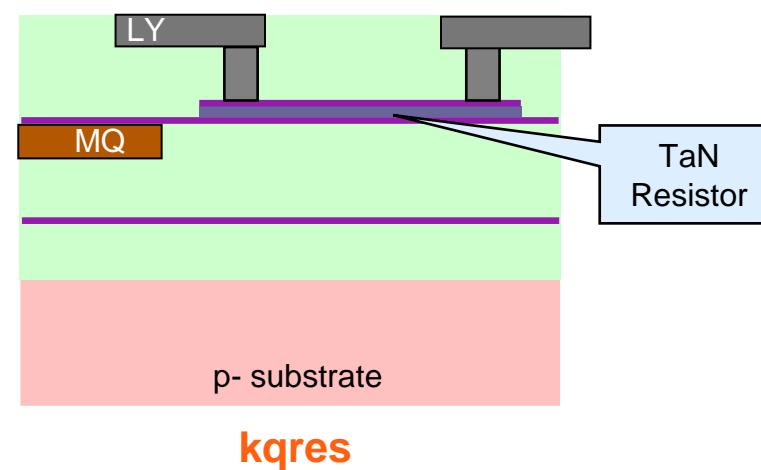
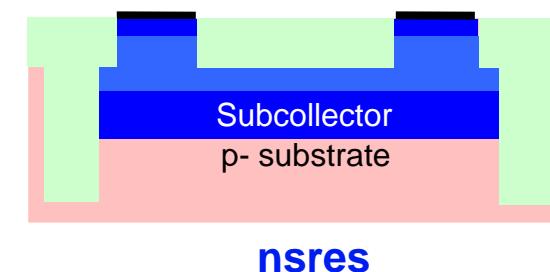
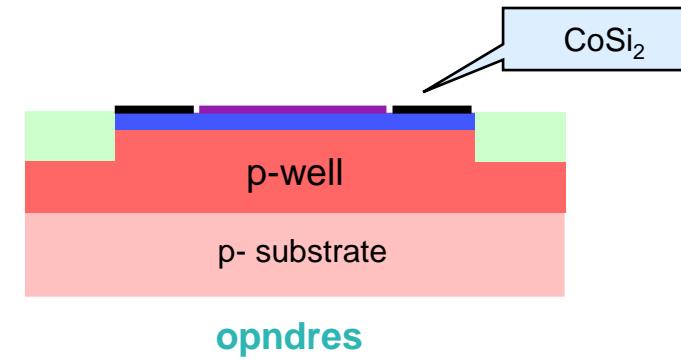
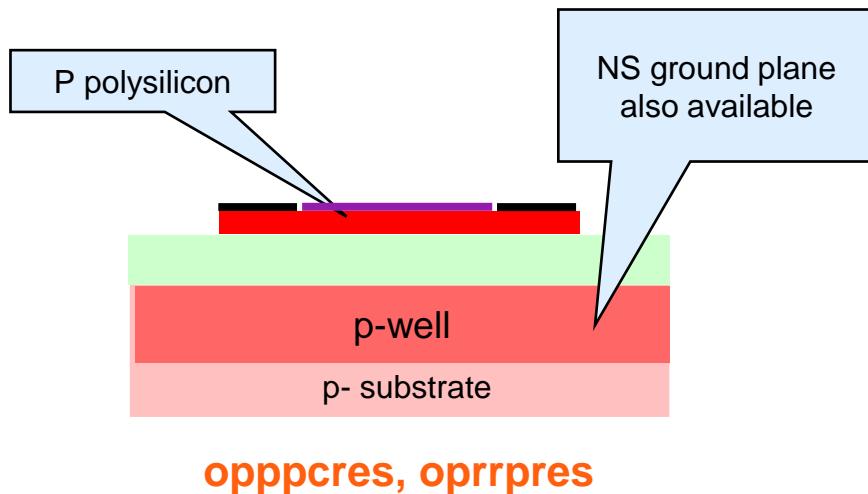
Device Name	Structure [additional mask]	Sheet Resistance ( $\Omega / \square$ )	Sheet Rs Tolerance	Current Limit (mA/ $\mu\text{m}$ )**	Voltage Coeff. ( ppm / V )	Rs Temp Coeff. (tc1 / tc2, ppm / °C)*
opndres	n+ Diffusion resistor [OP]	77 ± 9.5	± 13%	1.0	0	1800/1.3
oppccres	p+ poly over isolation [OP]	340 ± 51	± 15%	0.4 **	0	66/0.57
oprrpres	RR Poly over isolation [OP RR]	1700 ± 340	± 20%	0.1	-240	-1079/ 2.15
nsres	n+ Diffusion Subcollector	8.8 ± 1.32	± 15%	1.0	60	1586/1
kqres	TaN at MQ metal [KQ]	60.5 ± 4.8	± 8%	0.5 **	0	-399/0.72

$$* \Delta R = tc1 * T + tc2 * T^2$$

\*\* See Design Manual for the limit conditions and/or equations

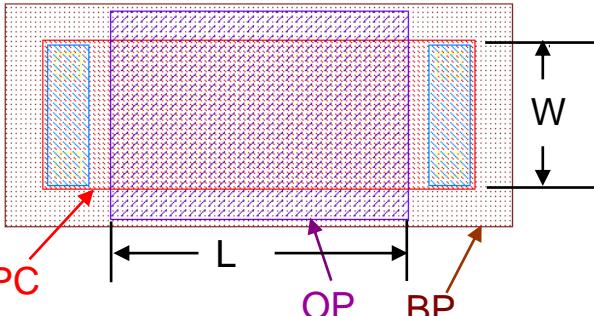
# Resistor Structures

- Silicide block defined by OP mask for diffusion and poly resistors
- Resistor ends have different electrical properties than body
  - Use long resistors to minimize end effects (GR 710R, GR712R)
- **Rectangular shapes only, no center taps**



# Resistor Properties Form

oppccres over sub



PC

OP

BP

L

W

Description: P+ poly OP Resistor

Backplane Option: sub

Specify Res by Geometry?

Resistance (total): 3.69388K Ohms

Resistance:

Width >= 0.2u: 200.0n M

Length >= 1.6u: 1.6u M

Number of Series Bars: 1

Parallel Bars: 1

Multiplicity: 1

Sub Resistance: 50.0 Ohms

Temperature Delta: 0.0 C

Enter length & width (R calculated) or resistance and width (L calculated)

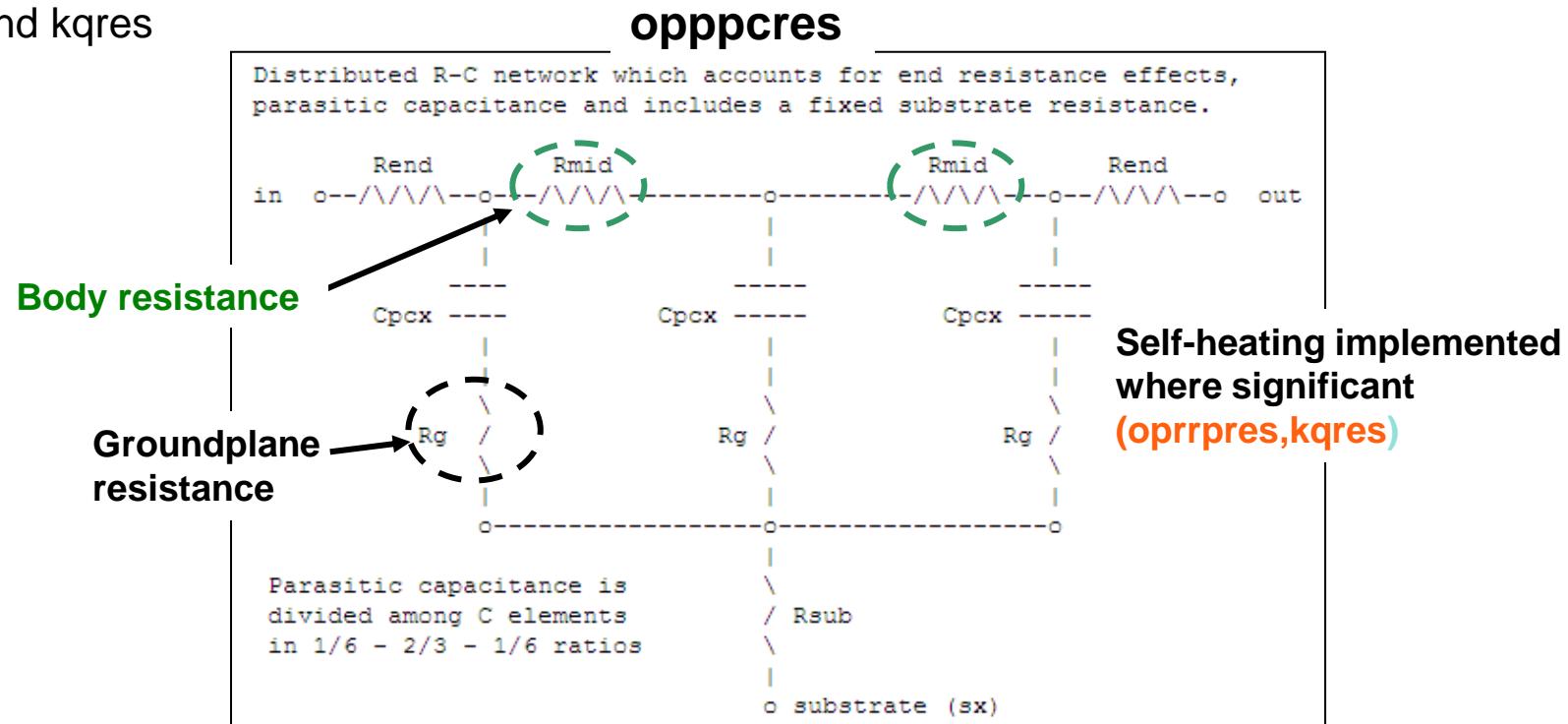
Series bars and multiplicity are mutually exclusive

Used by model. 50Ω default.

Device Temperature Rise from Ambient (deg C)

# Resistor Models

- “ $2\pi$ ” network models (RF by design)
- Effects included:
  - Device mismatch
  - Temperature coefficient of resistance (TCR)
  - Self-heating for oprrpres, and kqres
  - Ground plane resistance
  - Flicker (1/f) noise



# Resistor Current Limits

## 4.8.1 Resistor Specifications

The following specifications may be used as a guide in applications for the resistors.

Table 4-18. Resistor Design Specifications					
Specification	NS Diffusion	N+ Diffusion	P+Poly	RR poly	KQ BEOL
$R_s (\Omega/\text{sq}) (0V, 25^\circ\text{C})$	$8.8 \pm 1.76$	$77 \pm 9.5$	$340 \pm 51$	$1700 \pm 340$	$60.5 \pm 4.8$
Current Limit <sup>2</sup> (mA/um)	< 1.0	< 1.0	See Section 5.3.7.2 , Front-End of Line Resistors	< 0.1	See Section 5.3.7.3 , Back-End-Of-Line KQ Resistors

1. Sheet resistance:  $R_s \pm 3 \sigma$  tolerance

2. OP resistor current level is limited by heating.

### RR Polysilicon Resistor current Limitations:

With the allowed current density of 0.1 mA/μm and  $1700 \Omega/\square$ , the maximum heat generated by the RR resistor will be less than  $5^\circ\text{C}$ .

# P+ Poly Resistor Current Limits (1)

## 5.3.7.2 Front-End of Line Resistors

P+ polysilicon are limited to 0.4 mA/um unless further limited by metal electromigration as described below, under the assumption that the metal line is the same temperature as the resistor.

Resistors can heat up to a point where metal migration becomes an issue. Tabulated guidelines assume that the resistors are laid out with the metal leading to the resistor as wide as the resistor. This is for DC conditions for 100,000 hours of operation at the silicon temperature indicated.

### P+ Polysilicon Resistor current limitations:

*Table 5-16.P+ Poly Resistor current limitations*

<b>SiTemp C</b>	<b>3.6 V</b>	<b>5.5 V</b>
125	0.31 mA/um	0.30 mA/um
120	0.37 mA/um	0.35 mA/um
115	0.40 mA/um	0.39 mA/um
≤ 110	0.40 mA/um	0.40 mA/um

# P+ Poly Resistor Current Limits (2)

For P+ poly resistors, electromigration may be evaluated for specific cases by calculating the temperature rise for the resistor and using the electromigration limits from the Back-End-Of-Line reliability section under the assumption that the metal line is the same temperature as the resistor. AC operation can have a much relaxed criteria but 0.40 mA/um absolute maximum should be maintained.

The formula for thermal resistance (THERMRES) is:

$$THERMRES = 144150 \times AREA2^{-0.87121}$$

where,

$$AREA2 = (AREA + 5 \times WIDTH)$$

AREA is the area of the resistor ( $\mu\text{m}^2$ )

WIDTH is the resistor width ( $\mu\text{m}$ )

The Resistor temperature (ResTemp) is then:

$$ResTemp = SiTemp + (THERMRES \times Power)$$

where, SiTEMP is the base silicon temperature (degrees C) and Power is the dissipated power in the resistor (Watts)

# KQ Resistor Reliability

## 5.3.7.3 Back-End-Of-Line KQ Resistors

**Caution:** KQ resistors can produce high temperatures that can compromise integrity of metal lines leading up to the resistor as well as metal lines adjacent to the resistor. Adjacent resistors can heat each other compromising the resistor precision.

The maximum allowed current through any KQ resistor is 0.5 mA/um of width unless the metal leading to the resistor limits the current to a lower value or the change in resistance through life is more than the circuit can tolerate.

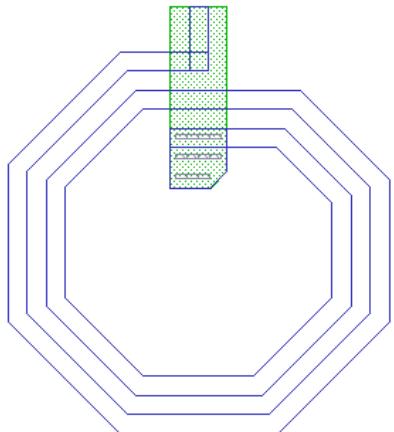
Table 5-17.KQ Resistor maximum current limits

Si Temp C	KQ maximum current limit (mA/um) <sup>1</sup> for each BEOL metal option		
	for 3 Levels of Copper Metal [M1, M2, MQ] (5 Total Levels of Metal)	for 4 Levels of Copper Metal [M1, M2, M3, MQ] (6 Total Levels of Metal)	for 5 Levels of Copper Metal [M1, M2, M3, M4, MQ] (7 Total Levels of Metal)
< 70	0.50	0.50	0.50
80	0.50	0.50	0.472
90	0.474	0.444	0.422
10	0.410	0.386	0.368
110	0.341	0.324	0.310
120	0.270	0.258	0.248
125	0.233	0.224	0.217

1. Maximum KQ resistor current limit using a 30 um wide resistor and only the LY design level for its wiring. Limits in table are instantaneous peak, at no time should dc+ac current exceed values shown in table. If the resistor experiences an AC signal then, the peak current must be less than or equal to these limits. Values increase if AM and LY design level wiring are used in parallel for electromigration considerations or the KQ resistor width is less than 30 um. However, the maximum allowed current limit for any KQ resistor is 0.50 mA/um.

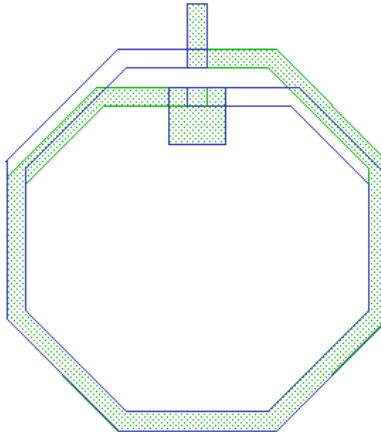
# Inductors

## AM and Dual Metal E1/MA Last Metals



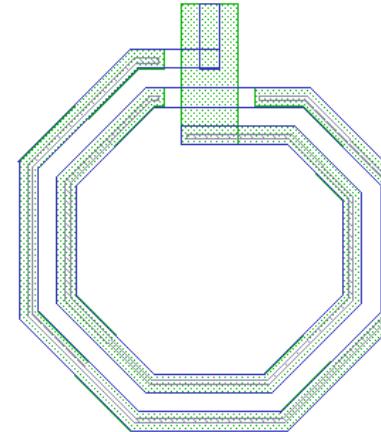
ind

Planar spirals  
(AM, MA)



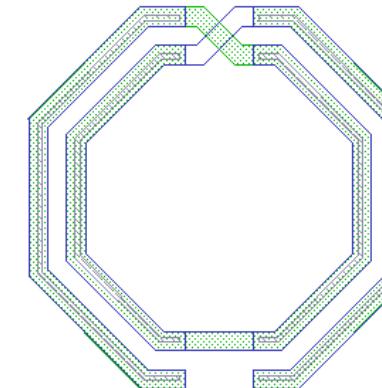
inds

Series spirals  
(MA/E1)



indp

Parallel spirals  
(MA/E1)



symind,symindp

Symmetrical inductor, with  
center tap  
(symind: AM/LY, MA/E1;  
symindp: MA/E1)

- High Q
- Lowest parasitic capacitance, but lower peak Q due to turn resistance

- Highest inductance density, but also higher parasitic capacitance turn-to-turn and lower-coil to substrate

- Lowest series resistance, but also higher parasitic capacitance turn-to-turn and lower coil to substrate

- Differential applications.
- Lowest parasitic capacitance to substrate, highest Q

# Single Layer Inductor (ind)

- Scalable High-Q Inductor
- Low series R
- Low capacitance (6 to 9  $\mu\text{m}$  total dielectric thickness)
- DT Lattice or M1 ground plane
- DT ground plane connected ground in layout using “BB” “IND” shape
- 0.1 – 48 nH
- Avoid large conducting planes and closed current paths around inductor (inductance, peak Q decrease)
- For DT ground plane, keep large substrate contacts > 80 $\mu\text{m}$  from inductor

## CDF Options:

Outer Dimension: 100 - 300  $\mu\text{m}$

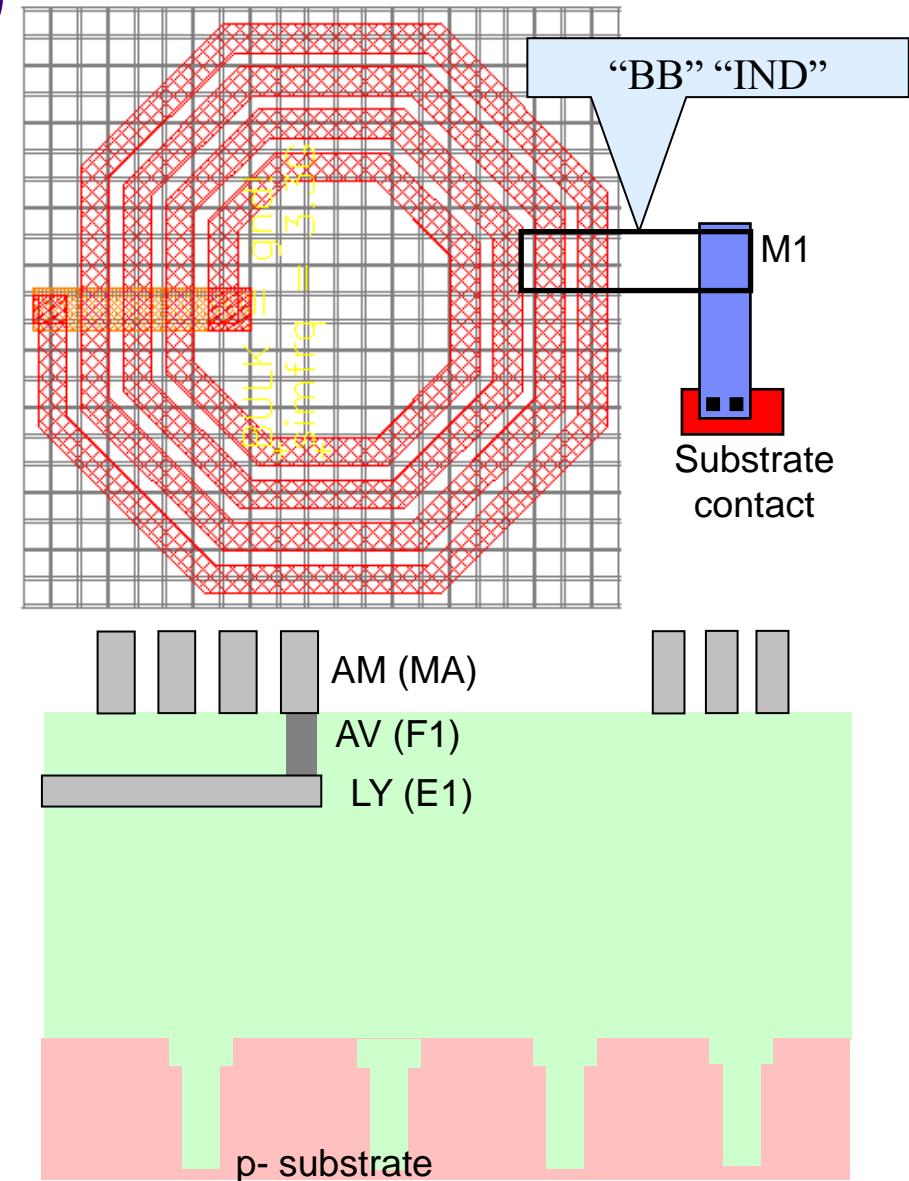
AM (MA) Width: 4-25  $\mu\text{m}$

Number of Turns: 1 min., 0.25 increments

Turn-Turn Space: 3-5  $\mu\text{m}$

Wire Options: 211,311,411,213, set by library properties

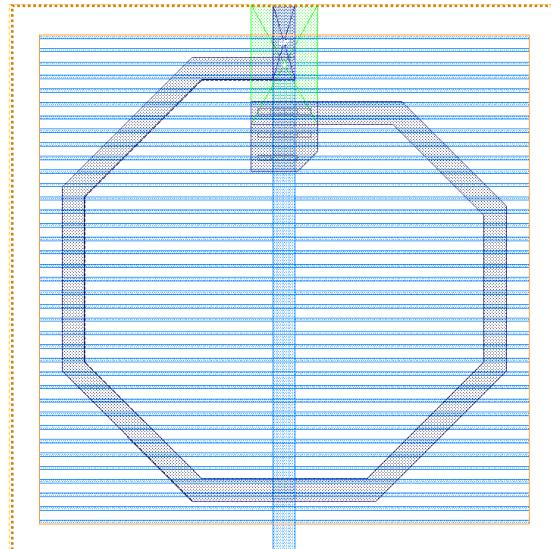
Ground plane: DT, M1



# Inductor Ground Planes

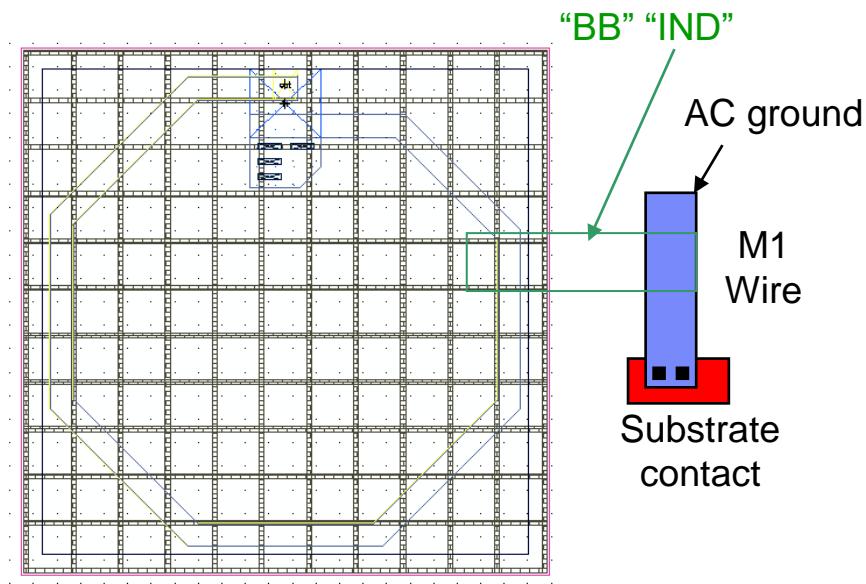
- **M1**

- Shielding from substrate losses/noise
- Higher parasitic capacitance: Lower self-resonance, sharper roll-off near peak Q
- If one side of the coil is AC ground, connect the inner terminal of the coil to the M1 ground plane using a low-impedance via/metal stack under the inside terminal.
- If neither side is AC ground, choose “External connection” in CDF and wire to suitable AC ground.



- **DT**

- Provides reduced capacitance to substrate
- Higher self-resonant frequency, lower peak Q
- Connect ground plane to an AC ground – **NOT sub!**
- Extraction connects ground plane to M1 touching a substrate contact



# Ind CDF Parameters

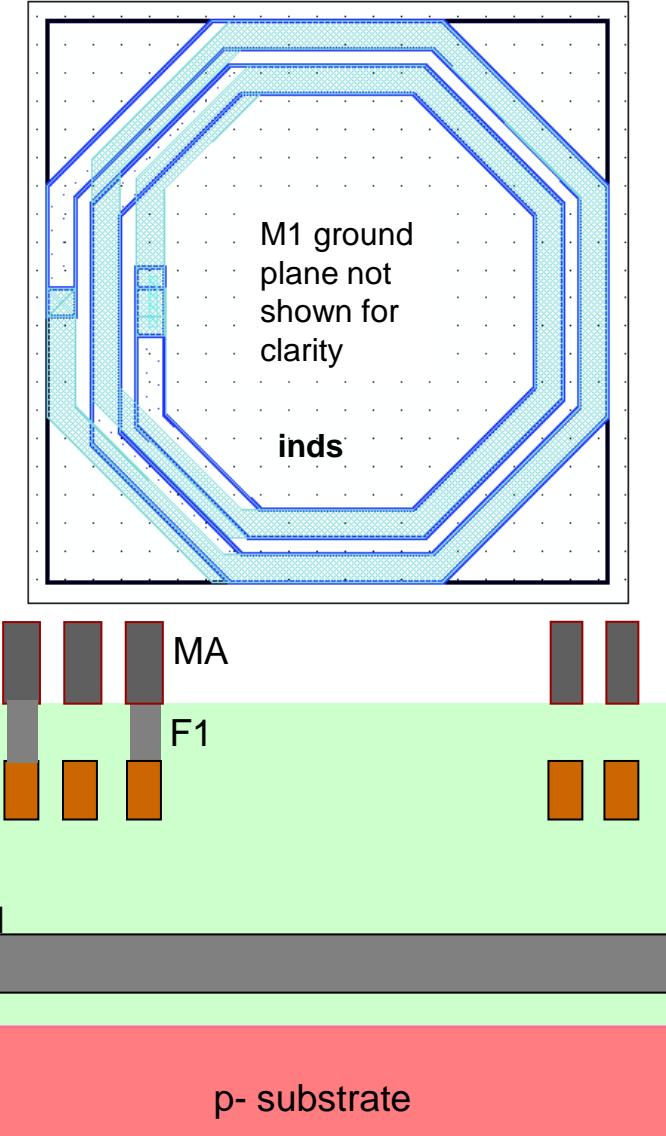
MA Option Shown

Spiral outer diameter and wire MA (AM) width	Outer Dimension 250.0 $\mu$ M
Possible n given by outer diameter and MA (AM) width	Metal Width 10.0 $\mu$ M
E1 (LY) width	n turns 2
Spacing between spirals	Max turns 6
Wireopt - Set by library properties	Exceed max turn limit? <input type="checkbox"/>
Select DT or M1 ground plane	Underpass Width 15 $\mu$ M
Device Temperature Rise from Ambient (deg C)	space 5.0 $\mu$ M
	Wireopt 211
	Groundplane <input checked="" type="radio"/> DT <input type="radio"/> M1
	Hollowness (Ri/Ro) 0.75
	Inductance <b>Call-backs</b> 1.722n H
	Peak Q Frequency 6.68G Hz
	Temperature Delta 0
	High Current Application <input type="checkbox"/>

# Series and Parallel Inductors (inds, indp)

- Available in Dual Metal E1/MA BEOL only
- Built at MA and E1 levels
- **inds – spirals in series**
  - Highest L per unit area
  - 0.25–180.2 nH
- **indp – spirals in parallel**
  - Highest Q (high 20's)
  - 0.09-46.5 nH

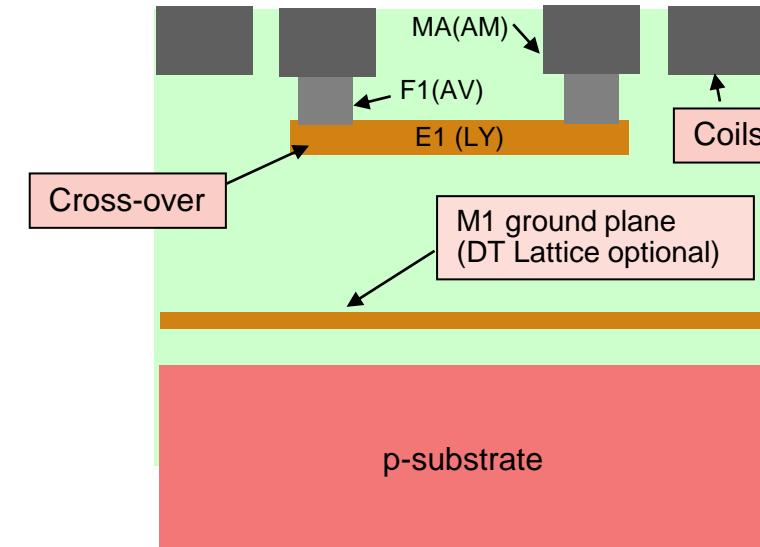
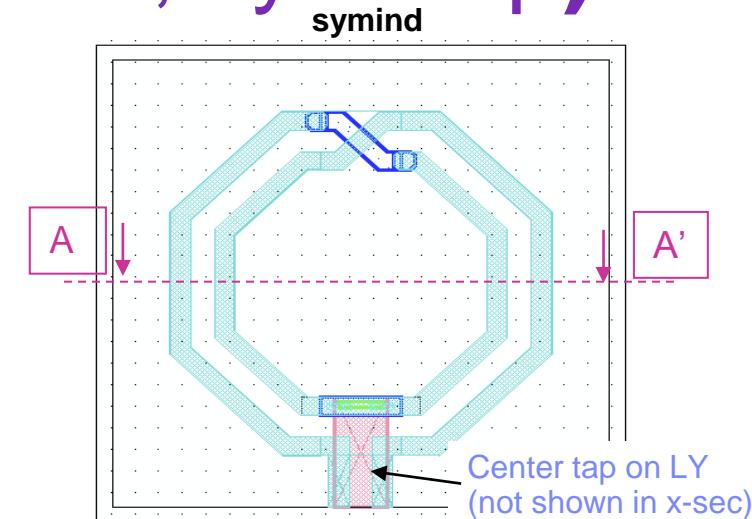
CDF Options	inds	Indp
Outer Dimension	100-300um	100-300um
Supported MA Turn width	4-25um	4-25um
Turn to Turn Space	3-5um	3-5um
Wire Option	213, 313, 413 (set by lib properties)	213, 313, 413 (set by lib properties)
Number of turns	1 min, 0.25 turn increments	1 min, 0.25 turn increments
Ground plane	DT, M1	DT, M1



# Symmetrical Inductor (symind, symindp)

- Symmetrical design, with a regular (symind) or a parallel (symindp) configuration
- The inductor in/out ports use the last metal
  - Optional center tap in LY
- **Symind** (0.05-40 nH), **sysminp** (0.03-40 nH)
- **symindp available in dual metal E1/MA BEOL only**  
Uses parallel MA / E1 coils
  - Differential Applications
  - Lowest parasitic capacitance to substrate, high Q

CDF Options	symind	symindp
Outer Dimension	50-300um	50-300um
Supported MA width	4.24-25um	4.24-25um
Turn to Turn Space	3-5um	3-5um
Wire Option	211, 311, 411, 213, 313, 413 (set by lib properties)	211, 311, 411, 213, 313, 413 (set by lib properties)
Number of turns	1 min, 1 turn increments	1 min, 1 turn increments
Ground plane	DT, M1	DT, M1



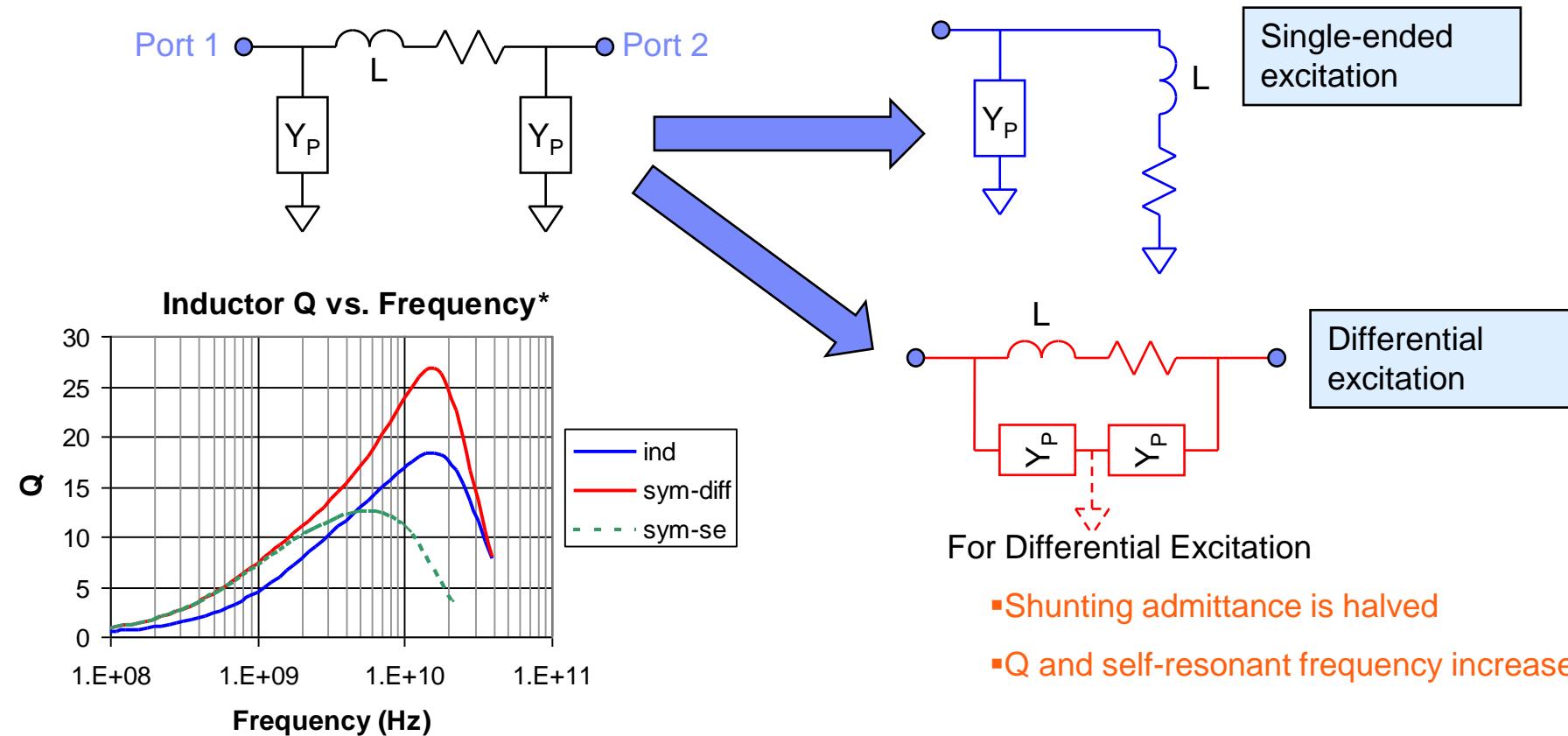
# Symmetrical Inductors Properties Form

symind		symindp	
Outer dimension	100 $\mu$ M	Outer dimension	250.00 $\mu$ M
Spiral width	6.48 $\mu$ M	Spiral width	10.00 $\mu$ M
n turns	1	n turns	1
Max turns	2	Max turns	6
Space	5.00 $\mu$ M	Space	5.00 $\mu$ M
Inductance	191.00 p H	Inductance	562.00 p H
Peak Q Frequency	53.74 G Hz	Peak Q Frequency	13.47 G Hz
cross via field width	<input checked="" type="radio"/> min <input type="radio"/> max <input type="radio"/> User Defined	Include centertap wire?	<input checked="" type="checkbox"/>
Include centertap wire?	<input checked="" type="checkbox"/>	Underpass width	15.00 $\mu$ M
Underpass width	13.6 $\mu$ M	Wireopt setting	213
Wireopt setting	213	Groundplane	<input checked="" type="radio"/> DT <input type="radio"/> M1
Groundplane	<input checked="" type="radio"/> DT <input type="radio"/> M1	High Current Application	<input checked="" type="checkbox"/>
Temperature Delta	0	Temperature Delta	0.0 C
High Current Application	<input checked="" type="checkbox"/>		

Dual Metal E1/MA Option shown

# Differential Symmetric Inductor

- Configured for differential excitation
  - Compact compared to standard spirals in differential LC-tank VCOs
  - Convenient to wiring due to the proximity of the 2 ports



\*8RF example. 8HP is similar to 8RF.

TTM-000008 Rev6

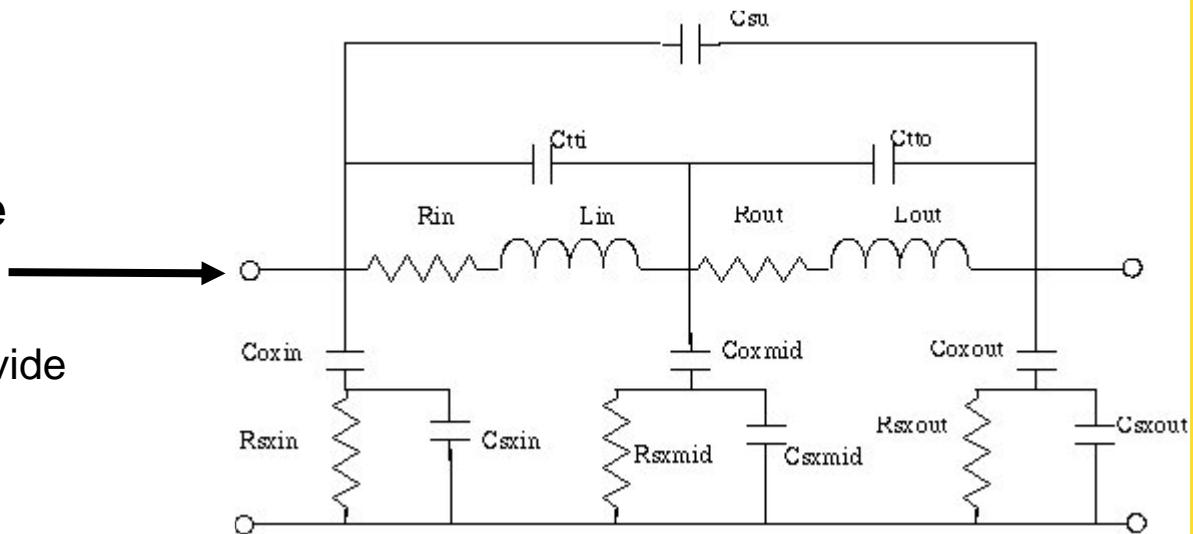
Confidential

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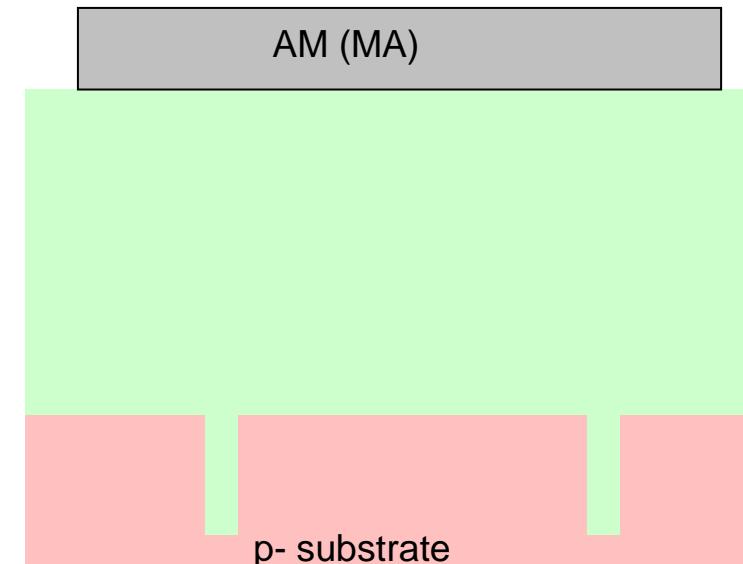
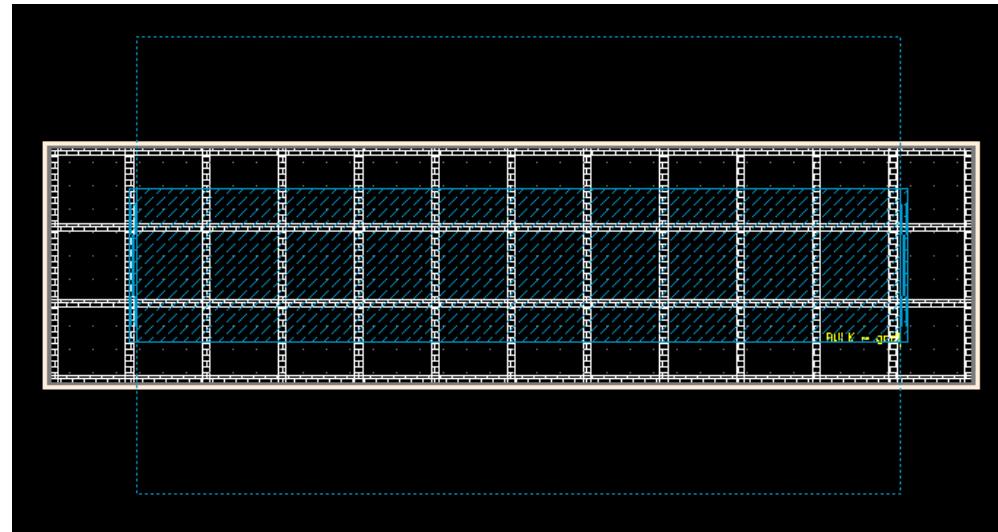
# Inductor Models

- Model Name and Nodes vary by inductor type
- Broadband Model
  - R-L ladder network replaces single elements to provide frequency-dependent behavior
  - Suitable for broadband and transient analysis
- Accurate Modeling of Losses as Function of Frequency
  - Skin Effect
  - Proximity Effect
- White Paper “On Chip Inductors and Their Figure of Merit” Available on Global-FoundryView
  - Inductor Figure of Merit
  - Inductor Technical Features
  - Design Trade Offs
- Wire the ground plane correctly as recommended in the Design Manual for valid inductor modeling



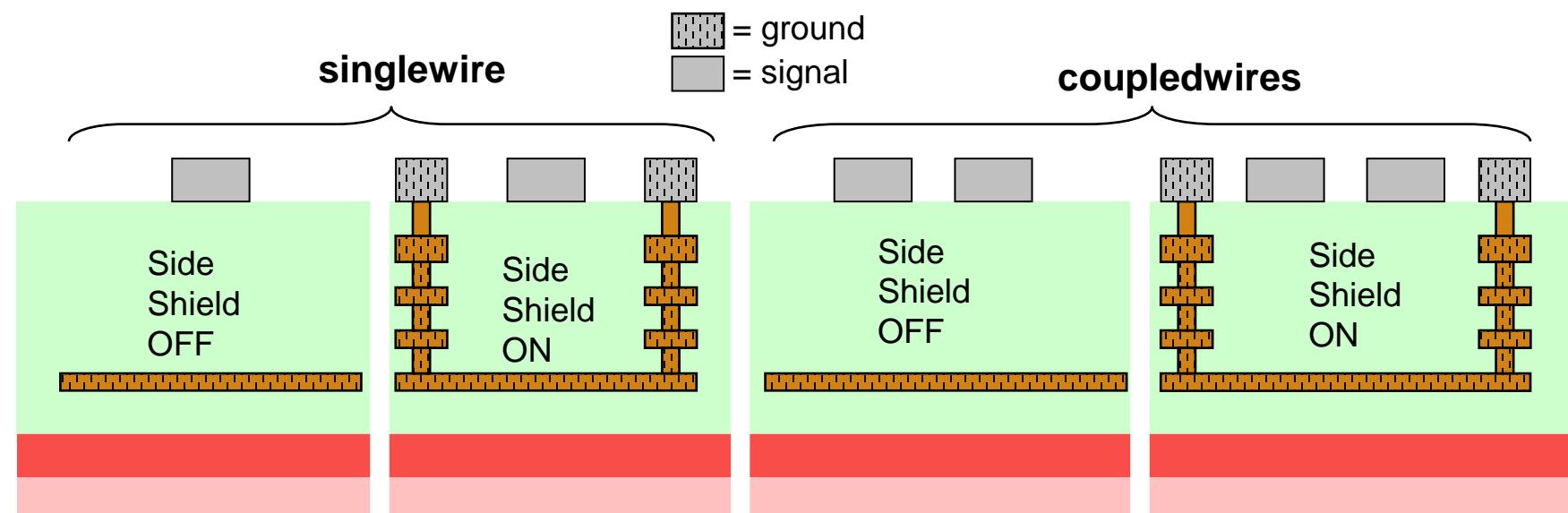
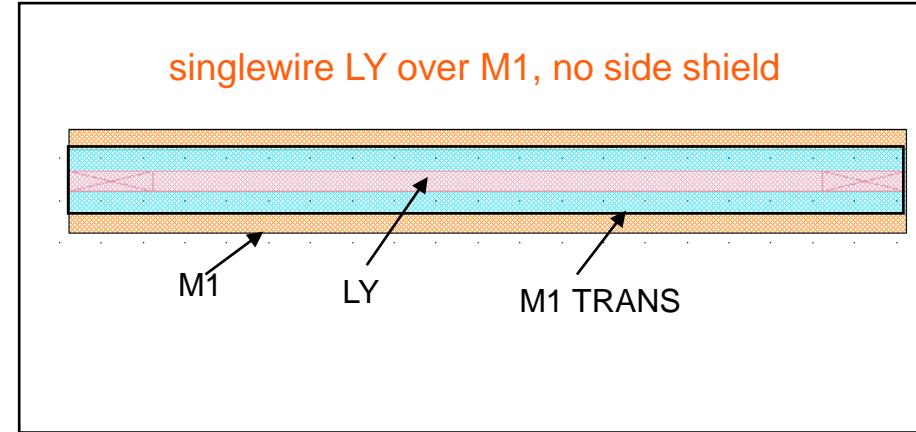
# RF Interconnect Line (rfline)

- AM (MA) metal over DT
- Inductor with a very low inductance value and high Q
- Transmission line model for section of top metal wire
  - “AM (MA)” “IND” identifies device
  - Length: 100-1500  $\mu\text{m}$
  - Width: 4-25  $\mu\text{m}$
- No device allowed under rfline



# Transmission Lines (singlewire, coupledwires)

- Purpose: Impedance-controlled interconnect for high frequency signals where space permits large ground planes
- Allow inclusion of controlled and predictable interconnect effects in simulations as early as the schematic design phase
- User choice of signal/shield metal layers
- Shielded transmission line
  - “OUTLINE” “TRANS” device ID
- “M1 “TRANS” etc. will not prevent automatic metal fill
  - Process limits maximum width



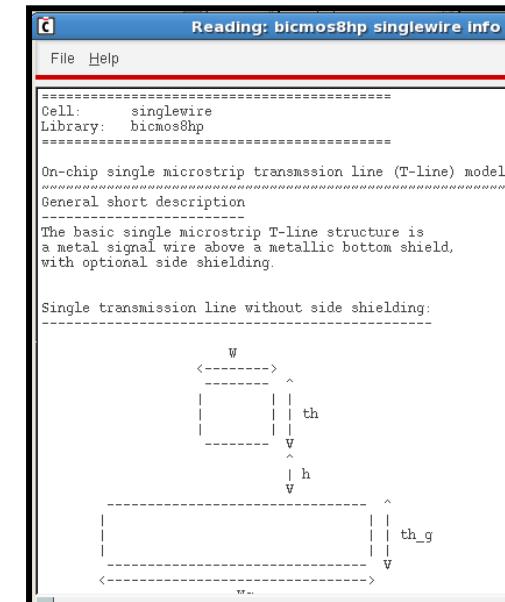
# Transmission Lines Properties Form (singlewire)

- Geometry/Metal Parameters
- Sets switch to include the effect of shield
- Include pattern fill in model?
- Displayed electrical characteristics parameters

*singlewire*

Info	
Bandwidth max [Hz]	200G Hz
length [m]	100.0u M
width [m]	4.0u M
side shielding	<input type="radio"/> on <input checked="" type="radio"/> off
Impedance calculator	<input type="radio"/> on <input checked="" type="radio"/> off
Wireopt	213
Signal layer	MA
Bottom shield layer	LY
Custom capacitance	<input type="radio"/> yes <input checked="" type="radio"/> no
Model pattern fill	<input checked="" type="radio"/> yes <input type="radio"/> no
Temperature Delta	0.0 C
max length [um]	180
Total Capacitance [F]	8.8845e-15
Total DC Resistance [Ohm]	0.158375
Total HF Inductance [H]	5.15482e-11

When “Info” button is depressed, singlewire information appears as a useful Design Aid



Dual Metal E1/MA Option Shown

# Transmission Lines Properties Form

**coupledwires**

Geometry/Metal Parameters

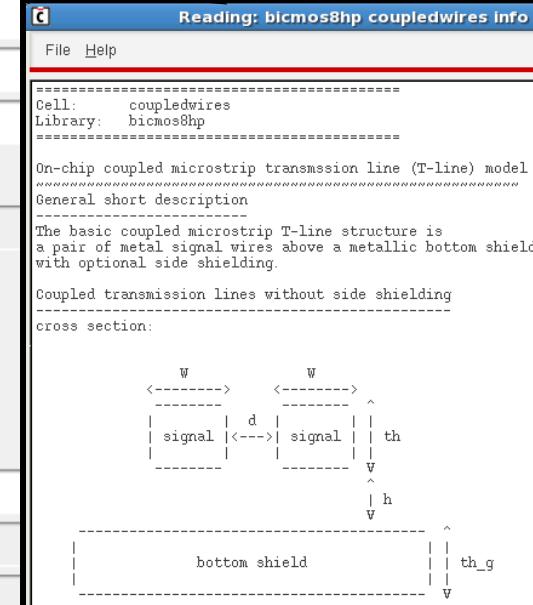
Displayed electrical characteristics parameters

Select Impedance Mode  
Odd, Even or Single

Dual Metal E1/MA Option Shown

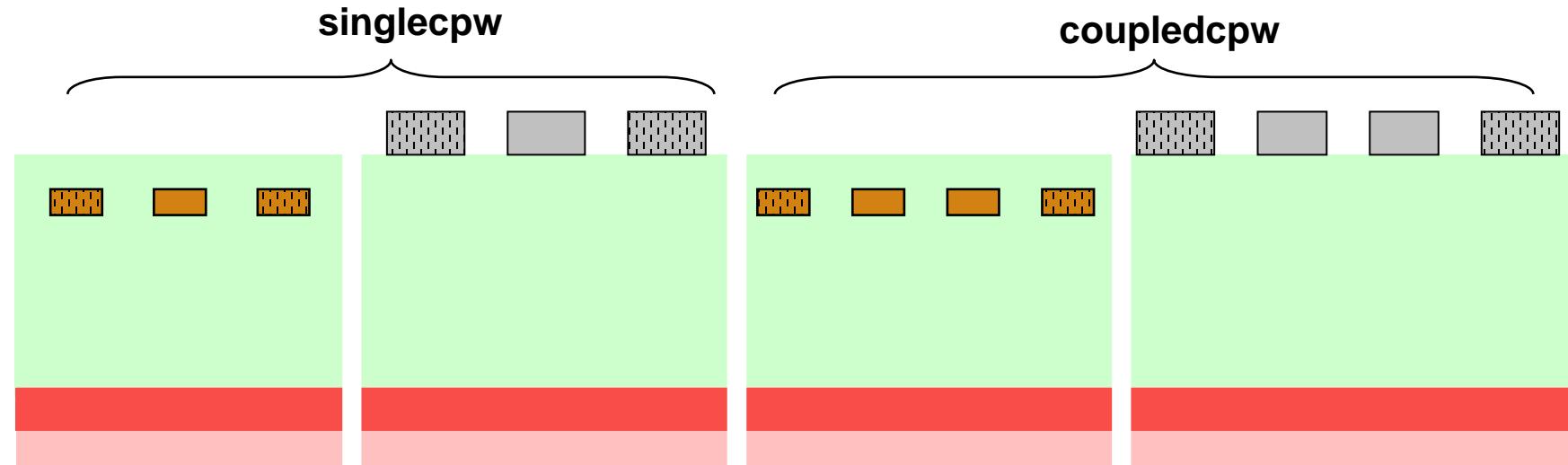
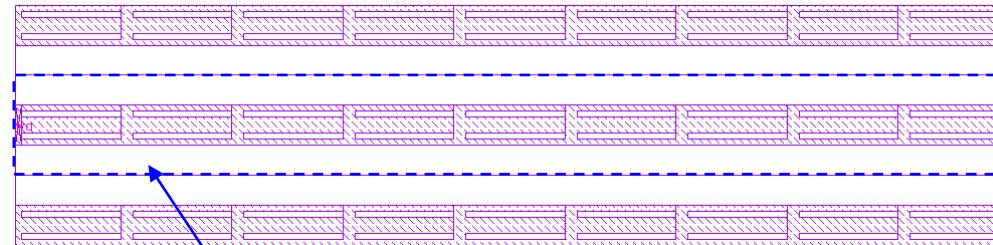
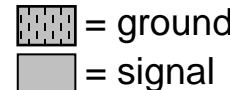
Info	
Bandwidth max [Hz]	200G Hz
length [m]	100.0u M
width [m]	4.0u M
distance [m]	10.0u M
side shielding	<input type="radio"/> on <input checked="" type="radio"/> off
Wireopt	213
Signal layer	MA
Bottom shield layer	LY
Custom capacitance	<input type="radio"/> yes <input checked="" type="radio"/> no
Model pattern fill	<input checked="" type="radio"/> yes <input type="radio"/> no
Temperature Delta	0.0 C
max length [um]	180
Total Capacitance [F]	6.67784e-15
Total Cross Capacitance [F]	3.49541e-15
Total DC Resistance [Ohm]	0.158375
Total HF Inductance [H]	5.10439e-11
Total LF Inductance [H]	5.83824e-11
Mutual HF Inductance [H]	1.75381e-11
Mutual LF Inductance [H]	1.72351e-11
Initial Frequency [Hz]	4.4328e+08
Time of flight [sec]	6.76742e-13
impedance mode	Odd
HF odd mode impedance [Ohm]	57.3892

When “Info” button is depressed,  
**coupledwires** information appears  
as a useful Design Aid



# Coplanar Waveguide (singlecpw, coupledcpw)

- Purpose: Critical wiring where defined ground planes are not possible
  - Clock distribution
  - Dense analog layout
- User choice of metal layer



# Coplanar Waveguide CDF Form (coupledcpw)

Geometry/Metal Parameters

Sets switch to include the effect of Crossing Lines in model?

Include pattern fill in model?

Displayed electrical characteristics parameters

Dual Metal E1/MA Option Shown

When T-line HELP button is depressed, waveguide Model Help Menu appears as a useful Design Aid

T-line HELP

Bandwidth max [GHz]	40
length [m]	100.0u M
width [m]	4.0u M
distance [m]	6.0u M
s [m]	6.0u M
Wireopt	213
Signal layer	MA
Crossing Lines Model	<input checked="" type="radio"/> full plane <input type="radio"/> custom
Full Plane	<input checked="" type="radio"/> none <input type="radio"/> above <input type="radio"/> below
Pattern Fill	<input checked="" type="radio"/> yes <input type="radio"/> no
Temperature	25
max length [um]	900
Total LF Capacitance [F]	8.83333e-15
Total LF Cross Capacitance [F]	5.30238e-15
Total DC Resistance [Ohm]	0.2625
Total LF Inductance [H]	5.4494e-11
Mutual LF Inductance [H]	2.00863e-11

Reading: bicmos8hp coupledcpw info

\*\*\*\*\*  
\* On-chip coupled coplanar transmission line (T-line) model  
\*\*\*\*\*

Technology: BiCMOS8HP  
Design Manual version: BiCMOS8HP ES #70P3264 EC# J93676, 00  
Simulators supported: spectre, hspiceS

\*\*\*\*\*  
\* General short description \*  
\*\*\*\*\*

The basic coupled coplanar T-Line structure is two metal signal wires of the width W between two coplanar of the width Ws = W (return path wires), above the silicon All metal levels are supported for the coplanar lines usage

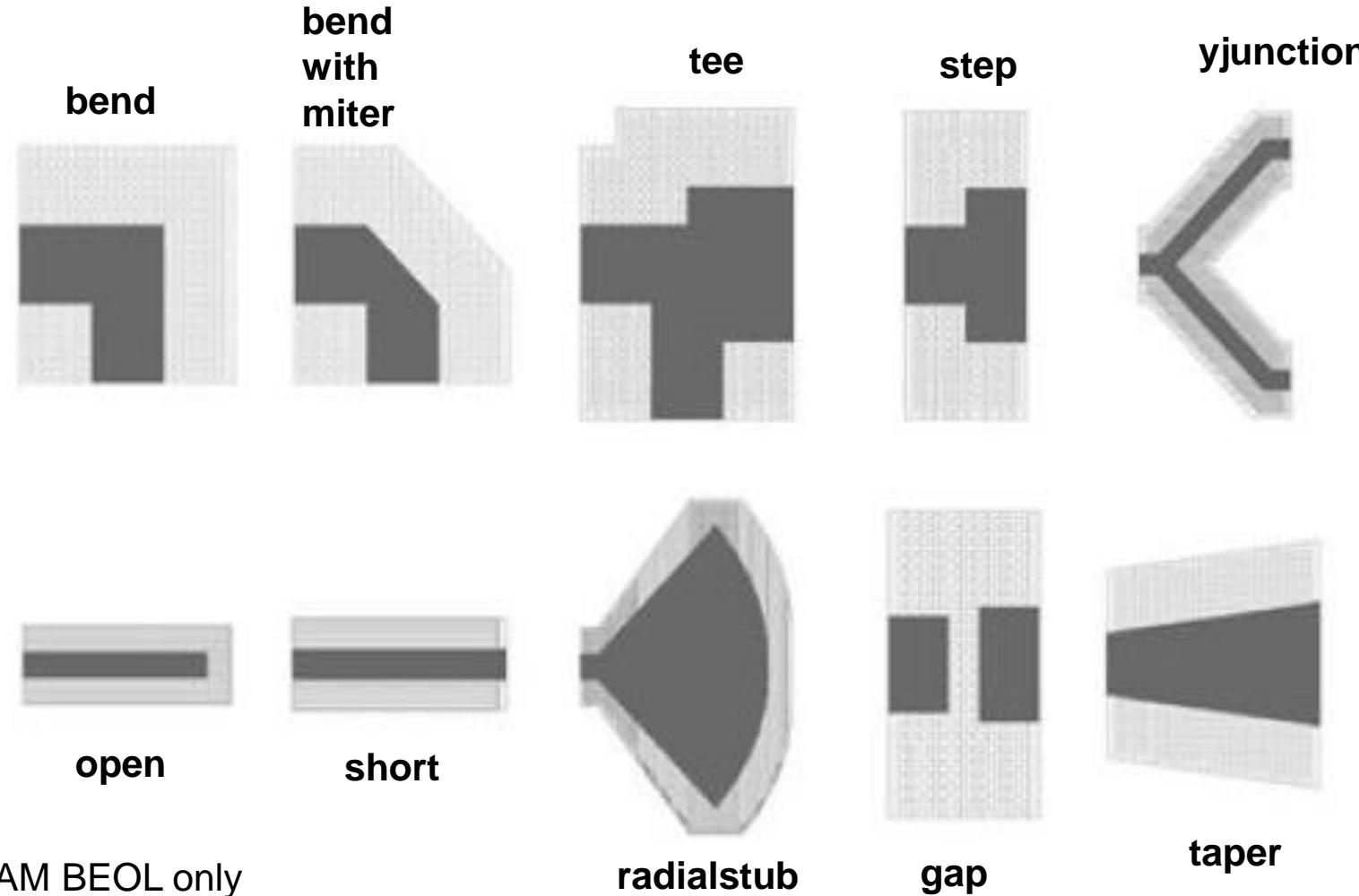
Coupled coplanar T-line cross section  
=====

W<sub>s</sub>      W      W      W<sub>s</sub>  
<----> <----> <----> <---->  
Return	s	d	s	Return						
path	<-->	Signal	<-->	Signal	<-->	path				
----- ----- ----- -----

\*\*\*\*\*  
\* Cross section description \*  
\*\*\*\*\*

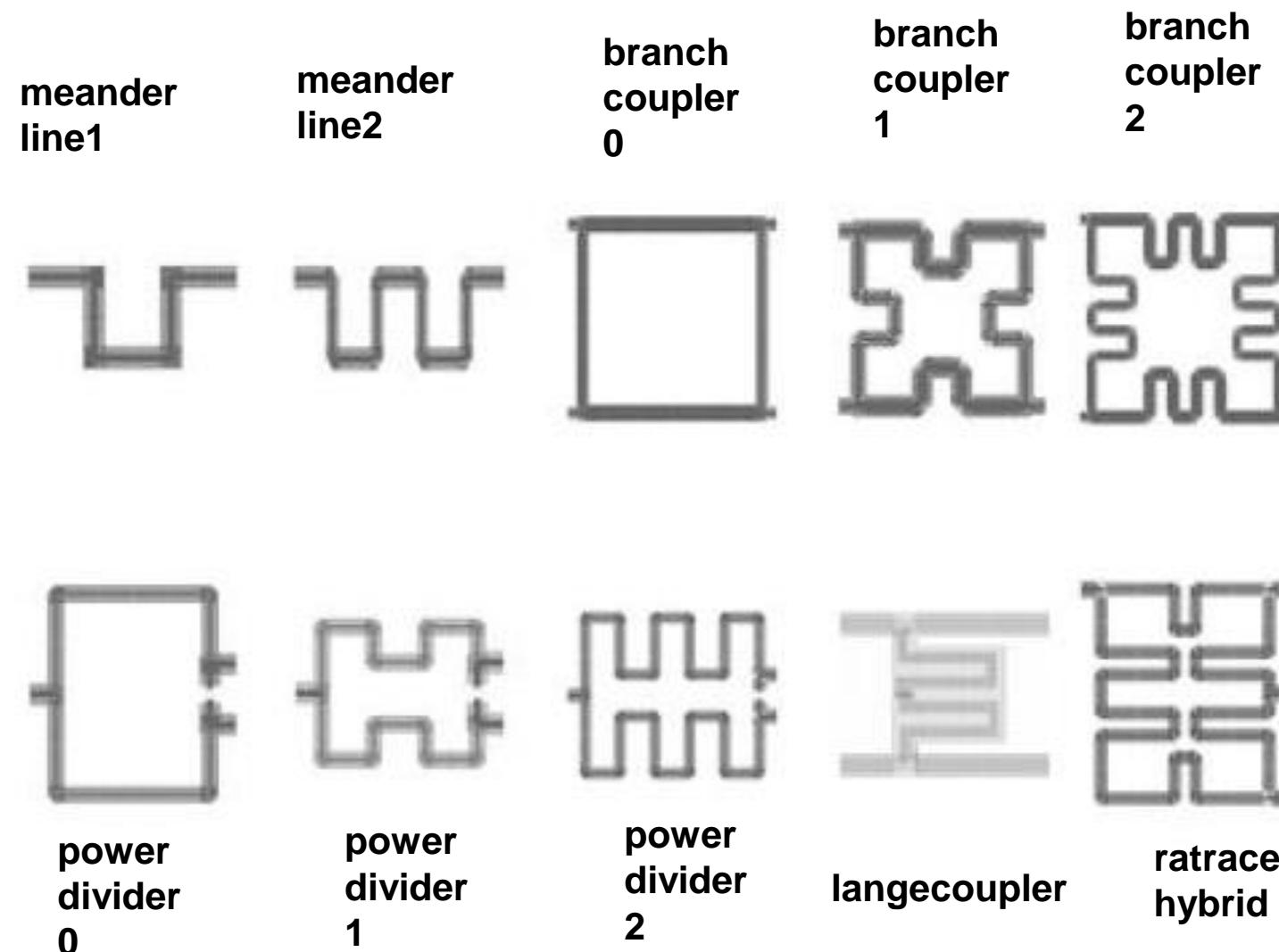
# Microwave/Millimeter Wave Passive Elements\* (1)

Unique distributed passives characterized for Millimeter wave circuits



\*AM BEOL only

# Microwave/Millimeter Wave Passive Elements\* (2)



\*AM BEOL only

# Distributed Passive Devices Modeling

## Modeling Features:

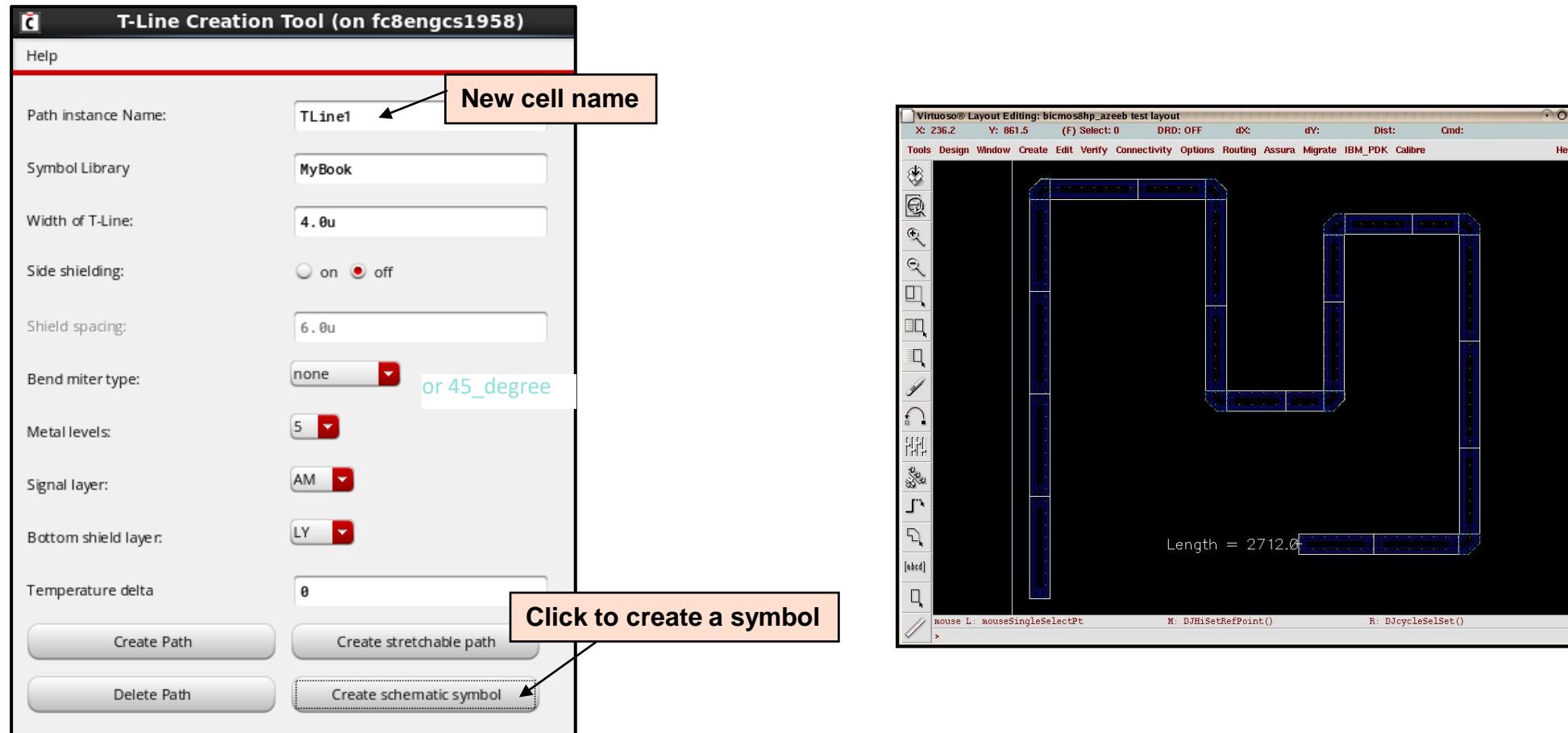
- Kit supports multiple distributed passive models each supporting several metal combinations for signal and return paths.
- All the models are designed for microstrip configuration although side-shields option is available for most of the devices.
- Large metal planes such as shields and low impedance lines on copper layer in the layout PCell are cheesed or slotted within the guidelines set by manufacturing.
- The design methodology provides accurate control of the characteristic impedance ( $Z_0$ ) and also isolates the signal line from silicon substrate.
- The supported distributed passive devices are designed to cover a bandwidth of DC till 120GHz.
- The models have been verified using full-wave EM solvers up to 120GHz and using VNA measurement up to 110GHz.

**See Section 4.26 in the Design Manual and Section 23 in Model Reference Guide for additional details**

# PDK Utility for Custom T-Line Creation & Simulation

To help create the arbitrary T line shape as an interconnect to fit into the existing space

- In layout window, under **PDK menu → Misc → Create T-Line Path**
- Draw the interconnect with a new cell name and it will generate symbol for simulations in the schematic.



# Electronic Fuse (efuse)

- **Silicided p+ polysilicon**

- No additional masks/processing

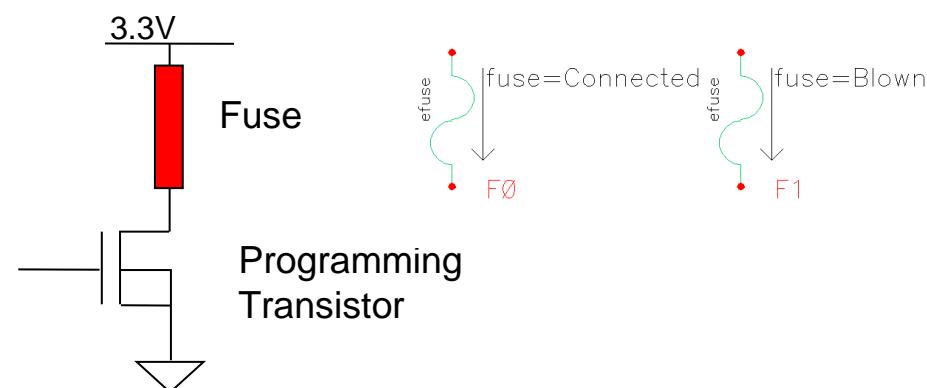
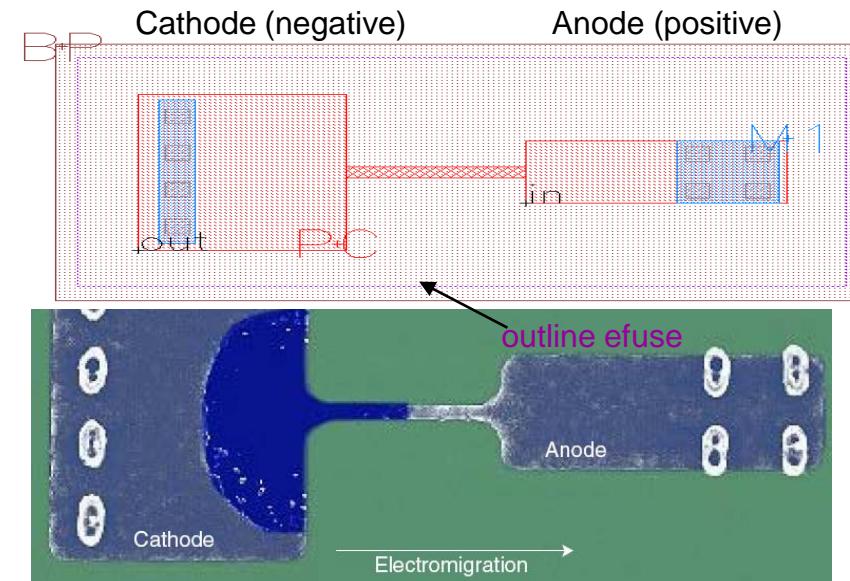
- **Programming**

- FET-switched current pulse (10-13.5 mA, 0.18ms-1ms)
  - Fuse mechanism - electromigration of silicide and boron depletion increases the resistance of the fuse link
  - Unprogrammed resistance  $50 < R < 130 \Omega$
  - Programmed resistance  $> 5 K\Omega$
  - Programming at wafer or package level

- **Applications**

- Programming memory array redundancy
  - Chip ID
  - Chip configuration

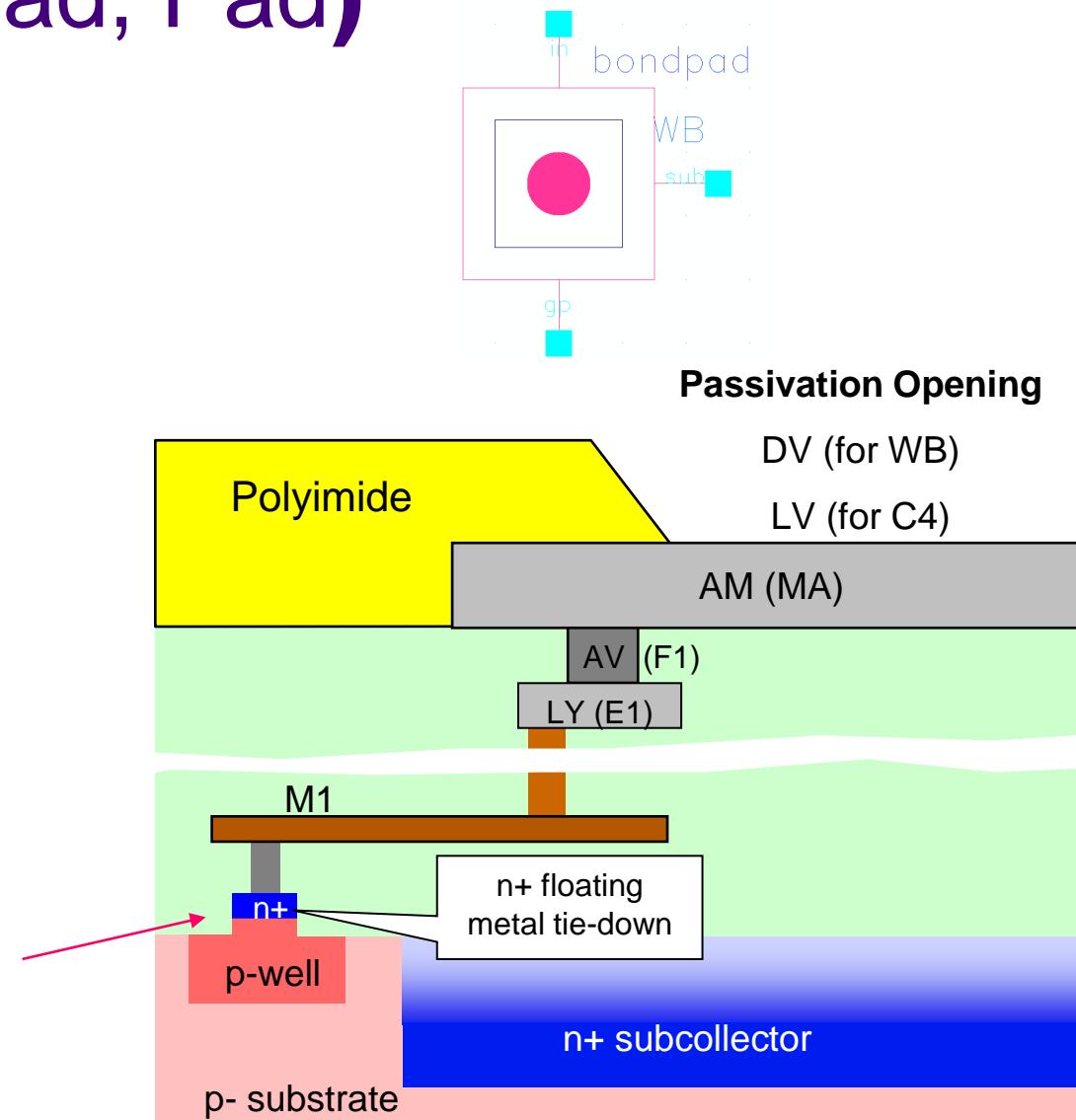
In simulation, parameter pblow=0 means “connected” and highest un-programmed resistance is used. pblow=1 corresponds to “blown” and lowest programmed resistance is used.



# Terminal Pad (bondpad, Pad)

- **bondpad**
  - Ground Planes : NS or M1 or BB
- **Pad** layout pcell for non-critical applications, allow some devices under the pad
  - Extracts as parasitic, not device
- **Wirebond**
  - 73  $\mu\text{m}$  minimum pitch\*
- **C4 (flip chip solder bump or copper pillar)**
  - C4 "size on pitch", in mils
  - "4 on 8", "4 on 9" & "5 on 10" available
  - Most devices allowed underneath except inductors and transmission lines and logo
- **Floating Metal Check**
  - Requires pad connection to diffusion to avoid process charging damage

\*Pitch depends on test and packaging vendor. This pitch is for GLOBALFOUNDRIES test and packaging.



# bondpad Properties Form

NS, M1, BB

Dimensions of metal

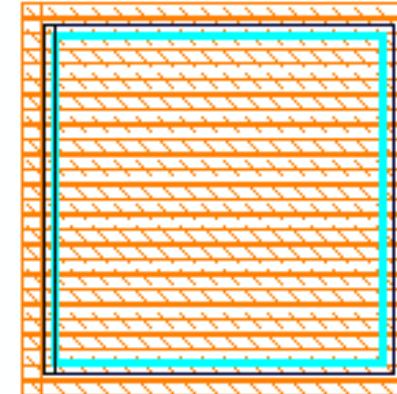
Wire bond or C4\*

M1 and row of contacts to ground plane

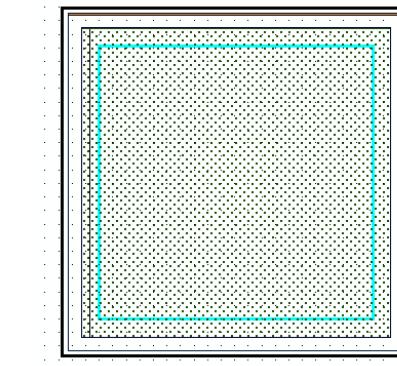
The screenshot shows the bondpad Properties Form with the following settings:

- Backplane: M1
- Length: 101.0u M
- Width: 101.0u M
- Type: WB
- Metal Shape: Rectangular or Octagonal
- Align Contacts to: length or width
- Wireopt: 411
- ESD label: FULL\_ESD or None HC\_POWER\_ESD LC\_POWER\_PAD CUSTOM\_ESD NO\_PROTECT\_HBM TEST\_PAD\_NOESD
- Subcircuit Name: bondpad

M1 Ground Plane



NS Ground Plane



\*Copper pillar designs require a marker shape CUPILLAR (PAD PILLAR), drawn exactly coincident with CHIPEDGE

# Structures and Devices Under Pads

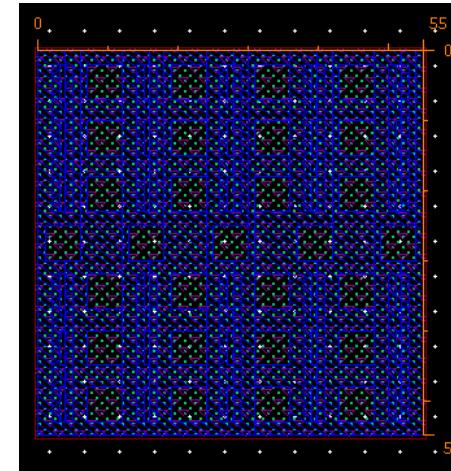
Terminal Type	bondpad (device)		Pad (not device)		
	Wire bond	C4	Wire bond	C4	
FETs, poly and diffusion resistors, mosvars, havar	No	No	Yes	Yes	
ESD diodes	No	No	Yes	Yes	
Efuse	No	No	No	Yes	
KQ Resistor	No	No	No	Yes	
TSV (through silicon via)	No	No	Yes	No <sup>1</sup>	
Thin M1-M2-M3-M4-MQ Metals	No	No	Yes	Yes	
Thick RF Metals: AM/LY, E1/LY/MA	No	No	Yes <sup>2</sup>	Yes	
Inductors, indline, transmission lines, SRAMs, VNCAP, LOGO	No	No	No	No	

<sup>1</sup>TSV and C4 are mutually exclusive

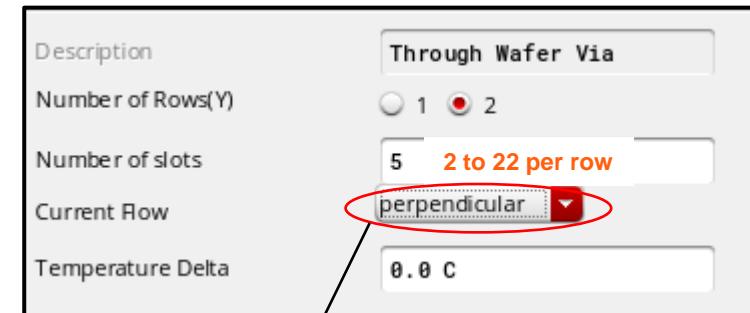
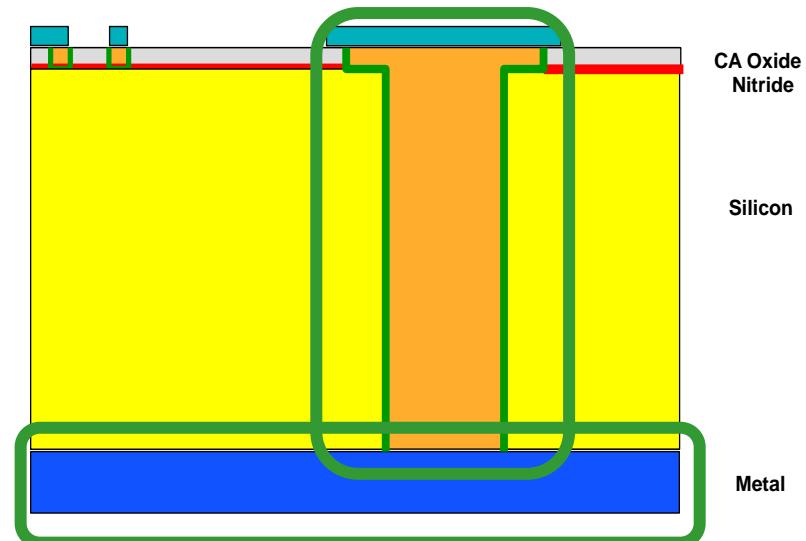
<sup>2</sup>E1 Rule restrictions apply

# Through Silicon Via (tsv2)

- Deep metal filled via with backside metallization
- Flexible TSV pcell design optimized for RF performance
- Model supports 100 um wafer thickness



5 Slot  
TSV2  
structure



access = identifies the direction of current flow to the slots, where

- 0: vertical to the slots from metal lines above M1
- 1: perpendicular to long edge of slots along M1 (default)
- 2: parallel to long edge of the slots along M1.

# Chip Pcell (chipguardring)

- Provides chipedge, crackstop, chip guard ring, logo and part number area
- Logo field with desired data
  - Use the alpha characters supplied in kit
  - Logo area does not receive pattern fill
- Rectangular or beveled edges
  - No data allowed in the beveled PROTECT areas
- Chip Origin ( $x=0, y=0$ ) must be at the lower left corner of the chip
- Maximum chip size
  - x: 20.00 mm
  - y: 20.00 mm
  - CHIPEDGE must be even multiples of 0.01  $\mu\text{m}$  and must be on grid.

## CDF Options:

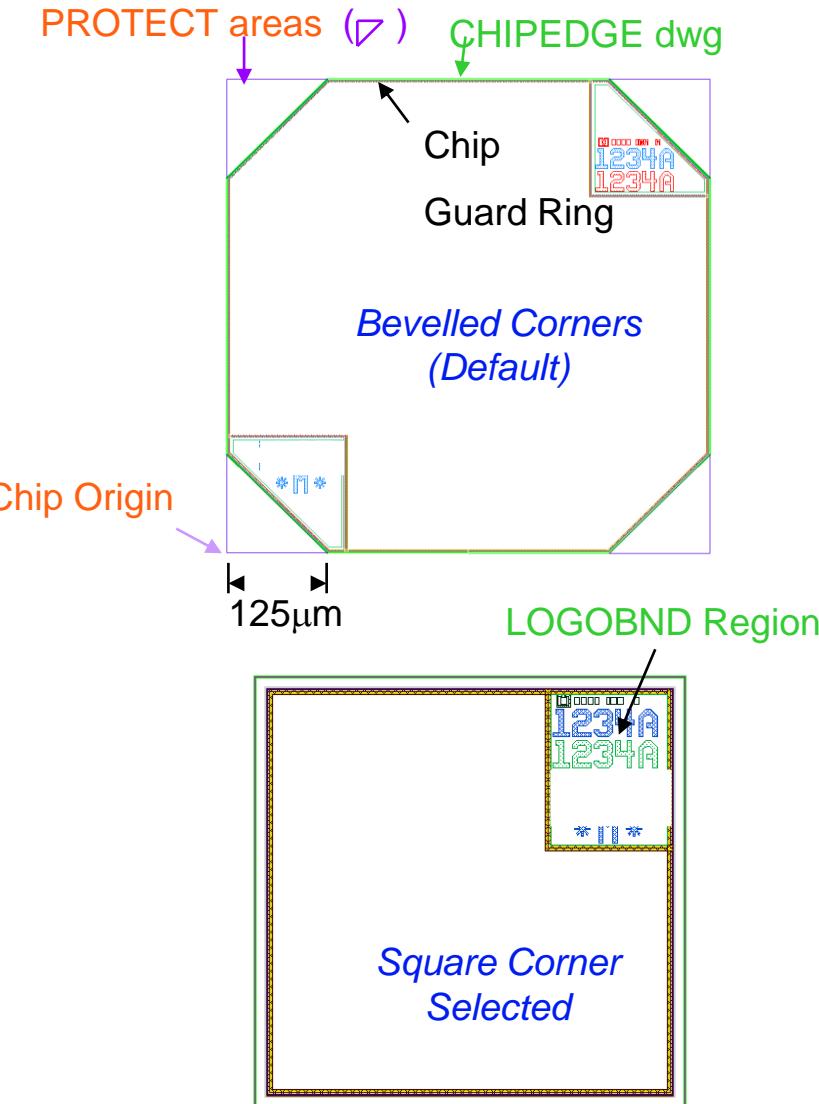
Length, Width

Square corner (Bevelled if unselected)

Remove Crackstop

Segmented

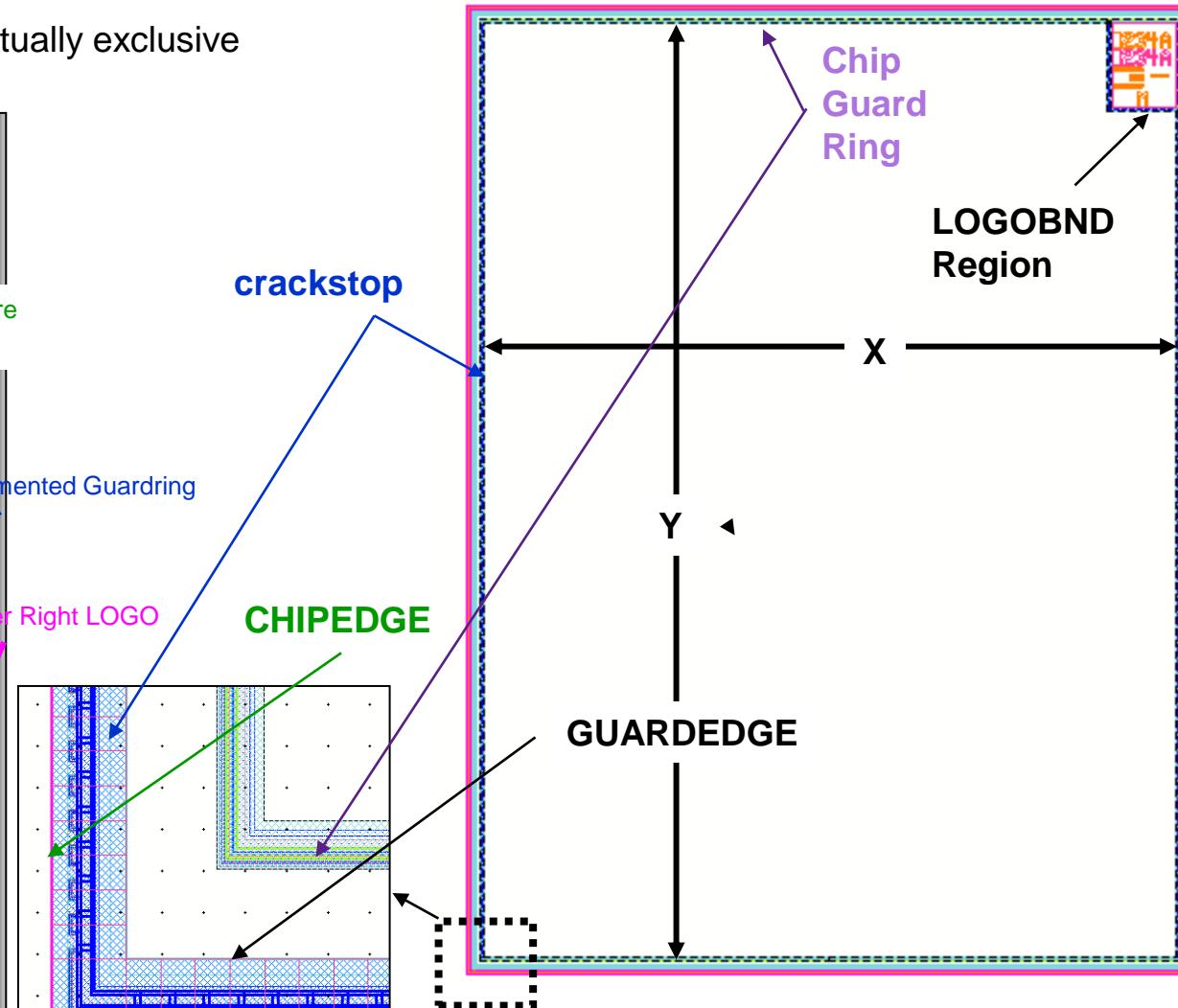
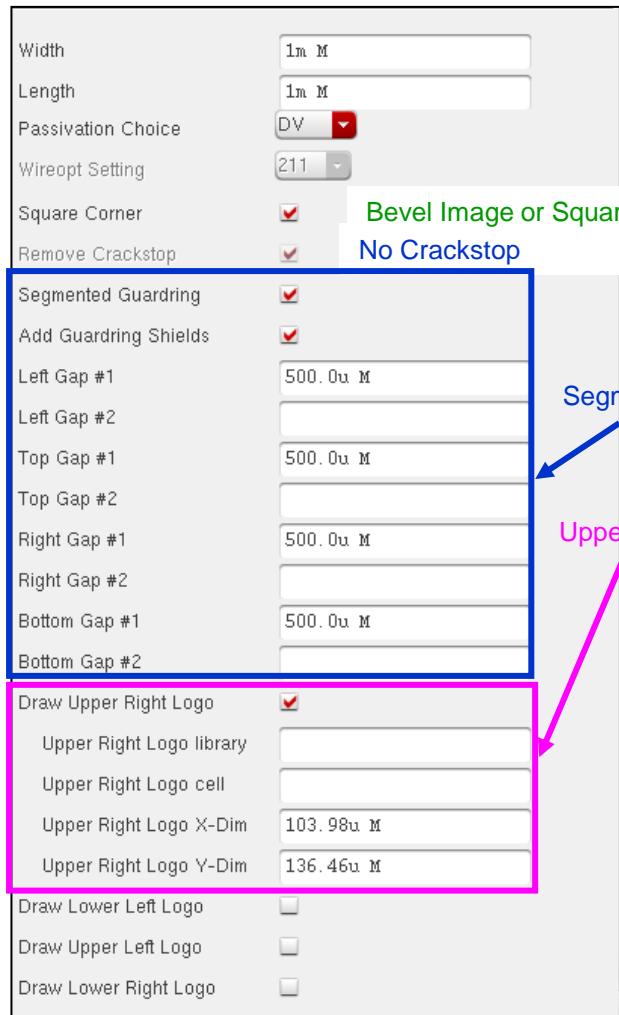
Add Custom Logo area



# Chipguardring Pcell (Layout only)

Shown with crackstop

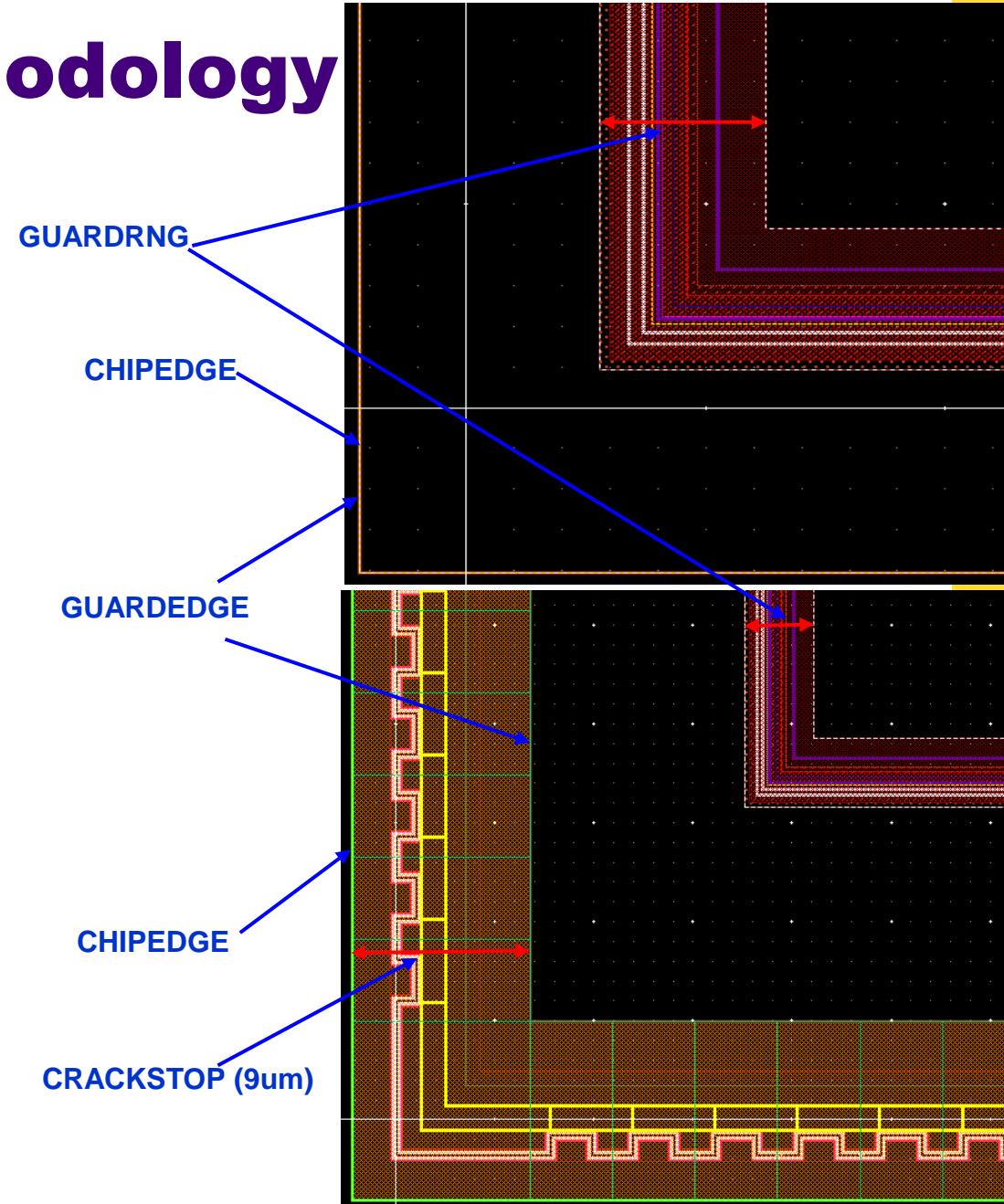
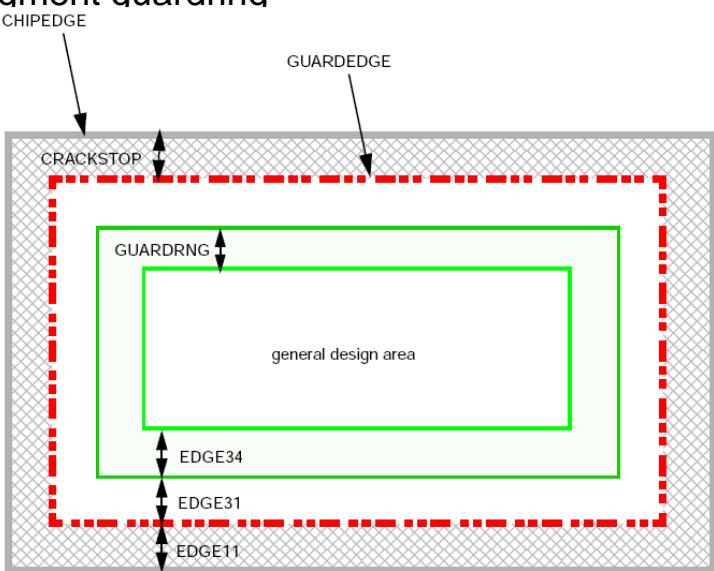
- Flexible pcell with or w/o crackstop
- Crackstop and Segmented Guardring are mutually exclusive
- Option to place custom LOGO



# Enhanced Crackstop Methodology

## Chipguardring P-cell

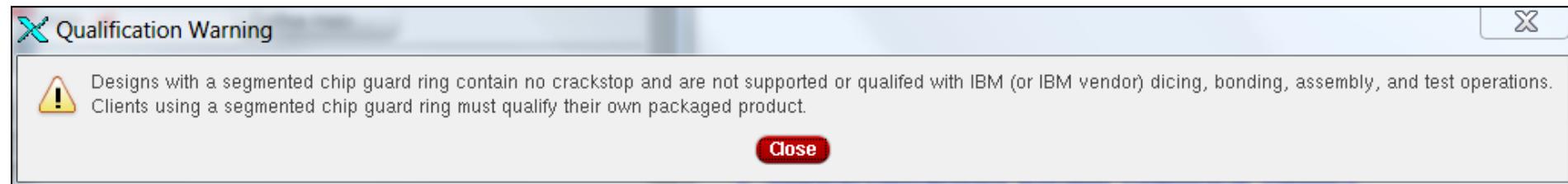
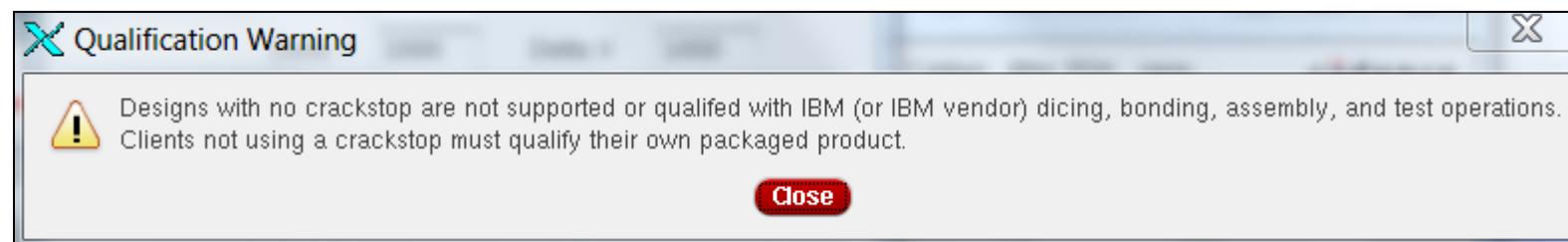
- “Chipguardring” p-cell contains:
  - CHIPEDGE
  - CRACKSTOP (optional)
  - GUARDEDGE
  - GUARDRNG
- “Chipguardring” p-cell parameters include:
  - Remove Crackstop
  - Segment guardring



# Remove Crackstop, Segment Guardring

- Clients are responsible for qualification of chips without Crackstop at their packaging vendor

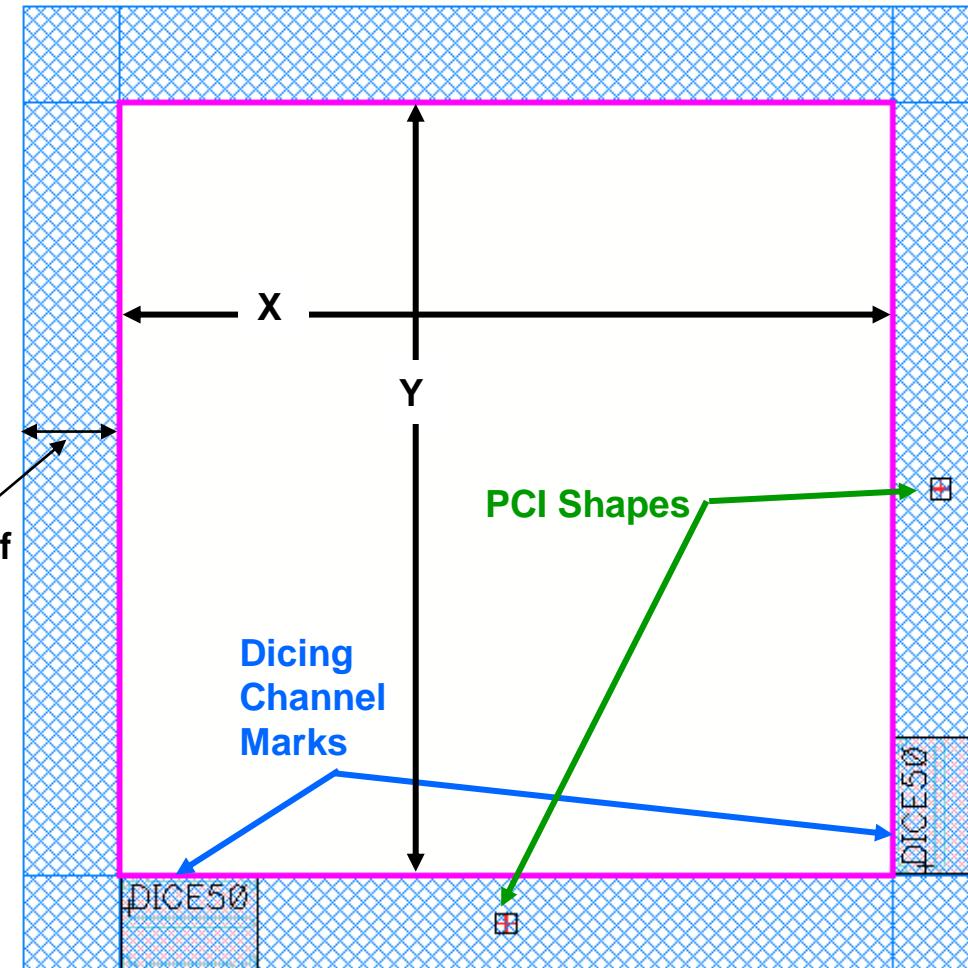
Remove Crackstop	<input checked="" type="checkbox"/>
Segmented Guardring	<input checked="" type="checkbox"/>
Add Guardring Shields	<input checked="" type="checkbox"/>
Left Gap #1	500.0u M
Left Gap #2	
Top Gap #1	500.0u M
Top Gap #2	
Right Gap #1	500.0u M
Right Gap #2	
Bottom Gap #1	500.0u M
Bottom Gap #2	



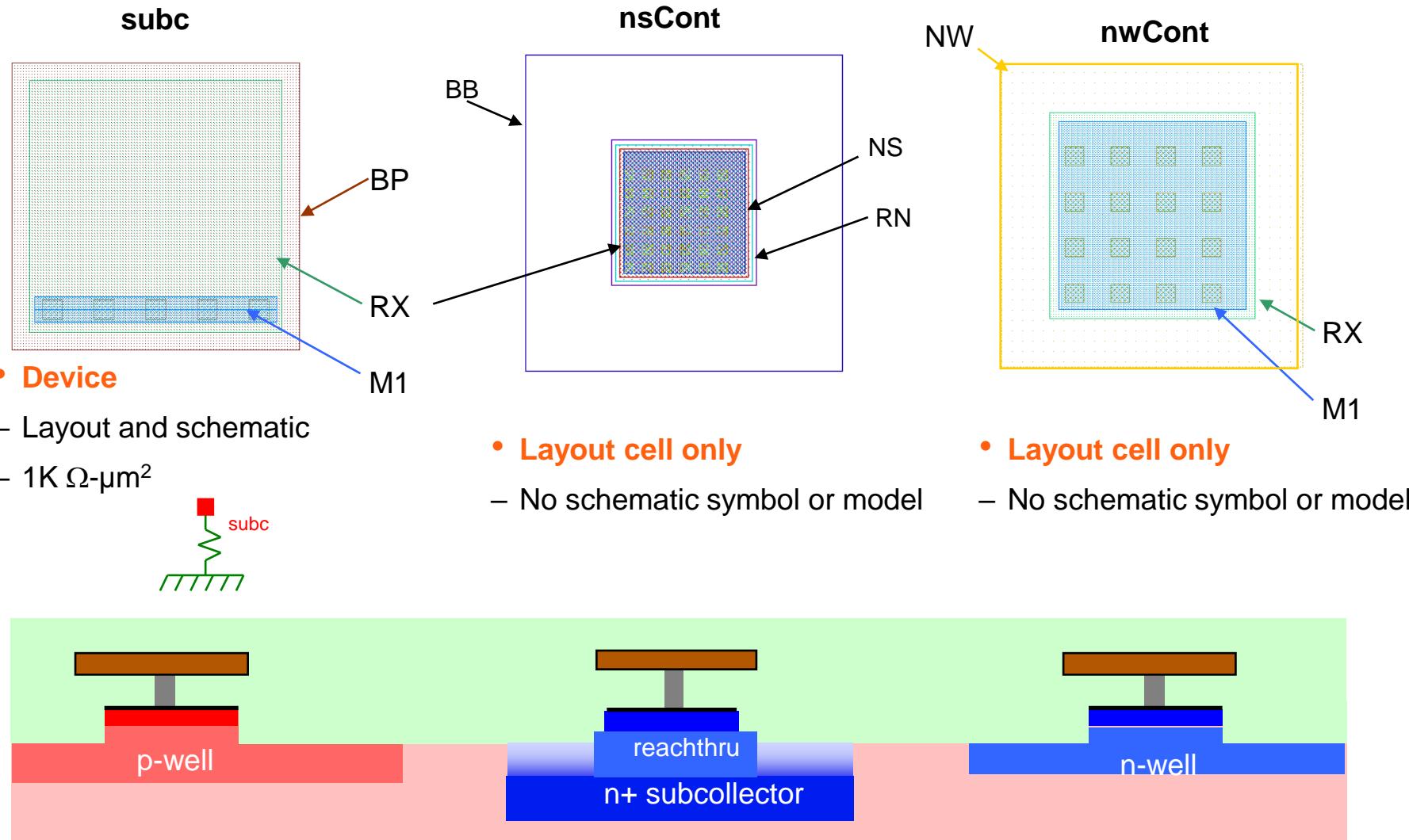
# dice\_channel

- For MPW use: PDK → Misc → Create MPW Matrix.
- Adds dicing channel around the chip.
- CDF Parameters include Dicing Channel Length, Width, Kerf Widths, Dice Mark and PCI

Width (X)	1m <input type="text"/>
Length (Y)	1m <input type="text"/>
Horizontal Kerf Width	50.0u <input type="text"/>
Vertical Kerf Width	50.0u <input type="text"/>
Wireopt setting	211 <input type="button"/>
Add Left Kerf	<input checked="" type="checkbox"/>
Add Right Kerf	<input checked="" type="checkbox"/>
Add Top Kerf	<input checked="" type="checkbox"/>
Add Bottom Kerf	<input checked="" type="checkbox"/>
Passivation Choice	DV <input type="button"/> LV or None
Dice Mark	<input checked="" type="checkbox"/>
PCI	<input checked="" type="checkbox"/>



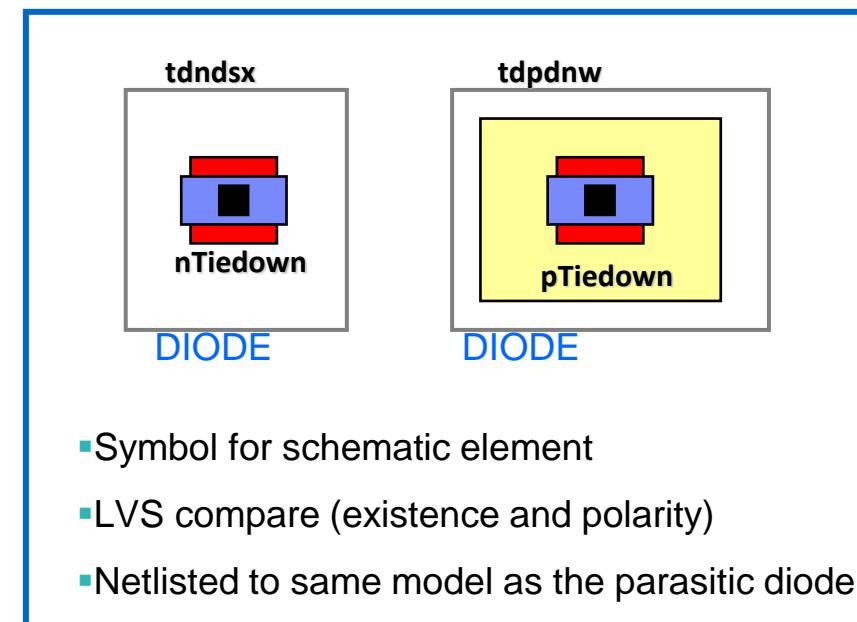
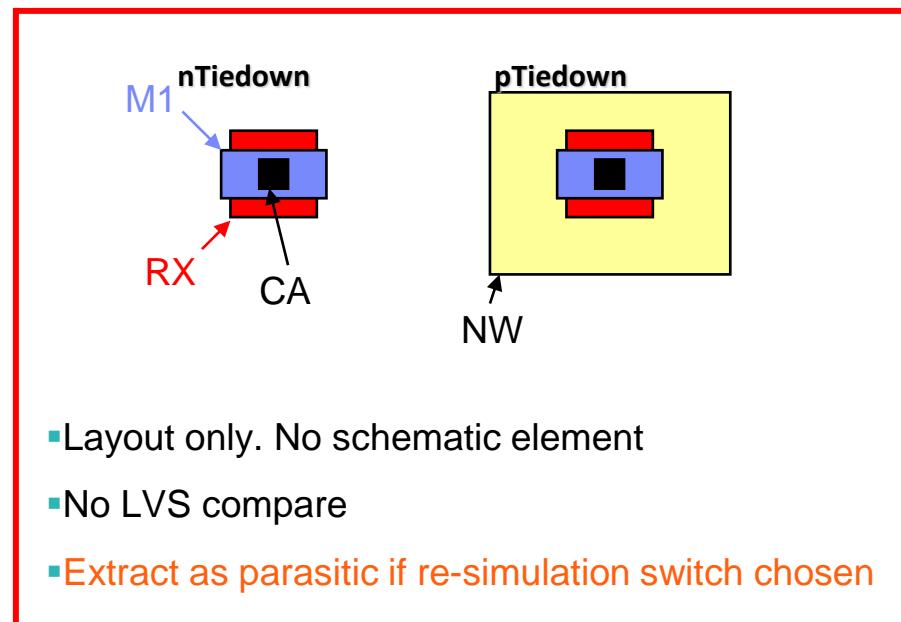
# Contact Pcells



# Tie-down Diodes (nTiedown, pTiedown)

## ▪ Tie-Down diodes

- Prevent in-process charge damage to gate oxide and MIM dielectric (Antenna Rules). Also required for nwell
- Option 1: Treat as parasitic elements
  - Use layout only cells nTiedown / pTiedown, extract as a parasitic diode for re-simulation from layout.
- Option 2: Treat as device enter in schematic and use in LVS comparison
  - Add “DIODE drawing” over cells nTiedown / pTiedown in layout.
  - Use symbol only cells tdndsx (n+ to pwell) / tdpdnw (p+ to nwell) in schematic



# Parasitic Diodes

- Not for use in schematic design
  - Generated by extraction tools
- No layout p-cells, ignored for LVS

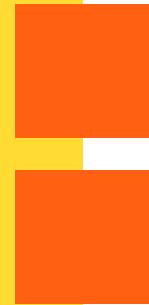
`diodenwsx` – n-well to substrate

`diodenx` – n<sup>+</sup> to substrate

`diodepnw` – p<sup>+</sup> diffusion to n-well

`diodepisx` – PI or T3 (n-buried layer of triple well NFET) to substrate

`diodepwpi` – p-well to PI or T3 buried-layer



# ESD Library

# ESD Library

- **esd8hp cdslib** is in addition to the **bicmos8hp/bicmos8xp cdslib**
- **esd8hp Library Elements**
  - Primitive/Standalone ESD pcells
  - Macro pcells
- **ESD Reference Guide**
  - ESD Ref Guide in conjunction with esd8hp library suitable as ESD Design kit
- **High Current ESD simulation**
  - High Current ESD Device Models
  - ESD High Current Simulation
- **ESD Design Review**
- **Layout Based Circuit level ESD Checks Tool Calibre PERC\_LDL**
  - An ESD layout verification tool
- **ESD BEOL Parameters**
  - Tables in design manual

# BiCMOS8HP ESD Reference Guide

- **ESD Reference Guide includes all aspects of ESD design:**
  - ESD Phenomena and Test Methods
  - ESD Protection Strategy Background
  - ESD Device Physics
  - ESD Design Kit Description
  - ESD Design Kit Data
  - ESD Compact Models
  - ESD Ground Rule Descriptions and Checking
  - ESD Design Review\*
  - ESD Design Guidelines
- Other ESD information can also be found in the following sources:**

- Design Manual
- Model Reference Guide
- cdslib User's Guide

130HPSIGE-8HP ESD Reference Guide

[130HPSIGE-8HP ESD Reference Guide](#)

Date: 07/17/20

DocumentHistory:

Design Manual	Reference Date	ESD Design Kit Version	ESD Reference Guide Date
PLM# DM-000418	07/17/20	V1.8_5.0	07/17/2020

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GLOBALFOUNDRIES Confidential Page 1 of 253

\*Contact [fdrytech@globalfoundries.com](mailto:fdrytech@globalfoundries.com)

# esd8hp Device Library

- **HBM and CDM ESD Protection Devices**

- **Standard dual well and T3 isolation well SINGLE Diodes**

- n+/pwell: esdnndsx (DW) ... for signal to ground protection
    - p+/nwell: esdvppnp, esdvppnp\_t3 (DW, T3) ... for signal to Vdd protection
    - n+/pwell: esdvppnpn (T3) ... for protection at various potentials

- **Standard dual well and T3 Isolation well MULTIPLE Diode strings**

- double\_diode\_n (DW/T3) ... for IO pads
    - antiparallel\_diodes (DW/T3) ... for power-to-power or ground-to-ground rails.
    - esdvppnp\_strings (DW) ... diode strings in dual well
    - esdvppnpn\_string (T3) ... diode strings in triple well

- **Standard dual well or T3 Isolation well ESD NFETs:** esdnfet ... for signal to Vss protection

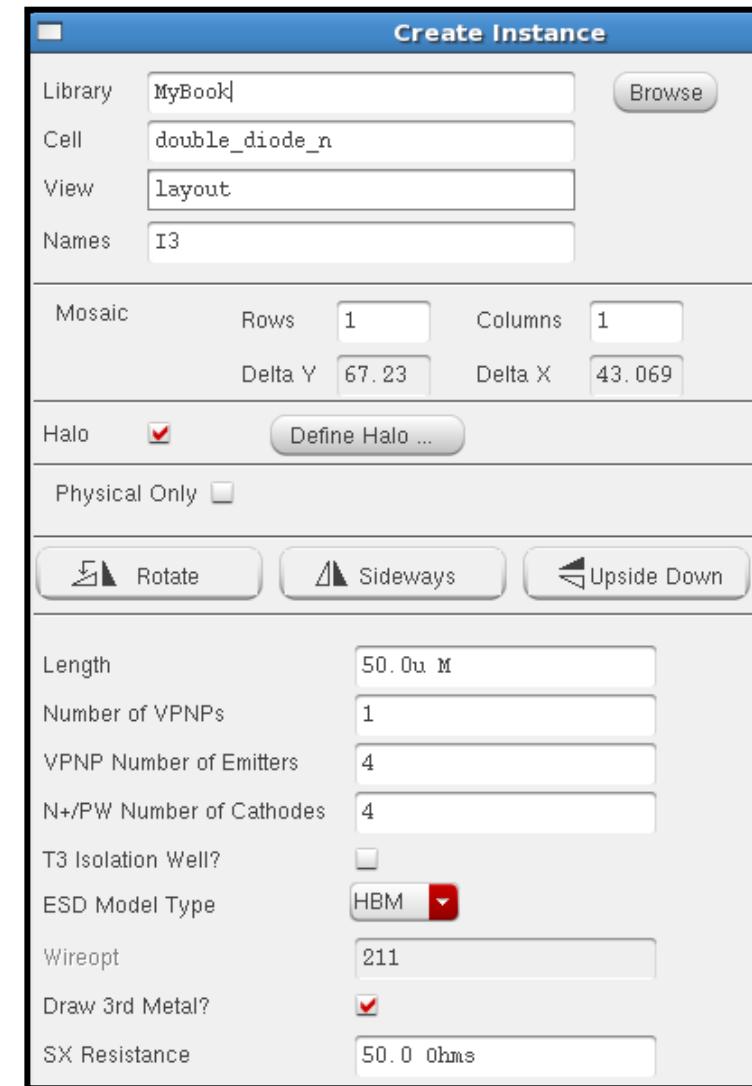
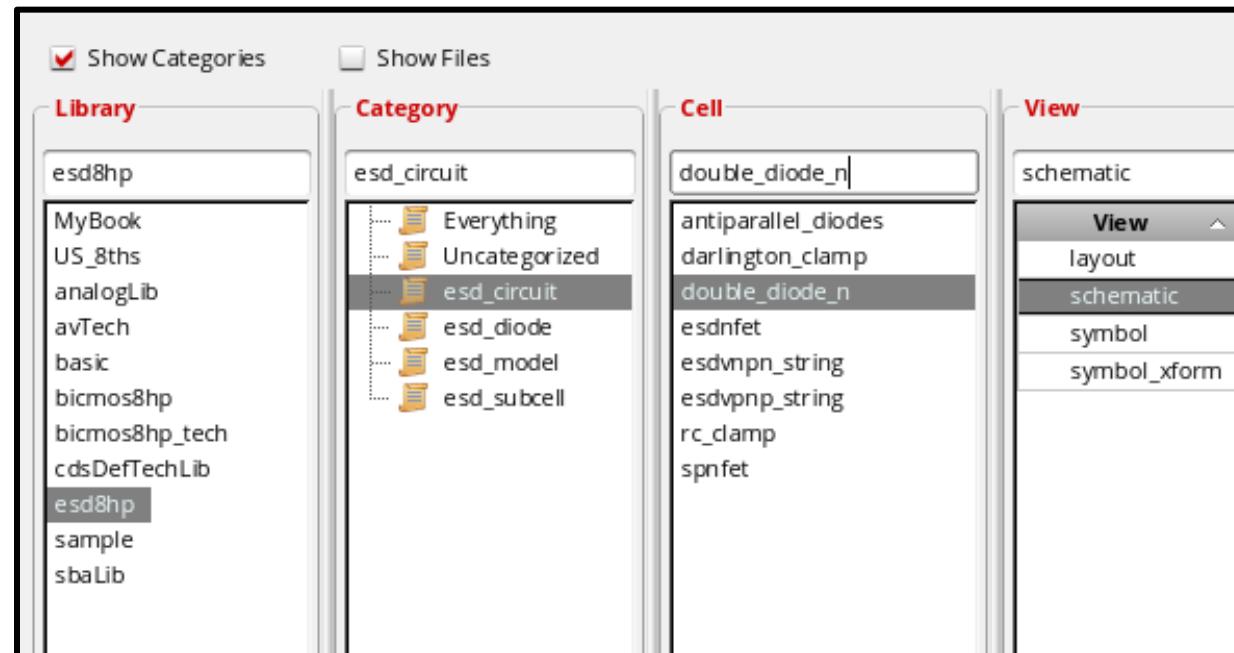
- **Standard dual well or T3 Isolation well Self-protected NFETs:** spnfet ...for output drivers

- **RC-Triggered Power Supply Clamps :** rc\_clamp ... for 1.2V or 2.5V or 3.3V power pads

- **Voltage Triggered Bipolar Darlington Clamp:** darlington\_clamp... for 2V or 3.6V power pads

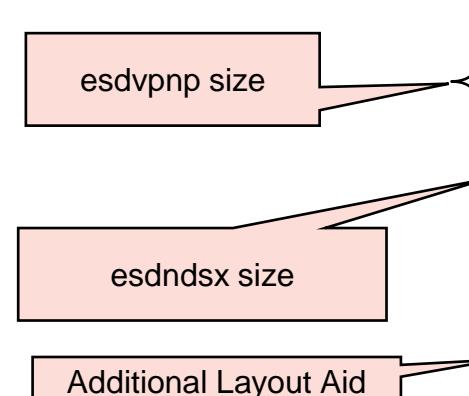
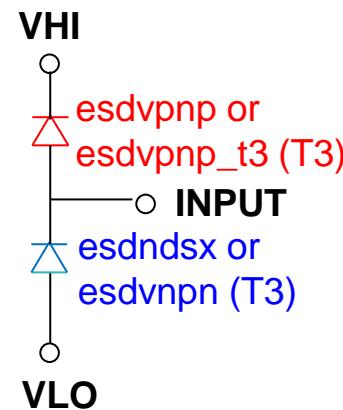
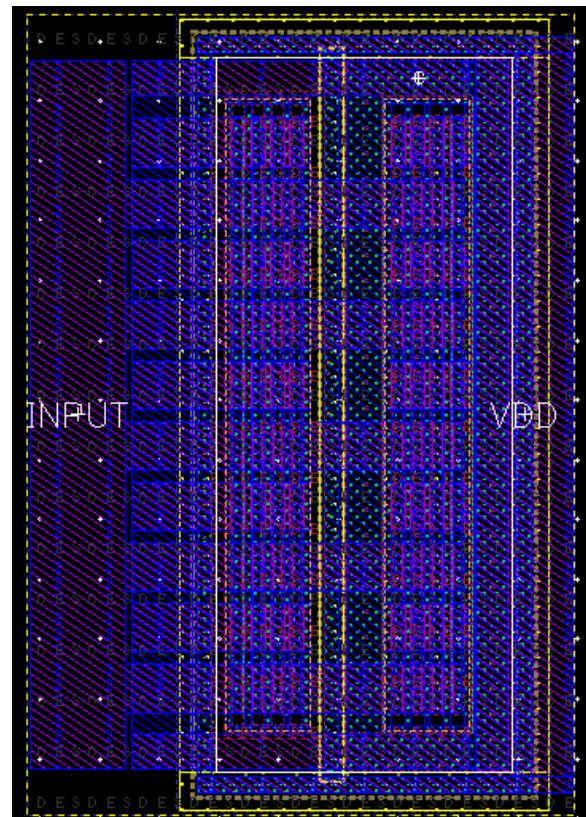
# ESD Hierarchical Circuits Direct Instantiation

- Hierarchical ESD devices can be placed directly in the design as instances, rather than created as fixed schematic sub-circuits in the design library.
- Parameters of existing instances can be modified without regeneration of a subcell.
- For designs with old version PDK
  - ESD library has been upgraded to skill-based symbols, schematics and layout.
  - Eliminate the need for the ESD Hierarchical Utility (PDK ESD Skill Utility).
  - Existing designs not impacted.



# Double Diode Macro (double\_diode\_n)

- Standard Dual Well or T3 Isolation Well Double Diode strings for IO pads
- T3 provides lower leakage
- Maybe placed under wire bond pads



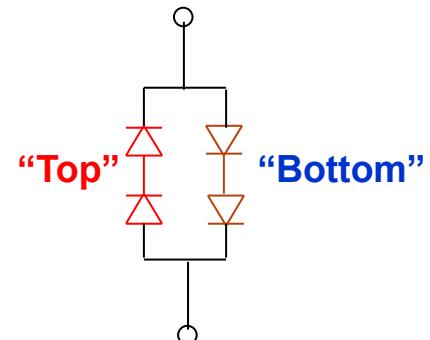
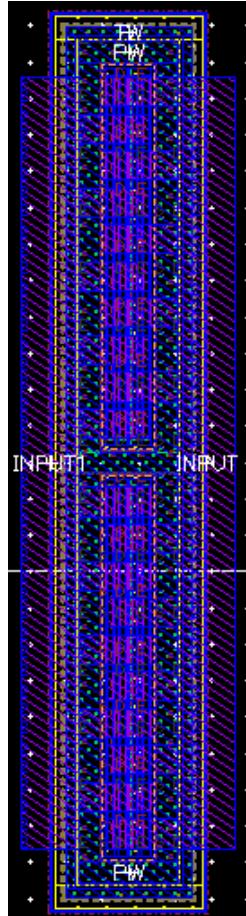
**double\_diode\_n (T3)**

Create Instance

Library	MyBook	Browse
Cell	double_diode_n	
View	layout	
Names	I1	
Mosaic	Rows 1	Columns 1
	Delta Y 67.23	Delta X 43.069
Halo	<input checked="" type="checkbox"/> Define Halo ...	
Physical Only	<input type="checkbox"/>	
Buttons: Rotate, Sideways, Upside Down		
Length	50.0u M	
Number of VPNPs	1	
VPNP Number of Emitters	4	
N+/PW Number of Cathodes	4	
T3 Isolation Well?	<input checked="" type="checkbox"/> DW or T3	
ESD Model Type	HBM <input checked="" type="radio"/> HBM or CDM	
Wireopt	211	
Draw 3rd Metal?	<input checked="" type="checkbox"/>	
SX Resistance	50.0 Ohms	

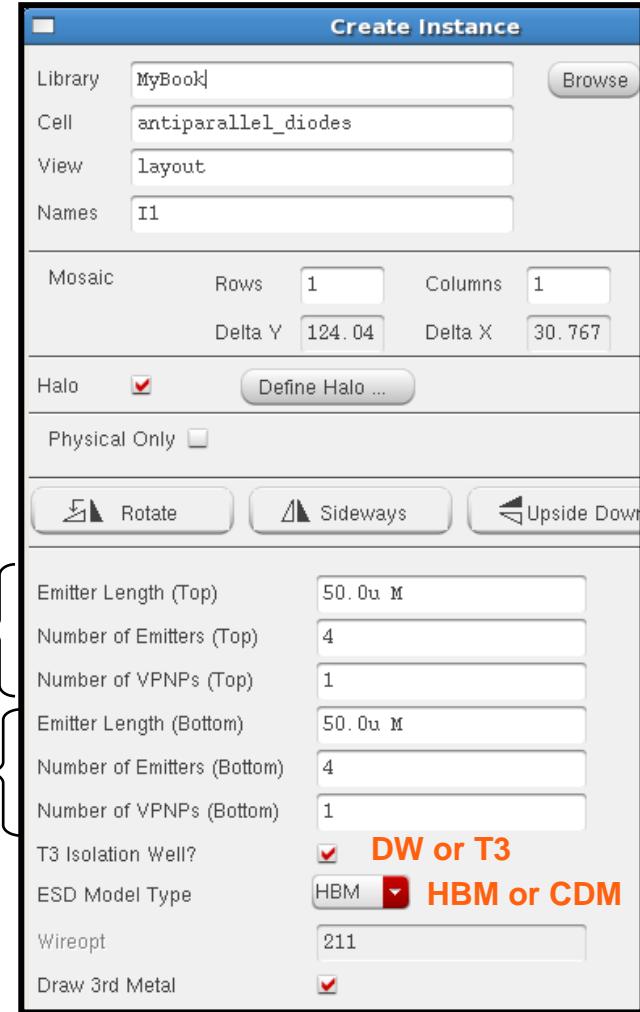
# Anti-parallel Diode Macro (antiparallel\_diodes)

- ESD diodes for power-to-power/ground-to-ground rails
- Standard Dual Well or T3. T3 provides lower leakage.
- May be placed under wire bond pads



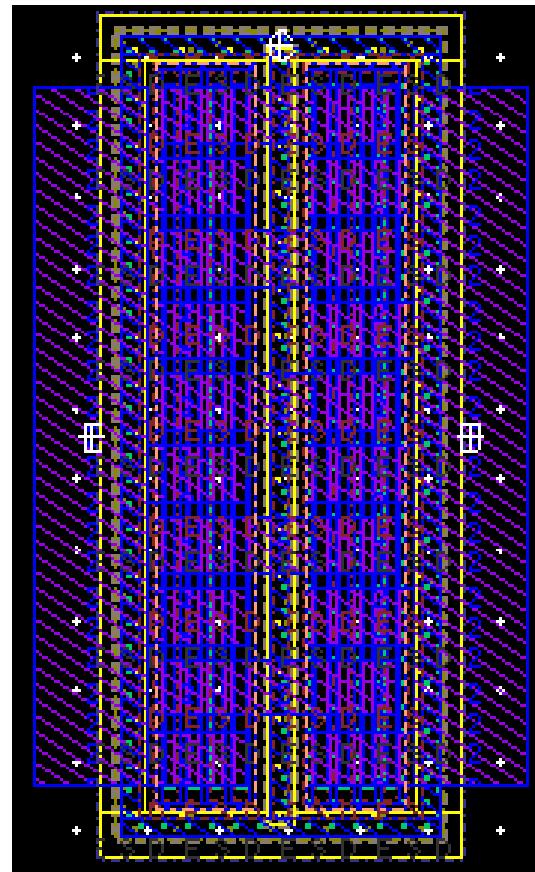
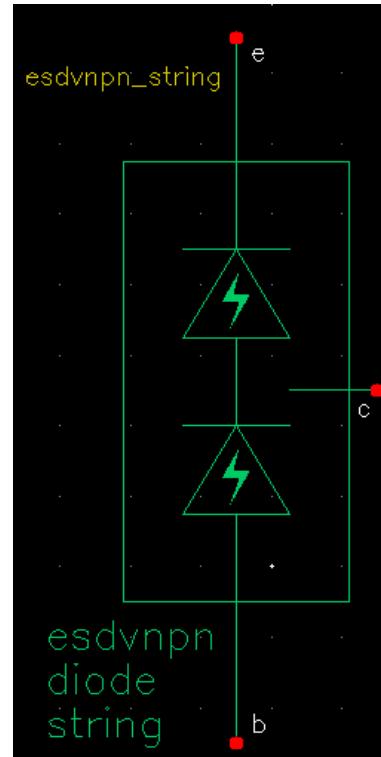
utilizes esdvpnp or esdvpnp\_t3 (T3)

antiparallel\_diodes

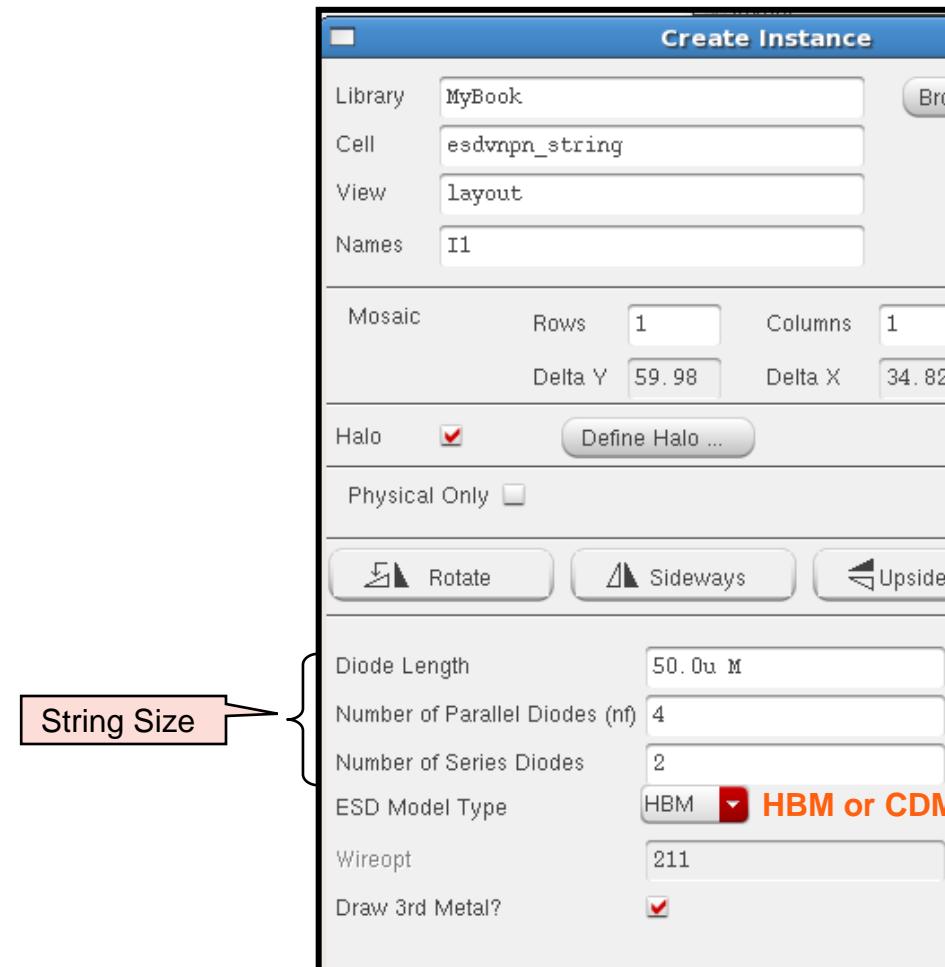


# N+/PW Diodes String in T3 Macro (esdvnpn\_string)

- N+/PW (esdvnpn) diodes string in T3
- Use to create a string of N+/PW (esdvnpn) diodes for negative ground applications

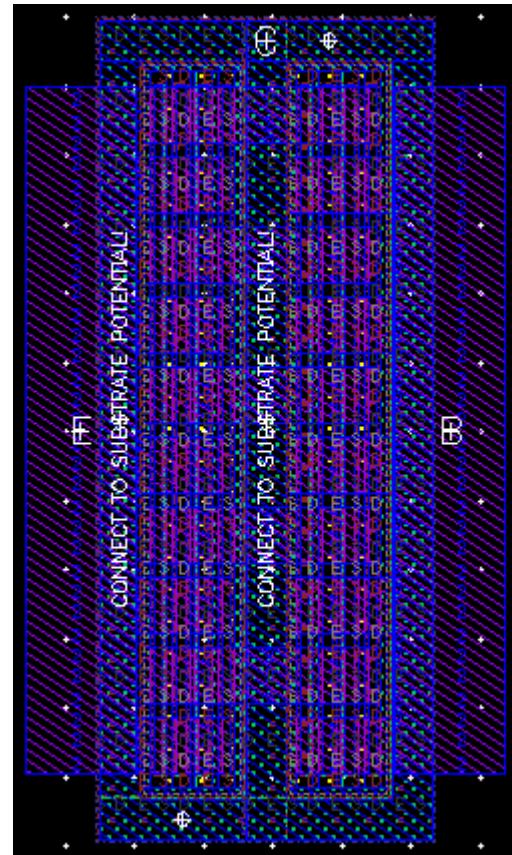
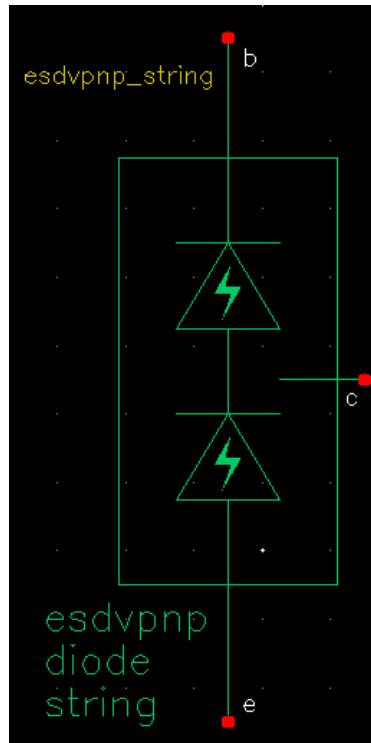


esdvnpn\_string

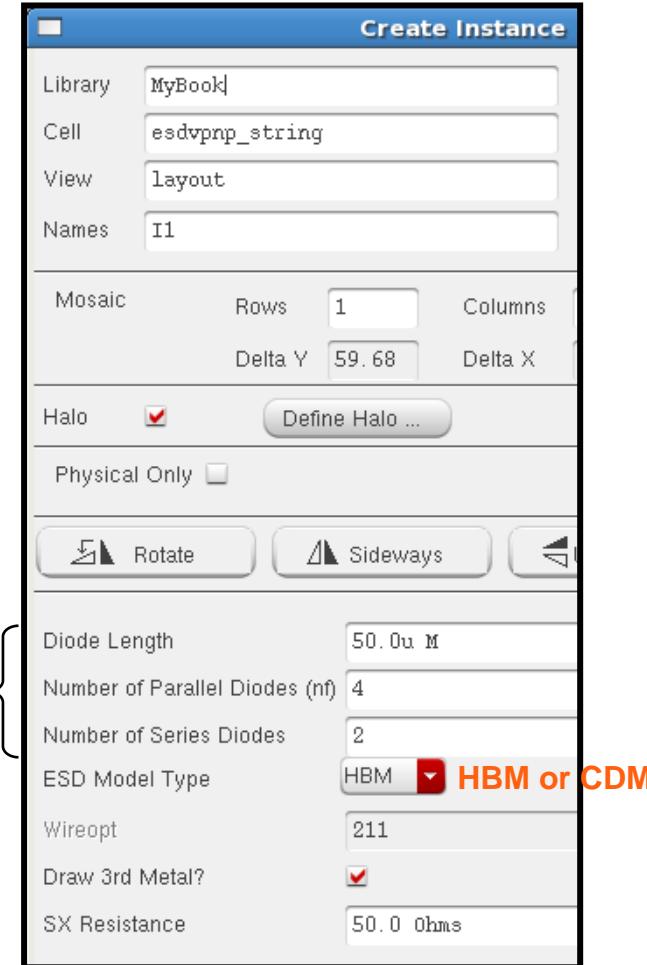


# P+/NW Diodes String Macro (esdvpnp\_string)

- P+/NW diodes (esdvpnp) string in standard Dual well

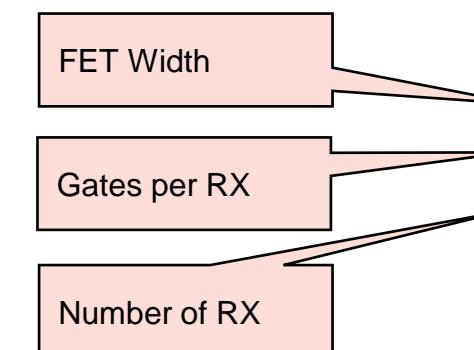
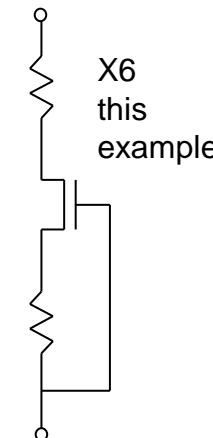
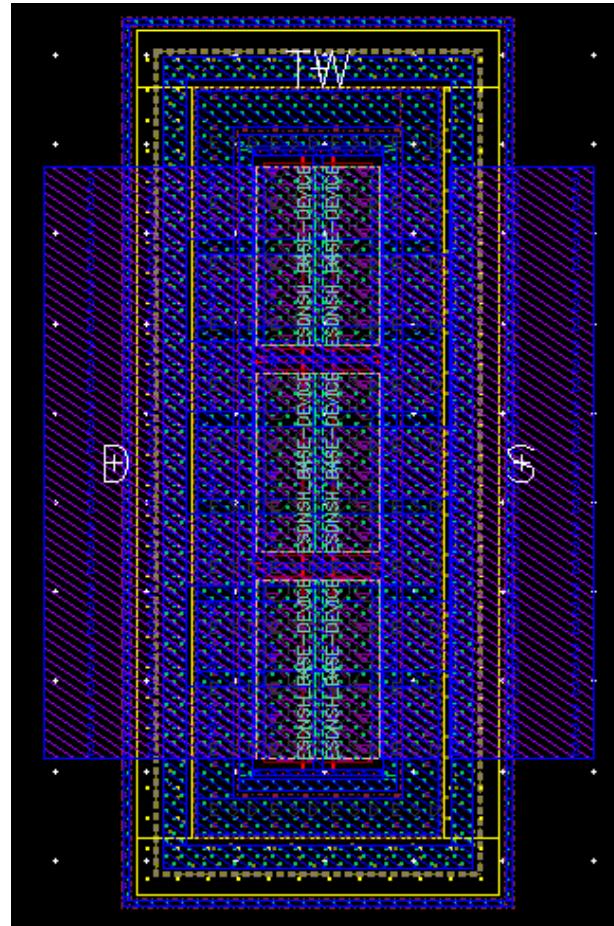


esdvpnp\_string



# Grounded Gate SBLK ESD NFET Macro (esdnfet)

- Standard Dual Well or T3 Ground Gate ESD NFET for Signal to Vss Power Supply Protection. T3 provides lower leakage.
- Silicide is blocked to form source/drain resistors

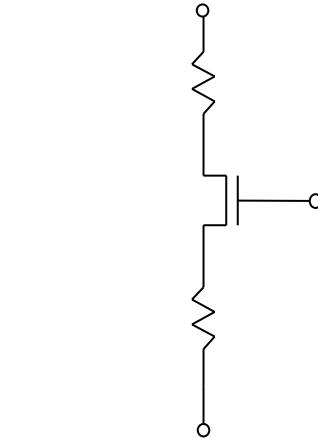
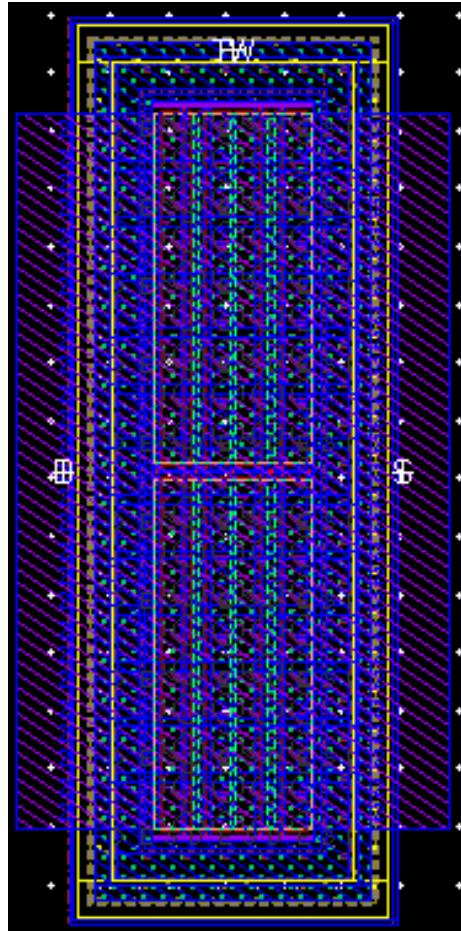


**esdnfet (T3)**

Library	MyBook	Brows...
Cell	esdnfet	
View	layout	
Names	I1	
Mosaic	Rows 1	Columns 1
	Delta Y 74.82	Delta X 37.22
Halo	<input checked="" type="checkbox"/> Define Halo ...	
Physical Only	<input type="checkbox"/>	
<input type="button" value="Rotate"/> <input type="button" value="Sideways"/> <input type="button" value="Upside Down"/>		
FET Voltage	1.5V	1.5V or 2.5V or 3.3V
T3 Isolation Well?	<input checked="" type="checkbox"/> T3 or Dual Well	
Length	120.0n M	
Width	10.0u M	
Number of fingers	2	
Repetitions	3	
Drain SBLK Width	2.09u M	
Source SBLK Width	490.0n M	
ESD Model Type	HBM	HBM or CDM
Wireopt	211	
Draw 3rd Metal?	<input checked="" type="checkbox"/>	

# Self-Protected ESD NFET Macro (spnfet)

- Standard Dual Well or T3 Self-protected ESD NFET for Output Drivers.
- T3 provides lower leakage.



FET Width  
Gates per RX  
Number of RX

**spnfet (T3)**

**Create Instance**

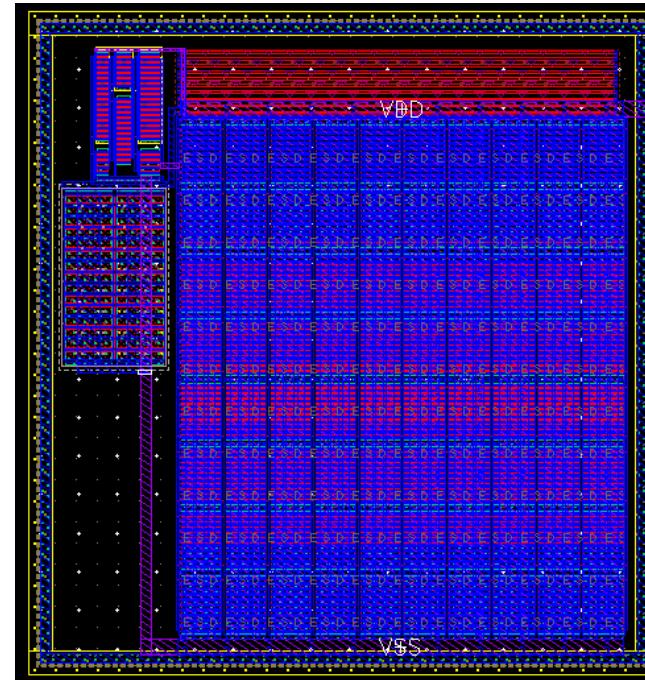
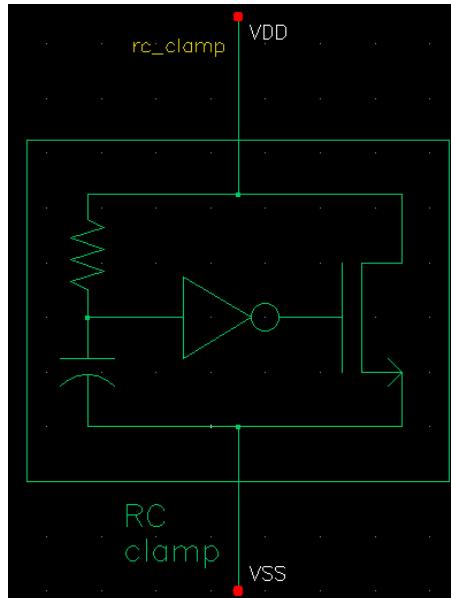
Library	MyBook	Browse
Cell	spnfet	
View	layout	
Names	I1	
Mosaic	Rows 1	Columns 1
	Delta Y 74.82	Delta X 37.22
Halo	<input checked="" type="checkbox"/> Define Halo ...	
Physical Only	<input type="checkbox"/>	
<input type="button" value="Rotate"/> <input type="button" value="Sideways"/> <input type="button" value="Upside Down"/>		
FET Voltage	1.5V	<input checked="" type="checkbox"/> 1.5V or 2.5V
T3 Isolation Well?	<input checked="" type="checkbox"/> T3 or Dual Well	
Length	120.0n M	
Width	30.0u M	
Number of fingers	4	
Repetitions	2	
Drain SBLK Width	2.09u M	
Source SBLK Width	490.0n M	
ESD Model Type	<input checked="" type="checkbox"/> HBM or CDM	
Wireopt	211	
Draw 3rd Metal?	<input checked="" type="checkbox"/>	

# Power Clamps

- **Conducts discharge from supply to ground**
- **Recommended for all chips**
  - Required when VDD – GND capacitance < 100 nF
- **Placement**
  - Uniformly distributed
  - < 1 Ω between any ESD device and nearest power clamp
  - No more than 25 I/Os per clamp
  - < 1 mm from any I/O to nearest power clamp
    - Sufficient to place in 4 corners of chips < 3 mm on edge
- **RC-triggered (slew rate) ESD power clamps and voltage-triggered Darlington power clamps are offered**

# RC Triggered Power Clamp (rc\_clamp)

- Standard Dual well or T3 RC Slew Rate Triggered Power Clamp for 1.5V or 2.5 V. T3 Provides lower leakage.
- Conducts discharge from supply to ground
- Recommended for all chips
  - Required when VDD – GND capacitance < 100 nF
- Used to keep NFET off during normal operation but keep the device on during the transient pulse of ESD event
- NFET must be wide enough to provide a low shunt resistance to ground under ESD conditions

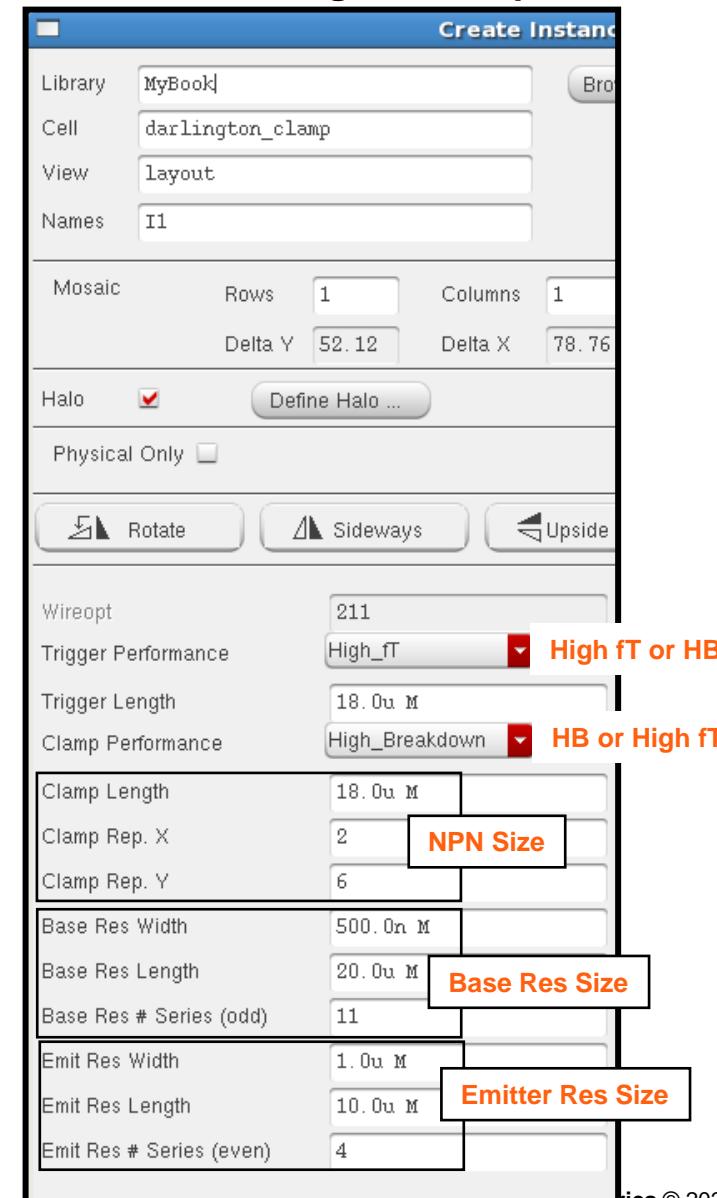
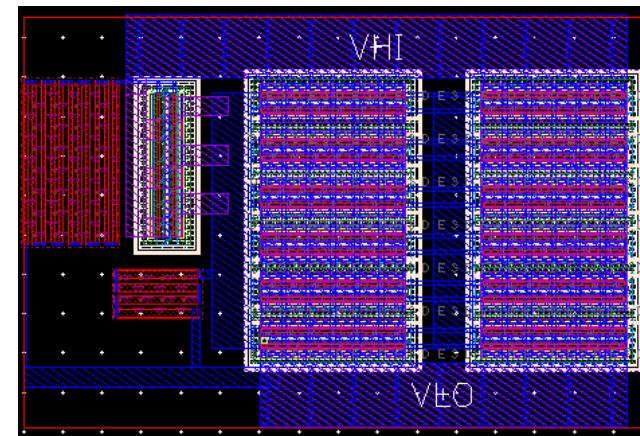
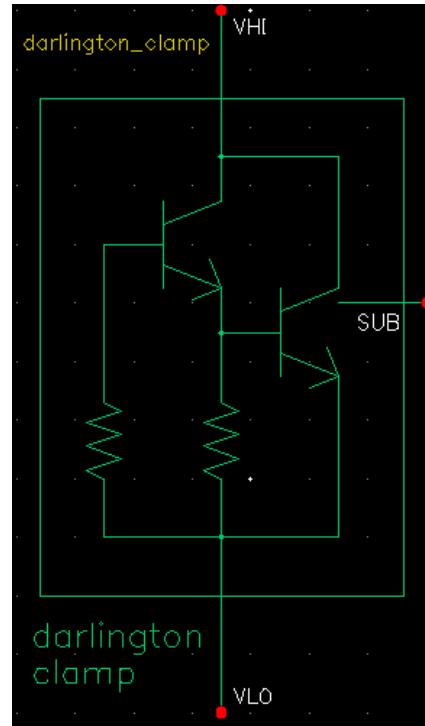


rc\_clamp

Wireopt	211
FET Voltage	1.5V 1.5V or 2.5V or 3.3V
FET Name	nfet nfet or dgnfet or nfet33
T3 Isolation Well?	<input checked="" type="checkbox"/> T3 or Dual Well
Draw 3rd Metal	<input checked="" type="checkbox"/>
Length (all FETs)	240.0n M
NFET Finger Width	5u M
NFET Num Fingers	10
NFET X Repetitions	10
NFET Y Repetitions	8
FET Size	
Cap Width	6.0u M
Cap Length	1.0u M
Cap Num Fingers (C1)	2
Cap Repetitions (C1)	0
Cap Num Fingers (C2)	15
Cap Repetitions (C2)	2
CAP Size	
Res Width	220.0n M
Res Length	56.0u M
Res Series Bars	10
RES Size	
Resistance (R1)	1.06039M Ohms
Est. Capacitance (C1+C2)	1.066492p F
Est. Time Constant (RC)	1.130897u s
INFO	

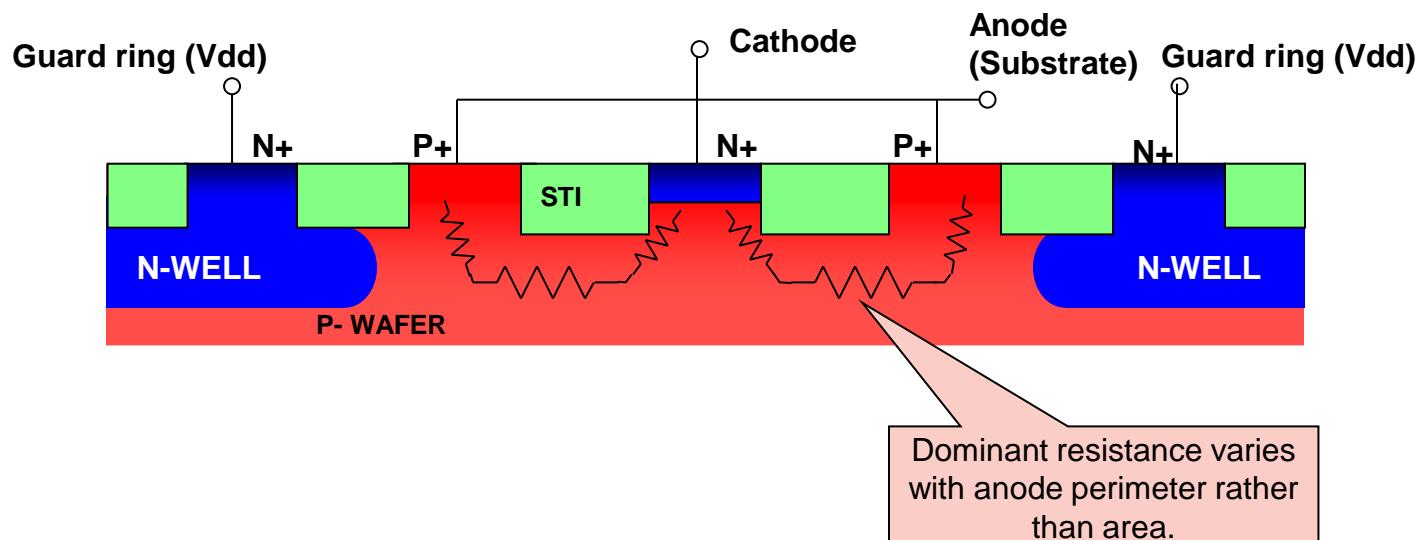
# Voltage Triggered Darlington Power Clamp (darlington\_clamp)

- Darlington Pair Network for Power Pad Protection 2V and 3.6V
- Select proper NPN type for trigger and clamp performance – See ESD Ref Guide for details



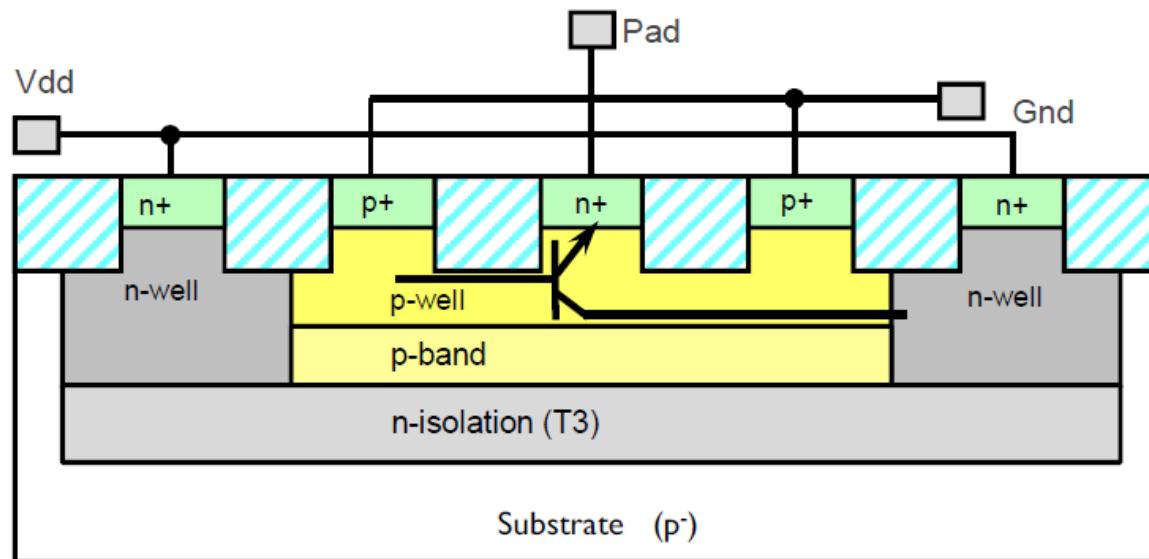
# N+ / Substrate Diode (esdndsx)

- Diodes are much more robust in the forward direction than the reverse.
  - 7-10X more Joule heating due to voltage drop
  - Diode  $R_{ON}$  is higher in the reverse direction
- An N-well guard ring is required to collect injected electrons
  - Minority carriers in p-substrate cause latch-up
- Diode  $R_{ON}$  and robustness are determined by perimeter rather than area



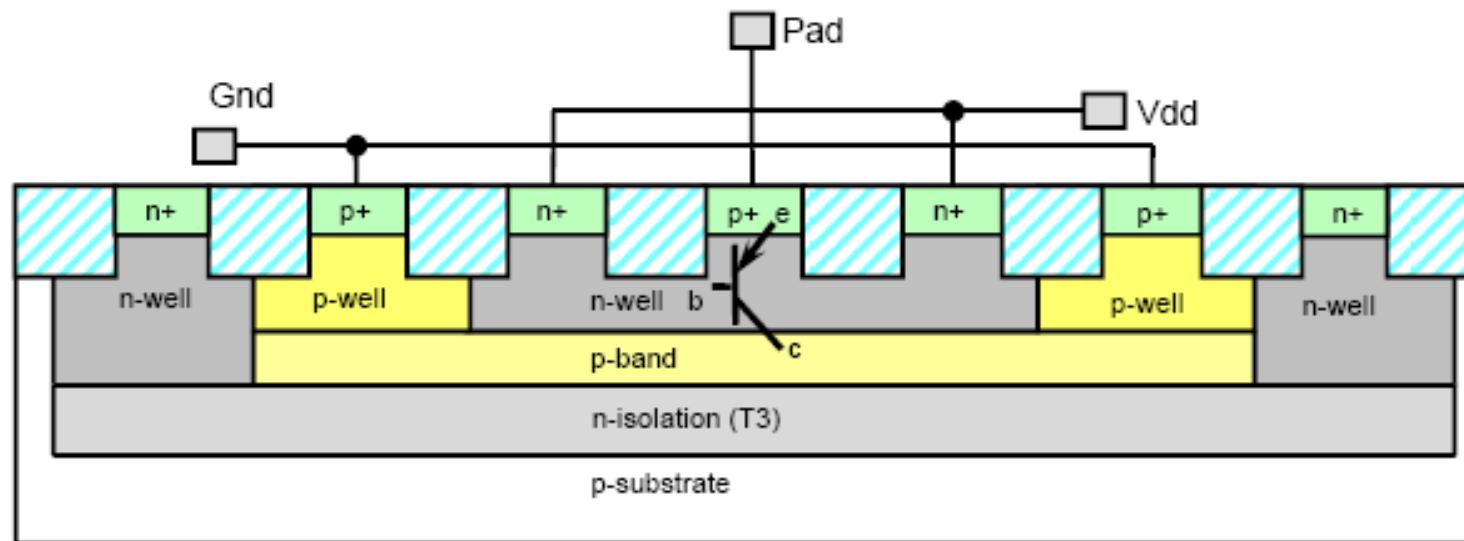
# N+/P-well Diode in T3 (esdvnpn)

*True Triple Well (TTW) N+/PW/T3 Diode  
(p-cell: esdvnpn)*



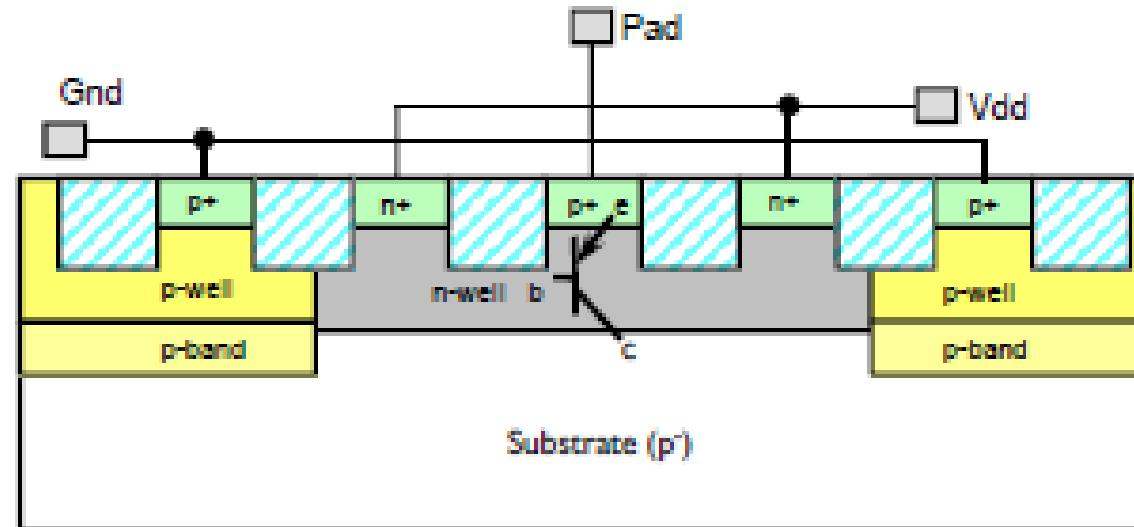
# P+/N-well Diode in T3 (esdvpnp\_t3)

*True Triple Well (TTW) P+/NW Diode  
(p-cell: esdvpnp, with TW enabled)*



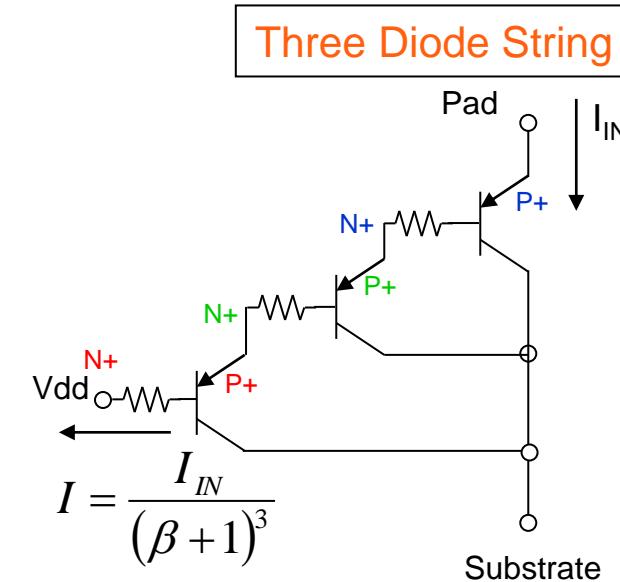
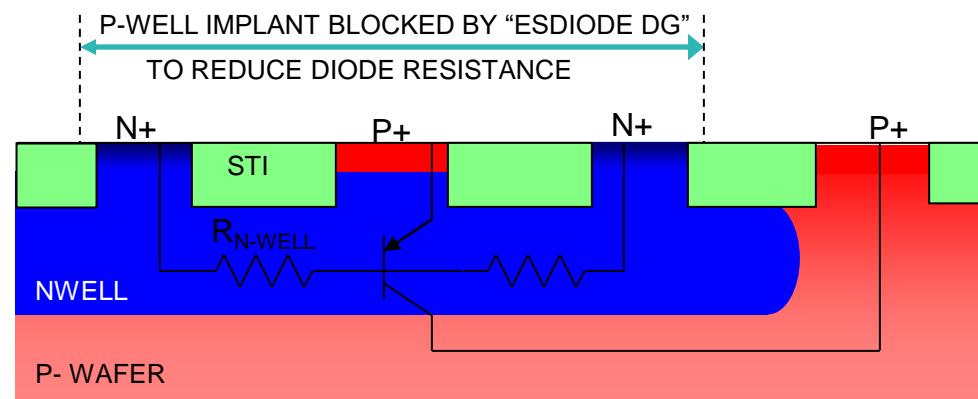
# P+/N-well Diode in substrate (esdvpnp)

*Dual Well (DW) P+/NW Diode  
(p-cell: esdvpnp, with TW disabled)*



# P+/N-well Diode in substrate

- Creates a parasitic vertical PNP transistor (low current  $\beta \sim 1.3$ )
  - Substrate contact ring to capture substrate current.
  - $\beta$  rolls off rapidly with increasing current.
- ESD tolerance and on-resistance area perimeter (vs. area-) dependent.



- P+/N-well diode strings form a Darlington transistor network that directs *most* of the current through the substrate at low currents.
- At high currents, beta roll-off reduces this effect.

$$\text{Overall } \beta_{\text{string}} = (\beta + 1)^3 - 1$$

# ESD Devices High Current Models

- Extend ESD devices (double diode, ESD fets etc.) compact models to cover ESD high current region
  - Verilog-A is used for high current behavior modeling when available
  - ESD high current models are verified under 100ns/30ns/1ns TLP corresponding to HBM/MM/CDM events
  - ESD RC-triggered power clamp may utilize standard MOSFET models for ESD simulation
  - Detailed Documentation and simulation setup included in Model Reference Guide/ESD Ref Guide
    - ESD global switches for ESD simulation
- ESD models capture device failure information upon simulation and report in log file by one of two error messages.
  - [IBMESD\_ERR\_301] Device %m: ESD high current failure at %f A, model is not validated for higher currents, simulator exited.
  - [IBMESD\_ERR\_301] Device %m: ESD high current failure at %f A.
- Transient simulation is recommended to be used to get more correct ESD results
  - Solution for multiple power and/or ground ESD designs
  - Suitable for ESD circuits associated with capacitive (and/or inductive) elements which can significantly affect transient behavior
  - Convergence problem may happen because of complicated mosfet capacitance models
    - May workaround this by turning-off all additional switch in model file, like self heating, impact ionization etc., to keep model as simple as possible
- Contact [fdrytech@globalfoundries.com](mailto:fdrytech@globalfoundries.com) for help

# ESD Simulation setup

- There are three global ESD parameters that need to be set up in design.scs file before running the ESD high current sim

Table 94. ESD global device parameters for ESD high current simulation

Parameter Name	Parameter Value	Description
esd_event	0 (default)	ESD device high current behavior disabled
	1	ESD device high current behavior under HBM event enabled
	2	ESD device high current behavior under MM event enabled
	3	ESD device high current behavior under CDM event enabled
esd_exit	0	Continue simulation if ESD failure encountered
	1 (default)	Stop simulation if ESD failure encountered
esd_extr	0 (default)	Metal wiring resistance and capacitance included in model
	1	Metal wiring resistance and capacitance not included in model

## ESD stimulate source setup

- HBM Source: Trise=7nS, Tfall=7nS, Twidth=100ns, I=HBM spec/1.5KΩ
- I\_HBM = 1.33A to present 2KV HBM spec
- MM Source: Trise=7nS, Tfall=7nS, Twidth=30ns, I=I\_MM
- I\_MM = 2.8A ~3.8A to present 200V MM spec
- CDM Source: Trise=250pS, Tfall=250pS, Twidth=1.2ns, I=I\_CDM
- I\_CDM = 7A ~10A to present 500V CDM spec

## For ESD simulation, there are 6 cases:

- Negative/Positive ESD pulse from IO to GND
- Negative/Positive ESD pulse from IO to VDD
- Negative/Positive ESD pulse from VDD to GND

# ESD Design Review Submissions

- Submit your ESD design review request to GLOBALFOUNDRIES Design and Technology Support at [fdrytech@globalfoundries.com](mailto:fdrytech@globalfoundries.com)
- Requested information for ESD design review
  - Schematics indicating the I/O devices present and important parameters
  - High level block diagram including all circuits that might be exposed to an ESD event
  - Diagram showing protection placed between the various supplies for multi-supply chips
  - All supplies need to be connected through some sort of an ESD discharge path.
  - Layout can be provided in GDS format
- Perform the ESD review early in the design cycle

# PERC

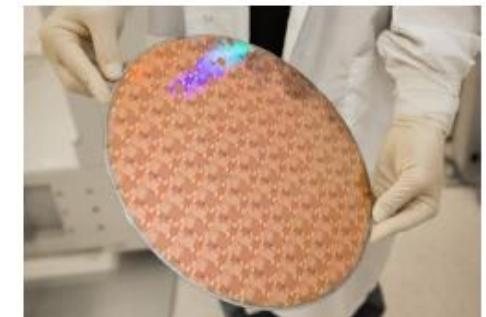
- PERC is a netlist based verification tool which verifies ESD designs.
- It works only with design netlists and relies on the user to provide design information about the power pads, I/O signal pads and ground pads.
- Using this information and the PERC ESD rules found in the GlobalFoundries design manual, PERC provides users ESD design feedback early in the design process.
- These are the ESD Schematic Level Checks (1kv HBM, 250V CDM/2kv HBM, 500V CDM)
- See BICMOS8HP V1.8\_5.0 Calibre PERC Release Notes for usage details
- This design kit component was verified using Calibre 2019.4\_46.30.
- Mentor Graphics Calibre Licenses Required:  
**calibreperc**.



GLOBALFOUNDRIES®

**BICMOS8HP PROCESS DESIGN KIT**

Calibre PERC Component Release Notes



Version: V1.8\_5.0

# PERC LDL

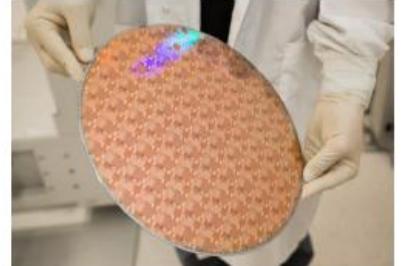
- PERC\_LDL – Programmable Electrical Rule Checking Logic Driven Layout
- Layout Based Current Density Verification
- Mentor Graphics product
- Basic steps involved with this tool:
  - GDS or Oasis layout
  - **MUST be LVS clean!**
  - Locates all ESD protection paths – connections from IO pads to ESD devices.
  - Performs a parasitic extraction of these paths and devices.
  - Applies an electromigration event at the defined pad location (user defined)
  - Evaluates and reports results of the ESD extracted path.
  - **PERC\_LDL is a SIMULATION of what would happen should an ESD event occur**

# Calibre Layout Programmable Electrical Rule Check (PERC\_LDL)

- Layout based Electro Static Discharge (ESD) rule checking
  - Verifies robustness of the interconnect between top level ports and ESD devices
  - PERC\_LDL output is current, current density and point-to-point resistances for metal interconnect between ESD-type structures
  - PERC\_LDL User Guide located in \$GF\_PDK\_HOME/ESD/PERC\_LDL/doc
    - Includes setup and running PERC\_LDL
    - Run.example file provided in the ..//PERC\_LDL/utils
      - Variable setup information and a command line example of running PERC\_LDL
  - Verified with Calibre v2019.4\_46.30
  - ESD rules checked provided in Design Manual Section 6.1
  - Calibre license required: calibreperc and calibrepercsp



**BICMOS8HP PROCESS DESIGN KIT**  
Calibre PERC\_LDL Component Release Notes



Version: V1.8\_5.0

File Name: bicmos8hp.PERC\_LDL\_ReleaseNotes.pdf

# ESD BEOL Parameters

- Attention must be paid to design the proper metal wires for ESD
- All RX diffusions of ESD devices within (ESDDUMMY, ESD\_CLAMP) must be connected to I/O pads with metal stack levels that meet the requirements in the following tables.
  - Table provided in Design Manual Section 6.2 (2KV HBM)
  - Additional data provided in ESD reference guide

## 6.2 ESD Metalization Parameters

The following tables show ESD parameters for metallization, CA, and via levels. All RX diffusions of ESD devices within (ESDDUMMY, ESD\_CLAMP) must be connected to I/O pads with metal stack levels that meet the requirements in the following tables. Use appropriate checking tools to verify these connections.

Table 6-2..ESD Metallization Current Density

Metalization Level	Notes	HBM $I_{FAIL}$ (A/ $\mu m$ )
M1	<sup>1 2 3</sup> , ,	0.13
M2-M4	<sup>1 2 3</sup> , ,	0.17
MQ	<sup>1 2 3</sup> , ,	0.27
LY	<sup>1 2</sup> ,	0.27
E1	<sup>1 2</sup> ,	0.33
MA. AM	<sup>1 2</sup> ,	0.33

1.Calculated from previous design rules. Subject to change pending hardware evaluation

2.Line width assumed to be  $\geq 1\mu m$

3.Minimum required metal width = target ESD current ( $I_{ESD}$ ) / current density ( $I_{FAIL}$ ).

Table 6-3.ESD Via Current Density

Metalization Level	Notes	HBM $I_{FAIL}$ ( $A/\mu m^2$ )
CA	<sup>1 2</sup> ,	1.31
V1-V3	<sup>1 2</sup> ,	0.83
VL	<sup>1 2</sup> ,	0.83
VY	<sup>1 2</sup> ,	0.83
AV	<sup>1 2</sup> ,	0.83
F1	<sup>1 2</sup> ,	0.83

1.Calculated from previous design rules. Subject to change pending hardware evaluation.

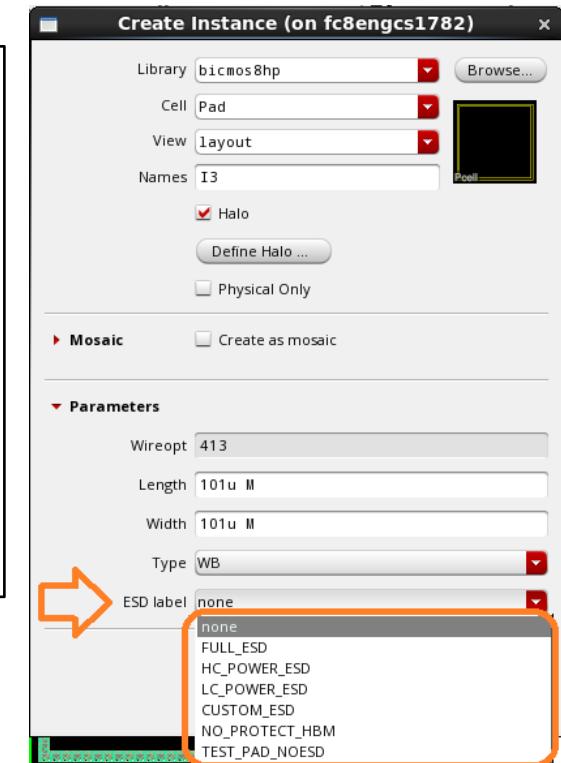
2.Minimum required CA or via area = target ESD current ( $I_{ESD}$ ) / current density ( $I_{FAIL}$ )

# Net Definitions for ESD Layout Checking

- The text labels used to initiate ESD checking are as follows:

Use HC_POWER_ESD label on ground net/pad as well. No check will be on ground pad	<table border="1"><tr><td><b>CUSTOM_ESD</b></td><td>Used on chip pads and chip pad nets that have a custom ESD solution. The custom ESD solution must be reviewed and approved by an ESD design technical representative before use. ESD design rules do not apply to these pads. Designers are responsible for using this label correctly.</td></tr><tr><td><b>FULL_ESD</b></td><td>Used to check all ESD and latchup design rules for signal pads with ESD protection.</td></tr><tr><td><b>HC_POWER_ESD</b></td><td>Used to check power supply or ground pins that achieve a chip capacitance of 100nF between the supply and ground</td></tr><tr><td><b>LC_POWER_ESD</b></td><td>Used to check power supply pins that do not achieve a chip capacitance of 100nF between the supply and ground.</td></tr><tr><td><b>TEST_PAD_NOESD</b></td><td>Used to define a pad that does not have ESD protection devices connected to it. None of the ESD design rules are applicable on these pads. GUARDRNG touching TEST_PAD_NOESD labels will flag an informational warning message that ESD checking is being bypassed. LDESD is the only level that permits these labels. These labels will be ignored on any other design or utility level.</td></tr></table>	<b>CUSTOM_ESD</b>	Used on chip pads and chip pad nets that have a custom ESD solution. The custom ESD solution must be reviewed and approved by an ESD design technical representative before use. ESD design rules do not apply to these pads. Designers are responsible for using this label correctly.	<b>FULL_ESD</b>	Used to check all ESD and latchup design rules for signal pads with ESD protection.	<b>HC_POWER_ESD</b>	Used to check power supply or ground pins that achieve a chip capacitance of 100nF between the supply and ground	<b>LC_POWER_ESD</b>	Used to check power supply pins that do not achieve a chip capacitance of 100nF between the supply and ground.	<b>TEST_PAD_NOESD</b>	Used to define a pad that does not have ESD protection devices connected to it. None of the ESD design rules are applicable on these pads. GUARDRNG touching TEST_PAD_NOESD labels will flag an informational warning message that ESD checking is being bypassed. LDESD is the only level that permits these labels. These labels will be ignored on any other design or utility level.
<b>CUSTOM_ESD</b>	Used on chip pads and chip pad nets that have a custom ESD solution. The custom ESD solution must be reviewed and approved by an ESD design technical representative before use. ESD design rules do not apply to these pads. Designers are responsible for using this label correctly.										
<b>FULL_ESD</b>	Used to check all ESD and latchup design rules for signal pads with ESD protection.										
<b>HC_POWER_ESD</b>	Used to check power supply or ground pins that achieve a chip capacitance of 100nF between the supply and ground										
<b>LC_POWER_ESD</b>	Used to check power supply pins that do not achieve a chip capacitance of 100nF between the supply and ground.										
<b>TEST_PAD_NOESD</b>	Used to define a pad that does not have ESD protection devices connected to it. None of the ESD design rules are applicable on these pads. GUARDRNG touching TEST_PAD_NOESD labels will flag an informational warning message that ESD checking is being bypassed. LDESD is the only level that permits these labels. These labels will be ignored on any other design or utility level.										

- For cell-level checking:** these text labels must be placed on an xxESD design level,
  - where xx = all\_metal\_levels
    - All nets connected to chip pads should be labeled
- For chip-level checking:** only the FULL\_ESD, HC\_POWER\_ESD or LC\_POWER\_ESD labels are valid
  - Chip pad text labels must be placed within the chip pad region (for example, the DV or LV passivation opening layer) and must be on the AMESD or MAESD design level over AM or MA.
  - Valid Pad Labels are available in the Pad pcell
  - All unlabeled chip pads are treated as FULL\_ESD and checked as I/O signal pads.





# **Digital Libraries, IOs and IP**

# BiCMOS8HP/8XP Digital Libraries, IOs and IP: GF

## ▪ Standard Cells Lib

- IP003779 Rev 1 : Digital Standard Cell Library 1.2V 12T RVT CDSLIB
- IP004314 Rev 2 : Digital Standard Cell 1.2V 12T RVT Library (not cdslib)

## ▪ IOs

- IP003416 Rev 2 : GPIO\_WB\_INLINE
- IP003804 Rev 2 : GPIO Base C4
- IP003448 Rev 0 : GPIO Support C4
- IP005669 Rev 2 : C4 GPIO – Automotive/High ESD Target

## ▪ EFUSE

- IP003812 Rev 0 : eFuse 8-Bit electronic fuse macro 3.3V
- IP004072 Rev 3 : eFuse 32-Bit electronic fuse macro 3.3V
- IP004367 Rev 4 : eFuse 128-Bit electronic fuse macro 3.3V
- IP005675 Rev 1 : Automotive/High ESD eFuse 128-Bit electronic fuse macro 3.3V
- IP003996 Rev 0 : eFuse Fsource 3.3V Programming Pad - Required for all eFUSE IPs

## ▪ PLL

- IP003481 Rev 0 : PLL –std (BiCMOS8HP\_PLL\_LP Kit -PLL8SFLP)

## ▪ SRAM

- IP003558 : 1-port SRAM1SD - RVT

Please contact your local GLOBALFOUNDRIES FAE for the IP access

# BiCMOS8HP/8XP Digital Libraries and IP: Vendors

## ▪ ARM

- IP003439 : Standard Cell Library 1.2V 12T RVT library
- IP003503 : SRAM Dual-Port RVT
- IP003830 : Register File – Two-Port RVT
- IP004454 : ROM – Via Programmable RVT

## ▪ S3

- IP00003419 : ADC – 12 Bit 80MSPS Pipeline

## ▪ RIDGETOP

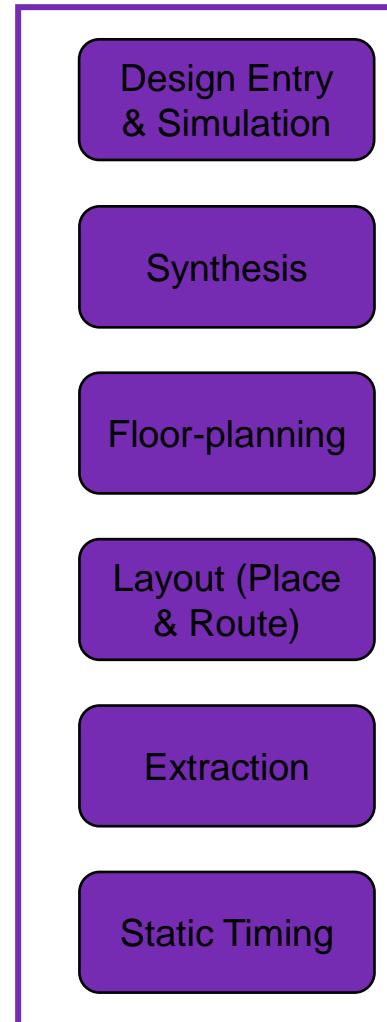
- IP0033845 : ADC - 12-Bit 650MSPS RadHard

## ▪ NOVOCELLLL

- IP004217 : 128-Bit OTP Memory
- IP004334 : 2568-Bit OTP Memory
- IP004229 : 512-Bit OTP Memory

Please contact your local GLOBALFOUNDRIES FAE for the IP access

# BiCMOS8HP/8XP GF Digital Libraries are Cadence Enabled



# GF Standard Cell Library: General Characteristics

- Device channel length:

$0.12\mu\text{m}$   $L_{\text{drawn}}$

- Supply voltage:

$1.5 \pm 0.1\text{V}$

- Operating (Junction) temperature range:

-  $40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (Automotive versions to  $150^{\circ}\text{C}$ )

- Standard cells height and tracks:

$4.8\mu\text{m}$ , 12 tracks

- Power

$0.009\mu\text{W}/\text{MHz/gate}$

# GF Standard Cell Library Installation

- Similar to downloading PDK kit, a copy of standard library is available on the Global-FoundryView.com website.
- Download File Name
  - cmos8hp\_sc\_1p2\_12t\_rvt.v.20170531.tgz\*
- Installs as : <install\_dir>/ibm\_cmos8hp (ibm\_cmos8xp)
- Since all logic cells in standard library are used M1 as the last metal stack, the standard library would be compatible with all available techfiles.

\*IP003779 (June 2, 2017). May change with updated release in future

# GF Standard Cell Library Directory Structure

<b>./cdl</b>	<b>CDL netlist for LVS checking</b>
<b>./doc</b>	<b>SC datasheets, test spec and change log</b>
<b>./gds2</b>	<b>GDS2 for Standard cell library</b>
<b>./layermap</b>	<b>Local copy of the PDK bicmos8hp.layermap</b>  (Boundary layer has been added)
<b>./lef</b>	<b>LEF for Standard cell library</b>
<b>./sch_netlist</b>	<b>Schematic netlists for simulation</b>
<b>./symbol_61</b>	<b>CADENCE OA symbol views</b>
<b>./synopsys</b>	<b>Standard Synthesis Timing Models</b>
<b>./verilog</b>	<b>Verilog behavioral models</b>
<b>.README</b>	

**Note: CDSLIB views may be published in separate package on the Global-FoundryView.com.  
Check with the FAE if it is absolutely needed.**

# GF Standard Cell Library : Documentation

- ..../README files contains:
  - General usage recommendations
  - Support notes
  - DRC/LVS PDK deck version and errata
- Databook contains detailed descriptions of each cell
  - Located in the .../doc/ directory of the kits

# GF Standard Cell Library: Drive Strengths & Performance

- Drive strengths for digital cells are identified with:
  - <cell>\_<drive-strength>: e.g. NAND2\_B, XOR2\_J
    - **Example: NAND2\_B**
      - NAND denotes the logical function
      - 2 denotes the number of inputs
      - B denotes the drive strength/performance level
      - Thus NAND2\_B denotes “logical NAND of 2 inputs at performance level B”
- Drive strengths (performance level) progress from **A** (weakest) through **Z** (strongest)
- Select optimal cell for performance and power consumption
- Performance level is based on the input transition and the output load

# GF Standard Cell Library: Basic Standard Cells

- **Primitive Logic**

- NAND, NOR, INVERT, etc.

- **Unique Logic**

- ADDF – Full Adder
  - CLK – Clock Driver
  - COMP2 – 2-Bit Comparator
  - MUX21 – 2:1 Multiplexer
  - DECAP – Decoupling Cap

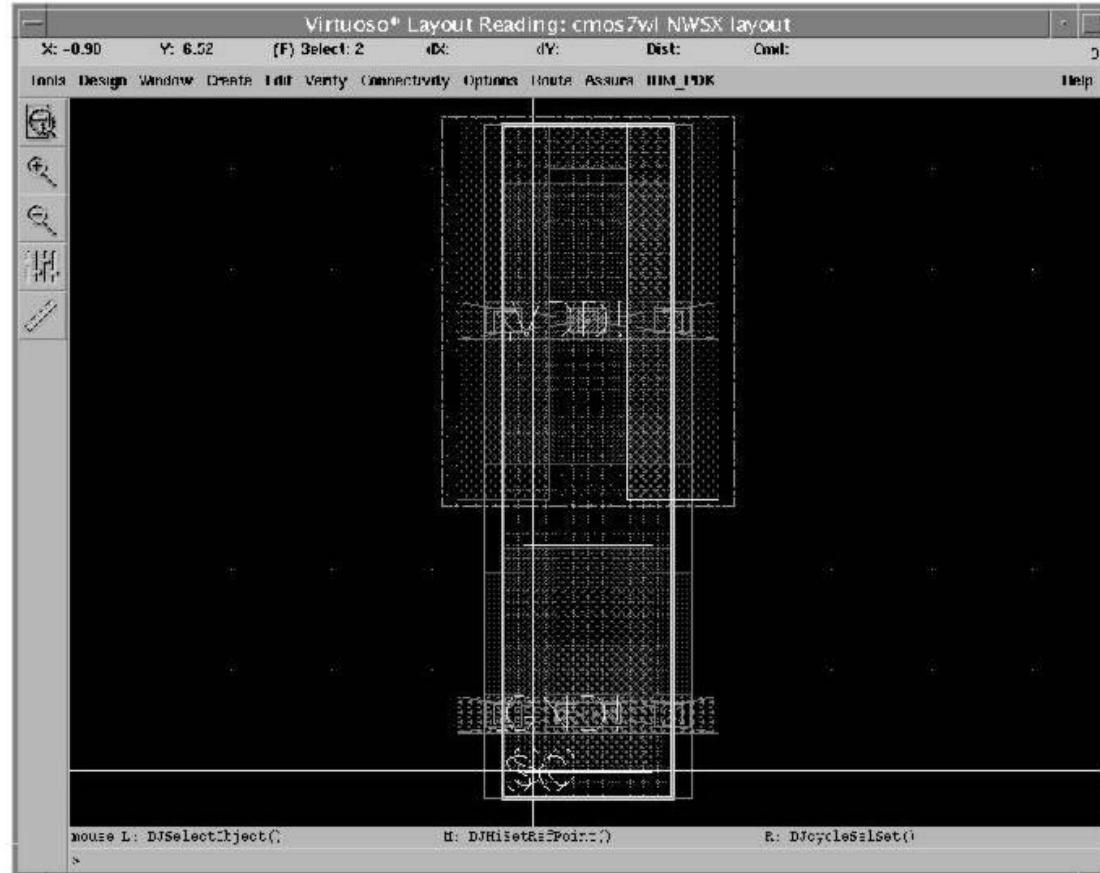
- **Complex Logic**

- AO21, OA21, etc.

- **Sequential Logic**

- DFF – D Flip-Flop
  - LATSR – Latch Set/Reset
  - SDFF – Scanable D Flip-Flop

# GF Standard Cell Library: Physical Design Cells



- **FILLx (x=1, 2, 4, 8, 16, 32, 64, 128)**
  - Single 'row' fill cells for n-well, power bus continuity
- **FGTIE**
  - Used as a floating gate tie down (diode) for antenna repair
- **NWSX**
  - Placed at regular intervals for substrate and n-well taps
  - Each individual cell has no n-well or substrate taps included

# GF Standard Cell Library: CDL Netlists

- Located in the `../cdl/` directory of the kits
- CDL – Circuit Description Language
- Not intended for post layout simulation
- Partial example for NAND2\_C:

```
*.SCALE MICRON
*.MEGA
.PARAM
.SUBCKT NAND2_C A B GND NW SX VDD Z
*.PININFO A:I B:I Z:O GND:B NW:B SX:B VDD:B
MTNA Z A net58 SX nfet M=1 l=120.0n w=1.07u nf=1 rf=0 ngcon=1 mSwitch=0
MTNB net58 B GND SX nfet M=1 l=120.0n w=1.07u nf=1 rf=0 ngcon=1 mSwitch=0
MTPB Z B VDD NW pfet M=1 l=120.0n w=1.07u nf=1 rf=0 ngcon=1 mSwitch=0
MTPA Z A VDD NW pfet M=1 l=120.0n w=1.07u nf=1 rf=0 ngcon=1 mSwitch=0
.ENDS
```

Design Entry  
& Simulation

Synthesis

Floor-planning

Layout (Place  
& Route)

Extraction

Static Timing

# GF Standard Cell Library: Simulation Models

- Industry standard Hardware Description Language (HDL) models
  - Verilog (.../verilog/)

Design Entry & Simulation

Synthesis

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# GF Standard Cell Library: Synthesis Models

- Liberty Format (.lib)
  - Located in the .../synopsys
- Supported by standard tools, e.g.:
  - Cadence Encounter RTL Compiler
  - Synopsys Design Compiler

Proccess	Temp.	Voltage	Name
=====			
Typical	25	1.20	PnomV1p20T025_STD_CELL_8HP_12T
Typical	25	1.50	PnomV1p50T025_STD_CELL_8HP_12T
Fast	-40	1.32	PbcV1p32Tm40_STD_CELL_8HP_12T
Fast	-40	1.62	PbcV1p60Tm40_STD_CELL_8HP_12T
Fast	-55	1.32	PbcV1p32Tm55_STD_CELL_8HP_12T
Fast	-55	1.62	PbcV1p60Tm55_STD_CELL_8HP_12T
Slow	125	1.32	PwcV1p08T125_STD_CELL_8HP_12T
Slow	125	1.40	PwcV1p40T125_STD_CELL_8HP_12T
Fast	125	1.60	P_Leak_FF_V1p60T125_STD_CELL_8HP_12T
			- Fast leakage current data

Design Entry  
& Simulation

Synthesis

Floor-planning

Layout (Place  
& Route)

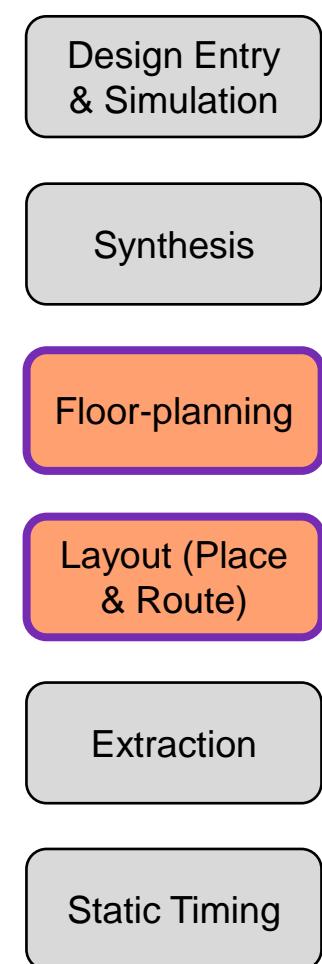
Extraction

Static Timing

Additional corners for Automotive

# GF Standard Cell Library: Physical Design Models

- Located in the `.../lef` directory of the kits
  - LEF – Library Exchange Format
  - Standard physical design syntax
    - Cell LEF, Antenna LEF and Technology LEF files
  - Supported by Cadence Place and Route Tools\*



\*Synopsys IC Compiler support available on request. Please check with your FAE.

# GF Standard Cell Library: Parasitic Extraction

- Supported PEX Tools:

- Assura QRC
- CalibreQRC
- Calibre xRC

Design Entry  
& Simulation

Synthesis

Floor-planning

Layout (Place  
& Route)

Extraction

Static Timing

# GF Standard Cell Library: Timing Models

- Synopsys timing models
  - Located in the `../synopsis/` directory of the kit  
.lib, .db,
  - Subdirectories devoted to various process, voltage, temperature operating conditions\*

\*Other PVT corners may be available by requesting through FAE.

Process	Temp.	Voltage	Name
=====			
Typical	25	1.20	PnomV1p20T025_STD_CELL_8HP_12T
Typical	25	1.50	PnomV1p50T025_STD_CELL_8HP_12T
Fast	-40	1.32	PbcV1p32Tm40_STD_CELL_8HP_12T
Fast	-40	1.62	PbcV1p60Tm40_STD_CELL_8HP_12T
Fast	-55	1.32	PbcV1p32Tm55_STD_CELL_8HP_12T
Fast	-55	1.62	PbcV1p60Tm55_STD_CELL_8HP_12T
Slow	125	1.32	PwcV1p08T125_STD_CELL_8HP_12T
Slow	125	1.40	PwcV1p40T125_STD_CELL_8HP_12T
Fast	125	1.60	P_Leak_FF_V1p60T125_STD_CELL_8HP_12T
			- Fast leakage current data

Additional corners for Automotive

Design Entry & Simulation

Synthesis

Floor-planning

Layout (Place & Route)

Extraction

Static Timing

# GF Standard Cell Library: Cadence AMS Simulation Enablement

- Symbol
  - Located in the `../symbol/61`
- Spectre netlist
  - Located in the `../sch_netlists`
- References **bicmos8hp/bicmos8xp** device library
  - Enables expanded netlisting capability
  - Spectre circuit simulation
  - Virtuoso Analog Design Environment
- Mixed-mode simulation
- Schematic-less design flow provided as reference (See next page)

Design Entry  
& Simulation

Synthesis

Floor-planning

Layout (Place  
& Route)

Extraction

Static Timing

# Schematic-Less Design Flow

- **Step 1: Initial Preparation**

- Copy symbol views and rename them to “auCdl” for CDL netlisting
- Copy symbol views and rename them to “spectre” for spectre netlisting
- Copy symbol views and rename them to other if applicable
  - Note: Implicit/Inherited connections do not work in this flow

- **Step 2: CDL Netlisting**

- Set the following in .cshrc
  - *setenv CDS\_Netlisting\_Mode “Analog”*
- Add the following in .simrc (in home or working directories)
  - *auCdl|CDFPinCntrl = t*
    - Note: This setting will ensure the term order in a CDL netlist in synch with CDF
- Generate a CDL netlist in a schematic window using PDK utility
  - Note: Make sure the netlist mode is set to “analog”
- Add a line to the newly created CDL netlist to include a library cell CDL netlist provided by a digital design kit.
  - For example:
    - *INCLUDE “./IBM\_CMHV7SF\_SC\_5V\_18T.cdl”*
- Run LVS, in either GUI or command modes

- **Step 3: Spectre Netlisting**

- Start ADE in a schematic window
- Set model libraries and add a library spectre netlist provided by a digital kit as one of model libraries
- Run a spectre simulation as usual

# **GF I/O Cells**

- Released as Additional IP components
- Types of I/O cells available
  - Wirebond Standard Basic IO Cells
  - C4 Standard Basic and Support IO Cells
- Directory Structure
  - Similar to Basic Standard Cell directory structure

# GF Standard Basic WB I/O Cells Offering\*

## ■ Basic Bidirectional I/Os

- Perimeter I/O (Wire bond I/O)
- Support 7AM,6AM,5AM and 6MA wiring levels
- Power supply: 1.5V, 1.8V, 2.5V, 3.3V
- Driver terminated impedance: 20Ω, 35Ω, 50Ω, 65Ω
- Signal latch options: Pull down, Pull up or none
- Drive strengths Level: A, B
- Typical cell size: 73um x 171um (W x H)
- JEDEC industry standard ESD protection

## ■ Other I/O support cells

- Power & Ground Cells with ESD protection
- Corner, Fill, Etc.

\* Additional metal stacks and I/O cells may be optionally requested through your FAE

# GF Standard Basic C4 I/O Cells Offering\*

## ■ Basic Bidirectional I/Os

- Flip chip solder bump
- Support 6AM wiring level
- Power supply: 1.5V, 1.8V, 2.5V
- Driver terminated impedance: 20Ω, 35Ω, 50Ω, 65Ω, 90Ω
- Signal latch options: Pull down, Pull up or none
- Drive strengths Level: A, B, C
- Typical cell size: 201.6um x 86.4um (W x H)
- JEDEC industry standard ESD protection

## ■ Other I/O support cells

- Power & Ground Cells with ESD protection
- Released in a separated package as “support\_c4\_io”

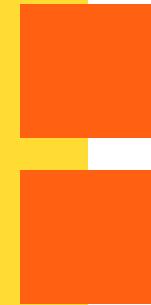
\* Additional metal stacks and I/O cells may be optionally requested through your FAE

# **GF PLL-Std IP : PLL8SFLP BiCMOS8HP\_PLL\_LP Kit\***

## **■Kit Contents**

- ./cdl** CDL netlist for LVS checking
- ./doc** PLL8SFLP datasheets, test spec and change log
- ./drc** DRC results summary (Assura Only)
- ./gds2** GDS2 for PLL8SFLP
- ./lef** LEF for PLL8SFLP
- ./lvs** LVS results summary (Assura Only)
  
- ./synopsys** PVT Corners for Timing Analyses
  
- ./verilog** Verilog behavioral models
- ./vhdl** Functional VHDL models
- ./vital** VITAL models

**\*Check with GLOBALFOUNDRIES FAE if additional IP is required**



# Simulation

# **BiCMOS8HP/BiCMOS8XP Simulation**

- **Simulation Environment and Documentation**
- **Simulation Capabilities**
- **HSPICE, Spectre and ADS Dynamic Link Simulation setups**
- **Accounting for Process Variation**
  - Monte Carlo simulations
  - Corner simulations

# Supported Simulators and Documentation

- **Supported Simulators**

- Cadence Spectre
- Synopsys HSPICE
- Keysight ADS (Interoperable PDK) – Schematic/Layout
- Keysight GoldenGate
  - Simulation in Cadence ADE Environment, uses Spectre Models
- Keysight ADS Dynamic Link
  - Simulation in ADS Environment, uses Spectre Models
- EM Simulators - Momentum, EMX and PeakView

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**BiCMOS8HP  
Model Reference Guide**

- **Extensive documentation in Model Reference Guide**

- Simulation control switches
- Model library structure and usage
- For each device
  - Features, restrictions, limitation, usage notes
  - Supported instance parameters
  - Sample model to hardware correlation plots
- MRG located in \$GF\_PDK\_HOME/doc/bicmos8hp\_model\_guide.pdf

Owner: RF Technology  
Compact Model Development

Version Date: March 12, 2021  
Release: V1.8\_5.4

- **Release Notes for each simulator**

- Supported simulator versions
- Simulator usage notes
- Example: \$GF\_PDK\_HOME/Models/Spectre/doc/

# EM (Electromagnetic ) Simulators Support

- Located in .../Emagnetic directory
- Momentum
  - Located in the ../Emagnetic/EMX directory : Momentum .ltd files
- EMX
  - Located in the ../Emagnetic directory : EMX .proc files
- ITF
  - Located in the ../Emagnetic/ITF directory : ITF .itf files
- PeakView
  - Located in the ../Emagnetic/PeakView directory : PeakView .py files
- Documentation
  - Located in \$GF\_PDK\_HOME/Emagnetic/<tool>/doc directory : Electromagnetic Enablement EM Guide bicmos8hp(8xp).EM\_guide.pdf file

# Simulation Capabilities

- **Nominal Simulations**
- **Monte Carlo**
  - Global process variation
  - Instance specific variation (mismatch)
- **Corners**
  - **Fixed corners for digital logic simulation**
    - Logical performance corners TT, FF, SS
    - Functional corners FS, SF, SSF (SS\_Functional), FFF (FF\_Functional)
  - **Custom Corner methodology for wide range of circuit types**
    - User defined corners
- **Wafer-Specific**
  - May be used to correlate circuit level simulation to hardware measurements on prototype parts.
  - An aid for users to take a minimal set of device measurement data from kerf PCM and then translate them to the internal model parameters to approximate, to the first-order, the measured device characteristics in the nominal simulation.
- **Global switches controlling associated devices' Impact Ionization, Self-heating, Substrate model and convergence aid**
  - Also see Model Reference Guide (MRG), "Global and local switches to aid convergences" Section for details

# Spectre Simulation Setup

```
include "<user_directory>/design.scs"  
include "<user_directory>/wafer.scs"  
include "<LIBRARY_PATH>/allModels.scs" section=XX
```

**ORDER IS IMPORTANT!! design.scs, wafer.scs and then allModels.scs**

- **design.scs**

- Contains global switches, corner parameters and other user-defined settings for simulations.
- Copy and edit switches as desired for simulations.

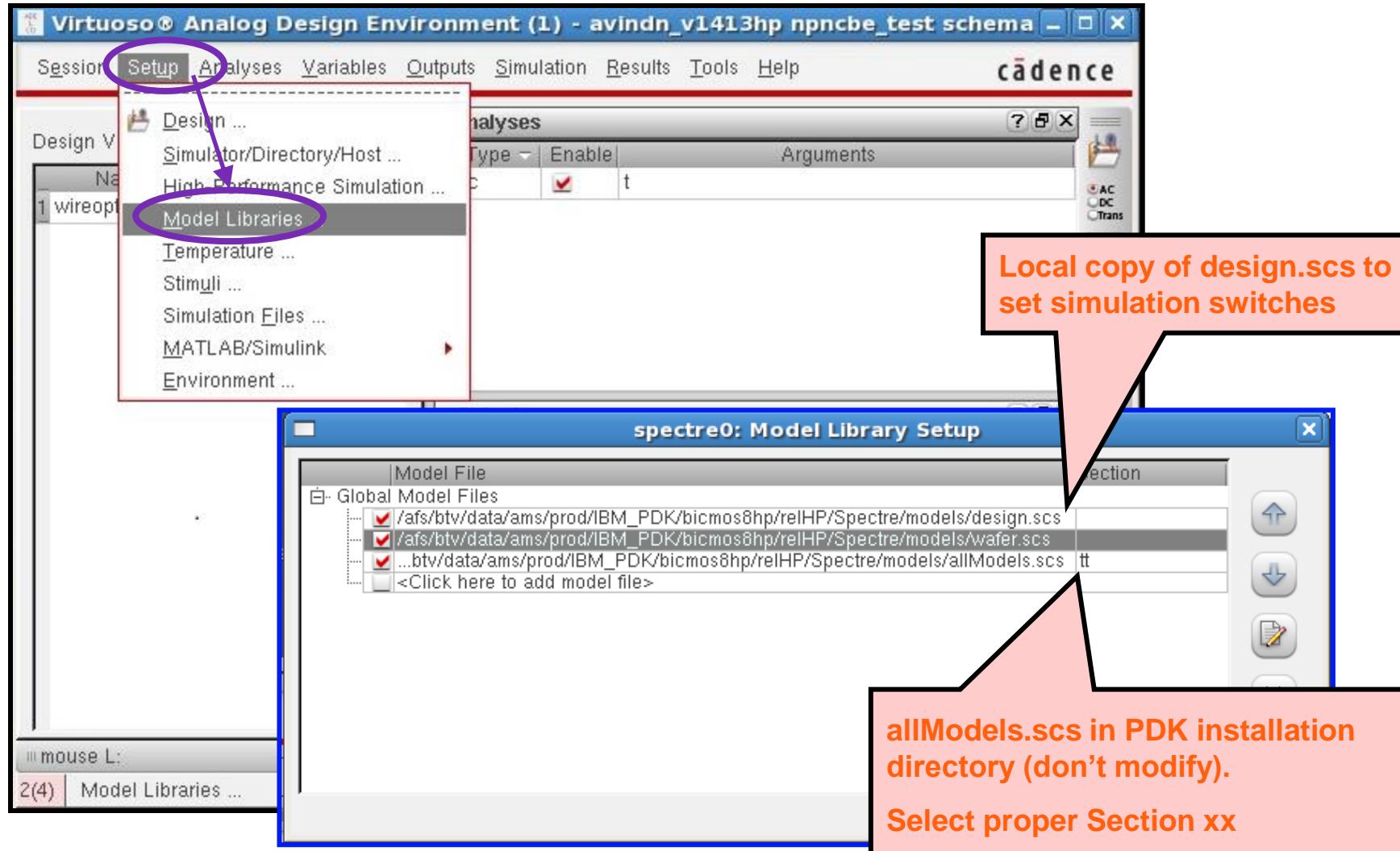
- **wafer.scs**

- Specify wafer-specific overrides using inline data parameters.

- **allModels.scs**

- File to specify all model include statements to support nominal, custom process corner and Monte Carlo simulation analysis options.
- Includes calls to other model files

# Analog Design Environment (ADE) - Spectre



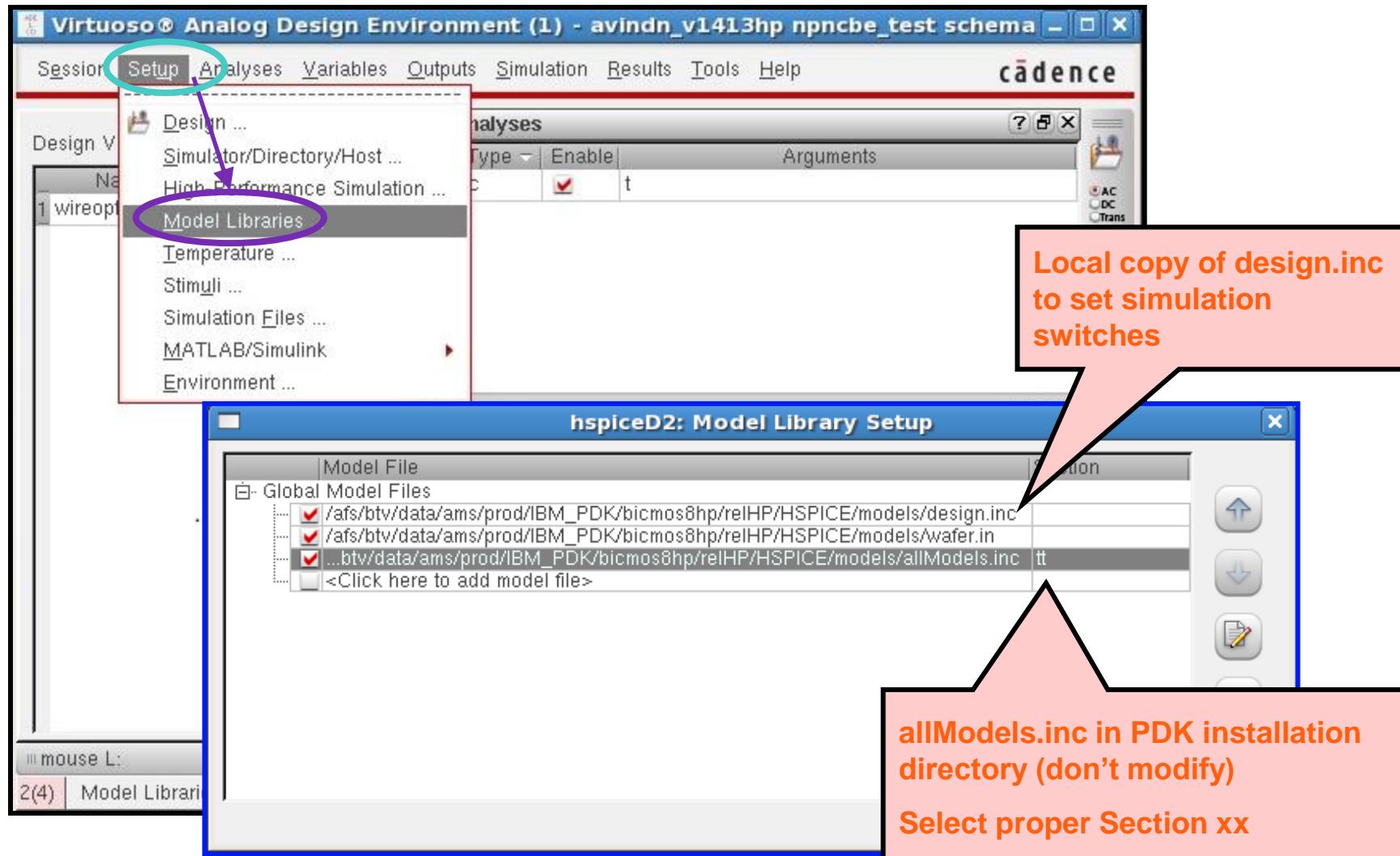
# HSPICE Simulation Setup

## Setup files required

```
include '<PDK model directory path>/design.inc'  
include '<PDK model directory path>/wafer.inc'  
include '<PDK model directory path>/allModels.inc' XX
```

- **design.inc (global switches and corner parameters)**
  - Copy to local directory and customize as desired
  - Change include statement to point to local file
- **wafer.inc (wafer specific parameters)**
  - Specify wafer-specific overrides using inline data parameters.
- **allModels.inc XX**
  - File to specify all model include statements to support nominal, custom process corner and Monte Carlo simulation analysis options
  - Includes **skew.file** (skew parameters, process distributions, corner parameters)
  - Includes **models.inc** separate device model files

# Analog Design Environment (ADE) - Hspice

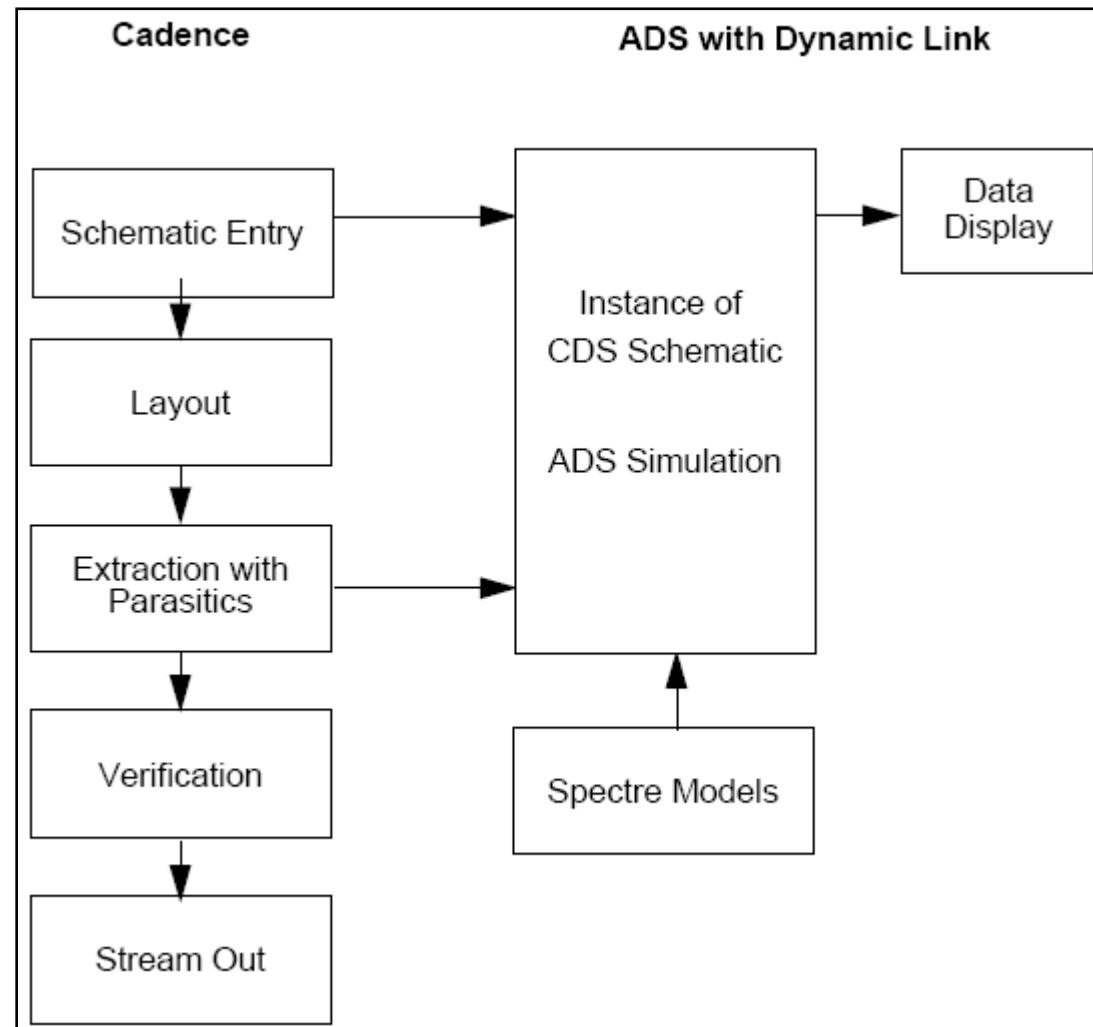


# **GoldenGate**

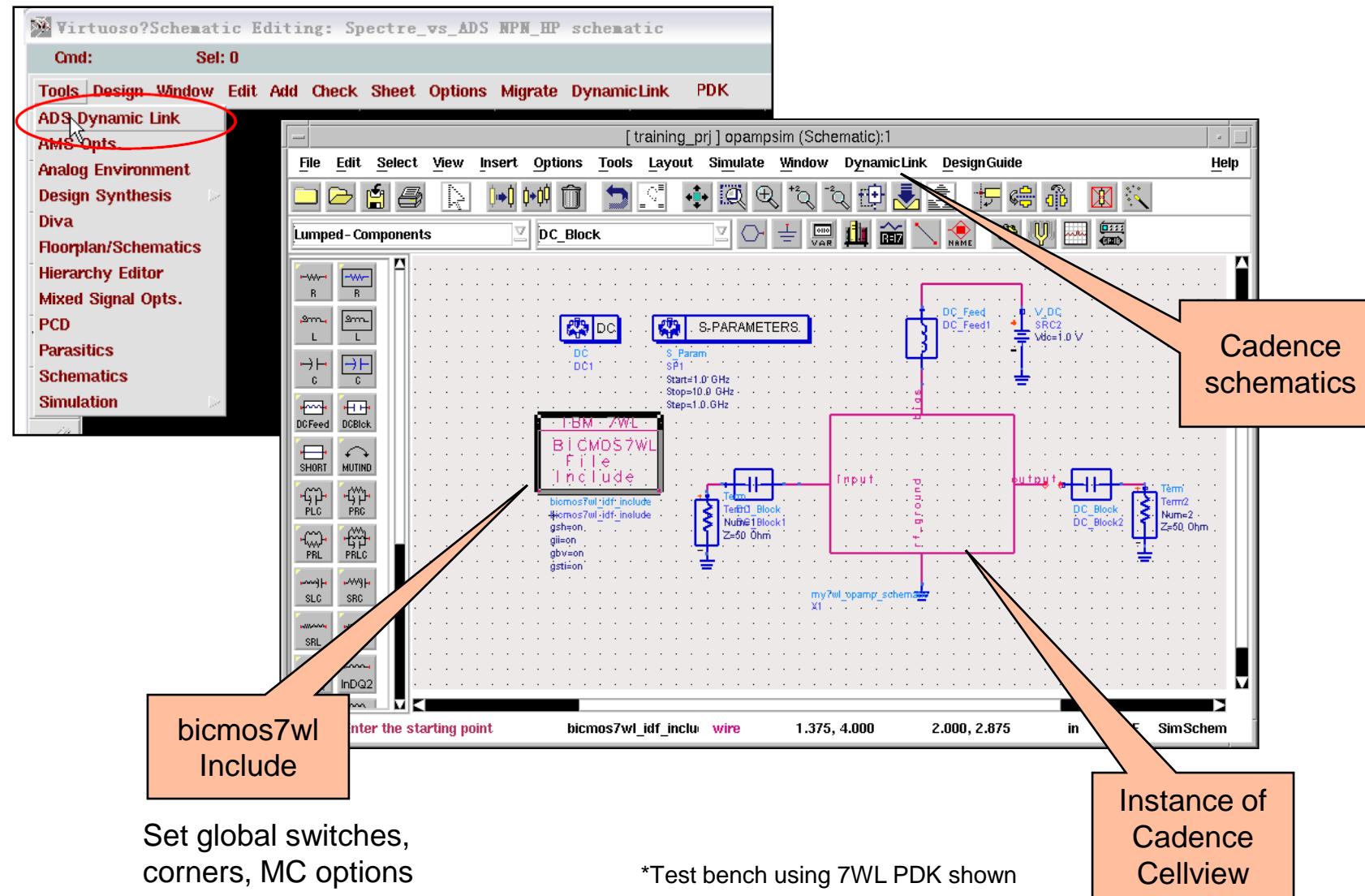
- **GoldenGate works entirely within the Cadence environment and does not require any additional enablement files.**
- **GoldenGate parses Spectre models directly.**
- **See GoldenGate Design Kit User's Guide for set up**

# ADS Dynamic Link

- Provides Simulation Interface between Cadence and ADS
- Simulates Cadence schematics in ADS
  - Design schematic entry in Cadence Virtuoso only.
- ADS simulation from the Cadence extracted view is supported in ADS Dynamic Link
- ADS version requirement and Documentation in PDK ADS User's Guide and Release Notes located in the `../$GF_PDK_HOME/ADS/doc` directory
  - `bicmos8hp(bicmos8xp)_ADS_users_guide.pdf` and `bicmos8hp(bicmos8xp) _ADS_users_rel_notes.pdf`



# ADS Dynamic Link Test Bench Example\*



# Design Variables (works with all simulators)

- Insert a variable as CDF parameter value instead of a numerical value
- Evaluated at simulation run time
- Supported for resistors, capacitors, and npns, and FETs
- Must be set to a valid dimension prior to Virtuoso XL or LVS
- For passive devices, unspecified parameter is automatically set to a negative number
  - Resistor example:  $L = 3 \mu\text{m}$ ,  $W = r1wid$ ,  $R = -1$
- When design variable used for FET
  - Calculation of S/D parasitics performed in the CDF netlisting

# Global Simulation Control Switches

- `design.scs` (Spectre, ADS)
- `design.inc` (HSPICE)

***gsh***  
Self-heating effects for  
NPN, VNPN and  
Resistor

***gstis***  
STI stress effect for  
FETs

***gwellss***  
NWell Proximity  
effect for FETs

***gbv*** (Spectre only)  
Breakdown warnings  
printed for FETs and  
NPNs

***gii***  
Ionization Impact for  
NPN and VNPN

- 0 **Global override: switch off for all instances**
- 1 **No override: use settings from each instance (set in CDF)\***
- 2 **Global override: switch on for all instances**

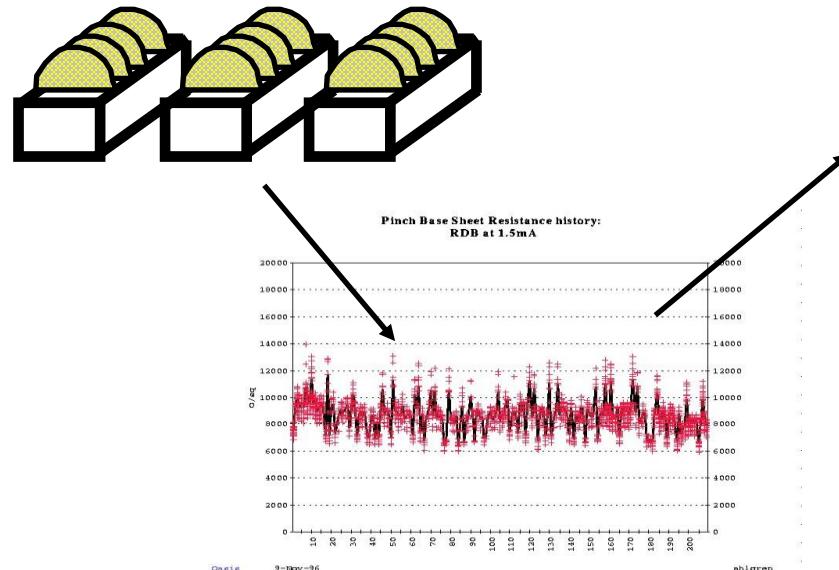
\* `gbv =1` FET warnings are on

# Accounting for Process Variation

- **Monte Carlo statistical simulations**
  - Best representation of long term manufacturing performance
  - Includes mismatch, important for differential circuits
  - Long simulation times for complex circuits
- **Corner simulations**
  - Faster simulations of circuit functionality under process extremes
  - Custom corner methodology for analog design
    - Calibrate with statistical simulations
      - Application note “Statistical and Corner Simulations” APN-000091
    - Insight into circuit sensitivities to device classes
- **Confirm simulated performance through process window hardware**
  - Vary key process parameters on experimental wafers

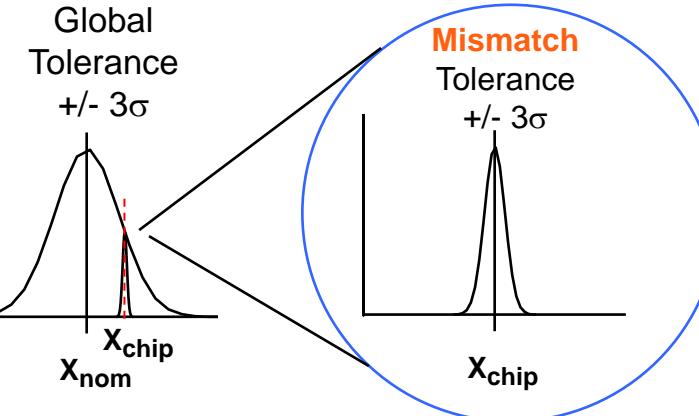
# Statistical Modeling (Monte Carlo)

- Represent process variations as Gaussian
- Lot to lot, wafer to wafer, chip to chip variation
  - “Global” process variation

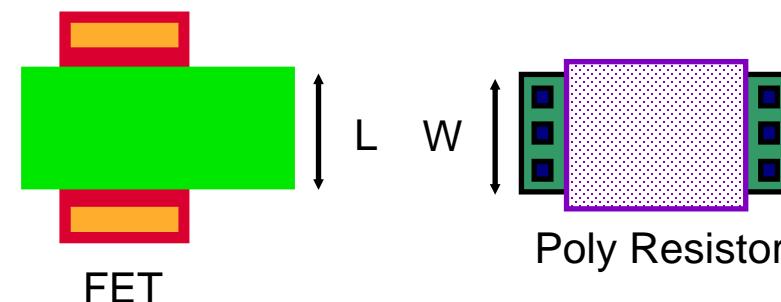


- Consistency between model limits, electrical specifications and manufacturing capability
- Monte Carlo mismatch assumes good layout practices

- Like devices, similar surroundings, close proximity

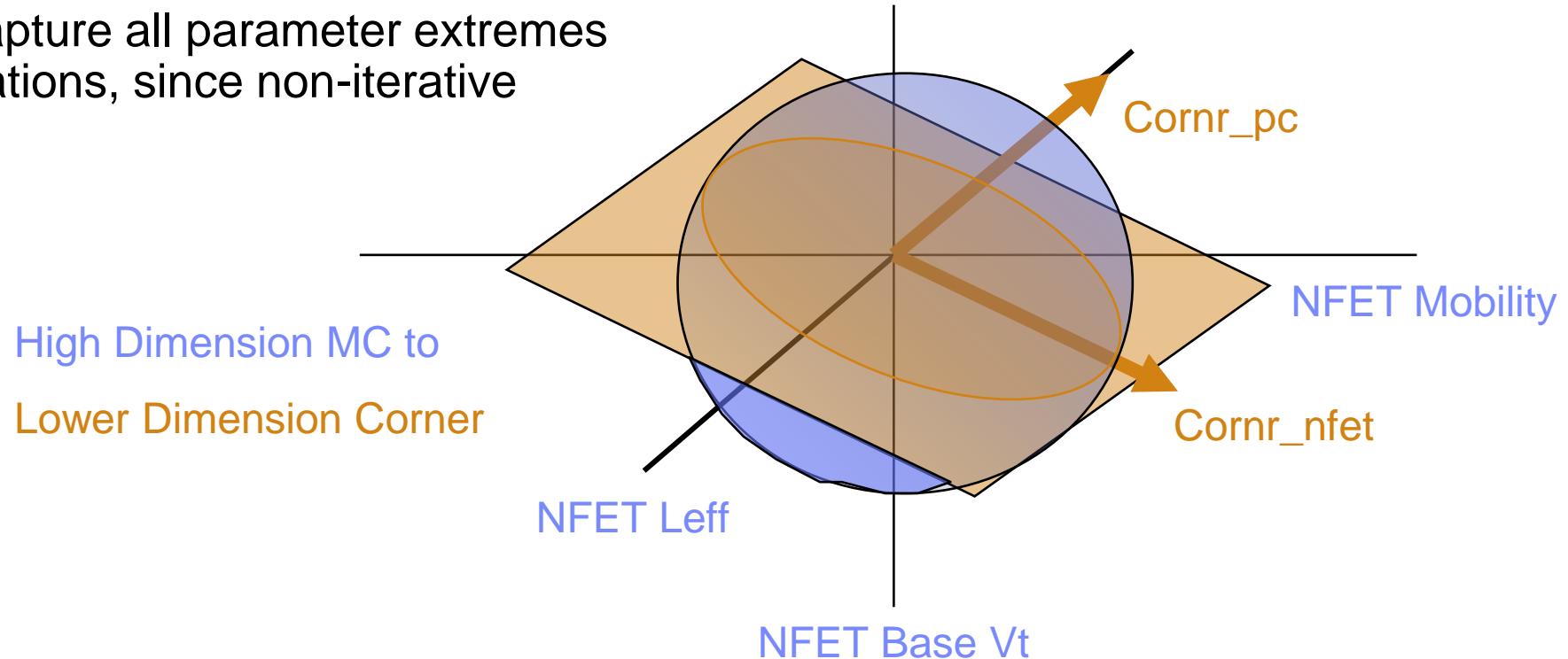


- First order correlations based on physical relationships or common/shared process steps
  - FET channel length (L) correlated to poly resistor width (W) through PC (poly) image bias



# Monte Carlo versus Corners

- Monte Carlo - specifies probability densities in multi-dimensional space
  - Many iterations required to see process extremes in statistical simulation
- Corner models collapse that space into pre-determined set of excursions from nominal
  - Deterministic
  - Can never capture all parameter extremes
  - Faster simulations, since non-iterative



# Custom Corner Analysis

- Adds a fixed skew to a subset of statistical process parameters
  - Maintains correlation between devices and process / model parameters
  - Supports Complex analog designs by user defined corner settings
- Corner values specified in
  - `design.scs` (Spectre, ADS)
  - `design.inc` (HSPICE)
- Recommended: Calibrate with Monte Carlo statistical analysis
  - Sensitivity analysis: determine direction and approximate value for corner parameters
  - Choose magnitude of skew sigma to match Monte Carlo  $3\sigma$  extremes for circuit parameter of interest

# Definition of Fixed Corners\*

## Performance Corners\*\*

Section	Corner Name	Definition	Purpose
<b>tt</b>	<b>TT</b>	Typical Model	Nominal device targets
<b>ff</b>	<b>FF</b>	Fast timing corner for CMOS Static Logic	Ring Oscillator Line Data and Monte Carlo simulation
<b>ss</b>	<b>SS</b>	Slow timing corner for CMOS Static Logic	Ring Oscillator Line Data and Monte Carlo simulation
<b>fs</b>	<b>FS</b>	Fast NFET/Slow PFET	Idsat and Vtsat NFET-to-PFET mismatch line data
<b>sf</b>	<b>SF</b>	Slow NFET/Fast PFET	Idsat and Vtsat NFET-to-PFET mismatch line data

## Functional Corners\*\*\*

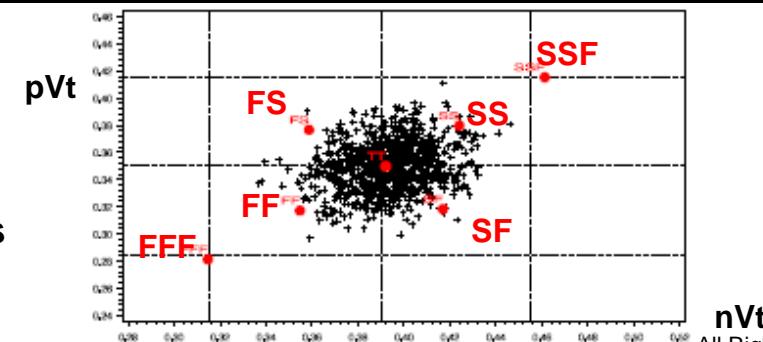
<b>fff</b>	<b>FF-Functional (FFF)</b>	3r Fast single device characteristics	Design Manual Limits for Idsat & Vtsat on wide/short & narrow/short FETs
<b>ssf</b>	<b>SS-Functional (SSF)</b>	3r Slow single device characteristics	Design Manual Limits for Idsat & Vtsat on wide/short & narrow/short FETs

Fixed corners are appropriate for digital circuits

\*See MRG Section 1.9

\*\*Design should meet specifications at these corners

\*\*\*Design should be functional at these corners



# Custom Corner Parameters

- **Multiple corner parameters**

- Grouped skew parameters allow quasi-independent control of device groups
- Shared corner parameters for process parameters that affect **single device group**
  - `cor_nfet` and `cor_pfet` affect all n- and p-type
  - `cor_bip`, `cor_res`, `cor_cap` & `cor_ind` for bipolars, resistor, capacitor & inductor skews
- Shared corner parameters for process parameters that affect **multiple device group**
  - `cor_tox`, `cor_pc` & `cor_rx`
  - Adjustable (-3 to +3) to cover full process range
- See the Model Reference Guide for more information (Section 2.2)

Table 5. Single Device Group Corner Parameters

Corner	Devices Affected in a Dominant Manner	Positive Corner Parameter Yields
cor_npn	npn, npnxp, nsres, pin	High current, high speed
cor_pnp	vppn	High current, high speed
cor_nmos	nfet(tw)	High current, high speed
cor_pmos	pfet	High current, high speed
cor_dgnmos	dgnfet(tw), nfet33(tw)	High current, high speed
cor_dgpmos	dgp fet, pfet33	High current, high speed
cor_resnd	opndres, sblkndres	High resistance
cor_respc	oppccres	High resistance
cor_resrr	oprrpres	High resistance
cor_reskq	kqres	High resistance
cor_cap	diffhavar, havar, dualmim, mim	High capacitance
cor_diode	divppn, sbd, diffncap, ncap, dgn cap	High current, high capacitance (sbd, ncaps)
cor_ind	tsv2, ind, symind, rflne, singlewire, singlecpw, coupledwires, coupledcpw, bondpad, bend, gap, open, radialstub, short, step, tee, yjunction	High Q

Table 6. Multiple Device Group Corner Parameters

Corner	Affected Parameter	Devices Affected in a Dominant Manner	Positive Corner Yields
cor_tox	thin oxide	nfet(tw), pfet, ncap, diffncap	High current and capacitance
cor_toxd	thick oxide	dgnfet(tw), dgp fet, dgn cap, nfet33(Tw), pfet33	High current and capacitance
cor_pc	lint (polysilicon width)	nfet(tw), dgnfet(tw), nfet33(tw), pfet, dgp fet, pfet33	High current
cor_rx	wint (STI width)	nfet(tw), dgnfet(tw), nfet33(tw), pfet, dgp fet, pfet33	High current
cor_noiN	NMOS flicker noise	nfet(tw), dgnfet(tw), nfet33(tw)	Low 1/f noise
cor_noiP	PMOS flicker noise	pfet, dgp fet, pfet33	Low 1/f noise

# Creating a Custom Corner File (design.scs)

```
parameters
+ mc_global      = 1
+ cor_npn        = 0
+ cor_pnp        = 0
+ cor_nmos       = 0
+ cor_pmos       = 0
+ cor_dgnmos     = 0
+ cor_dgpmos     = 0
+ cor_resnd      = 0
+ cor_respc      = 0
+ cor_resrr      = 0
+ cor_reskq      = 0
+ cor_cap         = 0
+ cor_diode      = 0
+ cor_ind         = 0
+ cor_tsv         = 0
+ cor_rx          = 0
+ cor_pc          = 0
+ cor_tox         = 0
+ cor_toxd        = 0
+ cor_noin        = 0
+ cor_noip        = 0
+ fet_dop_mis    = 1
+ fet_geo_mis    = 1
+ pc_nest         = 1
+ pc_orient       = 1
+ pc_dist         = 1
+ rx_dist         = 1
+ pc_nest_add    = 0.00
+ pc_orient_add   = 0.00
+ pc_dist_add    = 0.00
+ rx_dist_add    = 0.00
+ gstis          = 2
+ gwells          = 2
+ gsh             = 2
+ qii             = 2
+ esd_event       = 0
+ esd_exit        = 1
+ esd_extr        = 0
+ gbv             = 2
+ vcepdd          = 1.80
+ vcehb           = 3.55
+ fwdlim          = 0
+ waferthk        = 250u
```

Designer can set individual corner parameters as desired

Global switches

vcepdd: HP NPN C-E breakdown voltage warning level

vcehb: HB NPN C-E breakdown voltage warning level

The MOSFET-related parameter (cor\_tox\*, cor\_pc, cor\_rx, cor\_nmos, cor\_pmos) values in the design input file will be ignored whenever a fixed corner, other than the nominal process (tt), is selected.

The MOSFET bipolar, resistor, capacitor and inductor corner parameters in the design input file can be used in conjunction with the MOSFET fixed corners.

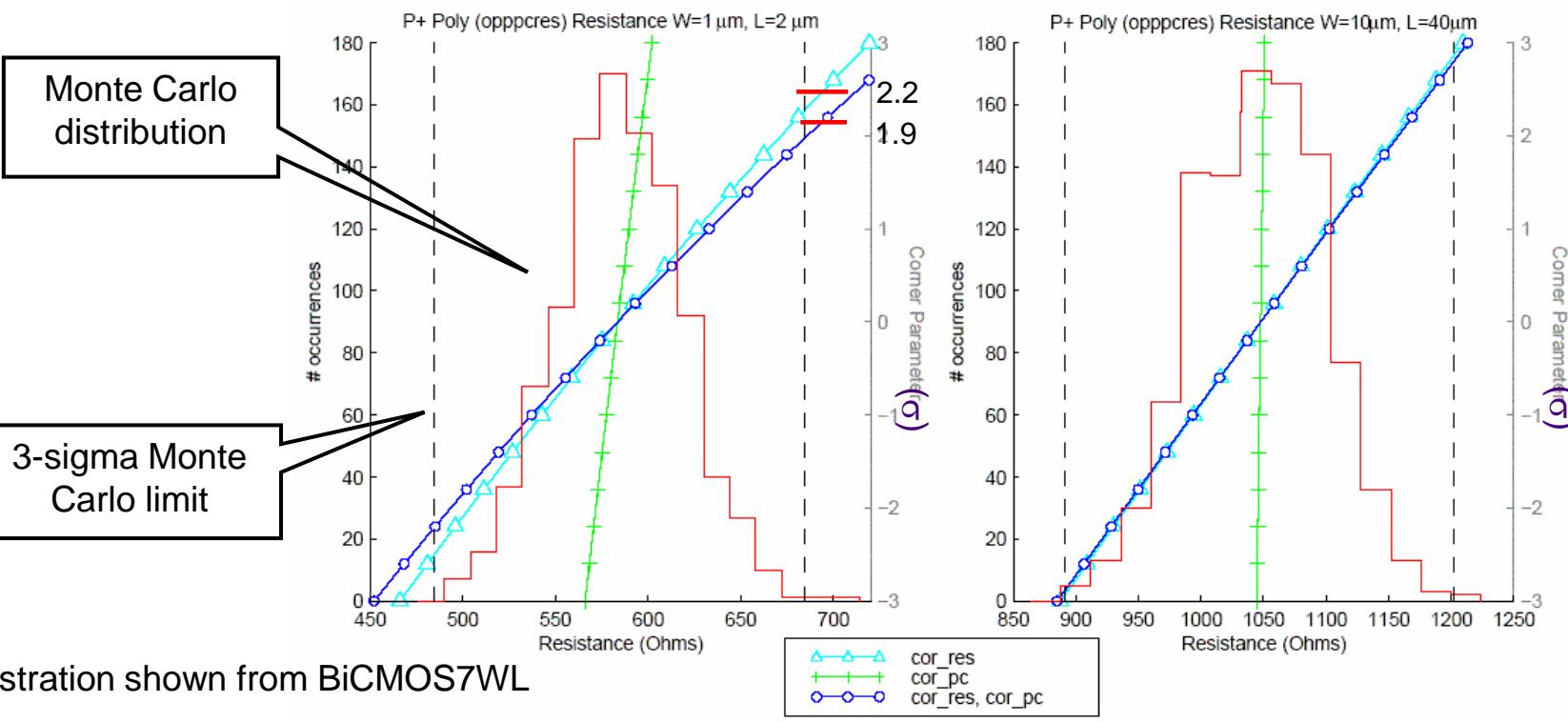
# Custom Corner Analysis Example\* - Resistor

## Small polysilicon resistor

- Sensitive to Sheet rho, End resistance, Polysilicon bias
- Need  $\text{cor\_res}$  and  $\text{cor\_pc} \sim 2$  to match  $3\sigma$  Monte Carlo

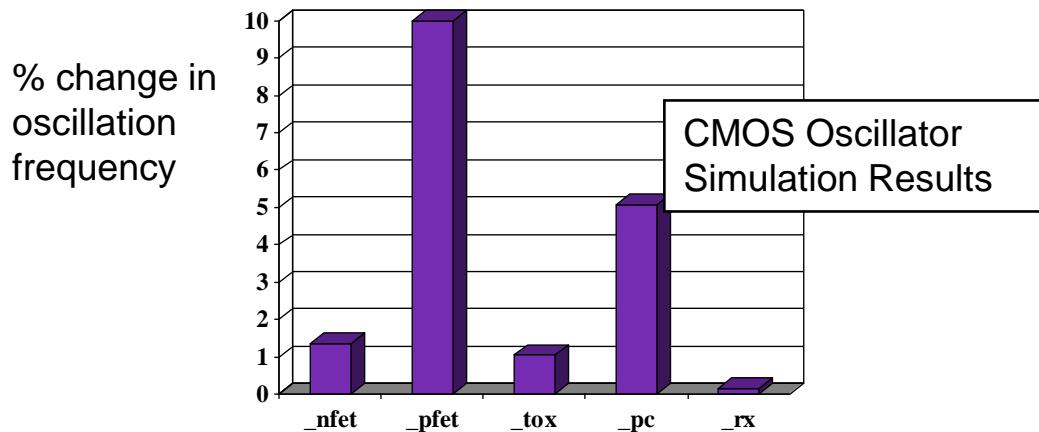
## Large polysilicon resistor

- Tolerance Sensitive only to sheet rho
- $3\sigma$  Monte Carlo matches  $\text{cor\_res}=3$



# Circuit Sensitivity Analysis

- Performance sensitivities to defined device groups and/or individual process parameters
  - Monitor circuit performance with a  $+\/-\sigma$  value for each parameter, one at a time
  - Determine which device groups drive circuit performance and in which direction
- Multiple corner combinations using different device groups highly recommended to define true "Best" / "Worst" Corners
  - e.g. "Fast MOSFETs" + "Low capacitors" or "Slow MOSFETs" + "Low Q inductors"
- Application notes: "Statistical and Corner Simulations" APN-000091 and "RF Reference Flow – 45RFSOI 12GHz LNA Example" APN-000213



CMRF6SF example

1-sigma Parameter Skew

A screenshot of the Global-FoundryView web interface. The left sidebar shows navigation links for PDK & Design Documents (Foundry: Design Technology Documents, IP Design Kits, Process Design Kits (PDK)), ASIC (ASIC News & Alerts, ASIC Design Kits (ASIC DK), ASIC Documentation), and a search bar. The main content area is titled "Design Technology Documents" and lists several application notes:

- APN-000095: C4 (Flip-Chip) I/O Placement Guidelines
- APN-000094: eFuse Principles and Implementation
- APN-000091: Statistical and Corner Simulations for RF/Analog IC Designs (highlighted with a yellow arrow)
- APN-000083: C4 (Flip Chip) ball sizes offered in Fabs 9 & 10

The "APN-000091" entry is highlighted with a yellow box and a red arrow pointing to it. The page also features a banner image of a cleanroom and a navigation bar with links like Home, Training Material, Notifications, Accounts, Contacts, My Devices, My Wafers, Products & Services, and PDK & Design Documents.

# Corner Analysis: A Step by Step Example

# Hints for Non-statistical Simulation (Corner Simulation) Settings

- Let `fixed_cor_sw = 0` to enable custom corner parameters controlled by user settings
- Specify all the process model parameters (`cor_*`)

These parameters can take values from a continuum of values between -3 and +3. It is the user's responsibility to ensure that the values specified are physically reasonable.

- Override global skew parameters if needed

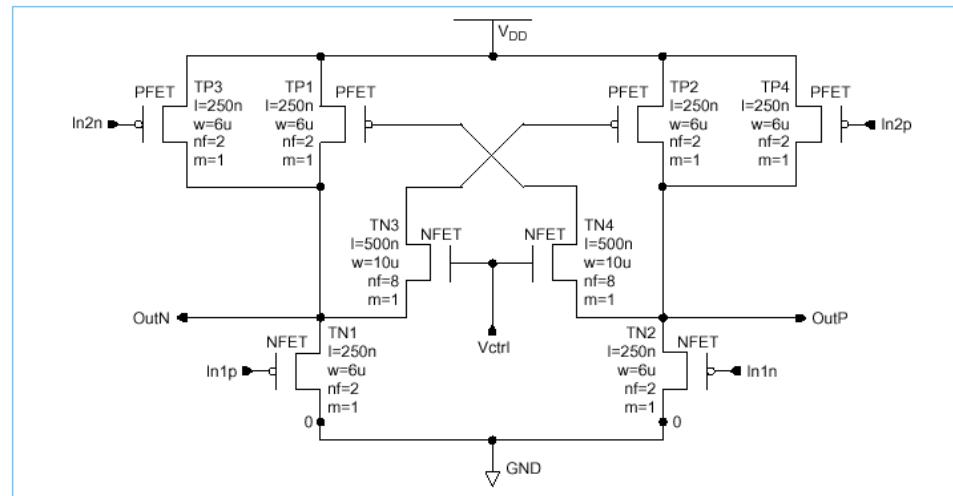
## 2.4.2 Non-Statistical Simulations

Table 14. Example of non-statistical simulation with custom user corner parameters enabled

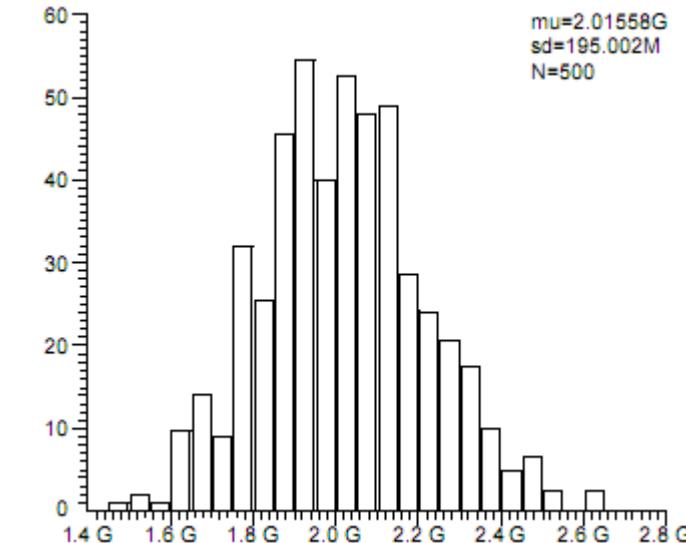
Control	Setting	Effect
mc_global	0	Non-statistical simulation. Parameter values are skewed in accordance with the <code>cor_*</code> settings. <code>cor_rx</code> and <code>cor_pc</code> move all FET channel length and widths together.
fet_dop_mis	0	
fet_geo_mis	0	
pc_nest	1	
pc_orient	1	
pc_dist	1	
rx_dist	1	
corner option	tt	
<code>cor_*</code>	-3 to +3	

# Custom Corner Analysis\* – Step 1

- Run Monte Carlo to determine 3-sigma performance for the circuit
  - Running Monte Carlo is the only way to correlate the corner with reality



VCO Delay Cell used in the Example



Monte Carlo Results ( $f_{osc}$ )

\*See Application Note “Statistical and Corner Simulations” on the Global-FoundryView Website

# Custom Corner analysis – Step 2

- Run sensitivity analysis to find the direction of corner parameter movement for worst case/best case directions
  - Provides sensitivity of the circuit to device types

Sweep each corner parameter from -1 to +1 to determine direction of sensitivity

\* Table 4. Corner Parameter Sensitivity of the VCO Oscillation Frequency

Corner Parameter	Change in $f_{osc}$ for Corner Parameter Change	
	From 0 to +1 (GHz)	From 0 to -1 (GHz)
cor_nmos	+ 0.037	- 0.032
cor_pmos	+ 0.219	- 0.205
cor_tox	+ 0.021	- 0.021
cor_pc	+ 0.102	- 0.094
cor_rx	+ 0.003	- 0.003
cor_res	0	0
cor_cap	0	0

\* From the Application Notes

Highly sensitive to  
cornr\_pfet

# Custom Corner analysis – Step 3

- Align the corner parameter signs for worst/best case

Is the shift positive, negative, or none?

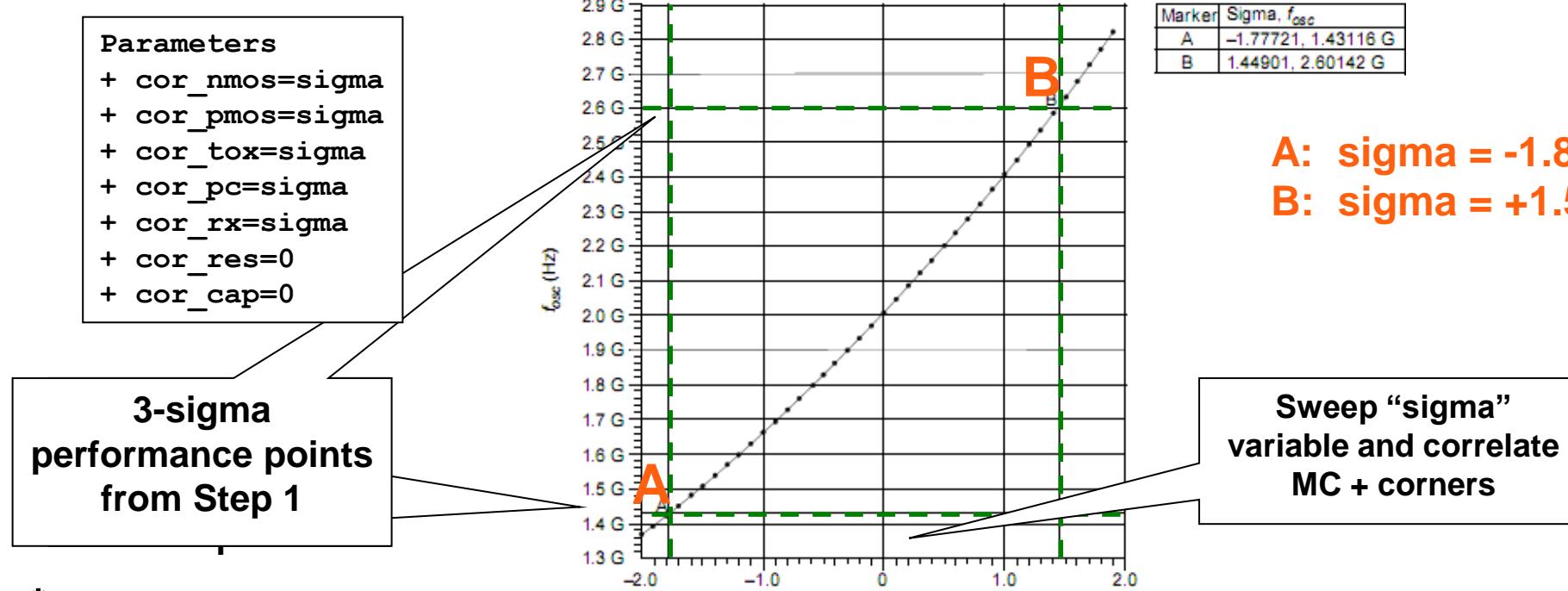
- \* *Table 5. Corner Parameters Signs Determined for the VCO Oscillation Frequency.* Signs are determined using the positive and negative performance shifts from *Table 4*.

Corner Parameter	Corner Parameter Sign Required for:	
	Positive Performance Shift	Negative Performance Shift
<b>cor_nmos</b>	+	-
<b>cor_pmos</b>	+	-
<b>cor_tox</b>	+	-
<b>cor_pc</b>	+	-
<b>cor_rx</b>	+	-
<b>cor_res</b>	None	None
<b>cor_cap</b>	None	None

- \* From the Application Notes

# Custom Corner analysis – Step 4a

- Set all relevant corner parameters to a variable (i.e. “sigma”)
  - cor\_nmos = sigma; cor\_pmos = sigma; cor\_pc = sigma; etc.
  - Sign determined in step 2: +sigma or -sigma
- Sweep variable (sigma) from -3 to +3
- Determine the value of (sigma) that matches the +3 / -3 performance from Monte Carlo (step 1)



\* Figure comes from the Application Notes

# Custom Corner analysis – Step 4b

- Create custom corner file to correspond to the specific corner
  - VCO\_fosc\_up3, VCO\_fosc\_down3

\* *Table 6. Corner Parameter Values for UP and DOWN Corner Simulations of the CMOS Oscillator*

Corner Parameter	Values of the Corner Parameters for:	
	UP Corner Simulation	DOWN Corner Simulation
cor_nmos	+ 1.5	- 1.8
cor_pmos	+ 1.5	- 1.8
cor_tox	+ 1.5	- 1.8
cor_pc	+ 1.5	- 1.8
cor_rx	+ 1.5	- 1.8
cor_res	0	0
cor_cap	0	0

VCO\_fosc\_up3  
Parameters  
+ sigma=1.5  
+ cor\_nmos=sigma  
+ cor\_pmos=sigma  
+ cor\_tox=sigma  
+ cor\_pc=sigma  
+ cor\_rx=sigma  
+ cor\_res=0  
+ cor\_cap=0

VCO\_fosc\_down3  
Parameters  
+ sigma=-1.8  
+ cor\_nmos=sigma  
+ cor\_pmos=sigma  
+ cor\_tox=sigma  
+ cor\_pc=sigma  
+ cor\_rx=sigma  
+ cor\_res=0  
+ cor\_cap=0

\* From the Application Note

# Wafer-Specific Simulation

- Wafer-specific override capability allows users to specify the inline measurement results in a separate file within the model directory, “wafer.scs”.
- Use of these wafer parameters is triggered by setting the k\_wafer switch equal to 1 (one) in this input file.
- Default setting for k\_wafer is 0 (zero).
- User should enter parameter values as they appear in the engineering snapshot of interest, i.e. without units.
- Defaults in the wafer file shipped with the design kit correspond to the nominal process (target) values.
- See Section 1 in Model Reference Guide for more details

# **Wafer-Specific Simulation - Wafer-specific model override**

- Feature may be used to correlate circuit level simulation to hardware measurements on prototype parts.
  - Wafer-specific model override provides an aid for users to take a minimal set of device measurement data from the kerf process control line monitors (kerf PCM) and then translate them to the internal model parameters to approximate, to the first-order, the measured device characteristics in the nominal simulation.
- **Wafer-Specific simulation enabled only for the Spectre/Hspice model library.**
  - Modify the switch “k\_wafer” in wafer.scs (wafer.inc) to enable the override capability.
    - By default this feature is disabled with “k\_wafer” = 0.
  - Modify values of Wafer-Specific Model in wafer.scs according to specific wafer PCM data of users’ interest.
  - Modified wafer.scs filename and path need to be specified in simulator setup
- **Use of the wafer-specific overrides and the other process corner analysis is mutually exclusive.**
  - Users should make sure that the fixed corner selection is set to tt.
  - A Monte Carlo simulation and a non-TT fixed corner simulation with k\_wafer=1 are not supported.
    - Users should make sure k\_wafer is set to 0 in the wafer.scs (wafer.inc) file.

# Creating a Wafer-Specific Simulation File(wafer.scs)

```
*****
*
* Wafer-specific overrides for a subset of model / process parameters are
* available and may be used to aid in the correlation of circuit level
* simulation to hardware measurements on prototype parts. These first-order
* parameters are defined using a minimal number of measurements on the inline
* kerf (PCM) monitors.
*
* Notes and Definitions:
*
*   k_wafer    Switch to enable (1) or disable (0) use of the
*              wafer-specific override parameters
*
* Use of this wafer-specific methodology and corner analysis is mutually
* exclusive. All corner parameter inputs are ignored when the k_wafer switch
* is enabled (k_wafer=1). Likewise, when the k_wafer switch is turned off
* (k_wafer=0), the wafer-specific parameter inputs are ignored in favor of
* any corner parameter values.
*
* Enter parameter values as shown in the wafer snapshot of interest. The
* defaults given here correspond to the expected nominal (target) values.
*
*****
*
parameters
+ k_wafer      = 0          // Switch to activate wafer specific parameters
*
* NPN Parameters
+ k_hpnpvbe    = 0.728    // HP NPN Vbe, default = 0.728 V
+ k_hpnpbeta   = 460       // HP NPN Beta, default = 460
+ k_hpnprdb    = 4000      // HP NPN Pinch Rdb, default = 4000 ohm/sq
+ k_hpnpcbe   = 8.0        // HP NPN B-E Cap, default = 8.0 fF/um^2
*
+ k_hbnpvbe    = 0.730    // HB NPN Vbe, default = 0.730 V
+ k_hbnpbeta   = 400       // HB NPN Beta, default = 400
+ k_hbnpnrb    = 2500      // HB NPN Pinch Rdb, default = 2500 ohm/sq
*
* VPPN Parameters
+ k_vpnpvbe    = 0.790    // VPPN Vbe, default = 0.790 V
+ k_vpnpbeta   = 230       // VPPN Beta, default = 230
*
* NFET Parameters
+ k_tox_nfet   = 3.03     // NFET Large Tox, default = 3.03 nm
+ k_vtlin_nfet = 0.17     // NFET 5x5 Vtlin, default = 0.17 V
+ k_idlin_nfet = 4.0       // NFET 5x5 Idlin, default = 4.0 uA/um
+ k_idsat_nfet = 525      // NFET 5x0.12 Idsat, default = 525 uA/um
+ k_colap_nfet = 0.35     // NFET Overlap Cap, default = 0.35 fF/um
+ k_cjunc_nfet = 1.05     // NFET Junction Cap, default = 1.05 fF/um
```

Change Switch from 0 to 1 to  
activate wafer spec parameters

Designer can set individual wafer  
parameters as desired



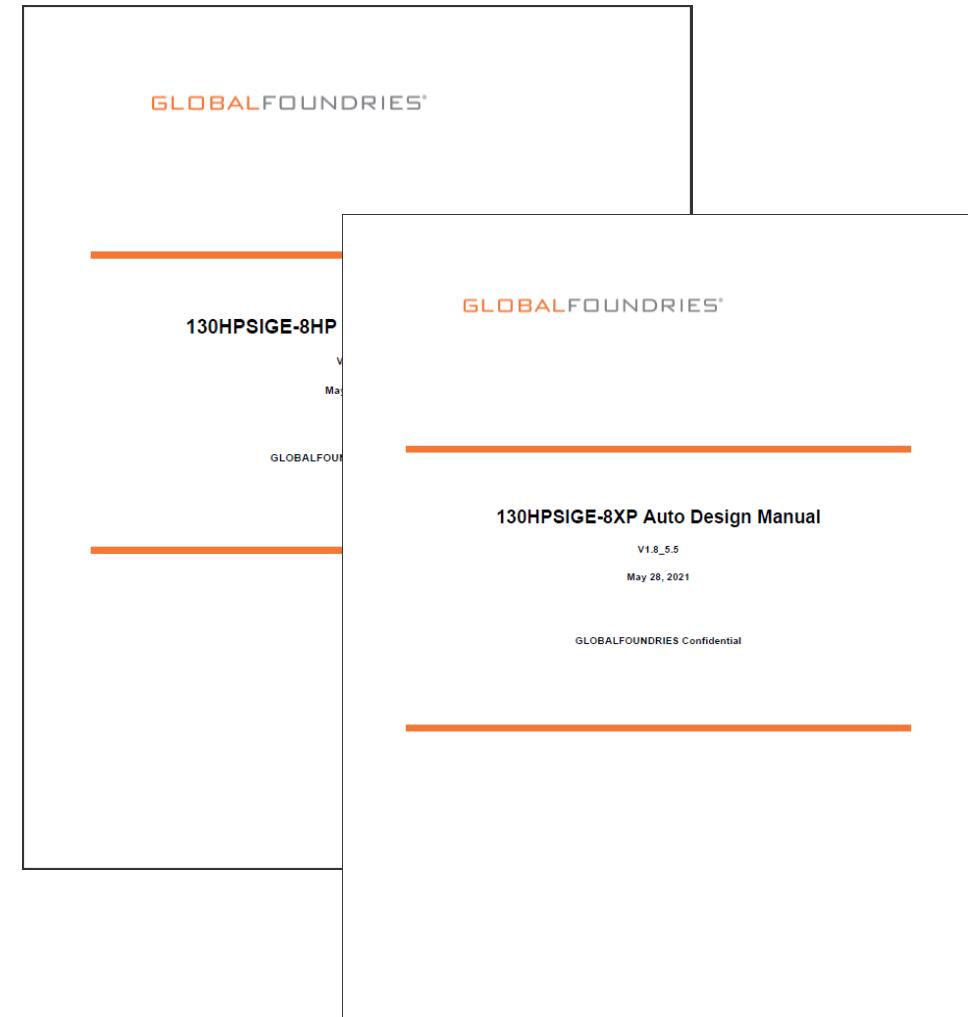
# **Design Layout Considerations**

# BiCMOS8HP/8XP Layout Topics

- Design Manual
- Physical Design/Mask Levels
- Design/Ground Rules
- Geometry Restrictions
- Process Control Images
- Complex Groundrules:
  - Floating Gate/Antenna Rules
  - Copper Dendrite Formation
  - Pattern Density Requirements
- Wiring Current Density and Electromigration
- Latch Up (LU) Prevention
- ESD Layout Rule Checking
- Common Techniques for Noise Minimization
- MIM Layout Considerations
- Inductor Layout Considerations
- Matching and Ratio Control
- Compact Designs
  - NWells at Same Potential
  - Butted Junctions
  - FETs sharing Common Active Region
  - MIM and Resistor Density Optimized Layouts
- Design for Productivity/Yield Enhancement
- Supported Cadence Feature - Multipart Path, Vias through techfile

# Design Manuals

- **Technology Reference Designations**
  - PDK: bicmos8hp (bicmos8xp)
  - G-FV : 0.13um/130HPSIGE-8HP-8XP
- **Design Manuals**
  - 8HP
    - Document Title : 130HPSIGE-8HP Design Manual
    - Document ID #: DM-000418
  - 8XP
    - Document Title : 130HPSIGE-8XP Design Manual Addendum
    - Document ID #: DM-000420
      - In addition to this, need BiCMOS8HP Design Manual DM-000418 also
- **Design Manuals located in [\\$GF\\_PDK\\_HOME/bicmos8hp\(8xp\)/doc](#)**



# BiCMOS8HP Design Manual Table of Contents

- **Structure consistent across technologies**

- 1: Technology Introduction
- 2: Physical Layout Information
- 3: Physical Design Rules
- 4: Electrical Parameters and Models
- 5: Reliability Design Rules and Models
- 6: Electrostatic Discharge (ESD) Protection
- 7: Design for Manufacturability
- Appendix A. Guidelines for Optimal Model-Hardware Correlation
- Appendix B. Total Standby Current (Idd)
- Appendix C. Design Hierarchy Guidelines
- Appendix D. Rule Syntax (Definitions)
- Appendix E. Definitions of Process-Related Terms
- Appendix F. Migration into Future Technologies
- Appendix G. Design Preparation .
- **Appendix H. Pattern Fill Rules**
  - H.1 Estimated Pattern Density Generation
  - H.2 Recommended Design Practices Related to Generated FILL and HOLES Shapes
- Appendix I. MxPLANE Information
- Appendix J. NO\_BAT Rules
- Appendix K. Decoupling Capacitor
- Appendix L. Change List

130HPSIGE-8XP Design  
Manual Addendum has  
design rules etc.,  
information specific to  
8XP only devices

# Design Levels: Physical Design Masks Information

## Design Manual Section 2.0

- **Manufacturing Design Grid : 0.01 μm**
  - Design database uses 0.001μm grid
- **Layer information, description given in Design Manual Sections 2.2-2.10**
  - 2.2: **Mask Level Definitions - Required mask levels. Drawn by designers.** RX, PC, NW, NR, CA etc.
  - 2.3: Design Services and Data Preparation Mask Levels - for GLOBALFOUNDRIES use only.
  - 2.4: KERF Dummy Design Levels - These levels are for GLOBALFOUNDRIES use only
  - 2.5: Dummy Design Levels and Utility Levels. **Drawn by designers.** BFMOAT, DIODE, ESDUMMY, etc.
    - *NOT MASKS but needed for Booleans, data prep and other checking*
  - 2.6: AutoHP: Dummy Design Levels and Utility Levels - Automotive Design
  - 2.7: Masks for Nondesign Levels
  - 2.8: Level Generation and Design Preparation
  - **2.9: Mask Metalization Options**
  - 2.10: **Truth Table**
- **Truth tables (2.10) list required drawn levels, derived levels, masks for all devices**

# Physical Design Preparation Example

- Devices use **Drawn Mask Levels**, **Dummy Design Levels** (drawn), and **Derived Mask Levels** (generated)

	NFET	PFET	NPN	Design Manual
<b>Drawn Levels</b>	<b>RX, PC, CA</b>	<b>RX, NW, PC, BP, CA</b>	<b>(DS, NS) RX, DT, RN, BB, PX, BX, (CX), LE, EX, NP, PB, CA, CE</b>	Table 2-1 Section 2.2
<b>Derived Levels</b>	<b>BH</b>	<b>BF, PH, BN, BP</b>	<b>BT, BF, BH, PF, PQ,</b>	Table 2-6 Section 2.7
<b>Dummy Levels</b>	<b>None</b>	<b>None</b>	<b>BPERI</b>	Table 2-4 Section 2.5

# Design Geometry Restrictions (S-Rules)

## Design Manual Section 2.11

- S1: The design grid must be an integer multiple of 0.01 um
- S2: Shapes with acute angles are not allowed
- S3: Shapes that intersect and overlap themselves are not allowed (shapes that abut themselves are permitted)
- S4: Shapes that cross themselves are not allowed (also known as bow ties and re-entrant shapes)
- S5: Shapes with zero area are not allowed
- S6: Only shapes that are orthogonal or on a 45 degree angle are allowed except in alphanumeric labels
- S7: Shapes that are formed with two lines that never intersect are not allowed
- S8: Shapes that are formed with the line op codes or path op codes are not allowed to have 45 degree bends – only orthogonal lines are allowed
- S9: Line end segments formed with line op codes or path op codes must have a length to width ratio > 0.5000
- S10: Text data is not allowed on any mask build layers
- S11: Path End Type 3 prohibited

All S-Rules are Class a rules. No waivers are granted. Design must pass them all.

# Reserved Levels

## Reserved Level Layout Rules **2.11.1**

These rules correspond to the Reserved Levels described in Table 2-2: Design Services and Data Preparation Mask Levels (Restricted) on page 38 and KERF Dummy Design Levels on page 39.

## AutoHP: Reserved Level Layout Rules - Automotive Design **2.11.2**

These rules correspond to the Reserved Levels described in Table 2-2: Design Services and Data Preparation Mask Levels (Restricted) on page 38 and KERF Dummy Design Levels.

# Design Rule Classification

## Class a: Manufacturing Critical – Most severe

Possible Impact to production tools or processes, Kerf/WAC, Mask Build

Examples: Min Width/Space/Area, Density, Geometry

## Class b: Significant Yield/Reliability Risk (30-90% yield impact) – Medium severity

Examples: Overlap spacing, Wide Metal Spacing

## Class c: Moderate Yield/Reliability Risk (5-30% yield impact) – Low severity

Examples: Inductor rules, Antennae rules, ESD rules

## Class d: Recommended Rules (Incremental yield enhancement) – Lowest severity

More conservative recommendations for line/space rules

Classification  
Column

Table 3-1. Polysilicon and Isolation Layout Rules (Part 1 of 7)

Rule	C I a s s	Notes	Description	Design	Wafer	Tol
1	a	-	PC width over RX for NFET device Lp.	≥ 0.12	0.092 <sup>1</sup>	0.022 <sup>1</sup>
2	a	-	PC width over RX for PFET device Lp.	≥ 0.12	0.092 <sup>1</sup>	0.022 <sup>1</sup>
3	c	-	PC width over RX for 45 degree NFET device Lp.	≥ 0.127	0.0990 <sup>1</sup>	0.029 <sup>1</sup>
3R	d	-	PC width over RX for 45 degree NFET device Lp.	≥ 0.140	0.1120 <sup>1</sup>	0.029 <sup>1</sup>

# AutoG: Design Rule Classification - Automotive Design

Column named: "Class", adjacent to "Rule" column, specifies Manufacturability Rule Classification with respect to DRC violations:

- **Class a rules:** Manufacturing Impact
  - No waivers will be granted for class a rule violations for AutoPro parts with the AUTO:dg marking layer
- **Class b rules:** Yield and Reliability Impact
  - No waivers will be granted for Class b rule violations for AutoPro parts with the AUTO:dg marking layer

## 3.4 AutoG: Polysilicon and Isolation Layout Rules - Automotive Design

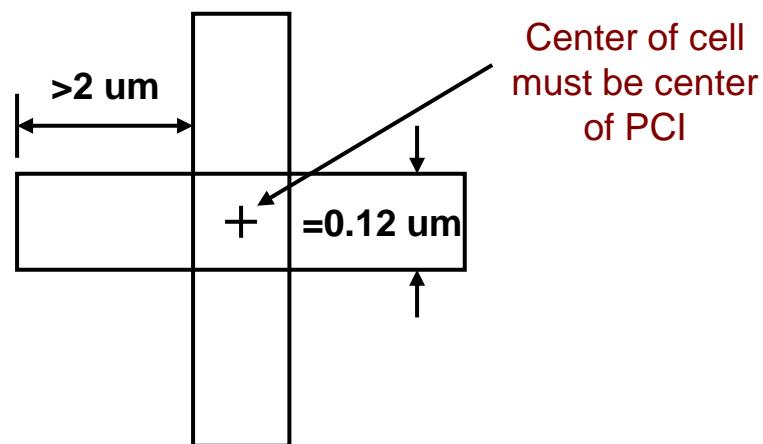
Table 3-2: Polysilicon and Isolation Layout Rules - Automotive Design

Rule	Class	Note	Description	Operator	Value	Wafer	Tolerance
A_120a	b	-	Only 45 degree PC gate vertices are allowed over RX. ## Automotive.	-	-	-	-
A_120c	b	-	PC notch over RX. ## Automotive.	$\geq$	0.33	-	-
A_123a	b	-	Only inside 45 degree RX vertices are allowed under (PC not over GRLOGIC). ## Automotive.	-	-	-	-
A_125	b	<sup>1</sup>	PC over RX must divide the RX into two or more diffusions. ## Automotive.	-	-	-	-
A_132	b	-	(PC intersect RX) must have an area ( $\mu\text{m}^2$ ). ## Automotive.	$\leq$	230	-	-

# Mask Process Control Images (PCI marks)

- PCIs are added into the PC (polysilicon) mask for line-width and registration control during PC mask making process.
- The PCI requirement is waived on any chip with a width or length shorter than 6mm on any side
- 40 PCIs required (Rule 784)
  - See Section 3.12 in Design Manual for more PCI details.
- PCI cells in dedicated PCING design layer “PCING” DG”
- PCI cell name must contain upper case character string “IPCI”
  - “IPCI” cannot occur in other cell names
- Layout cell “IPCI\_MEAS” provided in PDK

Shape must have 4 identical legs as shown and be  $\geq 0.42$  um from the nearest PC, PCING, RX, NP, CA, CABAR, CEBAR shape and  $\geq 1.02$  um from PB.

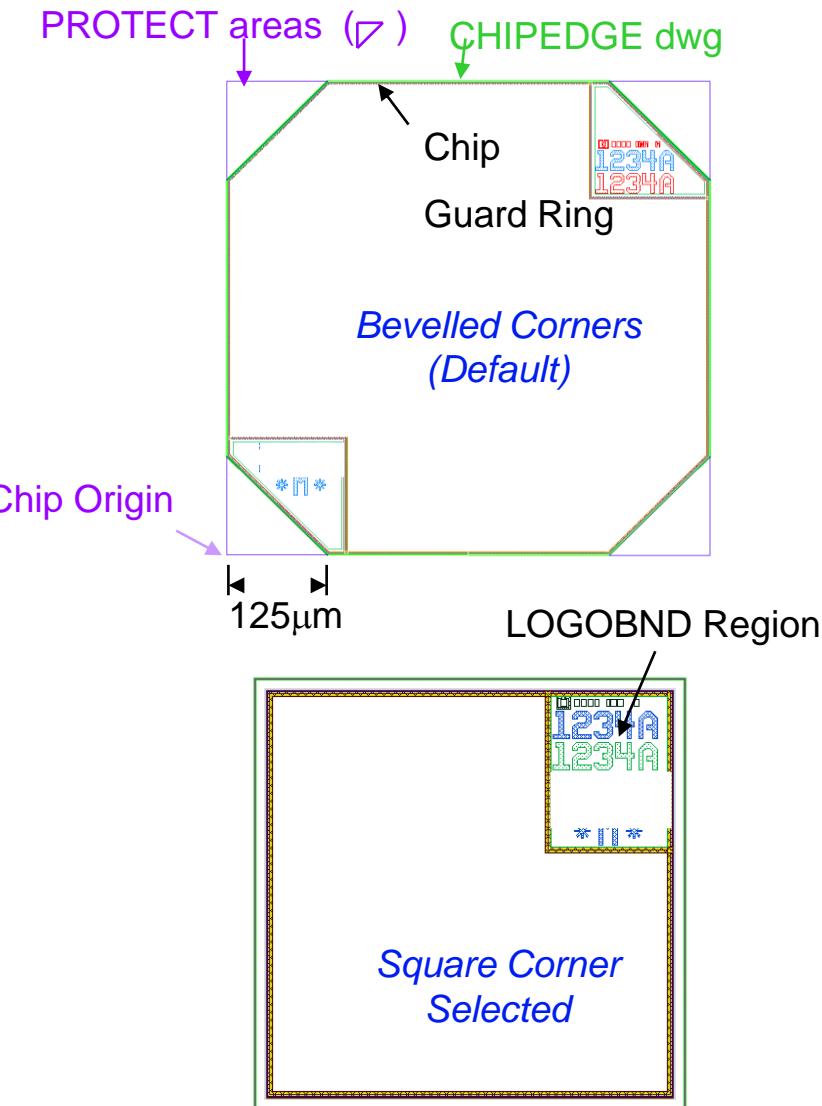


# Chip Pcell (chipguardring)

- Provides chipedge, crackstop, chip guard ring, logo and part number area
- Logo field with desired data
  - Use the alpha characters supplied in kit
  - Logo area does not receive pattern fill
- Rectangular or beveled edges
  - No data allowed in the beveled PROTECT areas
- Chip Origin ( $x=0, y=0$ ) must be at the lower left corner of the chip
- Maximum chip size
  - x: 20.00 mm
  - y: 20.00 mm
  - CHIPEDGE must be even multiples of 0.01  $\mu\text{m}$  and must be on grid.

## Pcell CDF Options Include:

Length, Width  
Square corner (Bevelled if unselected)  
Remove Crackstop  
Segmented  
Add Custom Logo area

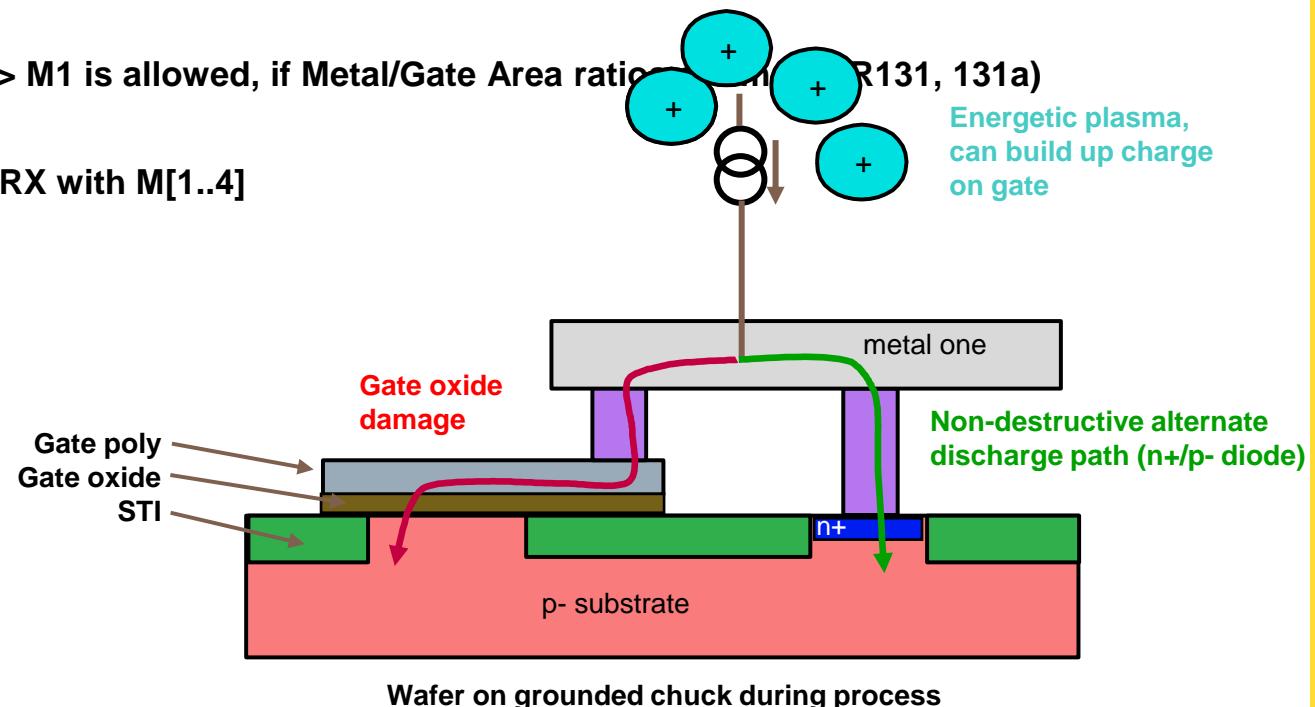


# BiCMOS8HP/8XP Complex Ground Rules

- Design Manual
- Physical Design/Mask Levels
- Design/Ground Rules
- Geometry Restrictions
- Process Control Images
- Complex Groundrules:
  - Floating Gate/Antenna Rules
  - Copper Dendrite Formation
  - Pattern Density Requirements
- Wiring Current Density and Electromigration
- Latch Up (LU) Prevention
- ESD Layout Rule Checking
- Common Techniques for Noise Minimization
- MIM Layout Considerations
- Inductor Layout Considerations
- Matching and Ratio Control
- Compact Designs
  - NWell at Same Potential
  - Butted Junctions
  - FETs sharing Common Active Region
  - MIM and Resistor Density Optimized Layouts
- Design for Productivity/Yield Enhancement

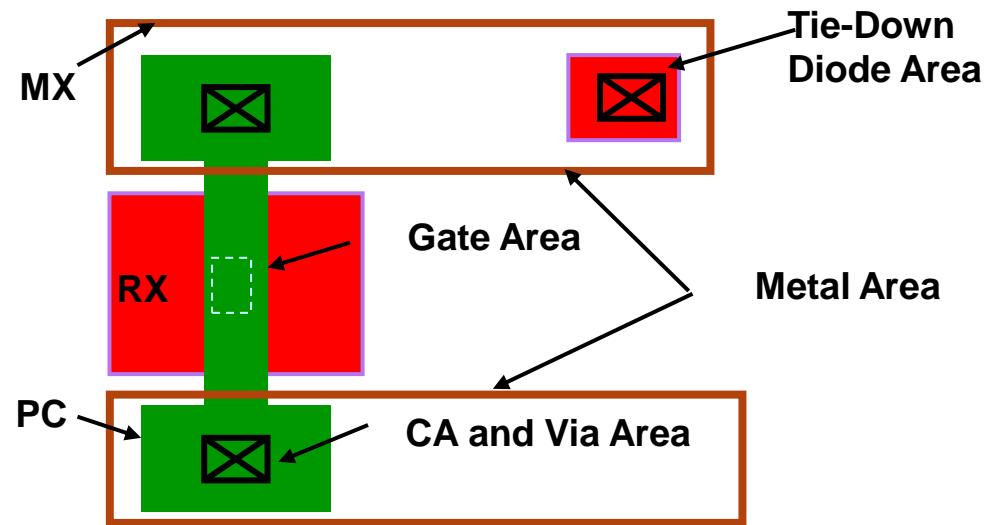
# Floating Gate / Antenna Rules

- Non uniform plasma in reactive ion etch and plasma assisted process can lead to gate charging
  - PC, metal, contact & via etch; dielectric deposition
  - RX connected to gates provide a discharge path
  - RX diodes are conductive at wafer processing temperatures
- Floating gate = PC intersecting RX that is not connected to valid RX tie-down
- Charging can result in threshold shift, hot carrier degradation, gate dielectric leakage and increased oxide reliability failures
- Require all gates tied to RX by M1 deposition, however > M1 is allowed, if Metal/Gate Area ratio < 1.4 (GR131, 131a)
- Gates connected to VL (Cu thin to thick via) must tie to RX with M[1..4]
  - Total (PC area/ Gate area) and (perimeter PC not over RX)/ Gate area) ratios need to be met (GR130a, 130c)
  - Metal/Gate Area ratios are checked on a level by level basis, not cumulative (GR131, 131a, 131b, 131c)



# Antenna Rules

- Antenna Rules are defined as ratios



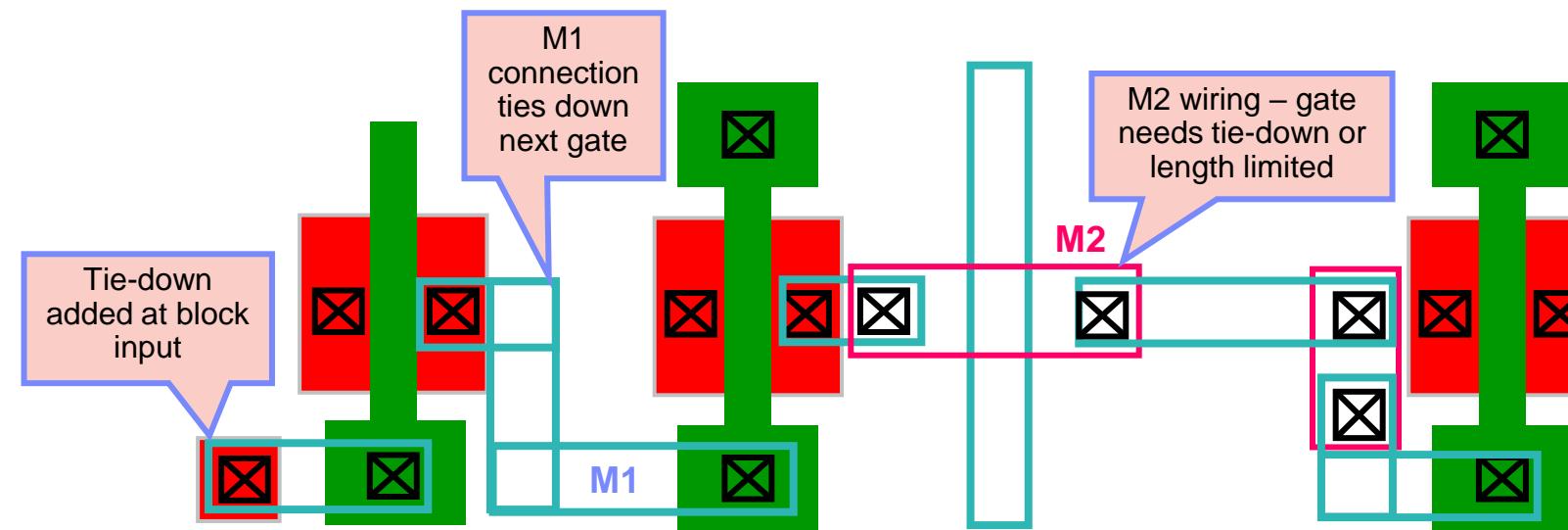
- Recommended that all gates be tied down to a diode at M1
  - All gates must be tied at M1
  - Gates tied to substrate contacts do not need to meet the tie-down diffusion area requirements.

- **Antenna Ratios**

- Rule 130a : PC Area / Gate Area  $\leq 100$
- Rule 130c: PC Perim (not RX)/ Gate Area  $\leq 210$
- Rule 131 : Thin Metal Area / (Gate Area + 5x Diffusion Area)  $\leq 150$
- Rule 131a : Thick Metal Area / (Gate Area + 2x Diffusion Area)  $\leq 150$
- CA and Vias limited for nets connected to gate (rules 131a, 131b, 131c)
- Applies for all PC over RX structures
  - FETs, pcdcap & mosvar
- **PC Area/Shape  $\leq 230\mu\text{m}^2$  (Recommended  $\leq 45\mu\text{m}^2$ ) – Rule 132**

# Floating Gate / Antenna Layout Considerations

- Within local circuit blocks
  - Use M1 wiring for FET to FET connections where possible
    - Drain of prior stage acts as tie-down diode
  - Add tie-down diode at circuit block input gates



- For global wiring
  - Add tie-down diodes as required to meet antenna rules
  - Via up/down to break large nets (antenna rules not cumulative)

# Metal Antenna Rule – GR131 Metal Area

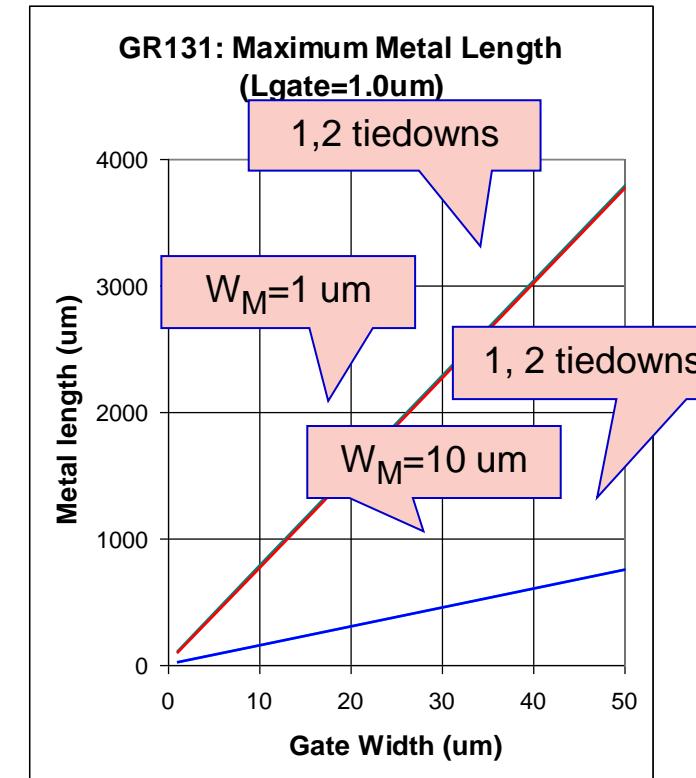
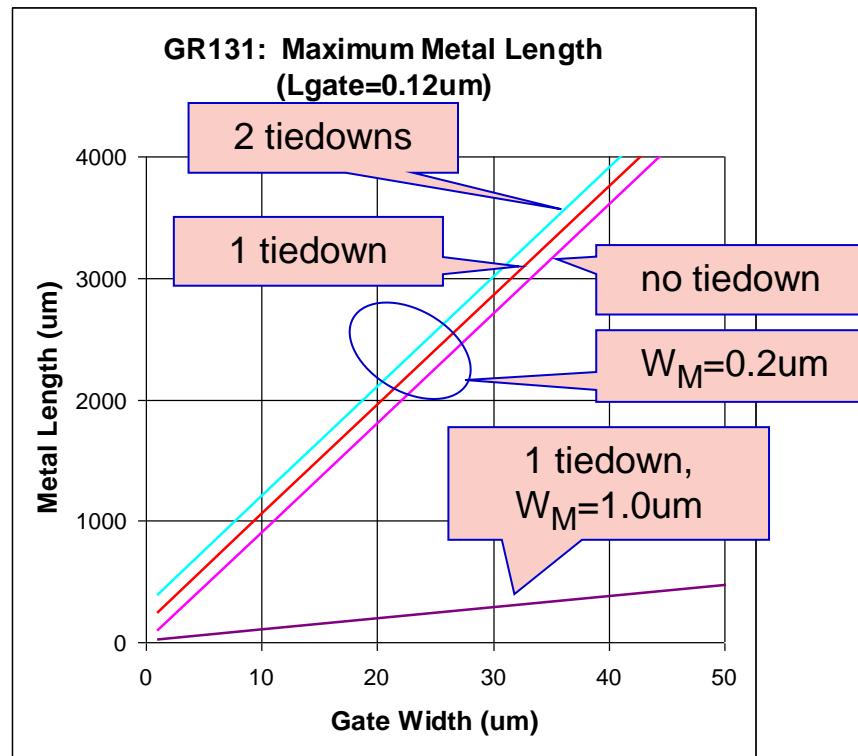
## Example Maximum Thin Metal Allowable Length

$$A_M \leq 150 * (A_G + 2 * A_D)$$

$$L_M \leq 150 * (L_G * W_G + 2 * A_D) / W_M$$

where  $A_M$ ,  $A_G$ ,  $A_D$  are area metal, gate, diffusion

Checked for each metal level individually



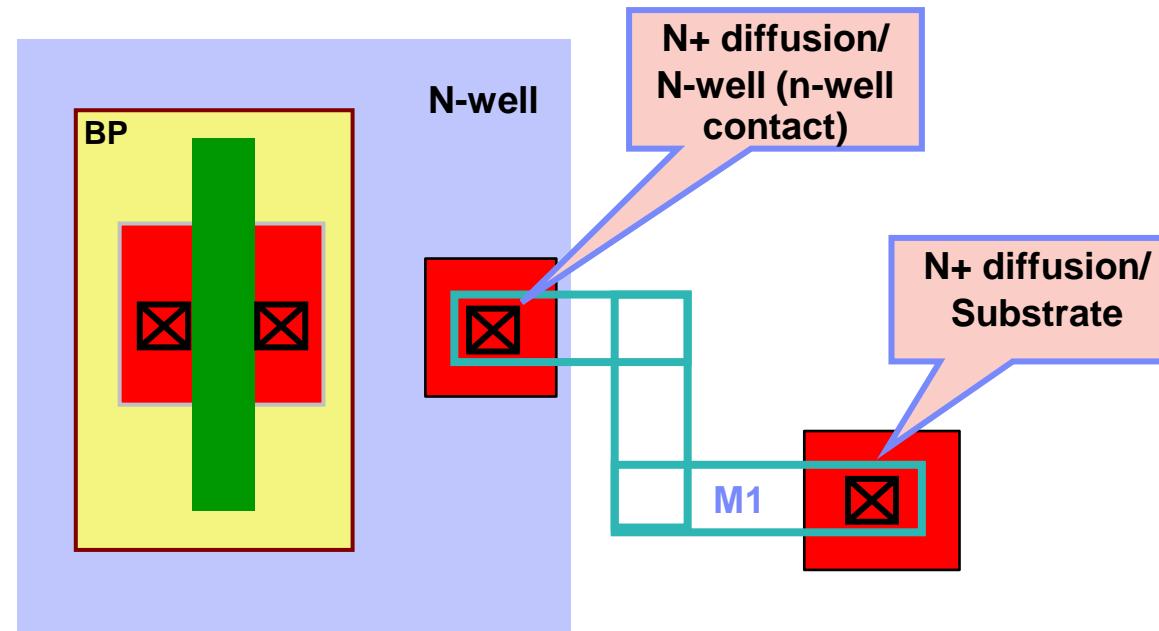
For A<sub>D</sub> = 0.1 μm<sup>2</sup>

# N-well & Triple Well Charging

- N-Well have high breakdown and low leakage at processing temperatures
- Charged by metal lines tied to the well
- Produces high electric field on devices with tied down gates
- Tie down required to prevent charging of nwell with respect to PC gate
- Every Nwell containing a gate must satisfy (Rule 134 / T3W134):
  - a RX diffusion in the N-well and triple wells must be connected to a RX diffusion in the substrate by the time M1 level is complete - See illustration Rule 134 next chart

# N-well Tied Down (GR 134)

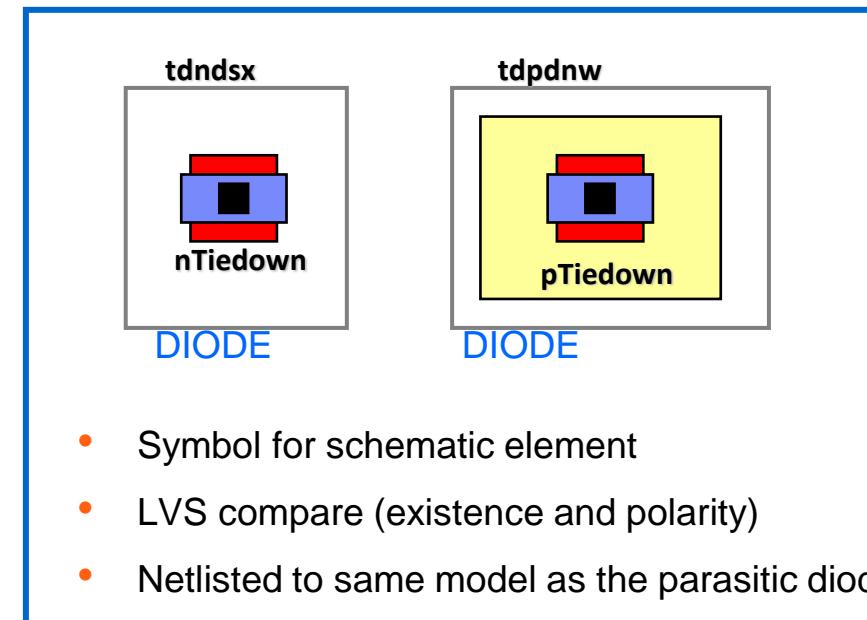
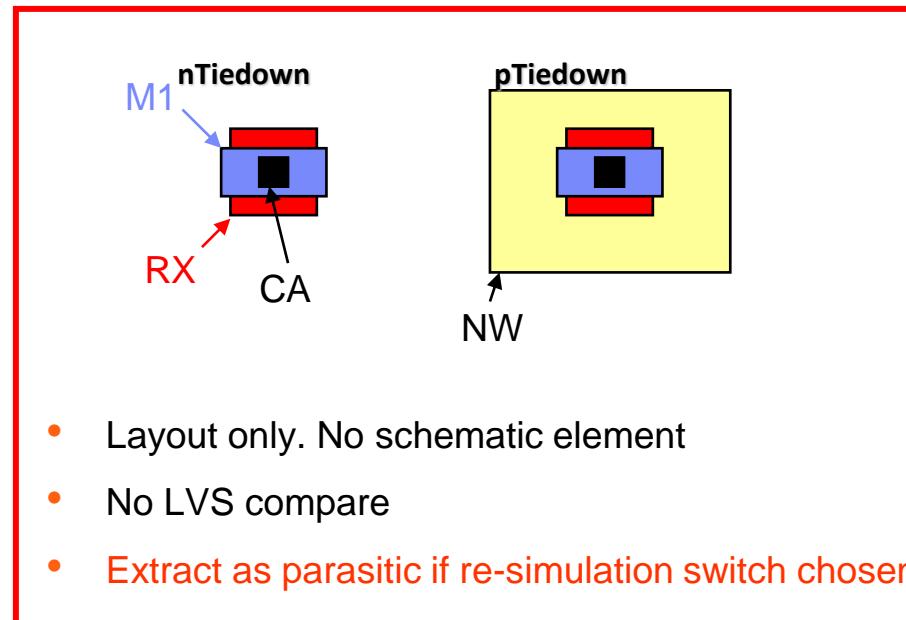
N-well tied down using N+ diffusion/N-well through M1 to N+ diffusion/substrate (GR 134)



# Tie-down Diodes (nTiedown, pTiedown)

## ▪ Tie-Down diodes

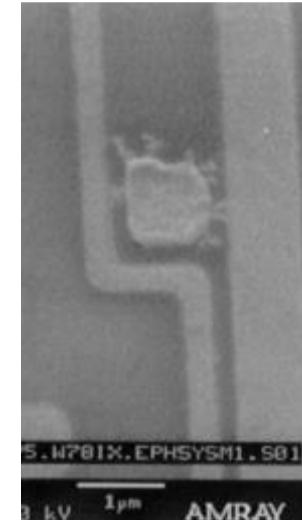
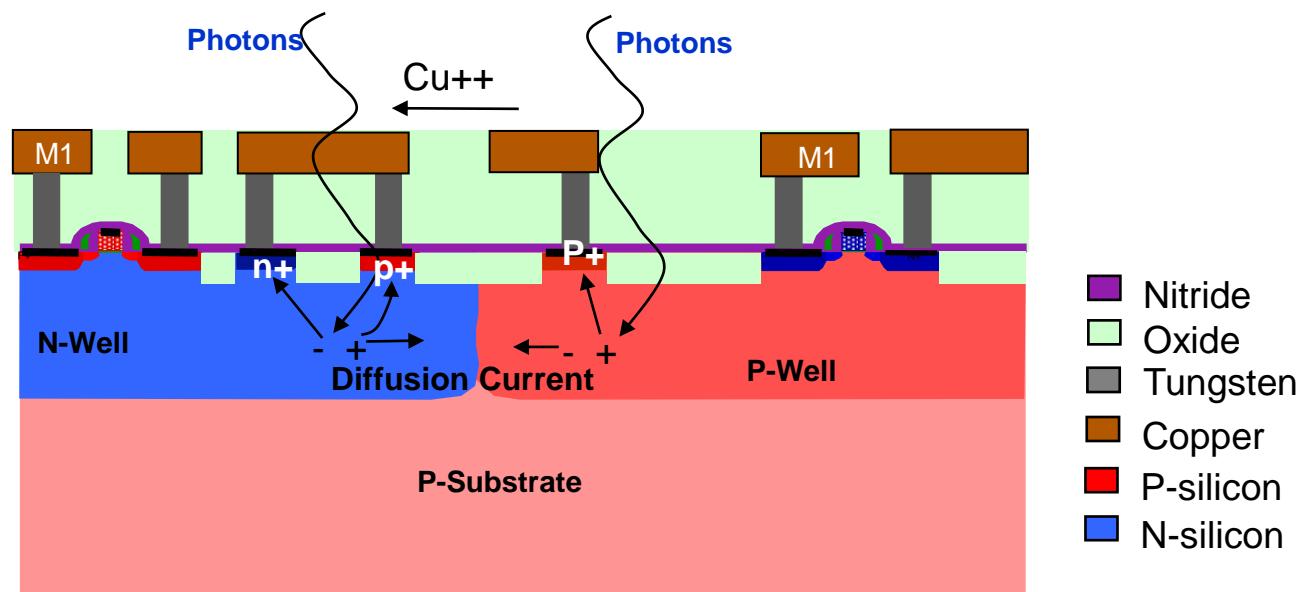
- Prevent in-process charge damage for gate and n-well (Antenna Rules)
- Option 1: Treat as parasitic elements
  - Use layout only cells nTiedown / pTiedown, extract as a parasitic diode for re-simulation from layout.
- Option 2: Treat as device enter in schematic and use in LVS comparison
  - Add “DIODE drawing” over cells nTiedown / pTiedown in layout.
  - Use symbol only cells tdndsx (n+ to pwell) / tdpdnw (p+ to nwell) in schematic



# Copper Dendrite Formation

- Yield/reliability sensitivity to metal shorts → Rules 594/T3W594, 595/T3W595
  - Photo-generated electron-hole pairs in N-well, P-well regions during processing
    - Electron-hole diffusion current in the silicon sets up potential difference
    - Metal connected to N-well contact charges negative
  - Current flows through electrolytic solution on the wafer
    - Results in de-plating and re-plating of copper - dendrite formation
      - Less concern if lower current density (more metal on N-well net beneficial)
      - Alternate path for holes in N-well to P+ in nwell (connected to N-well net) beneficial

dendrite formation



# Copper Dendrite Prevention Rules 594 & 595

- Rule 594: For nets that touch an N-well contact area ratio

- $[20*(M1..4) + (((RX \text{ over } BP) \text{ over } NW) \text{ not over PC})] / (\text{NW union PI}) \geq 0.20$

Growth of dendrites proportional to metal current density (more metal on n-well net, less current density)

Alternate photo current path and recombination through P+ to N-well junction reduces current density

Relates to volume of photo-generated electron-hole pairs

- All thin Cu metal and via levels are susceptible
  - Consider M[1..4] areas individually (NOT cumulative)
  - Thick Cu (including MQ) exempt due to larger metal spacing
- Rule 595: Similar rule for triple well NFET p-wells
  - PI only, not union NW
  - $[20*(M[1..4]) + (((RX \text{ over } BP) \text{ over } PI) \text{ not over PC})] / (PI \text{ not over NW}) \geq 0.20$

For T3, Rules T3W594a, T3W594b and T3W595 apply

# Pattern Density Requirements

- See DM section 2.13 Pattern Density Requirements
- Wafer manufacturing requires pattern density ranges for certain mask levels
  - Required for critical etch, photo and planarization process steps
- Designers must meet all Local and Global min/max Pattern Density requirements
  - Designers can generate FILL shapes on all layers that receive FILL using the FILLGEN tool supplied with the PDK
  - Further GF FILL during tapeout can be blocked by covering the design with xxEXCLUD layers, where xx=all filled layers
- Pattern Density = percentage of area covered by shapes on particular level
  - Global % coverage of level (chip area defined by union of "CHIPEDGE" "DG" and "CRACKSTOP" "DG" design levels)
  - Local % coverage of smaller areas stepped over entire chip area
- Post-processing of design data facilitates achieving required densities
  - GF generates Fill shapes during tapeout processing on RX, PC, 1x and 2x Cu wiring layers. i.e. M<sub>x</sub> (x=1,2,3,4,Q)
  - Hole shapes are added on 1x and 2x copper wiring layers, and all contact/via layers
- Other layers are the designers' responsibility
  - Designs must meet density requirenemts on layers not FILLED by GF before taping out the design
  - Estimated pattern density rules can highlight potential errors prior to the placement of FILL and HOLES

# Pattern Density Requirements (2)

- Design must meet manufacturing requirements at mask build after Design Services Post-processing Fill and Hole operations
  - **Designers must run and meet density checking on:**
    - Global pattern density: RX, PC, DT, EX, QY, LY, AM, E1, MA, LV, DV, SV
    - Local pattern density: RX, CA/CABAR, Mx (x=1-4, Q)
  - **Some levels are completely designer responsibility, e.g. LV, DV, SV**
  - **Other levels primarily addressed through FILL and HOLE post-processing by GLOBALFOUNDRIES, e.g. Mx**
  - **It is possible to design such that post-processing cannot meet pattern density requirements**
    - Some control of GLOBALFOUNDRIES generated fill is provided through exclusion layers (RX, PC, Mx)
    - xxEXCLUD levels prevent addition of auto fill shapes that places additional burden on the designer in areas sensitive to FILL
      - Designers must meet local density rules in RXEXCLUD, PCEXCLUD, MxEXCLUD areas
      - Verification tools assist in identifying problem areas
    - aFil and aFil2 Pcells provided in PDK to assist with designer-placed fill shapes
    - Custom fill cells advantageous as well. Create your own fill shapes using design rules in Appendix H

# Pattern Density Checking Methodology

- DRC checks Estimated Pattern Density [Local/Global] (EPD[L/G]), Drawn Pattern Density [Local/Global] (DPD[L/G]), and Final Pattern Density [Local/Global] (FPD[L/G]) for layers as shown in section 2.13
- Designs are signed off based on the Final Pattern Density rules, and class "a" Drawn Pattern Density Rules.
- Estimated Pattern Density are intended to highlight potential Final Pattern Density errors after Design Services is completed. There are generally Final Pattern Density rules for all Estimated Pattern Density rules. Please refer to the summary tables in section 2.13 for all of the relevant details
- There is also Cell Level Checking (CLC) and Chip level checking which enables the designer to get an early look at the state of pattern, even at the macro level of the design

Table 2-12: Pattern Density Checking Methodology by Level

Pattern Density Checking Methodology		Process Level										
		RX	PC	M1	M2	M3	M4	MQ	LY	E1	MA	AM
Explicit Estimation (EPD)	Global	x	x	x	x	x	x	x	x	x	x	x
Drawn Only		-	-	-	-	-	-	-	-	-	-	-
Explicit Estimation (EPD)	Local	x	x	x	x	x	x	x	x	x	-	-
Drawn Only		-	-	-	-	-	-	-	-	-	x	x

# Global Pattern Density Requirements

**Table 2-18: Global Pattern Density Rules Summary**

Level / Type of Check		Design Rule		Design Rule Value		Checking Boundary <sup>1,2</sup>
		Minimum	Maximum	Min.	Max.	
DT	drawn	DPDG_DT_min [a]	DPDG_DT_max1 [a]	1%	6%	CHIP
	drawn	-	DPDG_DT_max2 [b]	-	4.5%	CHIP
RX	drawn	-	DPDG_RX_max [a]	-	75%	CHIP
	estimated	EPDG_RX_min [a]	-	25%	-	CHIP
	final	FPDG_RX_min [a]	-	25%	-	CHIP
PC	drawn	-	DPDG_PC_max [a]	-	30%	CHIP
	estimated	EPDG_PC_min [a]	-	15%	-	CHIP
	final	FPDG_PC_min [a]	-	15%	-	CHIP

**Table 2-18: Global Pattern Density Rules Summary (continued)**

Level / Type of Check		Design Rule		Design Rule Value		Checking Boundary <sup>1,2</sup>
		Minimum	Maximum	Min.	Max.	
PH	drawn	DPDG_PH_min [a]	-	-	0.60%	CHIP
EV	drawn	-	DPDG_EV_max [a]	-	5%	CHIP
EX	drawn	DPDG_EX_min [a]	DPDG_EX_max [a]	0.1%	5%	CHIP
SV	drawn	-	DPDG_SV_max [a]	-	1%	CHIP
M1	estimated	EPDG_M1_min [a]	EPDG_M1_max [a]	25%	65%	CHIP
	final	FPDG_M1_min [a]	FPDG_M1_max [a]	25%	65%	CHIP
M2	estimated	EPDG_M2_min [a]	EPDG_M2_max [a]	25%	65%	CHIP
	final	FPDG_M2_min [a]	FPDG_M2_max [a]	25%	65%	CHIP
M3	estimated	EPDG_M3_min [a]	EPDG_M3_max [a]	25%	65%	CHIP
	final	FPDG_M3_min [a]	FPDG_M3_max [a]	25%	65%	CHIP
M4	estimated	EPDG_M4_min [a]	EPDG_M4_max [a]	25%	65%	CHIP
	final	FPDG_M4_min [a]	FPDG_M4_max [a]	25%	65%	CHIP
MQ	estimated	EPDG_MQ_min [a]	EPDG_MQ_max [a]	25%	65%	CHIP
	final	FPDG_MQ_min [a]	FPDG_MQ_max [a]	25%	65%	CHIP
LY	drawn	DPDG LY_min1 [a]	DPDG LY_max [a]	23%	70%	CHIP
	drawn	DPDG LY_min2 [b]	-	27%	-	CHIP
	estimated	EPDG LY_min [a]	EPDG LY_max [a]	23%	70%	CHIP
	final	FPDG LY_min [a]	FPDG LY_max [a]	23%	70%	CHIP
QY	drawn	-	DPDG_QY_max [a]	-	40%	CHIP
HY	drawn	-	DPDG_HY_max [a]	-	20%	CHIP
E1	drawn	DPDG_E1_min [a]	DPDG_E1_max [a]	25%	50%	CHIP
	estimated	EPDG_E1_min [a]	EPDG_E1_max [a]	25%	50%	CHIP
	final	FPDG_E1_min [a]	FPDG_E1_max [a]	25%	50%	CHIP
MA	drawn	DPDG_MA_min [a]	DPDG_MA_max [a]	27%	70%	CHIP
	estimated	EPDG_MA_min [a]	EPDG_MA_max [a]	27%	70%	CHIP
	final	FPDG_MA_min [a]	FPDG_MA_max [a]	27%	70%	CHIP
AM	drawn	DPDG_AM_min [a]	DPDG_AM_max [a]	27%	70%	CHIP
	estimated	EPDG_AM_min [a]	EPDG_AM_max [a]	27%	70%	CHIP
	final	FPDG_AM_min [a]	FPDG_AM_max [a]	23%	70%	CHIP
DV	drawn	-	DPDG_DV_max [a]	-	20%	CHIP
LV	drawn	-	DPDG_LV_max [a]	-	20%	CHIP

See Section 2.13 in Design Manual for more details.

# Local Pattern Density Requirements

Table 2-19: Local Pattern Density Rules Summary

Level / Type of Check		Design Rule		Design Rule Value		Checking Window / Stepping Size	Checking Boundary <sup>1,2</sup>
		Minimum	Maximum	Min.	Max.		
DT	drawn	-	DT20R [d]	-	20%	20x20/10	CHIP
	drawn	-	A_DT20 [d]	-	20%	20x20/10	CHIP
RX	drawn	-	DPDL_RX_max [a]	-	75%	126x126/63	CHIP
	estimated	EPDL_RX_min1 [a]	-	15%	-	200x200/100	CHIP

Table 2-19: Local Pattern Density Rules Summary (continued)

Level / Type of Check	Design Rule		Design Rule Value		Checking Window / Stepping Size	Checking Boundary <sup>1,2</sup>
	Minimum	Maximum	Min.	Max.		
PC	estimated	EPDL_RX_min2 [b]	-	-	20%	-
	estimated	CLC_EPDL_RX_min1 [d]	-	-	17%	-
	estimated	CLC_EPDL_RX_min2 [d]	CLC_DPDL_RX_max [d]	22% 73%	126x126/12.6	CELL
	final	FPDL_RX_min1 [a]	-	-	15%	-
	final	FPDL_RX_min2 [b]	-	-	20%	-
CA CABAR CEBAR	drawn	-	DPDL_PC_max [a]	-	80%	126x126/63
	estimated	EPDL_PC_min [d]	-	-	5%	-
	estimated	CLC_EPDL_PC_min [d]	CLC_DPDL_PC_max [d]	7% 78%	126x126/12.6	CELL
	final	FPDL_PC_min [d]	-	-	5%	-
	drawn	-	DPDL_CA_max1 [a]	-	16%	25x25/12.5
	drawn	-	DPDL_CA_max2 [d]	-	10%	25x25/12.5
TSV2	drawn	-	DPDL_CA_max3 [a]	-	12%	25x25/12.5
	drawn	-	CLC_DPDL_CA_max1 [d]	-	14%	25x25/2.5
	drawn	-	CLC_DPDL_CA_max2 [d]	-	8%	25x25/2.5
	drawn	-	CLC_DPDL_CA_max3 [d]	-	10%	25x25/2.5
	drawn	-	SV18 [a]	-	5%	300x300/150
	drawn	-	DPDL_M1CHEXCL_max [a]	-	80%	100x100/50
M1	drawn	-	DPDL_M1_max [a]	-	79.9%	19x19/1
	drawn	-	CLC_DPDL_M1_max [d]	-	78%	19x19/1
	estimated	CLC_EPDL_M1_min1 [d]	-	-	1.5%	-
	estimated	CLC_EPDL_M1_min2 [d]	-	-	6%	-
	estimated	CLC_EPDL_M1_min3 [d]	-	-	8.5%	-
	estimated	-	CLC_EPDL_M1_max [d]	-	83%	50x50/5
	estimated	EPDL_M1_min [a]	-	-	8%	-
	estimated	EPDL_M1_min1 [a]	-	-	1%	-
	estimated	EPDL_M1_min2 [a]	-	-	5%	-
	estimated	EPDL_M1_min3 [b]	-	-	8%	-
	estimated	-	EPDL_M1_max [a]	-	85%	50x50/25
	final	FPDL_M1_min [a]	-	-	8%	-

See Section 2.13 in Design Manual for more details. Only a partial list of rule shown

# Estimated RX and PC Local Density Checking

- **Estimated Local Density Checks**
  - Take into consideration expected RXFILL
- **Estimates the RX Local Density with expected RXFILL added**
  - Estimates are very close to what the density will be after Design Services
  - Estimated pattern density may differ slightly from the final density after FILL
  - It is the designer's responsibility to make sure that pattern density rules are met before tapeout
- **Rule divides chip into local checking windows and stepping sizes as shown in table 2-19**
  - Calculates existing RX density
  - Calculates area available for RXFILL
    - FILL rules in Appendix H of design manual
  - **Calculates final (RXFILL + RX) local density**
- **Potential problem areas for meeting local minimum requirement**
  - Arrays of polysilicon resistors, RXEXCLUD regions
- **Similar checks are performed for PC**
- **DRC provides Estimated Checks RX and PC layers as listed in Tableble 2-19**
- **GLOBALFOUNDRIES will add RFXILL and PCFILL to designs not blockes with EXCLUDE layers**

See Section 2.10 and Appendix H in Design Manual for more details

# Local Pattern Density – Metal Levels

- Required for manufacturing M1-M4, MQ, LY, E1, MA and AM levels
- Customers can generate FILL for all layers with the supplied FILLGEN tool
- GLOBALFOUNDRIES adds fill shapes to the following layers: M1-M4, MQ
- GLOBALFOUNDRIES add hole shapes to the following layers: M1-M4, MQ
  - R and C specifications assume hole shapes have been added
- Similar rules and conditions apply for LY, E1, AM and MA
- DRC provides Estimated Local Pattern Density Checks
  - Estimated Local Pattern Density Checks for metals are similar to Estimated RX/PC checks

**Table 2-13: Fill and Hole Generation Responsibility by Level**

Metallization Option	Levels on which GLOBALFOUNDRIES generates		Levels with Pattern Density Requirements	
	Fill Only	Fill and Holes	Global Pattern Density	Local Pattern Density
AM	RX, PC	M1, M2, M3, M4, MQ	RX, PC, DT, EV, EX, QY, LY, AM, LV, DV, SV	RX, CA, M1, M2, M3, M4, MQ
DM	RX, PC	M1, M2, M3, M4, MQ	RX, PC, DT, EV, EX, QY, LY, E1, MA, LV, DV, SV	RX, CA, M1, M2, M3, M4, MQ

See Section 2.10 and Appendix H in Design Manual for more details

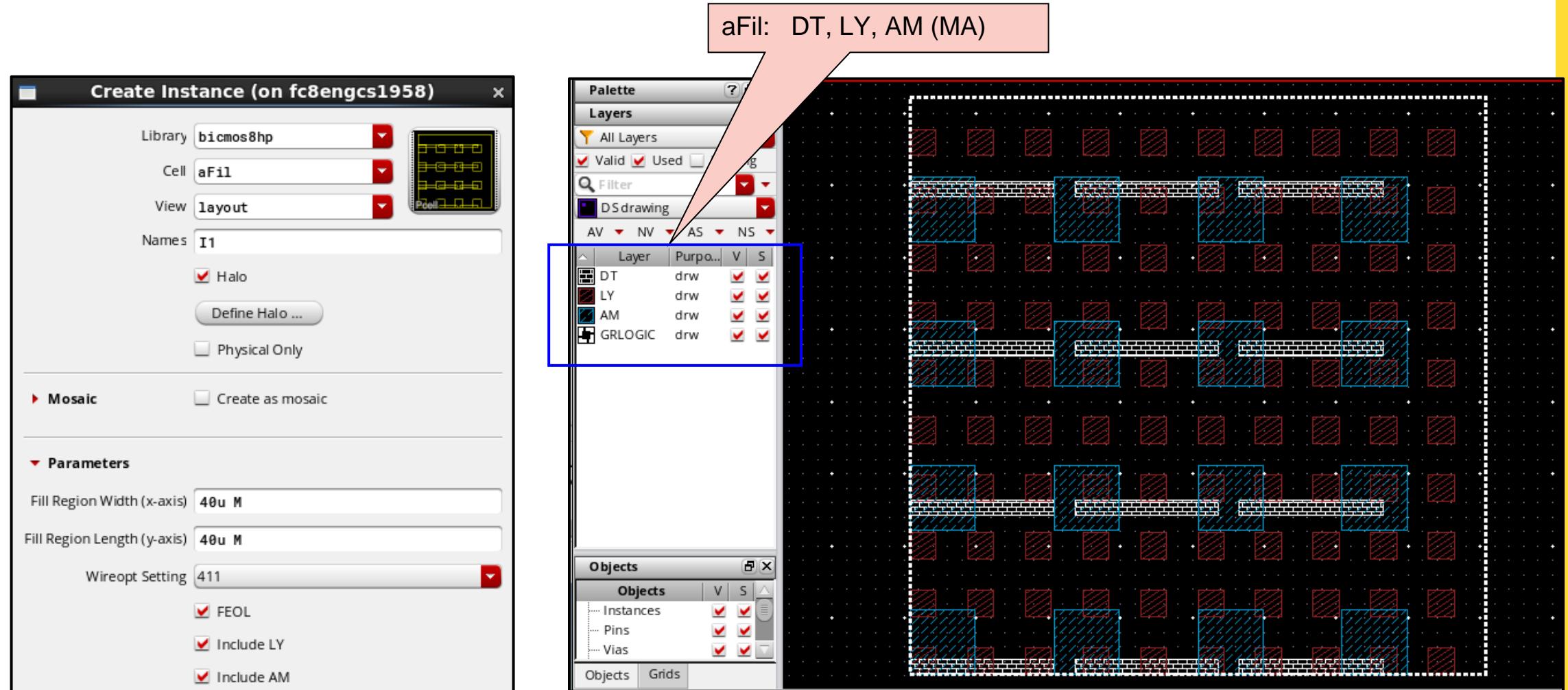
# FILL Targets (Standard, Low, and Fill Blocking Shapes)

Table 2-14: Fill Generation Density Targets by Level

Design Level	Target Density		Fill Modification Shapes	
	Std.	Low	Low Density	Fill Blocking <sup>1</sup>
RX	45%	20%	BONDPAD, IND_FILT, BFMOAT, RF_MODFILL	RXEXCLUD
PC	25.7%	20%	BFMOAT	PCEXCLUD, LOGOBND
		15%	BONDPAD, IND_FILT, TLINE, RF_MODFILL, (MA intersect MA_RFLINE)	
M1	45%	8.9%	BONDPAD, IND_FILT, RF_MODFILL	M1EXCLUD, LOGOBND
M2	45%	8.9%		M2EXCLUD, LOGOBND
M3	45%	8.9%		M3EXCLUD, LOGOBND
M4	45%	8.9%		M4EXCLUD, LOGOBND
MQ	45%	8.9%		MQEXCLUD, LOGOBND
LY <sup>2</sup>	20%	N/A	N/A	LYEXCLUD, IND_FILT, BONDPAD, RF_MODFILL, TLINE, LOGOBND, MA_RFLINE
E1 <sup>3</sup>	45%	N/A	N/A	E1EXCLUD, IND_FILT, BONDPAD, RF_MODFILL, TLINE, LOGOBND, MA_RFLINE
MA <sup>3</sup>	37.8%	N/A	N/A	MAEXCLUD, IND_FILT, BONDPAD, RF_MODFILL, MA_RFLINE, LOGOBND
AM <sup>3</sup>	45%	N/A	N/A	AMEXCLUD, IND_FILT, BONDPAD, RF_MODFILL, TLINE, LOGOBND

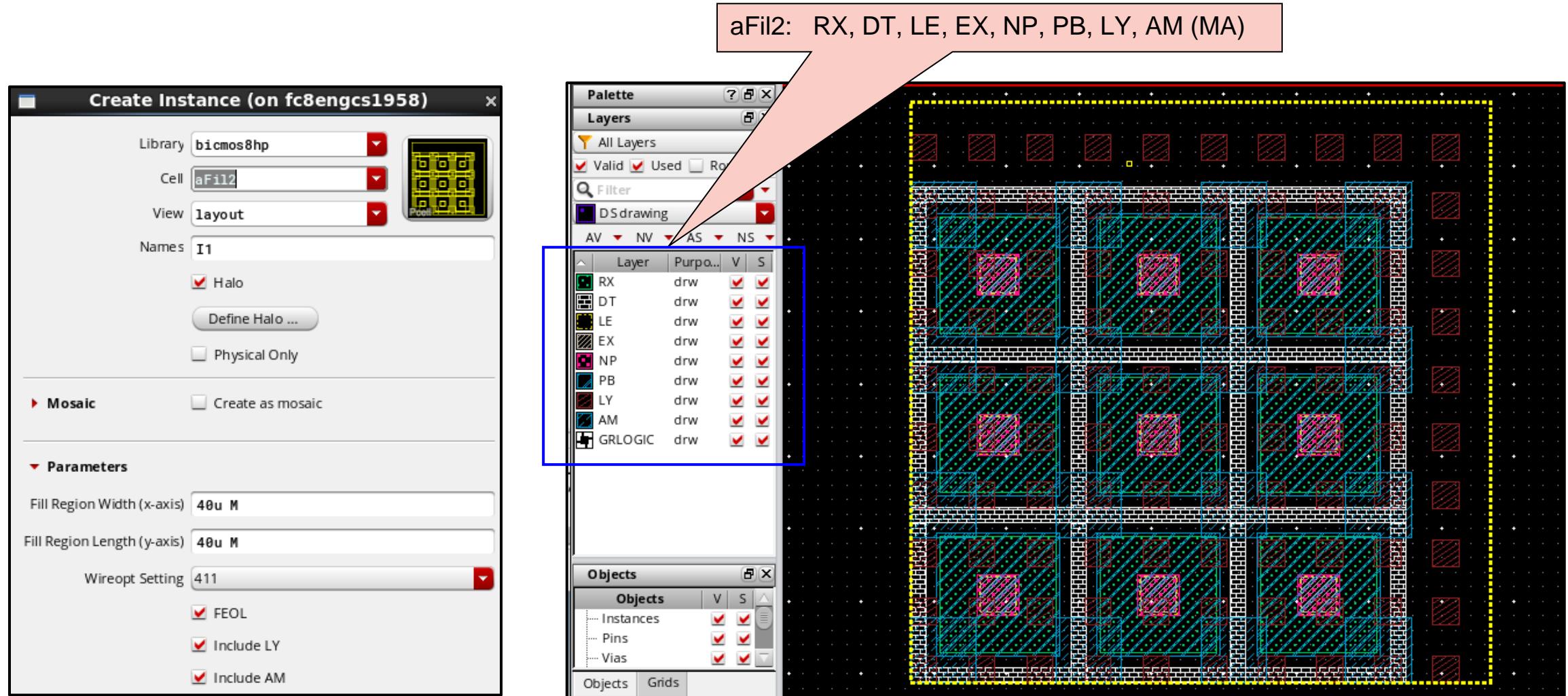
Designers may need to manually add dummy shapes under xxEXCLUD and LOGOBND

# aFil Pattern Density Aid Pcell



Use aFil or aFil2 for pattern density fill. aFil levels are limited.

# aFil2 Pattern Density Aid Pcell



Use aFil or aFil2 for pattern density fill. aFil2 has all levels

TTM-000008 Rev6

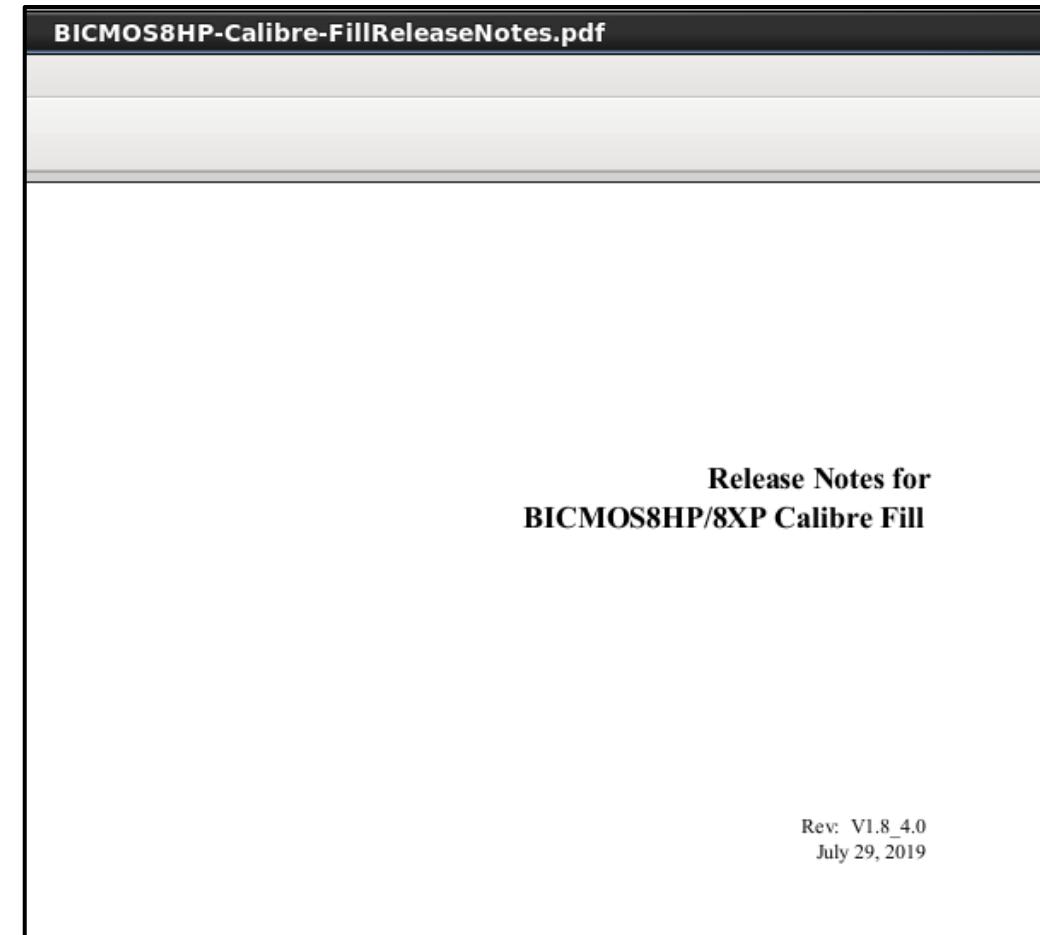
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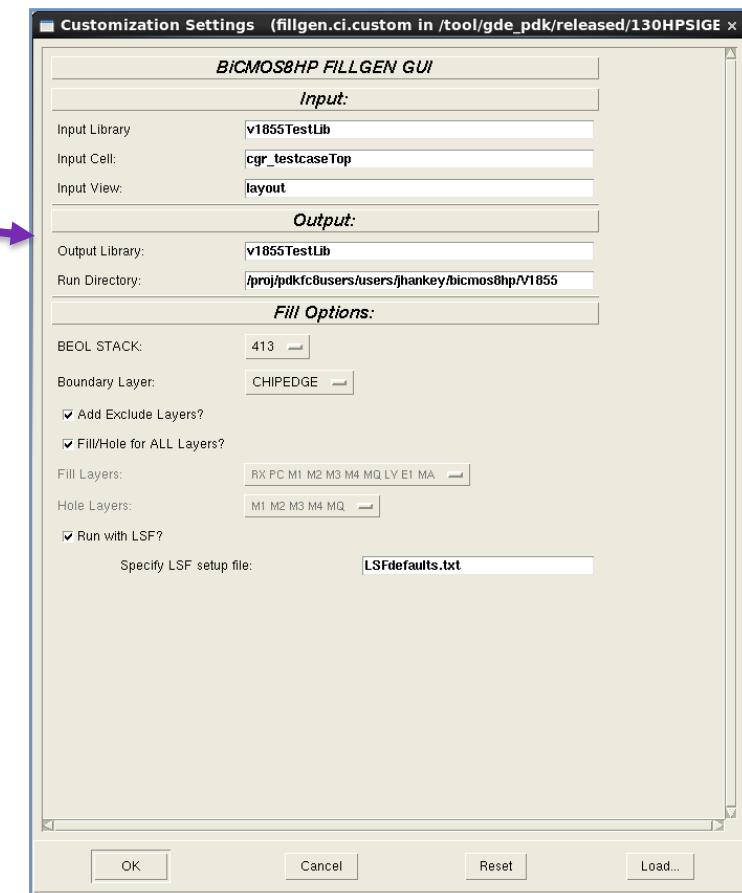
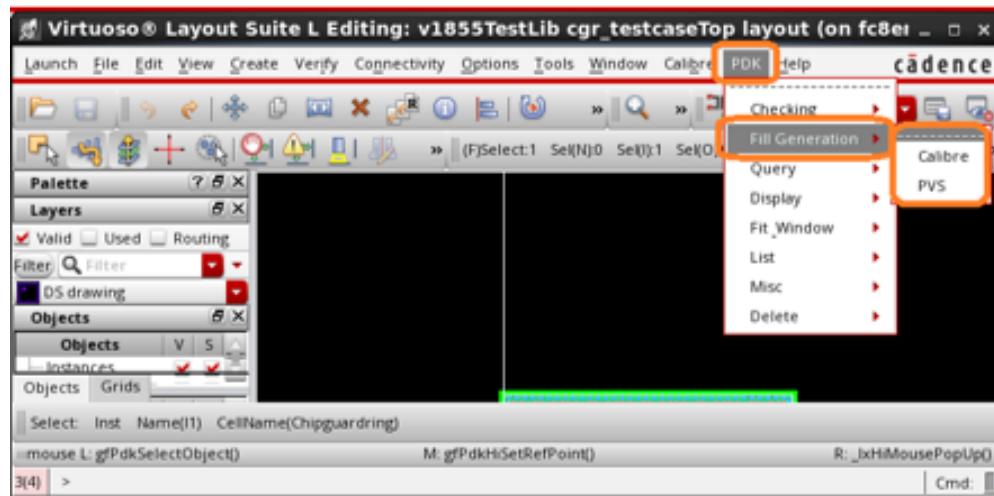
# FILLGEN Deck

- FILLGEN deck is provided that emulates the GlobalFoundries Post-and-Cheese-Fill
- Available with GUI and command line options
- FILLGEN rules are listed in the 8HP Design Manual, Appendix H.
- For more details, see Calibre FILLGEN Documentation in
  - /\$GF\_PDK\_HOME/FILLGEN/Calibre/doc



# FILLGEN Deck – GUI

- FILLGEN can be run with a GUI from the layout window and from the command line
- From the layout window: PDK --> Fill Generation --> Caliber/PVS

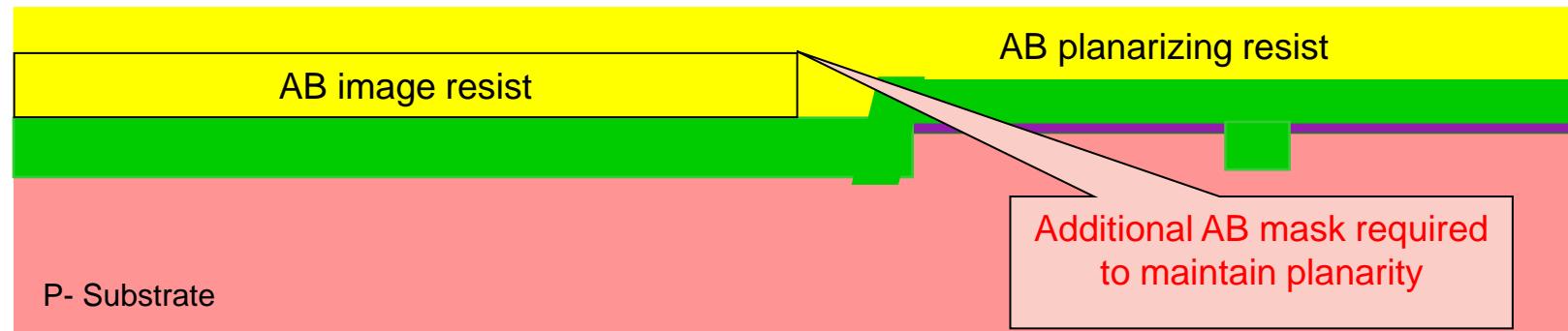


- FILL some layers or all layers.
  - **Note: RX and PC must always be filled at the same time**
- Add Exclude layers after FILL to block further FILL by GF after tapeout.
  - Layout must be passing pattern density rules if blocking FILL

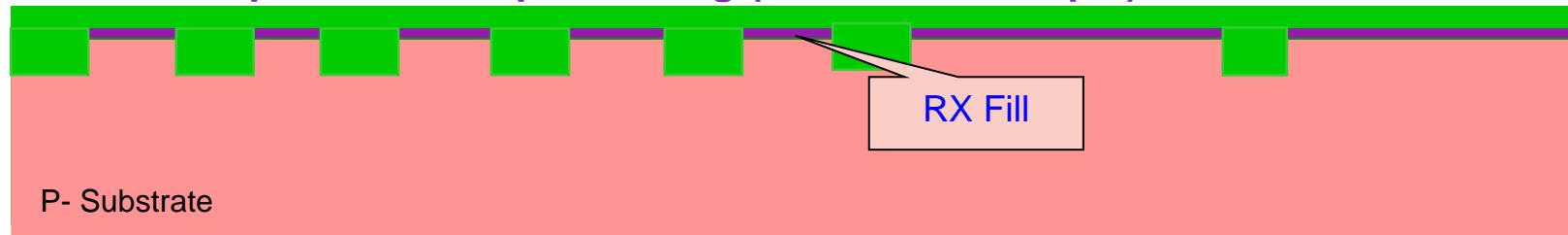
# RX Pattern Density Influences STI Planarization

- Large RX white space – hard to maintain planar STI surface
- **AB Mask Planarization Process (Old technique)**
  - Fills depression with photo resist at the start of CMP
- **RX Auto-fill - AB Mask-less Planarization Process (Current Technique)**
  - Eliminates AB mask and associated process steps and lower wafer cost

## AB mask planarization processing (Old Technique)



## Mask-less planarization processing (Current Technique)

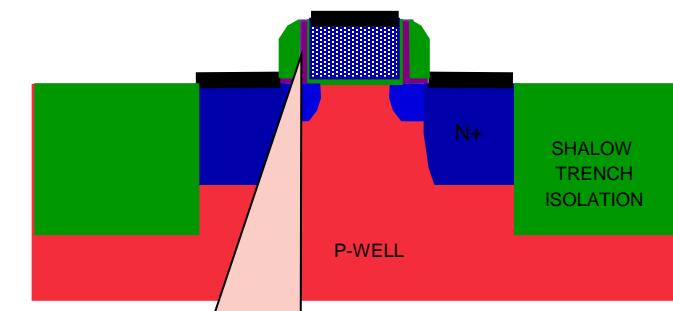


# RX Pattern Density Requirements

- **Global\* (GR PDRX): 25% to 75%**
- **Local: 15 (20) % to 75% (200 (126) mm x 200 (126) mm areas stepped 100 (63) mm)**
- **RX density requirements are due to the STI chemical mechanical polish (CMP) process to make uniform and planar STI structures**
- **Customers generate RXFILL with FILLGEN tool or Tapeout/Design Services will employ RXFILL routine as Pre-release to mask build**
- **Areas where RXFILL routines are not employed**
  - Product label areas defined by “LOGOBND”. See Image Pcell for details.
  - Under customer-drawn PC
  - Areas excluded by designer with RXEXCLUD
    - Designers must add fill in excluded areas using “RX” “DG”
- **Consult GLOBALFOUNDRIES if large areas of RXEXCLUD are contemplated**
- **If you fill RX, fill PC in that area as well**
  - Customer fill shapes on PC interfere with auto-fill on RX and vice-versa
  - See aFil2 Pcell

# PC Pattern Density influences polysilicon etch profile

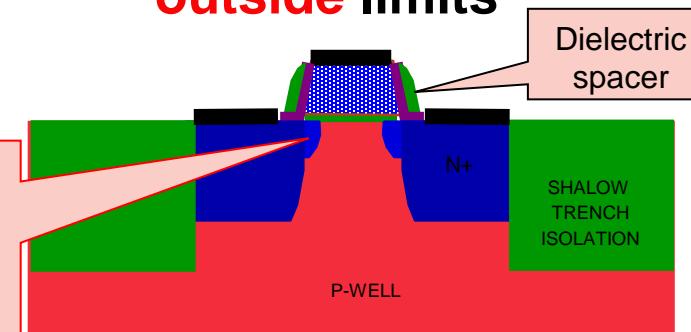
PC Pattern Density  
within limits



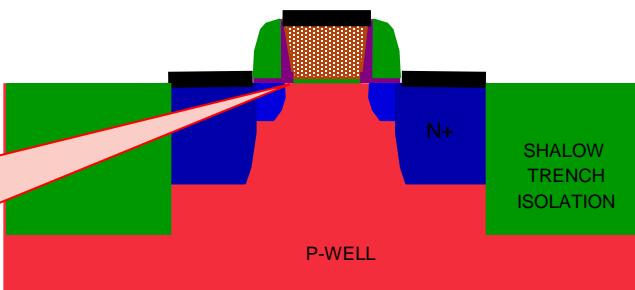
Sidewall angle of  
the polysilicon  
line, 90° ideally.

PC Pattern Density  
outside limits

Under-etch  
(low density):  
Incorrect S/D  
junction  
tailoring



Over-etch (high density):  
“Underlapped” devices due to  
recursive sidewall (hot-  
electron sensitivity)

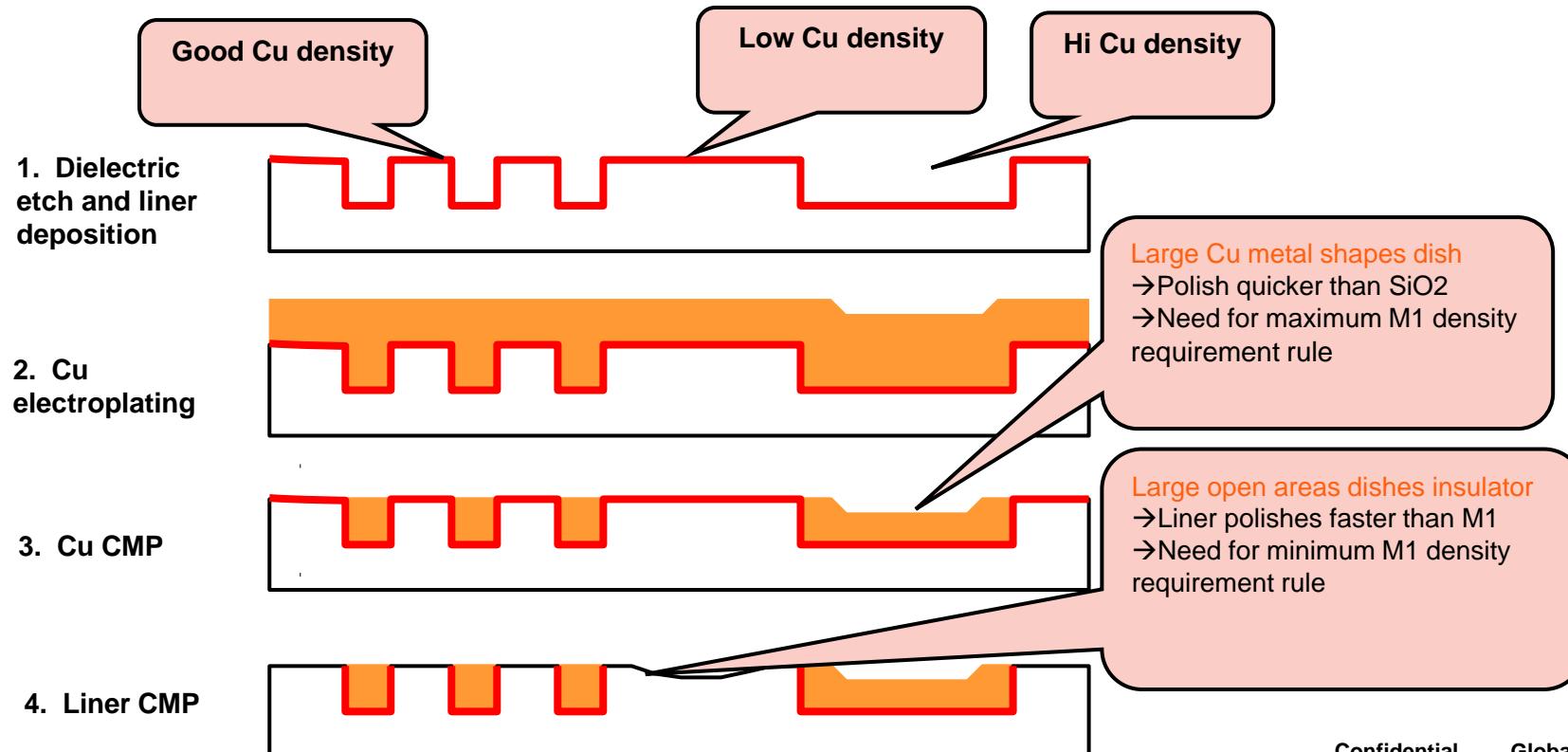


# PC Pattern Density Requirements

- **Global rule PDPC: Minimum 15%**
- **Local rule: Recommended Minimum > 5%, Required Maximum <80%**
  - PC density can impact channel length control
    - Large areas of dense polysilicon (e.g. decoupling capacitors) cause the local PC density to be very high.
    - Large areas of white space may cause degradation in the Across Chip Line width Variation (ACLV).
    - PC density limits are for control of PC line width and PC edge profiles during polysilicon etch
- **Customers generate RXFILL with FILLGEN tool or GLOBALFOUNDRIES Tapeout/Design Services will employ PCFILL routine as Pre-release to mask build**
- **Areas where PCFILL routines are not employed**
  - Fuse bays.
  - Product label areas defined by “LOGOBND” (See Image Pcell)
  - Over customer-drawn RX
  - Areas excluded by designer “PCEXCLUD”
- **Consult GLOBALFOUNDRIES if large areas of PCEXCLUD are contemplated**
- **If filling PC, fill RX in that area as well**

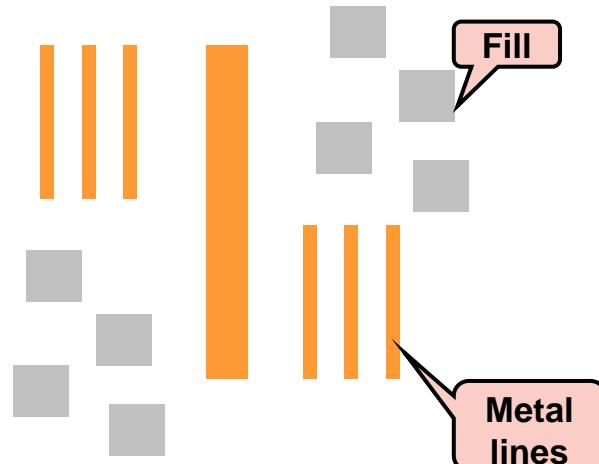
# Dishing in Cu Metal Levels

- High metal density causes over-etch, dishing in Cu
- Low metal density causes liner over-etch, dishing in insulator
- Dishing results in non-planar regions on higher levels
- Solution : Metal Holes in High Density and Fill in Low Density Regions



# Metal Fill Generation in Cu

- **Metal Fill (MxFILL shapes) eliminate large “white” spaces on a Cu metal level**
  - Adds metal shapes in low density Cu wiring layers and Cu vias (**prevents dishing**)
- **MxFILL layer shapes added by customer FILLGEN and/or GLOBALFOUNDRIES Tapeout/Design Services**
- **Design Manual Section Q: Fill and Hole Generation Design Rules**
  - Hole shapes can cover or partially cover vias if the vias are redundant
- **Wiring resistance and capacitance terms account for placement of MxFILL layer shapes**
- **Parasitic extraction decks account for hole shapes (R, C)**
  - Reliability equations account for fill shapes



- **MxFILL layer shapes are automatically excluded from:**
  - KQRES metal resistor
  - Transmission Lines
  - IND\_FILT regions receive reduced fill (8%)
  - Product label areas
    - Designer must place LOGOBND layer shapes over product label
      - Included in pcell Image in bicmos8hp Library
    - Customer fill required in logo area

# Metal Hole Generation in Cu

**Metal Hole (MxHOLE shapes) eliminate large Cu metal shapes**

Lowers Cu density on large Cu metal shapes (**prevents dishing**)

**MxHOLE layer shapes added by customer FILLGEN and/or GLOBALFOUNDRIES Design Services**

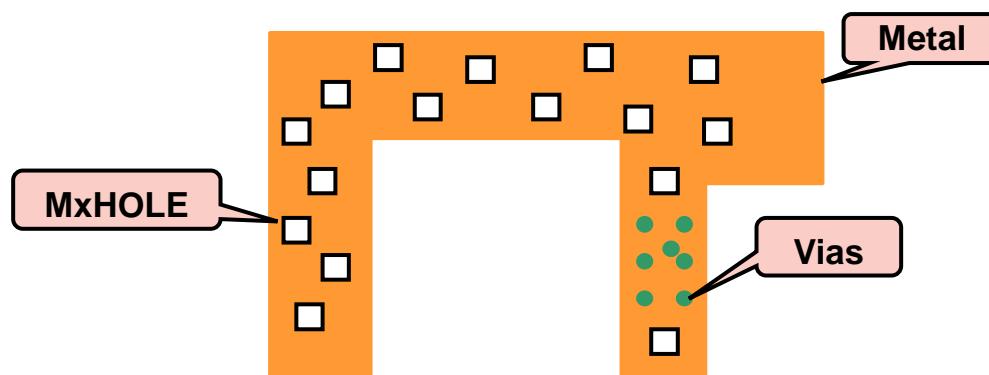
**Design Manual appendix H: Fill and Hole Generation Design Rules**

Hole shapes can cover or partially cover vias if the vias are redundant

**Wiring resistance and capacitance terms account for placement of MxHOLE layer shapes**

**Parasitic extraction decks account for hole shapes (R, C)**

Reliability equations account for hole shapes



## Areas where MxHOLE layer shapes cannot be placed:

- **Product label areas.** Designer must place LOGOBND layer shapes over product label in the Image Pcell
- **MxTRANS** (part of the transmission line pcell – do not create excluded areas using this layer)

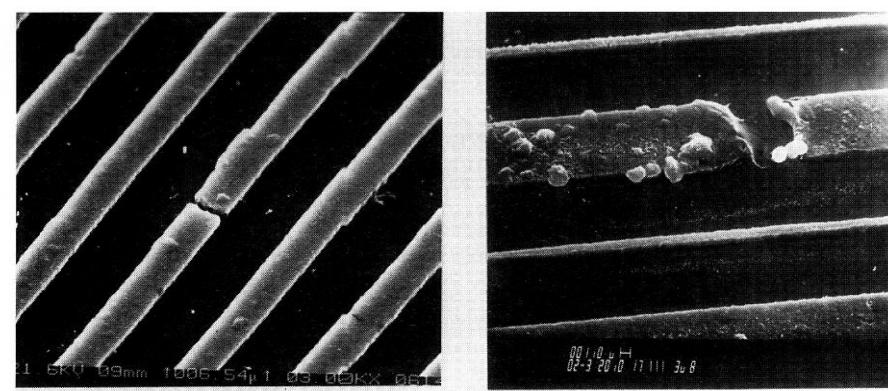
# Wiring Current Density and Reliability

- Be aware of the resistance of the wire
- High wire resistances may cause
  - Unacceptable I-R drops
  - Lower circuit Q
  - Lossy Transmission lines
- Single Vias may have very high resistance (>5 ohm) leading to unacceptable IR drops
- Different Metal Layers have different resistivity.
  - Choose appropriate wiring level consistent with electromigration and design requirements
- There are current limits (electromigration rules) for wires, vias and pads
  - Stay within safe operating current limits (DC and AC)
  - Electromigration rules are given in the design manual for meeting Reliability

# Electromigration Considerations and Rule Checks

- Electromigration occurs in all metal subject to electrical current
  - Can result in high resistance or open circuits over time
- Increases with time, temperature and current density
- Occurs in metal lines: wiring runs and in vicinity of vias/contacts
- GLOBALFOUNDRIES reliability specifications assume 100K power on hours (POH) at 100°C
- Electromigration Reliability rules and guidelines provided in Design Manual Reliability Section:
  - Calculation of current for AC and DC signals
  - Maximum current per width of metal line
  - Maximum current per via and CA
  - Time/Temperature adjustment factors for use conditions above or below
- Meeting Electromigration (EM) rules are designer's responsibility\*
  - EM rules are not coded in the checking deck.
  - There are no automatic checks.

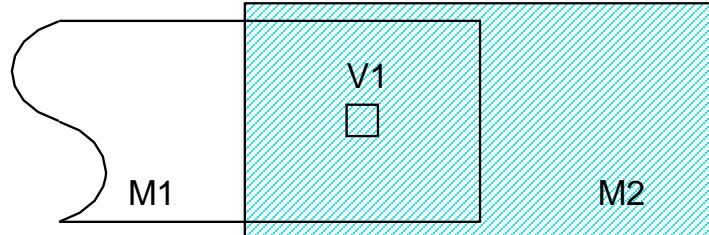
\*Cadence Voltus\_FI (EMIR-000113) and Apache Redhawk Totem (EMIR-000137) EMIR tools are supported



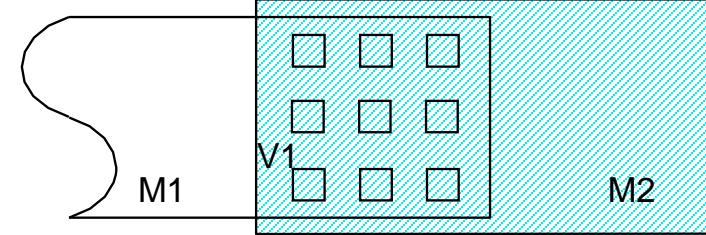
Example of open circuits resulting from excessive electromigration

# Vias - Considerations for Resistance and Reliability

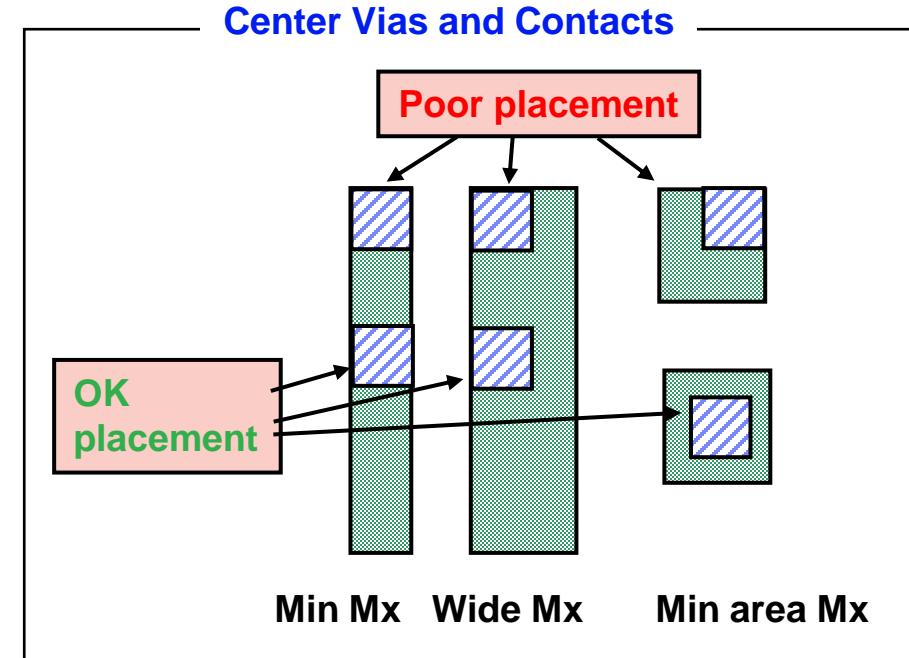
**Bad Via Design** – single via, current crowding and high resistance



**Good Via Design** – Multiple vias, distributed, low resistance



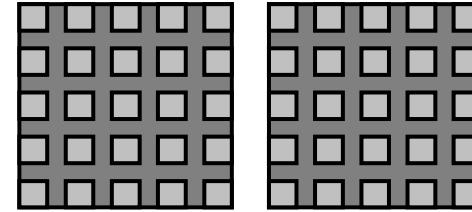
- Redundant vias **good** for yield and reliability
  - See next chart also
- Utilize array vias across metal width
  - Minimize current crowding
- Provide additional metal overlap
  - Via resistance independent of overlay
  - Aluminum reservoir for electromigration resistance
- Center Vias and Contacts



# Via Shorting

- Too many redundant vias at min space can cause merging

Worst

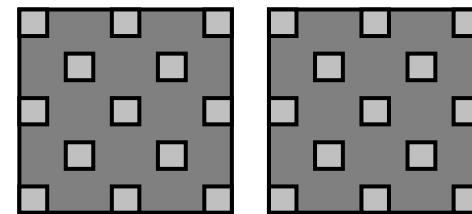


- Merged vias cause:

- Shorts when on different nets
- Visual defects when on same net
  - Cause production line inspection problems
  - Fatal defects at higher levels

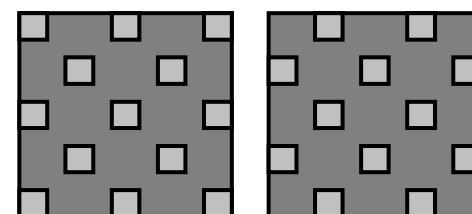
- Avoid min spaced vias same net and different net

Reduce number of vias  
(remove on diagonal)



Better

Reduce number of vias  
and stagger placement



Best

# Latchup (LU)

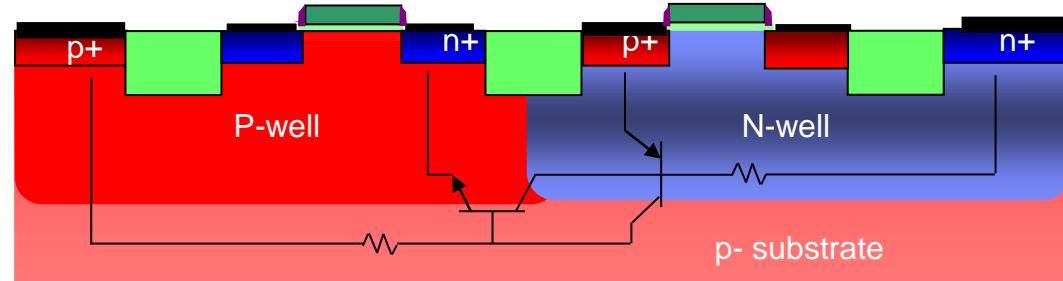
- **Internal Latchup**

- Occurs in circuits which are not connected to I/O or signal pads (C4 or wirebond pads)
- Parasitic silicon controlled rectifiers (SCR) formed in bulk CMOS are triggered by supply bounce, transmission line reflections or on-chip generation of carriers
- Controlled by limiting junction to n-well, p-well contact resistance

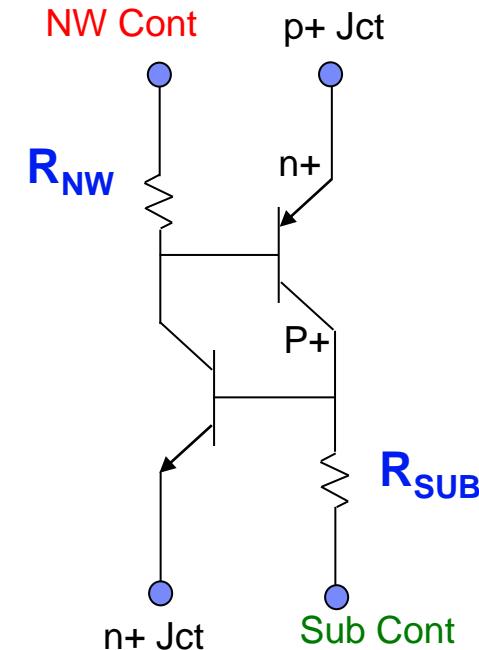
- **External Latchup**

- Triggered by off-chip signals received by I/O circuits.
- These signals create large voltage bounce or carrier injection to trigger latchup either in I/O or in weakest internal circuits adjacent to I/O cells (if these carriers are not contained in I/O)
- Controlled by collecting majority & minority carriers from forward biased junction

# Latchup Prevention Guidelines



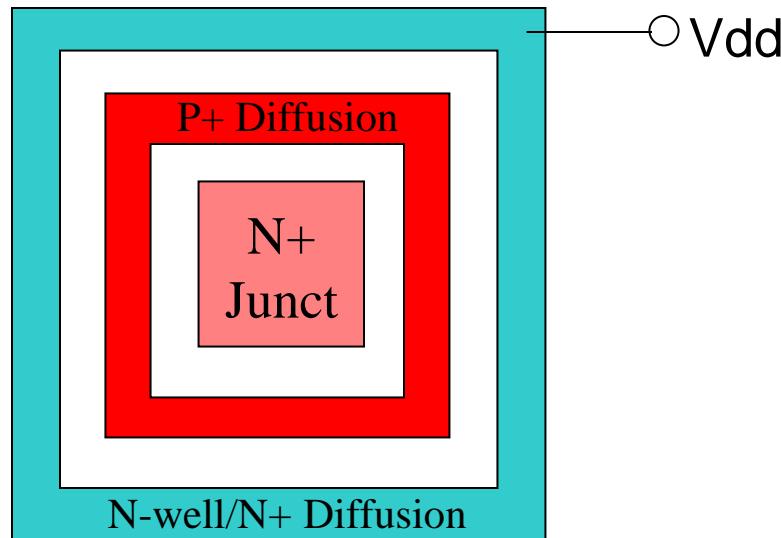
- Reduce bipolar gain
  - N+ to P+ junction spacing
    - GR260: RX P+ junction within NW
    - GR265: RX N+ junction to adjacent NW
- Minimize  $R_{NW}$  and  $R_{SUB}$ 
  - Make the **substrate/P-well contact big and close to the NFET**
    - GR268a: RX N+ junction to Substrate Contact  $\leq 38.12\mu\text{m}$
  - Make the **N-well contact big and close to the PFET**
    - GR268b1: RX P+ junction to Nwell Contact  $\leq 38.12\mu\text{m}$
  - Avoid minimum contact w/ high resistance
- Also See Section 3.38 of 8HP V1500 Design Manual (Latchup Guidelines, Layout Constraints and Rules)



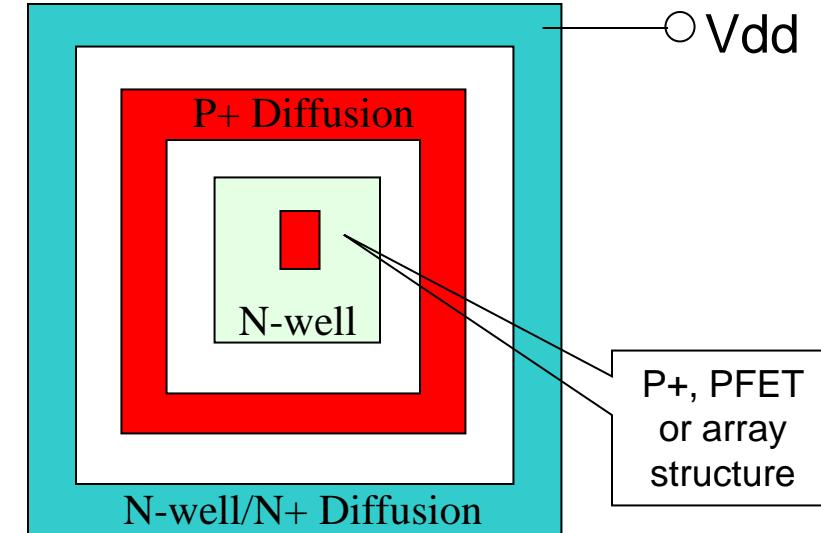
# Guard Rings for Latchup Prevention

- **Use Forward Biased Junction Guard Rings for Latch Up Prevention**

- Guard rings prevent current flow in the substrate
- All n+ regions connected to I/O must be in a guard ring as shown below
- All p+ regions connected to I/O must be within an N-well separate from all other circuitry and in a guarding as shown below



Guard Ring for  
N-channel devices

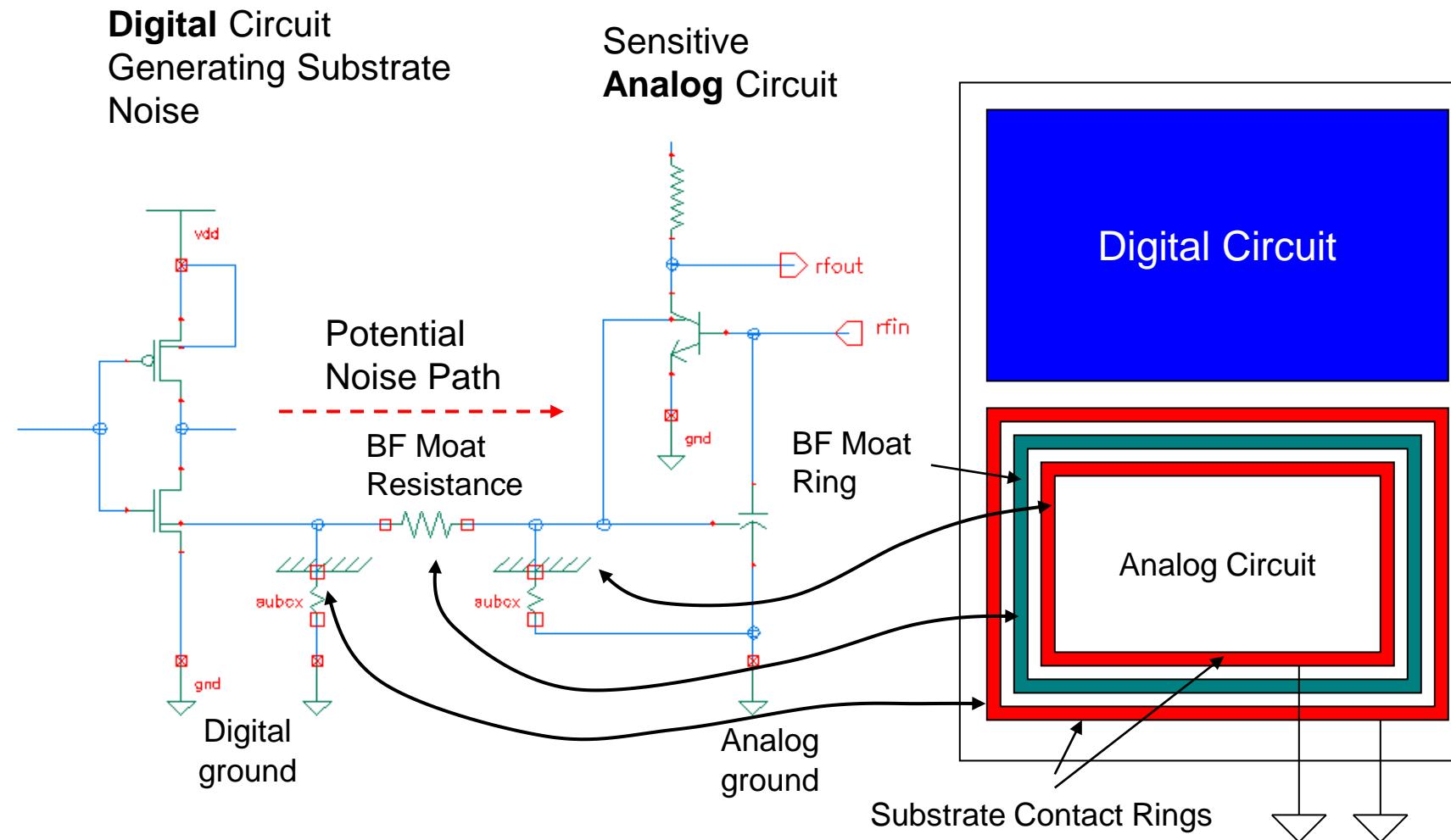


Guard Ring for  
P-channel devices

# Common Techniques for Noise Minimization

- **Separate on-chip grounds and supplies**
  - i.e., digital versus RF/analog
- **Low resistance substrate contacts within / surrounding circuit blocks**
  - Shunt substrate noise to grounds and maintain latch-up immunity
- **Isolation moats**
  - Increase substrate resistance between circuit blocks
  - Dampen noise transfer through the substrate
- **Groundshields**
  - Shunt substrate noise to AC ground
  - NS backplate available for resistors, mims, bondpads
  - Triple well (isolated p-well) nfets and (isolated n-well) pfets (T3 isolation)
- **Line to line capacitive coupling reduction**
  - Spread out critical signal wires
  - Intermix AC ground wires with signals
  - Truncated guardrings to shield capacitive coupling from chip guard ring
  - Segmented chip guard ring

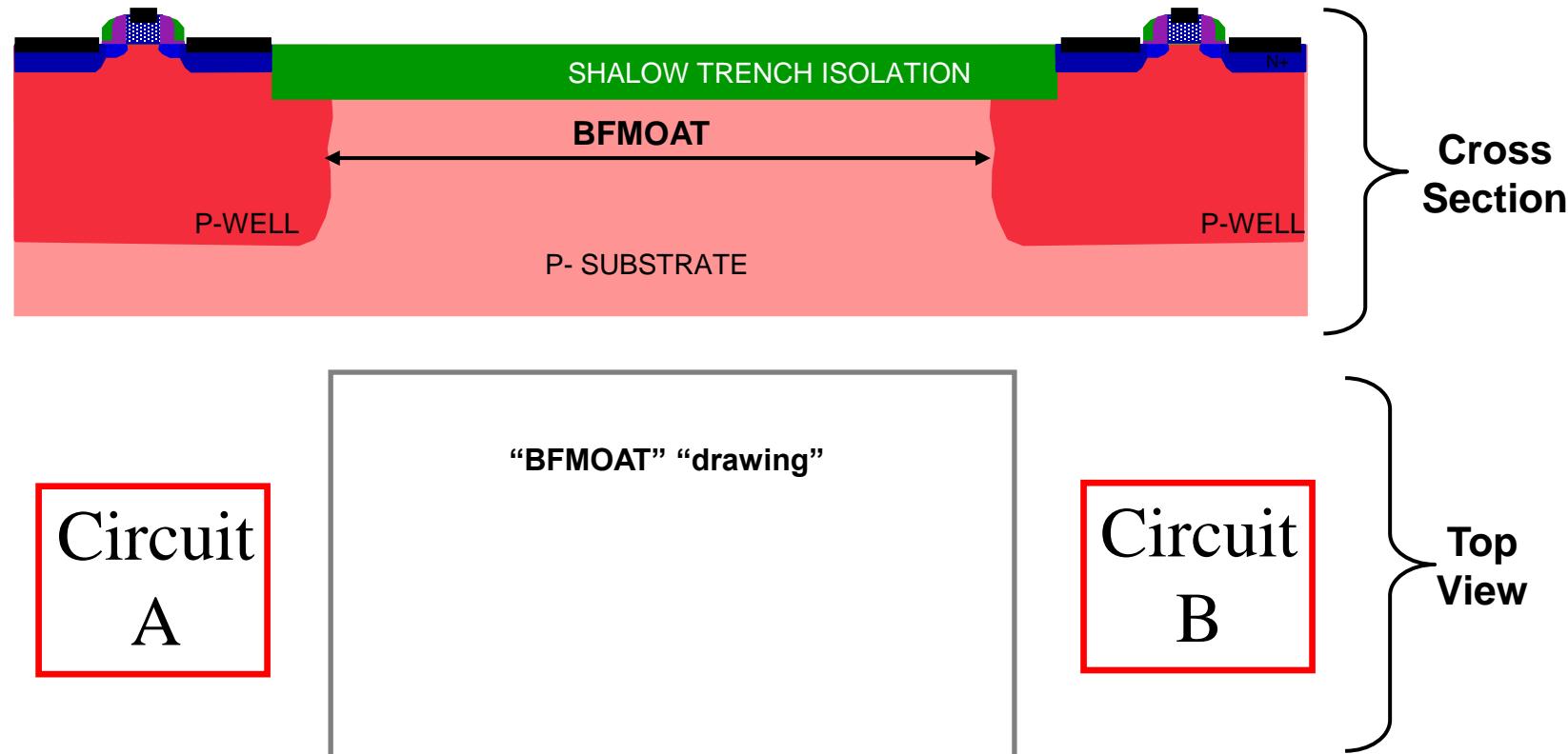
# Isolation Moat Structures\*



BFMOAT Resistance provides isolation between the noisy Digital and sensitive/quite Analog circuits

# BF Moat Isolation Structure

- Shapes drawn on “BFMOAT” “drawing” are regions blocked from p-well, n-well and triple well implant
  - Provides increased resistance between circuit blocks

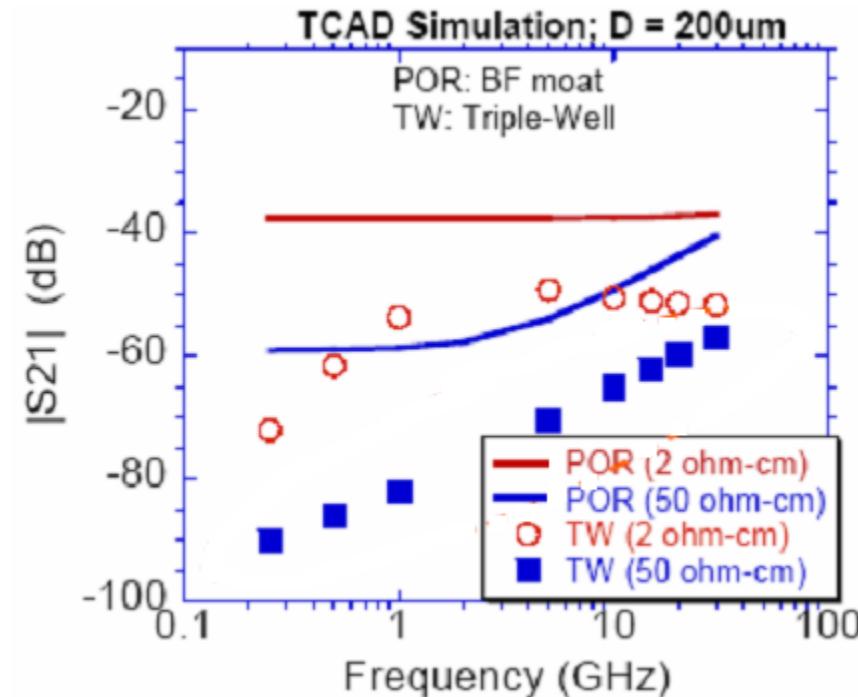


# Noise Isolation Data vs. BFMOAT Separation\*

- Significant improvement in substrate noise isolation, especially by combining high resistivity substrate and triple-well isolation

8RF Measurements for BFMOAT

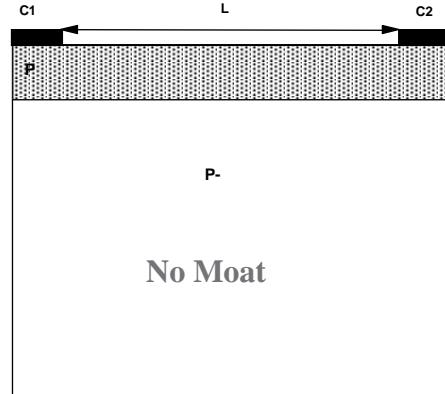
Measured	S21  at 5 GHz (dB) 2 ohm-cm	S21  at 5 GHz (dB) 50 Ohm-cm
100 um	-20.0	-21.5
200 um	-33.0	-36.0
300 um	-31.0	-43.5



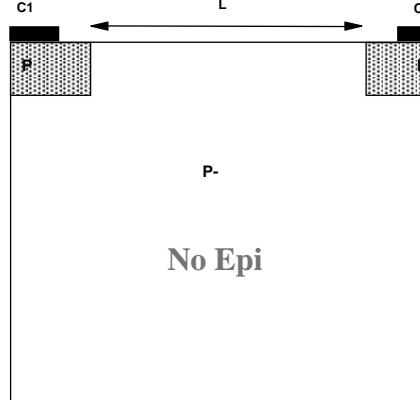
CMOS8RF Data

\* Additional information available in application note: Substrate Isolation Methodology (APN-000178)

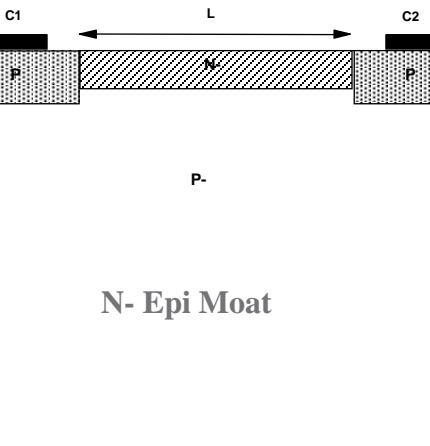
# Simulated Moat Structures Example from BiCMOS6HP (1)



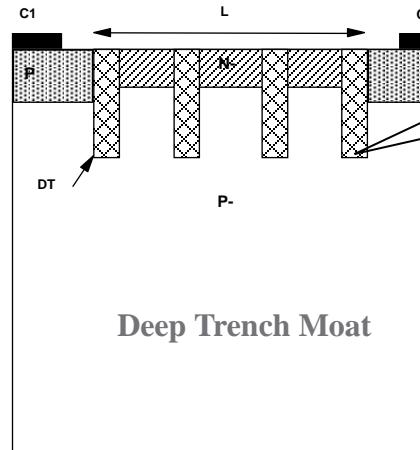
No Moat



No Epi



N- Epi Moat

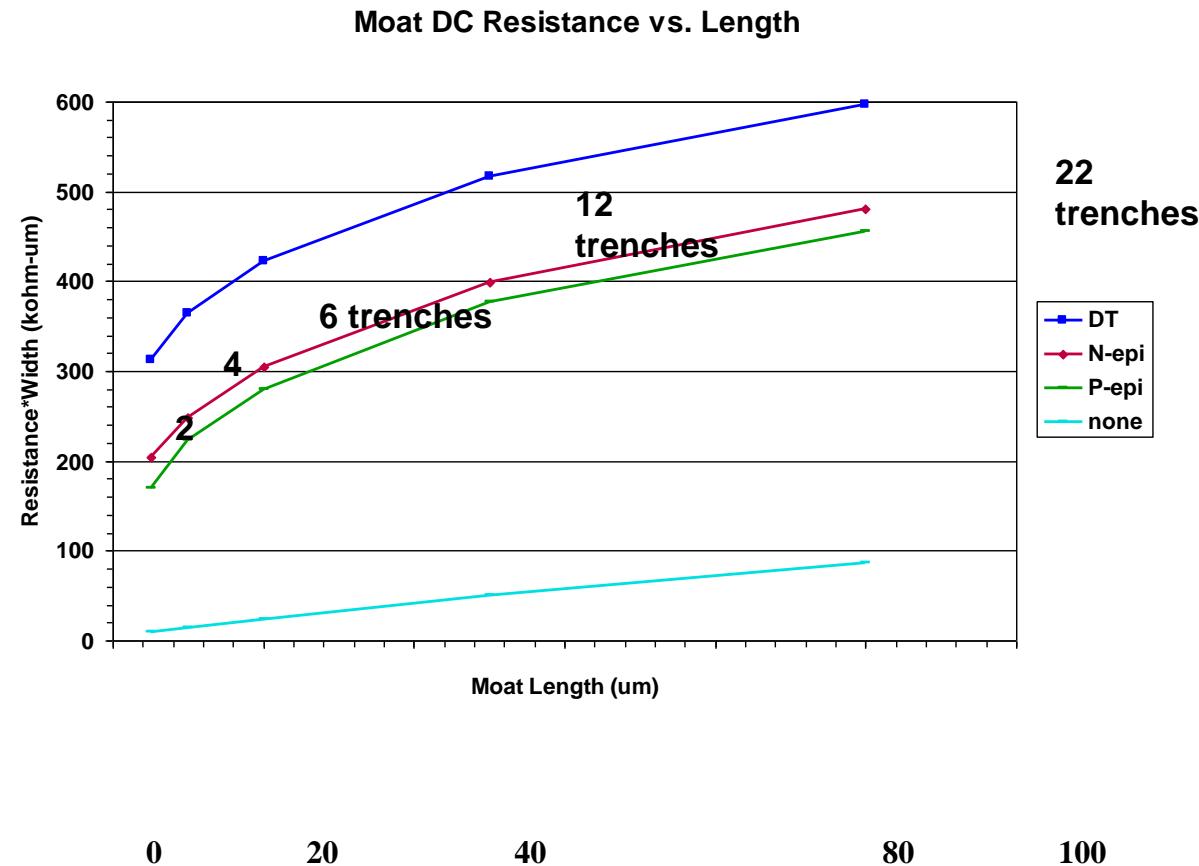


Deep Trench Moat

DT must be  
orthogonal to  
current flow (P  
channel stop  
implant)

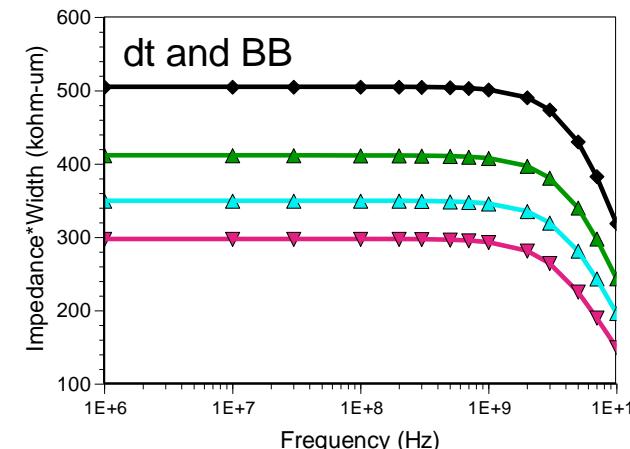
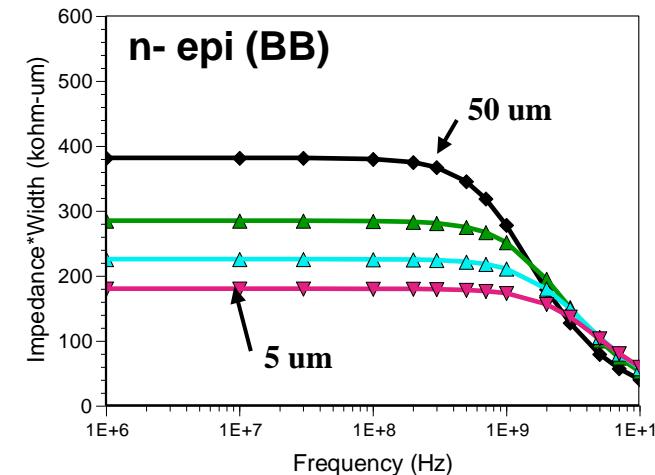
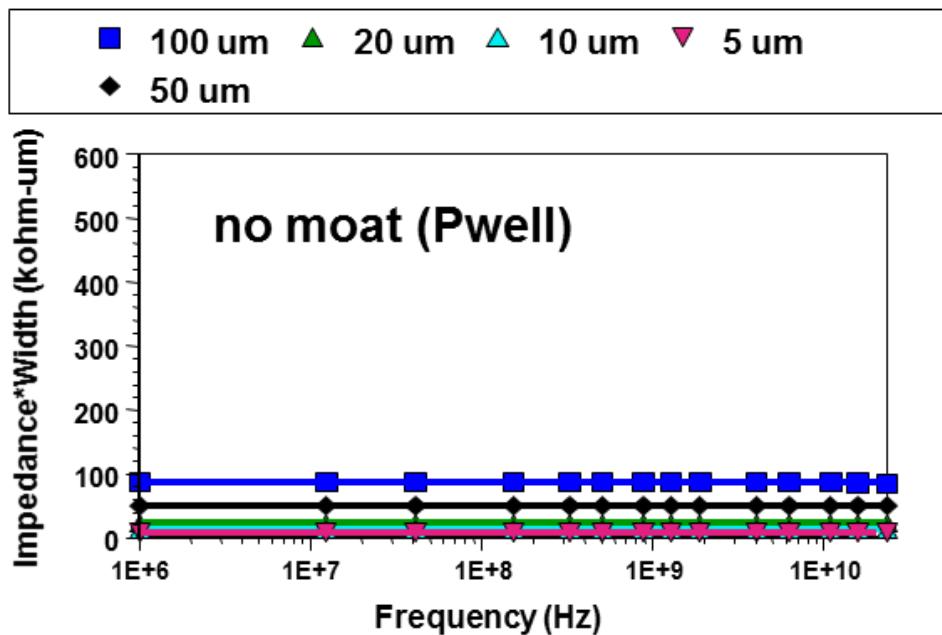
# Moat Simulation Results from BiCMOS6HP

## Example (2)



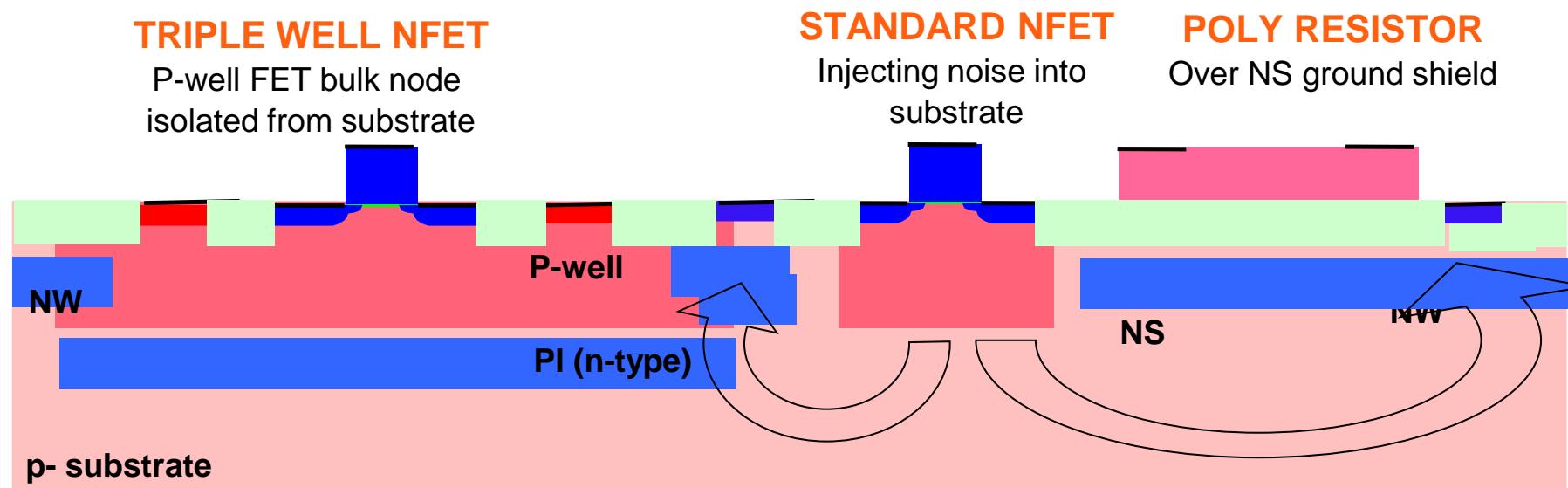
# AC Moat Simulation Results from BiCMOS6HP Example (3)

Best high frequency isolation  
with deep trench and BB (n- epi)



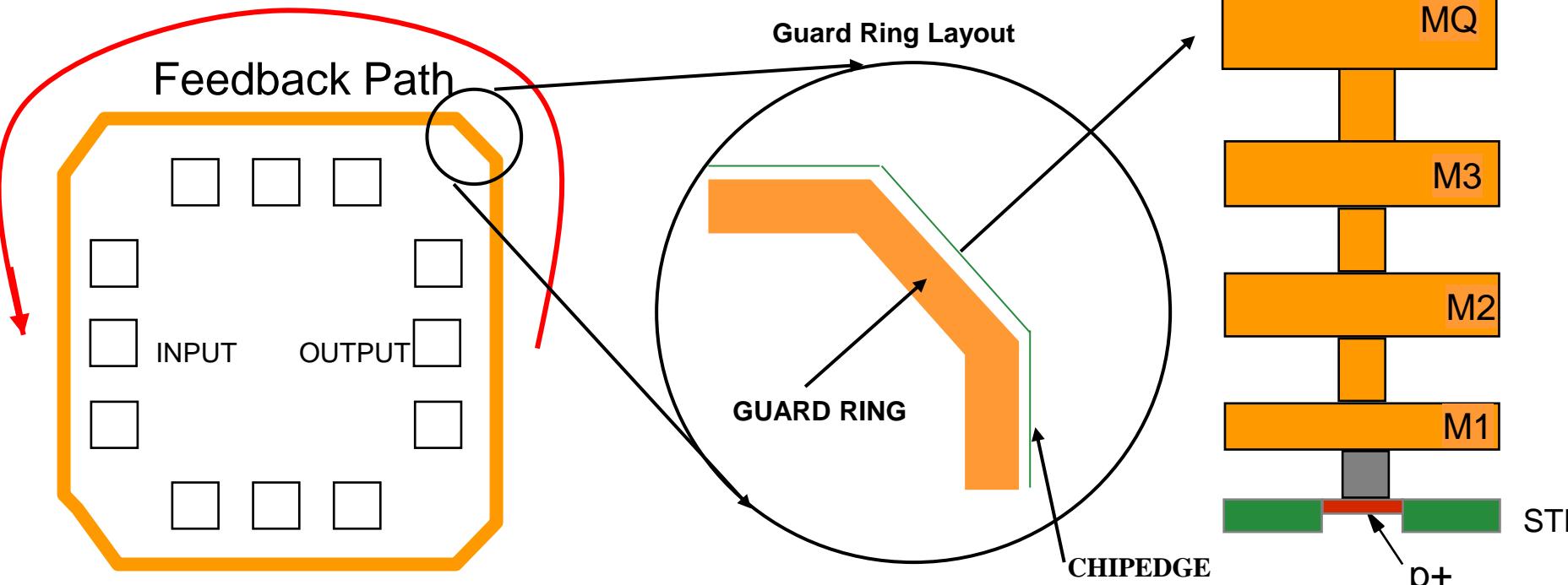
# Ground Shields

- **Ground shields - Shunt substrate noise to AC ground**
  - NS option under resistors, capacitors, bondpads
  - N-type PI layer under triple well NFETS shields FET body from substrate
- **Tie ground shields to quiet, low impedance AC ground**



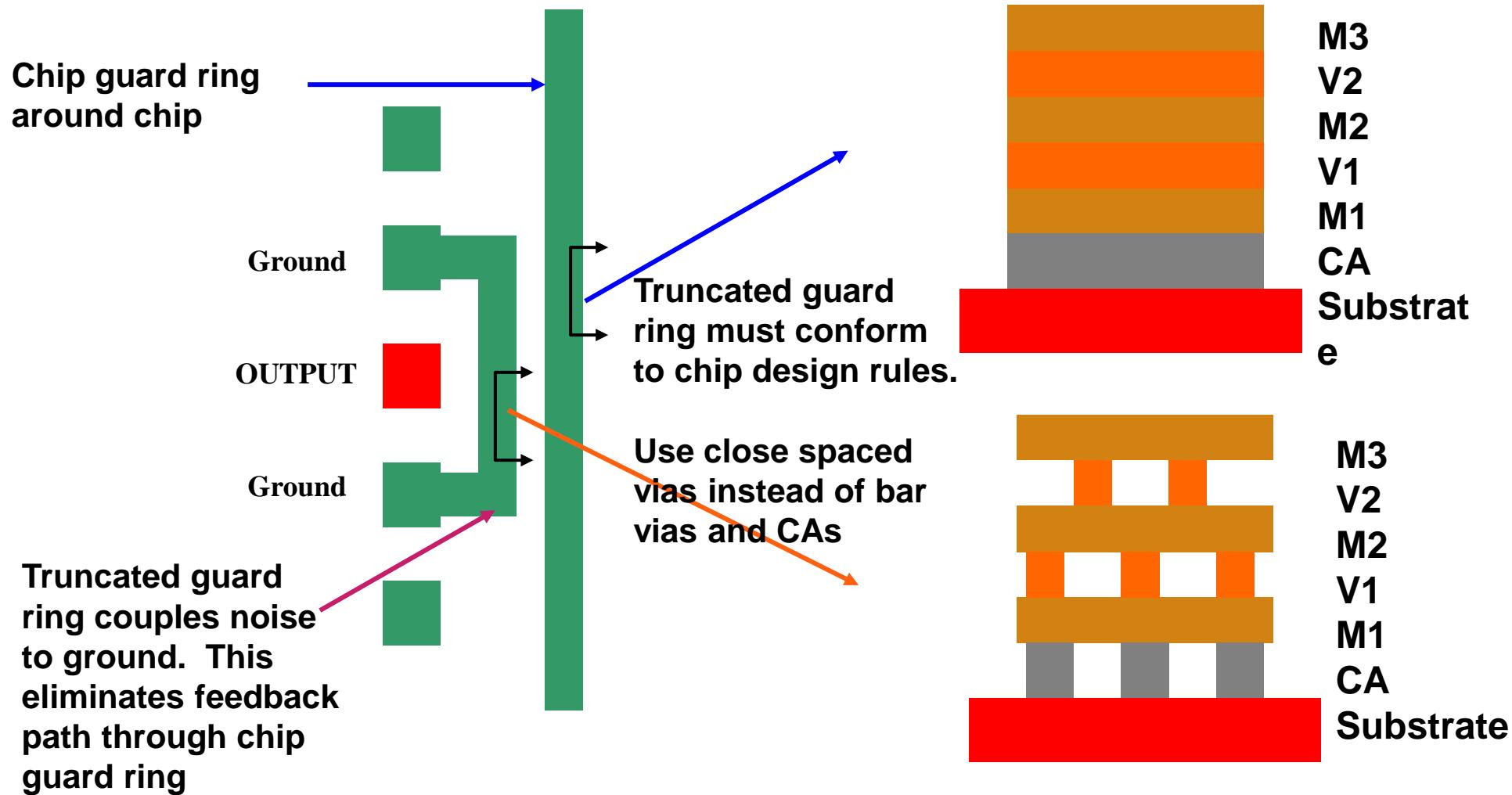
# Chip Guard Ring

- **Required - barrier to ionic contamination**
  - Chipguardring pcell in PDK
- **Chip Guard Ring is One Continuous Substrate Contact**
  - Potential feedback path around chip

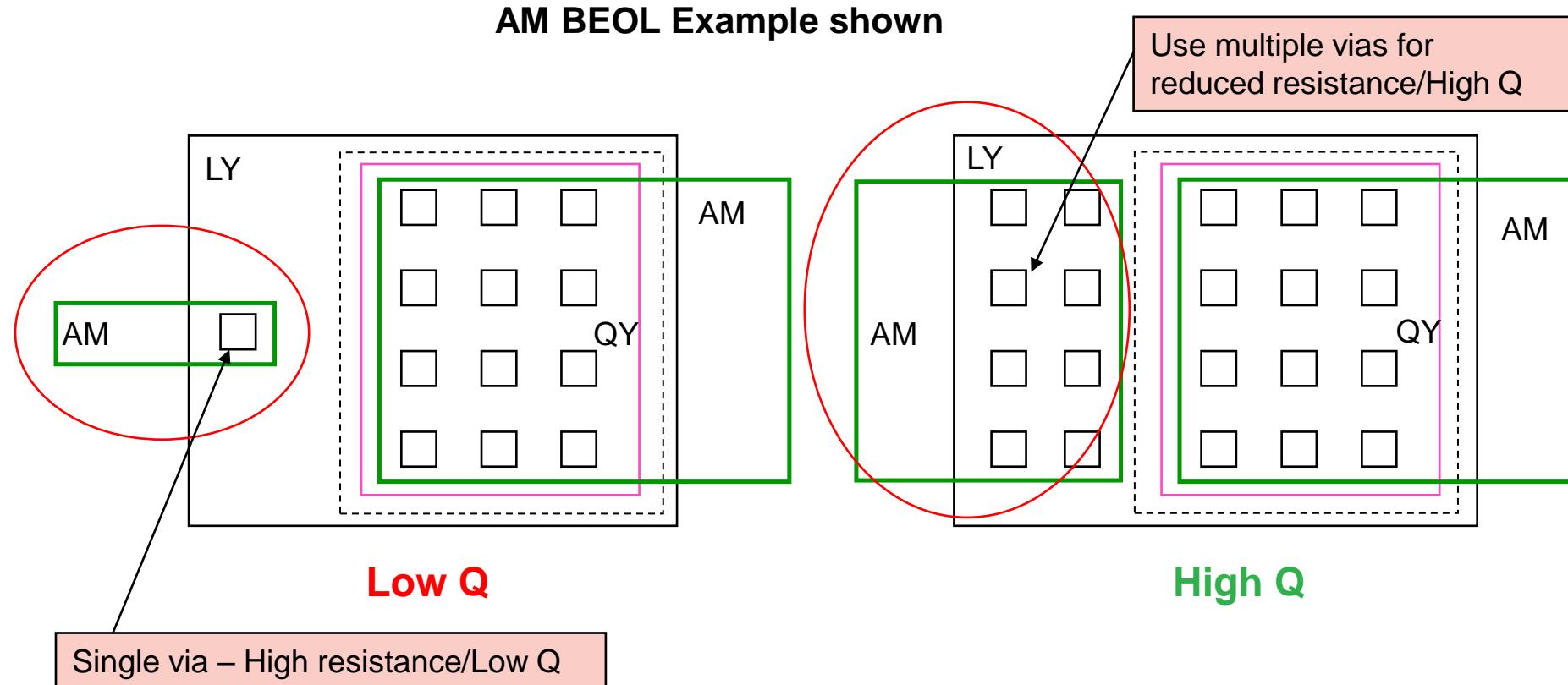


NOTE: Segmented guard ring option available in bicmos8HP Chipguardring pcell

# Truncated Guard Rings



# MIM Bottom Plate Connections

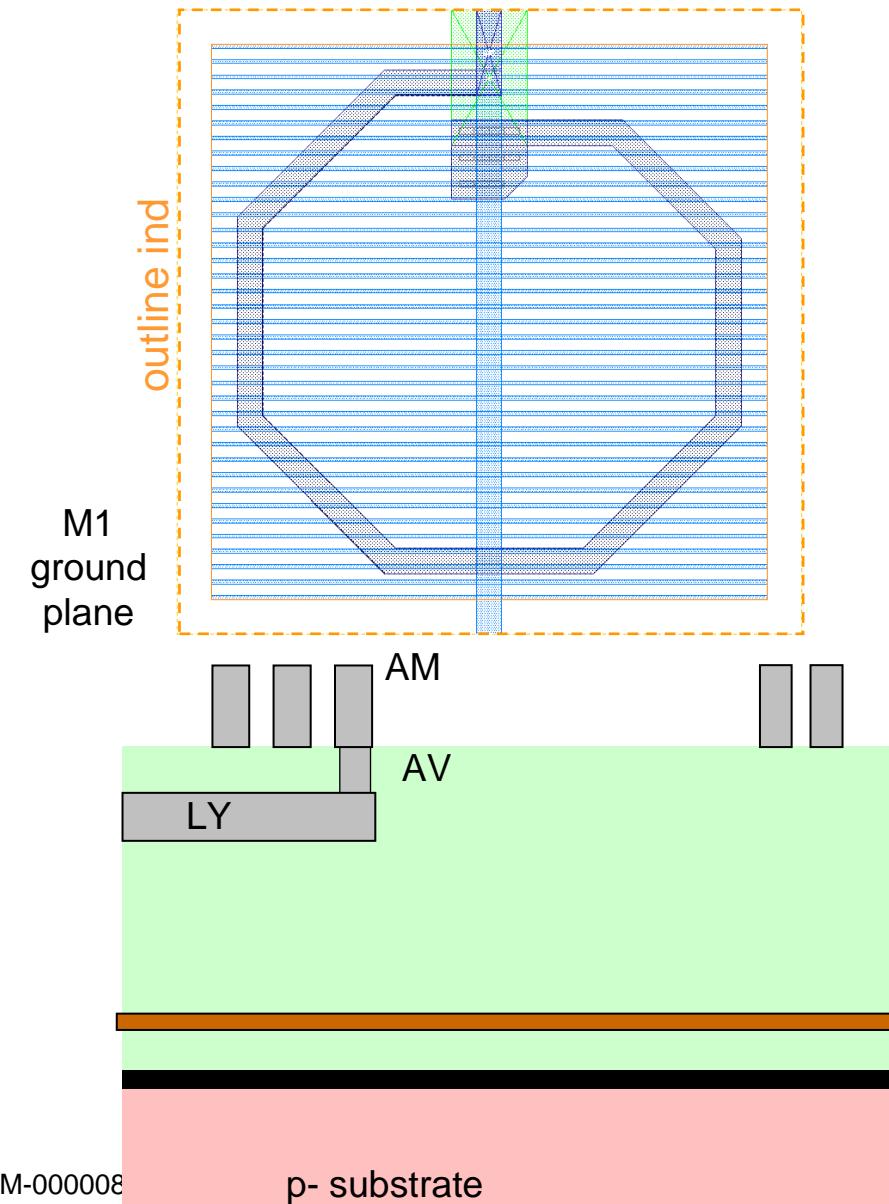


Bottom plate connections are not determined by the pcell. Pcell shapes are within dashed outline.

# Inductor Layout Considerations\*

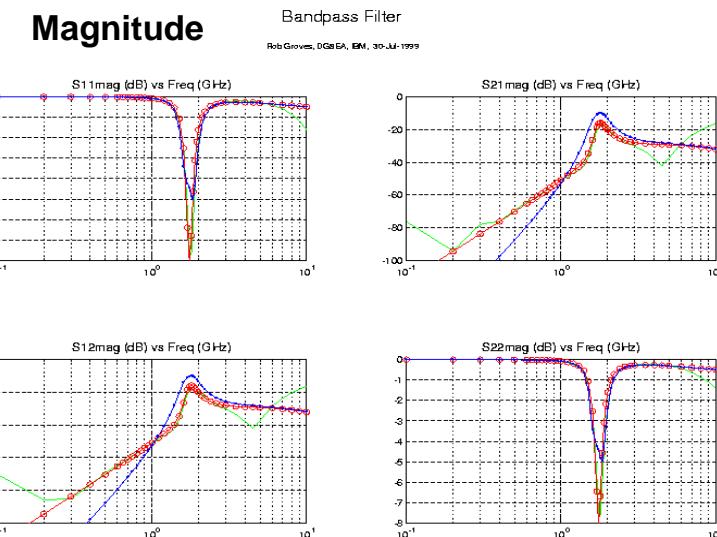
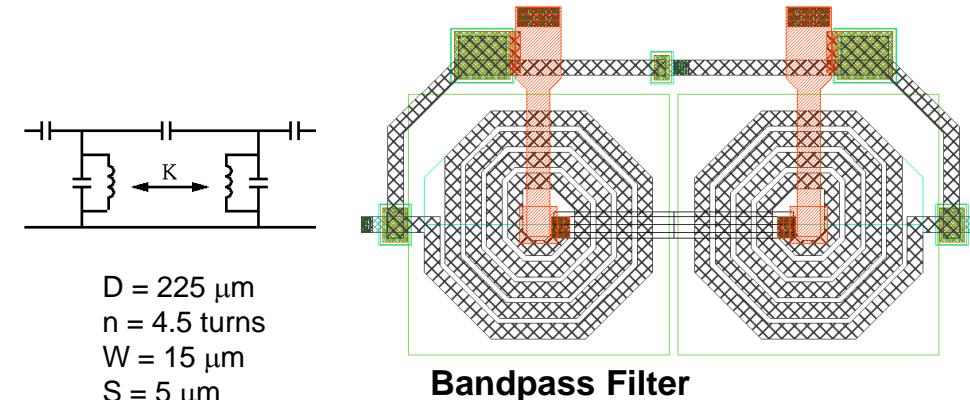
- Avoid large conducting planes and closed current paths around inductor (peak Q, self-resonance decrease)
- Place spiral  $>80\mu\text{m}$  from large substrate contacts
  - 50  $\mu\text{m}$  as an absolute minimum
- Place spiral at least 110  $\mu\text{m}$  away from C4 and 83  $\mu\text{m}$  away from wire bond pads
  - Avoid Induced eddy current in large metal
  - Minimize coupling and power loss
- Be aware of magnetically coupled feedback paths in high-gain circuits.
  - Adjacent or nearby inductor couple signals
- Recognition shape “outline” “ind”
  - Reduces RX, PC, and metal fill density underneath device
  - Device extraction and DRC
- DRC will identify shorted coils

\*See Sections 4.19 in the Design Manual also

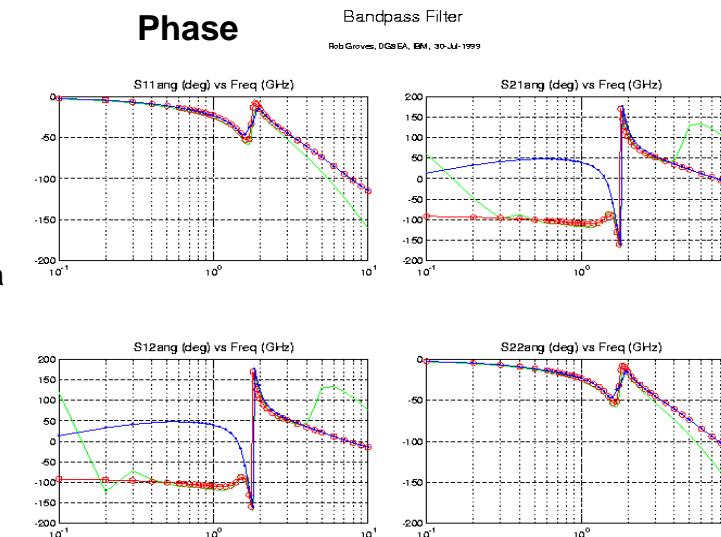


# Spiral Inductor Coupling – CMRF6SF Example

- Case Study: 1.9GHz Band pass filter with two spirals placed 40  $\mu\text{m}$  apart.
- Infer coupling coefficient by comparing measured S-parameters with simulated filter performance.
- Mutual coupling varies with the spacing as a fraction of inductor diameter.
- Insertion loss and Phase strongly affected by mutual coupling.
- The measured results for both Insertion Loss and Phase are closely matched by the simulation using  $K=0.1$ .
- Conclusion: Inductor separated by 20% of its diameter, the mutual coupling coefficient is about 0.1.



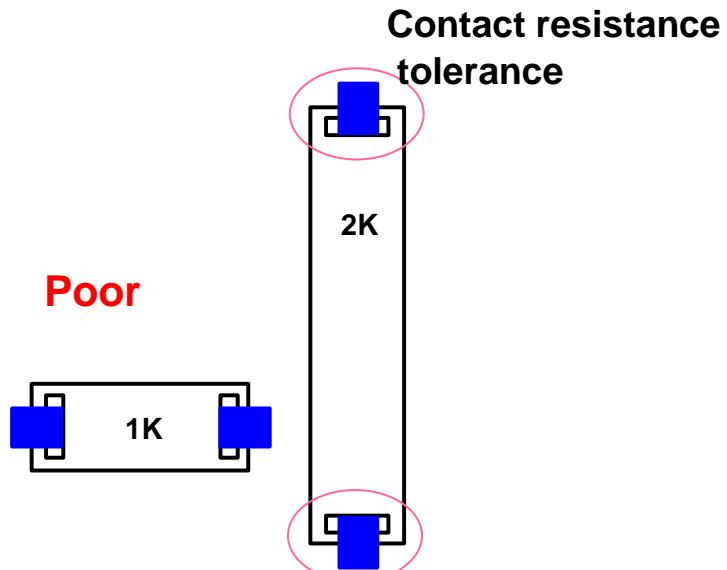
Green: measured data  
Blue: Model,  $k = 0$   
Red: Model,  $k = 0.1$



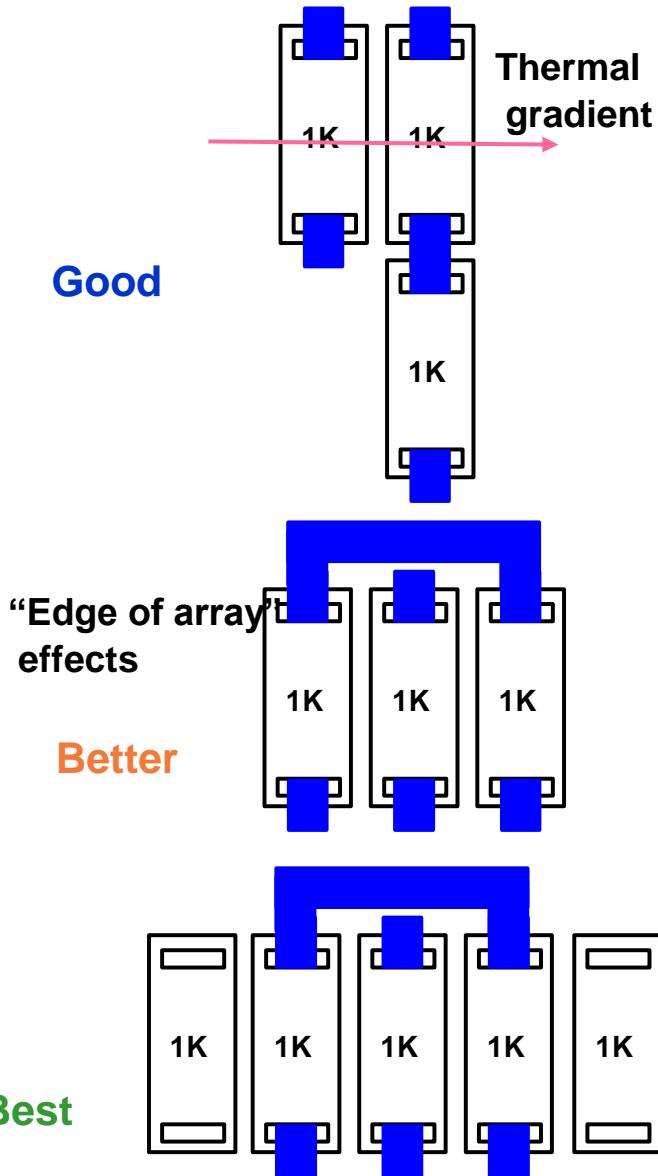
# Matching and Ratio Control

Reduce effects of process and thermal gradients through

- Small device separation
- Identical structures and orientation
- Unit cell approach
- Common geometric center
- Dummy cells



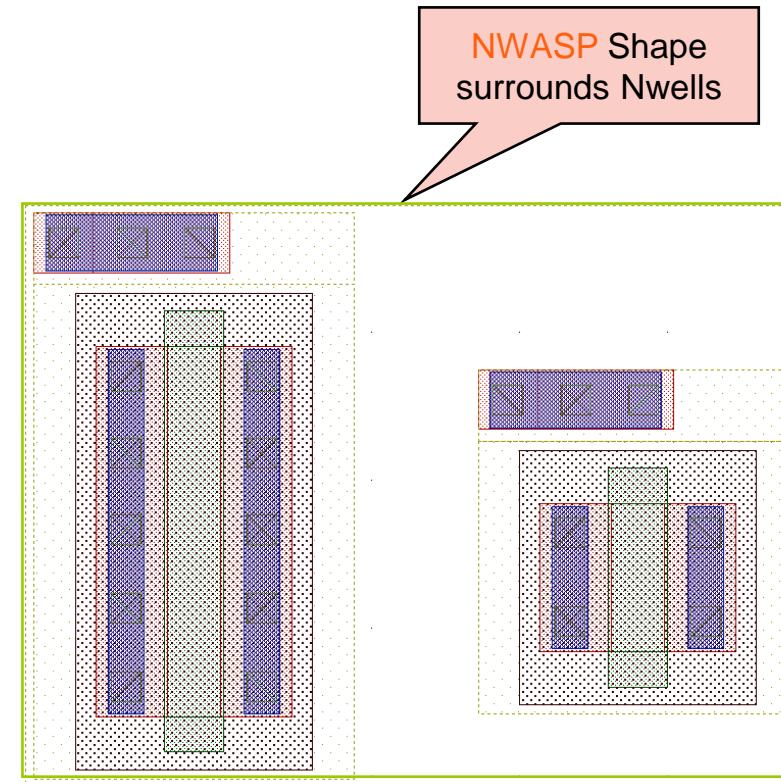
Poor



Best

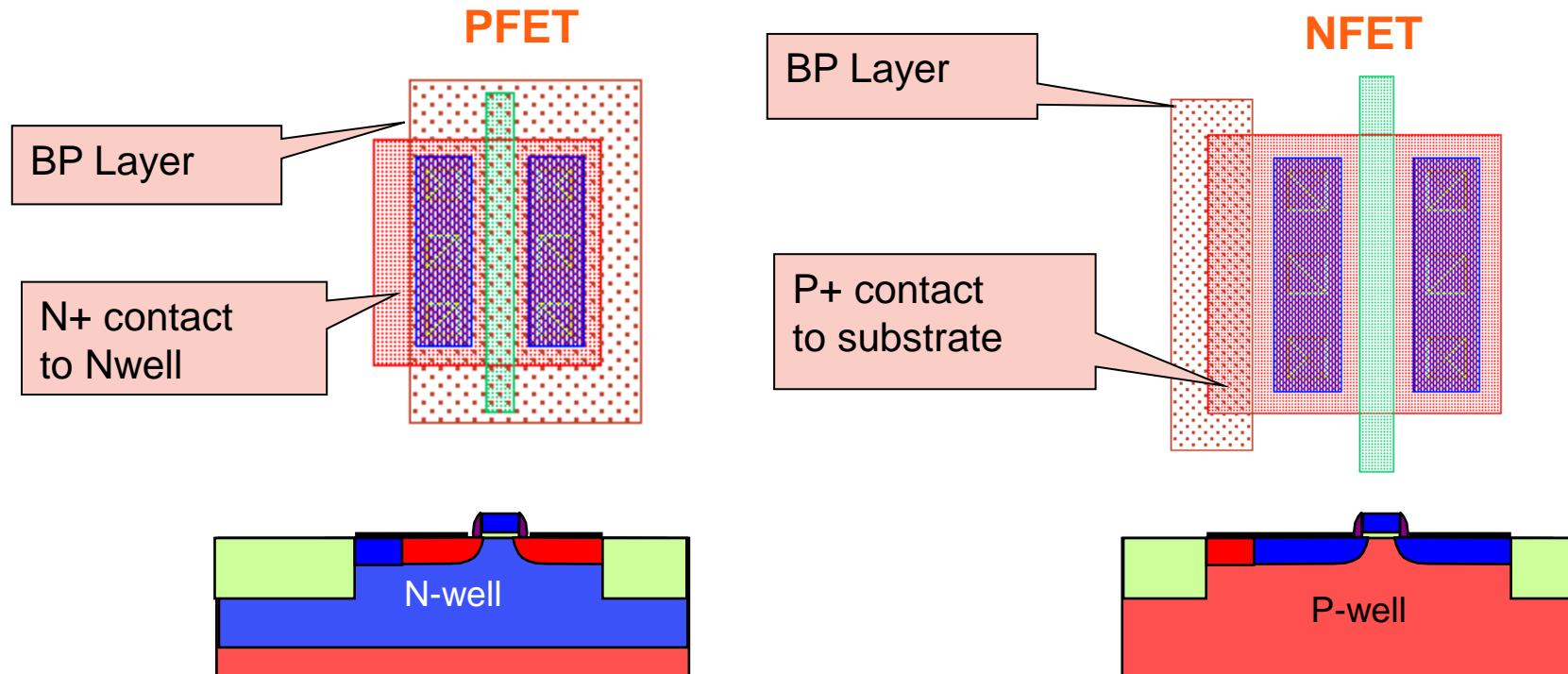
# N-wells At Same Potential – GR 252b

- NWASP shape must surround both n-wells
- No RX allowed between n-wells with reduced spacing
- N-well spacing reduced from  $0.92\mu\text{m}$  to  $0.70\mu\text{m}$ 
  - No need for isolation from N-well to N-well at same potential

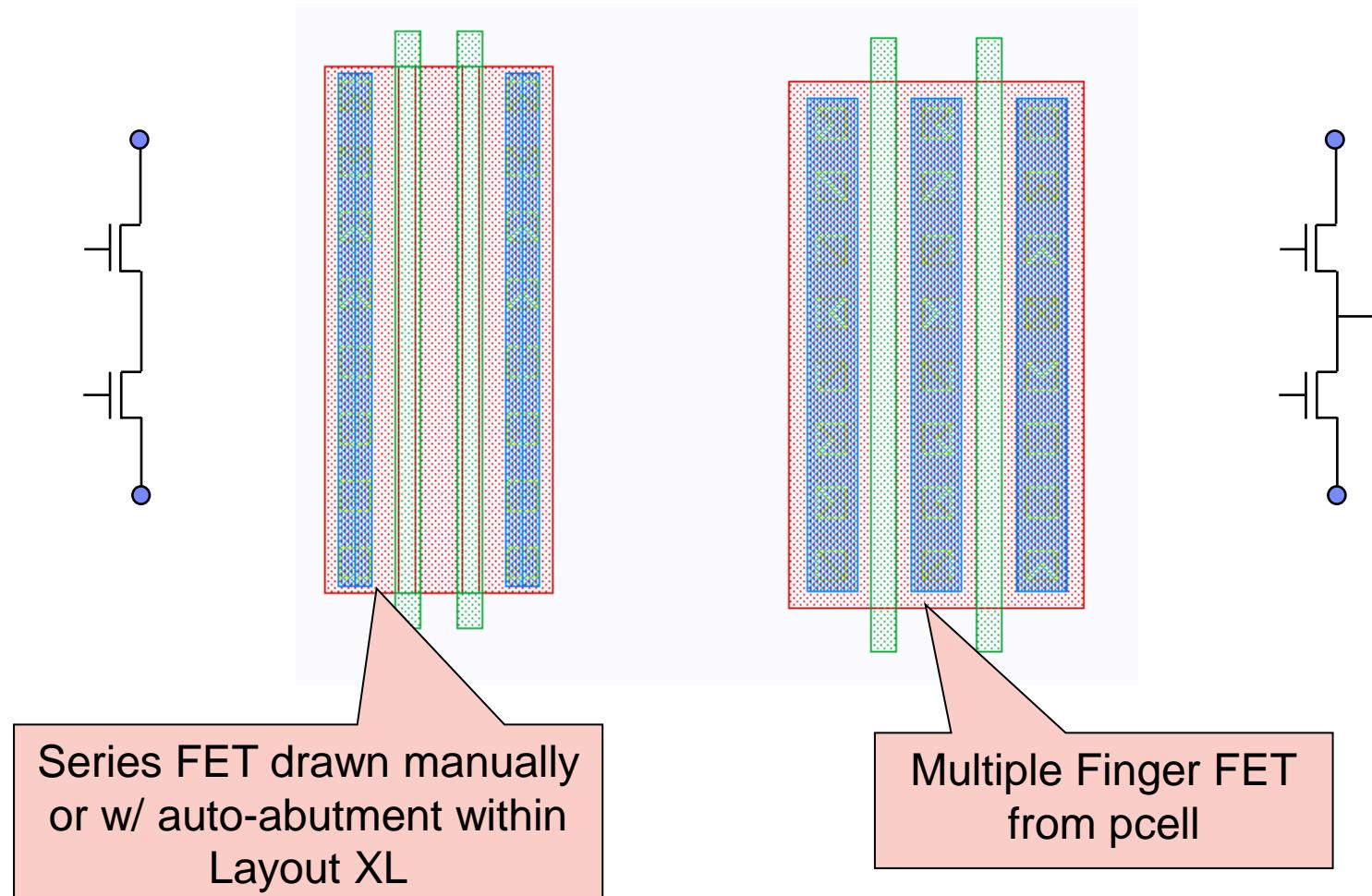


# Butted Junctions

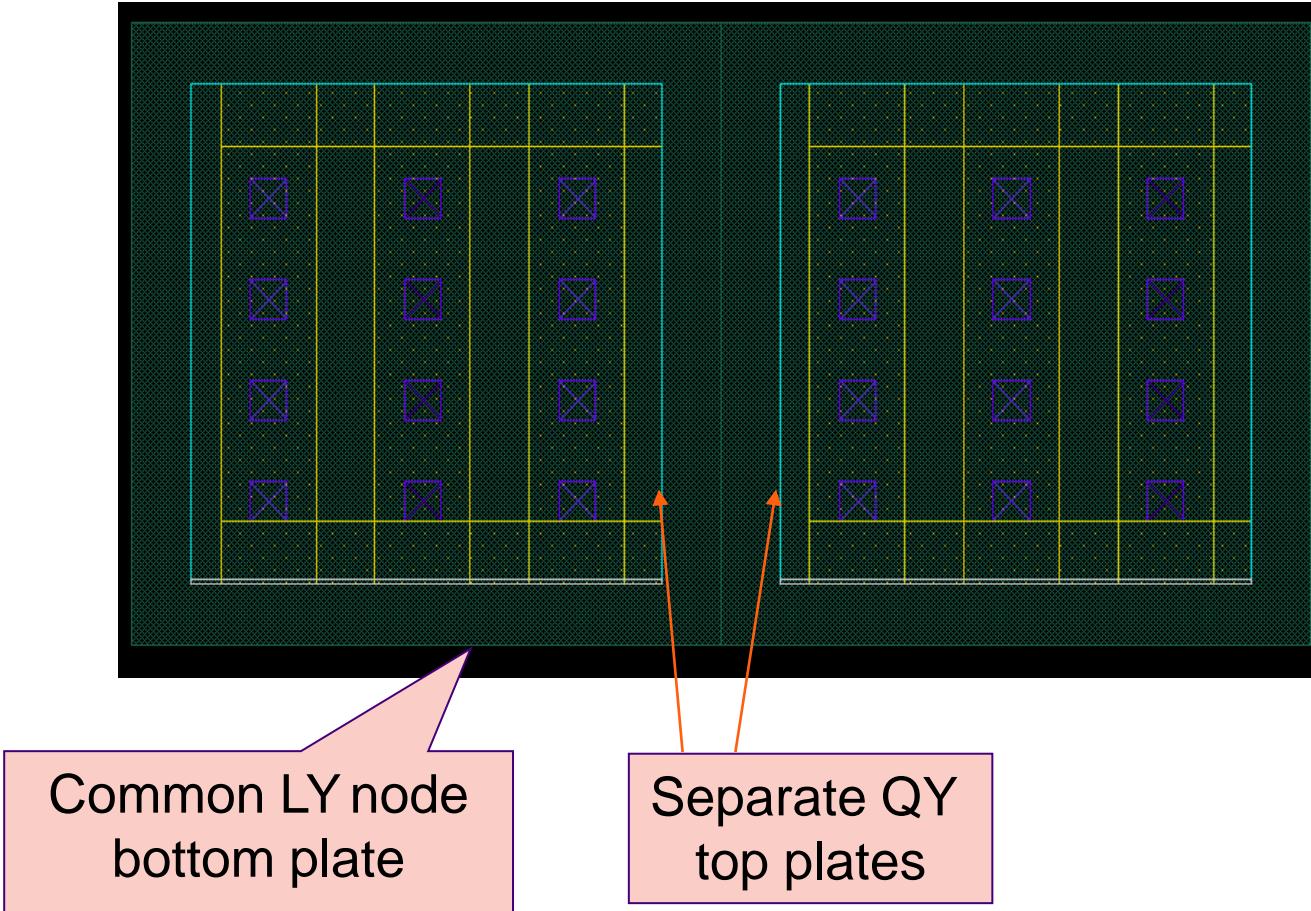
- SX or NW contact in the same RX diffusion as FET Source
- A butted junction in close proximity to an FET can affect the device
  - Butted junctions not recommended in analog, matching, or performance-critical circuits
- Source contact required – the lateral current carrying capability of the silicide



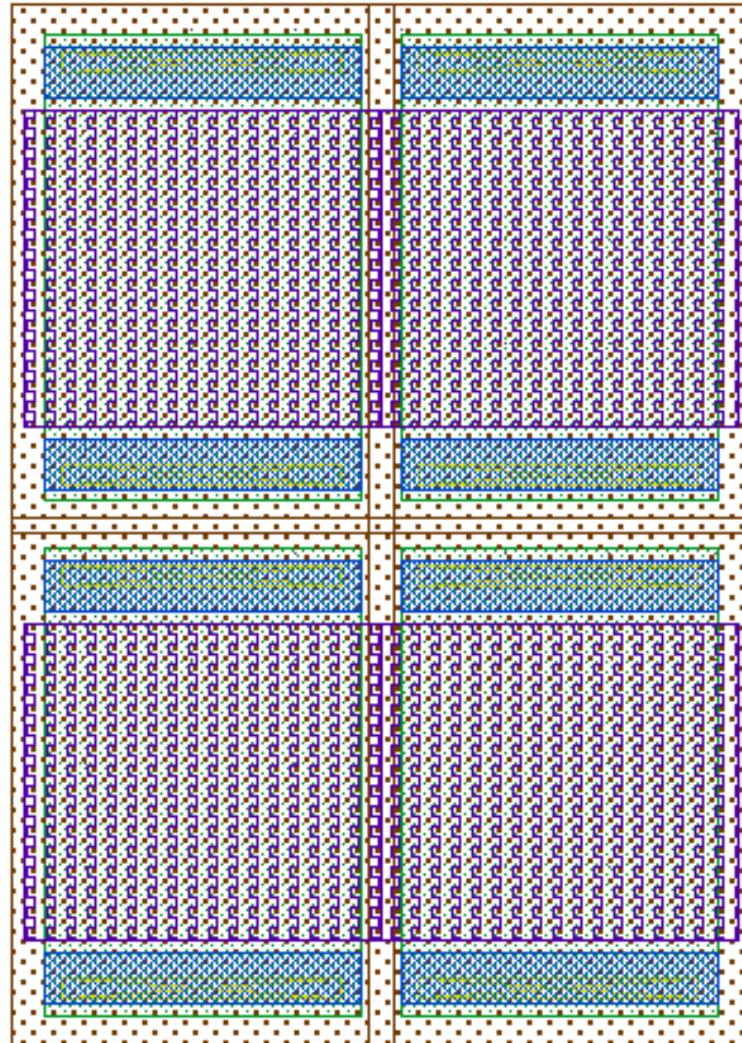
# FETs Sharing Common Active Region



# MIMs with Common Bottom Plate



# Resistors with Shared Shapes



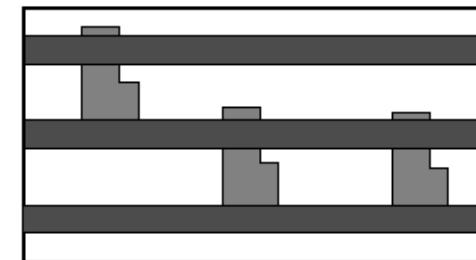
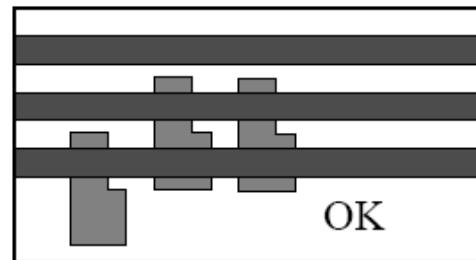
oppcres pcells placed such that OP shapes touch and the BP shapes merge

# Design for Manufacturability (DFM)

- Design practices can be optimized to increase defect-limited yields by optimizing white space in the design
  - Large effect on defect density and on critical area
- Some DFM practices are guidelines and cannot be easily coded in DRC deck. Examples:
  - Isolated vias (via opens)
  - Tightly Nested vias on different nets (via shorts)
  - Spread wires apart as space allows (shorts)
- Non-minimum Recommended, ‘R’, design rules with priorities (1 through 4, 1- Highest, 4-Least) summarized in the BiCMOS8HP Design Manual - Table 7-1, Section 7.1.1
  - Rules may not be coded in the BiCMOS8HP/BICMOS8XP DRC decks.
  - Recommended PC and RX Rules
    - Involve relaxing minimum ground rules
    - Reduce the critical area where defects are more likely to be fatal
    - Implement whenever there is no impact to chip performance and no impact to chip size/cost
    - Consider the rule priority and design tradeoff
  - Recommended CA Contact and NW Rules
    - Ensure repeatable well landed contacts to reduce the chance of opening
    - Ensure adequate spacing to avoid leakage considering printing bias
  - Recommended Metal (Mx) and Via (Vx) Rules
    - Avoid metal line shorting and open, under-contact vias

# Yield Enhancement Design Techniques

- **Space out elements as much as possible within the available space**
  - Wiring limited → Spread out the devices
  - Device limited → Spread out the wires

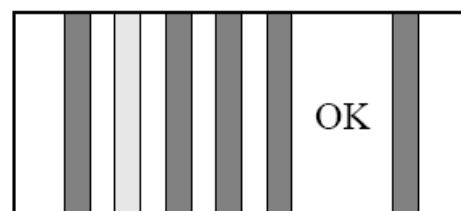


Better

See the Design  
Manual section 7.1  
“Yield Enhancement  
Design Techniques”  
for tips on layout for  
high yield.

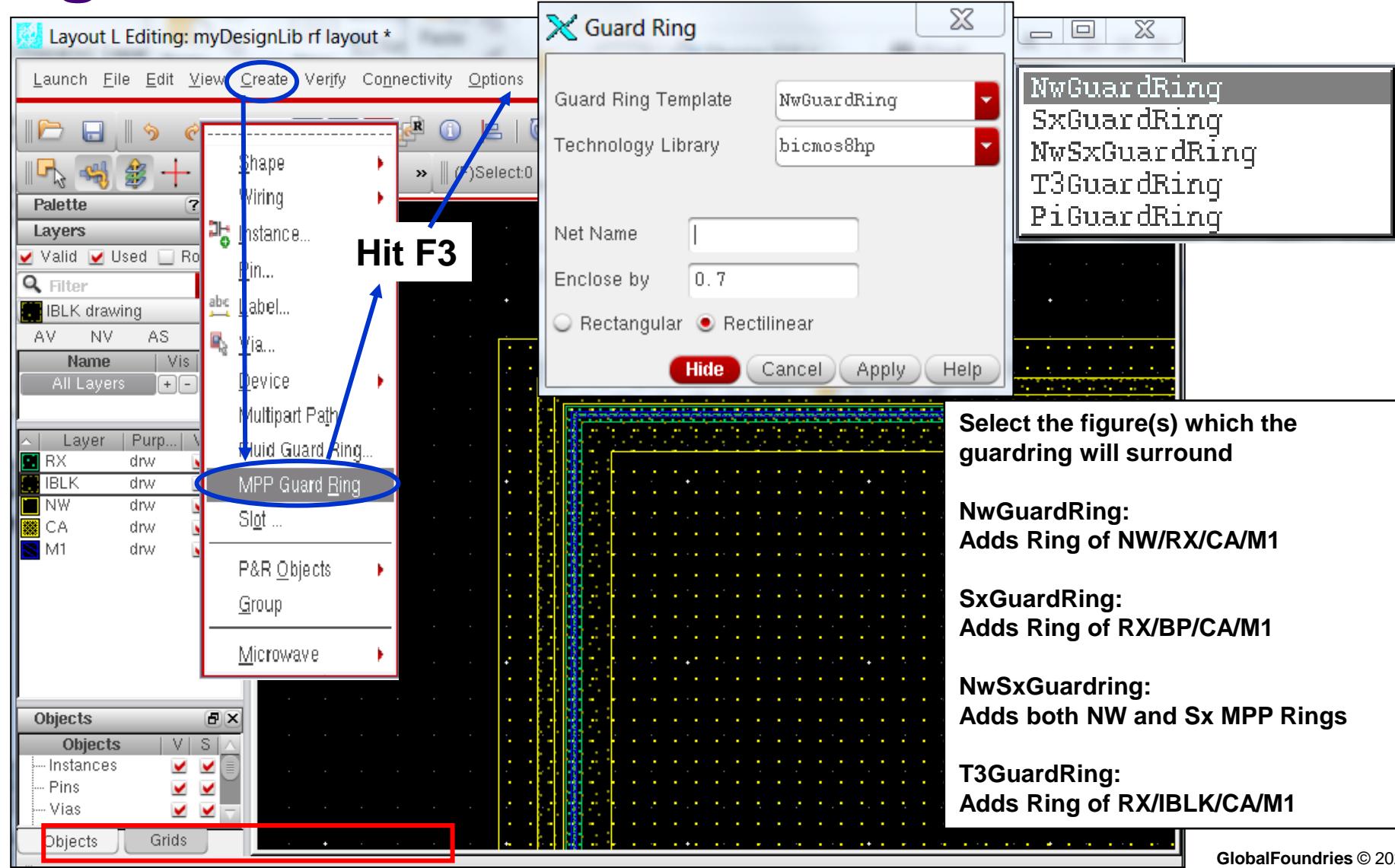
- **Distribute the wiring:**

- Within a layer, spread out the wires, and balance the wiring between levels.
- Avoid a very dense level matched with a very sparse level.



Better

# Multipart Path GuardRings - supported through techfile



# Multipart paths /continued

The screenshot shows the Virtuoso Layout Suite interface. In the top menu, 'Create' is circled in blue. A context menu is open over a 'Hit F3' label, with 'Multipart Path' highlighted and also circled in blue. The 'Create Multipart Path' dialog box is open, showing settings for 'Template Name: NwGuardRing', 'Name: path1', 'Technology Library: bimcos8hp', and 'Width: 0.72'. The right side of the dialog lists available templates: NwGuardRing, SxGuardRing, NwSxGuardRing, T3GuardRing, and PiGuardRing.

**NwGuardRing:**  
Adds NW/RX/CA/M1  
Useful for creating NW contacts

**SxGuardRing:**  
Adds RX/BP/CA/M1  
Useful for creating substrate and isolated pwell (N3 over NW) contacts

**NwSxGuardring:**  
Adds both MPPs

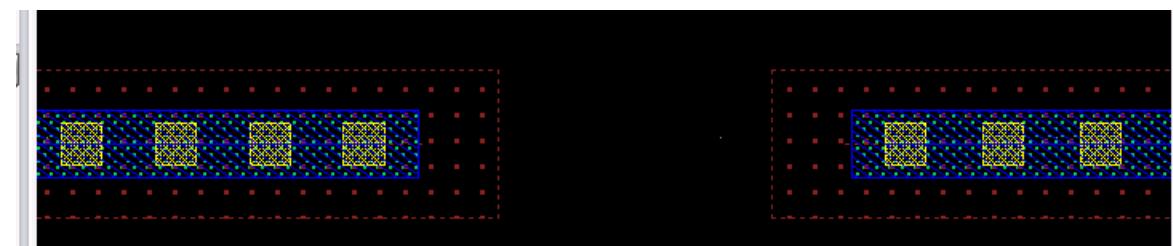
**T3GuardRing:**  
Adds RX/IBLK/CA/M1

CAD group can create custom MPP by editing techfile

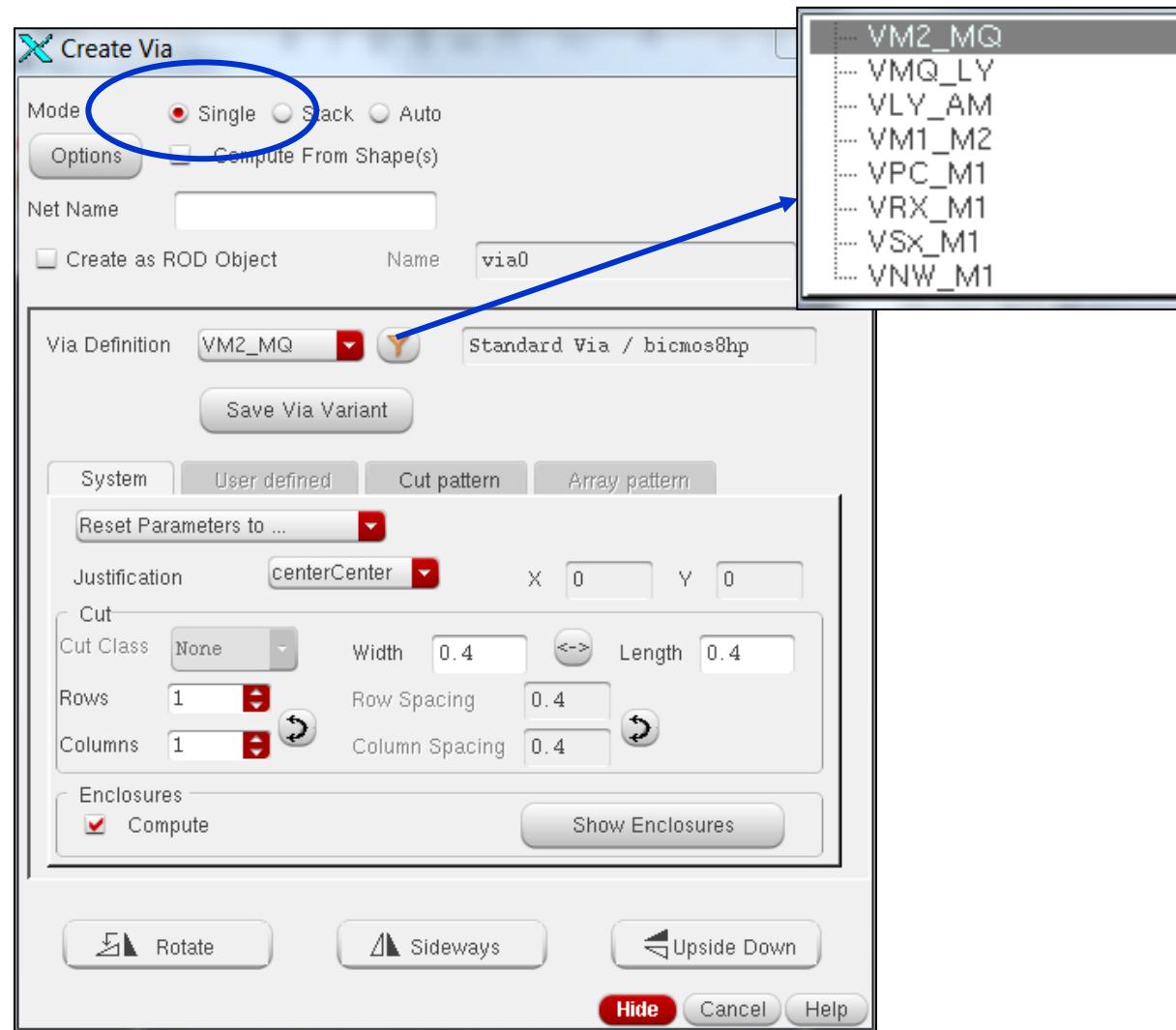
# MPP/continued

- Multipart Paths can be stretched or chopped after placement
- Borders around the contacts maintained (i.e. remain DRC clean)

```
multipartPathTemplates(  
; ( name [masterPath] [offsetSubpaths] [encSubPaths] [subRects] )  
;  
; masterPath:  
; (layer [width] [choppable] [endType] [beginExt] [endExt] [justify] [offset]  
; [connectivity])  
;  
; offsetSubpaths:  
; (layer [width] [choppable] [separation] [justification] [begOffset] [endOffset]  
; [connectivity])  
;  
; encSubPaths:  
; (layer [enclosure] [choppable] [separation] [begOffset] [endOffset]  
; [connectivity])  
;  
; subRects:  
; (layer [width] [length] [choppable] [separation] [justification] [space] [begOffset] [endOffset] [gap]  
; [connectivity] [beginSegOffset] [endSegOffset])  
;  
; connectivity:  
; ([I/O type] [pin] [accDir] [dispPinName] [height] [ layer]  
; [layer] [justification] [font] [textOptions] [orientation]  
; [refHandle] [offset])  
;  
; ( _____ )  
; (NuGuardRing  
; ("NW" "drawing") 0.72 nil extend 0 0 center )  
; (((RX" "drawing") 0.28 t)  
; ((M1" "drawing") 0.16 t)  
; (("NW" "drawing") 0.02 nil 0 right ))  
; )  
; nil  
; (((CA" "drawing") 0.16 0.16 t)  
; )  
;  
; (SxGuardRing  
; ("RX" "drawing") 0.28 t extend 0 0 center )  
;
```

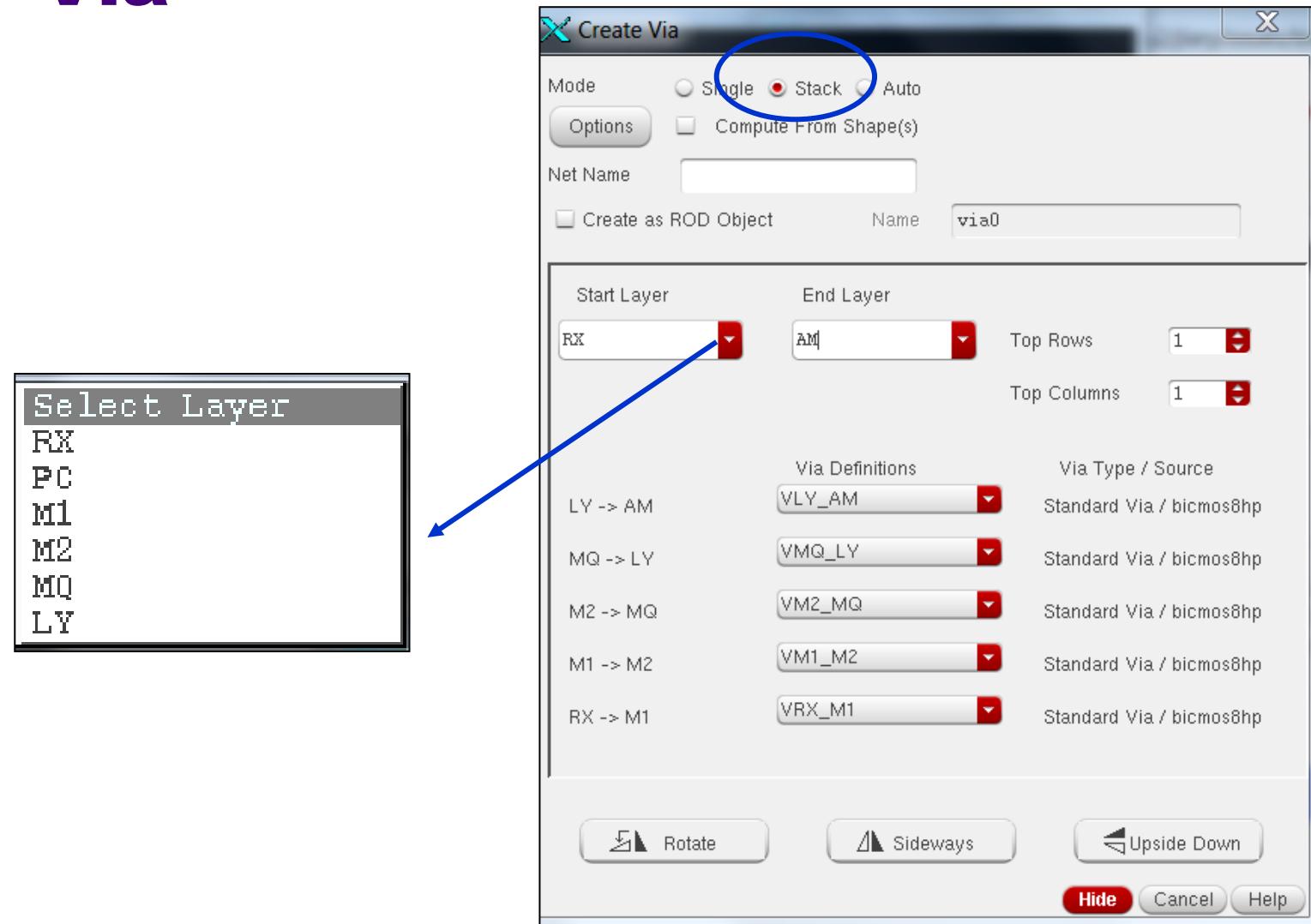


# vias supported through techfile - single vias Create → Via



# vias supported through techfile - stacked vias

## Create → Via





# **Design Kit Installation, Documentation and Support**

# BiCMOS8HP Design Kits and Supported Tools

## ▪ PDK Infrastructure

- Common infrastructure across all GlobalFoundries PDKs
- Each design kit component appears using the following hierarchy:  
`<PDK Install dir> / <Tech> / <Release> / <ToolType> / <ToolName>`
  - As an example, the Calibre DRC component is now located in the following path:  
`<customerRootDir>/bicmos8hp/V1.8_5.5/DRC/Calibre/`
- Environment variable setting “`GF_PDK_HOME`” is required prior to launching Cadence  
`Export GF_PDK_HOME = <PDK Install dir> /bicmos8hp/ V1.8_5.5`  
(or)  
`setenv GF_PDK_HOME <PDK Install dir> /bicmos8hp/ V1.8_5.5`

## • PDK Directory Structure

- `/Models/ Spectre, ADS (Dynamic Link), GoldenGate, HSPICE`
- `/DRC & LVS/Calibre, PVS`
- `/PEX/QRC, xRC`
- `/Emagnetic/ EMX, Momentum, Peakview, ITF`
- `/PlaceRoute/Innovus,ICC`
- `/doc/Design Manual, Model Ref Guide, ESD Ref Guide, LUP Ref Guide, Release Notes,`
- `/DesignEnv/ADS, ViewLayout,VirtuosoOA`
- `/Setup/install`
- `/FILLGEN/Calibre, PVS`
- `/ESD/PERC_LDL`
- `EMIR/Redhawk_Totem, Voltus_VoltusFI`

# Design Kit Versioning

- PDK releases are identified by a versioning scheme
- The letter V followed by four digits delimited by a period
- For example V1.8\_5.5
- Vw.x.y.z
  - **w = technology maturity**
    - **0 = alpha-level**
    - **1 = beta-level**
    - **2 = production-level**
  - **x = major release**
  - **y = interim release or hot fix**
  - **z = partial kit release/patch**
    - **Patch releases are cumulative**
      - Only need to install latest patch, contains updates from prior patches

# CMOS8HP V1.8\_5.5 PDK Vendor Tool Versions

This is a BiCMOS8HP/XP (130HPSIGE-8HP/XP) PDK patch release.

Supported tool versions for BiCMOS8HP/XP	
Tool	Version
Cadence Virtuoso	IC6.1.8-64b.500.11
Assura DRC	04.16.107_OA618
Assura LVS	04.16.001_OA618
Mentor Calibre DRC/LVS/xRC	2019.4_46.30
Cadence PVS DRC/LVS	19.12.000
Cadence QRC	19.13.020
Cadence Spectre (MMSIM)	MMSIM 19.10.237.ISR3
Keysight ADS	2020 update 1.0
Synopsys HSPICE	Q-2020.03

Note: Recommend to check bicmos8hp\_PDK\_ReleaseNotes.pdf file for supported tool versions in each kit version

# PDK Download (1)

From Global-FoundryView:

PDK & Design Documents → Process Design Kits (PDK) → Select 0.13um for Technology and 130HPSIGE-8HP-8XP → PDK 130HPSIGE-8HP

The screenshot shows the Global-FoundryView web application interface. The top navigation bar includes Home, Notifications (1), Accounts, Contacts, My Devices, My Wafers, Products & Services, PDK & Design Documents (highlighted in green), Team Rooms, Cases, and Groups. A search bar is located in the top right. The main content area has a banner image of a cleanroom. On the left, a sidebar menu lists Technology Solution Guide, PDK & Design Documents (selected, highlighted in blue), Foundry (Design Technology Documents, IP Design Kits, Process Design Kits (PDK) selected, highlighted in orange), and Incoming PDK. The main panel title is "Process Design Kits (PDK)". It shows dropdown menus for Technology (0.13UM) and Product (130HPSIGE-8HP-8XP). Below these are two checkboxes: "PDK 130HPSIGE-8HP V18.5.5 - Documents" (selected, highlighted in blue) and "PDK 130HPSIGE-8HP V18.5.5 - Metadata". A callout box labeled "3" points to the "Technology" dropdown. A callout box labeled "4" points to the "Documents" checkbox. To the right, a table lists the PDK details: PDK-000308, 0.13UM, GLOBALFOUNDRIES 130HPSIGE-8HP V18.5.0 PDK, Metal Stacks, and a list of metal stacks: 411 - M1\_M2\_M3\_M4\_MQ\_LY\_AM, 413 - M1\_M2\_M3\_M4\_MQ\_LY\_E1\_MA, 211 - M1\_M2\_MQ\_LY\_AM, 311 - M1\_M2\_M3\_MQ\_LY\_AM, 313 - M1\_M2\_M3\_MQ\_LY\_E1\_MA, 213 - M1\_M2\_MQ\_LY\_E1\_MA. A search bar at the bottom right says "Search your Provisioned Kits".

# PDK Download (2)

The screenshot shows a software interface for managing Process Design Kits (PDKs). At the top, there is a navigation bar with various links: Home, Chatter, Groups, Files, Ideas, PDK & Design Documents (which is the active tab), Cases, Bug/Work Requests, Dashboards, Reports, Accounts, Devices, Team Rooms, Master PDKs, Package, Specifications, ASIC IP Requests, Manage Email Notification, Waiver Collaborator, and a plus sign icon.

The main content area is titled "Process Design Kits (PDK)". It displays two dropdown menus: "0.13UM" and "130HPSIGE-8HP-8XP". Below these is a search bar with the placeholder "Search your Provisioned Kits" and a magnifying glass icon.

A sidebar on the left is titled "PDK & Design Documents" and contains a "Foundry" section with the following items:

- Design Technology Documents
- IP Design Kits
- Process Design Kits (PDK) (this item is highlighted in orange)

The main panel has a heading "Process Design Kits" and a "Subscribe Folder" button, which is highlighted with a green box and a purple arrow pointing to it. Below this are two buttons: "Email Link" and "Subscribe Selected Item(s)".

The table below has columns for "PDK Name", "PDK ID", "PDK Tech Geometry", "PDK Technology", and "PDK Last Updated".

Select **SubscribeFolder** to get notification when updates are available

# PDK Download (3)

Select desired PDK Components for download

PDK 130HPSIGE-8HP V1.8\_5.5 - Documents

V1.8_5.0_BASE (29-Jul-2020)	V1.8_5.1 (02-Sep-2020)	V1.8_5.2 (15-Sep-2020)	V1.8_5.3 (20-Nov-2020)	V1.8_5.3a (02-Dec-2020)	V1.8_5.4 (19-Mar-2021)	V1.8_5.5 (03-Jun-2021)
<input type="checkbox"/> Document Number  Filter DE Components	<input type="checkbox"/> Document Title  Filter DE Components	<input type="checkbox"/> Revision  Filter Revision	<input type="checkbox"/> Enablement  Filter Enablement	<input type="checkbox"/> Version		
<input type="checkbox"/> DE-000747	<input type="checkbox"/> PVS FILLGEN (130HPSIGE-8HP)		2	Other DE Specifications	V1.8_5.5	
<input type="checkbox"/> DOC-000179	<input type="checkbox"/> PDK Documentation (130HPSIGE-8HP)		16	PDK Documentation	V1.8_5.5	
<input type="checkbox"/> DRC-PV-000063	<input type="checkbox"/> PVS DRC (130HPSIGE-8HP)		10	DRC Runsets	V1.8_5.5	
<input type="checkbox"/> DRC-CC-000330	<input type="checkbox"/> Calibre DRC (130HPSIGE-8HP)		10	DRC Runsets	V1.8_5.5	
<input type="checkbox"/> DE-000439	<input type="checkbox"/> Calibre FIL GEN (130HPSIGE-8HP)		6	Other DE Specifications	V1.8_5.5	
<input type="checkbox"/> DM-000418	<input type="checkbox"/> Design Manual (130HPSIGE-8HP)		11	Design Manuals	V1.8_5.5	
<input type="checkbox"/> PR-000277	<input type="checkbox"/> PlaceRoute Cadence Innovus (130HPSIGE-8HP)		7	Place & Routes (P&R)	V1.8_5.5	
<input type="checkbox"/> EMIR-000137	<input type="checkbox"/> EMIR Apache Redhawk Item (130HPSIGE-8HP)		3	Electro-Migration/IR Check	V1.8_5.5	
<input type="checkbox"/> PR-000354	<input type="checkbox"/> PlaceRoute Synopsys ICC (130HPSIGE-8HP)				V1.8_5.5	

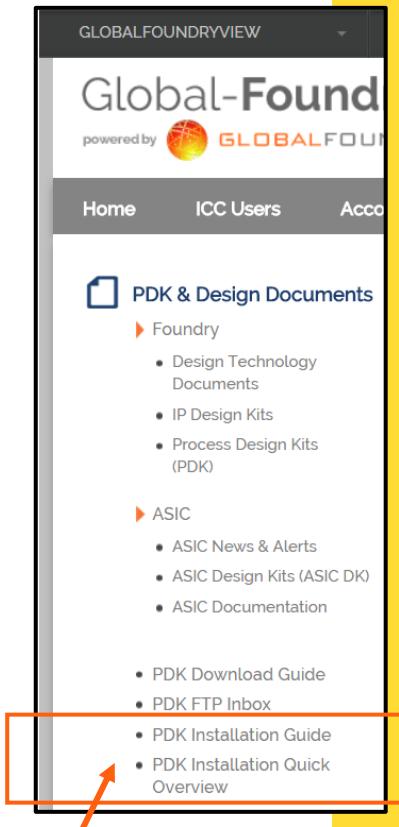
Document Title      File Name      Size

Document Title	File Name	Size
 Filter Document Title	 Filter File Name	
<input checked="" type="checkbox"/> Calibre DRC (130HPSIGE-8HP)	pdk-130HPSIGE-8HP-V1.8_5.5_DRC_Calibre.tar.gz	842 KB
<input checked="" type="checkbox"/> Calibre DRC (130HPSIGE-8HP)	pdk-130HPSIGE-8HP-V1.8_5.5_DRC_Calibre.tar.gz_update_20210601_162400+0000.log	1 KB

Each package released as \*.tar.gz  
log files (if displayed) are not required.

# PDK Installation

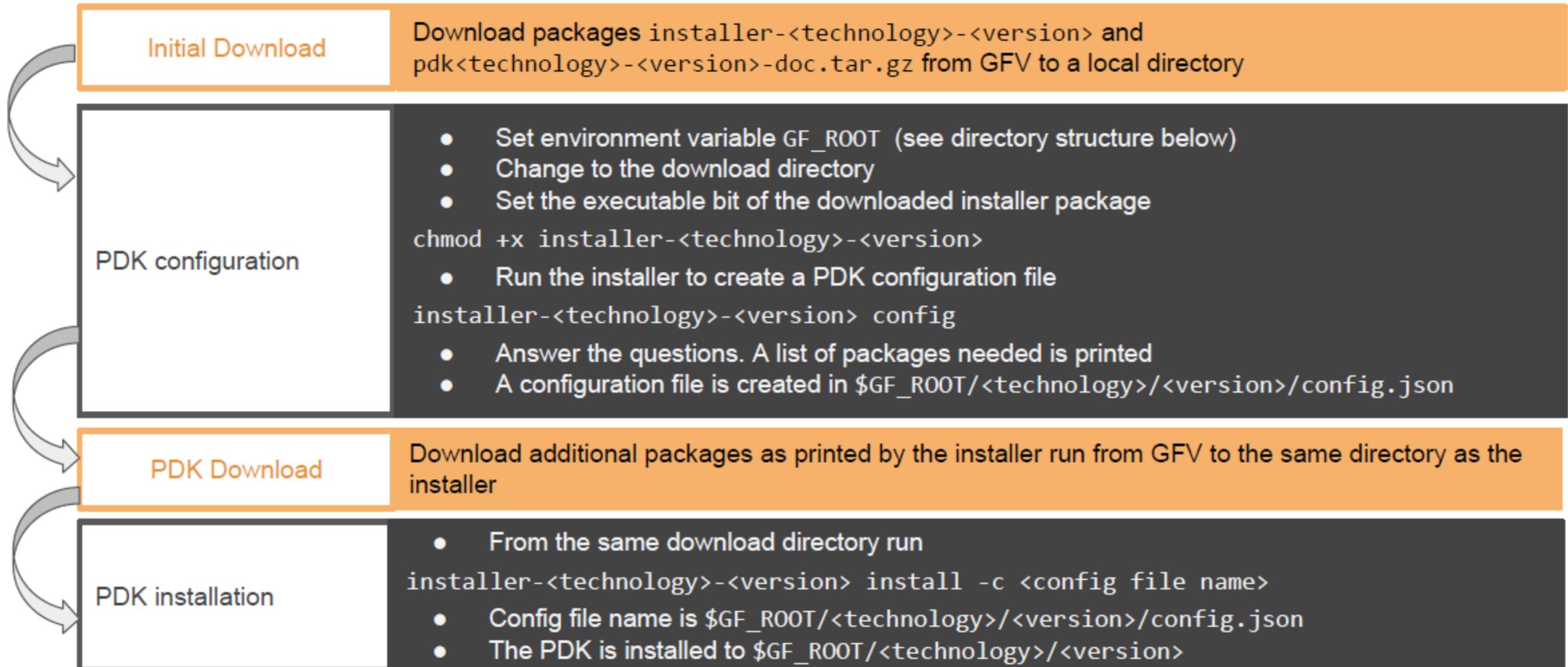
- Files can be manually unzipped/untarred into the customer specified PDK folder
  - Also can be installed by installer script provided in PDK
- It is recommended to follow the workflow and the directory structure described here.
- Additional information:
  - Read the documentation: `install.pdf` is in the `doc` package of your PDK
  - Look at the help text of the installer:
    - `install-<technology>-<version> -h` for general help
    - `install-<technology>-<version> config -h` for configuration help
    - `install-<technology>-<version> install -h` for installation help



Installer guide  
available in GF-V

# PDK Installation Contd...

## Recommended Workflow



# Cadence Quick Set Up

## ■ Set **GF\_PDK\_HOME** environment variable

- Must set prior to starting Cadence
- Set to the path of the PDK top level directory, i.e. the PDK installation level
  - e.g. /<GF\_ROOT>/<path>/130HPSIGE-8HP/V1.8\_5.5
  - Do not include the trailing "/" following the final directory of the path.

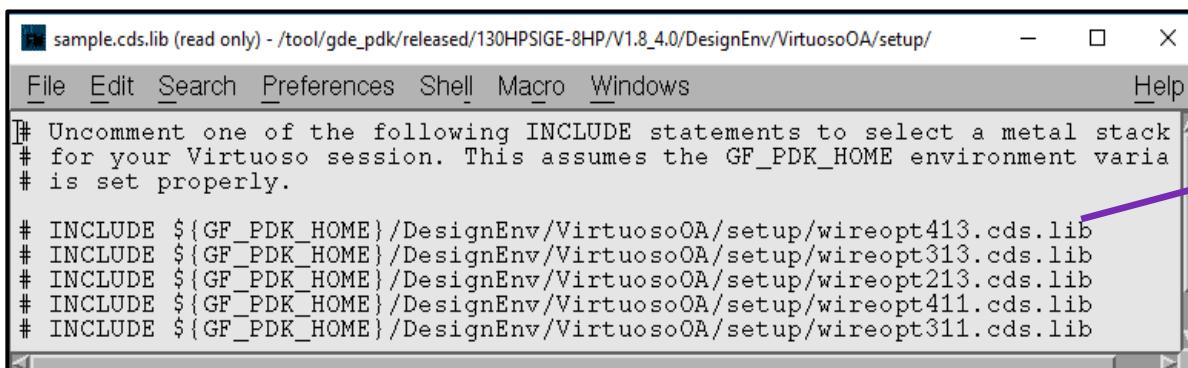
## ■ Copy essential files to start directory from **\$GF\_PDK\_HOME/DesignEnv/VirtuosoOA/setup/**

- **.cdsinit**, **.cdsenv**, **sample.cds.lib** and **display.drf**
  - PDK Bindkeys is preloaded in .cdsinit, update as needed.

```
load(strcat(gfPdkHome "/DesignEnv/VirtuosoOA/setup/ibmPdkBindkeys.i1"))
;Uncomment below for CDS-like bindkeys
;load(strcat(gfPdkHome "/DesignEnv/VirtuosoOA/setup/ibmPdkBindkeysCDS.i1"))
```

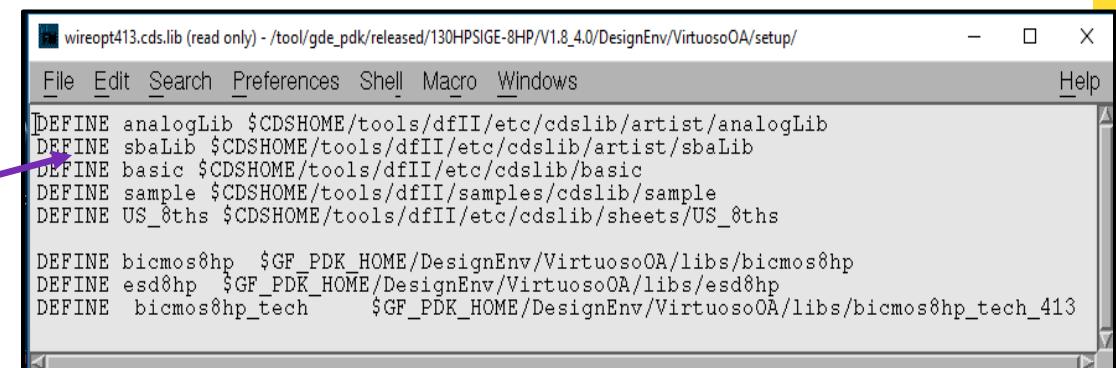
- Modify sample.cds.lib and rename the file to cds.lib

- Uncomment the needed metal stack for the design



```
# Uncomment one of the following INCLUDE statements to select a metal stack
# for your Virtuoso session. This assumes the GF_PDK_HOME environment varia
# is set properly.

# INCLUDE ${GF_PDK_HOME}/DesignEnv/VirtuosoOA/setup/wireopt413.cds.lib
# INCLUDE ${GF_PDK_HOME}/DesignEnv/VirtuosoOA/setup/wireopt313.cds.lib
# INCLUDE ${GF_PDK_HOME}/DesignEnv/VirtuosoOA/setup/wireopt213.cds.lib
# INCLUDE ${GF_PDK_HOME}/DesignEnv/VirtuosoOA/setup/wireopt411.cds.lib
# INCLUDE ${GF_PDK_HOME}/DesignEnv/VirtuosoOA/setup/wireopt311.cds.lib
```



```
DEFINE analogLib $CDSHOME/tools/dfII/etc/cdslib/artist/analogLib
DEFINE sbaLib $CDSHOME/tools/dfII/etc/cdslib/artist/sbaLib
DEFINE basic $CDSHOME/tools/dfII/etc/cdslib/basic
DEFINE sample $CDSHOME/tools/dfII/samples/cdslib/sample
DEFINE US_8ths $CDSHOME/tools/dfII/etc/cdslib/sheets/US_8ths

DEFINE bicmos8hp ${GF_PDK_HOME}/DesignEnv/VirtuosoOA/libs/bicmos8hp
DEFINE esd8hp ${GF_PDK_HOME}/DesignEnv/VirtuosoOA/libs/esd8hp
DEFINE bicmos8hp_tech ${GF_PDK_HOME}/DesignEnv/VirtuosoOA/libs/bicmos8hp_tech_413
```

# wireopt211.cds.lib Contents ( applies for other wireoptxxx.cds.lib also)

- Design kit offered “wireoptxxx.cds.lib” sample file defines all required PDK setup files.
  - “wireoptxxx\_cds.lib”, where xxx is the metal\_option (wireopt) supported by the PDK. One of them corresponds to the metal stack option used by a design library.
    - Standard Cadence supplied libraries
    - Device library/libraries
    - ESD library
    - Technology file library, “bicmos8hp\_tech”
      - ✓ Multiple stack compiled techfiles are supplied in the kit – the path definition for “bicmos8hp\_tech” identified which techfile is actually used, for example –

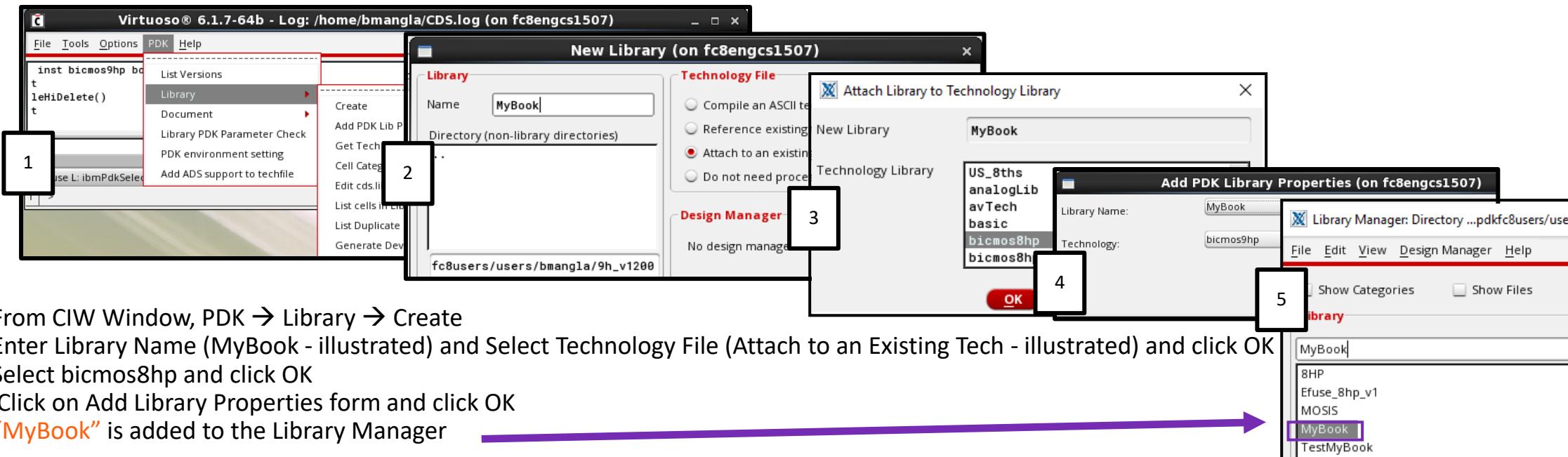
DEFINE bicmos8hp\_tech \$GF\_PDK\_HOME/DesignEnv/VirtuosoOA/libs/bicmos8hp\_tech\_211 (for 211)

- ✓ Multiple techfiles can be defined to support multiple metal stack featured design libraries co-existed in a same Cadence session, for example -

DEFINE bicmos8hp\_tech \$GF\_PDK\_HOME/DesignEnv/VirtuosoOA/libs/bicmos8hp\_tech\_211  
DEFINE bicmos8hp\_tech\_213 \$GF\_PDK\_HOME/DesignEnv/VirtuosoOA/libs/bicmos8hp\_tech\_213

# Create Design Library: Follow Steps 1 to 5

- Use the CIW menu PDK → Library → Create option
  - This defines GLOBALFOUNDRIES PDK library properties that are used by GLOBALFOUNDRIES PDK procedures and trigger functions.
- Attach to a reference library (“bicmos8hp” or “bicmos8hp\_tech”)
  - Recommended
  - Ensure appropriate metal stack definition of the “bicmos8hp\_tech” library in user cds.lib file
- Compiled with an alternate ASCII techFile
- All BEOL devices (MIMs, inductors, bondpads, vncap, ESDs) have a “`wireoptopt`” CDF parameter. The CallBacks rely on the metals defined in the techFile, responsible for the Pcells to draw the appropriate Metal layers.



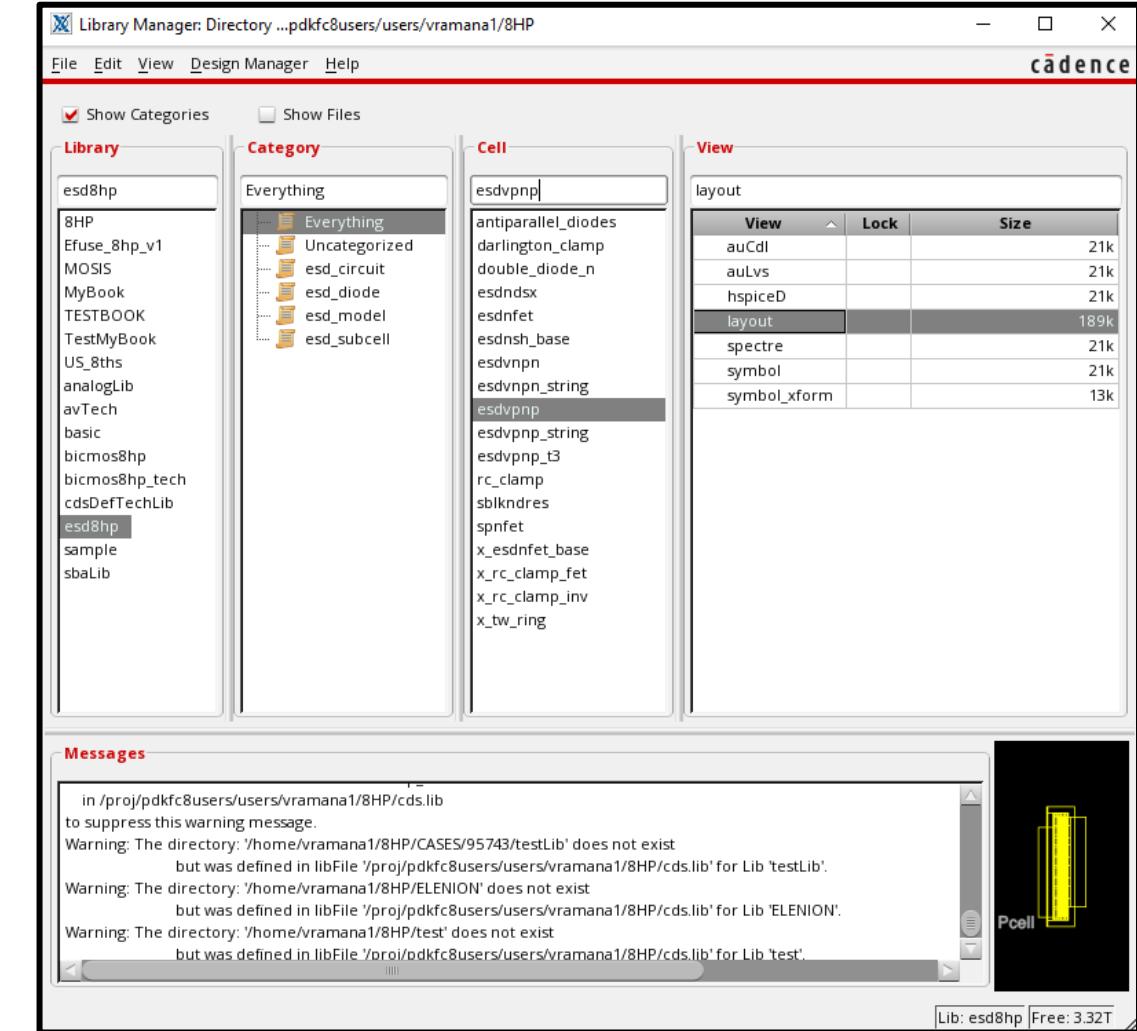
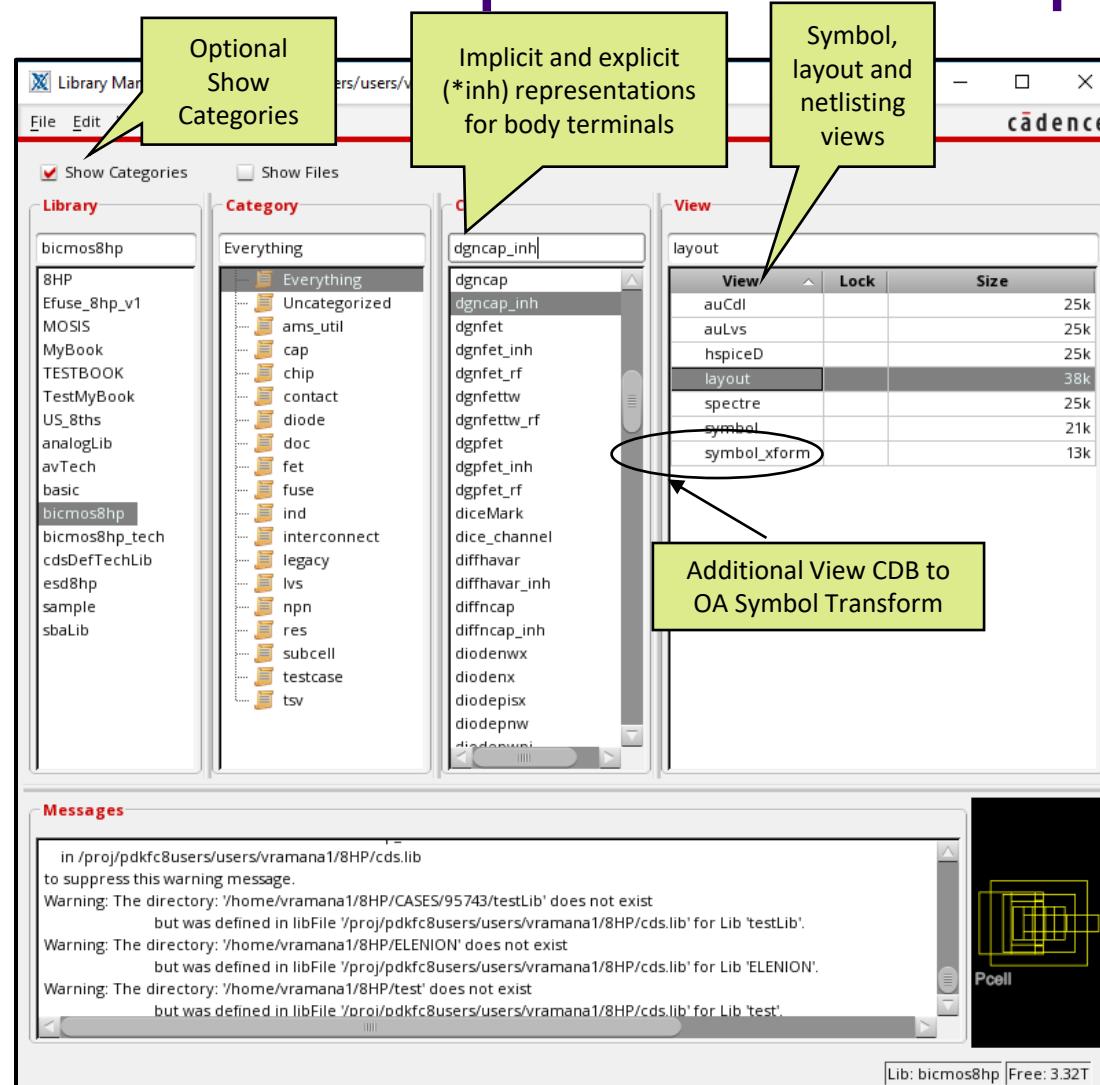
1. From CIW Window, PDK → Library → Create
2. Enter Library Name (MyBook - illustrated) and Select Technology File (Attach to an Existing Tech - illustrated) and click OK
3. Select bicmos8hp and click OK
4. Click on Add Library Properties form and click OK
5. “MyBook” is added to the Library Manager

See /DesignEnv/VirtuosoOA/doc/bicmos8hp.cdslib.rel\_notes.pdf for detail

# Wire Options and Required Techfiles

- **Wire Option 211 (AM last metal)**
  - 5 Levels of Metal (LoM) : M1-M2-MQ-LY-AM
  - `techfile211.tf` Techfile (**Default**)
- **Wire Option 311 (AM last metal)**
  - 6 Levels of Metal (LoM) : M1-M2-M3-MQ-LY-AM
  - `techfile311.tf` Techfile
- **Wire Option 411 (AM last metal)**
  - 7 Levels of Metal (LoM) : M1-M2-M3-M4-MQ-LY-AM
  - `techfile411.tf` Techfile
- **Wire Option 213 (MA last metal)**
  - 6 Levels of Metal (LoM) : M1-M2-MQ-LY-E1-MA
  - `techfile213.tf` Techfile
- **Wire Option 313 (MA last metal)**
  - 7 Levels of Metal (LoM) : M1-M2-M3-MQ-LY-E1-MA
  - `techfile411.tf` Techfile
- **Wire Option 313 (MA last metal)**
  - 8 Levels of Metal (LoM) : M1-M2-M3-M4-MQ-LY-E1-MA
  - `techfile411.tf` Techfile
- **Techfiles are located in the `cdslib/bicmos8hp` directory**

# bicmos8hp and esd8hp Device Libraries



NOTE: Explicit symbols end in "inh"

Implicit symbol use netSet property for missing terminal

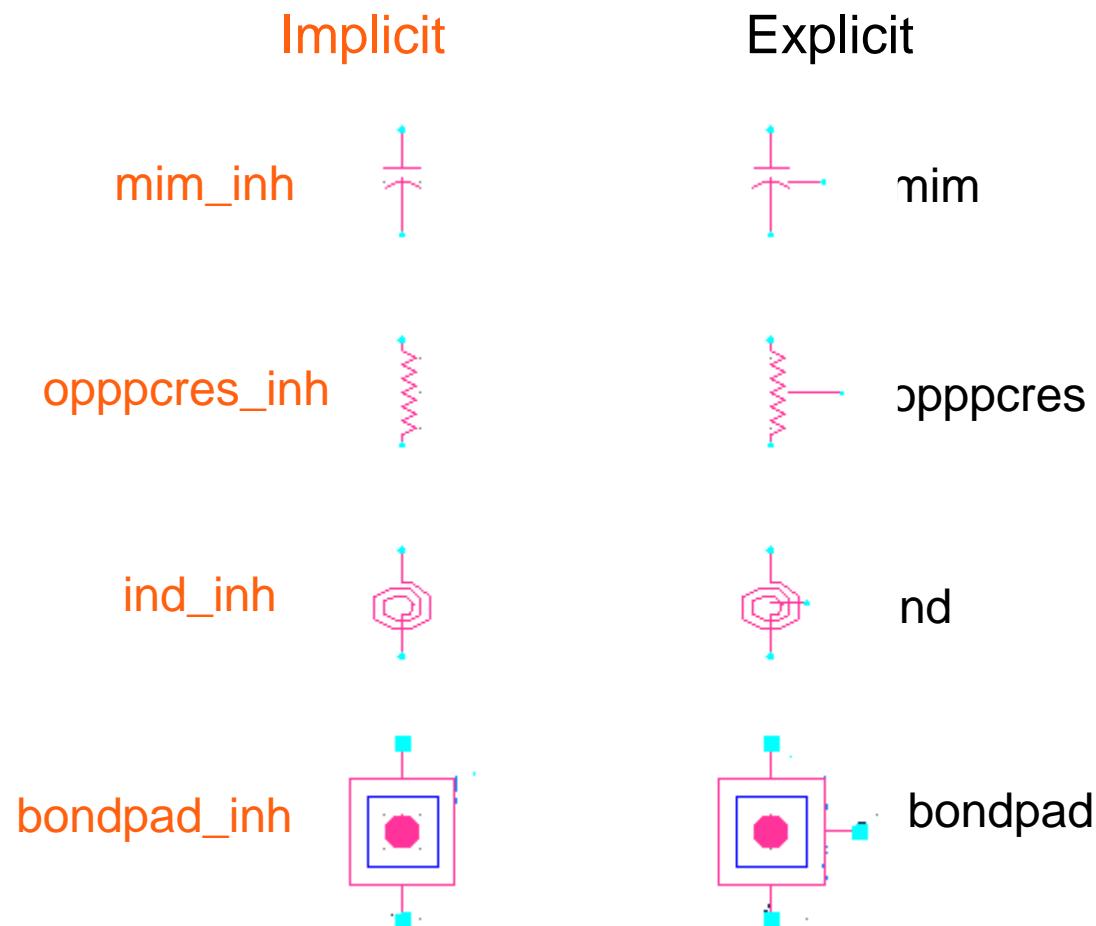
ESD devices may be instantiated directly. NO ESD Utility required.

# Implicit and Explicit Representations

PDK supports both implicit and explicit device representations

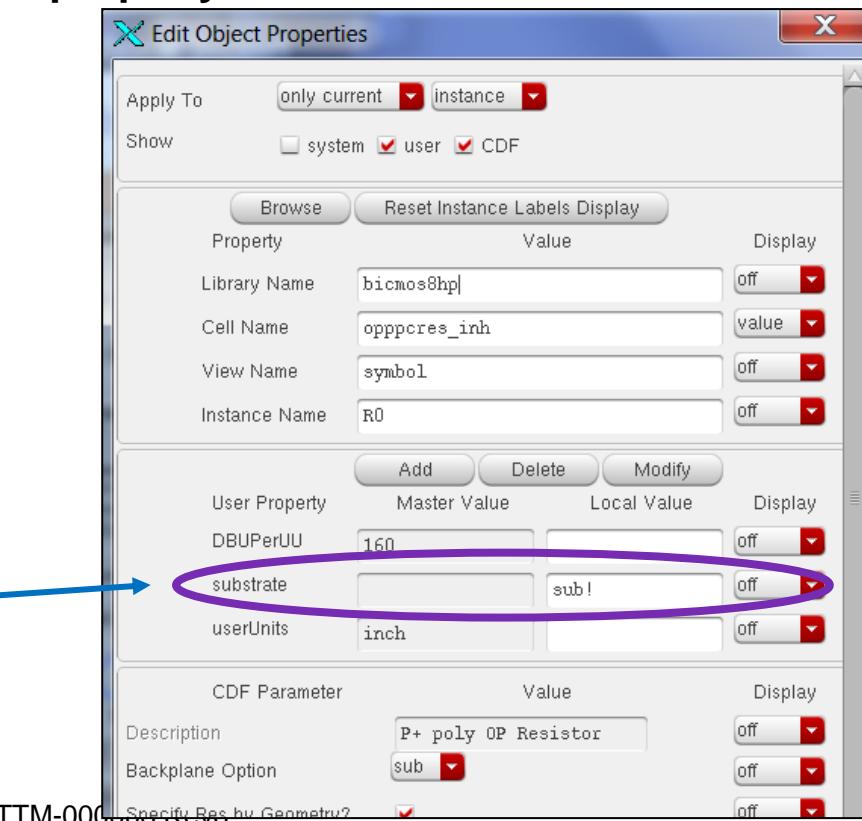
- **Implicit -- Substrate or backplate connections not shown in schematic**
  - Default value defined based on the device (inherited node)
    - sub! for substrate
  - Simplifies schematic appearance
  - Cell name ends in \_inh
- **Explicit -- All device terminals wire in schematic**
  - Most complete schematic representation
  - Explicit representation most transferable to all tools

# Implicit and Explicit Examples



# Implicit Terminal Connections

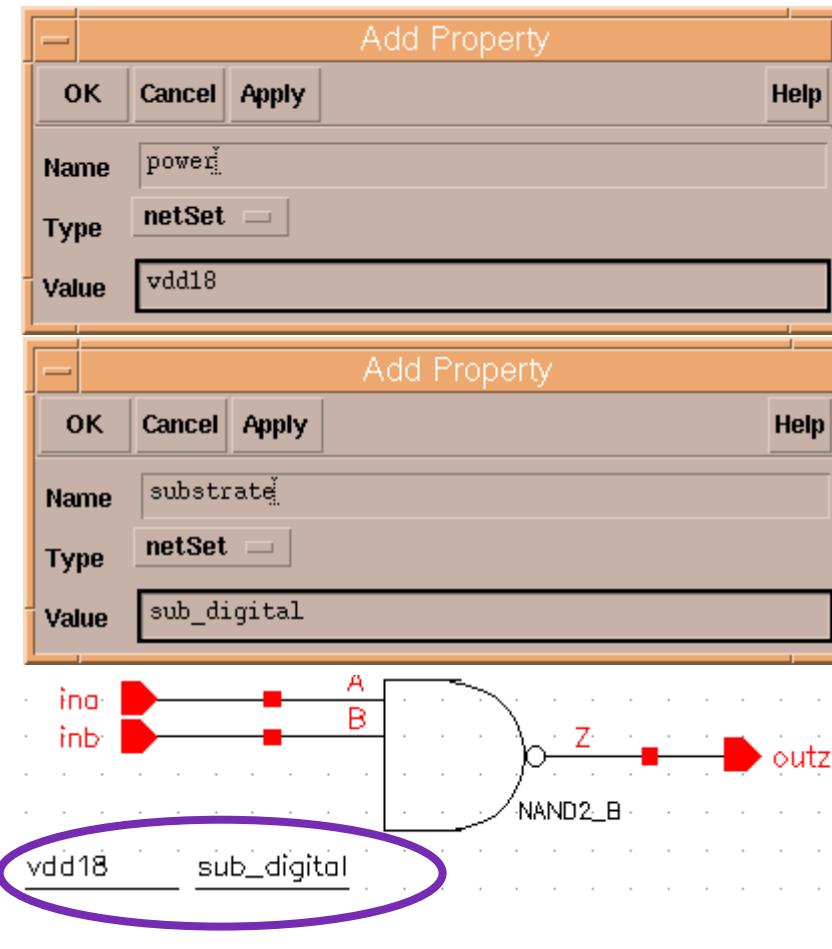
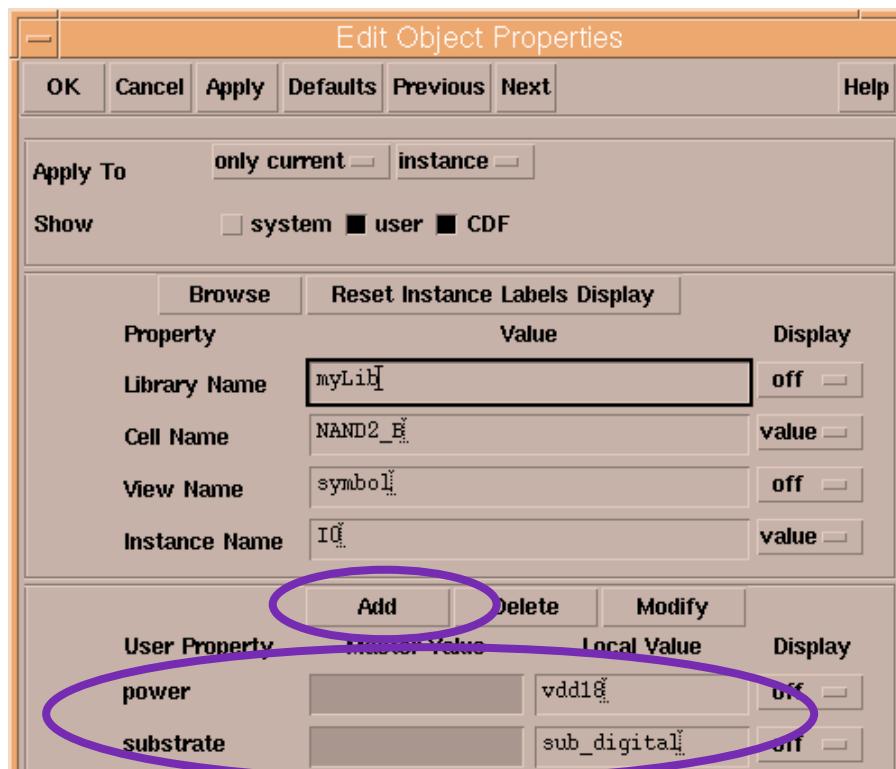
- “Inherited Connections” by added netSet property
  - Net expression associated with library element defines default
  - Designer adds netSet property at device level or higher level to modify
  - Propagates down through instance hierarchy, used for Spectre and CDL netlisting
- PDK Skill utility available in schematic to add/delete netSet property in CDF \*
  - PDK -> Misc -> Manage netSet Properties
  - Default or modified netSet property value shown in CDF



\* User also can manually add a netSet property directly in CDF

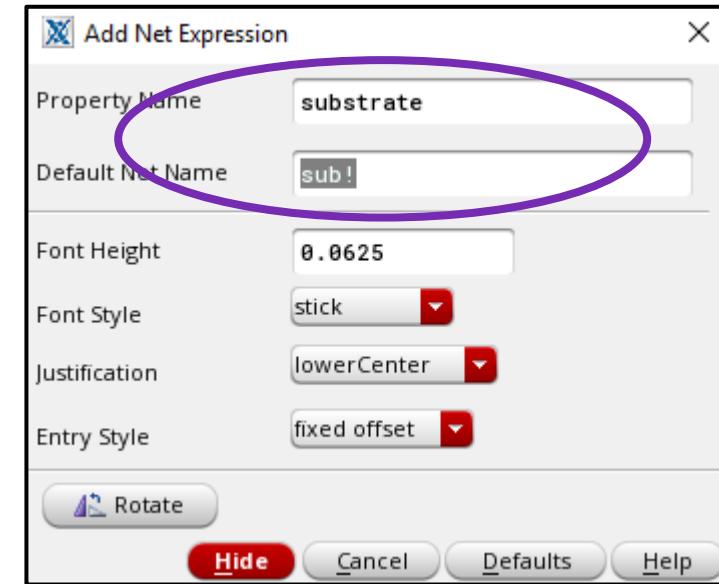
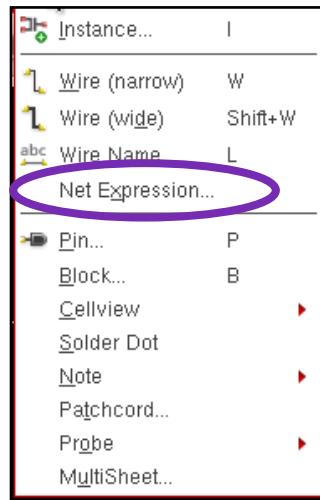
# Using netSet Properties through Hierarchy

- netSet properties apply through hierarchy allows for same cell re-use in multiple power domains



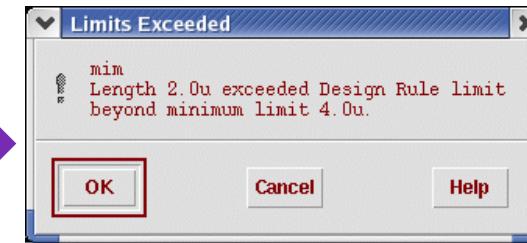
# Using netSet Properties – Named Wire

- Cadence supports netSet properties on named wires
  - Create → Wire Name → Net Expression
  - Allows use of explicit symbols with named wires and inherited connections
- Explicit symbols recommended for full compatibility with all netlisting views



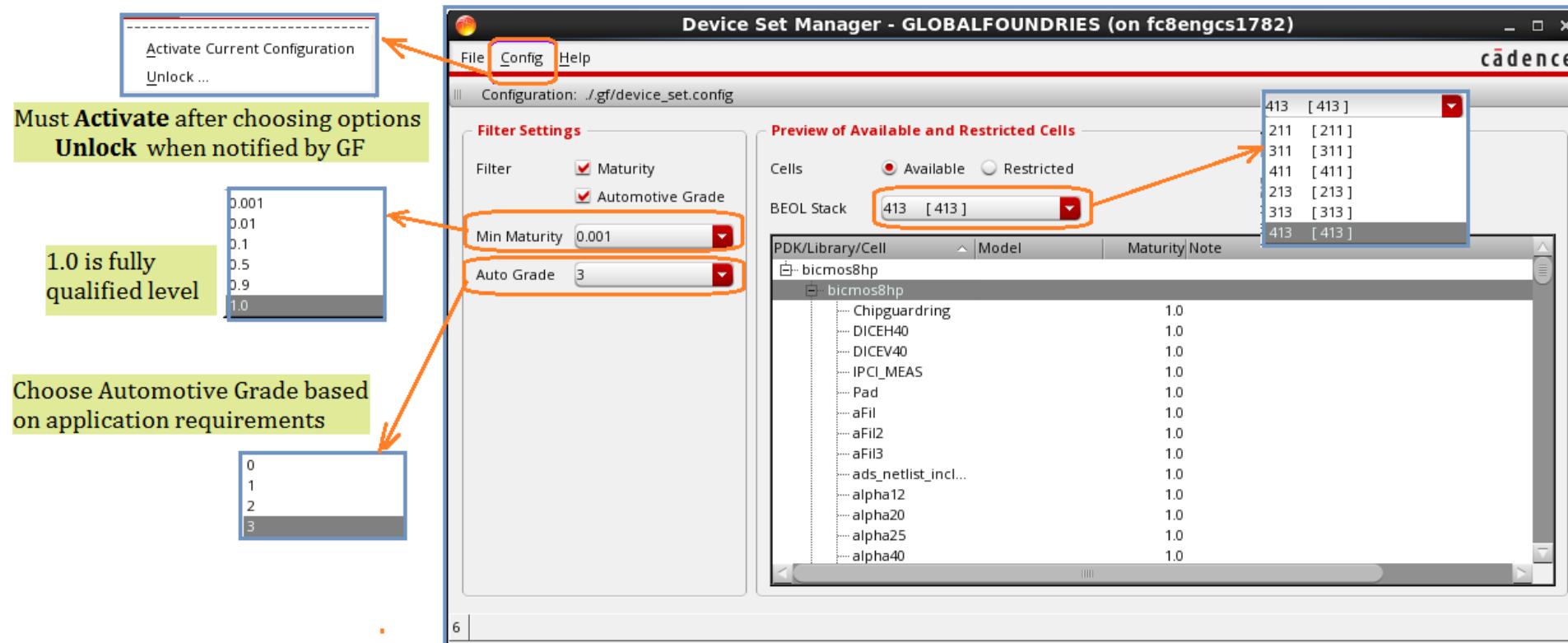
# Component Description Format (CDF)

- Individual Component Parameters defined in the CDF
  - Model, informational and layout pcell parameters
- CDF Callbacks defined in attached library SKILL file
  - Callbacks calculate various parameters from the user inputs
- Design variables supported for simulation
  - Sweep width, length for resistors, capacitors, fets, npns
- Range Checking also provided in CDF 
- “Pdk Parameter Check/Update” checks the current design CDF parameters and update
  - From schematic/layout window: PDK → Misc → Update CDF Parameters
  - From the CIW window, PDK → Library CDF Parameter Check



# Device Set Manager

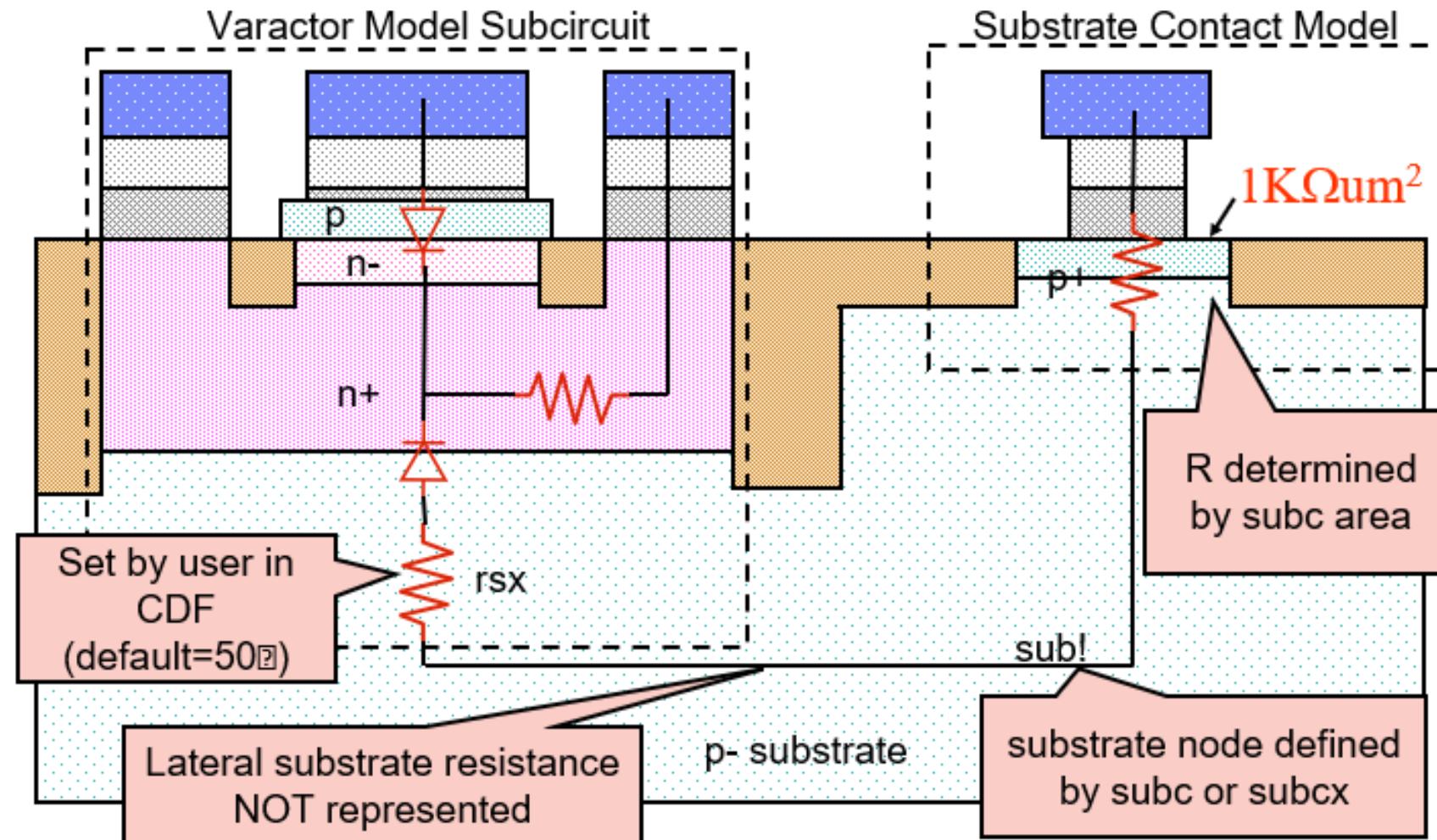
- PDK feature to customize the device set that should be used for a design based on maturity
- From the CIW window: PDK--> Device Set Manager



# Substrate Methodology

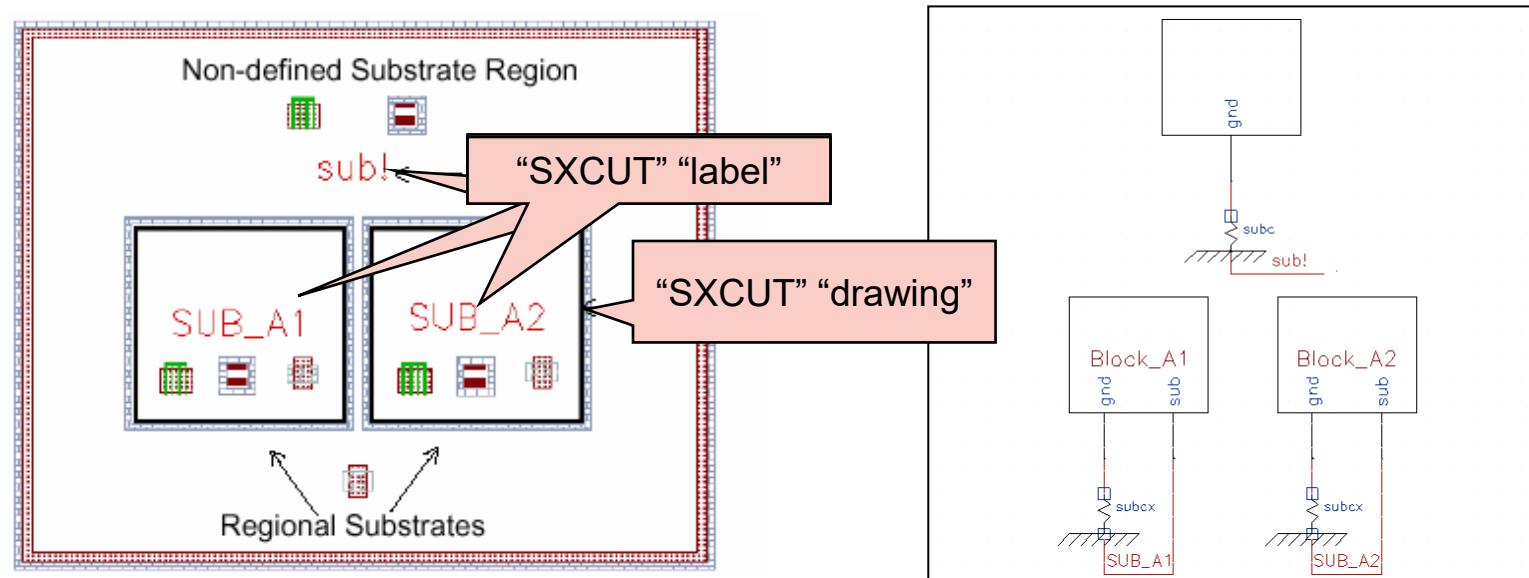
- **P- substrate (11-16 Ohm-cm)**
- **User controlled substrate resistance ( $R_{sx}$ ) in series with bulk node**
  - $R_{sx}$  included in model subcircuit for most devices
- **Substrate Connection from the metal to substrate region**
  - Modeled with a resistive device subc
  - Resistance determined by area of substrate contact
  - Device subc provides an explicit substrate node
  - Usually add a wire and add a wire name
- **Metal connection to subc may be to a global (ie, *gnd!*) or a local net**
- **Multiple substrate region network available for simulation and LVS**

# Substrate Network Illustration



# Regional Substrate Methodology

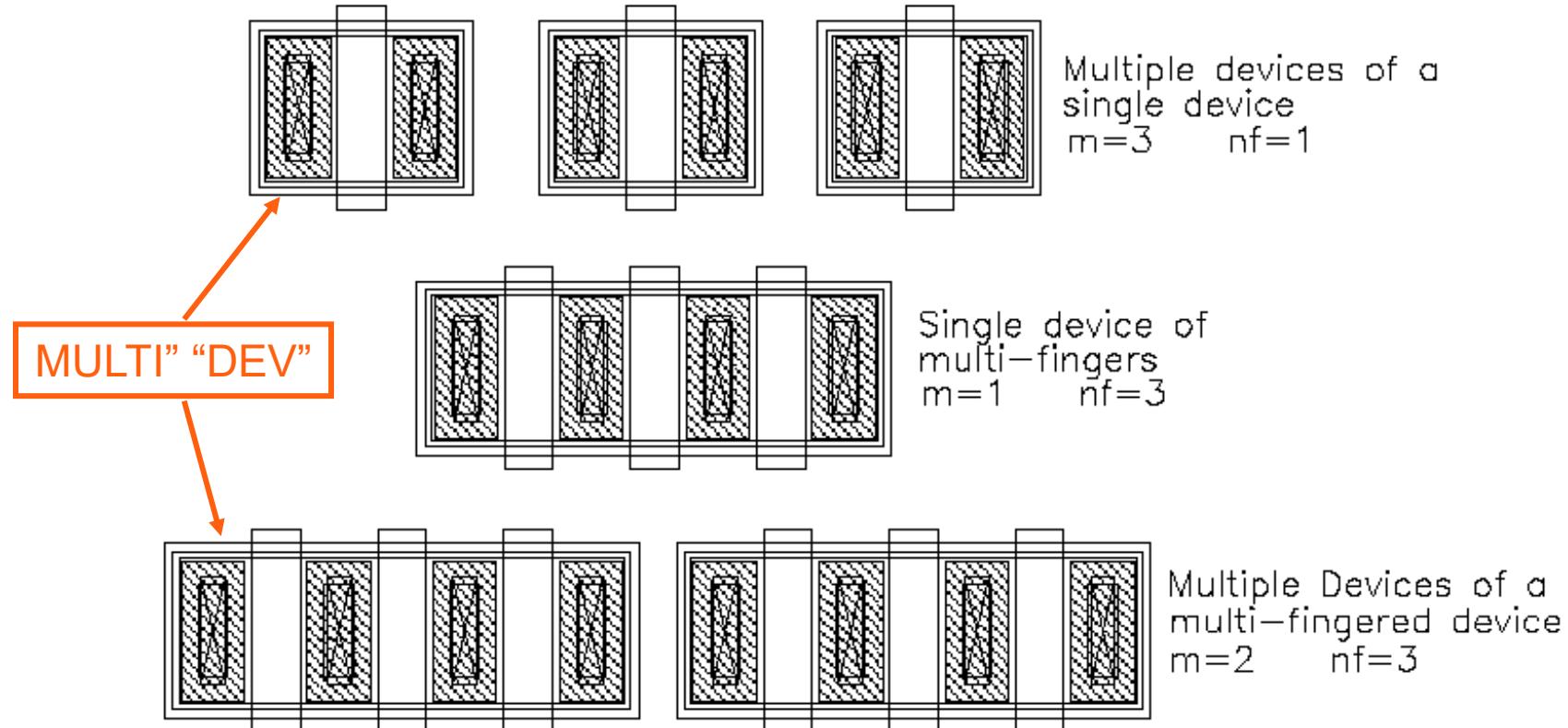
- Useful for creating substrate network for simulation and/or enforcing regional placement of devices in LVS
- Substrate regions defined by “SXCUT” “drawing”
  - Not associated with any mask layer
  - Isolates substrate regions for simulation and LVS only
- Label substrate regions with “SXCUT” “label”



# Multiplicity

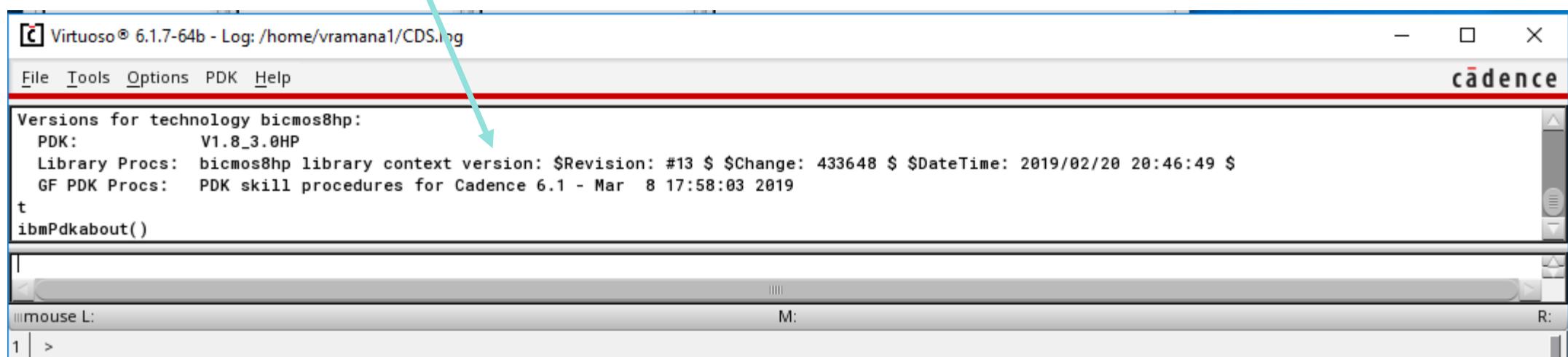
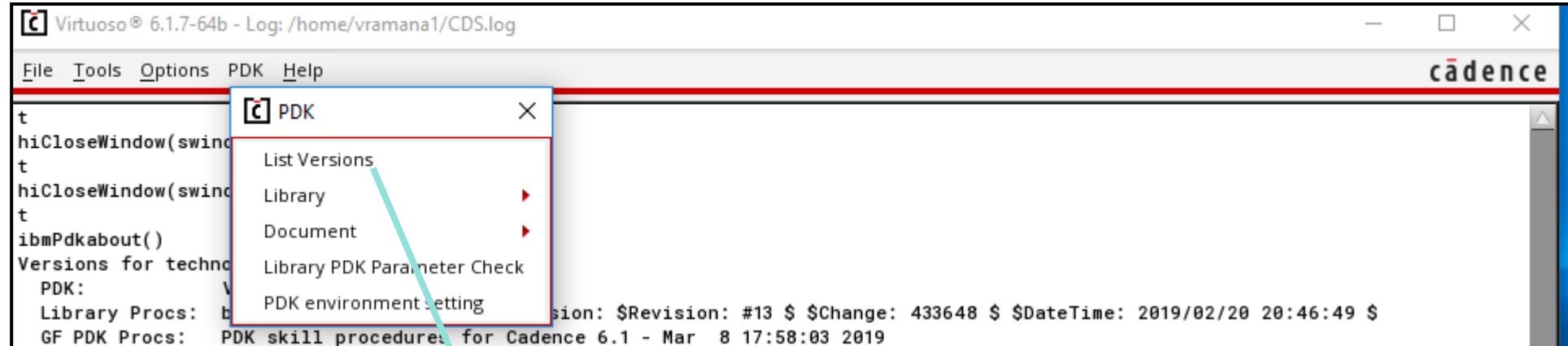
- Allows a group of identical devices wired in parallel to be represented by a single symbol in the schematic view
  - Improved clarity of schematic diagrams
  - Faster simulation time: single model call for multiple devices
- Rules and Considerations:
  - Devices must be identical, with identical node connections
  - Number of devices in parallel defined by parameter “m”
  - Device mismatch applied identically in Monte Carlo schematic simulation
    - Conservative representation of mismatch between sets of devices
    - For more realistic mismatch, use devices in parallel instead of multiplicity
- Virtuoso Layout Editor
  - For  $m > 1$ , pcell places recognition shape on layer “MULTI” “DEV” to indicate device is part of a multiple set
  - Layout pcells create a single device (not  $m$  devices)
    - Designer places  $m$  devices to correspond to schematic
- Virtuoso XL (schematic driven layout)
  - Creates  $m$  devices without wiring, w/ “MULTI” “DEV” shape
  - Layout CDF shows  $m=1$  (CDF parameter mSwitch retains actual value)
- Supported Devices
  - Resistors support parallel/series options or multiplicity, but not both
  - Diode devices support multiple stripes & devices
  - MOSFETs support multiple gate fingers & devices
  - Capacitors

# Multiplicity and Multi-finger FETs



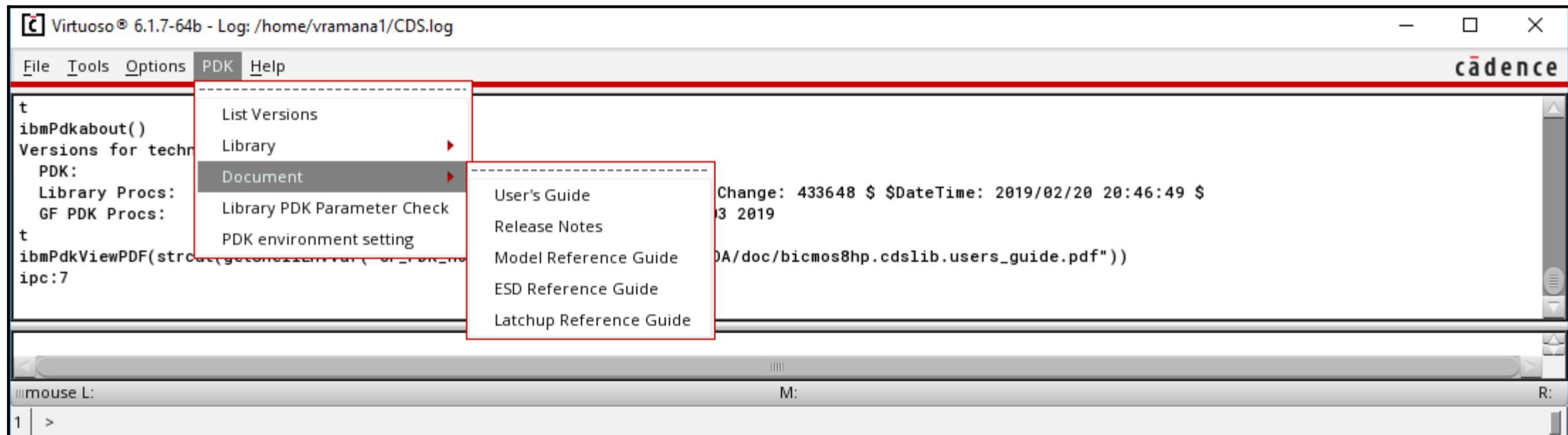
# CIW Utilities: PDK → List Versions

- Displays date and revision control of loaded cdslib elements
- May be requested for debug purposes of user's setup



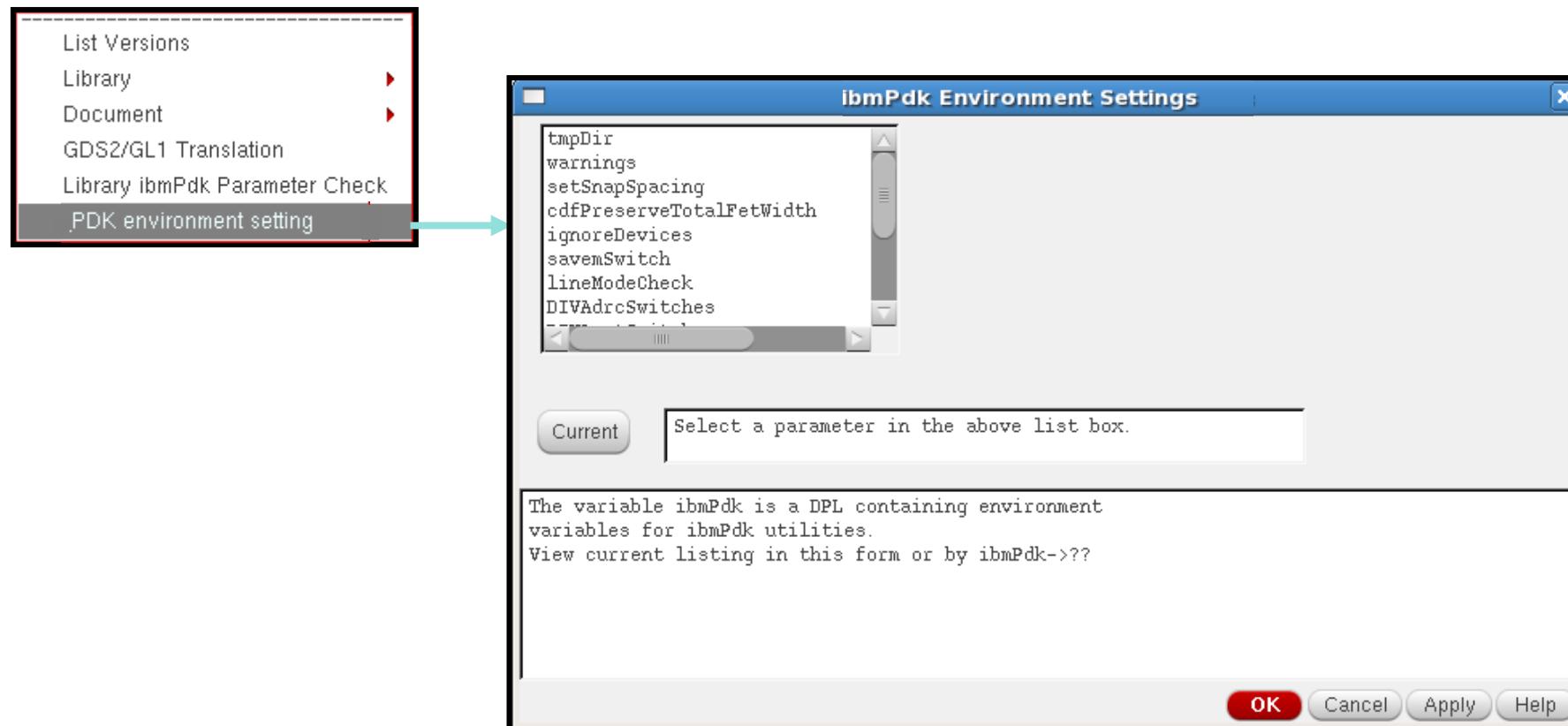
# CIW Utilities: PDK → Documentation

- Useful for accessing CDS design kit documentation within Cadence



# CIW Utilities: PDK → PDK environment setting

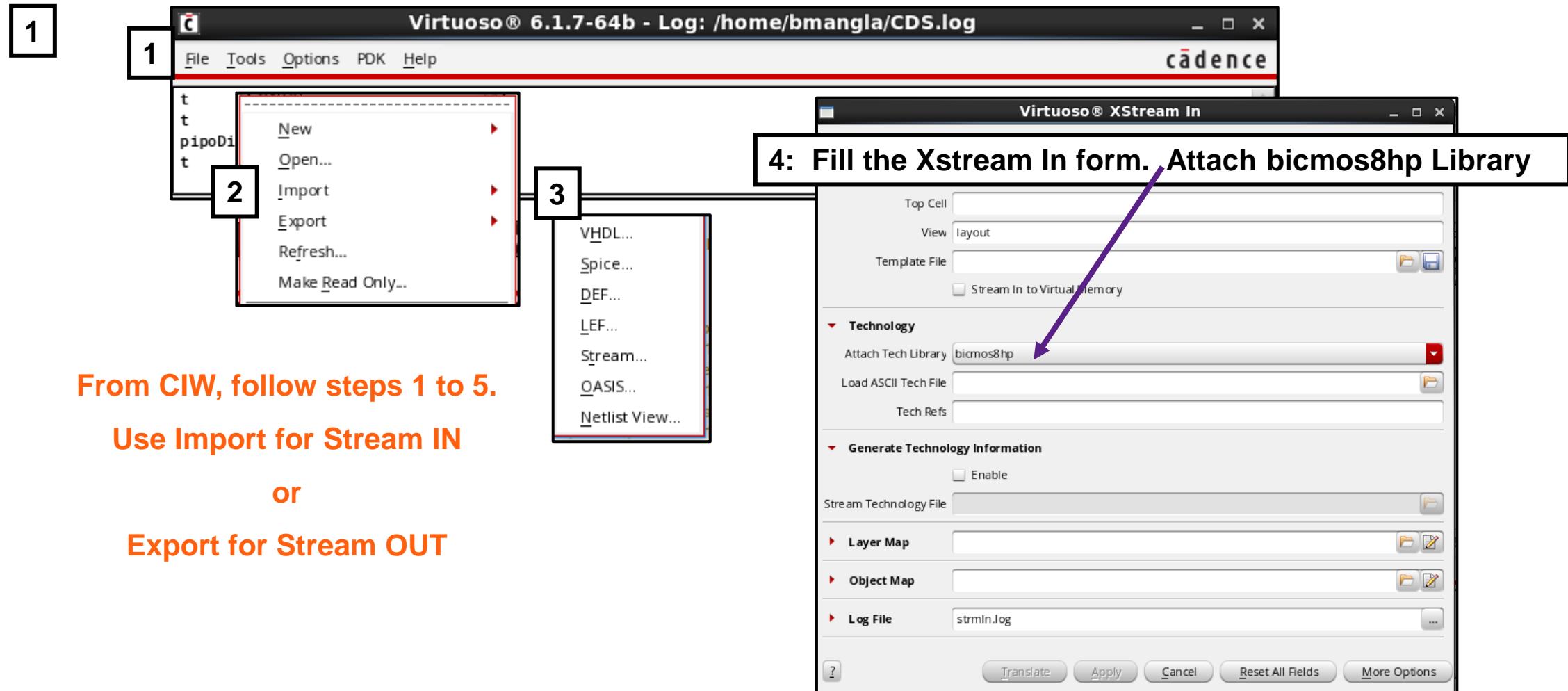
- Options that over-ride default settings for CDF and switch settings
- Set through ciw PDK → PDK environment settings or in .cdsinit



# CIW Utilities: Steam-in or Stream-out

## Procedure (1)

From CIW select **File → Import (Export) → Stream**



# CIW Utilities: Steam-in or Stream-out Procedure (2)

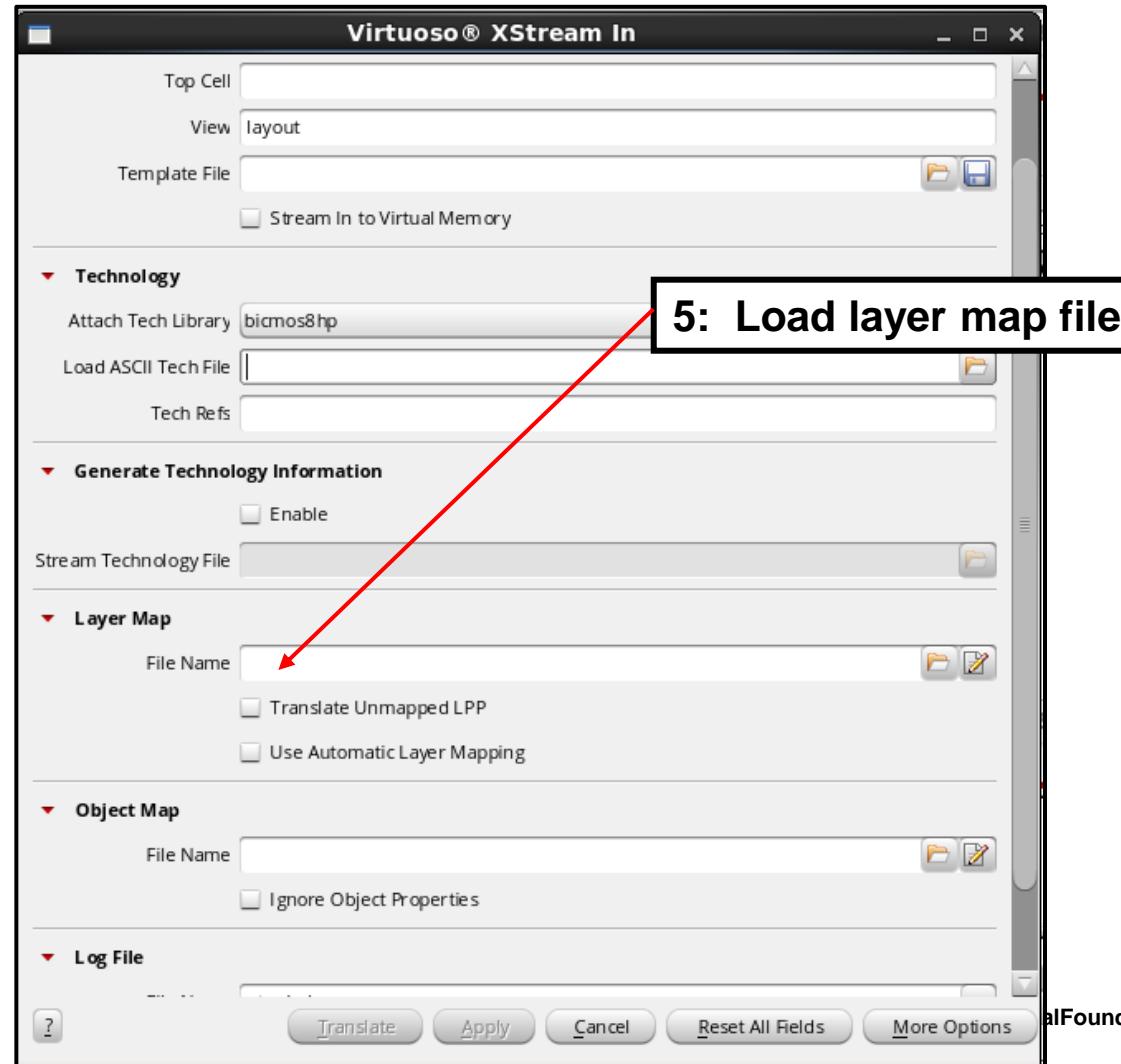
From CIW select **File → Import (Export) → Stream**

From CIW, follow steps 1 to 5.

Use Import for Stream IN

or

Export for Stream OUT



# Design Kit Version Migration

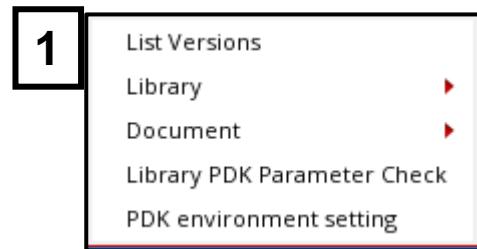
- Updated design kits released periodically

- Patch releases – non-zero last numeric digit, e.g. V1.8\_5.5
    - Only affected kit components provided
    - Cumulative – V1.8\_5.5 will contain fixes from V1.8\_5.3 and V1.8\_5.4 as well
  - Full kit releases – zero last numeric digit, e.g. V1.8\_5.0
    - Complete design kit installation
    - When migrating to a new design kit release:
      - Back up design libraries
      - Review Release Notes or README
      - Update “GF\_PDK\_HOME” to new path prior to CDS start up
      - Recompile techfile, merge display.drf if required
      - Run **Library PDK Parameter Check** on design libraries (See Next chart)
      - Further information in cdslib Release Notes and User’s Guide

# CIW Utilities: PDK → Library Pdk Parameter Check (1)

- Executes CDF callbacks to ensure consistency in calculated parameters
- Recommended periodically during design cycle
- Required when updating to new design kit version

From CIW, perform steps 1- 5

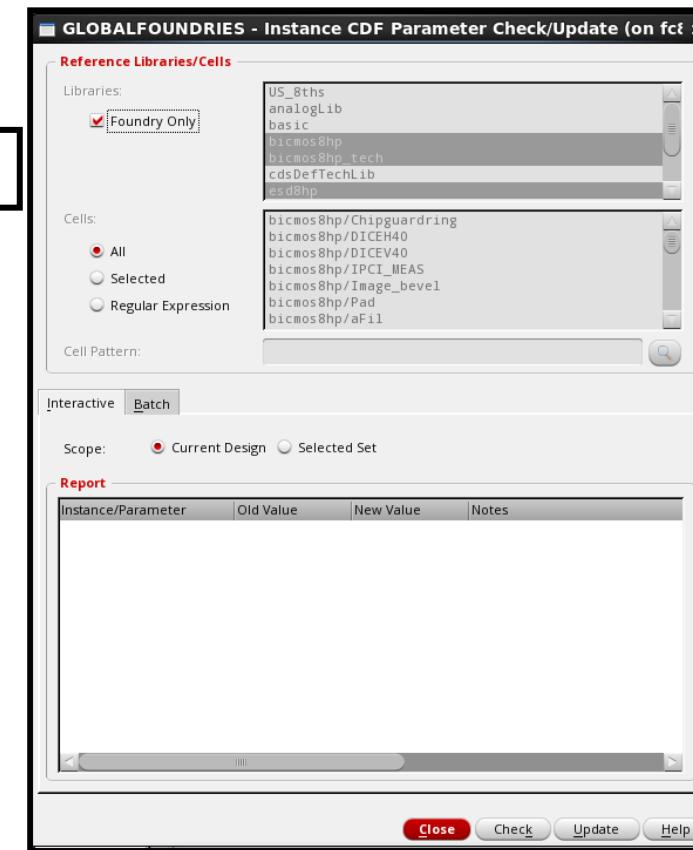


1. From CIW, select PDK → Library Pdk Parameter Check. GLOBALFOUNDRIES - Instance CDF Parameter Check/Update form will open.

2. Select options. Then click:-

Check to see a list of updates

Update to accept the CDF Parameter updates to your library



# Documentation Available in \$GF\_PDK\_HOME

Documentation available in \$GF\_HOME\_PDK/<version(V1.8\_5.5)>/doc folder

- Design Manual
- Model Reference Guide
- ESD Reference Guide
- Latch\_Up Reference Guide
- PDK Release Notes
- Model Release Notes (Spectre, ADS, GoldenGate, PeakView)
- EM Release Notes
- EM Guide
- Design Environment (VirtuosoOA and ADS)
  - cdslib Release Notes, cdslib\_users\_guide
  - adslib\_users\_guide (ADS)
- DRC Release Notes (Calibre and PVS)
- LVS Release Notes (Calibre and PVS)
- P&R ICC (Synopsis)
  - MW (Milkyway) Release Notes
  - Synopsis RC Extract Release Notes
- P&R Innovus (Cadence)
  - LEF Release Notes
  - Cadence RC Extract Release Notes

## Example Release Notes

/DRC/Calibre/doc/bicmos8hp.CalibreDRC.rel\_notes.pdf  
/DRC/PVS/doc/bicmos8hp.PVSDRC.rel\_notes.pdf  
/LVS/Calibre/doc/bicmos8hp.CalibreLVS.rel\_notes.pdf  
/LVS/PVS/doc/bicmos8hp.PVSLVS.rel\_notes.pdf

# Technical Support

- Application Notes and Training Material
  - Available on [www.Global-FoundryView.com](http://www.Global-FoundryView.com)
- Technical Support
  - [www.Global-FoundryView.com](http://www.Global-FoundryView.com) → Open a new Case (or manage existing Cases)
  - or email: [fdrytech@globalfoundries.com](mailto:fdrytech@globalfoundries.com)
  - Please always provide complete information
  - Technology, metal stack, design kit version, tool (Virtuoso, Calibre, etc.,) subversions, log files, test case ....



# **Automotive PDK Notes**

# 8HP/8XP Automotive Offering

- In addition to the standard foundry offering, an enhanced AutoPro flow has been defined to offer support for Automotive applications (Part no.: 01XL074) with the following exceptions to the commercial design flow:
- AUTO:dg marking layer coincident with CHIPEDGE:dg is required.
- 100um Through Silicon Via (70Y8337) and Vertical PNP (84Y6775) features are prohibited for automotive designs.
- Enhanced crackstop methodology (84Y7710) is required. Using the GF pcell (Chipguardring) will give you the enhanced crackstop.
- Checking additional automotive ground rules, designated by a "A\_" prefix in the rule name. These rules increase the severity class to allow for stricter enforcement. More details on severity classes on the next page.
- Wafer edge exclusion zone will be set at 5mm. (3mm is the standard wafer exclusion zone for 8HP commercial foundry flow. 8XP is always set at 5mm).
- The technology is being qualified to the AEC-Q100 Automotive Temperature Grade 1 standard. Once qualification is completed, it can be used for Automotive Temperature Grade 1-3 products. Automotive Temperature Grade 1 junction temperature range is -40C to +150C for 15 years at 10% power on. Contact your GLOBALFOUNDRIES Field Application Engineer for qualification status.
- The technology has not completed package evaluation to Automotive standard AEC-Q100 Temperature Grade 1 stress conditions. Contact your GLOBALFOUNDRIES Field Application Engineer for packaging option status.

# 8HP/8XP Automotive Offering and Severity Class Rule Definition

- No waivers will be granted for severity class a and severity class b rule violations for automotive designs
  - Severity class b rules will appear as class a after running through the parser.
- Severity class c rules should also be followed, and any violations are at the risk of the customer
  - Added A\_ automotive rules promote severity class c to a or b for specific rules that have a reliability risk
  - See discussion of ESD rules on the following pages
- Severity class d rules should be followed wherever space is available

## Class a rules: Manufacturing Impact

- All violations will require waiver approval for any design, test site or product.
- These rules ensure that the design is compatible with the manufacturing process and does not impact production tools & processes, mask build, process control monitors, kerf electrical test monitors, or other riders on a MPW
- Failure to follow these rules may result in rejection of the waiver request

## Class b rules: Yield & Reliability impact

- Violations will require waiver approval for all product designs unless the product deliverable is foundry grade Wafer Acceptance Criteria (WAC) only or a test site design.
- These rules are required to meet product yield, reliability, and device performance
- Automatic reject for Automotive Grade 1

## Class c rules: Modelling and circuit limited yield impact.

- Violations will require waiver approval for all product designs unless the product deliverable is Wafer Acceptance Criteria (WAC) only or a Test Site.
- These rules are required to ensure accuracy of the device models
- Violation of class c rules may impact circuit limited yield and RF performance.

## Class d rules: Improve manufacturability & performance stability

- Violations do not require waiver.
- Suggested ground rules and recommended rules to improve manufacturability

Class a, b violations lead to automatic reject for automotive

See next page for important information on ESD rules in these classes

# 8HP/8XP ESD for Automotive

- The ESD design rules in the table in section 3.13.3 of the design manual are designed to ensure that discrete protection devices meet 1kV Human Body Model (HBM) and 250 V (4A) Charged Device Model (CDM) requirements. These are class c rules.
- In order to meet automotive standards requirement of 2kV HBM and 750V (12A) CDM (for corner pins), recommended rules \*R (class d) must also be met.
- Please see ESD Reference Guide for relation between CDM voltage value, CDM peak current value and package size.
- Contact your GLOBALFOUNDRIES Field Application Engineer for more details on ESD protection.

# 8HP/8XP Device Model Updates

- Please review the Model Reference Guide for an expanded set of model-to-hardware correlation plots that illustrate many of the device characteristics up to junction temperature 150C.
- Model updates have been made for the following devices based on the full -40C to +150C junction temperature range data. See the release notes for details.
  - PIN / SBD Diodes
  - HA Varactors (havar and diffhavar)
  - Forward Bias (DI) Diode (divpnp)
  - Parasitic Junction Diodes
  - KQ BEOL Resistor
  - NS Resistor
  - Single MIM Capacitor
  - Dual MIM Capacitor



# **ADS Interoperable PDK (Schematic/Layout Design Kit)**

# 8HP/XP Interoperable ADS Design Kit

## ▪ADS Supported Version

- ADS 2020 update 1.0

## ▪ADS Schematic/Layout Design Kit

- Operates on the same Open Access database as Cadence

- Edits saved in ADS are reflected in CDS and vice versa

- Linux required for layout

- ADS runs Cadence pcell evaluation in the background
  - ADS Components

- PDK Components provided divided into 2 palette groups:

- bicmos8hp and esd8hp

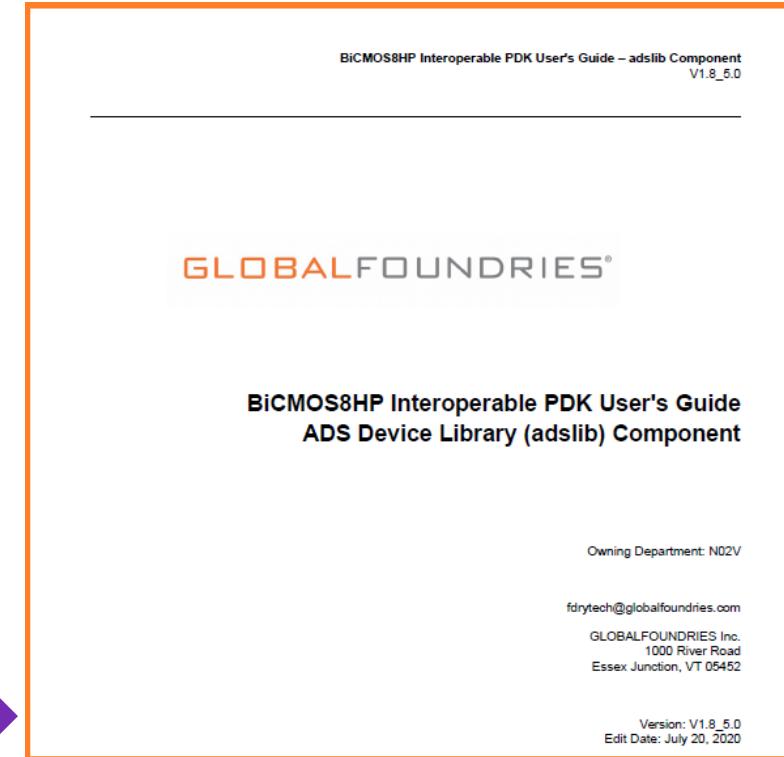
- Views for all devices

- Symbol and netlisting views
  - Parameterized layout cells (pcells)

## ▪ADS Set Up

## ▪Documentation

- BiCMOS8HP/XP Interoperable PDK User's Guide Located in  
\$GF\_PDK\_HOME/DesignEnv/ADS/doc



# BiCMOS8HP/XP ADS Design Kit

## Directory Structure

/130HPSIGE-8HP/XP/Vx.x\_x.x/DesignEnv/ADS/

- bicmos8hp/ main library
- esd8hp/ ESD components
- Bicmos8hp\_tech\_<stack>/ technology files
- ael/ general Application Extension Language functions
- lisp/ required LISP functions
- records/ equivalent of CDS categories
- artwork/ pcell functions
- bitmaps/ palette icons
- doc/ bicmos8hp.adslib.users\_guide.pdf
- lib.defs Library Definitions

# ADS Setup: Follow Steps 1 to 5

## 1. Ensure environmental variables are set

\$HPEESOF\_DIR/bin is added to the PATH variable,

LD\_LIBRARY\_PATH variable is defined,

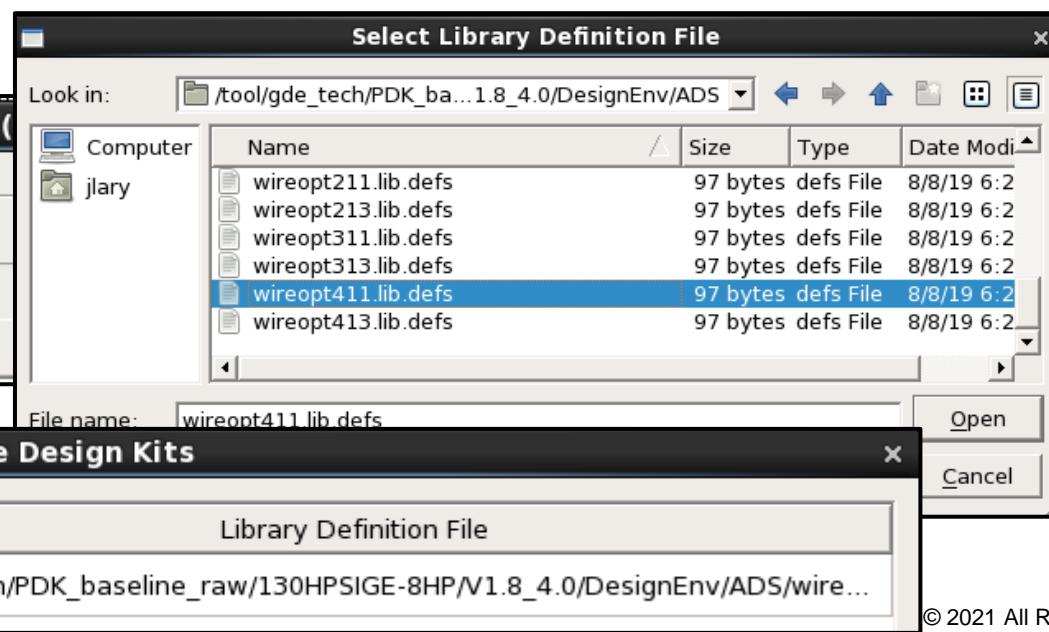
and that the ADS license location is defined.

For layout interoperability, virtuoso must also be in the PATH and CDS license defined  
(ADS runs Cadence in the background for layout)

## 2. From ADS Main Window, DesignKits → Manage Favorite Design Kits

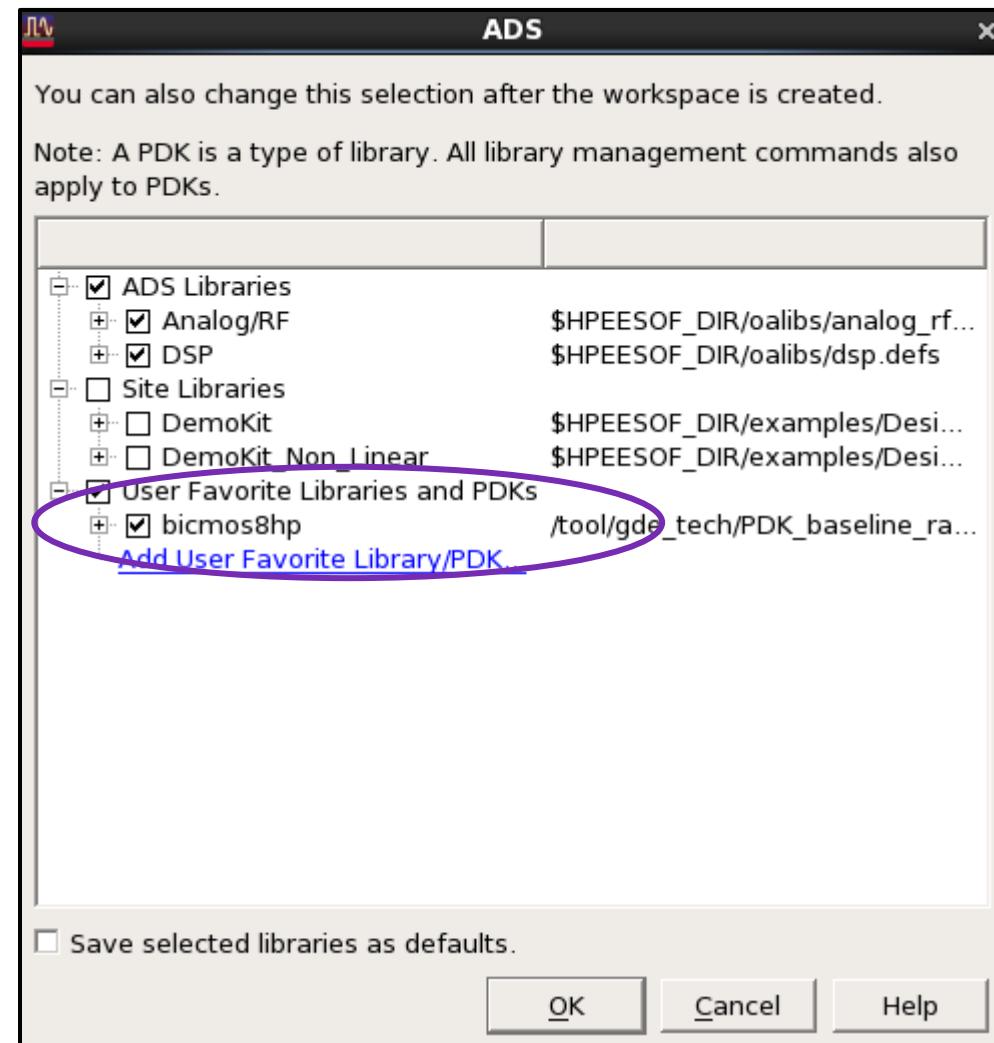
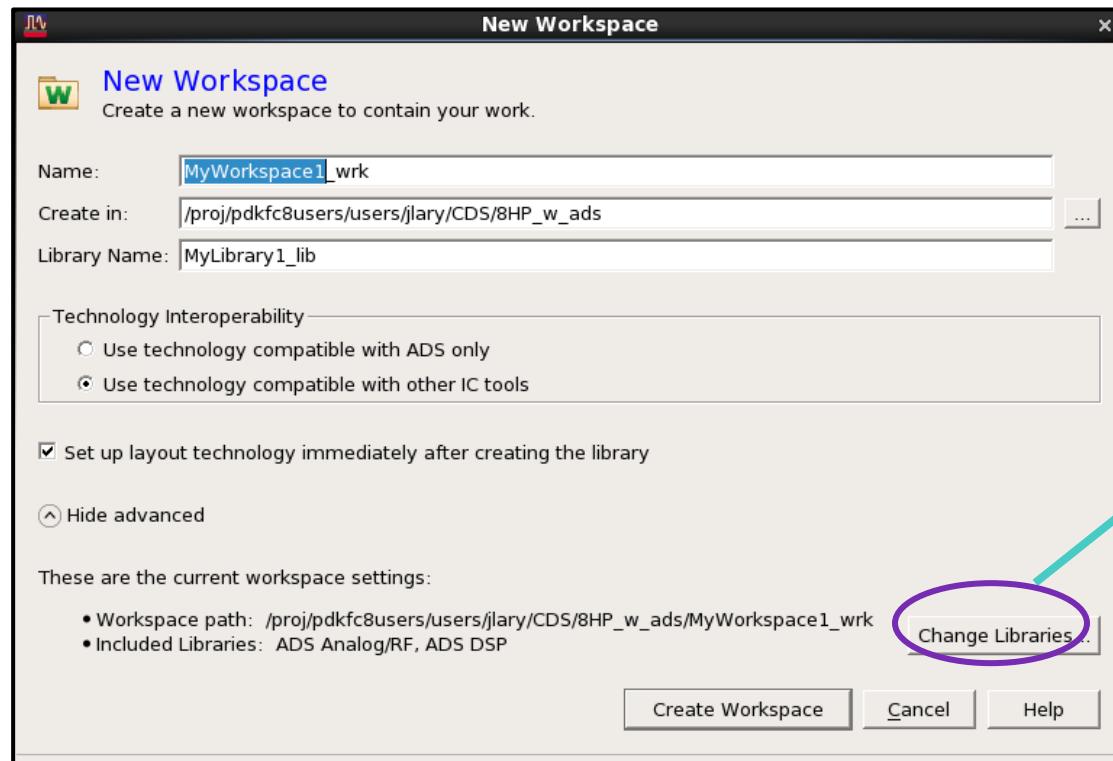
Navigate to the PDK installation directory /DesignEnv/ADS

and select the lib.defs for your stack



# ADS Setup

## 3. From ADS Main window, File → New Workspace



# ADS Setup

4. ADS will have created a directory for the workspace with necessary configuration files and a lib.defs file. User may add other existing library definitions through  
File → Manage Libraries → Add Library Definition File  
This additional library definition file can be loaded both in CDS and ADS

The screenshot shows two windows side-by-side. On the left is a code editor window titled 'lib.defs = (/proj/pdkfc8users/users/jlary/CDS/8HP\_w\_ads/MyWorkspace1\_'. It contains the following text:

```
INCLUDE $HPEESOF_DIR/oalibs/analog_rf.defs
INCLUDE $HPEESOF_DIR/oalibs/dsp.defs
INCLUDE /tool/gde_tech/PDK_baseline_raw/130HPSIGE-8HP/V1.8_4.0/DesignEnv/ADS/wireopt411.lib.defs
DEFINE MyLibrary1_lib MyLibrary1_lib
ASSIGN MyLibrary1_lib libMode shared
```

On the right is a 'Manage Libraries' dialog box. At the top, it says 'Libraries and library definition files used by this workspace.' Below is a table:

Name	Path
lib.defs	/proj/pdkfc8users/users/jlary/CDS/8HP_w_ads/MyWorkspace1_wrk/lib.defs
+ analog_rf.defs	\$HPEESOF_DIR/oalibs/analog_rf.defs
+ dsp.defs	\$HPEESOF_DIR/oalibs/dsp.defs
+ wireopt411.lib.defs	/tool/gde_tech/PDK_baseline_raw/130HPSIGE-8HP/V1.8_4.0/DesignEnv/ADS/wireopt411.lib.defs
MyLibrary1_lib	MyLibrary1_lib

At the bottom of the dialog box, there is a toolbar with several buttons: 'Add Library Definition File...', 'Add Design Kit from Favorites...', 'Add Library...', 'Configure Library...', 'Remove', 'Close', and 'Help'. The 'Add Library Definition File...' button is highlighted with a purple oval.

5. copy the display.drf from the PDK install directory to the workspace directory  
cp <installdir>/DesignEnv/VirtuosoOA/setup/display.drf

# Example kshell start-up script

```
export GF_PDK_HOME="/tool/gde_tech/PDK_baseline_raw/130HPSIGE-8HP/V1.8_5.5"
module load cadenceAssura/4.15.114_OA617
module load cadenceEXT/16.11.012
module load cadenceICOA/06.17.706
module load mentorCalibre/2018.4_34.26
module load cadenceSPECTRE/17.10.389
export CDS_Netlisting_Mode="Analog"
module load keysightADS/2020.1.0
export HPEESOF_DIR="/tool/eda/apps/keysightADS/2020.1.0"
export IDF_CDS_VERSION="4.4.6"
. $HPEESOF_DIR/bin/setCSF.ksh
ads
virtuoso &
```



# **Design Verification (DRC/LVS) and PEX Flows**

# Supported Verification and PEX Flows

Tool	Install Path
Cadence PVS DRC	\$GF_PDK_HOME/DRC/PVS
Cadence Assura DRC *	\$GF_PDK_HOME/DRC/Assura
Mentor Calibre DRC	\$GF_PDK_HOME/DRC/Calibre
Cadence PVS LVS	\$GF_PDK_HOME/LVS/PVS
Cadence Assura LVS *	\$GF_PDK_HOME/DRC/Assura
Mentor Calibre LVS	\$GF_PDK_HOME/LVS/Calibre
Cadence ASSURA QRC *	\$GF_PDK_HOME/PEX/QRC/ AssuraQRC
Mentor Calibre xRC	\$GF_PDK_HOME/PEX/xRC
Calibre QRC	\$GF_PDK_HOME/PEX/QRC

\*Require separate subscription/provisioning for these PDK components. Please consult your FAE

# Design Rule Categorization in Design Manual

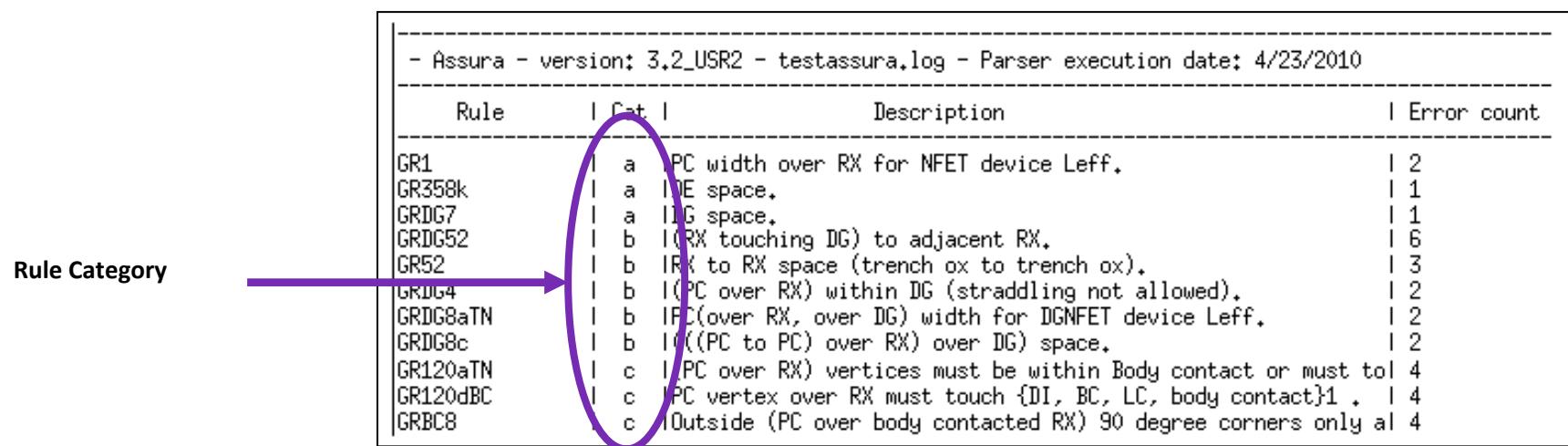
- **Class a: Manufacturing Impact– Most severe (severity1)**
  - Possible Impact to production tools or processes, GF Kerf/WAC, Mask Build, Other Riders (MPW)
  - Examples: Min Width/Space/Area, Density, Geometry
- **Class b: Yield and Reliability – Medium severity (severity 2)**
  - Examples: Overlap spacing, Wide Metal Spacing
- **Class c: Modelling and Circuit Related Yield Impact– Low severity (severity 3)**
  - Examples: Inductor rules, Antennae rules, ESD rules
- **Class d: Improve Manufacturing and Performance Stability– Lowest severity (severity 4)**
  - More conservative recommendations for line/space rules

Classification Column

Table 3-1. Polysilicon and Isolation Layout Rules (Part 1 of 7)							
Rule	C I a s s	Notes	Description		Design	Wafer	Tol
1	a	-	PC width over RX for NFET device Lp.	≥	0.12	0.092 <sup>1</sup>	0.022 <sup>1</sup>
2	a	-	PC width over RX for PFET device Lp.	≥	0.12	0.092 <sup>1</sup>	0.022 <sup>1</sup>
3	c	-	PC width over RX for 45 degree NFET device Lp.	≥	0.127	0.0990 <sup>1</sup>	0.029 <sup>1</sup>
3R	d	-	PC width over RX for 45 degree NFET device Lp.	≥	0.140	0.1120 <sup>1</sup>	0.029 <sup>1</sup>

# Parsing Script for Categorization of Design Rules

- Design rules categorized in Design Manual
  - Waivers are required for any class A violation.
- Parsing script provided in PDK
  - Perl script: drc\_results\_postprocessor.pl
    - Located in <install\_path>/<technology>/<release>/utils
    - Readme file provided for usage
  - Support parsing Assura(xxx.log) and Calibre(xxx.summary) DRC results



- Assura - version: 3.2_USR2 - testassura.log - Parser execution date: 4/23/2010				
Rule Category	Rule	Category	Description	Error count
	GR1	a	IPC width over RX for NFET device Leff.	2
	GR358k	a	IDE space.	1
	GRDG7	a	IGG space.	1
	GRDG52	b	I(RX touching DG) to adjacent RX.	6
	GR52	b	IRX to RX space (trench ox to trench ox).	3
	GRDG4	b	I(PC over RX) within DG (straddling not allowed).	2
	GRDG8aTN	b	I(PC over RX, over DG) width for DGNFET device Leff.	2
	GRDG8c	b	I((PC to PC) over RX) over DG space.	2
	GR120aTN	c	I(PC over RX) vertices must be within Body contact or must tol	4
	GR120dBC	c	I(PC vertex over RX must touch {DI, BC, LC, body contact})1 .	4
	GRBC8	c	IOutside (PC over body contacted RX) 90 degree corners only al	4

# Required Checks for Design Submission

- **Design should be DRC and LVS clean**
  - All Class “a” type DRC violations should be fixed prior to tape out
    - If errors are not fixable, contact [fdrytech@globalfoundries.com](mailto:fdrytech@globalfoundries.com) as soon as feasible
  - Customer is responsible for verifying LVS
    - GLOBALFOUNDRIES Tape Out Release Team does not run LVS verification
- **GLOBALFOUNDRIES Tape Out Release Team uses Calibre DRC deck for checking customer's BICMOS8HP(8XP) GDS for Release to Mask (RTM) House**

# Design Verification : Design Rule Checking (DRC)

- Layout design rules, described in Design Manual
- Design Geometry Restrictions
- Primary Layout Rules
  - Line, space, area checks
- Pattern Density Rules
  - Global and local rules
- Antenna Rules
- ESD Rules
- Electromigration Rules\*
  - Designer Responsibility
  - Electromigration rules not checked in DRC decks

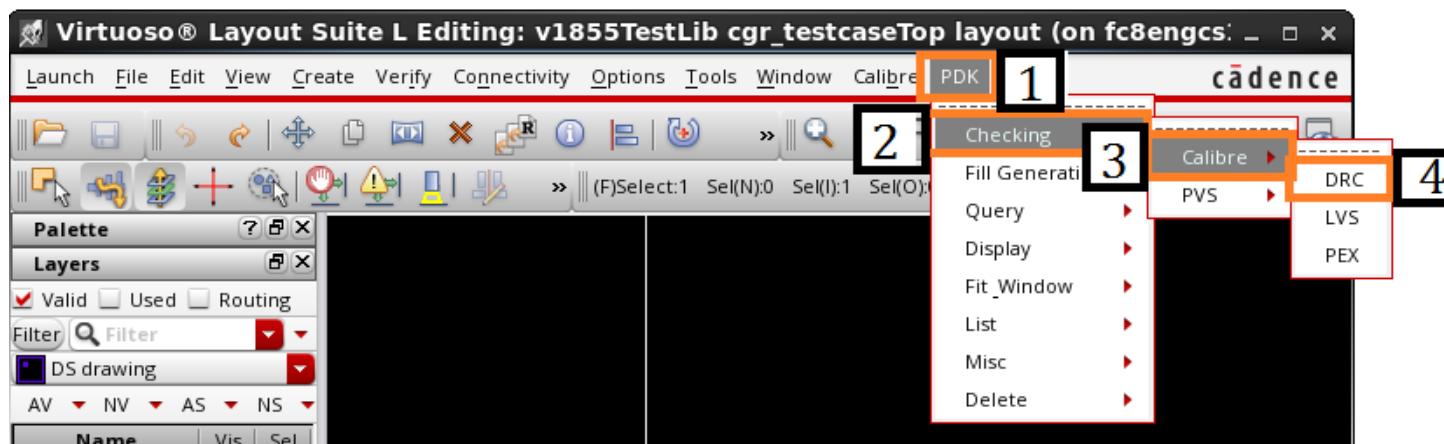
\*Apache Redhawk Totem (EMIR-000137) and Cadence Voltus\_FI (EMIR-000113) EMIR tools are supported

# Calibre DRC

- Installs into **\$GF\_PDK\_HOME/DRC/Calibre/**
- All required checks for design submission controlled by one main file – **bicmos8hp.drc.cal**
  - Include subdirectory contains multiple files with actual checks
- DRC function controlled by environment variables
- Layout gds2 must be on 0.01um grid
  - gds2 exported from Cadence with Calibre Interactive
- Documentation in **\$GF\_PDK\_HOME/DRC/Calibre /doc**
  - Calibre version tested, limitations, usage notes

# Calibre Interactive (through PDK Menu)

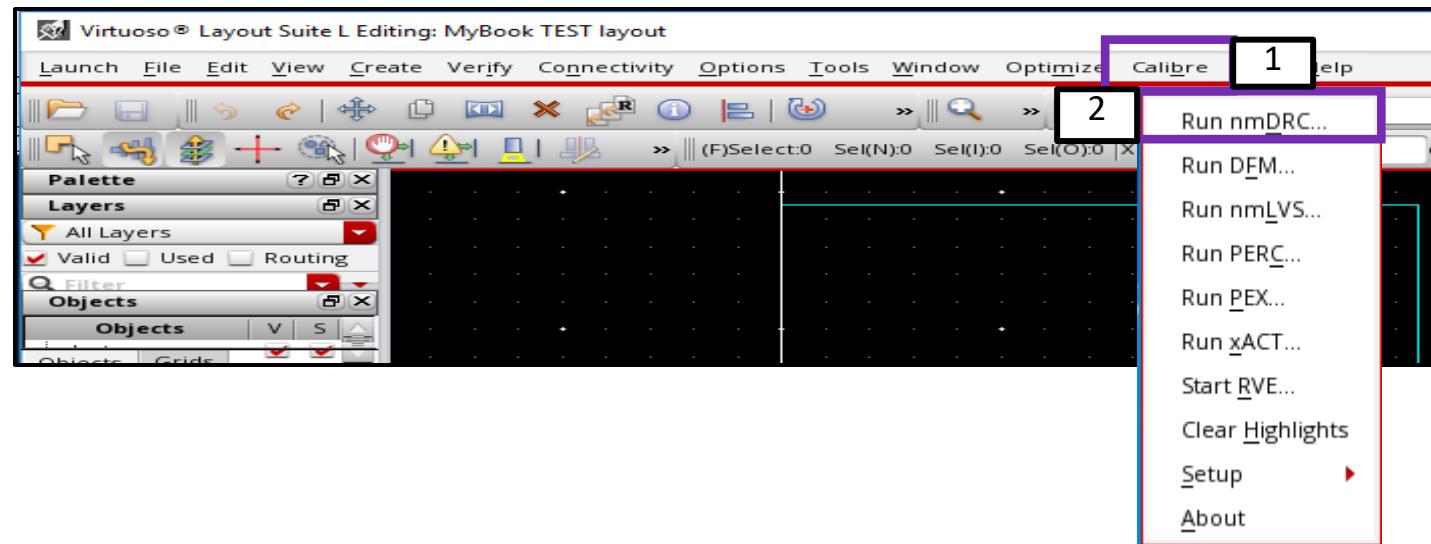
- Calibre Interactive support included in CDS design kit
  - Requires additional lines in .cdsinit file to load Calibre Interactive
    - See \$GF\_PDK\_HOME/DesignEnv/VirtuosoOA/setup/.cdsinit
- Environmental variables are required
  - PDK → Checking → Calibre → DRC
    - Launches menu for environmental variables
  - Or set variables in shell script prior to launching Cadence
  - Or load saved runset



Calibre DRC/LVS/PEX could be initiated from PDK menu, or the Calibre menu.  
GF Skill code pre-fills many fields.

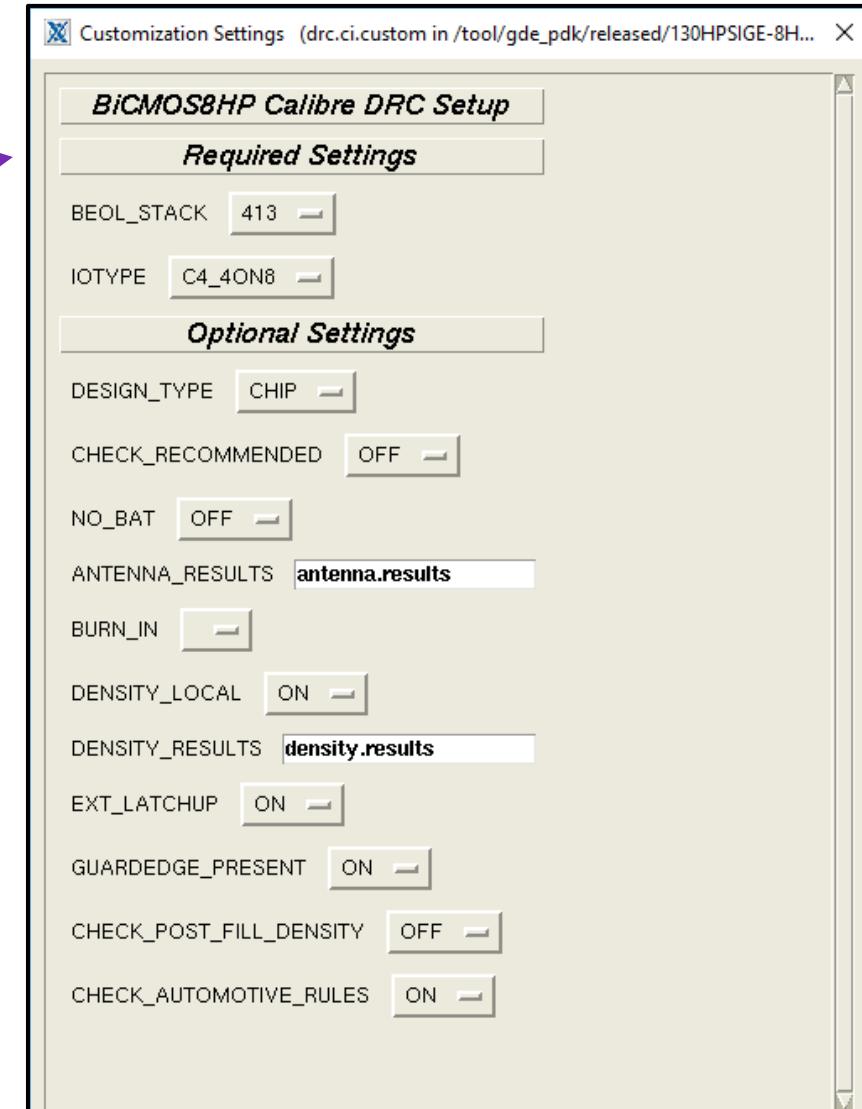
# Calibre Interactive (Launching through Calibre Menu)

From Calibre Menu : **Calibre** → Run nmDRC



# DRC Environmental Variable Setup

- Either DRC (from PDK Menu) or Run nmDRC (from Calibre Menu) will generate the customization settings



# Calibre DRC Environment Variables: Required Switches

Required Switches	Values	Description
GF_PDK_HOME	DRC Installation Directory	
BATCH	<b>None</b> , YES	Control batch mode setting
METAL_OPTION	211, 311, 411 213, 313, 413	BEOL metal stack
IOTYPE	C4_4ON8 , C4_4ON9 C4_5ON10 , CUPILLAR WB_INLINE	Type of IO
CHECK_POST_FILL_DENSITY	ON, OFF	Switch to activate final density check
CHECK_AUTOMOTIVE_RULES	ON, OFF	Activate specific ground rules for automotive
DENSITY_LOCAL	ON, OFF	Control whether density checks are run
DESIGN_TYPE	CELL, CHIP	Design type
GUARDEDGE_PRESENT	ON, OFF	
NO_BAT	ON, OFF	Turn off a subset of rules for GF bump, bond, assembly, and test processes
CHECK_RECOMMENDED	ON, OFF	Control recommended rule checks
BURN_IN	Blank, 1.5vdd	Check Design manual for more info
ANTENNA_RESULTS	<Specify Antenna File Name>	Name of antenna results file
EXT_LATCHUP	ON, OFF	Check Design manual for more info

Default shown in **BOLD**. See Calibre DRC Release Notes for complete list

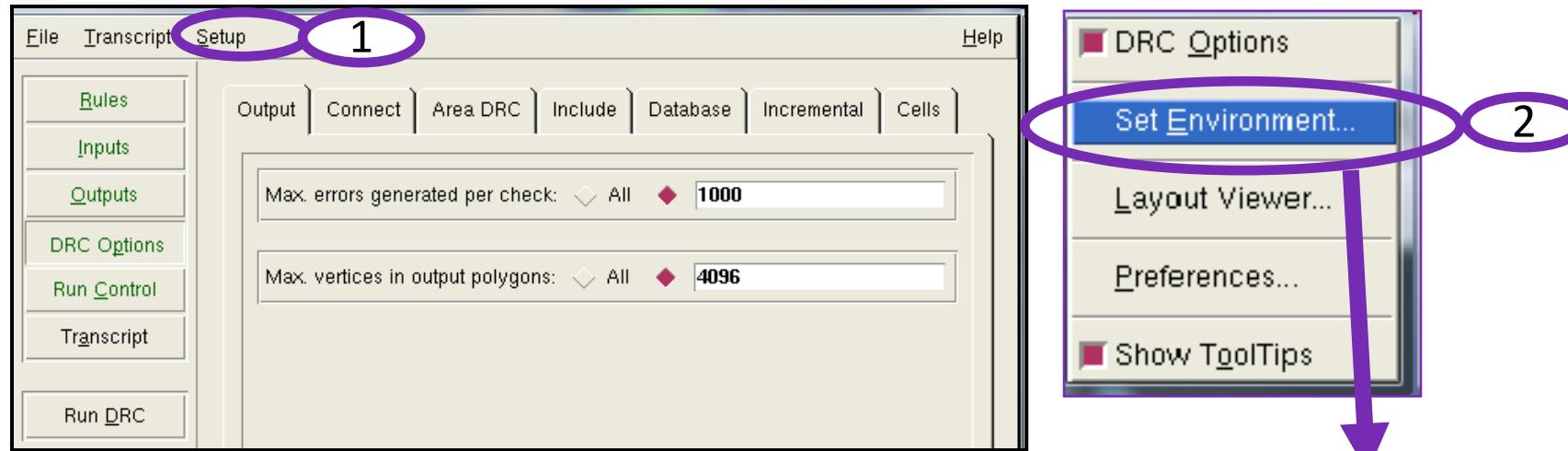
TTM-000008 Rev6

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# Calibre DRC Environmental Variable Setup – Old Method



**Setup → Set Environment**

**Note:** Use the Calibre Customization form to set DRC switches.

Values set using the "Set Environment Variables form will be overridden by the values set in the Customization Form!!!

Only values not set in the customization form can be set in the environmental variable form, like \$GF\_PDK\_HOME

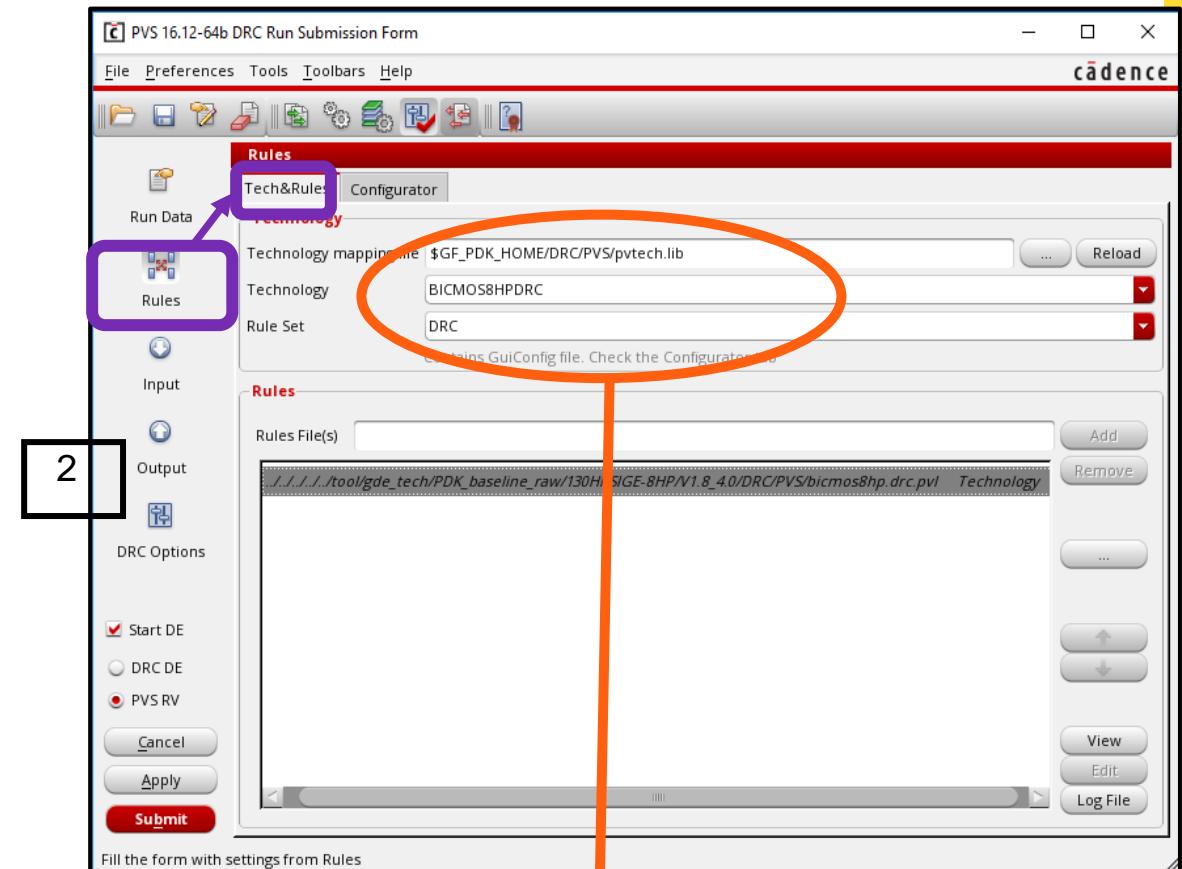
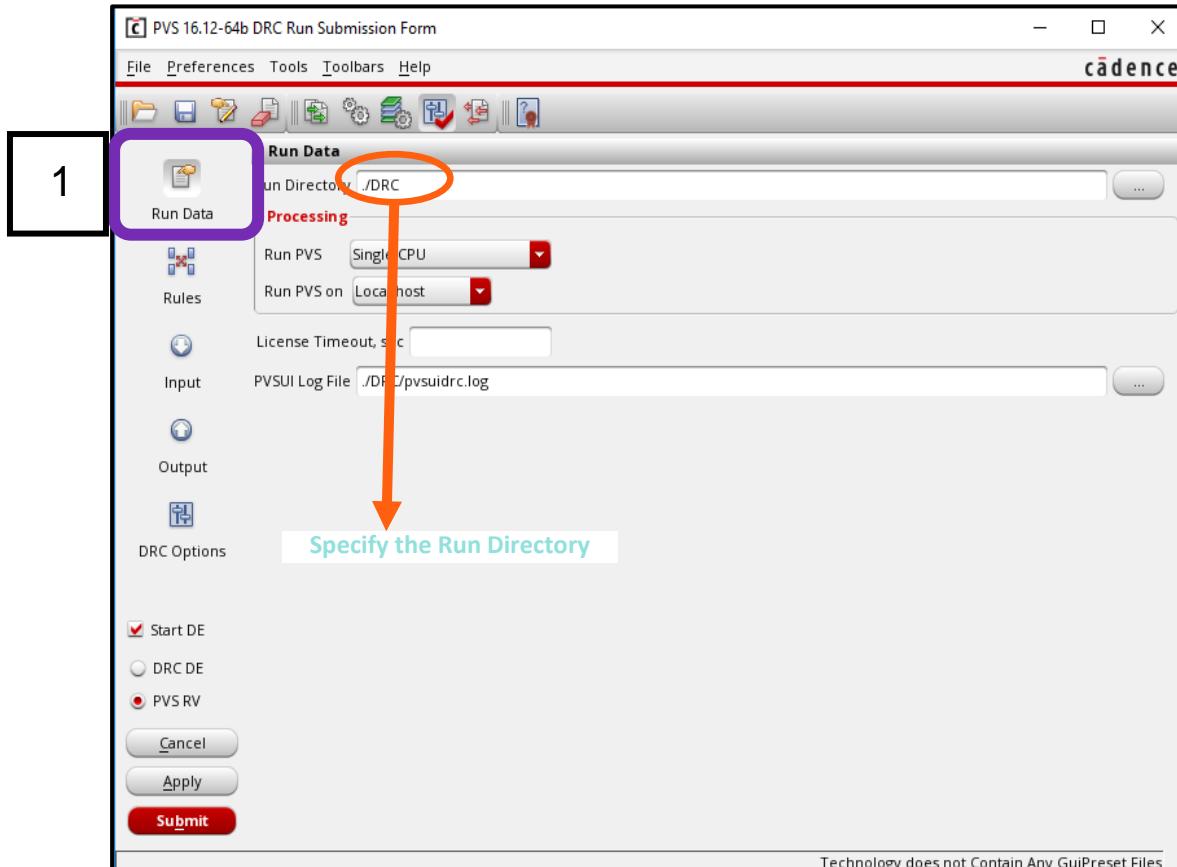
Name	Env.	Env. Value	Runset	Runset Value	Unset	In Rules
ANTENNA_RESULTS	x	<undefined>	<input checked="" type="checkbox"/>	antenna.results	<input type="checkbox"/>	<input checked="" type="checkbox"/>
BATCH	<input checked="" type="checkbox"/>	<undefined>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>
BEOL_STACK	<input checked="" type="checkbox"/>	413	<input checked="" type="checkbox"/>	413	<input type="checkbox"/>	<input checked="" type="checkbox"/>
BURN_IN	<input checked="" type="checkbox"/>	<undefined>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>
CHECK_AUTOMOTIVE_RULES	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	ON	<input type="checkbox"/>	<input checked="" type="checkbox"/>
CHECK_POST_FILL_DENSITY	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	OFF	<input type="checkbox"/>	<input checked="" type="checkbox"/>
CHECK_RECOMMENDED	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	ON	<input type="checkbox"/>	<input checked="" type="checkbox"/>
DENSITY_LOCAL	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	density.results	<input type="checkbox"/>	<input checked="" type="checkbox"/>
DENSITY_RESULTS	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	CHIP	<input type="checkbox"/>	<input checked="" type="checkbox"/>
DESIGN_TYPE	<input checked="" type="checkbox"/>	<undefined>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>
EXCLUDE_CELL	<input checked="" type="checkbox"/>	<undefined>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>
EXT_LATCHUP	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	ON	<input type="checkbox"/>	<input checked="" type="checkbox"/>
GF_PDK_HOME	<input checked="" type="checkbox"/>	/tool/gde_tech/PDK_baseline_raw/130HPSIGE-8HP/V1.8_4.0	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>
GUARDEDGE_PRESENT	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	ON	<input type="checkbox"/>	<input checked="" type="checkbox"/>
IOTYPE	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	C4_4ON8	<input type="checkbox"/>	<input checked="" type="checkbox"/>
LAYOUT_PATH	<input checked="" type="checkbox"/>	<undefined>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>
NO_BAT	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	OFF	<input type="checkbox"/>	<input checked="" type="checkbox"/>
RESULTS_DATABASE	<input checked="" type="checkbox"/>	<undefined>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>
SELECT_CHECKS	<input checked="" type="checkbox"/>	<undefined>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>
SUMMARY_REPORT	<input checked="" type="checkbox"/>	<undefined>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>

# PVS DRC

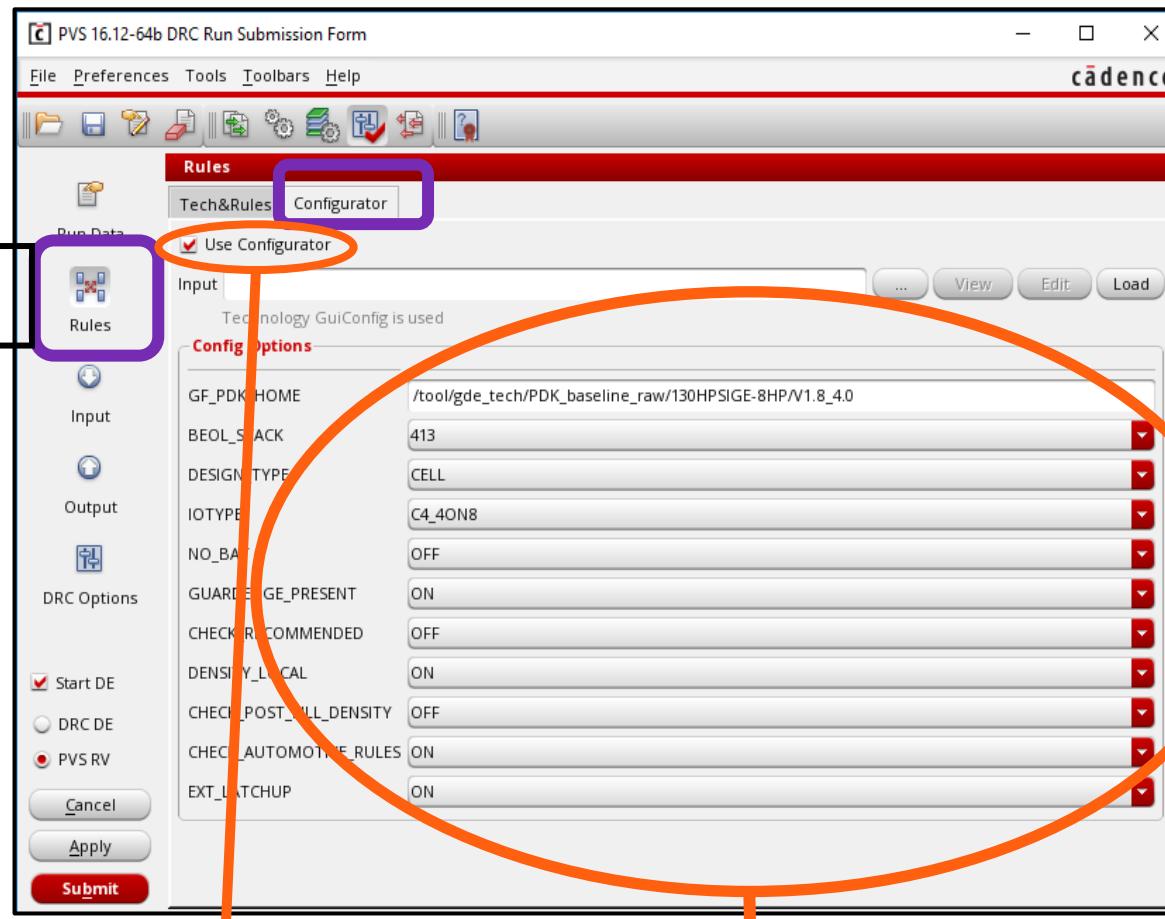
- Installs into **\$GF\_PDK\_HOME/DRC/PVS/**
- Launch interactive PVS DRC using the Cadence pulldown menu : **PVS → Run DRC (or)**  
PDK Pulldown menu : **PDK → Checking → PVS → DRC**
- All required checks for design submission controlled by one main file – **bicmos8hp.drc.pvl**
  - **Include** subdirectory contains multiple files with actual checks
- DRC function controlled by environment variables
  - .cshrc - “**setenv PVSTECHDIR\_DRC path**”
  - .kshrc - **export PVSTECHDIR\_DRC=“path”**
  - The shell variable **PVSTECHDIR\_DRC** should be set to the directory location of the deck / runset
- Documentation in **\$GF\_PDK\_HOME/DRC/PVS/doc**

# Run PVS DRC

From Layout Window, PDK → Checking → PVS → DRC  
Follow Steps 1 and 4 to complete the DRC Run Submission Form

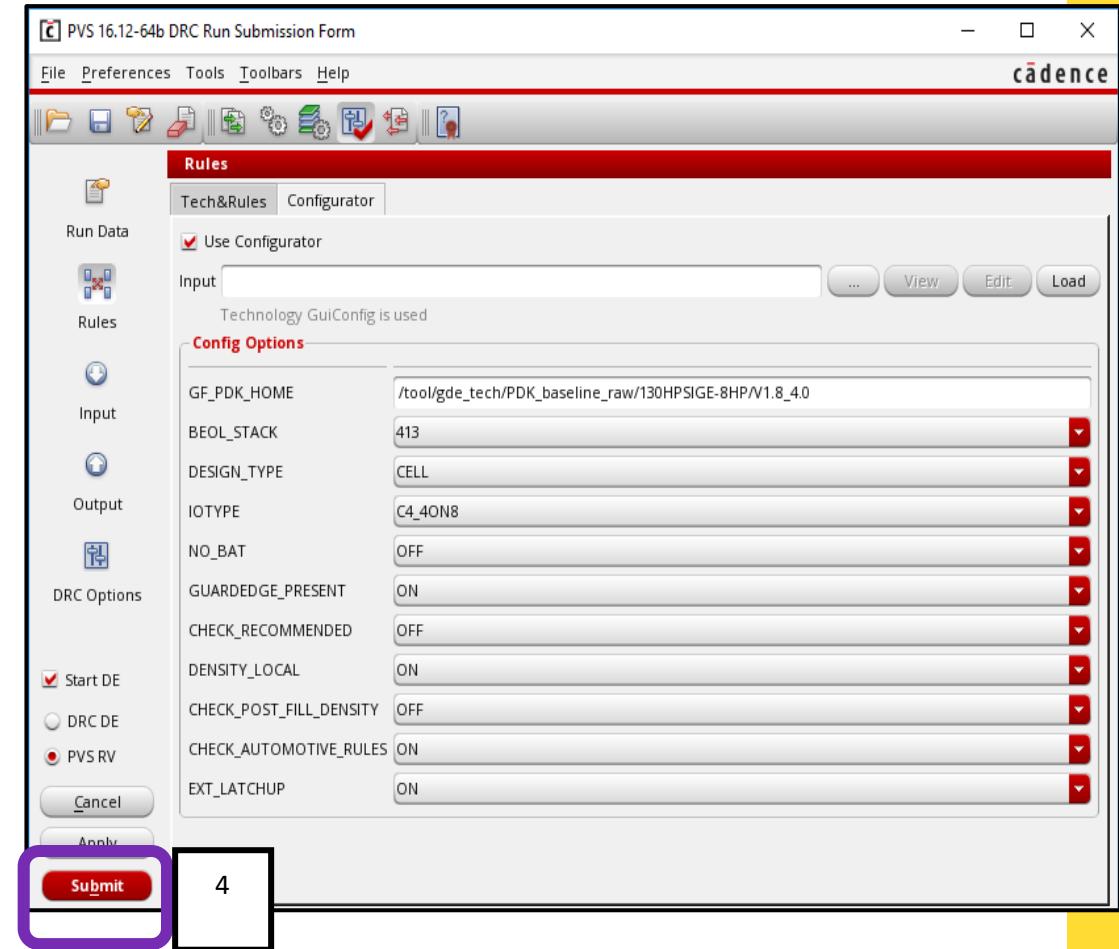


# Run PVS DRC Contd...



Check this box

Users to select the options- details in next page



# PVS DRC Environment Variables: Required Switches

Required Switches	Values	Description
TECHDIR	DRC Installation Directory	
BATCH	<b>None</b> , YES	Control batch mode setting
METAL_OPTION	211, 311, 411 213, 313, 413	BEOL metal stack
IOTYPE	C4_4ON8 , C4_4ON9 C4_5ON10 , CUPILLAR WB_INLINE	Type of IO
CHECK_POST_FILL_DENSITY	ON, OFF	Switch to activate final density check
CHECK_AUTOMOTIVE_RULES	ON,OFF	Activate specific ground rules for automotive
DENSITY_LOCAL	ON, OFF	Control whether density checks are run
DESIGN_TYPE	CELL, CHIP	Design type
GUARDEDGE_PRESENT	ON, OFF	
NO_BAT	ON, OFF	Turn off a subset of rules for GF bump, bond, assembly, and test processes
CHECK_RECOMMENDED	ON, OFF	Control recommended rule checks
BURN_IN	Blank, 1.5vdd	Check Design manual for more info
ANTENNA_RESULTS		Name of antenna results file
EXT_LATCHUP	ON, OFF	Check Design manual for more info

Default shown in **BOLD**

# PVS DRC Known Limitations

BiCMOS8HP Process Design Kit Release Notes – PVS DRC

## 6.0 Known Limitations

Below is a listing of known limitations of the BiCMOS8HP PVS DRC Component.

- Width-dependent spacing checks such as LY2a have been shown to flag false violations. This was discovered late in the IP testing process and requires a considerable amount of development work to make sure that PVS DRC produces results that is consistent with the other DRC tools that we offer. Work in this regard will be done to address this issue in the next PDK release.

**Added in V1.8\_4.0:**

**OZ15a** (multiple OZ shapes in the same BB) – This rule will generate errors, at this time, if multiple VPNPs are placed inside a single BB shape. This rule may be modified for the next PDK release.

# Layout Geometry Restriction Rules (S1 – S11)

- Calibre and PVS perform the checks for some of these rules during the data integrity check
- Results are placed into a separate database (srules\_errors.rdb), attached to the main error database
- A non-zero Check LAYOUT\_INPUT\_EXCEPTION\_RDBS in the results viewer indicates that there are errors to review in srules\_errors.rdb
- Rule names for these errors do not adhere to the design manual's naming convention, but instead reflects to type of check

The screenshot shows two windows side-by-side. On the left is the Calibre - RVE v2018.4\_44.36 : SxRule\_Errors.rdb interface. It has a toolbar at the top, a menu bar, and a main window titled 'Tile\_v1.db' with 'SxRule\_Errors.rdb'. A red box highlights 'Error Database' and an arrow points from it to the right window. Below this, a red box highlights 'List of Calibre data integrity checks errors' and an arrow points from it to the left window's results table. Another red box highlights 'Layer number (15.0)' involved in violation and an arrow points from it to the left window's detailed error message. The right window is a terminal or log window showing a list of layout input exception rules. A red box highlights 'List of typical error names' and an arrow points from it to the right window's content. The code in the right window includes comments explaining various layout rules like S1, S2, S3, S4, S5, S6, S7, S8, and S9.

```
LAYOUT INPUT EXCEPTION RDB "SxRule_Errors.rdb" BY EXCEPTION // setting the name of the RDB
//===== $1,$3,$4,$5,$8,$9 =====
LAYOUT INPUT EXCEPTION SEVERITY PATH_WIDTH_ODD 1 RDB // Ignore precision errors for off-grid centerline & report as off-grid
LAYOUT INPUT EXCEPTION SEVERITY PATH_WIDTH_MULTIPLE 3 RDB // S1 RULE - Off-Grid path envelopes
LAYOUT INPUT EXCEPTION SEVERITY PATH_EXTENSION_MULTIPLE 3 RDB // S1 RULE - Off-Grid path centerline ends
LAYOUT INPUT EXCEPTION SEVERITY PLACEMENT_MULTIPLE 1 RDB // S1 RULE - Off-Grid Instances Origin
LAYOUT INPUT PATH_EXTENSION_MULTIPLE 10 RDB // Number is the same as the resolution
LAYOUT INPUT PLACEMENT_MULTIPLE 10 RDB // Number is the same as the resolution
LAYOUT INPUT PATH_EXTENSION_MULTIPLE 10 RDB // Number is the same as the resolution
LAYOUT INPUT EXCEPTION SEVERITY PATH_DEGENERATE 1 RDB // S3 RULE
LAYOUT INPUT EXCEPTION SEVERITY PATH_NONSIMPLE 1 RDB // S3 RULE
LAYOUT INPUT EXCEPTION SEVERITY POLYGON_NONSIMPLE 1 RDB // S3 RULE
LAYOUT INPUT EXCEPTION SEVERITY POLYGON_DEGENERATE 1 RDB // S4 RULE
LAYOUT INPUT EXCEPTION SEVERITY POLYGON_NONORIENTABLE 1 RDB // S4 RULE // Setting to Warn and ignore
LAYOUT INPUT EXCEPTION SEVERITY PATH_NONORIENTABLE 1 RDB // S4 RULE
LAYOUT INPUT EXCEPTION SEVERITY ERROR_ON_INPUT YES 1 RDB // S4 RULE
LAYOUT INPUT EXCEPTION SEVERITY PATH_WIDTH_ZERO 1 RDB // S5 RULE
LAYOUT INPUT EXCEPTION SEVERITY POLYGON_AREA_ZERO 1 RDB // S5 RULE
LAYOUT INPUT EXCEPTION SEVERITY RECTANGLE_SIDE_ZERO 1 RDB // S5 RULE
LAYOUT INPUT EXCEPTION SEVERITY POLYGON_NOT_CLOSED 1 RDB // S5 RULE
LAYOUT INPUT EXCEPTION SEVERITY PATH_ANGLED 3 RDB // S8 RULE
LAYOUT INPUT EXCEPTION SEVERITY PATH_ENDSEGMENT_SHORT 1 RDB // S9 RULE
//===== Other Layout Input Exceptions =====
LAYOUT INPUT EXCEPTION SEVERITY LAYOUT_POLYGON 0 RDB // Used in PCI checks.
LAYOUT INPUT EXCEPTION SEVERITY ARRAY_PITCH_ZERO 1 RDB // 
LAYOUT INPUT EXCEPTION SEVERITY MISSING_REFERENCE 1 RDB // Allow layouts with cells referenced but not defined
LAYOUT INPUT EXCEPTION SEVERITY INSIDE_CELL 0 RDB // SUPPRESS cell name matching warning
LAYOUT INPUT EXCEPTION SEVERITY EXTENT_CELL 0 RDB // SUPPRESS extent cell name matching warning
```

List of typical error names

The output is similar for both  
Calibre and PVS

# Antenna Rules

- Design should meet antenna rules
  - Rules Require connectivity information ...
    - For example, CA connects M1 to RX and to PC
- ... and/or involve ratio of areas**
- Examples:
    - Antenna rules for gate oxide integrity
      - 130a: For each shape intersecting RX, the ratio of the total PC area to the PC (intersecting RX) area must be less than 100:1

# **Global and Local Density Checking\***

- Global pattern density requirements**

- Levels : RX, PC, DT, EV, EX, QY, LY, E1, MA, AM, LV, DV, SV
  - Minimum and / or maximum density on chip overall

- Local pattern density requirements**

- Levels : RX, PC, Mx (x=M1, M2, M3, M4, MQ), E1
  - Chip divided into smaller local checking boxes
  - Minimum and / or maximum density within localized regions
    - Checking box stepped across chip

- Incoming design data must meet global/local requirements**

\*Additional details in Layout Topics Section

# ESD and Recommended Rules

- **ESD Rules (Section 6 of Design Manual)**
  - To ensure robustness of I/Os for electro-static discharge events
  - Partial implementation in DRC decks
    - Check release notes for known limitations
  - Recommended, but not required\*
    - Not used as part of design submission criteria
- **Recommended Rules (Dispersed throughout Section 3 of Design Manual)**
  - Rules with “R” suffix
  - More conservative value for selected rules
  - May increase yield
  - Use only if no adverse affect on chip size and performance
  - Not used as part of design submission criteria

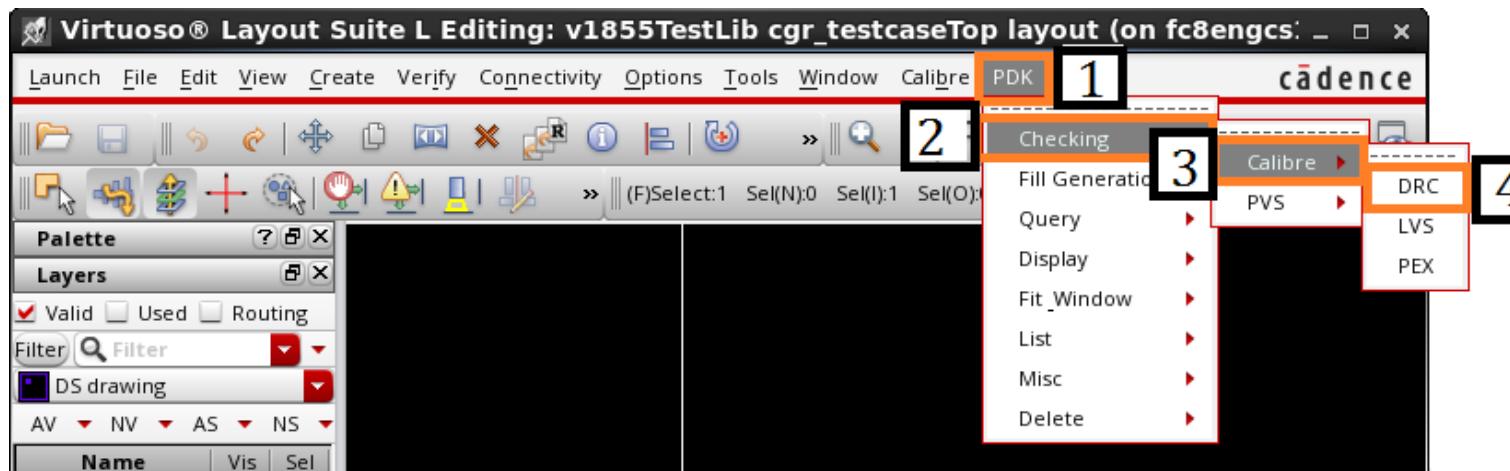
\*Required only when deliverable is a tested module

# Calibre Layout vs Schematic (LVS)

- **Calibre (Mentor Graphics)**
  - CDL netlist for Schematic Design Source
  - gds2 for Layout Extraction, exported from Cadence with Calibre Interactive
- **Installs into \$GF\_PDK\_HOME/LVS/Calibre/**
- **Required checks controlled by one main file – bicmos8hp.lvs.cal**
  - **Include** subdirectory contains multiple files with actual checks
- **LVS function controlled by environment variables**
  - .cshrc - “setenv TECHDIR path”
  - .kshrc - export TECHDIR=“path”
  - The shell variable TECHDIR should be set to the directory location of the deck / runset
- **Documentation in \$GF\_PDK\_HOME/LVS/Calibre /doc**
  - Calibre version tested, limitations, usage notes

# Calibre Interactive ( through PDK Menu)

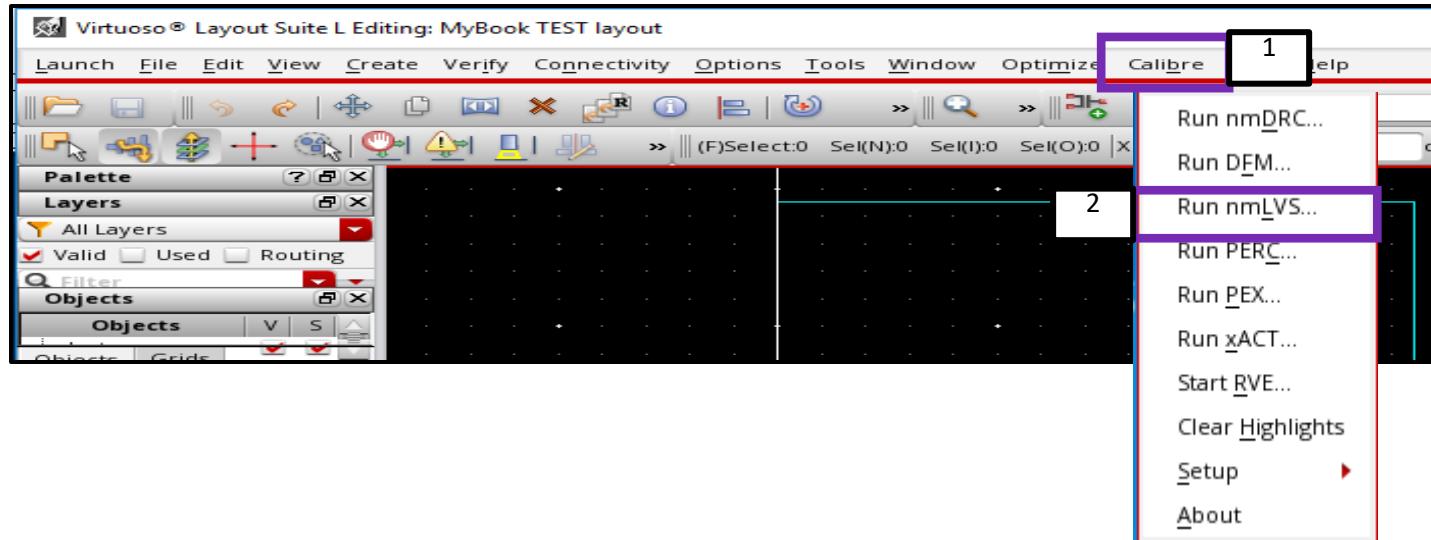
- Calibre Interactive support included in CDS design kit
  - Requires additional lines in .cdsinit file to load Calibre Interactive
    - See \$GF\_PDK\_HOME/DesignEnv/VirtuosoOA/setup/.cdsinit
- Environmental variables are required
  - PDK → Checking → Calibre → LVS
    - Launches menu for environmental variables
  - Or set variables in shell script prior to launching Cadence
  - Or load saved runset



Calibre LVS can be launched from either the PDK or Calibre menu options.  
All of the default settings are populated by the GF PDK Skill code

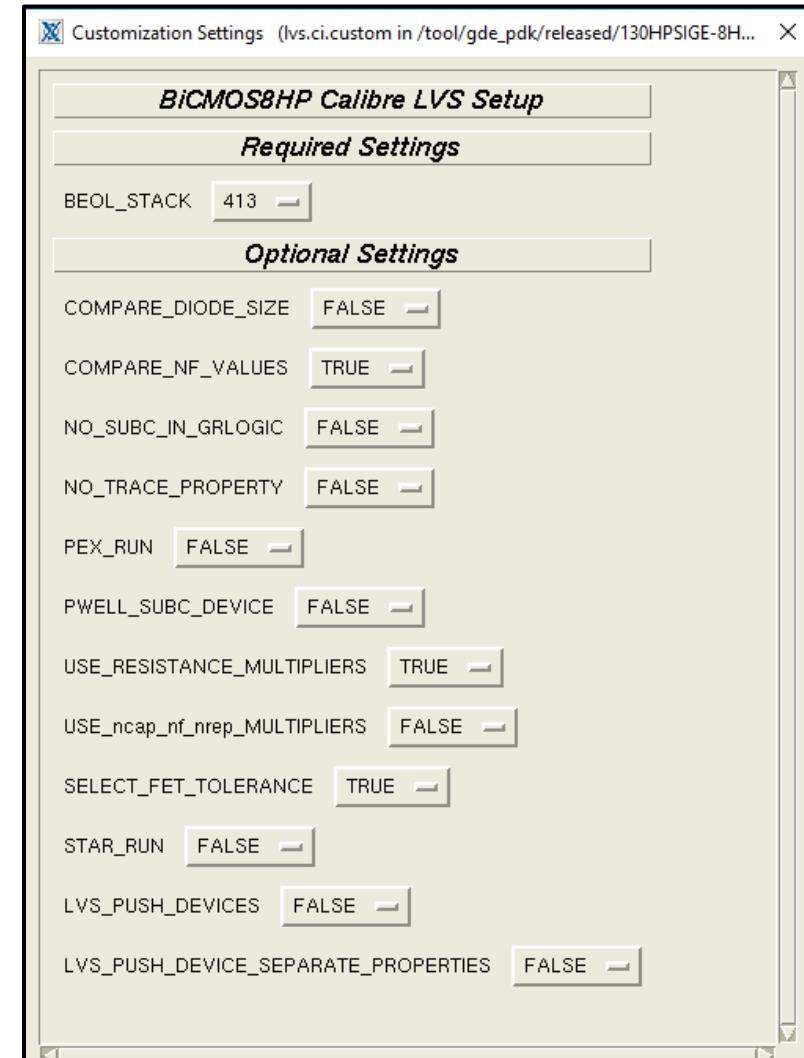
# Calibre Interactive (Launching through Calibre Menu)

From Calibre Menu : Calibre → Run nmLVS



# Calibre Interactive Mode

- LVS Environmental Variables may be set through menu
  - PDK→Checking→Calibre→LVS
- Alternatively
  - Calibre→Run LVS
- Environmental variables for LVS documented in
  - /\$GF\_PDK\_HOME/LVS/Calibre/doc/bicmos8hp.CalibreLVS.rel\_notes.pdf



# Calibre LVS Environmental Variables – Old Method

- NOTE: Do not use the "Set Environmental Variables" for to set the variables as in the past. The values set in this form will be overriden by the values set in the Customization Form. Only variables not managed in the customization form can be set in the Environmental Variable form, like \$GF\_PDK\_HOME
- Environmental variables for LVS documented in
  - /\$GF\_PDK\_HOME/LVS/Calibre/doc/bicmos8hp.CalibreLVS.rel\_notes.pdf

The screenshot shows a Windows-style dialog box titled "Set Environment Variables". It has two tabs at the top: "Set Env." (selected) and "Current Env.". Below the tabs is a section labeled "Set Environment Variables:" containing a table. The table has columns for "Name", "Env.", "Env. Value", "Runset", "Runset Value", "Unset", and "In Rules". The "Name" column lists various environment variables. The "Env." column contains checkboxes, many of which are checked. The "Env. Value" column contains variable values or undefined states. The "Runset" and "Runset Value" columns show checkboxes for setting run configurations. The "Unset" and "In Rules" columns also contain checkboxes.

Name	Env.	Env. Value	Runset	Runset Value	Unset	In Rules
BEOL_STACK	<input checked="" type="checkbox"/>	413	<input checked="" type="checkbox"/>	413	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
COMPARE_DIODE_SIZE	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
COMPARE_NF_VALUES	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	TRUE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
GF_PDK_HOME	<input checked="" type="checkbox"/>	/tool/gde_tech/PDK_baseline_raw/130HPSIGE-8HP/V1.8_4.0	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
INCLUDE_MX_FILL_IN_PEX	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
INCLUDE_PC_FILL_IN_PEX	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
LVS_PUSH_DEVICES	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
LVS_PUSH_DEVICE_SEPARATE_PROPERTIES	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
NO_SUBC_IN_GRLOGIC	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
NO_TRACE_PROPERTY	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PEX_RUN	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PWELL_SUBC_DEVICE	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
RUN_ERC	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SELECT_FET_TOLERANCE	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	TRUE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
STAR_RUN	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
USE_RESISTANCE_MULTIPLIERS	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	TRUE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
USE_ncap_nf_nrep_MULTIPLIERS	<input checked="" type="checkbox"/>	<undefined>	<input checked="" type="checkbox"/>	FALSE	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

# Calibre LVS Environment Variables

Required Switches	Values	Description	Env Variable Name
TECHDIR	\$GF_PDK_HOME/LVS/Calibre	PDK directory	\$TECHDIR
BEOL_STACK	211, 311, 411 213, 313, 413	BEOL metal stack	\$METAL_OPTION
COMPARE_DIODE_SIZE	FALSE, TRUE	Compare area of tiedown diodes (tdndsx,tdpdnw)	\$COMPARE_DIODE_SIZE
COMPARE_NF_VALUES	TRUE, FALSE	This option defines whether or not you wish to compare the 'nf' parameter on devices that have this parameter.	\$COMPARE_NF_VALUES
NO_SUBC_IN_GRLOGIC	TRUE, FALSE	This option will not extract substrate contact devices for LVS compare which are under GRLOGIC filter shape	\$NO_SUBC_IN_GRLOGIC

Default shown in **BOLD**

# Calibre LVS Environment Variables Contd..

Required Switches	Values	Description	Env Variable Name
<b>INCLUDE_PC_FILL_IN_PEX</b>	<b>FALSE, TRUE</b>	This option defines whether floating PC fill shapes will get passed to PEX for coupling.	<b>\$INCLUDE_PC_FILL_IN_PEX</b>
<b>INCLUDE_MX_FILL_IN_PEX</b>	<b>FALSE, TRUE</b>	This option defines whether floating metal fill shapes will get passed to PEX for coupling.	<b>\$INCLUDE_MX_FILL_IN_PEX</b>
<b>PEX_RUN</b>	<b>TRUE, FALSE</b>	This option defines a parasitic extraction on the layout.	<b>\$PEX_RUN</b>
<b>PWELL_SUBC_DEVICE</b>	<b>TRUE, FALSE</b>	This option will extract substrate contact devices under triple wells	<b>\$P WELL_SUBC_DEVICE</b>
<b>Use_ncap_nf_nrep_MULTIPLIERS</b>	<b>FALSE, TRUE</b>	This option compares the product of nf, nrep & m for ncp/ dgncap devices	<b>\$Use_ncap_nf_nrep_MULTIPLIERS</b>
<b>USE_RESISTANCE_MULTIPLIERS</b>	<b>FALSE, TRUE</b>	If your source netlist contains the parameter pbar > 1 or s > 1 on resistor devices, this must be set to TRUE to pick up the resistance multiplication.	<b>\$USE_RESISTANCE_MULTIPLIERS</b>

Default shown in **BOLD**

# Calibre LVS Environment Variables Contd..

Required Switches	Values	Description	Env Variable Name
<b>SELECT_FET_TOLERANCE</b>	<b>FALSE, TRUE</b>	0.5% tolerance is allowed for FETs	<b>\$SELECT_FET_TOLERANCE</b>
<b>STAR_RUN</b>	<b>FALSE, TRUE</b>	This option is set to TRUE to enable Star RC	<b>\$STAR_RUN</b>
<b>LVS_PUSH_DEVICES</b>	<b>FALSE,TRUE</b>	This option is set to TRUE to enable Star RC	<b>\$LVS_PUSH_DEVICES</b>
<b>LVS_PUSH_DEVICE_SEPARATE_PROPERTIES</b>	<b>FALSE, TRUE</b>	This option is set to TRUE to enable Star RC	<b>\$LVS_PUSH_DEVICE_SEPARATE_PROPERTIES</b>

Default shown in **BOLD**

# Device Filtering

- The Calibre LVS rules file will filter dummy or spare devices out of either netlist according to the following conventions:

FETs:	Devices with S/D/G pins all tied together will be filtered Devices with S/D/G pins all floating or unconnected will be filtered
Resistor:	Devices with both terminals shorted will be filtered Devices with both terminals floating or unconnected will be filtered
Capacitor:	Devices with both terminal floating will be filtered Devices with both terminals shorted will be filtered
Diode:	Devices with POS and NEG pins tied together

# PVS LVS

- Installs into **\$GF\_PDK\_HOME/LVS/PVS/**
- Launch interactive PVS LVS using the following Cadence pulldown menu :
  - PVS → Run LVS
  - PDK → Checking → PVS → LVS
- All required checks for design submission controlled by one main file – **bicmos8hp.lvs.pvl** which would call the Include subdirectory that contains multiple files with actual checks
- LVS function controlled by environment variables
  - cshrc - “setenv TECHDIR path”
  - .kshrc - export TECHDIR=“path”
  - The shell variable TECHDIR should be set to the directory location of the deck / runset
- Documentation in **\$GF\_PDK\_HOME/LVS/PVS /doc**
  - PVS LVS version tested, limitations, usage notes

# LVS Ports and Labels

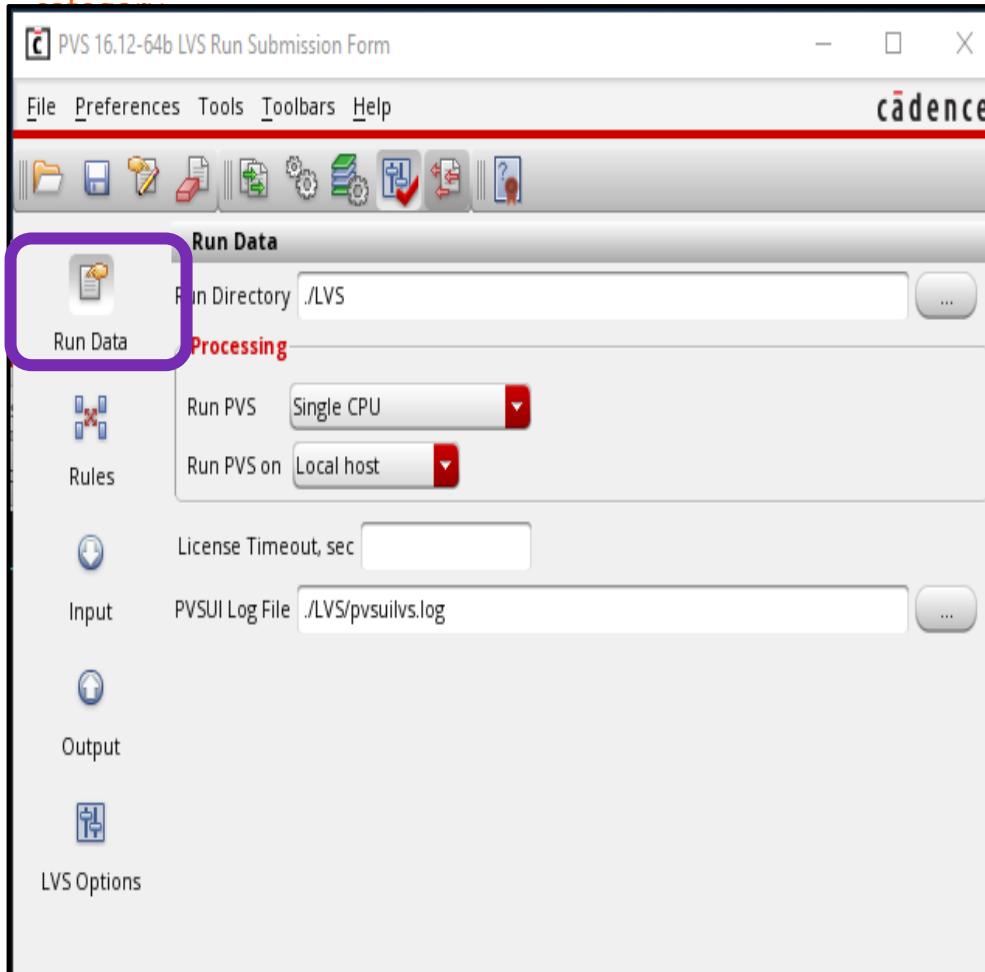
- Ports are defined as texted nets which are always compared by name between the schematic and the layout.
- Texted nets are nets that posses a user-given name but do not need to match in name or number between schematic and layout.
- The procedure for bicmos8hp is :
  - To create a Port in the layout, create a label using the layer name on purpose “pin” and place over the layer to be contacted.
  - To create a texted net, create a label using the layer name on purpose “label”. For example,
    - ✓ A label on M1 pn → creates port on M1 metal
    - ✓ A label on MA pn → creates port on MA metal
    - ✓ A label on MA II → creates a texted net on MA metal
    - ✓ A label on PC II → creates a texted net on PC

# Run PVS LVS

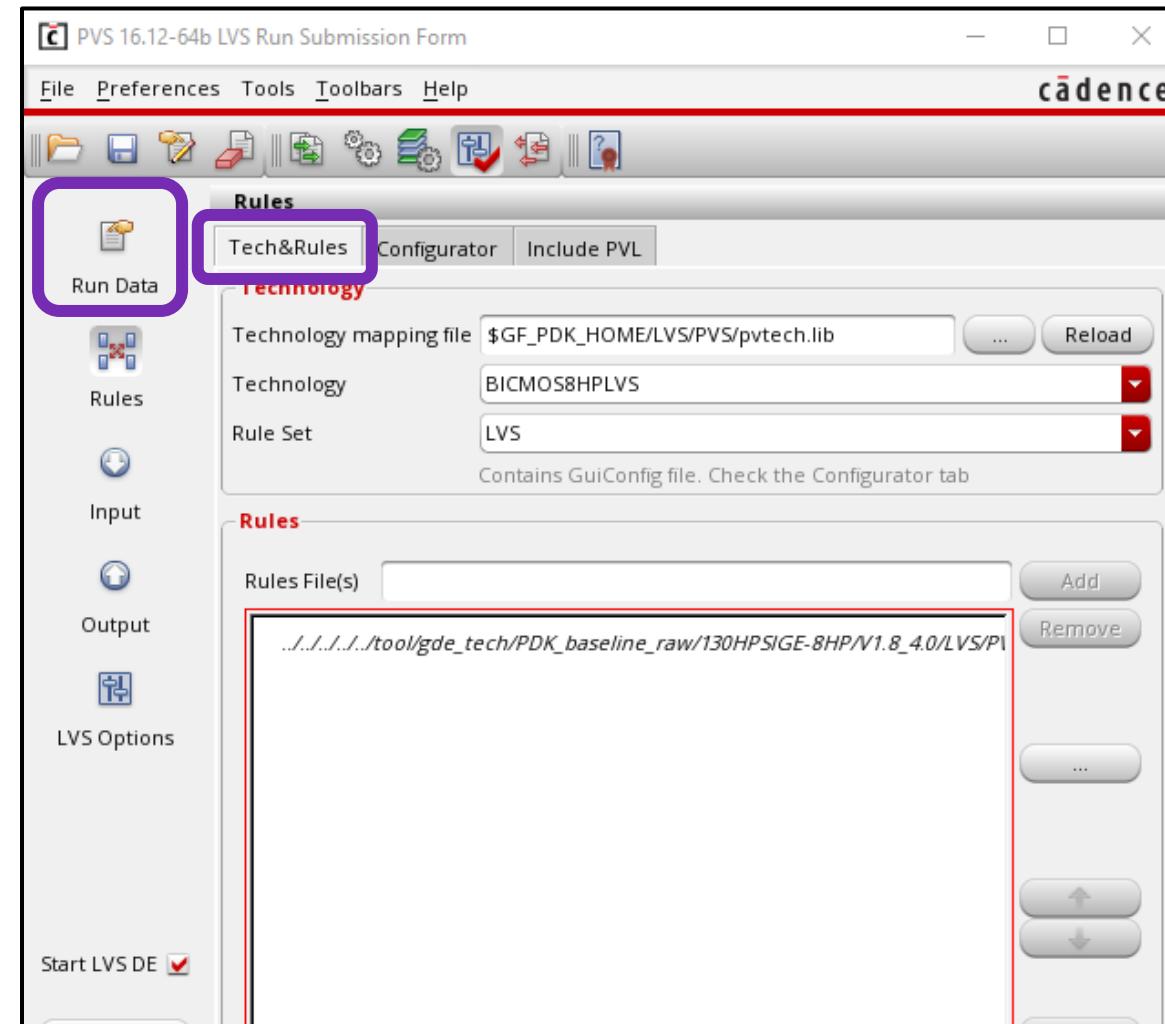
From Layout Window, PDK → Checking → PVS → LVS

Follow Steps 1 and 4 to complete the LVS Run Submission Form

1. The PVS DRC submission form will allow to set the run directory path as well as host and CPU through the 'Run Data' section.



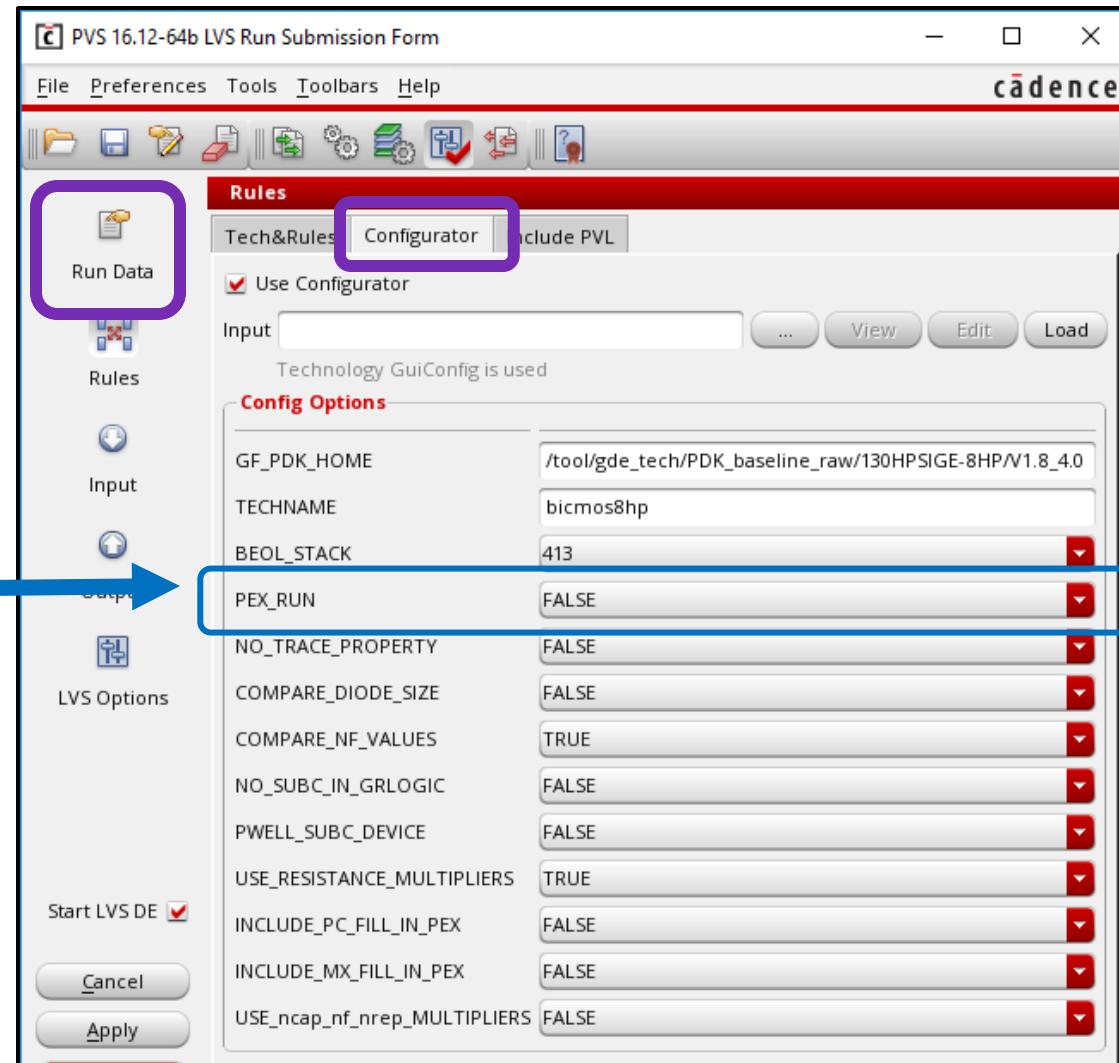
2. The 'Rules' category set "csoi8sw\_lvs" and "LVS\_Default" in the 'Tech&Rules'



# Run PVS LVS Contd..

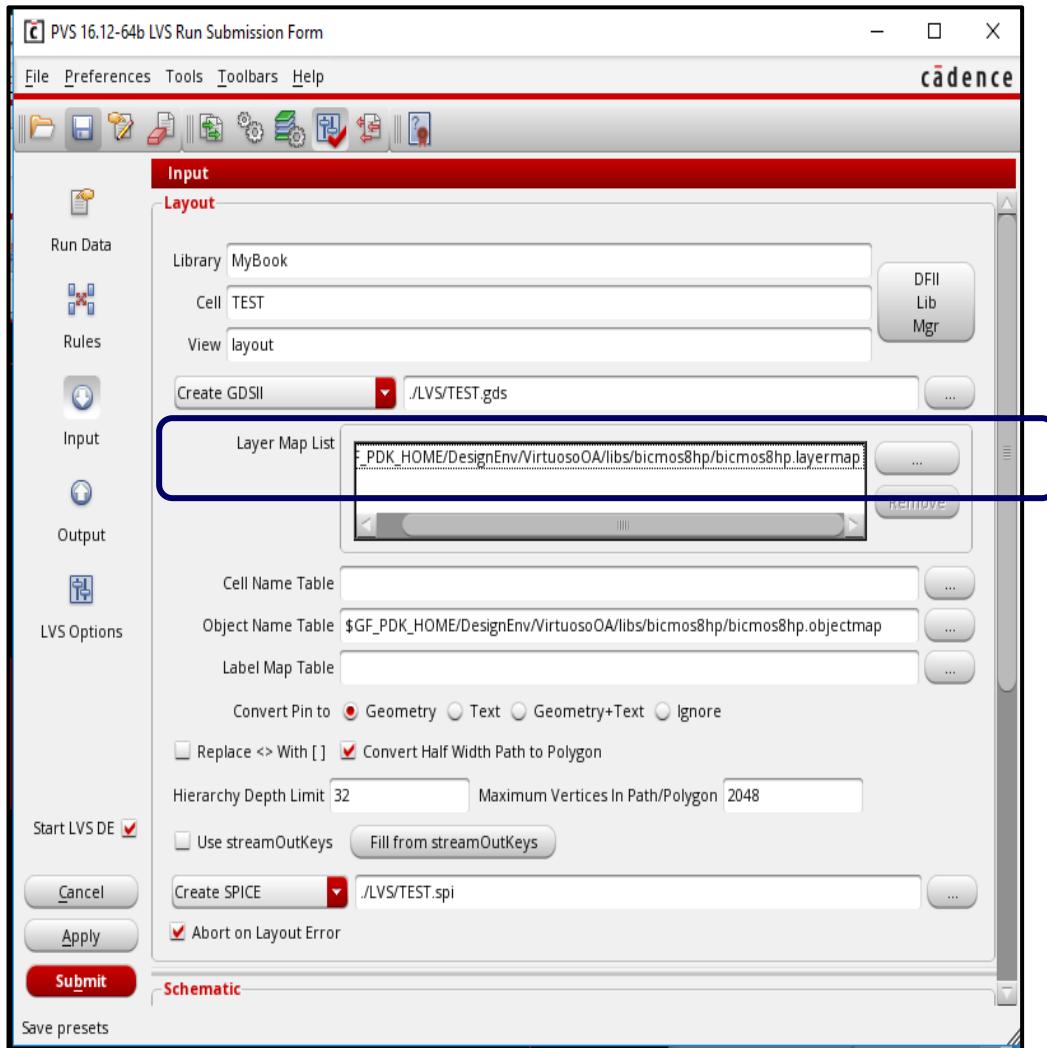
3. The 'configurator' category sets all LVS environmental variables

Set PEX\_RUN="TRUE" for a PVS LVS to QRC run

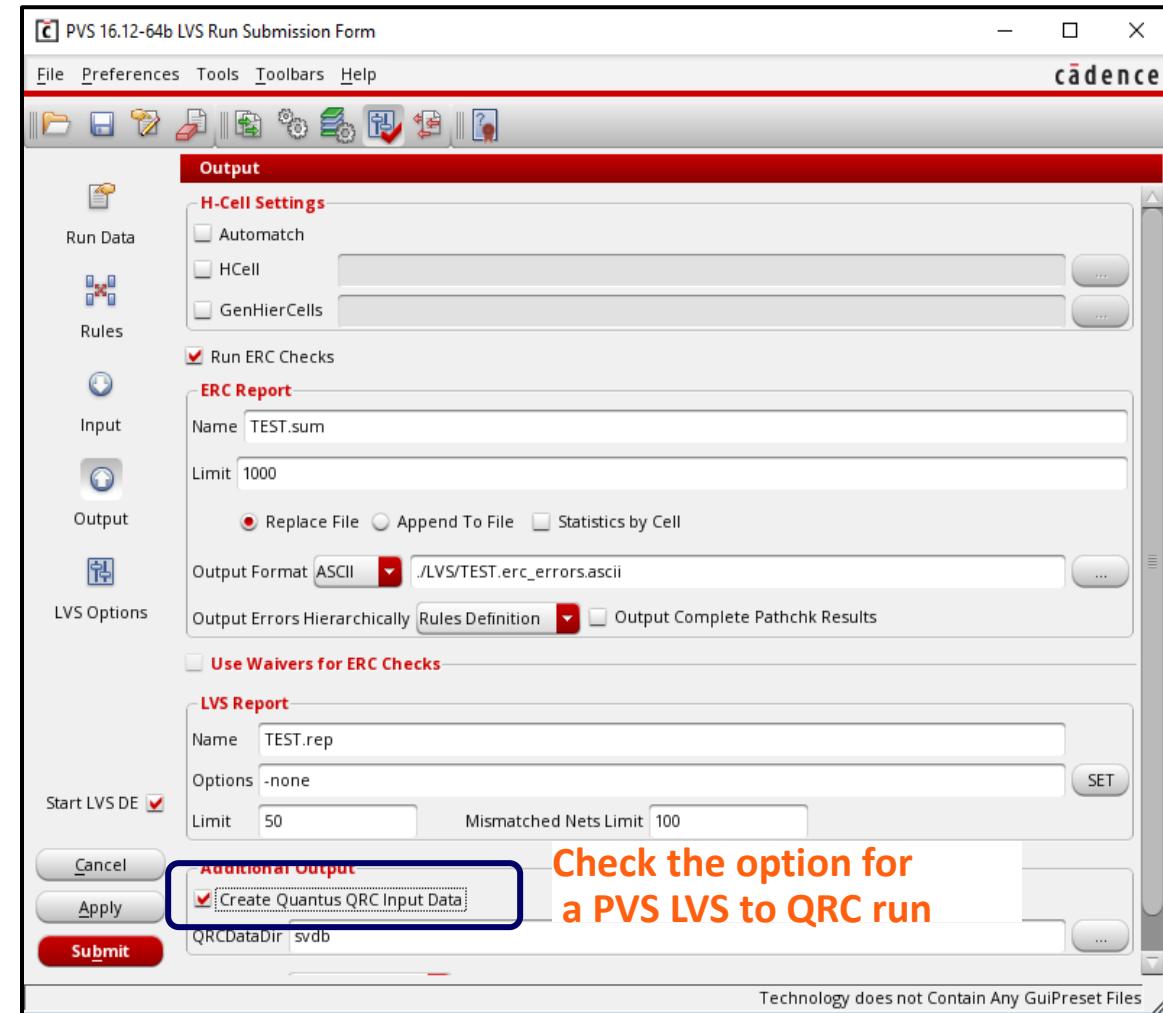


# Run PVS LVS Contd...

## 4. INPUT



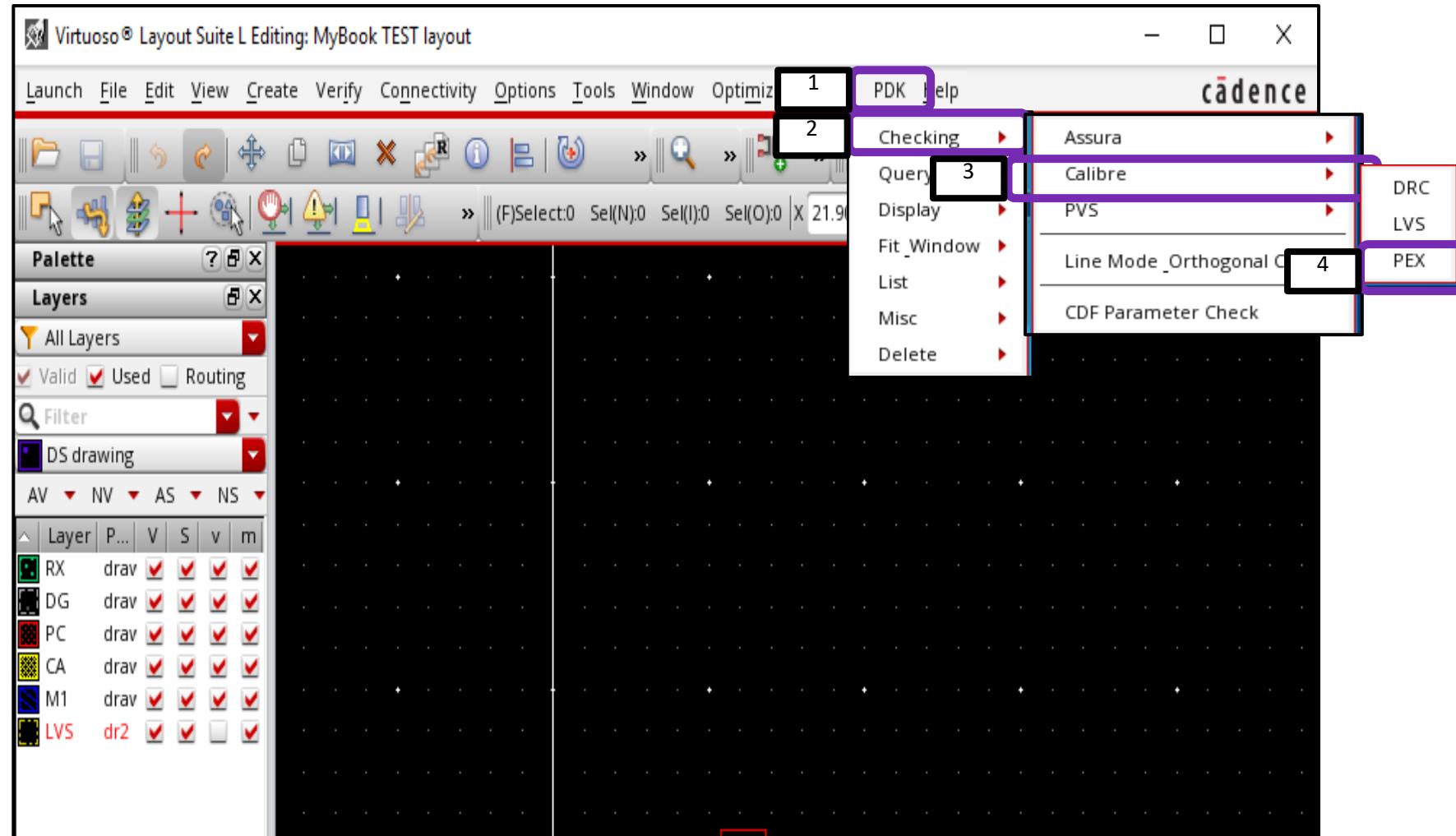
## 5. OUTPUT



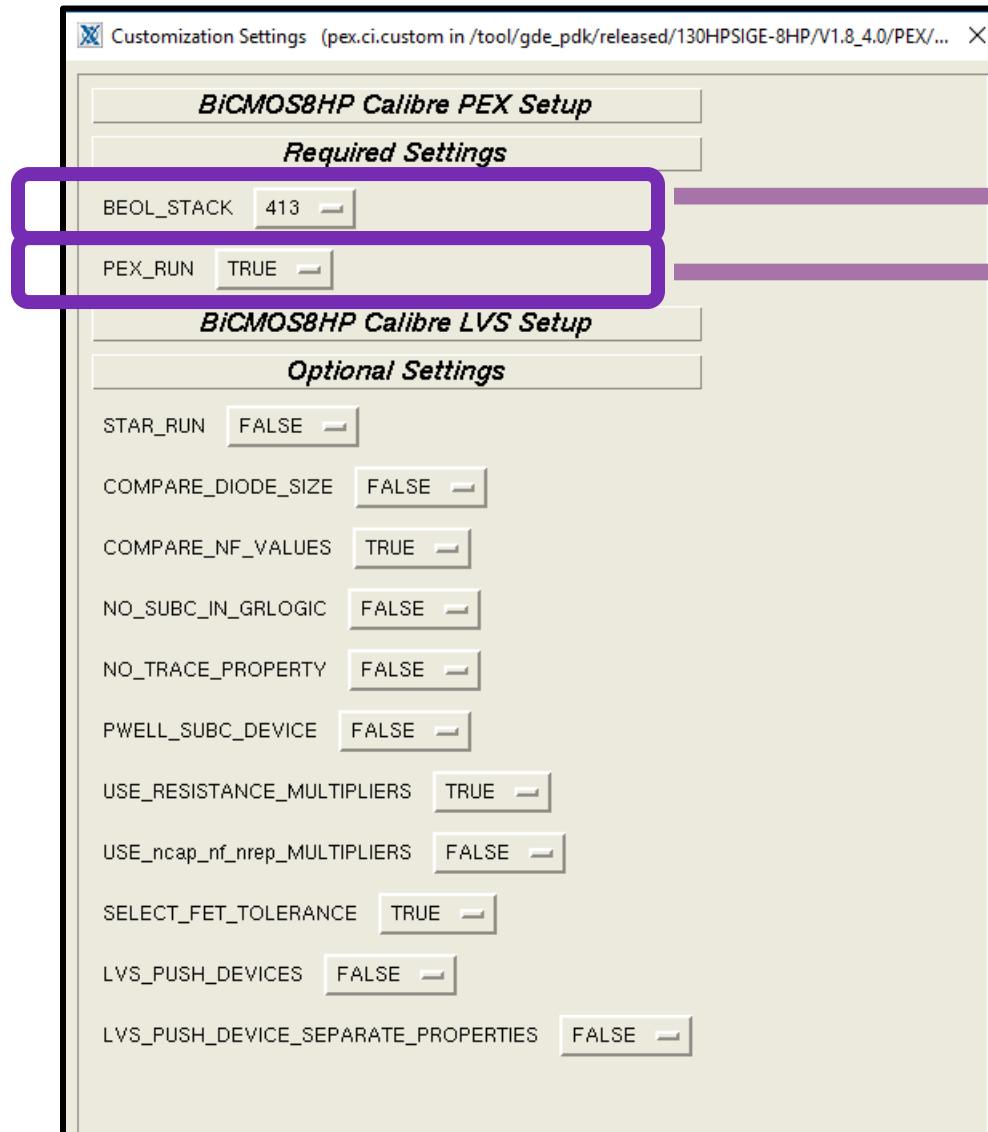
# Calibre xRC Overview

- Install Path: \$GF\_PDK\_HOME/PEX/xRC
- Cadence support through Calibre Interactive GUI and DFII output format
  - CALIBREVIEW with cellmap file
    - \$GF\_PDK\_HOME/PEX/xRC/calview/bicmos8hp\_calibre.cellmap
- Use CALIBREVIEW for re-simulation
- Request LVS operation (Calibre LVS)
  - PEX\_RUN=TRUE required for accurate fet parameters
  - PEX\_RULES : used to choose the proper rules file.

# Calibre xRC: Starting Calibre PEX from PDK (1)

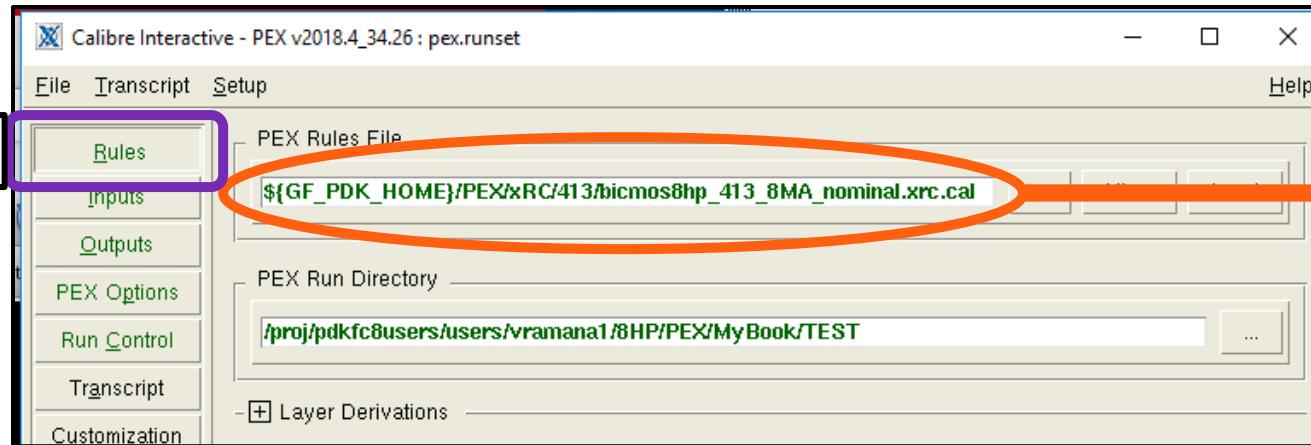


# Calibre xRC: Starting Calibre PEX from PDK (3)

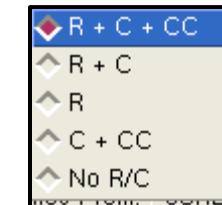
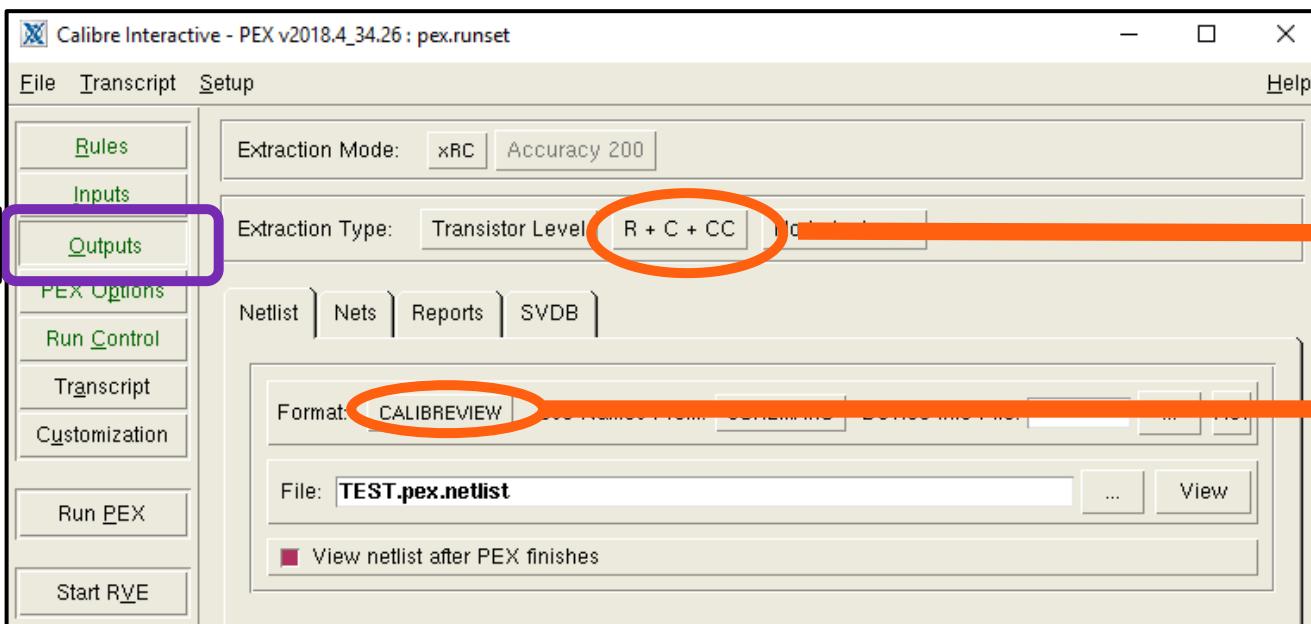


Choose the correct Metal Stack  
PEX\_RUN to be set to TRUE for  
accurate FET parameters

# Calibre xRC: Starting Calibre PEX from PDK (4)



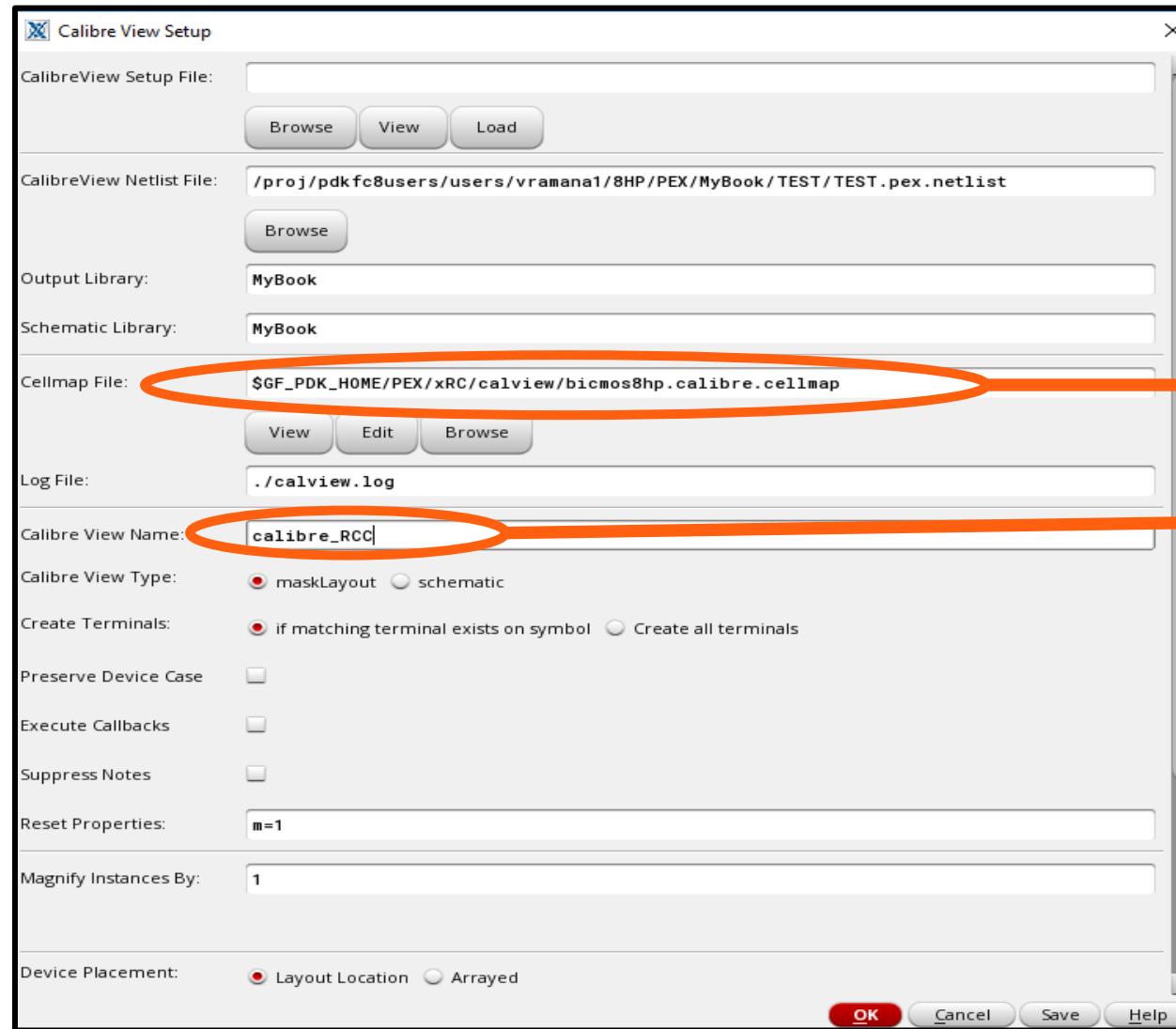
Make sure that the correct metal stack rule file is loaded



Choose the Transistor Level Extraction type

Choose from Calibreview, DSPEF, ELDO,Hspice, Spectre, SPEF

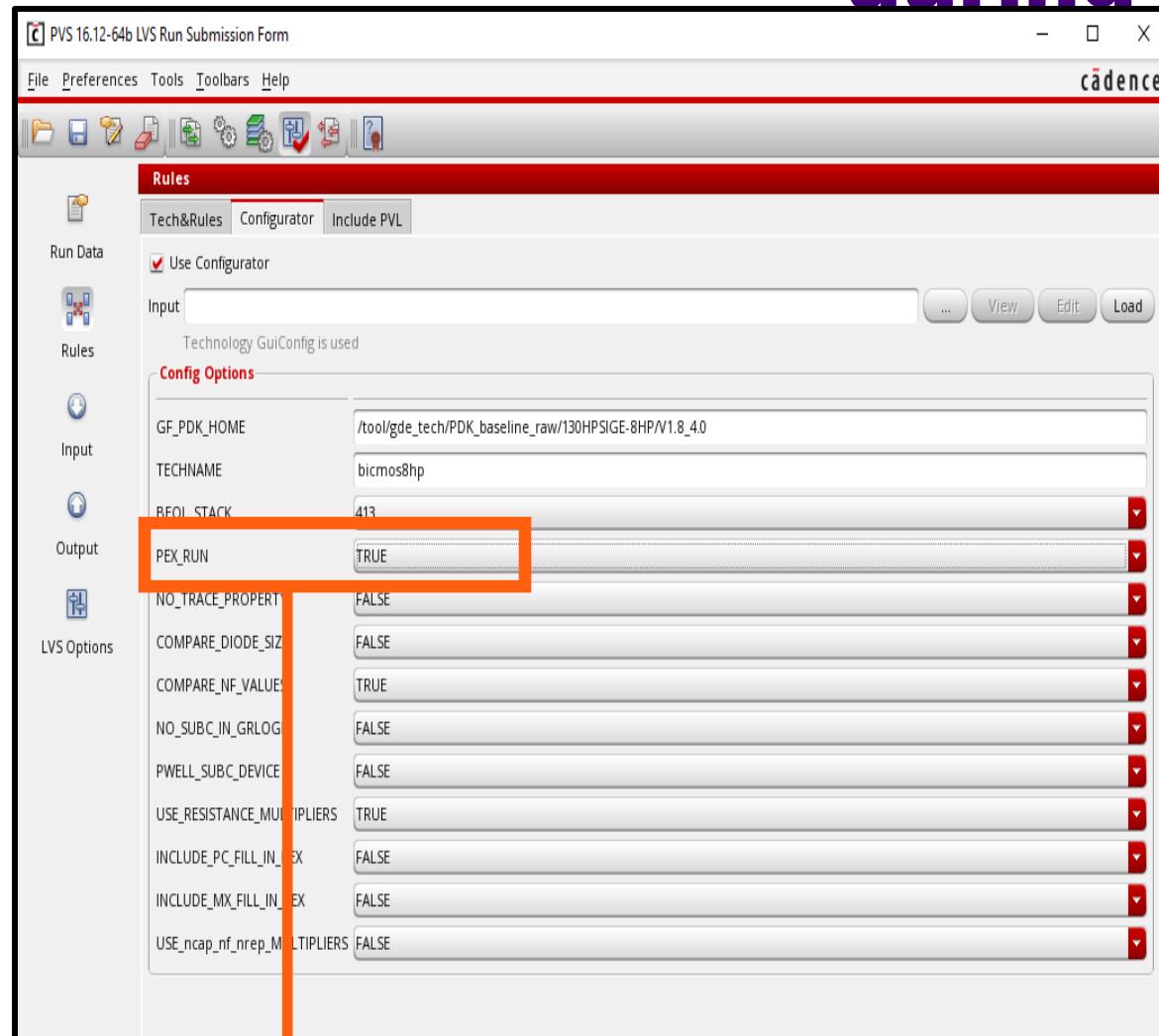
# Generating a Calibre View (DFII) Output Database from xRC



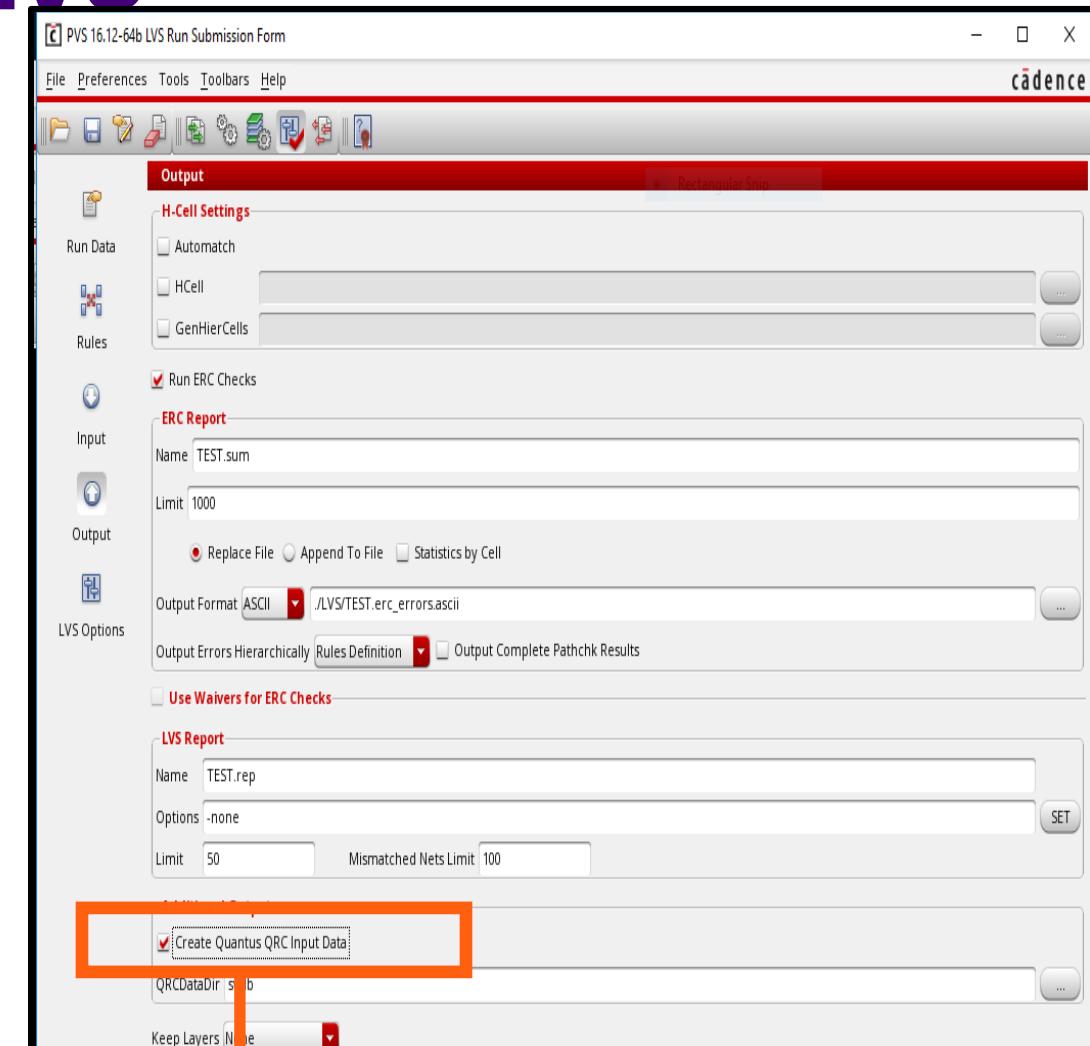
Specify the calibre cellmap file

Specify the Calibre View name

# PVS QRC Flow – Features to be checked ON during LVS



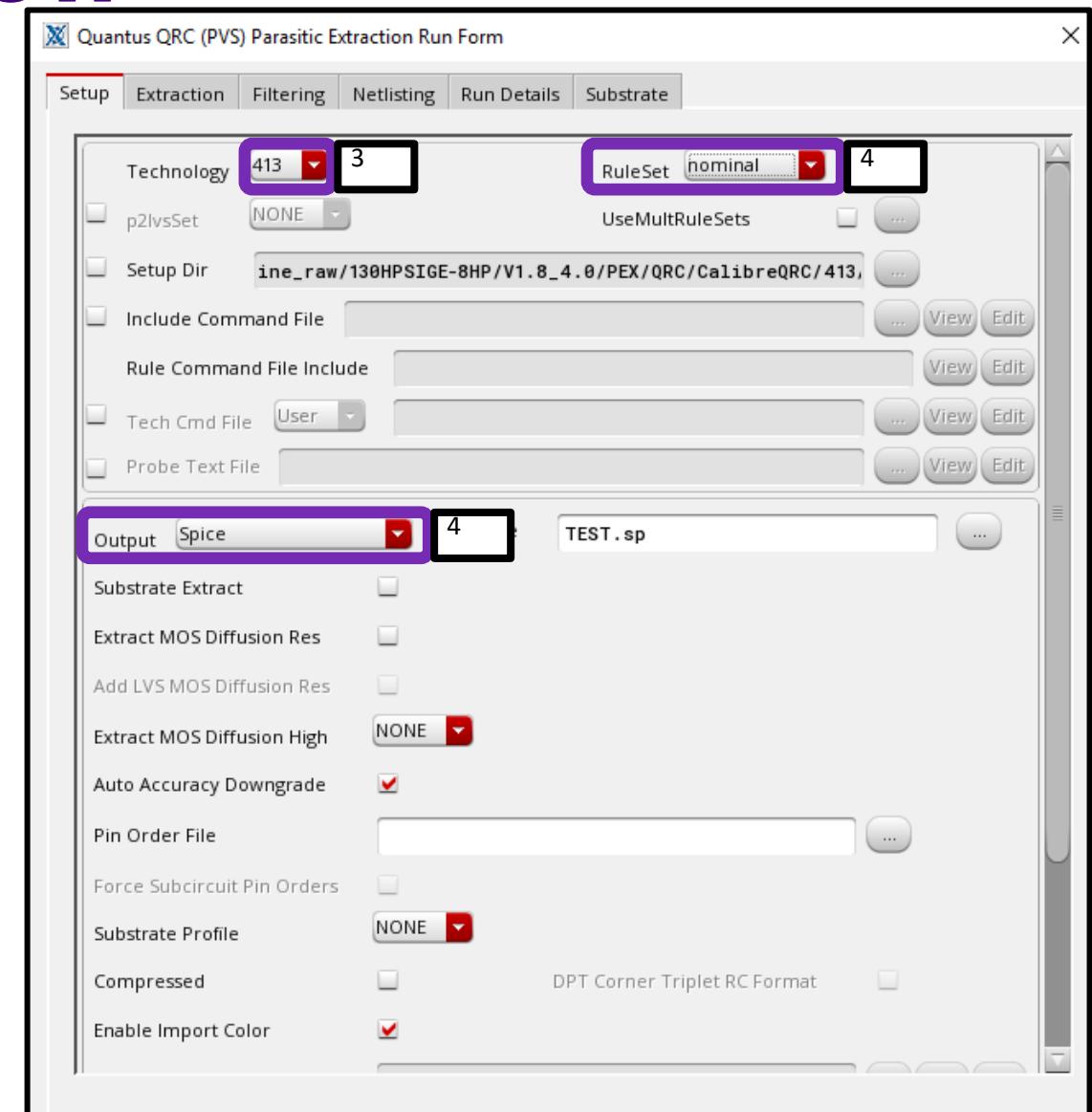
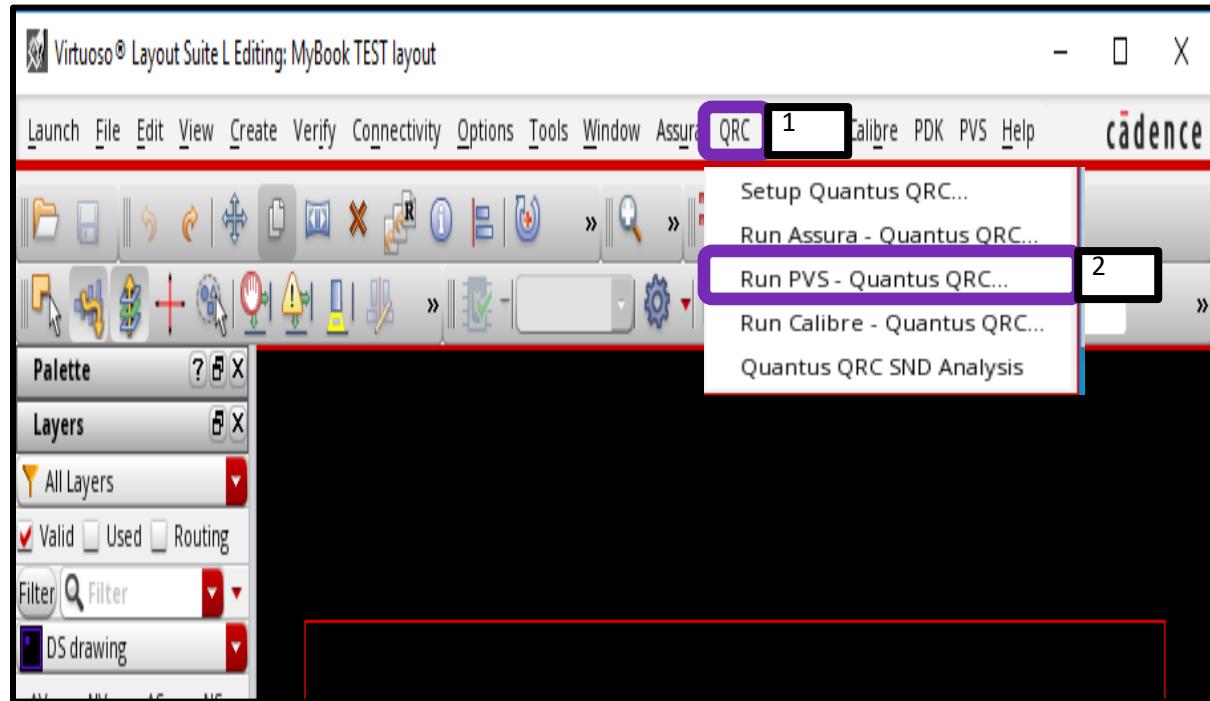
PEX\_RUN=TRUE



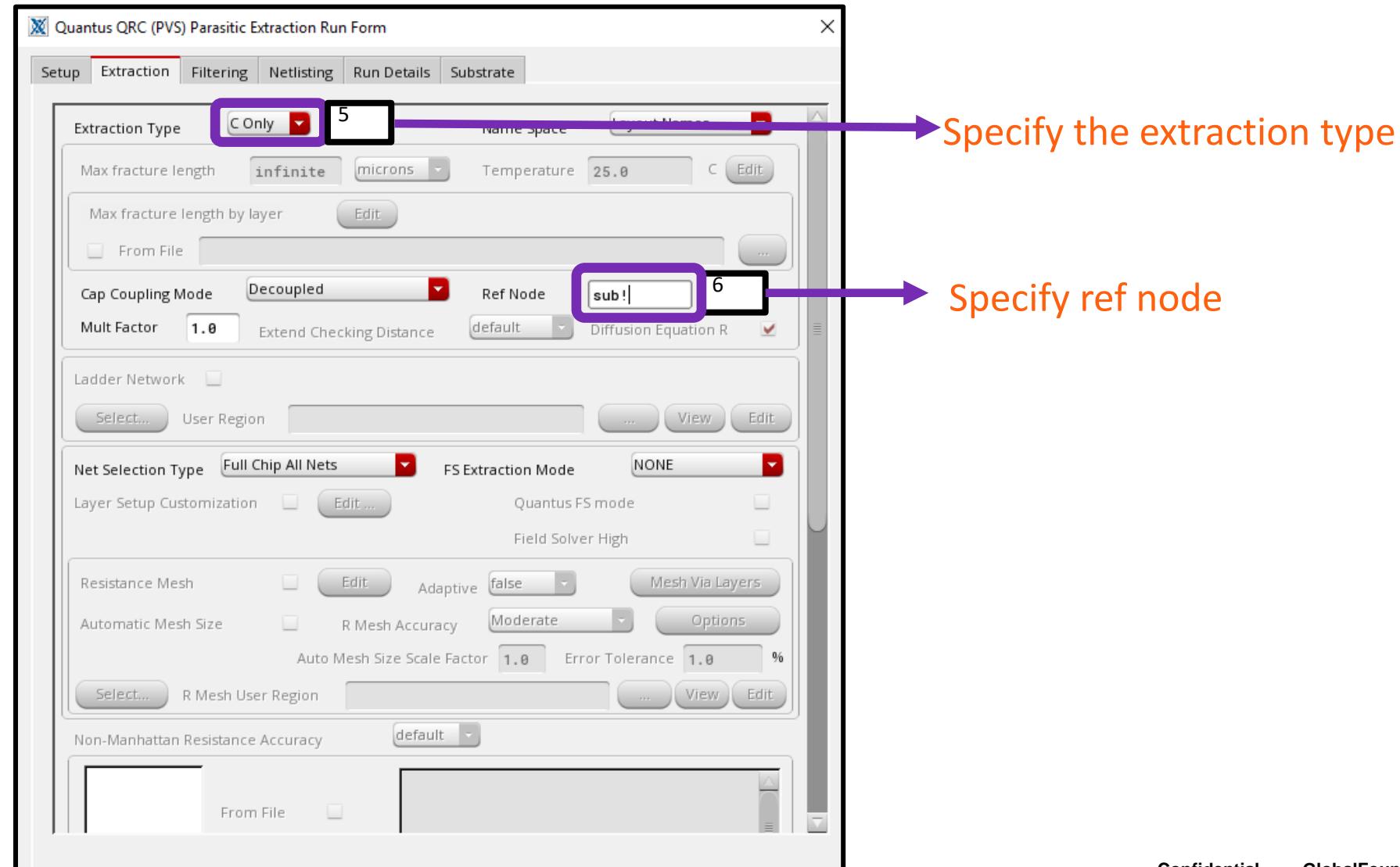
CHECK THIS BOX

# Running PVS- QRC Flow

Follow Steps 1 to 6



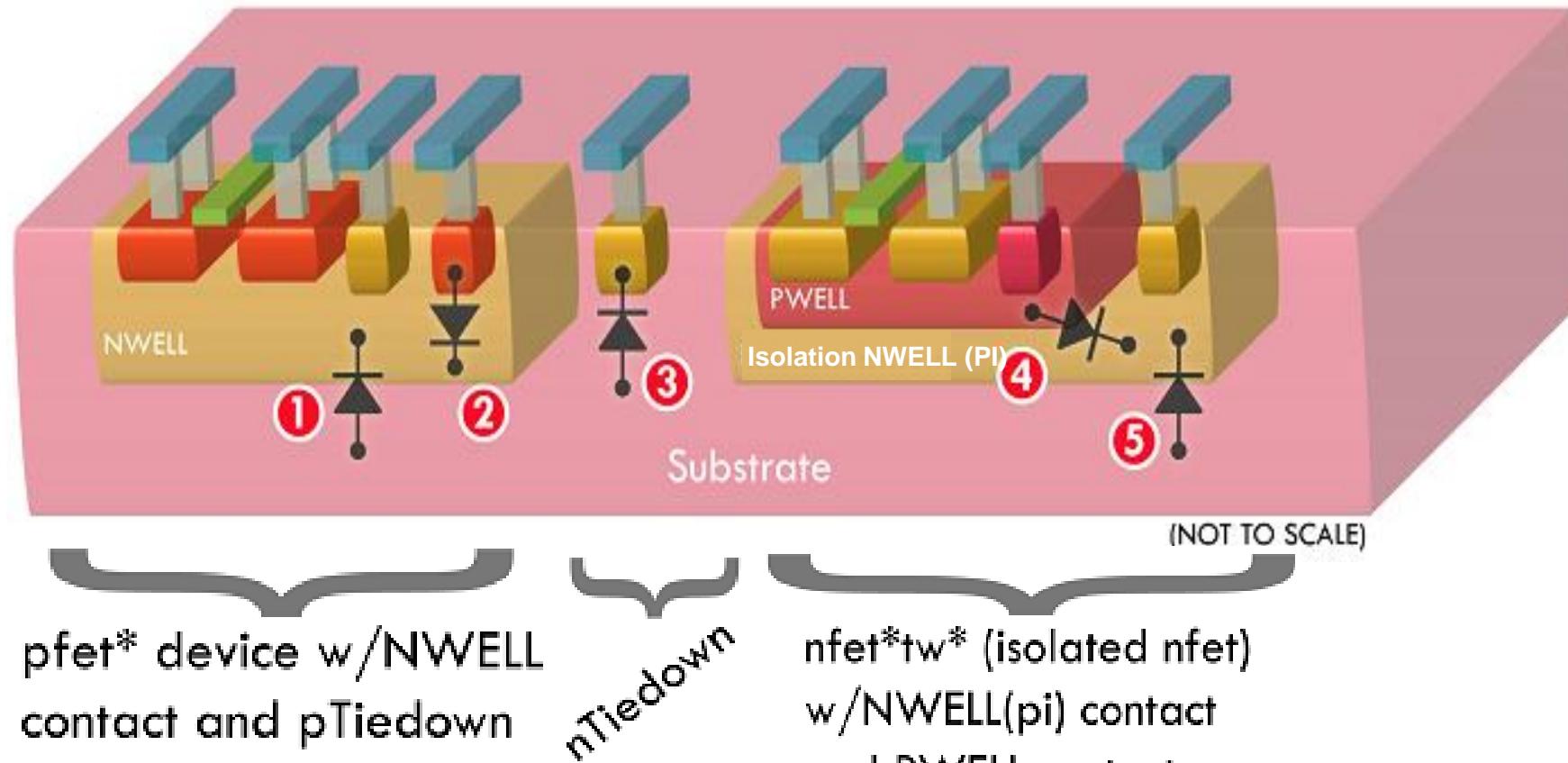
# PVS- QRC Flow (contd..)



# **BiCMOS8HP/BiCMOS8XP Parasitic Extraction: Special Topics**

- Parasitic Diodes
- MIM Bottom Plate Parasitics
- Bondpad Parasitic Modeling
- Parasitic Simulation Netlisting

# Parasitic Diode Extraction



- 1: NWELL to Substrate Junction;      2: P+-to-N WELL Junction (pTiedown);  
3: N+-to-Substrate Junction (nTiedown);    4: PWELL-to-NWELL(pi) Junction;  
5: NWELL(pi)-to-Substrate Junction.

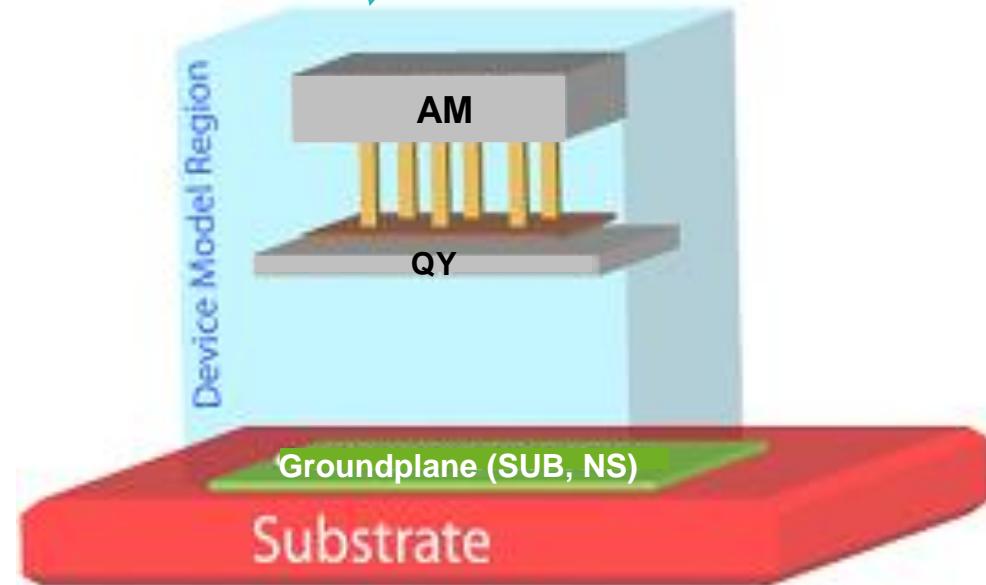
! Resimulate\_extracted switch

# MIM Bottom Plate Parasitic Modeling

## MIMcap schematic simulation assumptions:

- No routing or user layer placement beneath QY bottom plate
- Device model estimates bottom plate parasitic with model call parameter 'est' =1

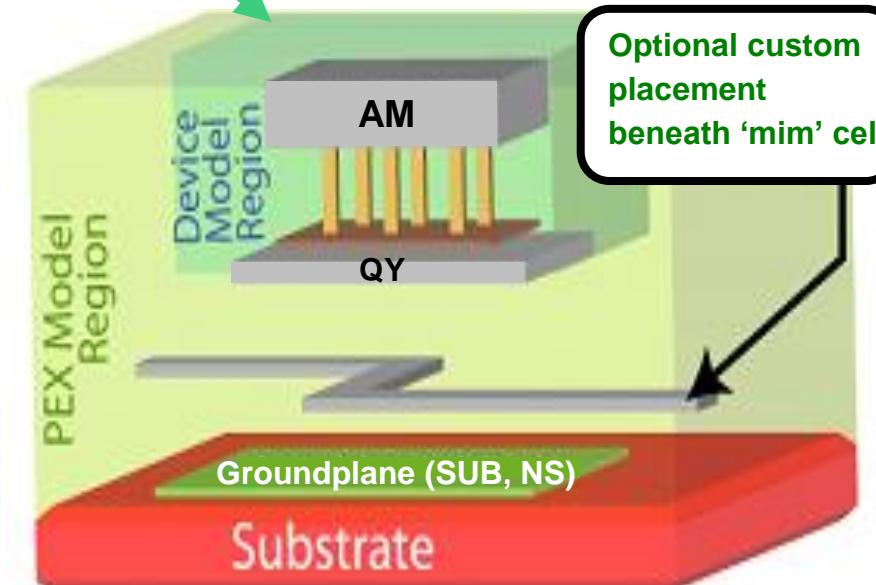
"CM0 (B T G) mim l=8.5u w=8.5u  
c=153.4505f m=1 est=1 tlev1=4 tlev2=1 ..."



## MIMcap post-layout simulation assumptions:

- Possible routine or user layer placement beneath QY bottom plate
- Device model does NOT estimate bottom plate parasitic ('est=0')
- Bottom plate parasitic must be modeled via parasitic extraction

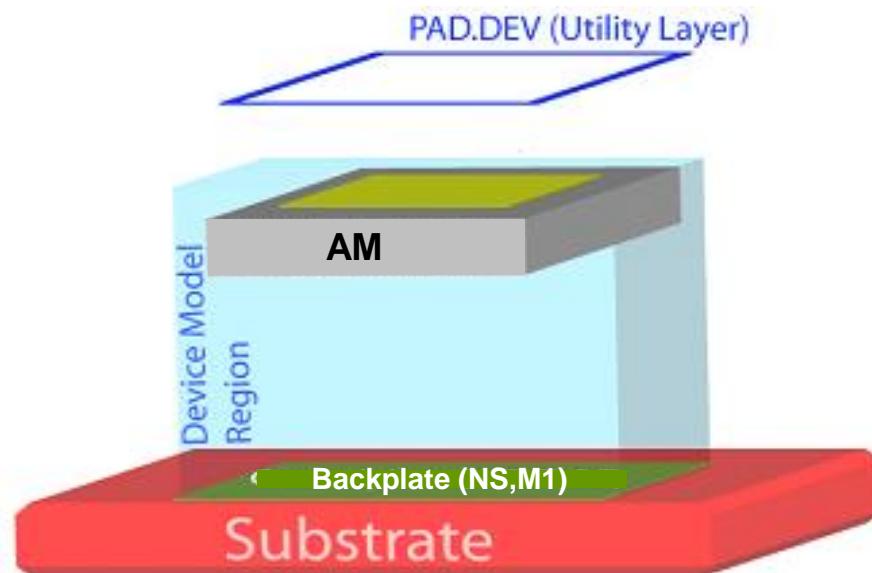
l+0 (B T G) mim l=8.5e-06 w=8.5e-06 c=1.5345e-13  
m=1 est=0 tlev1=4...  
l+5 (B G) capacitor c=6.171e-15  
l+3 (T G) capacitor c=2.227e-15



# “bondpad” Pcell vs. “Pad” Pcell Usage

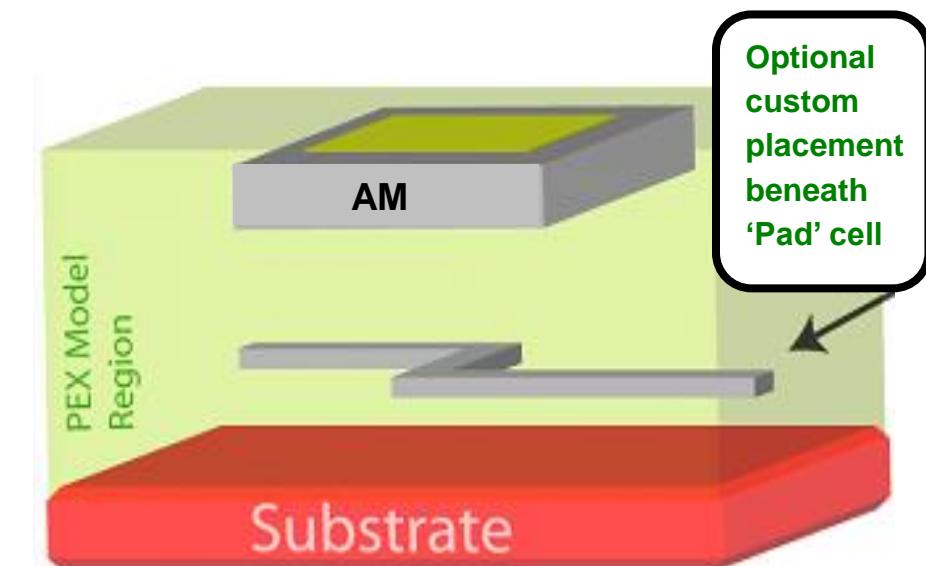
## “bondpad” Pcell: Layout Cell with Device Model

- Does not allow user shape placement under AM layer.
- (PAD.DEV) layer is used to identify modeled bondpad devices for DRC and device extraction purposes.

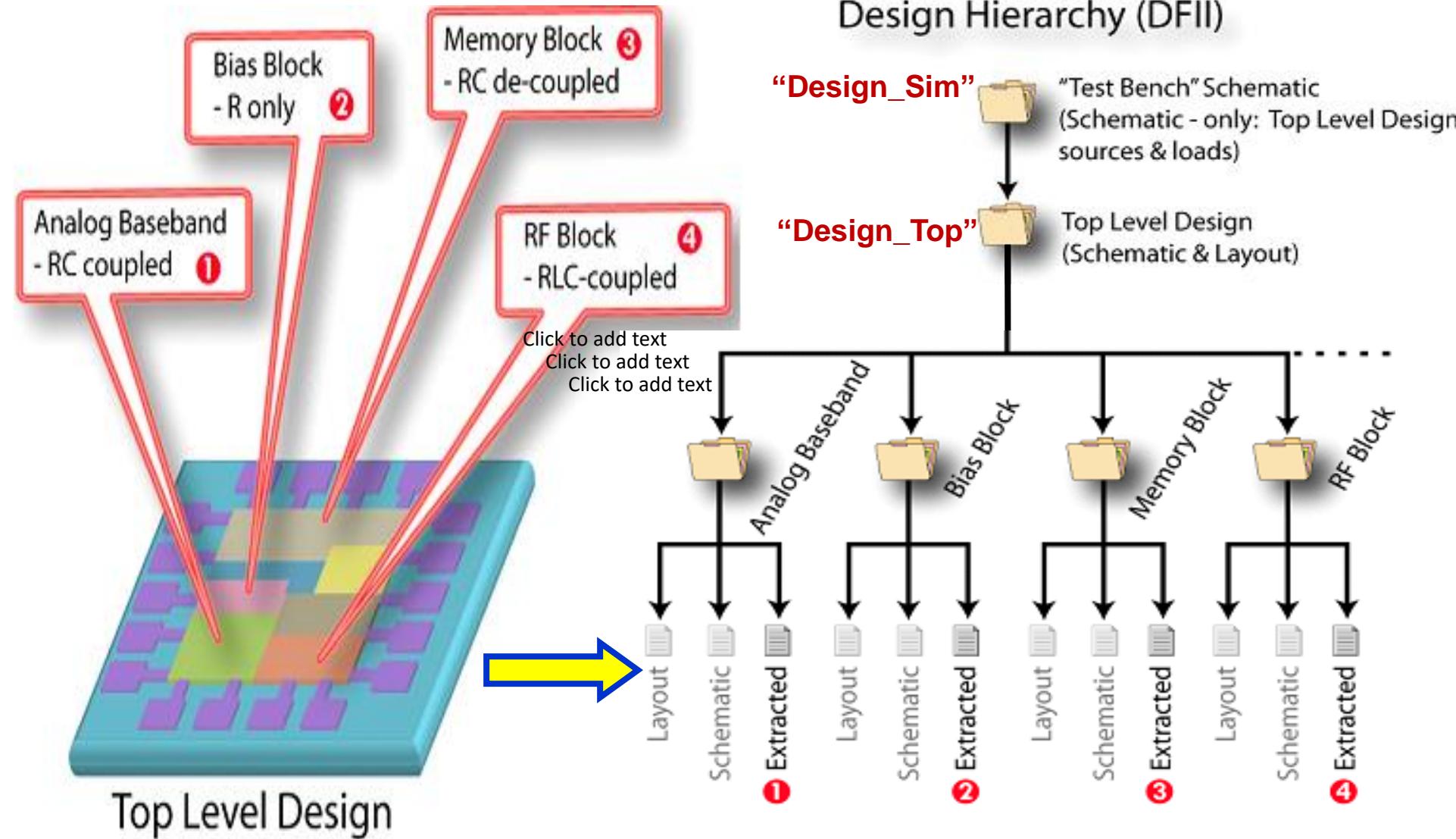


## “Pad” Pcell: Layout Cell Only (No Device Model)

- Does allow certain shape placement under Am layer.
- Pad modeled during parasitic extraction phase.



# Parasitic Re-Simulation: Simulating DFII Extracted views

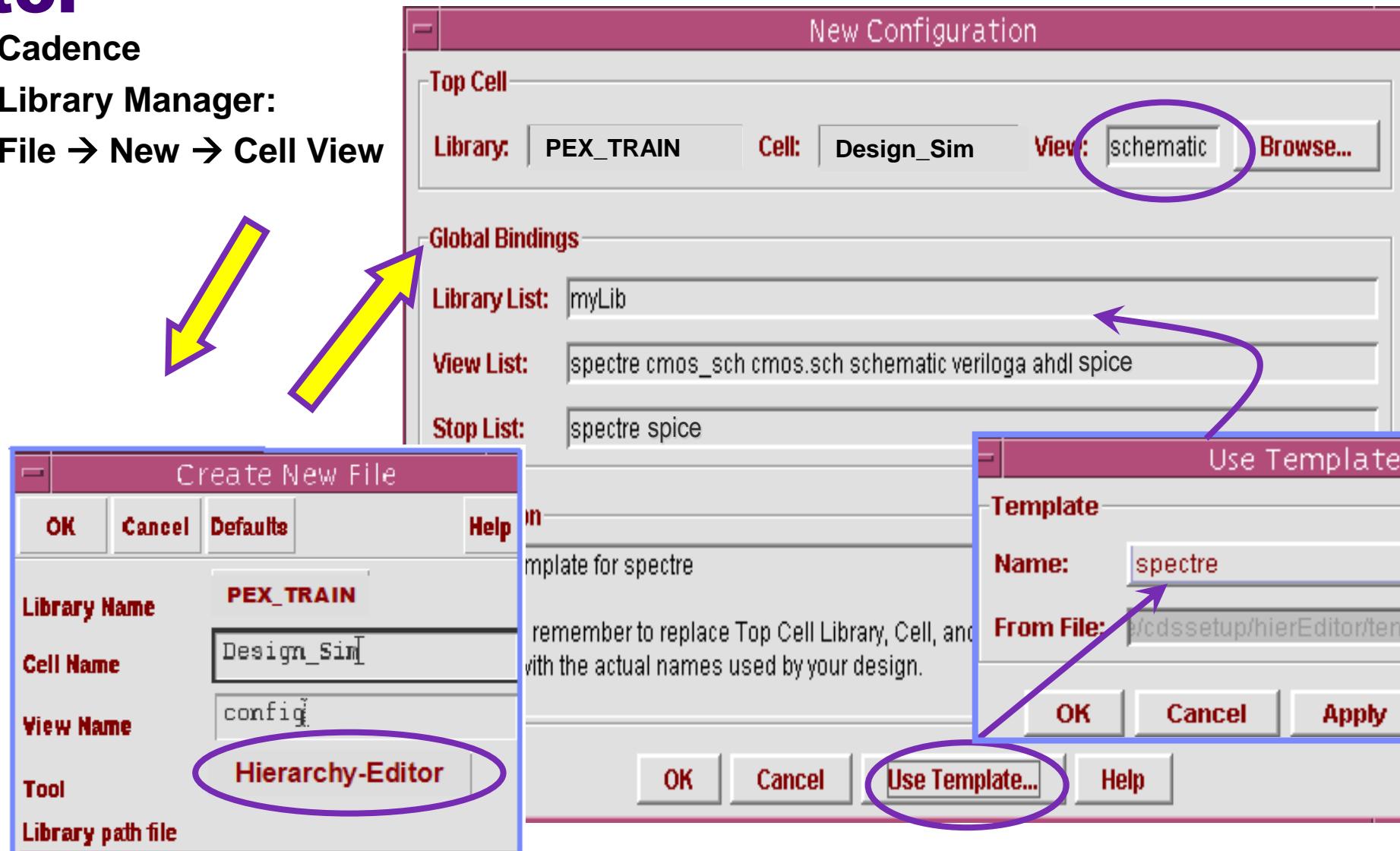


# Parasitic Re-Simulation: The Hierarchy Editor

Cadence

Library Manager:

File → New → Cell View



# Parasitic Re-Simulation: The Hierarchy Editor

File Edit View **Hierarchy Editor Form** Plug-Ins Help

Top Cell

Library: PEX\_TRAIN Cell: Design\_Si View: schematic

Global Bindings

Library List: PEX\_TRAIN

View List: spectre cmos\_sch cmos.sch schematic verilog

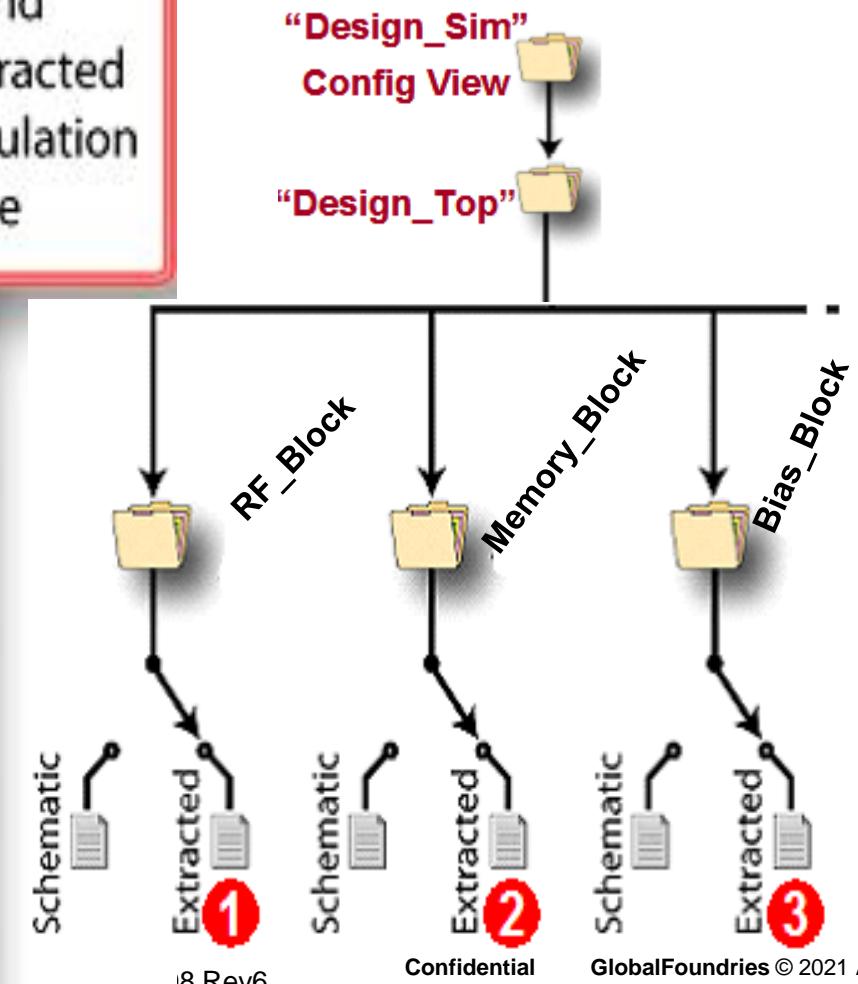
Stop List: spectre spice

Cell Bindings

Library	Cell	View Found	View to Use	Inherited VI...
PEX_T...	Bias_Block	extracted	extracted	③ spectre cmo...
PEX_T...	Design_Sim	schematic		spectre cmo...
PEX_T...	Design_Top	schematic		spectre cmo...
PEX_T...	Memory_Block	extracted	extracted	② spectre cmo...
PEX_T...	RF_Block	extracted	extracted	① spectre cmo...
analo...	presistor	spectre		spectre cmo...
analo...	vdc	spectre		spectre cmo...
bicmo...	diodenwx	spectre		spectre cmo...
bicmo...	nfetx	spectre		spectre cmo...
bicmo...	pcapc	spectre		spectre cmo...
bicmn...	nfetx	spectre		spectre cmo...

Select between schematic and parasitic extracted view for simulation netlist source

## Design Hierarchy (DFII)



# Version History

Version 1	All Sections as new	
Version 2	All Sections updated to the V1.5_0.0 PDK	June 15, 2017
Version 3	All Sections updated to the V1.8_4.0 PDK	October 7, 2019
Version 4	Fixed ADS Interoperable PDK simulation support pages	September 4, 2020
Version 6	All Sections updated to the V1.8_5.5 PDK	November 16, 2021



# Thank You



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