A 24-30GHz GaN-on-Si Variable Gain Low-noise Amplifier MMIC

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Abstract—This paper presents the design of a 24-30GHz variable gain low noise amplifier (VGLNA) with improved gain flatness for 5G millimeter-wave front-ends. Designed with a 100nm GaN-on-Si MMIC technology, the 3-stage VGLNA features with >20dB gain tuning range and ±0.5dB gain flatness over the operating frequency range. At the highest gain level, the noise figure (NF) of the LNA ranges from 0.89 dB and 1.25 dB, with the output and input return loss less than -10 dB. The average P_{1dB} in the whole band is around 14 dBm. The VGLNA chip occupies 1.5×0.8 mm², and dissipates 26mW to 361.5 mW DC power at various gain levels.

Index Terms—low noise amplifier, variable gain; GaN MMIC; millimeter-wave.

I. Introduction

With superior power handling capability and efficiency, the wide-bandgap GaN technology becomes prevalent in high-performance power amplifiers (PA). In the past decade, extensive studies have demonstrated that GaN monolithic microwave integrated circuit (MMIC) is a very promising PA solution for the upcoming 5G millimeter-wave (mmW) applications. It is foreseeable that the large-scale 5G mmW phased-array can benefit from monolithically integrated front-ends, which typically includes PA, LNA and antenna switches. Therefore, the researches on GaN-based LNA become popular [1].

The key advantages offered by GaN technology for LNA include robustness and linearity [2]. The traditional GaAs LNA based receiver usually requires a diode power limiter before the LNA to protect it from large incoming RF power. The limiter can be avoided in the highly rugged and linear GaN LNAs, which extends the dynamic range of the receiver and possibly lower the NF. Actually, the noise performance of GaN LNA is not inferior to the widely used GaAs counterpart. As technology advances, the state-of-the-art GaN LNA shows comparable NF to the best GaAs LNAs at Ka band and beyond with better linearity [3-4].

While most of the present GaN LNAs are based on SiC substrate, the GaN-on-Si MMIC technology is exhibiting great potential for mmW applications. Although with higher substrate loss and lower thermal dissipation capability, the GaN-on-silicon technology has much lower substrate cost and larger substrate size. Thus, it can be more cost effective for commercial products. Recent study has demonstrated that GaN-on-Si LNA can achieve similar NF performance as the state-of-the-art GaN-on-SiC LNAs [5].

As the signal strength received by the receiver may vary significantly, a VGLNA can effectively prevent the next-stage circuit from saturation. Saturation could easily occur when the following stages adopt silicon-based technologies, i.e. CMOS, which normally show worse linearity than III-V semiconductors, like GaN. More importantly, VGLNA can reduce the power consumption by using the low gain mode in certain scenario. Besides, using a VGLNA in the front-end can further extend the dynamic range of the receiver. VGLNA designs have been reported in GaAs technology at X band or below [6-8], but still rare in GaN or at higher frequency bands. In this paper, we propose a Ka-band GaN-on-Si VGLNA. An optimized RC feedback is adopted to minimize the gain fluctuation throughout the gain tuning range. The designed VGLNA achieves less a gain flatness than 1dB over 24-30 GHz while maintains a low NF around 1.1 dB, which is well suitable for 5G mmW applications (i.e. Band n257 and n258).

II. VGLNA MMIC Design

A. The design of GaN LNA circuit

The schematic of the overall VGLNA proposed in this paper is shown in Fig. 1. It applies three amplified stages for the purpose of enough gain. The first and the second stages adopt the simple common-source (CS) structure to achieve low input VSWR, low noise figure and high gain.

For the first stage, which dominates the overall NF of the entire LNA, the source degeneration feedback topology is used as it typically exhibits a well noise performance. the input impedance of the first stage Z_{in} can be expressed as (1). Inductive reactance L_s in the source lead of the HEMT M_1 increases the real part of the input impedance. (2) shows that the value of L_s and the inductive reactance L_G in the gate lead is determined by the required NF. With proper impedance loading at the output of the HEMT, the input impedance of the M_1 and the optimum noise match impedance become compatible.

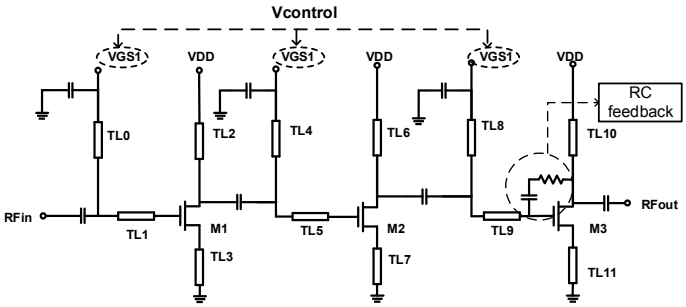

Fig. 1. The schematic of the VGLNA.

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TABLE I
COMPARISON WITH STATE-OF-THE-ART KA-BAND LNA MMIC

Work	Process	Freq. [GHz]	Gain [dB]	NF [dB]	Gain Flatness [dB]	S11/S22 [dB]	P1dB [dBm]	OIP3 [dBm]	Size [mm]
[4]	GaAs	26 – 33	33	1.8-1.6	0.7	<-12	--	--	1.3 x 2.8
[5]	GaN	18-31	>20	>1.43	--	<-10	16	--	2.3×1.0
[3]	GaN	30-39.3	10	1.9-2.2	>2*	S22<-10	--	5-20	3.115×1.12
[2]	GaN	27.5-28.5	21	<2.7	>2*	S22<-10	>12.5	--	3x2
This work	GaN	24-30	**21-22**	0.89-1.25	**<0.5**	<-10	14	**>28**	**1.5×0.8**
			10-11	<2.3	**<1**	<-10	15	**20**	
			0	<5.9	**<1**	S22<-10	15	**20**	

(*: the data was estimated by observation, --: the data was not provided)

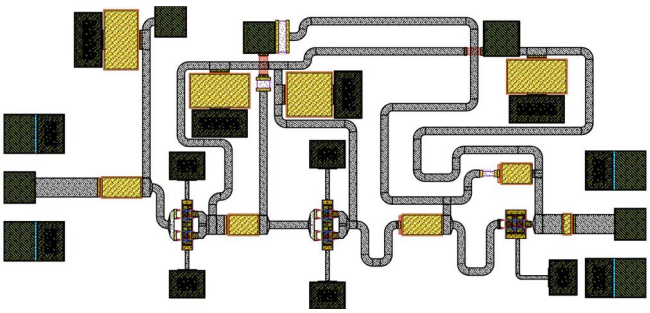

Fig. 2. The layout of the VGLNA MMIC.

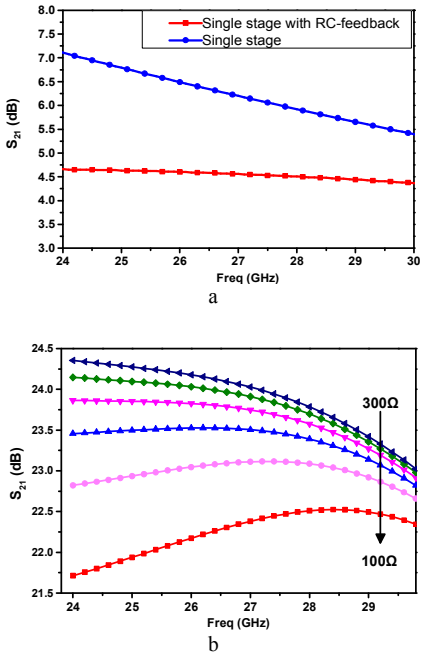

Fig. 3. Simulated difference in gain of amplifier circuit at V_{DS}=3.5 V.a. gain of amplifier circuit with or without RC negative feedback.b. gain comparison among different value of resistor.

$$Z_{in} = s(L_G + L_S) + \frac{1}{sC_{GS}} + g_{m1}\frac{L_S}{C_{GS}} \quad (1)$$

$$NF = 1 + \gamma\frac{4(g_m L_S)^2}{R_S g_m}\frac{1}{C_{GS}(L_G + L_S)} \quad (2)$$

where L_G and L_S are the gate and source inductances respectively which are replaced by the microstrip line, C_{GS} is the gate-source parasitic capacitance.

In the first two stages, a 4×25 μm HEMT is selected for the low noise figure and high gain performance but it will deteriorate stability. The bias voltage of the HEMT is suitable for V_{GS}=-0.8V and V_{DS} =3.5V where the transconductance of the 4×25 μm HEMT peaks.

The third stage adopts the resistance negative feedback topology as shown in the Fig.1, which compensates for the gain partially sacrificed for the gain flatness characteristic. The disadvantage of adopting negative feedback is that the noise figure of this stage is deteriorated and it occupies more chip area. However, under the high gain of the first two stages, the NF of the overall circuit increases little.

B. Gain-control with improved gain flatness

Fig.3 illustrates the effect of the resistance negative feedback on the gain of LNA. The comparison of the gain curves in Fig.3 (a) shows that the overall gain at 30 GHz of amplifier circuit without feedback drops 2.5 dB after amplified by the first two stages, but the ripple of the improved circuit is compensated by the last stage. The value of resistance determines the degree of negative feedback as shown in the Fig.3 (b). The proper negative feedback will improve the return loss of the device and eliminates the roll-off of the gain over the gain control.

Various techniques have been reported to achieve gain control in the VGLNA design [6-9]. In this work, the circuit adopts the biasing technique which is known for its wide range of power adjustment with low DC power dissipation and simple topology [10]. The biasing technique is favorable especially for low-noise amplifiers as the noise generated by the gain-control transistors has a relatively lower effect on the overall linearity and gain flatness compared to other approaches.

There are two bias controlling methods to vary the gain, changing the value of V_{GS} or V_{DS}. However, compared with changing the V_{DS}, controlling V_{GS} can maintain good output matching over the gain control. In this design, a unified control of the gate voltage of the overall circuit is adopted, in order to

reduce power consumption and realize well inter stage matching. It can be found that the overall gain reduces from 20 dB to 0 dB by adjusting the V_{GS} from -0.8V to -1.4V.

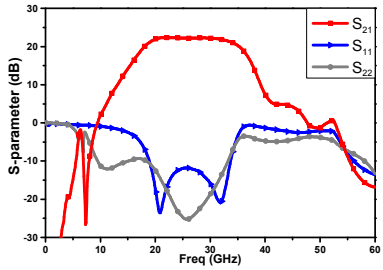

Fig.4. Simulated small-signal gain, input and output return loss of the VGLNA at highest gain level.

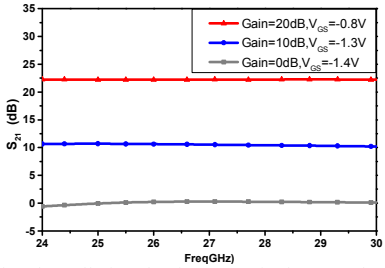

Fig.5. Simulated small-signal gain respectively at 20 dB, 10 dB, 0 dB.

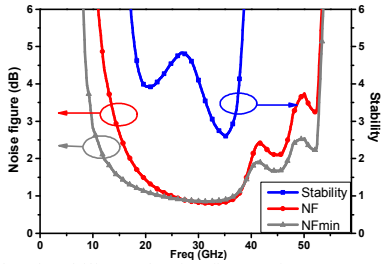

Fig. 6. Simulated stability and noise figure of VGLNA MMIC at 20 dB.

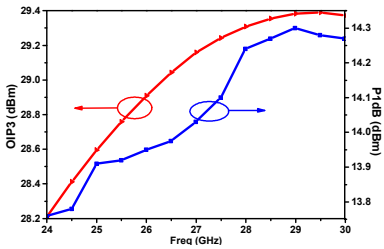

Fig. 7. Simulated P_{1dB} and OIP_3 of VGLNA MMIC at 20 dB.

Fig. 4 shows the post-layout simulation results of the VGLNA. When the gain is greater than 20 dB, the input and output return losses are less than -10 dB over 18-32 GHz. The ripple of the gain can be limited to 0.5 dB at highest gain level.

Fig. 5 shows the small signal gain at different gate biases. The ripple of the gain in each grade is almost less than 1 dB.

Fig. 6 illustrates the stability and noise of the circuit when the small signal gain is 20 dB. It indicates that the circuit is unconditionally stable over the 0-60 GHz frequency range. The VGLNA achieves a very ultra-low NF of 0.89 dB at 30 GHz, while the NF over the 24-30 GHz is maintained below 1.25 dB.

Due to the high breakdown electric field of GaN technology, an obviously high P_{1dB} and OIP_3 was achieved, as shown in Fig. 7, P_{1dB} and OIP_3 are greater than 14 dBm and 20 dBm in each gain state. Table I compares this work with other Ka-band LNAs. It verifies the excellent gain flatness achieved by out design. Besides, in terms of chip size, our VGLNA is also a very compact design.

III. Conclusion

In this paper, a broadband GaN-on-Si VGLNA is reported, demonstrating a 20 dB maximum gain and an average NF of about 1.1 dB over 24-30 GHz. The gain of the VGLNA can be tuned by V_{GS} from 0 to 20 dB and the ripple at different gain level is maintained below 1 dB, which is among the best performed VGLNAs at mmW bands. The proposed GaN VGLNA on silicon substrate still maintains a good linearity (P_{1dB} >14 dBm, OIP_3>20 dBm), which is comparable to the those on SiC substrates.

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