A 65nm CMOS 6-18 GHz Full 360° 6-bit Phase Shifter

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***Abstract* — A unique full 360° vector-sum phase shifter is presented and demonstrated in this paper. To eliminate the phase error caused by the variation of bias current of VGA, the phase shifter employs a new VGA that adjusts amplitude by selecting different sub-gm cells of I- and Q-paths, which results in a very low RMS phase error. The measured RMS phase error is < 1.1° between 7-17 GHz and < 1.8° between 6-18 GHz, and the RMS gain error is < 0.55 dB between 6-18 GHz. The core chip size is 0.52×0.78 mm^2 with a total current of 36 mA, from a 1.2 V supply voltage.**

***Index Terms* — Active circuits, MMICs, phased arrays, phase shifters, wideband.**

I. Introduction

Phased arrays can provide fast beam forming and suppress the interferences from different directions which leads to better SNR and higher channel capacity [1]. So as an indispensable part, phase arrays are becoming more and more popular with the continuous development of 5G communication. And it is necessary to fabricate them by CMOS technology to lower the cost and scale. Phase shifters, the most important elements in phase arrays, have been researched for decades. Various techniques such as switched transmission lines, high-pass/low-pass networks, all pass networks, and vector summation have been developed to improve the resolution of phase shifters [2]. In this paper, we employ vector summation to implement a full-360° 6-bit phase shifter in 65 nm CMOS technology.

In vector sum phase shifter, an in-phase/quadrature network is used to generate I/Q signals, and the output phase is synthesized by adding the I/Q signals with proper amplitude weightings and polarities. VGAs that can adjust amplitudes precisely are therefore quiet necessary. Most vector sum phase shifters employ Gilbert-cell type VGAs to add the I/Q signals and adjust the amplitudes by monitoring the bias current of the VGAs [3]. However, the accuracy of amplitude controlling is limited due to the nonlinearity of the MOSFETs, and thus results in a bad RMS phase error. Besides, it is not an easy task to accurately generate the required variable bias currents when the phase resolution of the phase shifter becomes high since the variation range of current is huge.

To solve the above problems, we proposed a unique phase shifter which adjusts the I/Q amplitudes by selecting different sub-gm cells . Working in this way, the linearity of transistors is no longer a restriction since the bias current of each sub-gm cells is invariable when it is selected to work. And as various bias current is not needed any more, it becomes much easier to design the phase shifter. For verification, a 6-bit 6-18 GHz phase shifter in 65 nm COMS technology using the above technique is designed and tested.

II. Circuit Design

The architecture of the proposed 6-bit phase shifter is shown as Fig. 1. At the beginning, it adopts an I/Q network to precisely split the input signal into in-phase and quadrature vector signals over a wide bandwidth. Since the accuracy of output phase heavily depends on the precision of the I/Q signals, a three-stage poly phase filter (PPF) is used here as I/Q network because it can work stably over a wide bandwidth even with the variation of the process. Besides, an optimal layout technology for the three stage PPF is used to further improve the accuracy of the I/Q signals [4]. However, the large insertion loss introduced by the PPF makes the phase shifter presented a low gain.

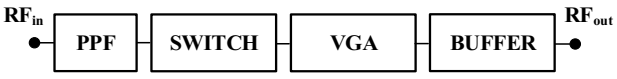

Fig. 1. The proposed phase shifter architecture

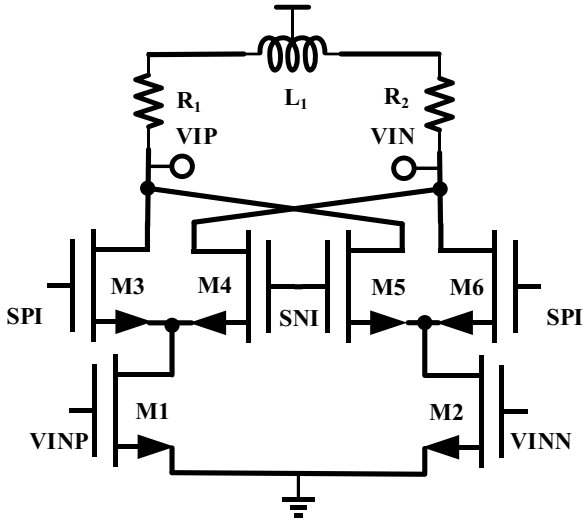

Fig. 2. The circuit of the switch

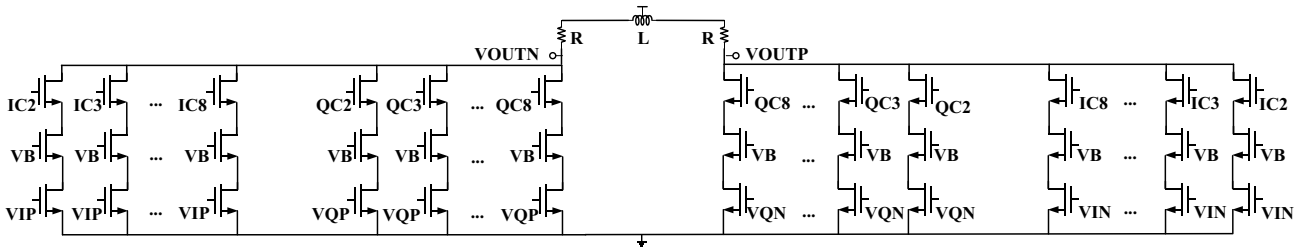

Fig. 3. The circuit of the VGA

As the phase shifter is designed to achieve a full-360° phase shift, and the VGA can only control the phase shift in one quadrant, a switch shown as Fig. 2 is employed to extend the phase shift to the four quadrants by changing the polarities of the I/Q signals. An additional benefit that comes with the switch is that as an amplifier, it also compensates part of the loss caused by the PPF.

Fig. 3 shows the VGA used in the phase shifter, where the VIP, VIN, VQP and VQN are the inputs that are connected to the outputs of switches. As mentioned earlier, the VGA selects different sub-gm cells of the I- and Q-paths to work respectively through the switch transistors to adjust the amplitudes. And it adds the I/Q signals in the current domain at the output to synthesize the required signal. A 6-bit phase shifter has 64 phase states in general, 16 phase states in each quadrant. According to $\tan(\pi/2-\theta)=1/\tan(\theta)$, only 8 phase states in the range of 0°~45° need to be realized through sub-gm cells, and the other 8 phase states can be got by exchanging the on and off states of the switch transistors of the I- and Q-paths. The needed A_I and A_Q to implement 8 phase states can be calculated through the Equation

$$\tan\theta_{out}=\frac{A_I}{A_Q} \tag{1}$$

and

$$A_I^2+A_Q^2=K, \tag{2}$$

where θ_{out} is the desired phase, A_I and A_Q are the gain of the I-path and Q-path respectively, K is a constant. Then the number of the sub-gm cells and their scaling factors which realize these required gains can be decided. In this paper, each signal path adopts 6 sub-gm cells and the scaling factor is designed as 2:3:4:6:8:8. For example, to achieve the phase state of 22.5°, the sub-gm cells with weights of 3, 8 of I path and 4, 6, 8, 8 of Q path can be chosen to work.

Finally, the output buffer composed of a differential common source amplifier and two source followers is used.

III. MEASUREMENTS

The 6-bit phase shifter is designed and fabricated in 65 nm CMOS technology. And the microphotograph of the phase shifter is presented in Fig. 4. The chip is measured on Cascade Summit 12000M probe station with GSGSG probes using an Agilent N5242A Vector Network Analyzer.

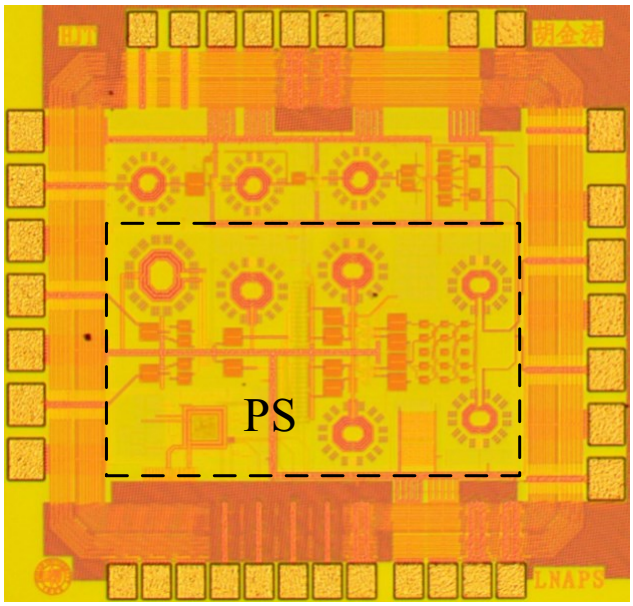

Fig. 4. The microphotograph of the phase shifter (in the dashed-line area)

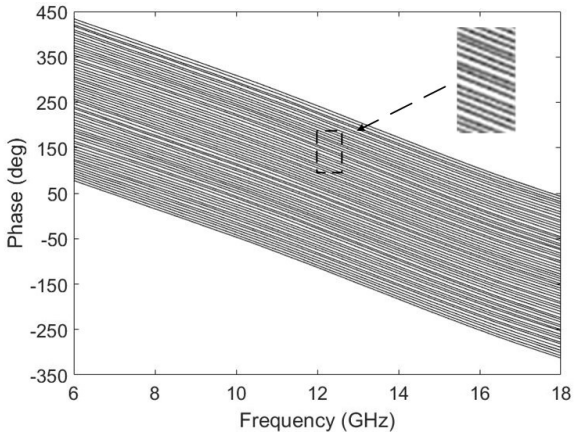

Fig. 5. Measured unwrapped insertion phase

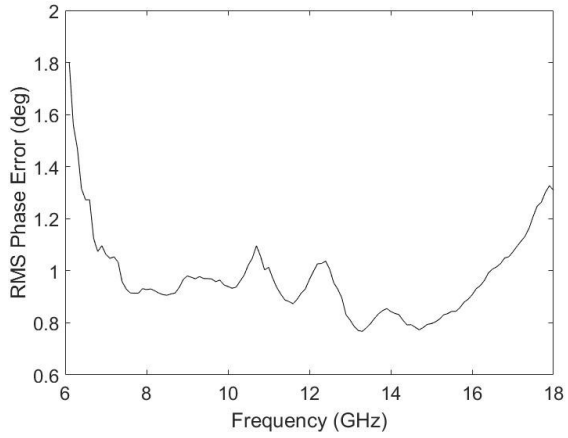

Fig. 6. RMS phase error

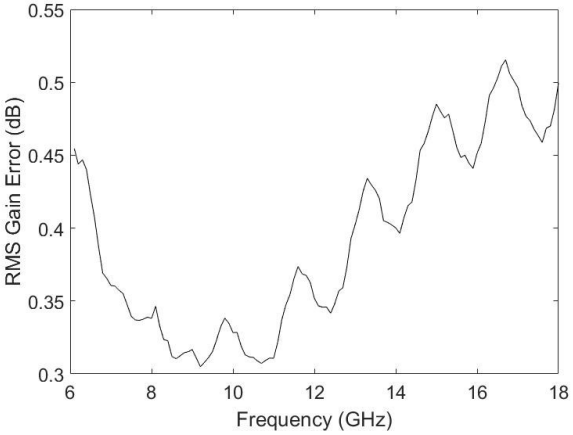

Fig. 7. RMS gain error

The measured unwrapped insertion phase versus frequency for all 64 phase states is shown as Fig. 5. With reference to 0°, Fig. 6 and Fig. 7 show the RMS phase error and RMS gain error of the phase shifter which are calculated from the measurement results by means of the method proposed in [5]. Over the requested 6-18 GHz band, the RMS phase error is below 1.8° over and the RMS gain error is less than 0.55 dB. The peak gain is -10dB, and the gain variation is within $\pm$5 dB. And the measured input-referred 1-dB compression point is 0 dBm. The performance summary and comparison with other works is shown in Table I.

IV. CONCLUSION

In this work, a unique full 360° variable 6-bit phase shifter based on the vector-sum technique is demonstrated with very low RMS phase error and RMS gain error over a wide bandwidth. In this phase shifter, a method is proposed to adjusts I/Q signals by enabling different sub-gm cells, which improves the phase shift accuracy significantly. It is known from the measurement results that RMS phase error remains lower than 1.8° from 6 GHz to 18 GHz, and the RMS gain error is less 0.55 dB, thereby validating the approach.

TABLE I PERFORMANCE COMPARISON

	Technology	Freq (GHz)	RMS phase error(°)	RMS gain error(dB)
[1]2016 MTT	250 nm BiCMOS	8-11	<6	<1.5
[2]2016 MTT	130 nm CMOS	4.9-5.9	<9.7	<0.7
[5]2012 MTT	180 nm CMOS	2.3-4.8	<1.4	<1.1
[6]2015 CICC	65 nm CMOS	2-20	<1.22	<1.5
This work	65 nm CMOS	6-18	<1.8	<0.55

ACKNOWLEDGEMENT

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