



Chapter 6

Frequency Response of

Amplifiers

中科大微电子学院

黄 鲁

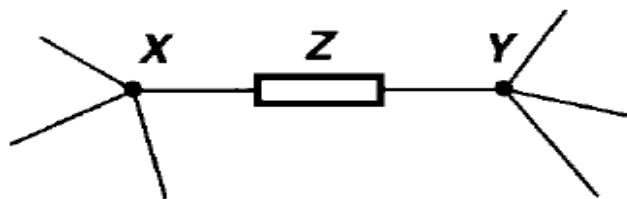
教材：模拟CMOS集成电路设计

Behzad Razavi



6.1 general considerations

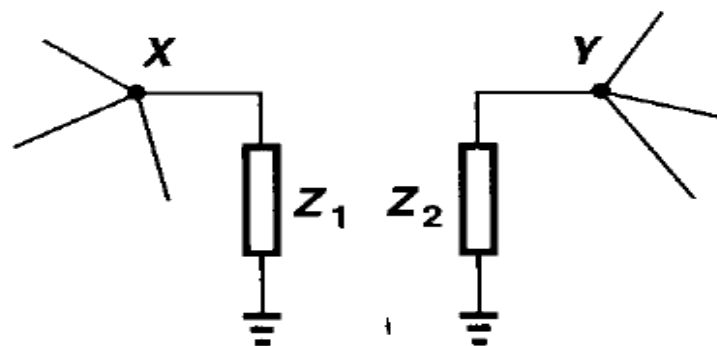
6.1.1 Miller Effect



输入、输出阻抗？

(a)

Miller's theorem



(b)

Figure 6.1 Application of Miller effect to a floating impedance.

- 设X和Y之间增益= V_Y/V_X ，由另一条支路提供

$$\frac{V_X - V_Y}{Z} = \frac{V_X}{Z_1}, \quad \frac{V_Y - V_X}{Z} = \frac{V_Y}{Z_2}$$

得 $Z_1 = \frac{Z}{1 - \frac{V_Y}{V_X}}$, $Z_2 = \frac{Z}{1 - \frac{V_X}{V_Y}}$, 注意 $\frac{V_Y}{V_X}$ 为增益，正常为负

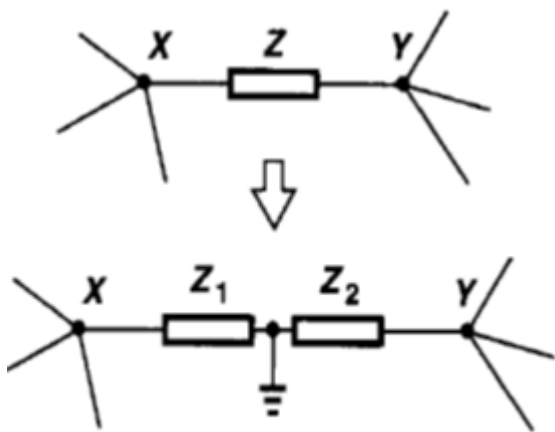
输入阻抗变小，一般不好



Miller effect (cont.)

于是 $\frac{Z_1}{Z} = \frac{V_X}{V_X - V_Y}$, $\frac{Z_2}{Z} = \frac{V_Y}{V_Y - V_X}$

$\therefore \frac{Z_1}{Z} + \frac{Z_2}{Z} = \frac{V_X}{V_X - V_Y} + \frac{V_Y}{V_Y - V_X} = 1$, 即 $Z_1 + Z_2 = Z$



$Z_1 + Z_2$ 之间某点可以接地,
X与Y反向

Figure 6.33



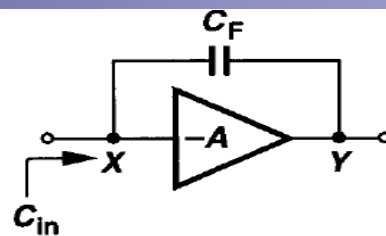
例6.1 计算图6.2输入电容

$$Z = \frac{1}{C_F s}$$

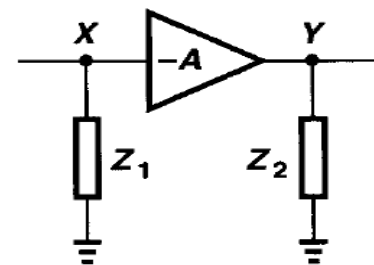
$$\frac{V_Y}{V_X} = -A, \quad A \text{ 为正}$$

$$Z_1 = \frac{Z}{1 - \frac{V_Y}{V_X}} = \frac{\frac{1}{C_F s}}{1 + A} = \frac{1}{(1 + A)C_F s}$$

$$Z_2 = \frac{Z}{1 - \frac{V_X}{V_Y}} = \frac{\frac{1}{C_F s}}{1 + \frac{1}{A}} = \frac{A}{(A + 1)C_F s} \approx \frac{1}{C_F s}$$



(a)



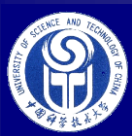
(b)

Figure 6.2

the input capacitance is equal to $C_F(1 + A)$.

密勒效应的物理意义：
输入阻抗变小！

$A \gg 1$ 时，X点小信号电压很小



Miller 效应计算输出阻抗的错误情况

如果X和Y点同相，Miller 效应不能正确计算输出阻抗。

验证例：输入
输出同向。
拆掉R1

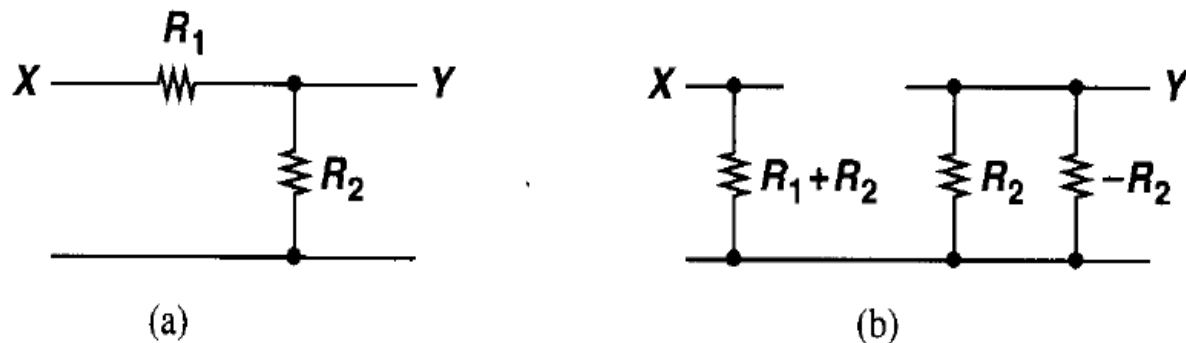


Figure 6.3 Improper application of Miller's theorem.

$$Z_1 = \frac{Z}{1 - \frac{V_Y}{V_X}} = \frac{R_1}{1 - \frac{R_2}{R_1 + R_2}} = R_1 + R_2$$

无论输入输出是同相或反相，
密勒定律计算输入阻抗正确！

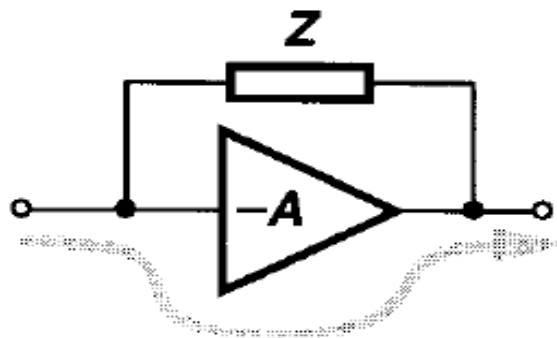
$$Z_2 = \frac{Z}{1 - \frac{V_X}{V_Y}} = \frac{R_1}{1 - \frac{R_1 + R_2}{R_2}} = -R_2$$

输入输出同相时，
密勒定律计算输出阻抗明显错误！

应为 $R_1 \parallel R_2$



Miller theorem应用要求



Main Signal Path

Figure 6.4 Typical case for valid application of Miller's theorem.

输入阻抗计算正确，
但输出阻抗和增益
计算正确前提是：
输入与输出反相。

Miller's theorem proves useful in cases where the impedance Z appears in parallel with the main signal

应用米勒效应进行电路简化计算的另一个局限性：

可能丢掉传递函数零点（该频率下两条支路输出之和为“0”，实为 $1+/-j$ ）



6.1.2 极点与结点的关联（前向结构）

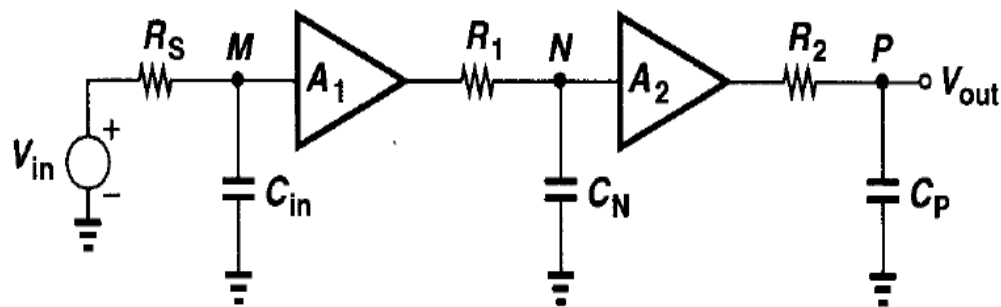


Figure 6.6 Cascade of amplifiers.

极点：频率（传递函数幅频特性）
 结点或节点：信号通道电路连接点
 R_1 and R_2 model the output resistance of each stage.

- 复频域定义， $s = \sigma + j\omega$ ($\sigma \leq 0$)
- $s = j\omega$ 得到稳态频率响应。
- A_1 、 A_2 为低频增益。

$$\frac{V_{out}}{V_{in}}(s) = \frac{\frac{1}{C_{in}s}}{\frac{1}{C_{in}s} + R_s} * A_1 * \frac{\frac{1}{C_Ns}}{\frac{1}{C_Ns} + R_1} * A_2 * \frac{\frac{1}{C_Ps}}{\frac{1}{C_Ps} + R_2} = \frac{A_1}{1 + R_s C_{in}s} \cdot \frac{A_2}{1 + R_1 C_Ns} \cdot \frac{1}{1 + R_2 C_Ps} = \frac{A_1}{1 + s/\omega_{in}} \cdot \frac{A_2}{1 + s/\omega_1} \cdot \frac{1}{1 + s/\omega_2}$$

低频增益加分母极点

- 结论:在前向结构的电路中，每个结点j的时间常数（极点）：

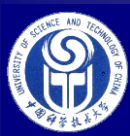
τ_j = 节点到地总电阻 * 节点到地总电容，
 其倒数对应各极点的角频率

$$\omega_j = \frac{1}{\tau_j}$$

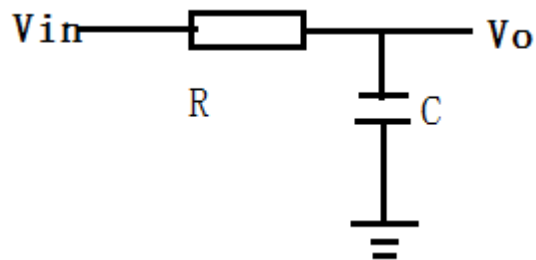
极点（角频率）表示
 比低频时下降3dB

即信号通道上每个结点阻容值乘积（时间常数）之倒数贡献一个极点。

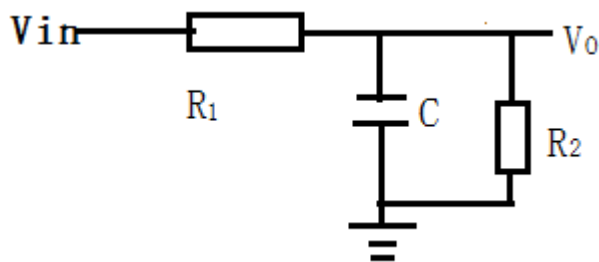
- 如有RC反馈回路，结论不成立。



验证：极点时间常数=节点到地总电阻*总电容

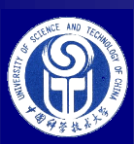


$$A = \frac{V_o}{V_{in}} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} \times \frac{R}{R} = \frac{\frac{1}{sC} \parallel R}{R}$$
$$= \frac{\tilde{C} \parallel R}{R} \quad (\text{即 } \frac{1}{sC} \text{ 记为 } \tilde{C}) = \frac{1}{1 + sCR}$$

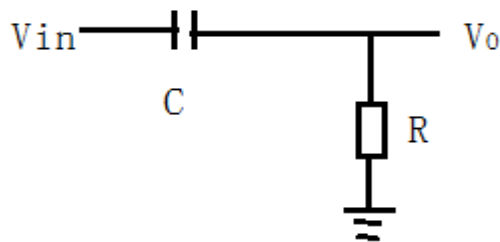


Vo节点到地总电阻为 $R_1 \parallel R_2$

$$A = \frac{V_o}{V_{in}} = \frac{\tilde{C} \parallel R_2}{R_1 + \tilde{C} \parallel R_2} \times \frac{R_1}{R_1} = \frac{\tilde{C} \parallel R_2 \parallel R_1}{R_1} \times \frac{R_2 \parallel R_1}{R_2 \parallel R_1}$$
$$= \frac{1}{1 + sC(R_1 \parallel R_2)} \times \frac{R_2 \parallel R_1}{R_1} = \frac{1}{1 + sC(R_1 \parallel R_2)} \times \frac{R_2}{R_1 + R_2}$$
$$\text{低频 } A_0 = \frac{R_2}{R_1 + R_2}$$

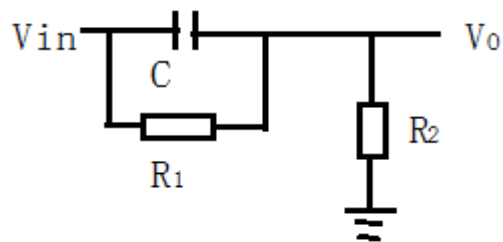


验证（续）：极点时间常数=节点到地总R*总C



$$A = \frac{V_o}{V_{in}} = \frac{R}{R + \frac{1}{sC}} = \frac{sCR \text{ (真正零点)}}{1 + sCR}$$

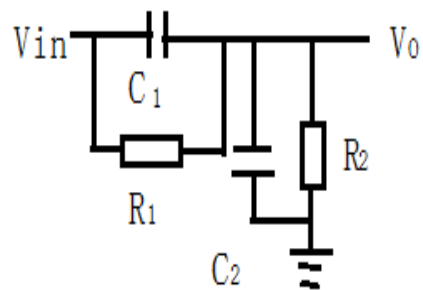
极点（分母=0时角频率）结论仍然正确，高频时 $A_{\infty} = 1$



$$\begin{aligned} A = \frac{V_o}{V_{in}} &= \frac{R_2}{R_2 + \frac{1}{sC} \parallel R_1} \times \frac{\frac{1}{sC} \parallel R_1}{\frac{1}{sC} \parallel R_1} = \frac{\frac{1}{sC} \parallel R_1 \parallel R_2}{\frac{1}{sC} \parallel R_1} \times \frac{R_1 \parallel R_2}{R_1 \parallel R_2} \times \frac{R_1}{R_1} \\ &= \frac{1 + sCR_1}{1 + sC(R_1 \parallel R_2)} \times \frac{R_1 \parallel R_2}{R_1} = \frac{1 + sCR_1}{1 + sC(R_1 \parallel R_2)} \times \frac{R_2}{R_1 + R_2} \end{aligned}$$

重复利用 $\frac{\frac{1}{sC} \parallel R}{R} = \frac{1}{1 + sCR}$

低频 $A_0 = \frac{R_2}{R_1 + R_2}$ ，极高频 $A_{\infty} = \frac{R_1}{(R_1 \parallel R_2)} \times \frac{R_2}{R_1 + R_2} = 1$

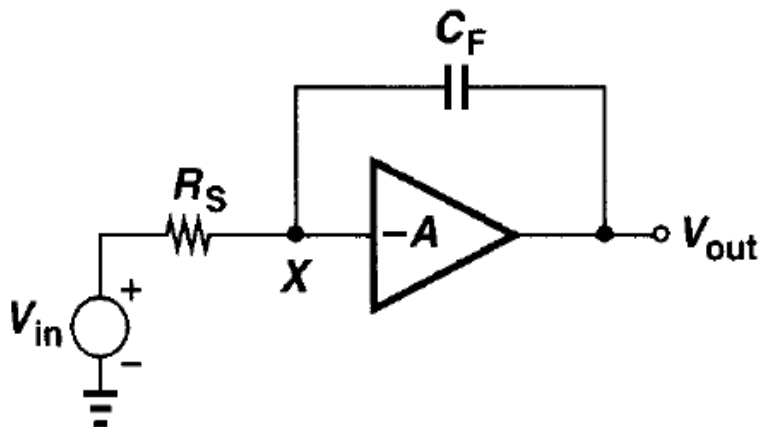


$$\begin{aligned} A = \frac{V_o}{V_{in}} &= \frac{\frac{1}{sC_2} \parallel R_2}{\frac{1}{sC_1} \parallel R_1 + \frac{1}{sC_2} \parallel R_2} \times \frac{\frac{1}{sC_1} \parallel R_1}{\frac{1}{sC_1} \parallel R_1} = \frac{(\frac{1}{sC_2} \parallel R_2) \parallel (\frac{1}{sC_1} \parallel R_1)}{\frac{1}{sC_1} \parallel R_1} \times \frac{R_2 \parallel R_1}{R_2 \parallel R_1} \\ &= \frac{1}{1 + s(C_1 + C_2)(R_1 \parallel R_2)} \times \frac{R_2 \parallel R_1}{\frac{1}{sC_1} \parallel R_1} \times \frac{R_1}{R_1} = \frac{1 + sC_1R_1}{1 + s(C_1 + C_2)(R_1 \parallel R_2)} \times \frac{R_2}{R_1 + R_2} \end{aligned}$$

低频 $A_0 = \frac{R_2}{R_1 + R_2}$ ，极高频 $A_{\infty} = \frac{C_1R_1}{(C_1 + C_2)(R_1 \parallel R_2)} \times \frac{R_2}{R_1 + R_2} = \frac{C_1}{C_1 + C_2}$



结点与极点关联的电路局限性



- 输入极点:

$$1/[R_S(1 + A)C_F] \text{ (in rad/s).}$$

前馈电路，
或单一性质反馈器件

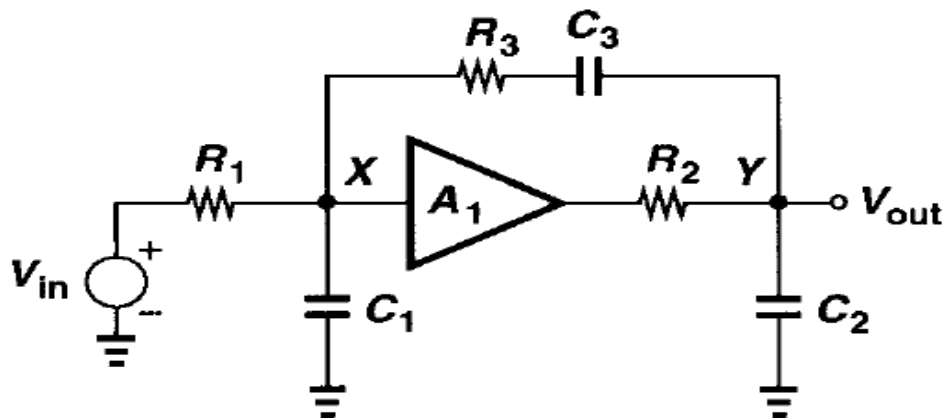
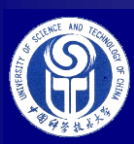


Figure 6.7 Example of interaction between nodes.

- Example 6.3

- X超过1个极点。
- 每个结点贡献一个极点的结论不成立



Example 6.4

- Neglecting channel-length modulation. Calculate the transfer function of common-gate stage shown in fig.6.9

At node X, $C_S = C_{GS1} + C_{SB1}$, giving a pole frequency

$$\omega_{in} = \left[(C_{GS1} + C_{SB1}) \left(R_S \parallel \frac{1}{g_{m1} + g_{mb1}} \right) \right]^{-1}$$

at node Y, $C_D = C_{DG} + C_{DB}$, yielding a pole frequency

$$\omega_{out} = [(C_{DG} + C_{DB})R_D]^{-1}.$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S} \cdot \frac{1}{\left(1 + \frac{s}{\omega_{in}}\right) \left(1 + \frac{s}{\omega_{out}}\right)}, \quad (6.13)$$

where the first fraction represents the low-frequency gain of the circuit. Note that if we do not neglect r_{O1} , the input and output nodes interact, making it difficult to calculate the poles.

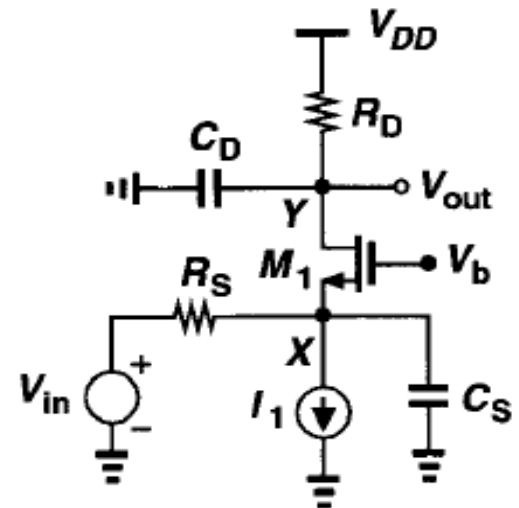


Figure 6.9 Common-gate stage with parasitic capacitances.



6.2 Common-Source Stage

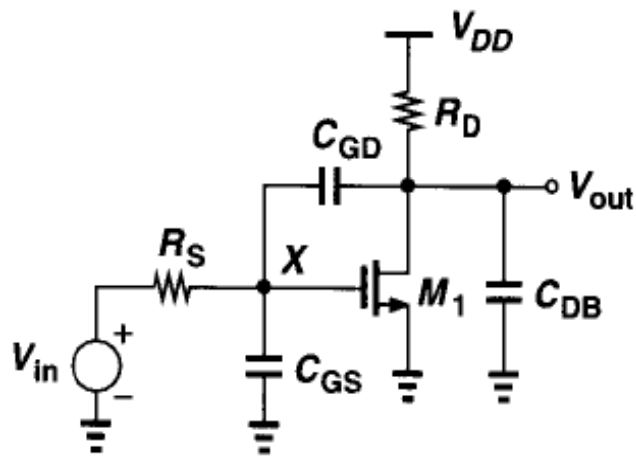


Figure 6.10 High-frequency model of a common-source stage.

Assuming that $\lambda = 0$

输入节点电容 $C_{GS} + (1 - A_v) C_{GD}$, $A_v = -g_m R_D$

频率升高, M_1 输入下降:

$$\frac{V_{GS}}{V_{in}} = \frac{\frac{1}{s[C_{GS} + (1 + g_m R_D)C_{GD}]}}{R_S + \frac{1}{s[C_{GS} + (1 + g_m R_D)C_{GD}]}} = \frac{1}{sR_S[C_{GS} + (1 + g_m R_D)C_{GD}] + 1}$$

输出节点: $C_{DB} + (1 - A_v^{-1})C_{GD} = C_{DB} + C_{GD}$

频率升高, V_{out} 下降:
$$\frac{R_D \parallel \frac{1}{s(C_{DB} + C_{GD})}}{R_D} = \frac{1}{sR_D(C_{DB} + C_{GD}) + 1}$$

$$\omega_{in} = \frac{1}{R_S[C_{GS} + (1 + g_m R_D)C_{GD}]}. \quad (6.14)$$

$$\omega_{out} = \frac{1}{R_D(C_{DB} + C_{GD})} \quad (6.15)$$

密勒定律用于近似计算!
使节点与极点关联。



传输函数的估算

We then surmise that the transfer function is

$$\frac{V_{out}}{V_{in}}(s) = \frac{-g_m R_D}{\left(1 + \frac{s}{\omega_{in}}\right) \left(1 + \frac{s}{\omega_{out}}\right)} \quad (6.18)$$

Miller定律截断了输入输出前向通路,导致(6.18)丢失零点,仅用作近似计算.

极点的物理意义:

- (1) 带宽: 最低频极点 (主极点) 一般为3dB带宽截止频率。
- (2) 反馈系统稳定性 (也与零点相关)。

多极点总带宽

$$\text{低通 (高频截止): } \frac{1}{\omega^2} = \frac{1}{\omega_1^2} + \frac{1}{\omega_2^2} + \dots + \frac{1}{\omega_n^2}$$



Obtain the exact transfer function

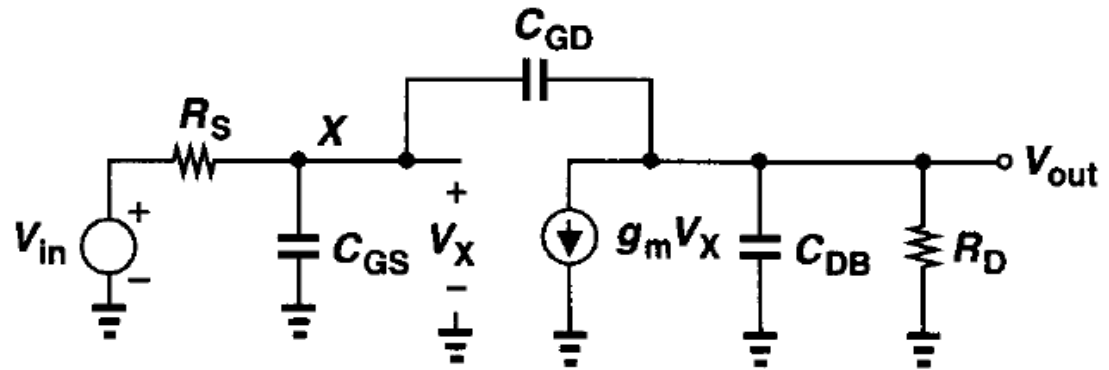
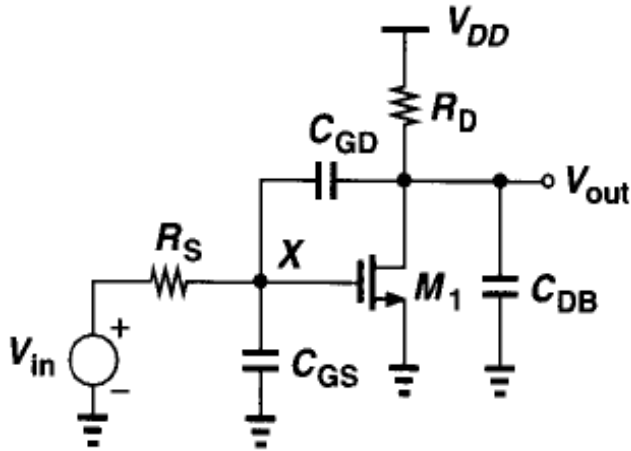


Figure 6.12 Equivalent circuit of Fig. 6.10.

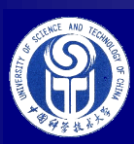
$$\frac{V_X - V_{in}}{R_S} + V_X C_{GS} s + (V_X - V_{out}) C_{GD} s = 0 \quad (6.19)$$

$$(V_{out} - V_X) C_{GD} s + g_m V_X + V_{out} \left(\frac{1}{R_D} + C_{DB} s \right) = 0 \quad (6.20)$$

From (6.20), V_X is obtained as

$$V_X = - \frac{V_{out} \left(C_{GD} s + \frac{1}{R_D} + C_{DB} s \right)}{g_m - C_{GD} s}$$

which, upon substitution in (6.19), yields



Obtain the exact transfer function (cont.)

$$-V_{out} \frac{[R_S^{-1} + (C_{GS} + C_{GD})s][R_D^{-1} + (C_{GD} + C_{DB})s]}{g_m - C_{GD}s} - V_{out} C_{GD}s = \frac{V_{in}}{R_S}$$

That is,

$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + [R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})]s + 1} \quad (6.23)$$

有1个零点!

where $\xi = C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB}$.

- C_{GS} 、 C_{GD} 、 C_{DB} 形成环路,只有2个是独立的,因此本电路是2个极点的2阶微分方程。second-order differential equation

$$\left(\frac{s}{\omega_{p1}} + 1\right) \left(\frac{s}{\omega_{p2}} + 1\right) = \frac{s^2}{\omega_{p1}\omega_{p2}} + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)s + 1$$

assume $|\omega_{p1}| \ll |\omega_{p2}|$? the coefficient of s is approximately equal to $1/\omega_{p1}$

It follows from (6.23) that $\omega_{p1} = \frac{1}{R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})}$ (6.26)

the coefficient of s^2 is equal to $(\omega_{p1}\omega_{p2})^{-1}$, we have ω_{p2} 比较(6.14)



直观方法（密勒定律）可简单粗略计算极点

讨论:

$$\omega_{p1} = \frac{1}{R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + \underbrace{R_D(C_{GD} + C_{DB})}} \quad (6.26)$$

密勒近似计算

$$\omega_{in} = \frac{1}{R_S[C_{GS} + (1 + g_m R_D)C_{GD}]} \quad (6.14)$$

How does this compare with the “input” pole given by (6.14)? The only difference results from the term $R_D(C_{GD} + C_{DB})$, which may be negligible in some cases. The key point here is that the intuitive approach of associating a pole with the input node provides a rough estimate with much less effort. We also note that the Miller multiplication of C_{GD} by the low-frequency gain of the amplifier is relatively accurate in this case.

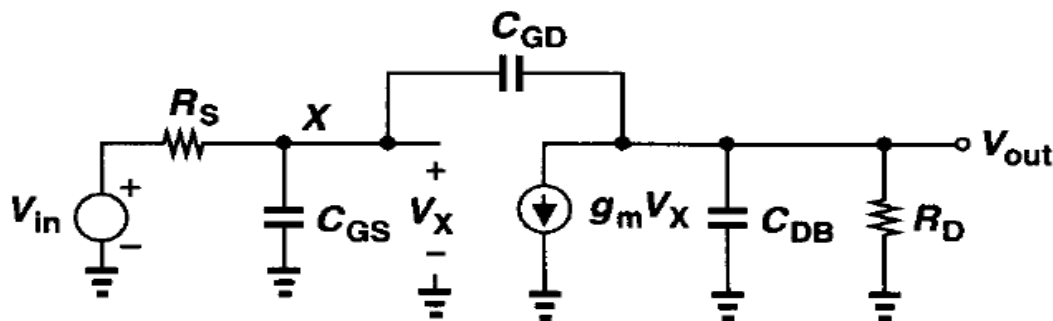
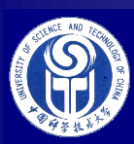


Figure 6.12 Equivalent circuit of Fig. 6.10.



C_{GS} 较大时可近似计算输出极点

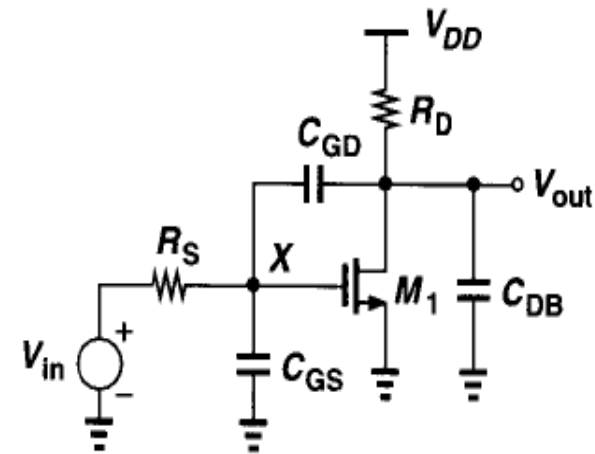
From (6.23), we can also estimate the second pole of the CS stage of Fig. 6.10. Since the coefficient of s^2 is equal to $(\omega_{p1}\omega_{p2})^{-1}$, we have

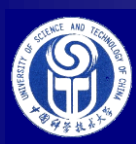
$$\begin{aligned}\omega_{p2} &= \frac{1}{\omega_{p1}} \cdot \frac{1}{R_S R_D (C_{GS} C_{GD} + C_{GS} C_{DB} + C_{GD} C_{DB})} \\ &= \frac{R_S (1 + g_m R_D) C_{GD} + R_S C_{GS} + R_D (C_{GD} + C_{DB})}{R_S R_D (C_{GS} C_{GD} + C_{GS} C_{DB} + C_{GD} C_{DB})}\end{aligned}$$

If $C_{GS} \gg (1 + g_m R_D) C_{GD} + R_D (C_{GD} + C_{DB}) / R_S$, then

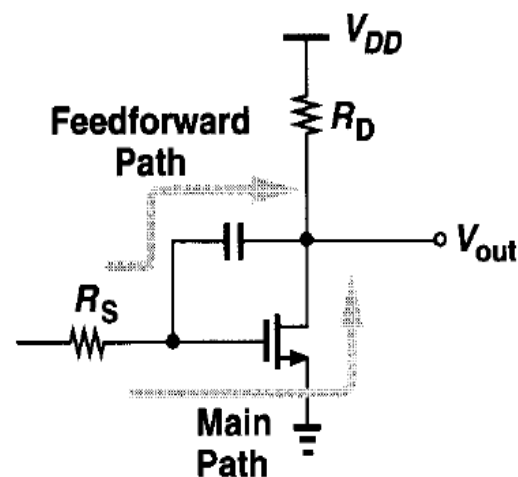
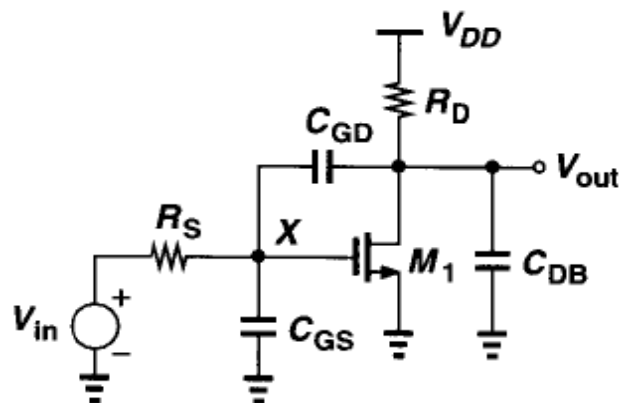
$$\begin{aligned}\omega_{p2} &\approx \frac{R_S C_{GS}}{R_S R_D (C_{GS} C_{GD} + C_{GS} C_{DB})} \\ &= \frac{1}{R_D (C_{GD} + C_{DB})},\end{aligned}\tag{6.34}$$

即(6.15)





零点



$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + [R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})]s + 1} \quad (6.23)$$

$\omega_z = +g_m/C_{GD}$ 零点产生：输入输出有阻容两条支路

C_{GD} provides a feedforward path that conducts the input signal to the output at very high frequencies

a zero in the right half plane introduces stability issues in feedback amplifiers.

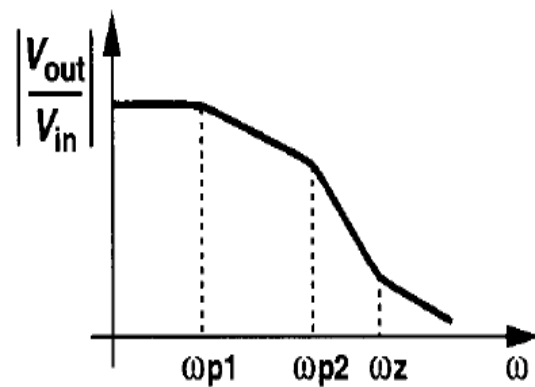
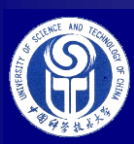


Figure 6.14



Calculation of the zero

$$V_{out}(s_z) = 0 \quad s = s_z$$

零点频率上小信号输出为“0” ($=1+j$)，实质是：
输入输出之间直通电容路径传输的容性信号
(与s频率成正比的虚数信号)
与MOS跨导传输的阻性信号幅度相等。

$$1 \pm \frac{j\omega}{\omega_z} = "0", \text{ 零点角频率时实为 } 1 \pm j$$

大于零点频率后，在输出负载上由输入输出之间直通电容路径传输的容性虚信号将超过MOS跨导传输的阻性实信号。

输出电压小信号可由输出短流电流得到相同虚实分量： $V_1 C_{GD} s_z = g_m V_1$

$$s_z = +g_m / C_{GD}$$

s_z 很大，即零点频率很高

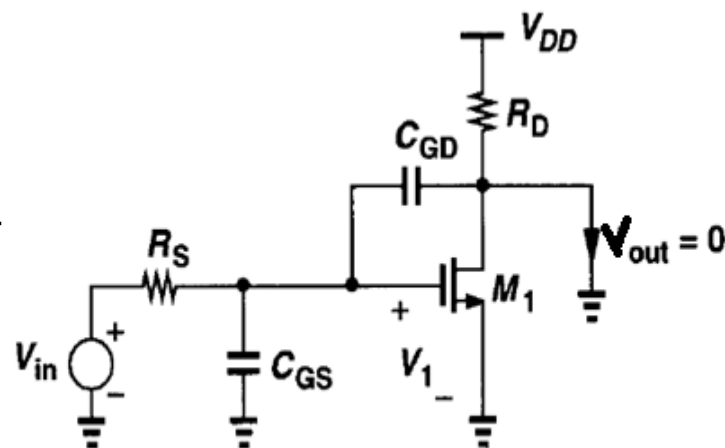
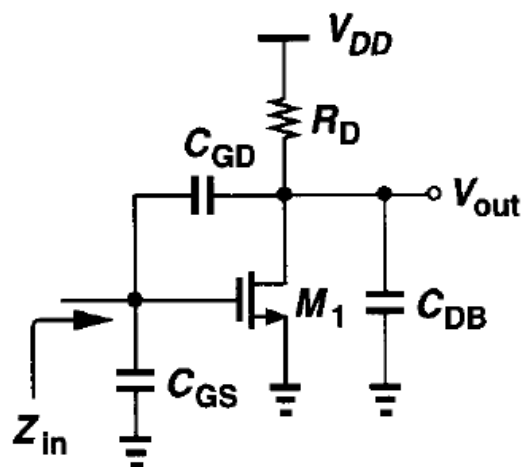


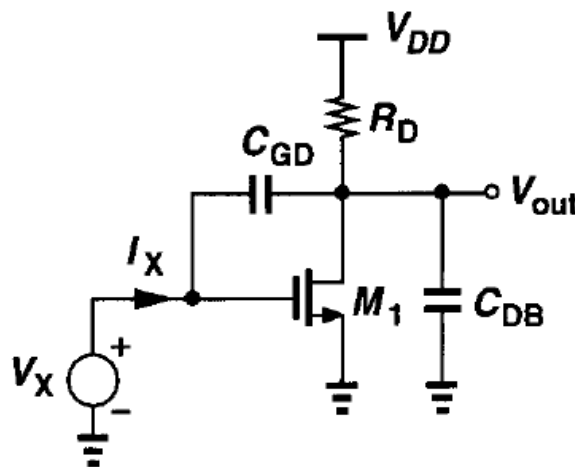
Figure 6.15 Calculation of the zero in a CS stage.



Calculation of input impedance of CS stage



(a)



(b)

计算技巧：
先不计 C_{GS}

Figure 6.16 Calculation of input impedance of a CS stage

In high-speed applications, the input impedance of the common-source stage is also important. As a first-order approximation, we have from Fig. 6.16(a)

密勒效应近似:

$$Z_{in} = \frac{1}{[C_{GS} + (1 + g_m R_D)C_{GD}]s}$$

But at high frequencies, the effect of the output node must be taken into account. Ignoring C_{GS} for the moment and using the circuit of Fig. 6.16(b), we write

精确计算:

$$(I_X - g_m V_X) \frac{R_D}{1 + R_D C_{DB} s} + \frac{I_X}{C_{GD} s} = V_X$$



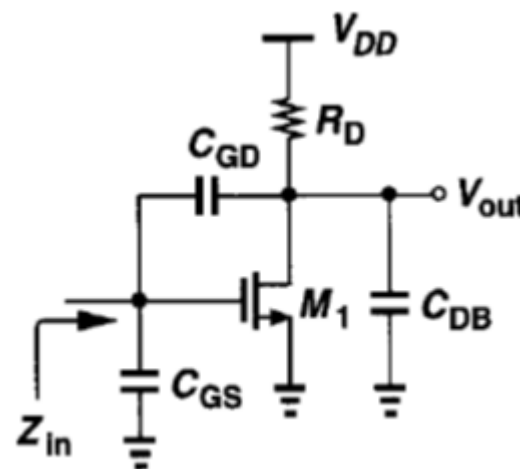
Calculation of input impedance (cont.)

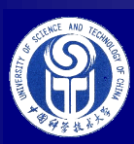
$$\frac{V_X}{I_X} = \frac{1 + R_D(C_{GD} + C_{DB})s}{C_{GD}s(1 + g_m R_D + R_D C_{DB}s)} \quad (6.38)$$

The actual input impedance consists of the parallel combination of (6.38) and $1/(C_{GS}s)$.

精确的总输入阻抗:

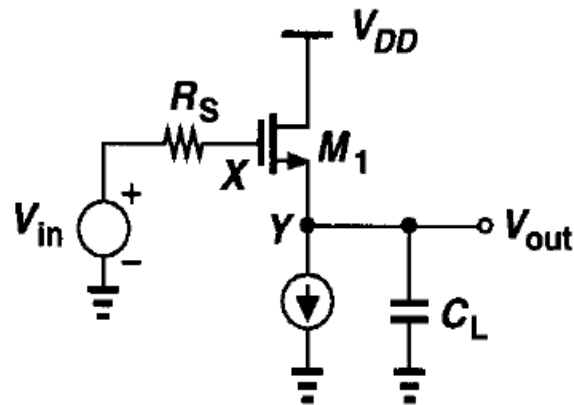
$$Z_{in} = \frac{1 + R_D(C_{GD} + C_{DB})s}{C_{GD}s(1 + g_m R_D + R_D C_{DB}s)} \parallel \frac{1}{C_{GS}s}$$





6.3 Source Followers

Source followers are occasionally employed as level shifters or buffers.



低频:

$$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S} \quad (3.80)$$

注意：式3.80中的 R_S 是源极电阻。不是左图信号源电阻

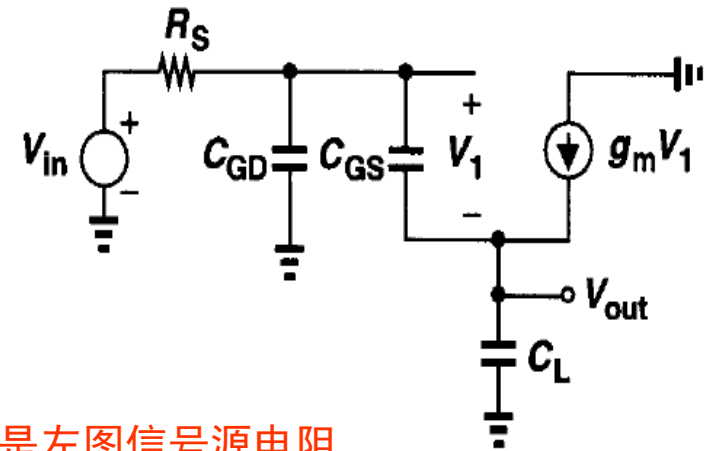


Figure 6.17 (a) Source follower, (b) high-frequency equivalent circuit. 同相

The strong interaction between nodes X and Y through C_{GS} makes it difficult to associate a pole with each node in a source follower.

$$V_1 C_{GS} s + g_m V_1 = V_{out} C_L s$$

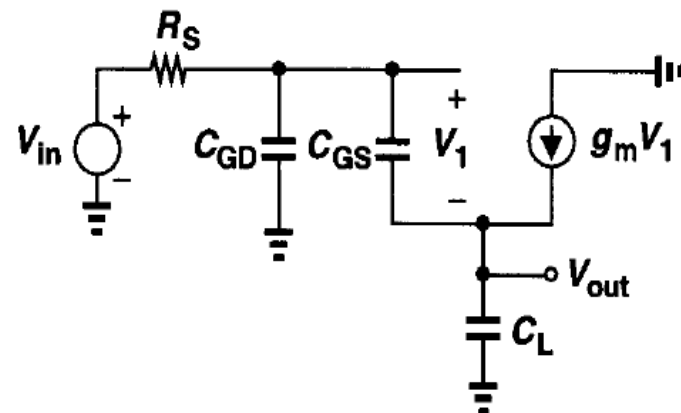
obtaining

$$V_1 = \frac{C_L s}{g_m + C_{GS} s} V_{out} \quad (6.40)$$



Source Followers (cont.)

$$V_{in} = R_S[V_1 C_{GS} s + (V_1 + V_{out}) C_{GD} s] + V_1 + V_{out}$$



Substituting for V_1 from (6.40), we have

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m + C_{GS}s}{R_S(C_{GS}C_L + C_{GS}C_{GD} + C_{GD}C_L)s^2 + (g_m R_S C_{GD} + C_L + C_{GS})s + g_m} \quad (6.42)$$

If the two poles of (6.42) are assumed far apart, then the more significant one has a magnitude of

$$\omega_{p1} \approx \frac{g_m}{g_m R_S C_{GD} + C_L + C_{GS}} = \frac{1}{R_S C_{GD} + \frac{C_L + C_{GS}}{g_m}} \quad (6.44)$$

if $R_S = 0$, then $\omega_{p1} = g_m / (C_L + C_{GS})$ 1个极点



Input impedance of SF

$$V_X = \frac{I_X}{C_{GS}s} + \left(I_X + \frac{g_m I_X}{C_{GS}s} \right) \left(\frac{1}{g_{mb}} \parallel \frac{1}{C_L s} \right)$$

$$Z_{in} = \frac{1}{C_{GS}s} + \left(1 + \frac{g_m}{C_{GS}s} \right) \times \frac{1}{g_{mb} + C_L s}, \text{ 式 (6.46)}$$

$$\text{低频时: } Z_{in} \approx \frac{1}{C_{GS}s} + \frac{g_m}{C_{GS}s} \times \frac{1}{g_{mb}} = \frac{g_m + g_{mb}}{s C_{GS} g_{mb}}$$

$$= \frac{1}{s C_{GS} \frac{g_{mb}}{g_m + g_{mb}}}$$

$$\text{总输入电容 (低频)} = C_{GS} \frac{g_{mb}}{g_m + g_{mb}} \parallel C_{GD}$$

$$\text{高频时: } Z_{in} = \frac{V_X}{I_X} \approx \frac{1}{C_{GS}s} + \left(1 + \frac{g_m}{C_{GS}s} \right) \times \frac{1}{s C_L} = \frac{1}{s C_{GS}} + \frac{1}{s C_L} + \frac{g_m}{C_{GS} C_L s^2} \text{ 负阻}$$

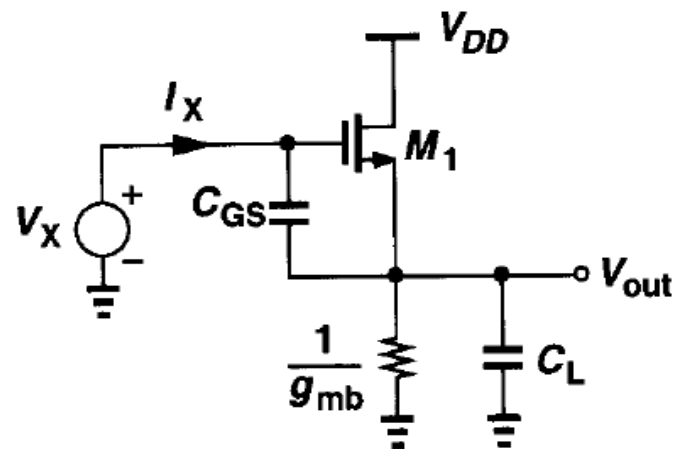
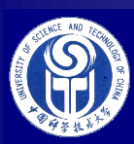


Figure 6.18 Calculation of source follower input impedance.

先不计 C_{GD}



Output impedance of SF

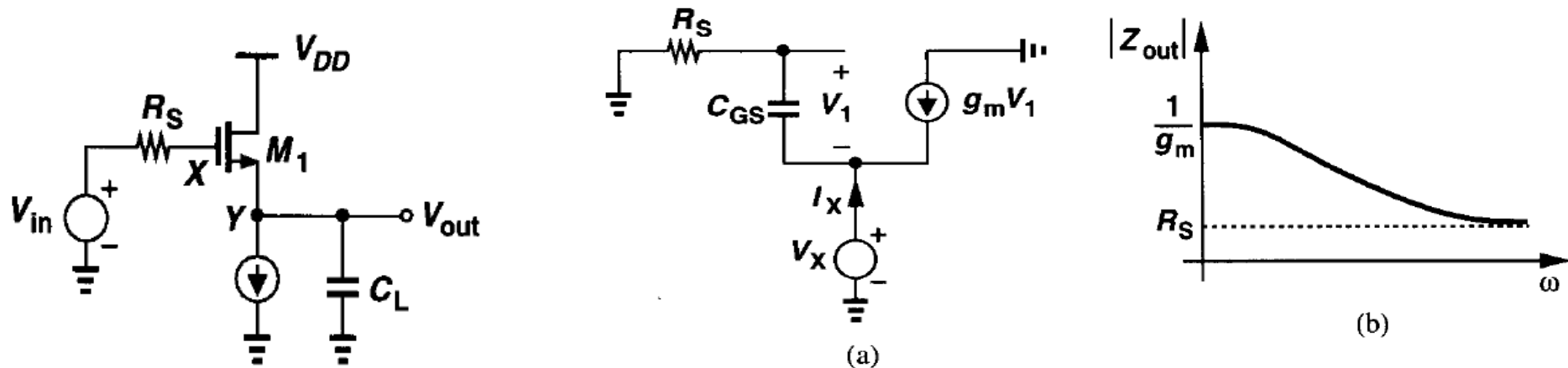


Figure 6.20 Calculation of source follower output impedance.

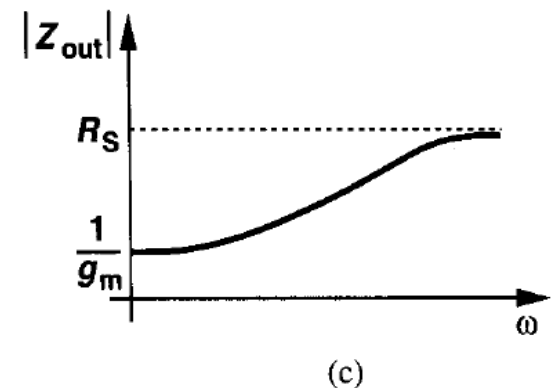
体效应和沟道长度调制效应产生的等效电阻,
以及CSB位于输出到地,先不计,最后再并联简化计算.

neglecting C_{GD}

$$V_1 C_{GS} s + g_m V_1 = -I_X$$

$$V_1 C_{GS} s R_S + V_1 = -V_X$$

$$Z_{out} = \frac{V_X}{I_X} = \frac{R_S C_{GS} s + 1}{g_m + C_{GS} s}$$



Operating as buffers, $1/g_m < R_S$.
must lower the output impedance.



Output impedance of SF (cont.)

Since the output impedance *increases* with frequency, we postulate (假设) that it contains an *inductive* component.

Z_{out} equals $1/g_m$ at $\omega = 0$ and R_S at $\omega = \infty$.

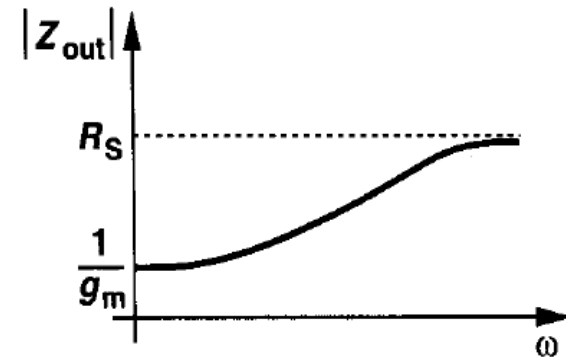
$$R_2 = 1/g_m, R_1 = R_S - 1/g_m,$$

$$Z_{out} = R_2 + sL \parallel R_1$$

$$Z_{out} - R_2 = \frac{R_S C_{GS} s + 1}{g_m + C_{GS} s} - \frac{1}{g_m} = \frac{C_{GS} s (R_S - \frac{1}{g_m})}{g_m + C_{GS} s}$$

$$\frac{1}{Z_{out} - \frac{1}{g_m}} = \frac{1}{R_S - \frac{1}{g_m}} + \frac{1}{\frac{C_{GS} s}{g_m} \left(R_S - \frac{1}{g_m} \right)}$$

$$L = \frac{C_{GS}}{g_m} \left(R_S - \frac{1}{g_m} \right)$$



(c)

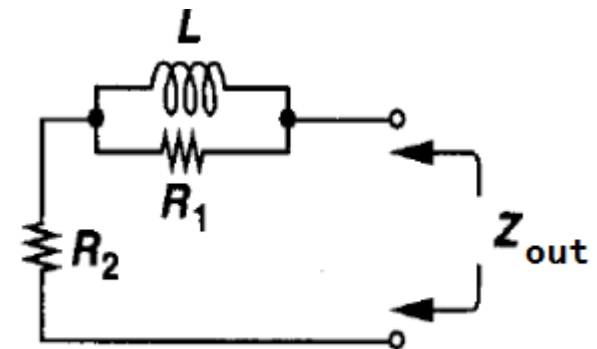


Figure 6.21 Equivalent output impedance of a source follower.



Output impedance of SF (cont.)

$$L = \frac{C_{GS}}{g_m} \left(R_S - \frac{1}{g_m} \right)$$

The dependence of L upon R_S implies that if a source follower is driven by a large resistance, then it exhibits substantial inductive behavior. As depicted in Fig. 6.22, this effect manifests itself as “ringing” in the step response if the circuit drives a large load capacitance.

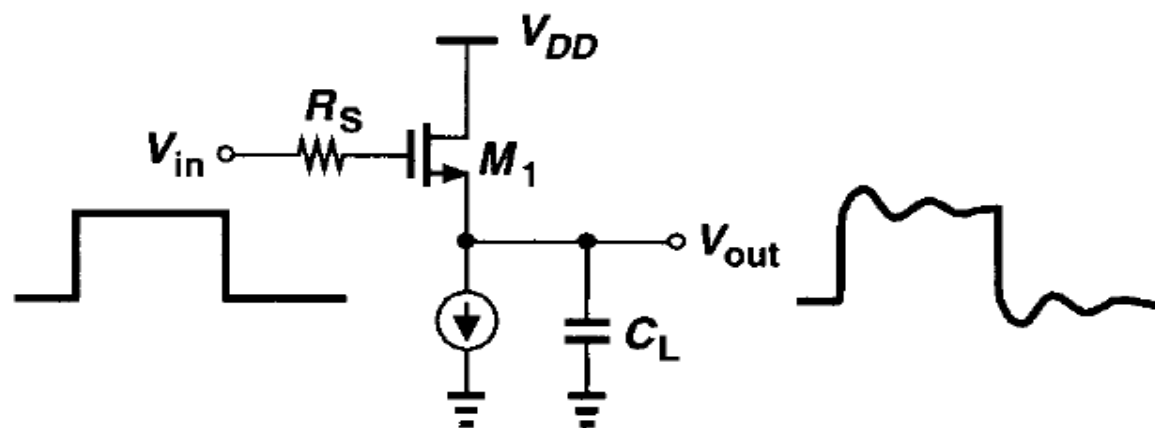


Figure 6.22 Ringing in step response of a source follower with heavy capacitive load.



Example 6.6

Calculate the transfer function of the circuit shown in Fig. 6.19(a).

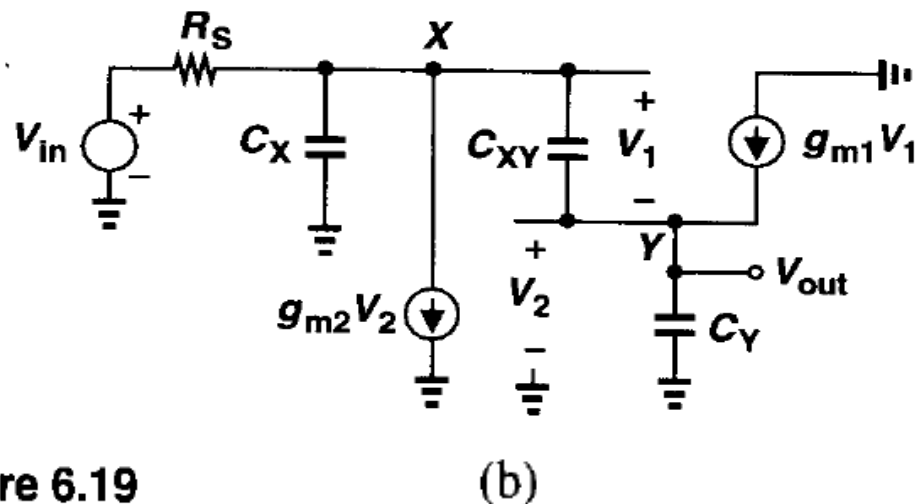
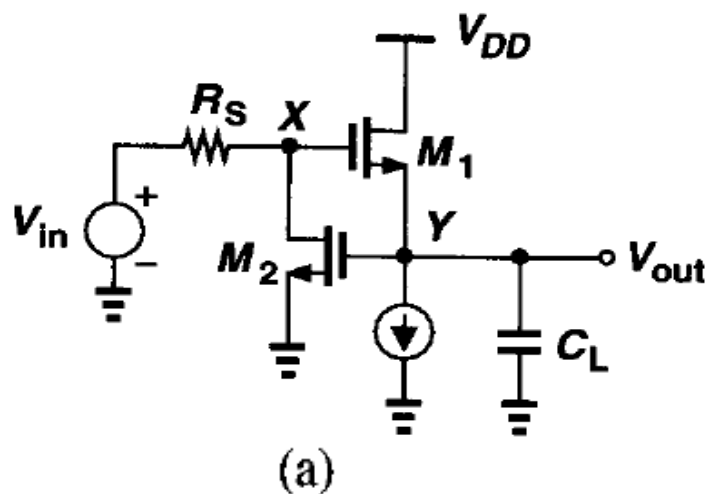


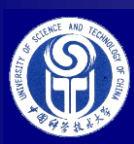
Figure 6.19

Solution

$$C_X = C_{GD1} + C_{DB2} \quad C_{XY} = C_{GS1} + C_{GD2} \quad C_Y = C_{SB1} + C_{GS2} + C_L$$

this circuit has three capacitances in a loop and hence a second-order transfer function.

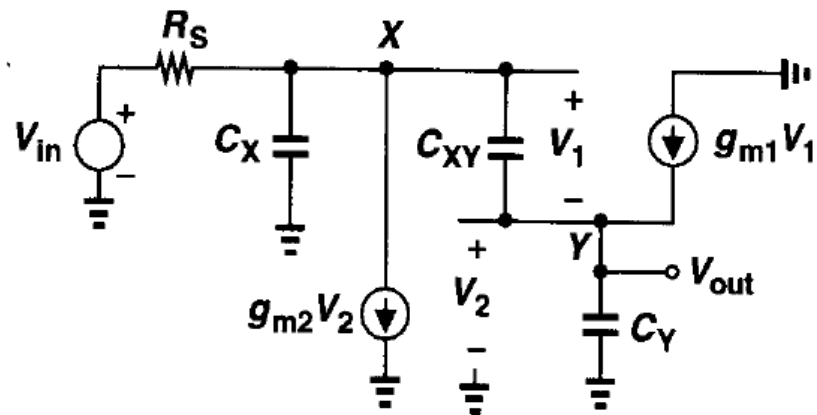
$$(V_1 + V_{out})C_X s + g_{m2}V_{out} + V_1 C_{XY} s = \frac{V_{in} - V_1 - V_{out}}{R_S} \quad (6.49)$$



Example 6.6 (cont.)

$$V_1 C_{XY} s + g_{m1} V_1 = V_{out} C_Y s$$

$$\text{hence } V_1 = V_{out} C_Y s / (C_{XY} s + g_{m1})$$



$$(6.49) \rightarrow \frac{V_{out}}{V_{in}}(s) = \frac{g_{m1} + C_{XY} s}{R_S \xi s^2 + [C_Y + g_{m1} R_S C_X + (1 + g_{m2} R_S) C_{XY}] s + g_{m1} (1 + g_{m2} R_S)} \quad (6.50)$$

$$\text{where } \xi = C_X C_Y + C_X C_{XY} + C_Y C_{XY}$$

无M2中的受控电流源时:

$$g_{m2} = 0 \rightarrow \frac{V_{out}}{V_{in}}(s) = \frac{g_m + C_{GS} s}{R_S (C_{GS} C_L + C_{GS} C_{GD} + C_{GD} C_L) s^2 + (g_m R_S C_{GD} + C_L + C_{GS}) s + g_m} \quad (6.42)$$

利用M2改变零极点设计。本例增益太小，无实际用途



6.4 Common-gate stage

由例6.4图6.9式(6.11)~(6.13)

$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S} \cdot \frac{1}{\left(1 + \frac{s}{\omega_{in}}\right)\left(1 + \frac{s}{\omega_{out}}\right)}, \quad (6.13)$$

得:

$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S} \frac{1}{\left(1 + \frac{C_S}{g_m + g_{mb} + R_S^{-1}}s\right)(1 + R_D C_D s)}$$

(忽略沟道长度调制效应)

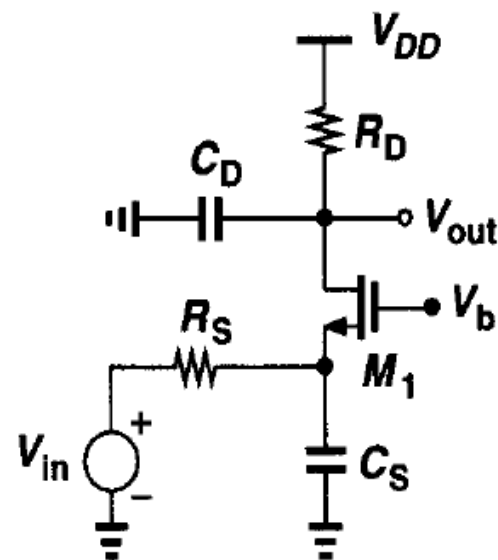


Figure 6.23 Common-gate stage at high frequencies.



$$\lambda \neq 0.$$

If channel-length modulation is not negligible, $\lambda \neq 0$.

From Eq. (3.110),

$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O}$$

$$\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}},$$

we have

$$Z_{in} \approx \frac{Z_L}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}, \quad (6.57)$$

$$\text{where } Z_L = R_D \parallel [1/(C_D s)]$$

Since Z_{in} now depends on Z_L , it is difficult to associate a pole with the input node.

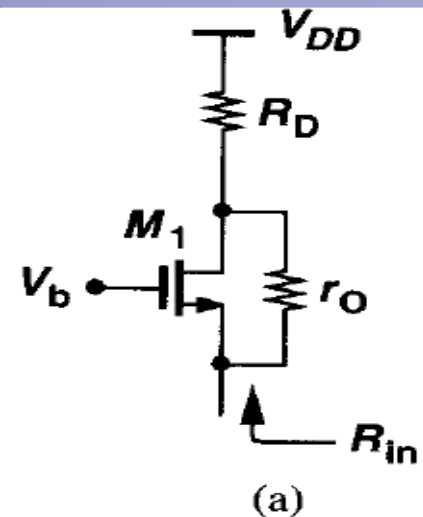
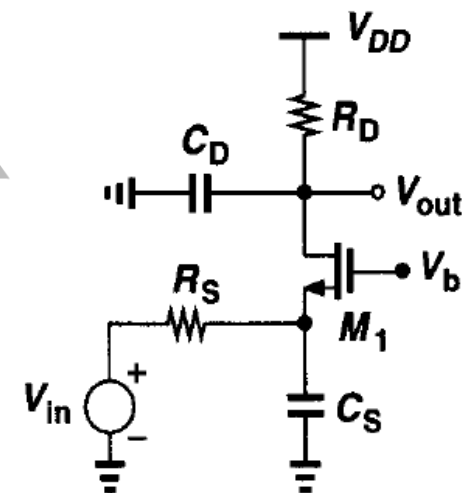
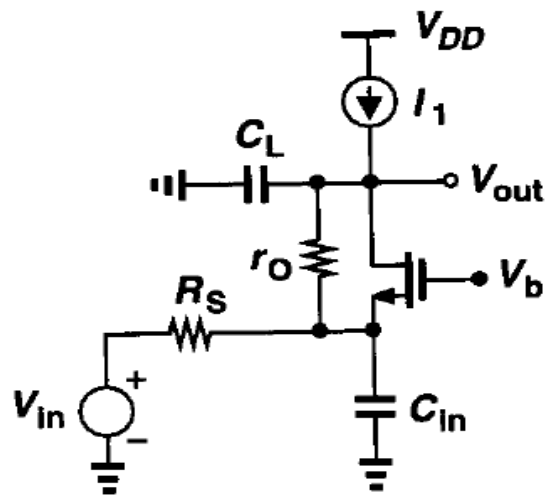


Figure 3.45

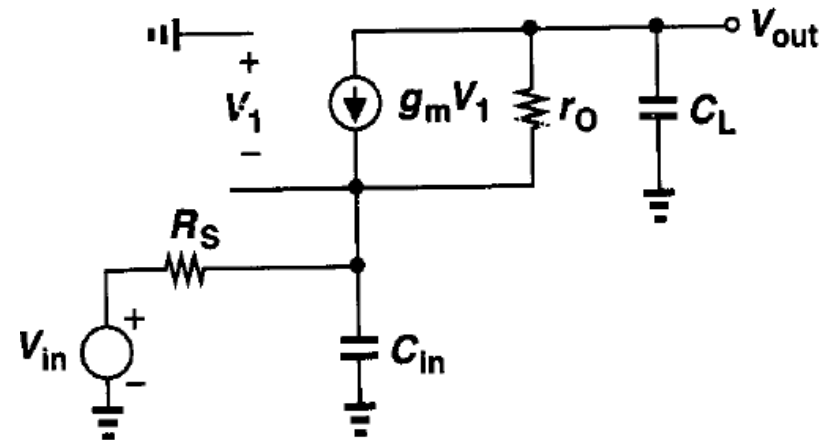




Example 6.7: 计算传递函数和输入阻抗



(a)



(b)

Figure 6.24

$$(-V_{out}C_Ls + V_1C_{in}s)R_S + V_{in} = -V_1$$

$$V_1 = -\frac{-V_{out}C_LsR_S + V_{in}}{1 + C_{in}R_Ss}$$

$$r_O(-V_{out}C_Ls - g_m V_1) - V_1 = V_{out}$$



Example 6.7 (cont.)

$$\rightarrow \frac{V_{out}}{V_{in}}(s) = \frac{1 + g_m r_O}{r_O C_L C_{in} R_S s^2 + [r_O C_L + C_{in} R_S + (1 + g_m r_O) C_L R_S] s + 1}$$

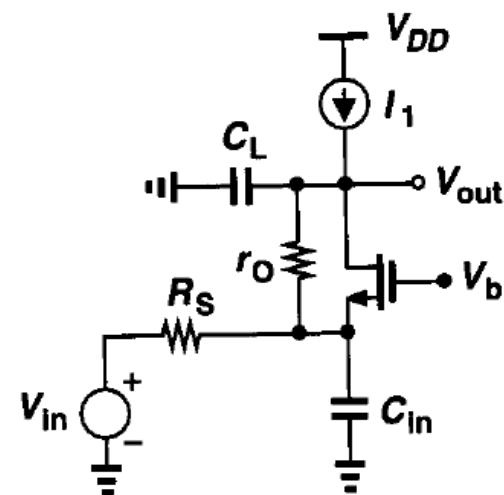
body effect can be included by replacing g_m with $g_m + g_{mb}$.

the gain at very low frequencies is equal to $1 + g_m r_O$.

from (6.57)
$$Z_{in} = \frac{1}{g_m + g_{mb}} + \frac{1}{C_L s} \cdot \frac{1}{(g_m + g_{mb}) r_O}$$

note that as C_L or s increases, Z_{in} approaches $1/(g_m + g_{mb})$

hence the input pole
$$\omega_{p,in} = \frac{1}{\left(R_S \parallel \frac{1}{g_m + g_{mb}} \right) C_{in}}$$



(a)

C_L lowers the voltage gain

the output impedance of the circuit drops at high frequencies.



6.5 Cascode Stage

A到X的增益为: $\frac{-g_{m1}}{g_{m2} + g_{mb2}}$

$$\omega_{p,A} = \frac{1}{R_S \left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m2} + g_{mb2}} \right) C_{GD1} \right]}$$

A到X的增益小 (~ 1)，米勒效应电容小。
主极点大，适合高频。

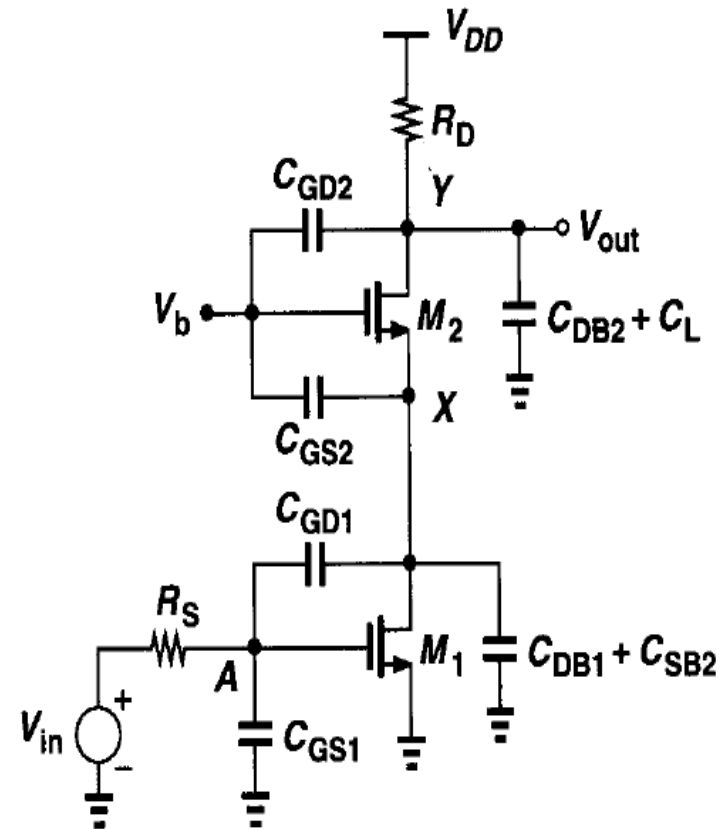


Figure 6.25 High-frequency model of a cascode stage.



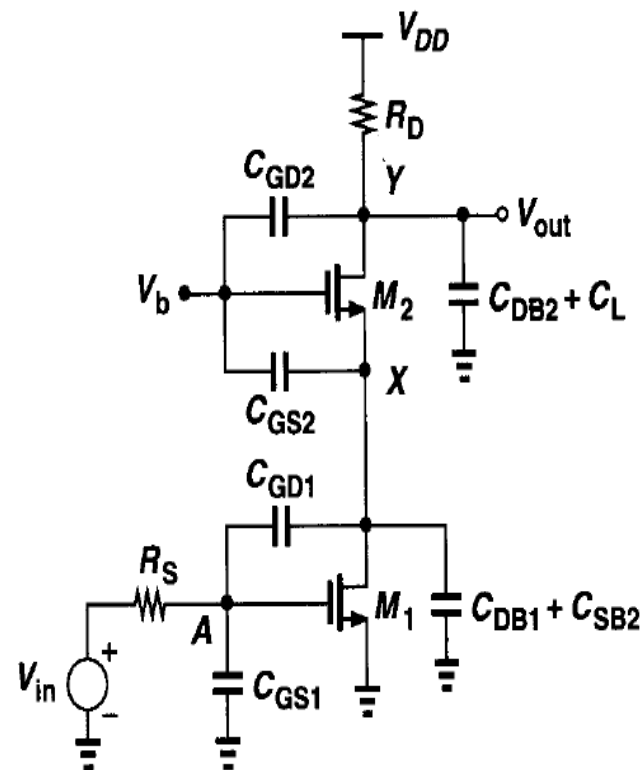
Cascode Stage (cont.)

$$\omega_{p,X} = \frac{g_{m2} + g_{mb2}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}}$$

A 到 X 增益 ≈ -1

the output node yields a third pole:

$$\omega_{p,Y} = \frac{1}{R_D(C_{DB2} + C_L + C_{GD2})}$$





6.6 Differential pair

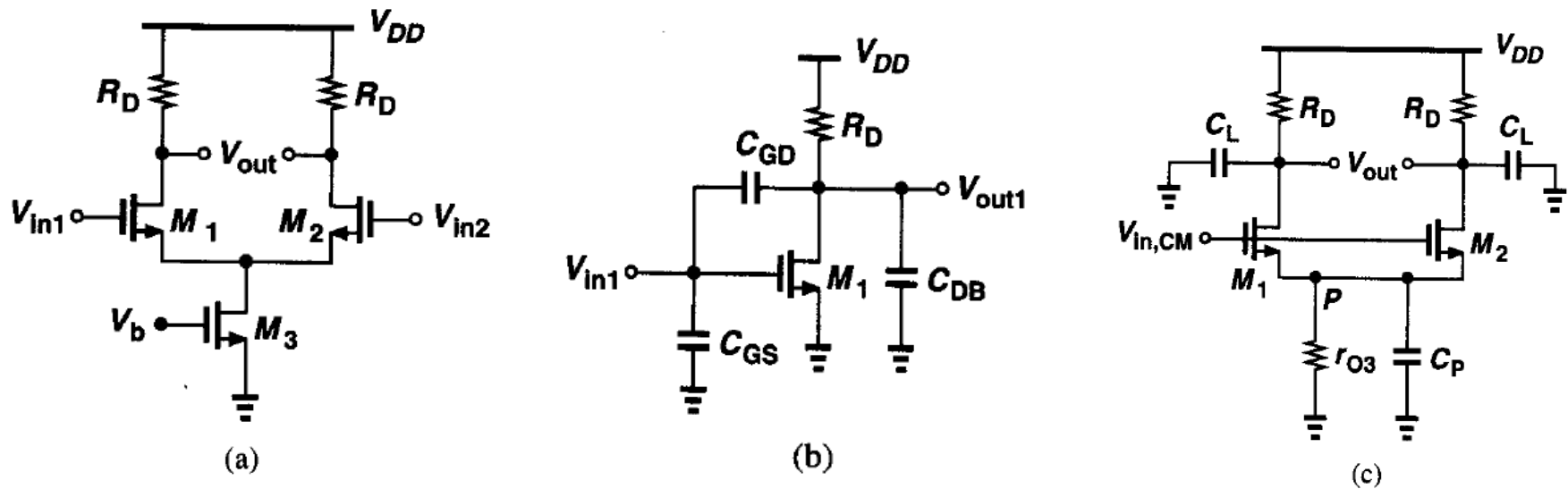


Figure 6.27 (a) Differential pair, (b) half-circuit equivalent, (c) equivalent circuit for common-mode inputs.



失配的影响：

仅考虑跨导失配：

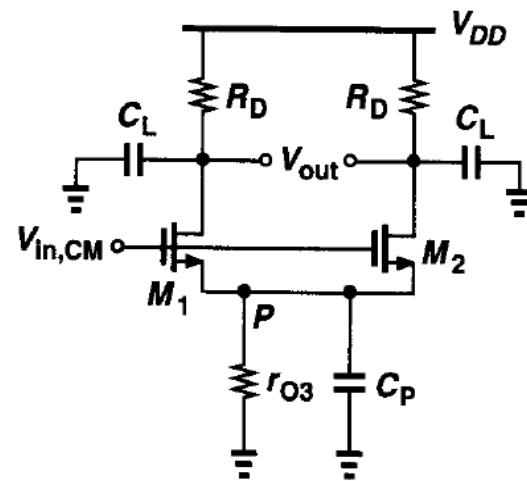
第4章，低频：

$$A_{CM-DM} = - \frac{\Delta g_m R_D}{(g_{m1} + g_{m2}) r_{o3} + 1}$$

当尾电流源 L_3 大，则 W_3 大，故 C_{GD3} and C_{DB3} 大。

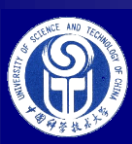
$$C_p \approx C_{GD3} + C_{DB3} + C_{GS1} + C_{SB1} + C_{GS2} + C_{SB2}$$

$$A_{CM-DM} = - \frac{\Delta g_m [R_D \parallel \frac{1}{sC_L}]}{(g_{m1} + g_{m2}) [r_{o3} \parallel \frac{1}{sC_p}] + 1}$$



(c)

CM信号的影响在于电路失配将CM转换成了DM信号！



$$\begin{aligned}
 A_{CM-DM} &= \frac{\Delta g_m [R_D || (\frac{1}{C_{LS}})]}{(g_{m1} + g_{m2}) [r_{o3} || (\frac{1}{C_{PS}})] + 1} = \frac{\Delta g_m \frac{R_D}{R_D C_{LS} + 1}}{(g_{m1} + g_{m2}) \frac{r_{o3}}{r_{o3} C_{PS} + 1} + 1} \\
 &= \frac{\Delta g_m R_D (r_{o3} C_{PS} + 1)}{(R_D C_{LS} + 1) [(g_{m1} + g_{m2}) r_{o3} + r_{o3} C_{PS} + 1]} \\
 &= \frac{1}{(g_{m1} + g_{m2}) r_{o3} + 1} \times \frac{\Delta g_m R_D (r_{o3} C_{PS} + 1)}{(R_D C_{LS} + 1) \left[\frac{r_{o3} C_{PS}}{(g_{m1} + g_{m2}) r_{o3} + 1} + 1 \right]} \\
 \text{高频时} &= \frac{\Delta g_m R_D}{(g_{m1} + g_{m2}) r_{o3} + 1} \times \frac{1}{R_D C_{LS} + 1} \times \frac{r_{o3} C_{PS} + 1}{\frac{r_{o3} C_{PS}}{(g_{m1} + g_{m2}) r_{o3}} + 1}
 \end{aligned}$$

$$\therefore A_{DM} = \frac{g_m R_D}{(1 + \frac{s}{\omega_{in}})(1 + \frac{s}{\omega_{out}})}$$

\therefore 共模抑制比 $CMRR = \frac{A_{DM}}{A_{CM-DM}}$ 随频率升高而下降

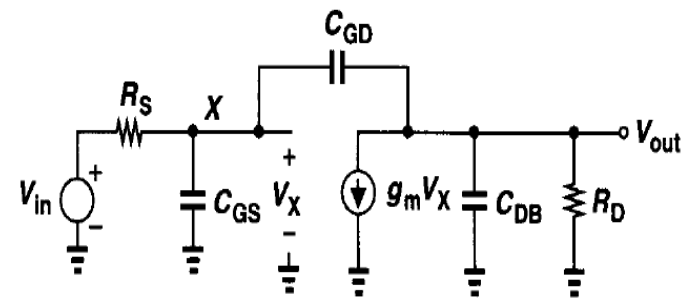
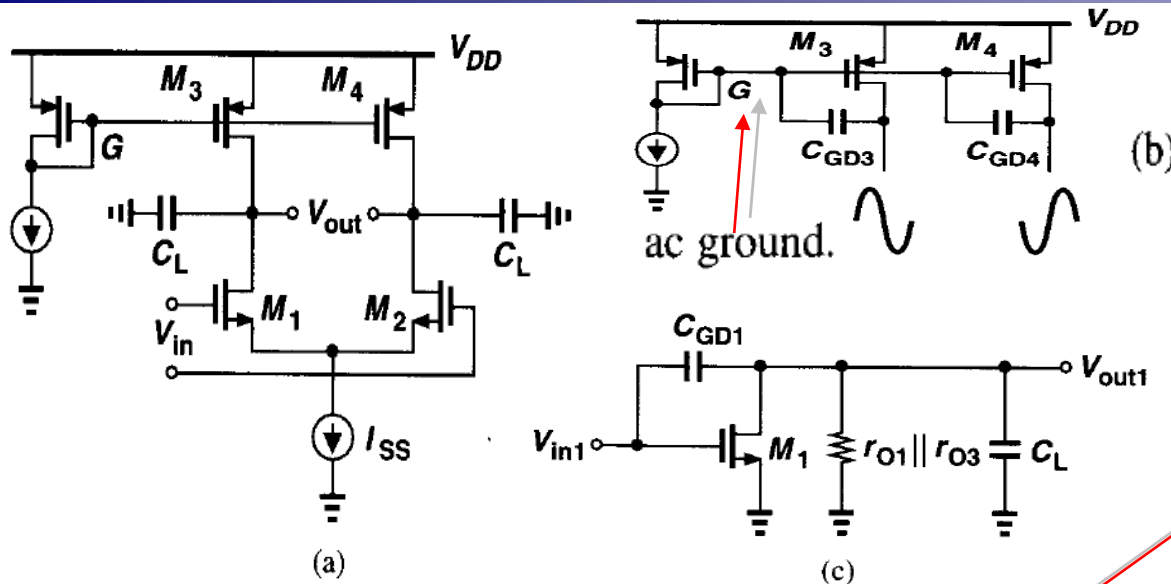


Figure 6.12 Equivalent circuit of Fig. 6.10.

Figure 6.29 (a) Differential pair with current-source loads, (b) effect of differential swings at node G , (c) half-circuit equivalent.

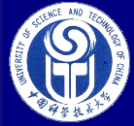
$$\text{Eq. (6.23)} \quad \frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD} s - g_m) R_D}{R_S R_D s^2 + [R_S (1 + g_m R_D) C_{GD} + R_S C_{GS} + R_D (C_{GD} + C_{DB})] s + 1}$$

$$R_S = 0, R_D = r_{O1} \parallel r_{O3}$$

用 $C_L = C_{GD1} + C_{DB1} + C_{GD3} + C_{DB3}$ 替换公式中 C_{DB} , C_{GD3} 替换 C_{GD}

high value of $r_{O1} \parallel r_{O3}$ makes the output pole, given by $[(r_{O1} \parallel r_{O3}) C_L]^{-1}$, the “dominant” pole.

“单” 极点(不考虑输入极点时)



differential pair with active current mirror

contains two signal paths with *different* transfer functions.

The path consisting of M_3 and M_4 includes a pole at node E , approximately given by g_{m3}/C_E , where C_E denotes the total capacitance at E to ground. This capacitance arises from C_{GS3} , C_{GS4} , C_{DB3} , C_{DB1} , and the Miller effect of C_{GD1} and C_{GD4} .

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

severe trade-off between g_m and C_{GS} of PMOS

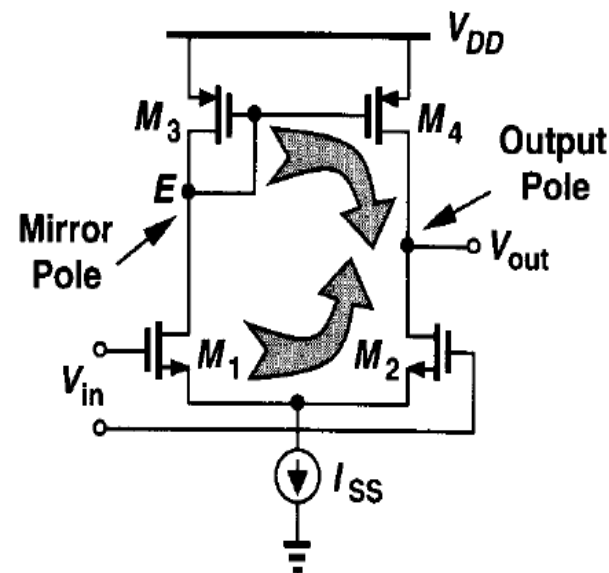


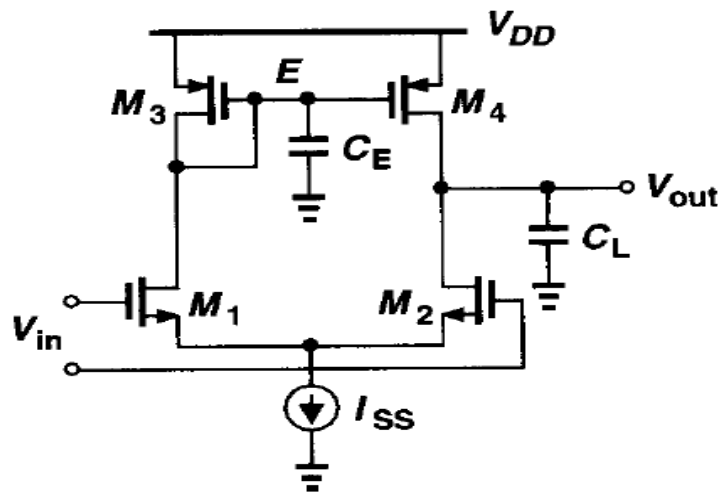
Figure 6.30 High-frequency behavior of differential pair with active current mirror.

The pole associated with node E is called a “mirror pole.”

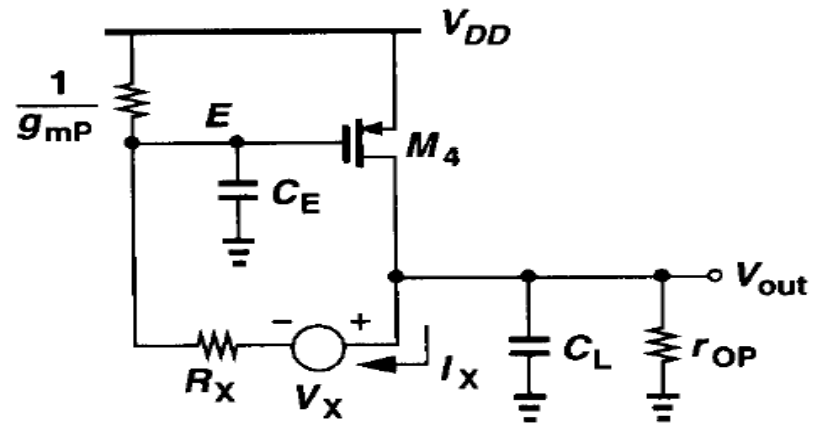
有源电流镜负载放大器不是标准的全差分电路；
非全差分电路不能利用半边电路获得传递函数。



电流镜负载差动放大器的频率响应



(a)



(b)

Figure 6.31 (a) Simplified high-frequency model of differential pair with active current mirror, (b) circuit of (a) with a Thevenin equivalent.

from the analysis of Fig. 5.26, $V_X = g_{mN} r_{ON} V_{in}$ $R_X = 2r_{ON}$.

Here, the subscripts P and N refer to PMOS and NMOS devices, respectively.

assumed $1/g_{mP} \ll r_{OP}$

small-signal voltage at E

$$V_E = (V_{out} - V_X) \frac{\frac{1}{C_{ES} + g_{mP}}}{\frac{1}{C_{ES} + g_{mP}} + R_X}$$

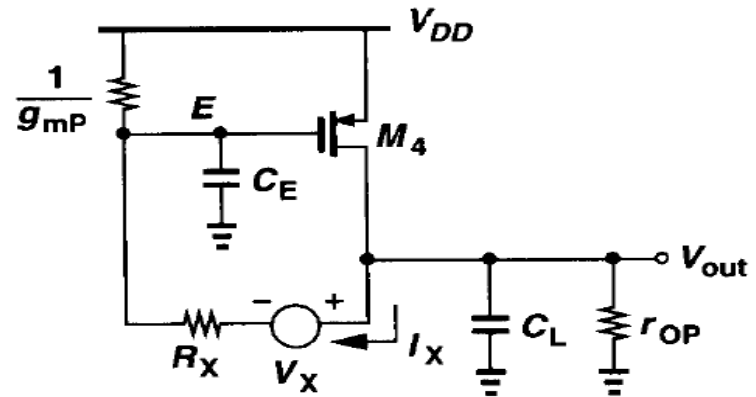


带电流镜负载差动对的频率特性(续)

the small-signal drain current of M_4 is $g_{m4} V_E$.

$$-g_{m4} V_E - I_X = V_{out}(C_L s + r_{OP}^{-1})$$

$$I_X = V_E (g_{mP} + sC_E)$$



$$\rightarrow \frac{V_{out}}{V_{in}} = \frac{g_{mN} r_{ON} (2g_{mP} + C_E s)}{2r_{OP} r_{ON} C_E C_L s^2 + [(2r_{ON} + r_{OP}) C_E + r_{OP} (1 + 2g_{mP} r_{ON}) C_L] s + 2g_{mP} (r_{ON} + r_{OP})} \quad (6.74)$$

Since the mirror pole is typically quite higher in magnitude than the output pole, ($g_{mP} * r_{OP} \gg 1$)

utilize the results of Eq. (6.25) $\frac{s^2}{\omega_{p1}\omega_{p2}} + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)s + 1$ assuming $2g_{mP} r_{ON} \gg 1$

$$\rightarrow \omega_{p1} \approx \frac{2g_{mP} (r_{ON} + r_{OP})}{(2r_{ON} + r_{OP}) C_E + r_{OP} (1 + 2g_{mP} r_{ON}) C_L} \approx \frac{1}{(r_{ON} \parallel r_{OP}) C_L} \quad (6.76)$$

$$\omega_{p2} \approx \frac{g_{mP}}{C_E} \quad \text{which is also expected.} \quad \text{零点 } \omega_{ZX} = \frac{2g_{mP}}{C_E}$$



带电流镜负载差动对的频率特性(续)

- 根据零极点,得
$$\frac{V_{out}}{V_{in}} = \frac{A_0(2 + s/\omega_{p2})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}$$
$$= \frac{A_0}{1 + s/\omega_{p1}} \left(\frac{1}{1 + s/\omega_{p2}} + 1 \right)$$

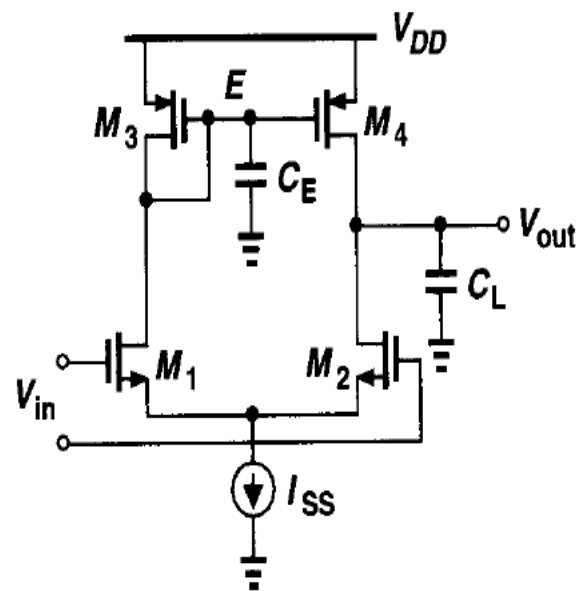
- 左平面零点的作用:

电路由慢通路(M1、M3和M4)和快通路(M1和M2)并联(信号相加)组成。

快通路: $A_0/(1 + s/\omega_{p1})$

慢通路: 带宽有所缩小 $A_0/[(1 + s/\omega_{p1})(1 + s/\omega_{p2})]$

带电流镜负载的差动对:
具有镜向极点的缺点。





Example 6.9

Not all fully differential circuits are free from mirror poles. Fig. 6.32(a) illustrates an example, where current mirrors M_3 - M_5 and M_4 - M_6 “fold” the signal current. Estimate the low-frequency gain and the transfer function of this circuit.

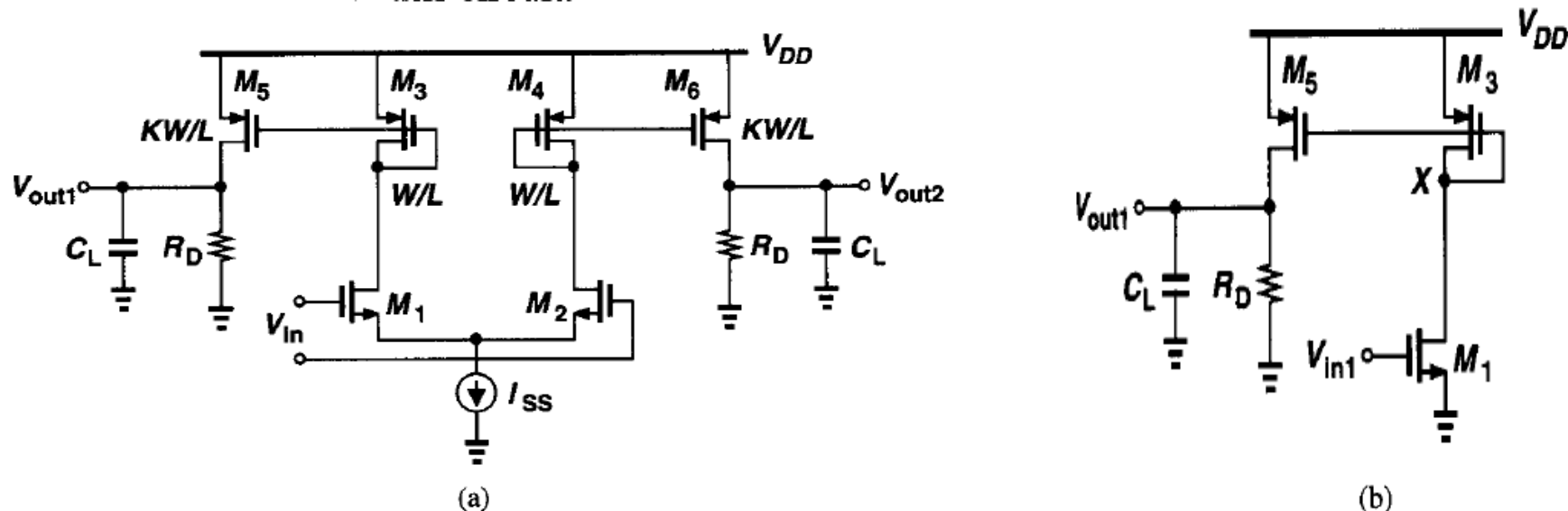


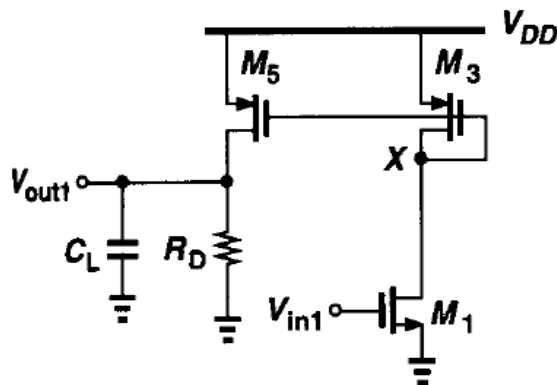
Figure 6.32

differential half-circuit

an overall low-frequency voltage gain $A_v = g_{m1} K R_D$



Example 6.9 (cont.) transfer function



(b)

思路: $\frac{V_{out1}}{V_{GS1}} = \frac{V_{out1}}{V_X} \times \frac{V_X}{V_{GS1}}$

$$\frac{V_{out1}}{V_X}(s) = -g_{m5}R_D \frac{1}{1 + R_DC_Ls}$$

$$\frac{V_X}{V_{GS1}} = -g_{m1} \frac{1}{g_{m3} + C_Xs}$$

$$C_X \approx C_{GS3} + C_{GS5} + C_{DB3} + C_{GD5}(1 + g_{m5}R_D) + C_{DB1} + C_{GD1} (?)$$

Note that we have neglected the zero due to C_{GD5} .