

A 27-29.5GHz 6-Bit Phase Shifter with 0.67-1.5 degrees RMS Phase Error in 65nm CMOS

Qin Duan³, Zhi-Jian Chen^{1*}, Fengyuan Mao¹, Yu Zou¹, Bin Li¹, Guangyin Feng¹, Yanjie Wang¹, Xiao-Ling Lin²

¹ School of Microelectronics, South China University of Technology, Guangzhou, Guangdong, 510640, China

² Electronic Product Reliability and Environmental Testing Research Institute, Guangzhou, 510610, China

³ Guangzhou Haige Communications Group Incorporated Company, Guangzhou, 510663, China

Email: chenzhijian@scut.edu.cn

Abstract-A 27-29.5GHz 6-bit switch-type phase shifter (PS) using 65nm CMOS process is presented in this paper. The PS incorporates 6 series phase shift bits to realize the relative phase shift varying from 0° to 354.375° with a step of 5.625°. Novel design approaches for phase shift bit and bits cascading sequence are proposed to improve the bandwidth and the RMS phase error. The post-layout simulation results show that the PS exhibits an ultra-low RMS phase error of 0.67°-1.5° and RMS gain error of 0.63dB-0.8dB from 27GHz to 29.5GHz. The input and output return loss are both better than -10dB and the core size is 0.90×0.35 mm².

Keywords—phase shifter, CMOS, bandwidth, RMS phase error, RMS gain error

I. INTRODUCTION

Due to the lower latency, higher data rates and improved link robustness, the fifth-generation (5G) wireless communication technology is developing rapidly these days [1]. At present, one of the most challenging aspect of 5G technology is the vulnerability of millimeter-wave signals to the weather and obstacles. Therefore, the beamforming technology with a phased-array which steers and focuses the radio wave to a desired direction attracts many attentions recently [2]. Several millimeter-wave phased-array transceiver (TRX) integrated circuits (ICs) were presented in the past few years [3-4], exhibiting an excellent radiated performance and compact integration potential. Phase shifter is an indispensable module in phased-array to control the phase of wave in each TRX element. It can be designed in the RF front-end (RFFE), baseband (BB) or local oscillator (LO) modules, as shown in Fig.1. The trend to compactly integrate more elements in a phased-array transceiver makes passive RF phase shifter more attractive due to its simplicity. In addition, digital control PS helps to reduce complexity compared to analog PS which requires AD/DA converters or other more complex modules. Usually, RMS phase error and gain error are the main index to evaluate the performance of PS. Several digital control PSs were reported for phased-array applications in [5-7], but the RMS phase error was rarely less than 1°, and the detailed improvement methods of RMS error were rarely mentioned.

In this paper, a 27-29.5GHz 6-bit switch-type passive phase shifter is designed with 65nm CMOS process for

implementing complex 32- or 64-element phased-array IC. To lower the RMS phase error and gain error, some novel and effective design methods are proposed and analyzed for both phase shift bit and the cascade. In section III, the results of post-layout simulation exhibit an ultra-low RMS phase error of 0.67° - 1.5° and RMS gain error of 0.63-0.8 dB across the working band.

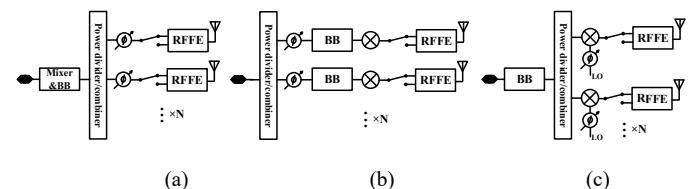


Fig. 1. Three types of implements of the phase shifting: (a)RF phase shifting, (b) baseband phase shifting and (c) LO phase shifting

II. CIRCUIT DESIGN

A. 5.625°Phase Shift Bit

A small relative phase shift can be simply implemented by a single inductor and bypass switch, as shown in Fig.2, which is usually used as a 5.625° phase shift bit. When the MOSFET switch is on, the input and output are shorted by a small parasitic resistance R_{on} and experiences no phase shift (reference state). When the switch is off, the signal passes through the series inductor with small phase lagging (phase shifting state). To improve the insertion loss, a several k-ohm body-float resistance R_B is introduced and a wide transistor is used to lower R_{on} .

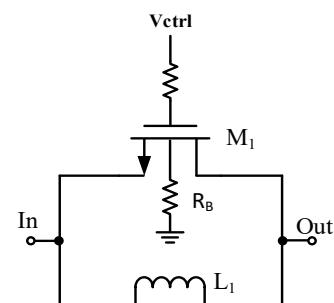


Fig. 2. The schematic of a 5.625° phase shift bit.

B. 11.25° , 22.5° and 45° Phase Shift Bit

It is difficult for a single inductor to provide sufficient phase lagging and maintain acceptable loss simultaneously, because a large series inductance inevitably leads to high return loss. Therefore, a π -network low-pass filter (LPF) is preferable and is chosen to realize the bidirectional impedance matching, as shown in Fig.3 (a), which is usually used as a 11.25° , 22.5° or 45° phase shift bit. The traditional design approaches are as follow: in reference state, the M_2 is on and M_{X2} is off respectively. The inductor L_{X2} is adjusted to resonate with parasitic capacitor C_{off} at center frequency to create a high impedance seen at the node X, and therefore the signal is shorted by R_{on} with no two-port phase shift, as shown in Fig.3 (b). In phase shifting state, as shown in Fig.3 (c), the M_2 is off and M_{X2} is on. The signal is delayed when passing through the π -network LPF. Fig.4 (a) shows the two-port phase shift simulation results of 45° bit in different state. It can be seen that the 45° relative phase shift can only be realized accurately at 28GHz. The bandwidth is greatly limited due to the different slope of two curves, where the slope of two-ports phase at a certain frequency can be written as:

$$K_p = \frac{d\phi}{df} \quad (1)$$

What's worse is that Fig.4 (b) presents a large gain error during state switching because the loss caused by R_{on} in the reference state is much lower than the loss caused by low-pass filter in the phase shift state. Therefore, remaining the K_p and loss constant in different states are desired to increase the bandwidth and lower the gain error.

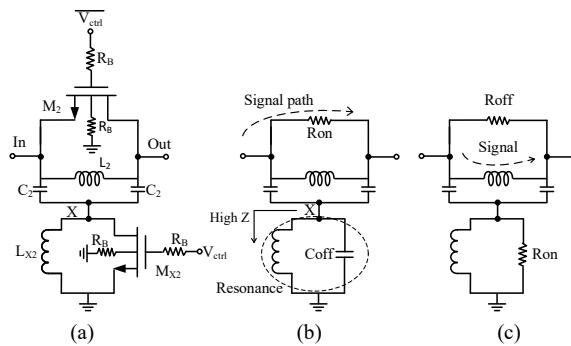


Figure 3. the schematic of a 11.25° , 22.5° or 45° phase shift bit: (a) the schematic, (b) the equivalent circuit in reference state (c) the equivalent circuit in phase shifting state

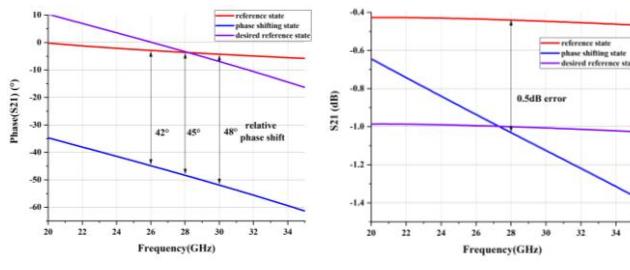


Fig. 4. The two-port S-parameter simulation results of 45° bit in different state.
(a) two-port phase shift simulation. (b) S21 simulation

Fig.5 shows the solution. In reference state, the inductor L_{X2} is chosen to resonate with C_2 slightly below the working frequency so that the second signal path can be generated to create negative K_p . The K_p can be adjusted by moving the resonance frequency so as to fit the K_p in phase shifting state, as shown in Fig.6. Since L_{X2} is no longer chosen to resonate with C_{off} , the high impedance seen at node X vanishes and thus the signal experience higher loss in reference state.

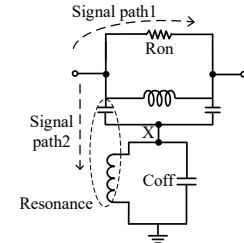


Fig. 5. The equivalent circuit of optimized 45° bit in the reference state.

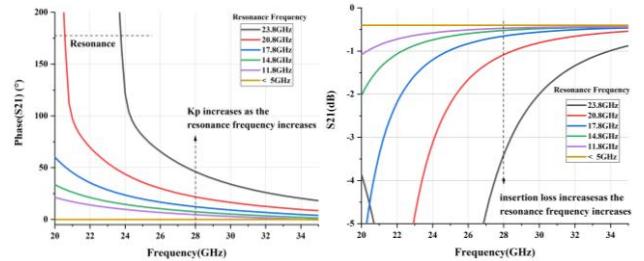


Fig. 6. The two-ports S-parameter simulation results of the optimized 45° bit in the reference state. The K_p and the loss can be changed by moving the resonance frequency.

C. 90° and 180° Phase Shift Bit

To achieve larger relative phase shift, a T-network high-pass filter is incorporated in reference state to create leading, as shown in Fig.5, which is usually used as a 90° or 180° phase shift bit. The wave experiences leading and lagging when switching the states and thus a large relative phase shift can be generated. Additionally, the K_p in reference state can be readily adjusted by the high-pass filter to fit the K_p in phase shift state.

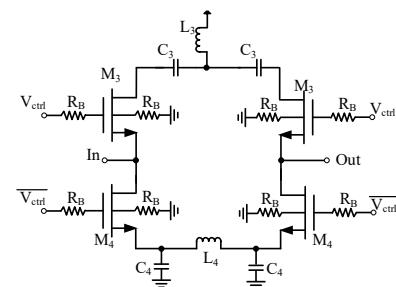


Fig. 7. The schematic of 90° or 180° phase shift bit.

D. Phase Shift Bits Cascading

The main difficulty of phase shift bit cascading is to realize a low RMS phase error. Due to the loading effect, the relative

phase shift of a single bit is affected by the state of other bits. Take the cascade of 45° and 90° phase shift bits with 2° offset as an example, when the latter is in the reference state, the actual relative phase shift of former may be accurate 45° , but when the latter is switched to the phase shift state, the actual relative phase shift of former may be offset to 47° . This kind of error is inevitable because ensuring a constant impedance during the state switching is unrealistic. Additionally, this error will accumulate as the number of bits increases and greatly deteriorates the accuracy.

To reduce RMS phase error, some errors can be deliberately introduced when designing the phase shift bit. Quoting the above example (2° offset), the actual phase shift value of former can be design as 44° when the latter is in the reference state. When the latter is switched to the phase shift state, the actual phase shift value will be offset to 46° , which apparently lowers the RMS phase error, as shown in Table I.

TABLE I RMS CALCULATIONS OF 2-BIT PS WITH 2° OFFSET

	Reference phase (deg)	Phase(deg) before optimization	Phase(deg) after optimization
State 0	0	0	0
State 1	45	45	44
State 2	90	90	90
State 3	135	137	136
RMS error	0	1	0.5

III. LAYOUT AND SIMULATIONS

After iterations, the cascade sequence of 6 phase shift bits is finally determined as 180° bit, 5.625° bit, 11.25° bit, 45° bit 22.5° bit and 90° bit, and the final layout of the PS is shown in Fig.8.

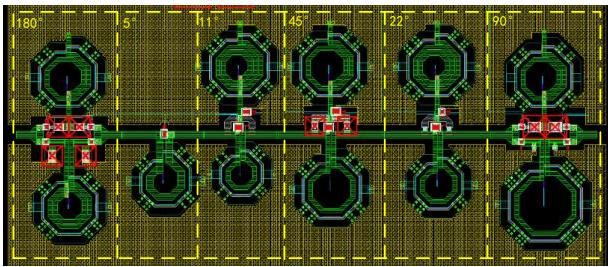


Fig. 8. The Final Layout of the Proposed Phase Shifter

The transmission lines and dummy layer are simulated with electromagnetic simulation tool. The transistor models based on measurement are provided by process design kit. The EM simulations are performed to obtain accurate simulation results. Fig.9 represents the simulation results of two-port phase shift and S_{21} over 64 states. The simulated results of RMS phase error and the RMS gain error at 28GHz is shown in Fig.10, which is 0.67° and 0.63 dB, respectively. The average gain of 64 states is -8.3 dB and the maximum gain variation is 2.7 dB at 28GHz.

The results of input and output return loss over 64 states are shown in Fig.11. The S_{11} and S_{22} are better than -10 dB in the working frequency range of 26-30GHz.

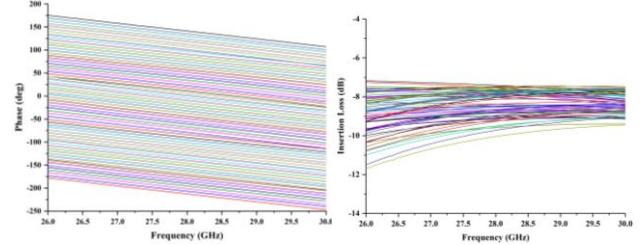


Fig. 9. The simulation results of the two-port phase shift and the insertion loss over 64 States.

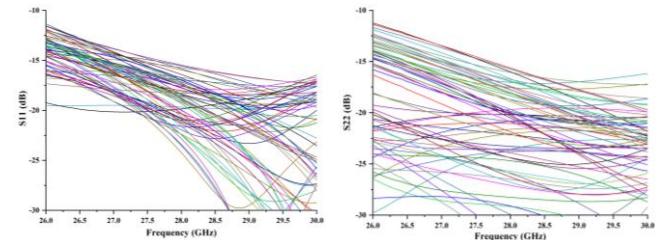


Fig. 10. The simulation results of the return loss over 64 states

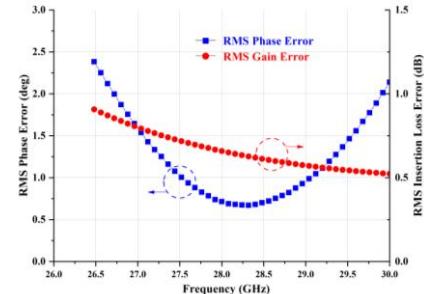


Fig. 11. The simulation results of RMS phase error and gain error

IV. CONCLUSION

A 27-29.5GHz 6-bit switch-type phase shifter designed with 65nm CMOS process is presented in this paper. With the optimization of phase shift bits and bits cascading sequence, the proposed phase shifter realizes an ultra-low RMS phase error of 0.67° - 1.5° and RMS gain error of 0.63 - 0.8 dB in a frequency band of 27-29.5GHz. The input and output return loss are better than 10 dB over 64 states. Table II summarizes the performance comparison of switch-type phase shifters.

TABLE II. PERFORMANCE SUMMARY AND COMPARISON

	[2]	[5]	[7]	This work
Process	65nm CMOS	0.18um SOI	0.18um SOI	65nm CMOS
source	Simulation	Measure	Measure	Simulation
Freq(GHz)	26.5-29.5	5-6	25-31	27-29.5
Gain (dB)	-7	-4.8	-6.5	-9

RMS Phase error (deg)	1.5-3	10	1.2-1.8	0.67-1.5
RMS MAG error (dB)	NA	0.4	0.4-0.6	0.63-0.8
Chip Size (mm ²)	NA	1.03	0.53	0.32

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