GaN MMIC Differential Multi-function Chip for Ka-Band Applications

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***Abstract*— High data rate communications have become possible due to improvements in microelectronics, and is based on new topological concepts of architecture. The development of 5G networks using the Ka-band is one of the challenges for new telecommunication systems based on individually controlled active antennas (AESE). The control system is usually developed using silicon processes but this approach does not allow a fully embedded transceiver as the front-end module must be connected to the core-chip module and to its digital control interface. With the GaN power technologies providing high PAE, an interesting issue consists in designing a fully integrated GaN MMIC multi-function chip for highly integrated systems. This work presents, for the first time, a GaN attenuator-phase shifter covering a wide range of frequencies from 30 GHz to 40 GHz. Moreover, this circuit is a balanced version of the attenuator-phase shifter to target an improved linearity and to take full advantage of GaN power amplifiers.**

***Keywords*— attenuator, Gallium Nitride, Ka-band, MMIC phase shifter, quadrature amplitude modulation (QAM).**

I. Introduction

The design of attenuator and phase shifter circuits is usually developed in SiGe and CMOS technologies for their high performance and high integration advantages over III-V technologies. Nevertheless, the permissible power level of these circuits does not exceed 20dBm, thus the power gain necessary to compensate interconnections losses quickly become more difficult to reach, especially in the Ka-band. In contrast, III-V technologies can overcome this drawback at the circuit level by making possible a higher integration level when embedded with the power module and switches of the front-end [1]. Moreover due to their higher permissible power level when using GaN technologies, the required gain of power amplifier is less important. This subsequent solution allows the implementation of a single chip with a full monolithic design, with Serial Input Parallel Output Interface developed on the same chip (i.e. normally-on and normally-off devices to drive the attenuator and phase shifter states)[2]. Next generation solid state GaN devices offer reduced surface chip for a given output power due to a better drain current, a higher breakdown voltage and junction temperature. Then, the step for phase array systems (used in radar and electronic warfare, but also future telecommunication systems) is to provide these technologies with such embedded attenuator – phase shifter circuits, next designed as 'core-chips' or multi-functions chip (with fully integrated module when enhanced and depletion mode transistors are available). This work is focused on a large bandwidth demonstrator (30 GHz-40 GHz), using a differential structure to improve the linearity of the circuit since this one will be located directly before (or possibly from part to part of) the power amplifier. This work makes use of electrical and EM simulations to secure the design of each cell, and then of the full 11-bit (5 attenuation states, 6 phase-shift states).

Following this introductory paragraph, the second section presents the individual architecture of each cell composing the 11-bit core-chip. Since the initial requirements are stringent (up to 30% bandwidth, inter-stage matching and error functions reduction over the targeted frequency band), the design procedure is presented. The third section presents the measured MMIC chip, digitally controlled by Arduino to set the 2048 states. The constellations associated to a frequency range are discussed in section IV. A conclusion defines the trade-off on the modulation schemes regarding the targeted bandwidth: for a large one (29%), or a reduced one (11%) centered on 35 GHz. Different alternatives of design (single-ended version) are introduced (and discussed in the final version), also considering the linearity of these GaN digitally controlled circuits.

II. Core-Chip Design and Simulation

This work has been motivated by the OMMIC corporation in the race of GaN circuits and systems towards high frequencies, and specifically the Ka-band. The portfolio of OMMIC provides the users with many GaN modules, mainly dedicated to power amplifiers, but also robust low-noise amplifiers, and now evolves towards new functions such as core-chips to propose a large variety of circuits that can be embedded on a single chip (featuring overall smaller areas as it overcomes bonding on RF, DC and/or control states).

The stringent specifications are given below:

-bandwidth from 30 GHz to 40 GHz
-dynamic attenuation range larger than 15dB
-dynamic phase shift between 0°-360°
-attenuator and phase shift errors as low as possible (according to the number of used bits as discussed in section III).

Specifically, each cell has to be matched at its input and output port (less than 15 dB); this makes it complicated to accommodate performances (S_{ij}) and matching conditions (S_{ii}) over such initially defined large bandwidth. This issue has been considered as specific keypoint during our design procedure, but will be addressed in another paper.

As previously stated, GaN transistors are excellent options for analog high frequency power modules. However, the large surface area (in comparison with vertically stacked Heterojunction Bipolar Transistors in BiCMOS processes) introduce phase shifts that have to be carefully accounted for.

The core-chip under consideration is composed of 11 different cells, and the fulfillment of the system's specifications needs an objective procedure during the design steps as given below:

1)-Ideal topology analysis (best situation case) using only GaN transistors from OMMIC's design kit D01GH, and lumped elements. The HEMT devices feature 100 nm gate length, with various gate development (number of gate fingers and gate width). Applicability to the targeted frequency band 30-40 GHz and performance/matching management. These simulation results establish minimum achievable errors.

2)-Simulation of the cell using real electrical model of the reactive elements, followed by minimization of errors in the design layout; the sensitivity of non-symmetrical parts of the circuit is considered to lower the common mode conversion.

3)-EM simulations to validate the electrical design and to reduce the risk factor during the design steps when including real elements and lines (same procedure for each of the 11 cells)

4)-Global electrical and EM simulations. The organization of cascaded cells for reduction of errors is also considered (management of mismatch and performances interactions for 11 factorial possible organizations of the 11-bit core-chip). This strategy has been used for single ended design (discussion in section IV).

Examples of ideal topologies are given as an illustration for the 5 attenuators and for the 6 phase shifters in Fig. 1.

The 6-bit phase shifter and 5-bit attenuator is designed for an ultimate target resolution of 5.625° and 0.5dB for this 11-bit configuration. However, as discussed in the next section, this generic Ka-band GaN MMIC core-chip can be used for multi-purpose applications, with the knowledge that there is a trade-off between frequency range and modulation scheme complexity (the larger the frequency band, the lower the quadrature-amplitude modulation complexity).

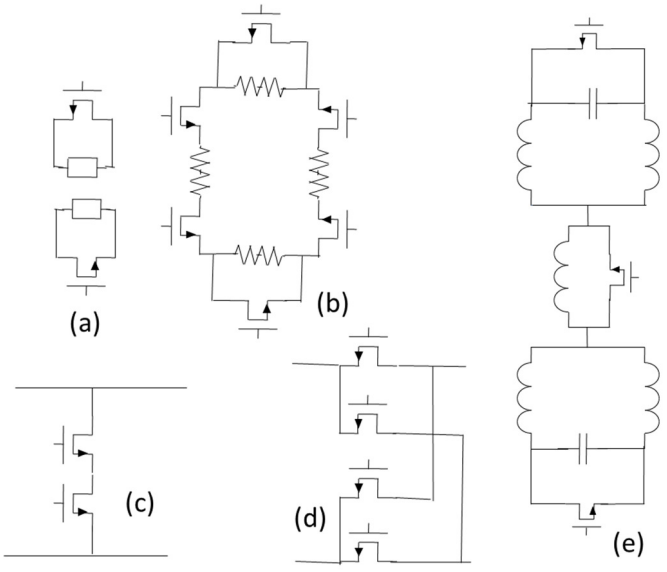

Fig. 1. ideal topologies for Phase Shifters (a)delay line 5,5°, (d)quad-switch 180° and (e)switched filter 11,25°, 22.5°, 45° and 90°) and Attenuators (c)loaded line 0.5dB and 1dB,(b)π-resistive network 2db, 4dB,and 8dB.

Fig. 2a depicts the simulated constellation of phase and attenuation making use of the 11-cells of the core-chip, centred at 35 GHz. The good global coverage can be appreciated and becomes even more difficult to achieve with increasing frequency band. For balanced S-parameter simulations, the common-mode and differential-mode have been investigated, and prior to any design analysis, the simulation environment has been validated by using two methods; the mathematical formalism can be found in [3] and correlates with the simulation setup dedicated to our measurements, based on the application note form Keysight [4]. Moreover, if the targeted phase errors (resp. attenuation errors) must be considered as first order parameters during the design of the phase shifter (resp. attenuator), it must be highlighted the necessity to also consider, in turn, the impact of attenuation (resp. phase) variations for the overall RMS of the core-chip. Fig. 2b presents the RMS errors over the 30 GHz – 40 GHz frequency band. A reduced attenuation error is obtained between 33-37 GHz (below 1 dB), while a degradation occurs for the larger frequency band (30-40 GHz) up to 1.5 dB.

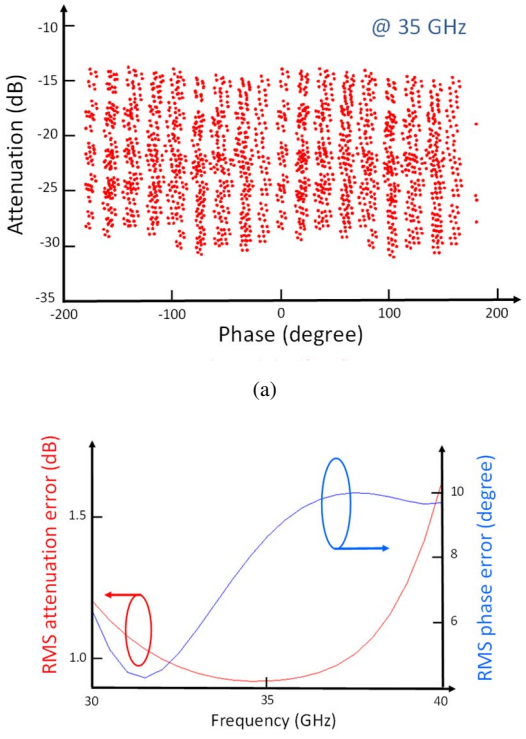

Fig. 2. (a) EM simulations of the 11-bits balanced core-chip (2048 states) (b) RMS attenuation and phase errors from 30 GHz to 40 GHz.

The constellation from the multi-function chip, as illustrated in Fig. 2, can be used at various frequencies to change the pattern of a multiple-antenna system (such as phase arrays).Such a multi-function circuit can be used to emulate any phase shift and amplitude constellation over a wide frequency band; the control of the switches within the 11-cell module can be achieved by using enhancement depletion technology as provided by the D01GH foundry.

This degraded RMS errors explains the reduced pattern size when increasing the frequency band as explained in the next section. Despite of the phase shift RMS non-centred profile, it can be stated that an advantage is taken from the 6-bit phase-shifter coverage to realize the phase shift and attenuator states according to the desired frequency bandwidth (i.e. 30 GHz-40 GHz 16-states, and 33 GHz-37 GHz 64 states).

III. Core-Chip MMIC

An image of the Ka-band GaN core-chip is depicted in Fig.3. The circuit is externally driven: bonding wires are used for electrical connection of the MMIC to an external PCB (gate control biasing). Dedicated software has been developed on an Arduino to set the 2048 different states of the core-chip.

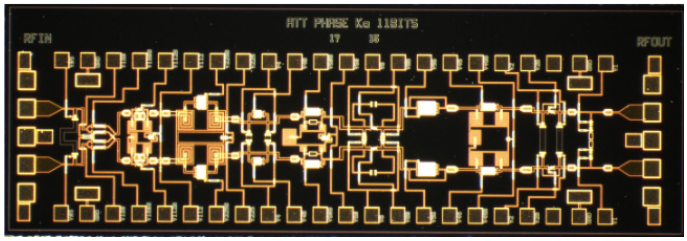

Fig. 3 Image of the GaN Ka-band Core-chip featuring 11 digitally controlled states (6 phase shifters and 5 attenuators)

The MMIC is positioned on an epoxy-PCB secured with an electrically conductive adhesive, the connections between the chip and the PCB bias tracks are ensured by bonding wires. GSGSG probes are used to measure the four port single-ended S-parameter of the MMIC, leading to the extraction of the balanced S-parameters by using the mathematical analysis developed in [3]. Measurements are done using the Keysight N5247A four-port PNA-X Microwave Vector Network Analyser. Calibration is performed using SOLT correction method. The phase (resp. attenuator) accuracy is better than 0.5° (resp. 0.1dB) over the considered frequency range.

The digital control of the 11 cells constituting the core-chip (2 transistors per cell) is performed by an Arduino module driven by a computer.

IV. Trade-Off Between Modulation Scheme and Frequency-Band

A. *64-states pattern between 33 GHz and 37 GHz*

The pattern presented in Fig.4 makes use of the complete characterization using the 11-bit facilities (i.e. 2048 states represented by blue dots). Some white regions indicate that the least significant bits do not allow an accurate coverage of the pattern using a full 11-bit definition. Nevertheless, the least significant bits can be used as fine adjusting parameters to match the core-chip coverage according to the desired pattern: Fig. 4 illustrates the possibility to implement a 64-QAM pattern with the designed core-chip (red symbols). This pattern is still efficient between 33 GHz and 37 GHz (i.e. 11% bandwidth), with 18 dB dynamics for the attenuation (by step of 2.4 dB), and 360° coverage (by step of 45°).

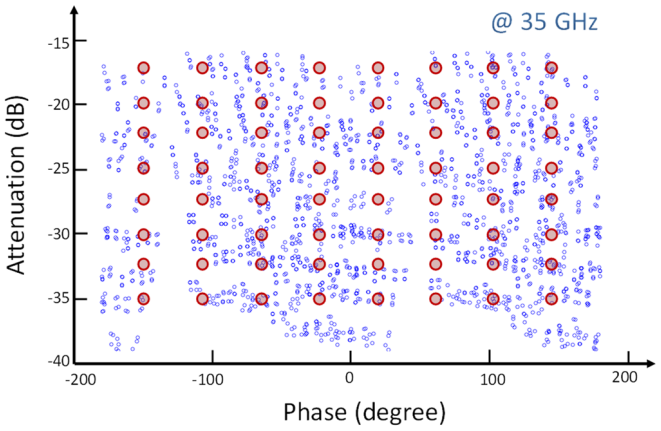

Fig. 4. Measured core-chip pattern of the GaN-MMIC circuit @ 35 GHz, with evidence of a 64-states pattern (red circles, 8x8 states). This constellation is valid between 33 GHz and 37 GHz. Blue dots are related to the 11-bits pattern featuring 2048 states.

B. *16-states pattern between 30 GHz and 40 GHz*

For an increased bandwidth up to almost 30% (still centred at 35 GHz), unsurprisingly the constellation coverage degrades.

Nevertheless, a 4x4 pattern can be used for a 16-states as proposed in Fig. 5. As the area of blue dots (i.e. 2048 states

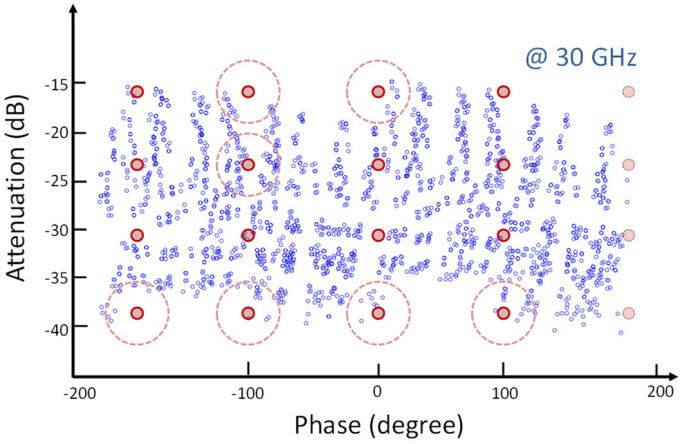

Fig 5. Measured core-chip pattern of the GaN-MMIC circuit @ 30 GHz, with evidence of a 16-states pattern (red circles, 4x4 states). This pattern is valid between 30 GHz and 40 GHz. Blue dots are related to the 11-bit pattern featuring 2048 states. Red dashed circles feature the area where the symbol still applies for 16-states for critical situations with low availability of blue dots, and without producing error of symbol. Symbols on the right part (360°) are already synthetized on the left part (0°)

from the 11-bits full characterization of the core-chip) is less patterned than that presented in Fig. 4, the use of least significant bits can help in providing symbols at the vicinity of the red symbols (as illustrated by the dashed circle area for the most critical situations in Fig. 5). The dynamic in attenuation is still of 18 dB at 30 GHz and at 40 GHz (step of 7 dB), while the 360° angle coverage is synthetized by steps of 90°.

C. *Comparison with single ended version*

Other GaN core-chips have been designed, such as a single-ended version, still in the Ka-band and based on a different procedure of design. This design is optimized for reduced RMS errors at 35 GHz, and takes advantage of the organization of the 11-cells to improve the performances of the overall circuit (step 4 from the procedure). This second circuit is currently in fabrication. The simulated constellation at 35 GHz, illustrated in Fig. 6, shows better repartition of phase and attenuation than that presented in Fig. 2a.

D. *Linearity*

Moreover, linearity simulations and measurements have been performed at 30 GHz, 35 GHz and 40 GHz on the balanced topology depicted in Fig. 3.

From simulation at the device level, compression point features variable output power with the sizing and the biasing of the device, with lowest power simulated at 10 dBm input compression point (common gate configuration, 1 finger of 15 µm gate length). It must be noticed that the topology (serial or shunt device) plays a strong role in the linearity of the circuit (individual cell and final chip). The shunt topology allows higher power levels than what the device can handle alone, like for SPDT series-shunt topologies [5]. This last point releases constraints on sizing versus power for the transistors from first stages of the core-chip.

From measurements, input power up to 25 dBm is applied to the device in single ended configuration. After calibration steps and with 3 dB correction using the balanced configuration, the linearity is still observed at 30 GHz, 35 GHz and 40 GHz over the power sweep. Thus, we assume that our Ka-band multi-chip circuit can handle input powers higher than 28 dBm. Dedicated high power (balanced) driver amplifier is needed to verify the linearity limitation of our chip, however the achieved performances are largely above the best results based on SiGe technologies at 20.5 dBm [6].

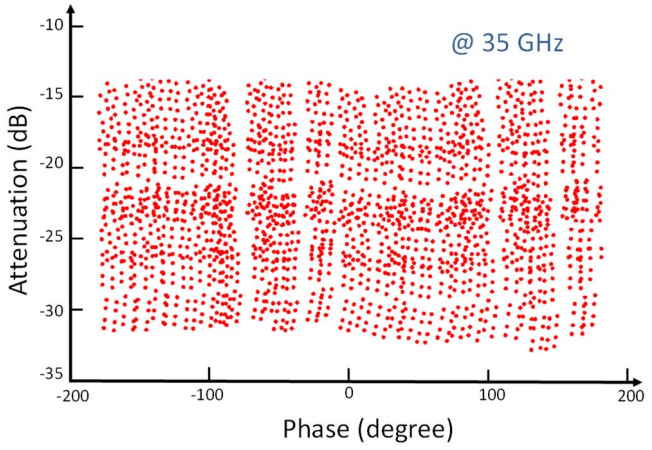

Fig. 6. Simulated constellation of 11-bit single ended core-chip at 35 GHz

Finally, this work demonstrates the feasibility of variable multi-symbols patterns up to 30% bandwidth in the Ka-band, with realistic operable settings.

V. Conclusion

The design of attenuator and phase shifter modules is a key point for new telecommunication or radar applications, as it allows focusing an antenna in a given direction to improve the radio-link budget efficiency, thus allowing the use of higher frequency bands and so the improvement of the data rate. For the first time, this paper demonstrates the feasibility of a MMIC GaN core-chip module that is digitally controlled, over a wide frequency bandwidth up to 30% in the Ka-band. The dynamic is 18 dB in attenuation over 30 GHz and 40 GHz. Measurements have demonstrated that a 64-states pattern can be used from 33 GHz to 37 GHz, while a 16-states pattern still operates for a wider frequency range between 30 GHz and 40 GHz. GaN core-chips can take advantage of the normally-on and normally-off transistor devices to design the digital control circuit of such a system. Then, a fully integrated transceiver module demonstrating high linearity can be developed in the Ka-band using this GaN technology. The integration can largely be improved using these modules for very small surface antennas at such elevated frequencies.

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