A 28 GHz Reflective-Type Transmission-Line-Based Phase Shifter

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***Abstract*— This work presents a 28 GHz reflection type transmission-line (TL) based phase shifter. The proposed architecture employs a completely passive approach to double the phase shift achievable using a TL when compared to conventional architectures. The phase shifter, along with a preceding low noise amplifier and buffer, is implemented in a 65 nm CMOS process. The fabricated chip achieves a measured phase resolution of 11.25° at 28 GHz, with an rms error of 3° and a total phase shift of 180°. The insertion loss of the phase shifter alone is 17 dB. The active area of the entire phase shifter, including LNA and buffer is 0.41 mm^2.**

***Index Terms*— Beamforming, CMOS, 5G cellular communications, rms phase error, low power, low-noise amplifier (LNA), millimetre-wave, reflection-type transmission line phase shifter (RTTLPS), passive phase shifter, capacitive bridge based hybrid coupler, MOS switch.**

I. Introduction

THE next generation of mobile communication demands a higher data rate and bandwidth. There is an immediate need for improved millimeter-wave (mmWave) integrated circuits for 5G cellular communication in the 26.5 GHz to 29.5 GHz frequency band [1]. Atmospheric losses are relatively higher at mmWave frequencies, so electronic beamforming has to be implemented at both the base station and mobile front-ends to provide higher effective isotropic radiated power (EIRP) [2], [3]. The beam needs to be highly directive to point to the desired user. This can be achieved using a combination of an electronic phase shifter with fine resolution and a variable gain amplifier.

To further improve the data rate and spectrum efficiency, a phased array beamformer supporting dual-polarized MIMO has previously been introduced in [4]–[6], with an RF-path bidirectional phase shifter common for both transmit and receive paths, as shown in the representative diagram of Fig. 1. RF-path phase-shifting [7] can be both compact and low power. However, it should provide a variable phase with low gain variation, fine phase shift resolution, fast phase switching speed and low power. If required, the gain variation with phase change can be corrected using DAC based techniques with some area overhead [8]. Since the phase shifter noise and non-linearity directly affect the signal path, a passive phase shifter, which is also bidirectional, is preferred over active ones.

The various types of mmWave phase shifting techniques are illustrated in Fig. 2. These include true-time delay based phase-shifters like 1) switched type passive phase shifter

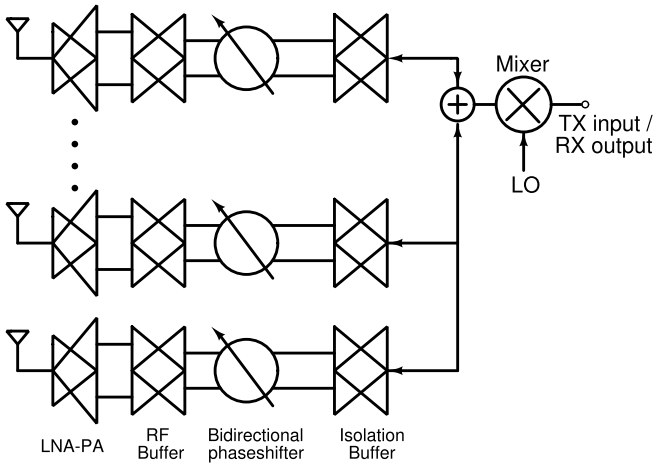

Fig. 1. Block diagram of bi-directional transceiver.

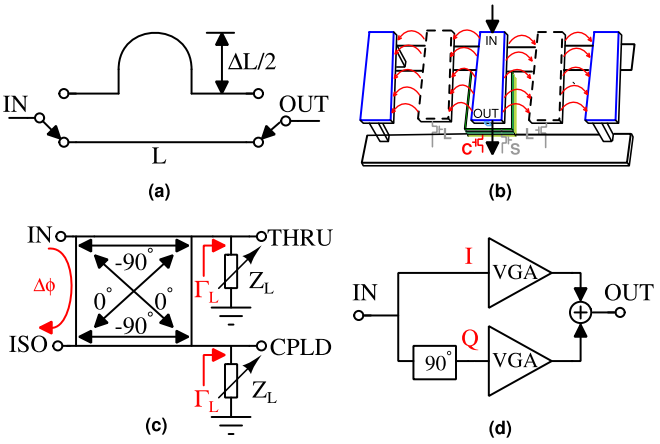

Fig. 2. Types of mmWave phase shifter (a) Basic concept of switched type phase shifter. (b) Basic concept of tunable t-line phase shifter. (c) Reflection type phase shifter. (d) Vector modulator based phase shifter.

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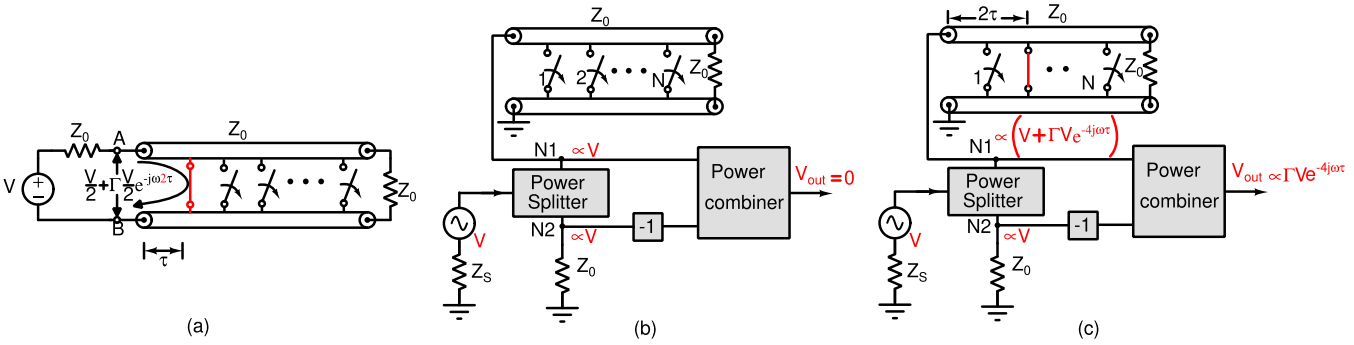


Fig. 3. (a) Basic Concept of switched transmission line phase shifter. (b) Conceptual schematic to get rid of non-delayed signal. No signal appears at the output when all the switches are open. (c) One switches is ON, only the delayed signal appears at the output.

(STPS) (Fig. 2(a)) where the phase of the signal is controlled by switching the different delay paths [9], [10]; 2) tunable TL phase shift is shown in (Fig. 2(b)). Here TL electromagnetic properties are varied using "L" and "C" control bit to provide variable delay [11], [12]; and non-delay based phase-shifters like 3) reflection-type phase shifter (RTPS) achieving phase shift(Fig. 2(c)) by varying the termination impedance for a quadrature 3-dB coupler [13]–[15]; and 4) vector-modulator-based active phase shifter (Fig.2(d)) that use two quadrature signals with different amplitudes to achieve desired phase [16], [17].

In this article, a new reflection-type TL based phase shifter (RTTLPS) is presented, whose delay can be varied using digitally controlled switches. Some of the attractive features of the proposed RTTLPS are given here:

- Phase-shift corresponding to twice the delay of TL is obtained.
- Gain control can be achieved by varying the reflection coefficient.

In this work, a 2-bit DAC (off-chip) is used to reduce gain variation due to loss along the TL during phase-shift by controlling switch resistance (reflection coefficient). Also, we have explored gain tuning in discrete steps by turning ON multiple switches together (which requires only a change in digital logic).

We have designed the phase shifter to cover only 180° phase range as an additional 180° phase change can be achieved by flipping the positive and negative signals in a fully differential design. The paper is organized into six sections. Section II illustrates the proposed phase-shifter architecture followed by implementation details in Section III and IV. Measurement results are discussed in Section V, and Section VI concludes the paper.

II. Proposed Reflection-Type Transmission Line Based Phase Shifter

A. Evolution of the Phase Shifter

TL based phase shifters have been implemented in the past using the following approaches:

- Cascading TLs of different lengths [9].
- Varying the capacitance or inductance of the transmission line [18].

In both of the above approaches, an incident signal is applied at one port of the TL, and the delayed signal is collected at the other end. If reflective termination is used for the TL, then it is possible to use the delay of the TL segment twice, and consequently, the delayed signal appears at the same port as that of the incident signal. The reuse of unit delay elements results in area savings and reduced power consumption in active implementation of the delay line. However, the active approach is accompanied by noise and linearity penalty [19]. Recently, [20] has presented a reflection type true-time-delay element using a variable-order all-pass filter. This is a low-frequency technique where the delay is tuned by controlling the order of the filter.

To avoid any linearity penalties, a completely passive reflection-type transmission line based phase shifter (RTTLPS) is proposed in this work for mmWave beamforming front-ends. There is also an additional motivation to provide a wider operating bandwidth compared to a conventional RTPS. In an RTPS, reflective loads are narrowband in terms of phase as well as group delay. So, even though the coupler used in an RTPS has an ideal wideband response; the phase shift or group delay will be narrowband. The basic concept of the proposed RTTLPS is illustrated in Fig. 3(a). Here, the input signal source is connected to a terminated TL which is periodically loaded with switches. The source impedance and TL termination are the same as the TL characteristic impedance, Z_0. At any time, only one switch in the bank of switches is closed while the rest of the switches are kept in an open state. The total voltage across terminals A-B is given by

$$V_{AB} = \frac{V}{2} + \Gamma\frac{V}{2}\exp(-j\omega 2\tau) \tag{1}$$

where V is the source voltage, Γ is the reflection coefficient at the closed switch, ω is the angular frequency of the signal, and τ is the time delay of the TL from Port A-B to the switch. When the signal is incident at Port A-B, the signal reflected by the closed switch appears at Port A-B after a delay of 2τ while the transmitted signal is absorbed by the termination, Z_0.

The second term in (1) above is a scaled and, more importantly, delayed version of the incident signal. The above-mentioned delay can be controlled by choosing an

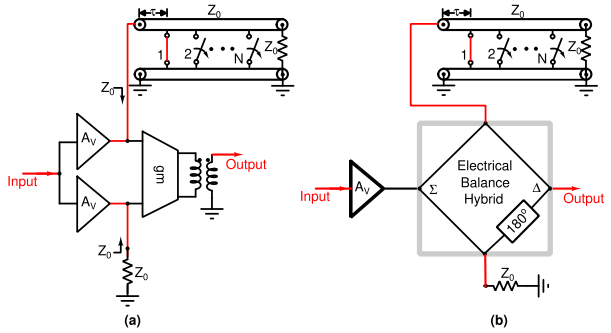


Fig. 4. Cancellation of non-delayed signal: (a) Active approach. (b) Passive approach employing Hybrid coupler.

appropriate switch to be closed. Hence, we can realize a digitally tunable delay line if the second term from (1) can be isolated.

B. Hybrid Coupler as Power Splitter and Combiner

Fig. 3(b) and Fig. 3(c) show one possible way to isolate and extract the delayed signal component in (1) above. Here, the input signal is split into two parts; one half of it is fed to the switch-loaded TL while the other half is inverted in phase. When none of the switches is closed (Fig. 3(b)), the two parts of the signal entering the power combiner are equal and opposite to each other, resulting in a null output. When one of the switches is turned ON (Fig. 3(c)), the input of the TL contains delayed and non-delayed versions of the input signal, as discussed in the previous subsection. Signals from the TL port and the Z_0 termination port are then combined inside the power combiner, resulting in the cancellation of the non-delayed term. The resultant signal consists of only the scaled and delayed version of the input signal, as desired.

The cancellation of the non-delayed portion of the signal can be performed using an active approach, as shown in Fig. 4(a). Here, the input signal is split into two paths using a pair of matched gain stages (A_v), and the non-delayed signal is cancelled using a differential transconductor (g_m). Careful observation reveals that the two gain stages of Fig. 4(a) can be merged to feed the Σ port of a 180^0 hybrid coupler, while the output with the cancelled non-delayed signal can be collected at its Δ port, as indicated in Fig. 4(b).

From Fig. 4, we observe that for the active case to have gain equal to the passive case, g_m needs to be at least $\frac{1}{2|Z_{OUT}|}$ where Z_{OUT} is the impedance of the next stage. Here, the hybrid coupler provides a power gain of $\frac{1}{4}$, as explained later. As there is no compulsion to split the power consumption between A_v and g_m in the passive case, it gives more freedom in optimizing power consumption to trade-off gain/noise and linearity. More importantly, it also allows for the possibility of employing this phase shifter in a bidirectional fashion, which, as indicated earlier, is an important aim of this work. Reworking the active approach for bidirectional operation is expected to increase parasitic capacitance and power consumption.

In this work, therefore, we have chosen the hybrid coupler based passive phase shifter, and its operation is now explained. When all the switches are in OFF state and the TL is

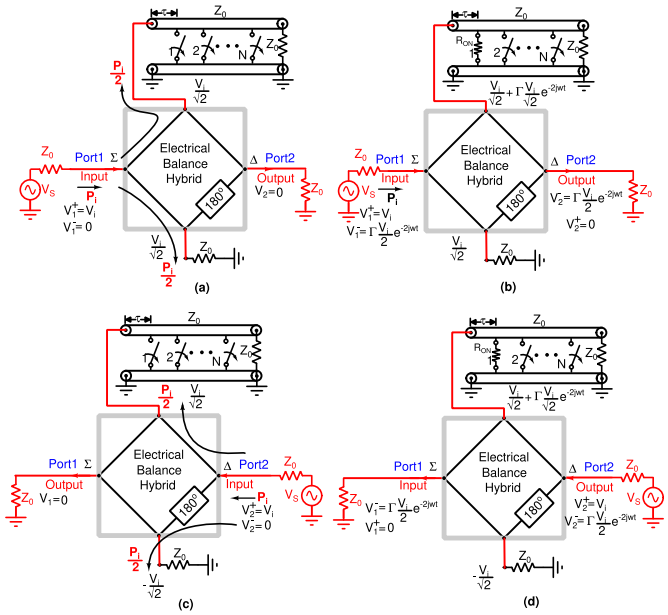


Fig. 5. Principle of operation of RTTLPS implementation using an electrical balance based hybrid coupler.

terminated with Z_0 (Fig. 5(a)), there is complete isolation between the Σ and Δ ports of the coupler. When the first switch of the TL is turned ON (Fig. 5(b)), reflected power is equally split between the Δ and Σ ports. Therefore, both the input return loss and insertion loss are equal and are given by

$$S_{\Sigma\Sigma} = S_{\Delta\Sigma} = \frac{1}{2}\Gamma \exp(-j\omega 2\tau) \tag{2}$$

Similarly, from Fig. 5(c) we see that when the signal is incident at the Δ port under balanced conditions, half of it reaches the TL port. Once the TL switch is turned ON (Fig. 5(d)), half of the power reaching the TL port is reflected back to the Δ port, resulting in the following S-parameter matrix for the RTTLPS

$$[S] = \frac{1}{2}\Gamma \exp(-j\omega 2\tau)\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \tag{3}$$

The overall phase shift of the RTTLPS is given by

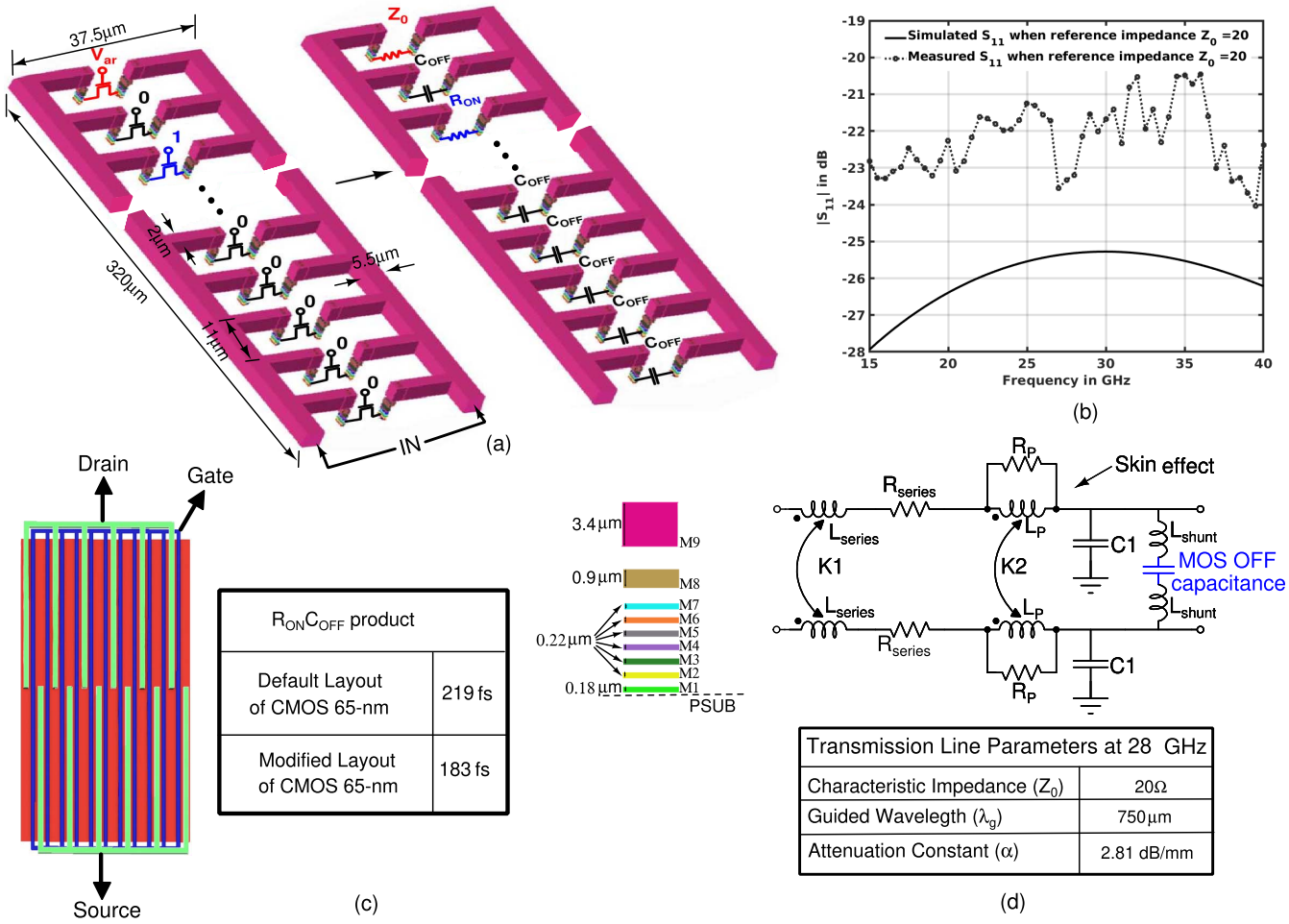
$$\phi = \angle\Gamma - 2\omega\tau \tag{4}$$

When the switches of the TL are ideal, $\Gamma = -1$. Based on (3) and (4), we conclude the following

- Due to its passive nature, the proposed RTTLPS is bi-directional with 6 dB insertion loss and 6 dB matching at both the ports.
- The phase shift can be varied by turning ON switches connected at different TL lengths.
- ϕ varies linearly with ω (assuming ideal hybrid coupler) resulting in true-time delay.
- TL with a total delay of τ results in a maximum phase-shift corresponding to 2τ delay.

III. CMOS Implementation of the Front-End Building Blocks

The proposed front-end is implemented in a 65 nm CMOS process. The implementation details of the building blocks



$R_{ON}C_{OFF}$ product	
Default Layout of CMOS 65-nm	219 fs
Modified Layout of CMOS 65-nm	183 fs

Transmission Line Parameters at 28 GHz	
Characteristic Impedance (Z_0)	20Ω
Guided Wavelegth (λ_g)	750µm
Attenuation Constant (α)	2.81 dB/mm

Fig. 6. (a) Switched transmission line implementation. (b) Characteristic impedance of MOS loaded transmission line. (c) MOS layout to reduce $R_{ON}C_{OFF}$ product and BEOL of the CMOS 65nm process. (d) Modelling of a unit section of switched transmission line.

of the proposed circuit are described below, followed by the complete RTTLPS in the next section.

A. Switch Loaded Transmission Line

A coplanar stripline structure is chosen to realize the TL as it allows differential signalling. The TL is implemented on the top 3.4 μm thick metal layer to minimize losses. The drain and source of minimum channel length NMOS devices are periodically connected between the two lines of the TL to act as switches, shown in Fig. 6(a). The gate terminal is controlled by digital logic to toggle the NMOS switch state selectively. The termination resistance is also realized with a tunable gate NMOS device. The reflection coefficient, looking into the closed switch of the TL in Fig. 6(a) is given by

$$\begin{aligned}\Gamma &= \frac{R_{ON}||Z_0 - Z_0}{R_{ON}||Z_0 + Z_0} \\ &= \frac{-Z_0}{2R_{ON} + Z_0} \\ &= \frac{-\tau_{seg}}{2R_{ON}C_{seg} + \tau_{seg}}\end{aligned} \tag{5}$$

where τ_{seg} and C_{seg} is the delay and total capacitance of the TL segment between two switches respectively. R_{ON} is the ON-state resistance of NMOS switch. C_{seg} is the sum of C_{OFF} (capacitance between source-drain of the switch in OFF state) and distributed capacitance between the lines of the segment. It is important to *maximize* $|\Gamma|$ to keep insertion loss (IL) of the RTTLPS low. In an effort to maximize $|\Gamma|$, we can space the two lines of TL apart resulting in $C_{seg} = C_{OFF}$ in the limiting case (assuming constant capacitance to the substrate is negligible compared to practical values of C_{OFF}). Using this, (5) can be re-written as

$$\Gamma_{MAX} = \frac{-\tau_{seg}}{2R_{ON}C_{OFF} + \tau_{seg}} = \frac{-\tau_{seg}}{2\tau_{cmos} + \tau_{seg}} \tag{6}$$

where, $\tau_{cmos} = R_{ON}C_{OFF}$ is a constant in any given CMOS process. (6) indicates that there is a strong trade-off between the minimum IL ($|\Gamma_{MAX}|$) and phase-resolution (τ_{seg}) of proposed RTTLPS, and it is independent of switch size. In this work, $\tau_{seg} = 0.5$ ps is chosen to achieve the desired phase resolution of 11.25° at 28 GHz and thus the number of switches needed to achieve 180° phase at 28 GHz would be 16.

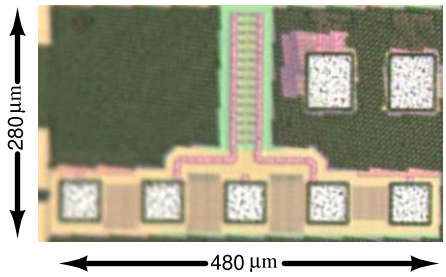


Fig. 7. Die photograph of stand-alone transmission line containing only 15 switches to characterize TL.

Characteristic impedance (Z_0) of the TL is decided by the switch size (C_{OFF}) once τ_{seg} gets fixed. Larger switch size reduces the guided wavelength as a result of the slow-wave effect [21] and hence reduces the overall series loss of the line but lowers the Z_0 which can make the hybrid coupler design challenging. In this work, we have chosen $Z_0 = 20\,\Omega$. The stand-alone TL with periodically loaded NMOS switches is first implemented (Fig. 7) to characterize its S-parameters. The characteristic impedance of the NMOS loaded TL is plotted in Fig. 6(b). Termination resistance for the TL during the measurement is varied using a 5-bit DAC, resulting in a discrepancy with simulation result where very fine step size was used to achieve the best matching.

A custom layout is implemented for the NMOS switch (Fig. 6(c)) where the Metal1 routing does not have any direct overlap sideways with another Metal1 routing in the neighbouring fingers, resulting in lower C_{OFF}. We obtain $\tau_{CMOS} = 183$ fs which is 15% lower than that obtained from standard layout techniques. Using these values, we achieve $|\Gamma_{MAX}| \approx 0.56$.

As evident from Fig. 6(a), C_{OFF} periodically loads the TL similar to capacitive loading in a slow-wave TL structure [21] resulting in a shortening of guided wavelength. EMX electromagnetic simulator is used to optimize the final TL dimensions. A small section of a differentially coupled TL can be modelled as shown in Fig. 6(d). Any imbalance in the TL structure may result in a small common-mode signal which can be rejected using a balun. The need for the balun and differential TL will be explained in detail in section IV. Under low-loss assumptions, the characteristic impedance of the differential TL is given by

$$Z_0 = \sqrt{\frac{L_{diff}}{C_{diff}}} = \sqrt{\frac{2L_{series}(1-K1) + 2L_p(1-K2)}{\frac{C1}{2} + \frac{C_{MOScap}}{1-(2\omega^2 L_{shunt} C_{MOScap})}}} \quad (7)$$

The TL parameters are also extracted in the presence of C_{OFF} and are tabulated. Detailed EM simulations indicate that the phase-shift is not linear with switch setting for the first few positions, where the length of the transmission line is less than 0.1λ since it takes some sections for the switch loading to be treated as periodic loading. Therefore, the 6^{th} switch setting is set as the reference phase and hence the total number of switches to achieve 180° would be 21. In this work, we have used 28 switches to account for any process variation. The simulated loss due to the TL with switch combination for a 180° phase-shift at 28 GHz is around 6 dB.

B. Hybrid Coupler

A capacitive bridge based 180° hybrid coupler [22] is chosen, which acts as a power splitter and combiner, as shown in Fig. 8(a). Here, the Port 3 and Port 4 terminations are implemented using NMOS devices operating in the linear region. The value of their resistance is set to be equal to the Z_0 of the differential TL. The stand-alone hybrid coupler, whose die photo is shown in Fig. 8(b), was fabricated and characterized. The measured and simulated S-parameters of the stand-alone hybrid coupler, with Port 1 as input and Port 2 as output, are plotted in Fig. 8(c) when the bridge is balanced. The measured S_{11} and S_{22} are below -10dB and -6dB respectively, over a 4 GHz band around 28 GHz. The isolation under balanced load conditions is maintained below 33dB. Next, one of the NMOS loads is turned OFF to characterize the loss of the hybrid coupler. The measured and simulated insertion losses of the hybrid coupler (including the matching transformers) are 13.3 dB and 12 dB respectively at 28 GHz, as plotted in Fig. 8(d). For an ideal unbalanced hybrid coupler, insertion loss is 6 dB. The simulated stand-alone insertion loss of the balun that connects the TL is 1.3 dB. The balun loss appears twice due to reflection. The input and output coupled inductors contribute a loss of at least 2 dB while the rest of the loss is caused by the interconnect.

C. LNA With Buffer

The RTTLPS, being a passive circuit, introduces loss in the receive signal path. The simulated loss of the combined phase-shifter structure is 17 dB. To compensate for this loss and to achieve a reasonable noise figure, a source degenerated common source amplifier with a buffer stage precedes the phase shifter. The schematic of the differential LNA and buffer is shown in Fig. 8(e). The inductor L_G can be replaced with a balun to make the input single-ended. A slow-wave transmission line structure is used to reduce effective area and loss, while the width of the MOS transistor MN1 is chosen to maximize f_T. The buffer stage is used to provide matching for the low input impedance of the hybrid coupler. The simulated noise figure and voltage gain of the combined LNA and buffer stage (Fig. 8(f)) is 3.3 dB and 11.8 dB at 28 GHz, respectively. The performance parameters of the LNA and Buffer stage are tabulated in Fig. 8(g).

IV. Design and Implementation of Complete RTTLPS

The complete circuit implementation of the proposed RTTLPS is shown in Fig. 9(a). The Z_{TL} component of Fig. 8(a) is replaced with the switch loaded TL and terminated with an NMOS device operating in the triode region. Matching of the termination impedance with the characteristics impedance of the TL is crucial. Consider the case when the resistance corresponding to voltage V_{Var1} (Z_L) is not equal

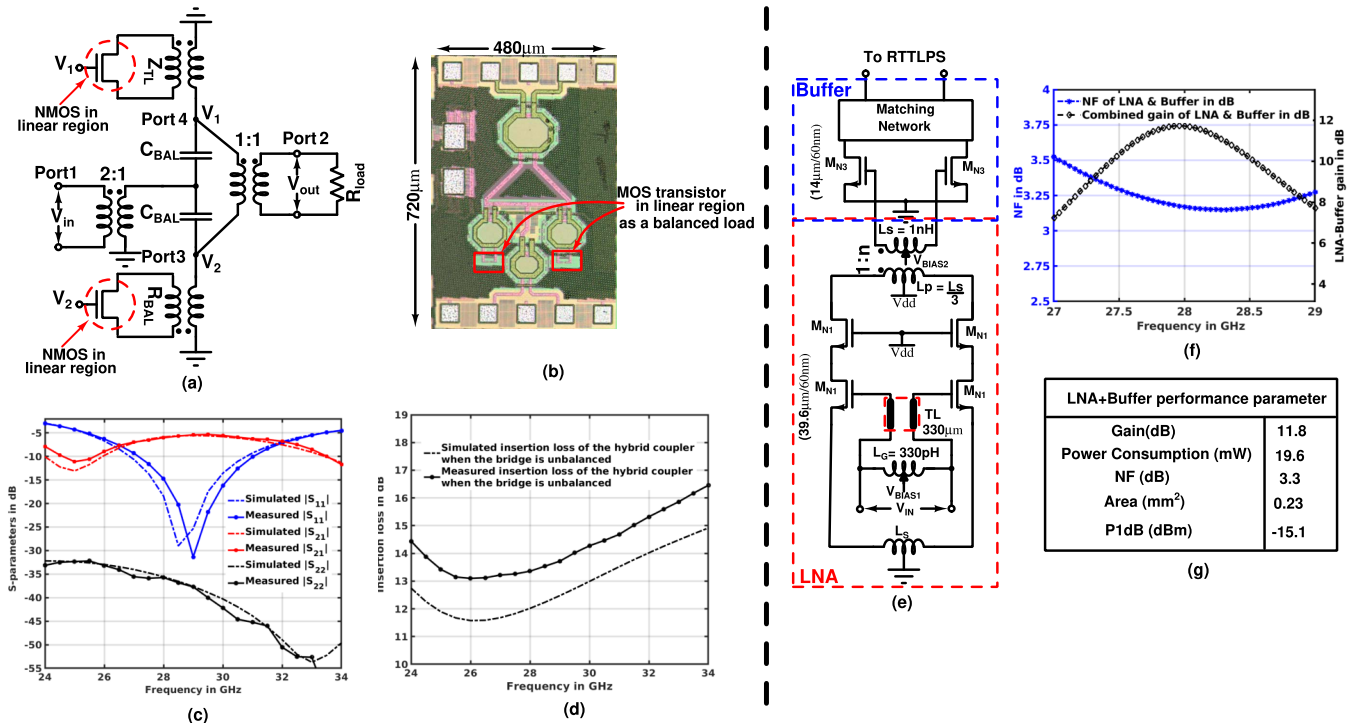


Fig. 8. (a) Capacitive bridge based Hybrid Coupler. (b) Die photograph of stand-alone hybrid coupler. (c) S-parameter of stand alone Hybrid coupler when bridge is balanced. (d) Insertion loss of Hybrid coupler with unbalanced bridge load. (e) Schematic of LNA+Buffer. (f) Simulated NF of and voltage gain for LNA+Buffer. (g) Simulated LNA+Buffer performance parameters.

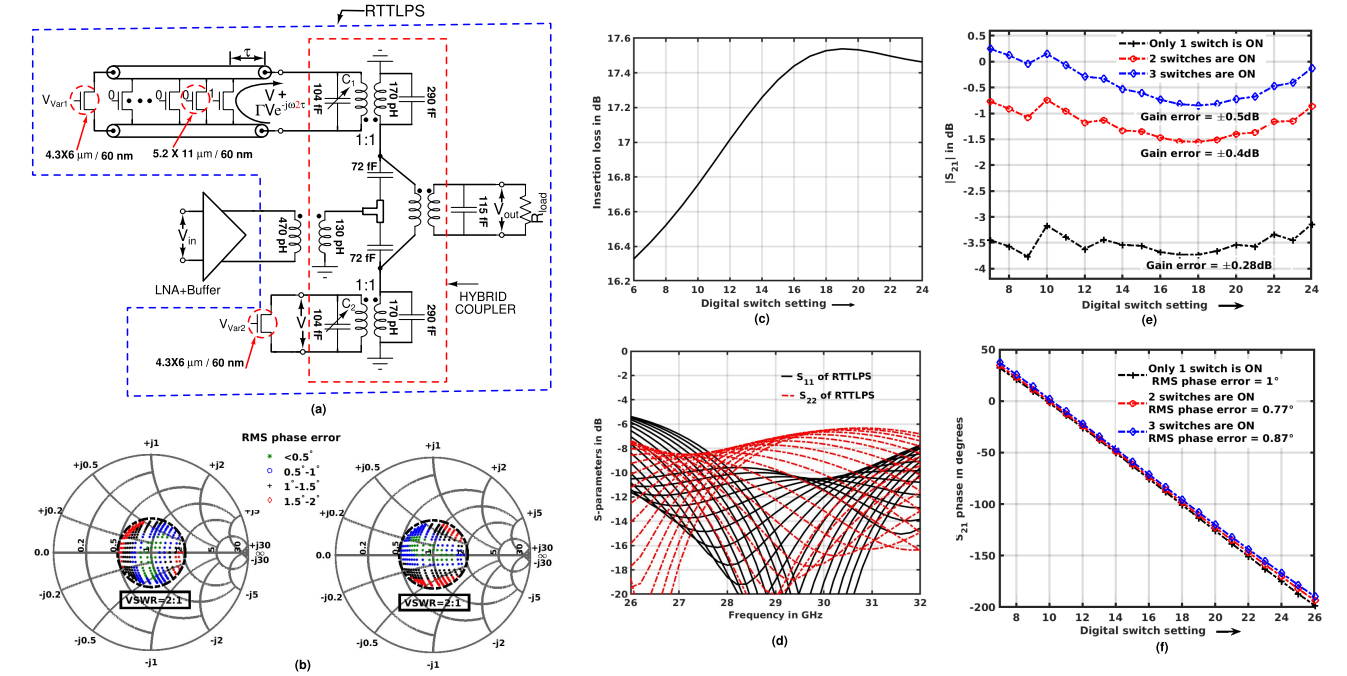


Fig. 9. (a) Implementation of RTTLPS. (b) RMS phase error when source(left) and load(right) impedance varies in VSWR≤2:1 range. (c) Simulated insertion loss of RTTLPS. (d) Simulated S_{11} and S_{22} of RTTLPS across digital switch setting. (e) Simulated S_{21} magnitude and (f) phase variation across switch setting when the gate voltage of closed switch(es) is controlled using 2-bit DAC.

to Z_0. When the first switch is turned ON, the voltage V_{out} is of the form

$$V_{out} \propto \frac{V_{in}}{2} - \Gamma \frac{V_{in}}{2} e^{-j\omega 2\tau} + (1-\Gamma)^2 \frac{V_{in}}{2} \frac{Z_L - Z_0}{Z_L + Z_0} e^{-j\omega 2N\tau} + \ldots \quad (8)$$

From (5) and (8), we can deduce that S_{21} varies for different switch settings when load and source impedance is not equal to Z_0. Similarly, if there is a mismatch in the two paths, the non-delayed component in (1) will not be cancelled, and the output comprises multiple reflected signals and a residual non-delayed component. Thus, it is crucial

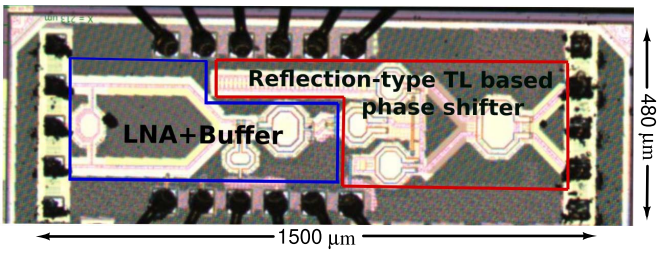


Fig. 10. Die photograph of front-end.

to match the impedance at the balanced port to minimize S_{21} variations. A small varactor of value ±20fF (Fig. 9) is added in shunt with capacitance C_1 and C_2 to account for any mismatch between the two paths due to layout asymmetry. The low value of characteristic impedance Z_0 makes the transformer design challenging and increases the insertion loss of the hybrid coupler. From (7) and (5), we know that loss due to reflections also increases for low values of Z_0. A differential TL offers higher Z_0 compared to a single-ended one and is thus preferred. The simulated insertion loss (IL) of the RTTLPS at 28 GHz is plotted in Fig. 9(c) with respect to the digital switch setting over a 180° phase shift range. IL variation is around 1dB. The simulated input and output return losses (Fig. 9(d)) are better than 9.8 dB and 7.5 dB respectively at 28 GHz for all digital switch settings used to achieve 180° phase shift. Discrete gain tuning of the RTTLPS by turning ON successive switches simultaneously is presented in Fig. 9 (e,f). Here, the 2-bit DAC is used to control the gate voltage from 0.65 V to 1.1 V with a step size of 150 mV to minimize the $|S_{21}|$ variation. When two successive switches are turned ON,

$$Equivalent\ R_{ON,2} \approx \frac{R_{ON}}{2}$$

and, when three successive switches are turned ON,

$$Equivalent\ R_{ON,3} \approx \frac{R_{ON}}{3}$$

Fig. 9 (e,f) shows gain tuning of around 3 dB while maintaining the phase coverage with less than 1° rms error.

The proposed RTTLPS expects the source and load impedances to be equal to the reference impedance of the respective phase-shifter ports for ideal operation. To illustrate the effect of source and load impedance variations, we set up a test-bench with our designed switched TL connected to an ideal lossless hybrid coupler. Fig. 9(b) shows the rms phase error due to source and load impedance variations in the VSWR≤2:1 range for 180° phase-shift using this test-bench.

V. Measurement Results

The proposed phased array front end is fabricated in a 65 nm CMOS process occupying an area of 1.5 × 0.48 mm^2, as shown in the die micrograph of Fig. 10. Pad inductance and capacitance were de-embedded from the measurements using an on-chip open pad, through and short de-embedding structures [27]. The chip was characterized using a 150RF MPS FormFactor probe-station with differential GSGSG probes. All S-parameters were captured using a 4-port vector network analyzer (Keysight N5247A PNA-X).

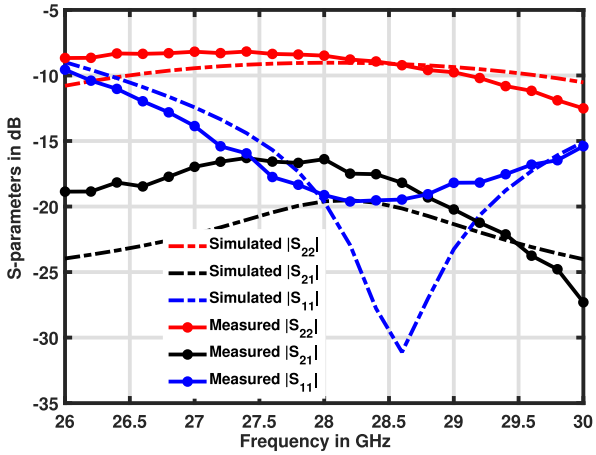


Fig. 11. Comparison of measured and simulated S-parameters of the front-end when all the TL switches are OFF.

The S-parameters of the complete phased array front-end is plotted in Fig. 11. The measured S_{21} is −17.5 dB when all switches of the switched transmission line are OFF, and the resistance corresponding to terminating NMOS is set to be equal to the characteristic impedance of the transmission line. The required gate voltage of the NMOS is determined by characterizing the stand-alone transmission line. The return losses at input and output ports, S_{11} and S_{22}, are maintained below −10dB and −8dB respectively, over the 4GHz band.

The phase of S_{21} at 28 GHz is plotted in Fig. 12(a) when the switches are turned ON one by one from switch setting 7 to 23. The measured phase change per switch setting is around 11.25°, and the rms phase error[1] is 2.8°. Simulations suggest that this error is mainly due to two reasons. The mismatch between the two paths and the impedance seen by the TL line is not perfectly matched. This error can be minimized further through a more compact and symmetric layout. The magnitude variation in S_{21} for a phase shift of 180° is ± 0.4 dB, as plotted in 12(b). The three primary factors responsible for S_{21} magnitude variation is (a) increase in the loss along the length of the transmission line (b) residual layout asymmetry and (c) change in the input return loss with switch setting. A two-bit DAC was used to control the voltage at the gate of the switch to minimize these S_{21} variations. Fig. 12(c,d) shows the S_{21} phase and magnitude response in the potential 5G frequency band 26.5 GHz-29.5 GHz against switch settings 7-23 when the ON switch gate voltage is optimized for operation at 28 GHz.

Next, the input power is varied to find the input-referred 1-dB compression point, P1dB, for three different maximum gain (maximum $|S_{21}|$ occurs when the switches are set for minimum phase setting) settings, as plotted in Fig. 12(d). The measured P1dB is around −16.2 dBm, and does not vary with multiple switches being turned ON simultaneously, i.e. even with a gain variation of 3 dB. The simulated IIP3 for all switch settings shows that the worst-case IIP3 is always above 9 dBm.

Fig. 14 shows a phase variation of ±1.5° between the cases when only 1 switch is ON versus when 3 switches are turned

[1]The S_{21} phase response was fitted to a linear fit in Matlab. The difference between this linear ideal fit and S_{21} phase at each switch setting to achieve 180° is used to calculate rms phase error.

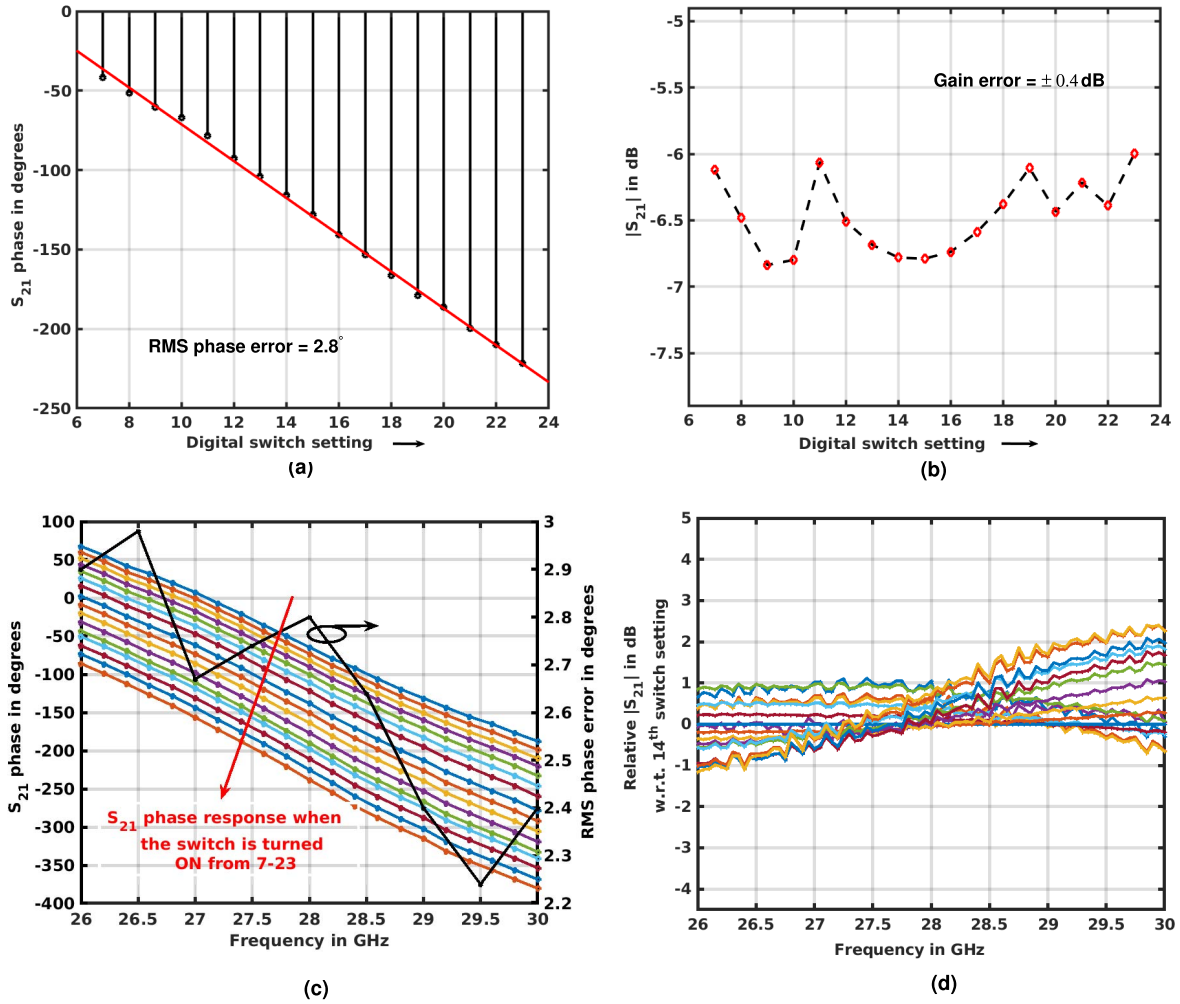


Fig. 12. Measured results (a) S_{21} phase measurements at 28 GHz: phase shift versus digital switch setting. (b) S_{21} amplitude variation in dB versus digital switch setting. (c) S_{21} phase and (d) magnitude variation across frequency for different digital switch setting when the closed switch gate voltage is optimized for 28 GHz operation.

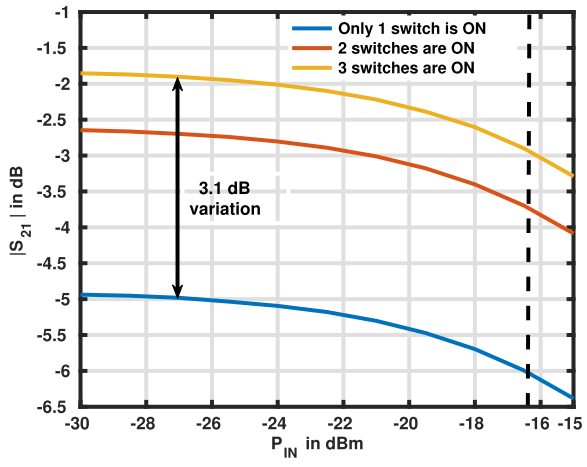


Fig. 13. Measured output compression of the front-end at 28 GHz.

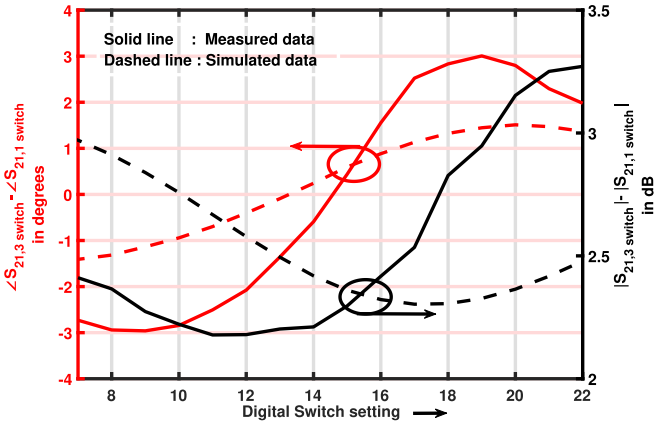


Fig. 14. Plot of phase and magnitude difference between the cases when only one switch is ON and when all the three switches are ON.

ON. Gain variation in such a scenario is around 1 dB with an average shift of close to 3 dB, thus aiding the design of the variable gain amplifier in a phased array receiver. During this measurement, the gate voltage of the ON switch is always fixed to 1.2 V, and then 3 successive switches are turned ON to capture the shift in S_{21}. When more than 3 switches are

TABLE I
PERFORMANCE COMPARISON WITH RECENTLY REPORTED *mm*-WAVE PHASE SHIFTERS

Reference	[14]	[15]	[23]	[24]	[25]	[26]	[12]	This work
Technology process	65 nm CMOS	65 nm CMOS	130 nm BiCMOS	45 nm CMOS SOI	130 nm CMOS	65 nm CMOS	130 nm SiGe	65 nm CMOS
Approach	RTPS	RTPS	RTPS	STPS	Hybrid	Trombone TL	Tunable TL	RTTLPS
Frequency (GHz)	28	29	61	28	60	15-40	28	28
Phase range /Max delay	360°	379°	367°	360°	360°	40 ps	190°	180°
Phase/Delay resolution	DAC dependent 11.25°	DAC dependent 22.5°	DAC dependent 5°	Digital 11.25°	Digital 22.5°	Digital 5 ps	Digital 11.25°	Digital 11.25°
RMS phase error (°)	0.3	-	-	5	7	-	0.6	2.8
Insertion loss (dB)	7.45-8.05	8.25	10.2	6-13	12.3-16.3	14	9.3	15.5 to 17.5
Maximum gain error (dB)	0.3	1	0.75	0.8	1.7	2	0.25	0.4
Input return Loss (dB)	6.7	23	10.4	8	12	10	-	9.8*
Power consumption (mW)	0	0	0	0	19.5	24.6	0	0
Area (mm^2)	0.16	0.076	0.16	N/A	0.1	0.99	0.18	0.17**
Gain control possible?	No	No	No	No	No	No	No	**Yes(3dB)**
Phase-shift per unit TL length at 28 GHz (degree/μm)	-	-	-	-	-	0.13	0.1	**0.62**

*Post-layout simulation results (as LNA and buffer precede the RTTLPS) ** Phase shifter core (hybrid coupler and transmission line)

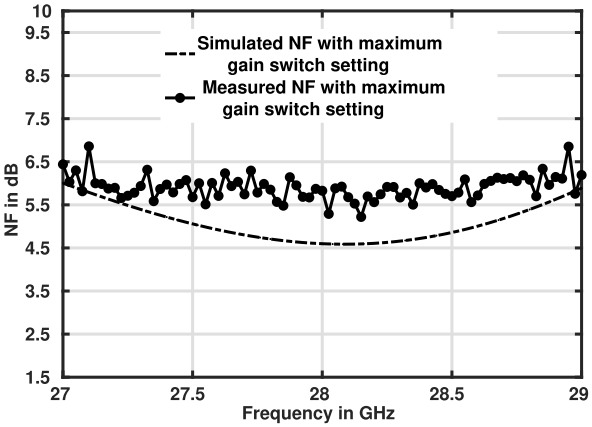


Fig. 15. Measured and simulated single-ended NF for digital switch setting corresponding to maximum $|S_{21}|$.

turned ON simultaneously, the change in equivalent R_{ON} is not significant enough to cause an appreciable change in S_{21}.

Fig. 15 plots the measured and simulated NF of the front-end single-ended receiver for digital switch setting corresponding to the maximum magnitude of S_{21}. NF varies between 5.5 dB and 6.5 dB in 2 GHz band.

A comparison of recent 28 GHz RF phase shifters is shown in Table I. [25] uses digitally controlled variable gain amplifiers (VGAs) with I and Q signals to obtain the desired phase shift but has poor rms phase error. [26] is a true time-delay circuit with trombone structure employing eight switches distributed along the TL. Similarly, in [12], the phase is varied by changing L and C of the TL while keeping its effective Z_0 constant. To achieve a phase shift of 180° at 28 GHz, the trombone TL [26] and tunable delay line [12] based phase shifters require 1.4 mm and 2 mm line length respectively while the proposed RTTLPS needs only 290 μm. The RTPS based approach in [14], [23] requires a high-resolution DAC to achieve fine resolution, while the STPS based approach of [24] requires a large die area. The approach proposed in this work presents a fresh way to achieve phase shift and gain control with a low-resolution DAC, whose insertion loss is expected to reduce as technology nodes scale down.

VI. CONCLUSION

A switched TL based passive phase shifter with a 5-bit resolution at 28 GHz is introduced. Since there is no varying element such as capacitor or inductor, the characteristic impedance of the transmission line Z_0 is relatively constant with phase variation. A low-resolution, 2 bit DAC can be used to minimize S_{21} phase and amplitude variations. Gain can be further tuned in discrete steps by turning ON multiple switches simultaneously. The insertion loss in this approach is partly technology-dependent and is expected to improve at higher technology nodes.

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