High-Power *X*-Band 5-b GaN Phase Shifter With Monolithic Integrated E/D HEMTs Control Logic

Weijun Luo, Hui Liu, Zongjing Zhang, Pengpeng Sun, and Xinyu Liu

***Abstract*— A high-power *X*-band GaN-based 5-b digital phase shifter with control logic circuit on-chip is demonstrated for the first time, which is implemented with monolithic integrated GaN E/D HEMTs fabrication process. Gate trench etching together with Al_2O_3 as gate dielectric is used to form the gate of the E-mode GaN HEMTs. Switched filter and high-pass/low-pass topology are used to design the 11.25°/22.5° and 45°/90°/180° phase shifters, respectively. A novel three stages control logic circuit is described and characterized. The fabricated 5-b phase shifter demonstrates an rms phase error less than 4.5°, an rms amplitude error less than 0.6 dB, an insertion loss less than 11 dB, and an input–output return loss better than −10 dB across 8.5–11.5 GHz for all 32 states. In addition, the phase shifter exhibits a typical $P_{1\ dB}$ input power of 34.8 dBm in the continuous wave power handling capability measurement at 9 GHz.**

***Index Terms*— Control logic circuit, GaN HEMTs, high pass/low pass, phase shifter, switched filter, X-band.**

I. Introduction

PHASE shifter is a key component of active phased-array antennas for radar, communication, and navigation applications [1]. Though the widely used solid-state phase shifters are based on the p-i-n diode and GaAs FET, they have their limitations. The p-i-n diode phase shifters can handle high power, but they require significant dc current to drive which results in higher insertion loss [2]. Although the GaAs FET phase shifters have low insertion loss, they have limited RF power handing capability [3]. In recent years, GaN HEMTs has progressed significantly which can be operated in high voltage (−100 V), high power density (−10 W/mm), high temperature (−600 °C), high frequency (−300 GHz), and radiation conditions. Therefore, GaN HEMTs are promising candidates for robust high power handling capacity, compact, low insertion loss, and low-cost microwave phase shifters. Though several GaN-based phase shifters have been reported [4]–[7], they are all 1-b phase shifters. Up to now, there are no GaN-based phase shifters with more than 1-b that has been reported. Besides, phase shifters often integrated with other components in a transmit/receive (T/R) module or other telecommunication systems with single-ended (positive) control voltages. However, the control voltage of depletion-mode (D-mode) GaN HEMTs is negative. Therefore, control logic circuit, transferring the negative control voltages to positive, is essential for GaN-based phase shifters and other microwave components. Due to the fabrication challenges of enhanced-mode (E-mode) GaN HEMTs [8], which are indispensable for control logic circuits, there are no GaN-based phase shifters or other microwave components with control logic circuits have been reported.

In this paper, a high-power *X*-band AlGaN/GaN HEMTs-based 5-b phase shifter with monolithic integrated E/D HEMTs control logic is demonstrated for the first time, overcoming the above technical issues. The integrated E/D-mode AlGaN/GaN HEMTs fabrication process has been discussed. The 5-b *X*-band phase shifter combined with on-chip control logic is designed and optimized with the E/D-mode AlGaN/GaN HEMTs to realize low insertion loss, high phase resolution, and good return loss performances. The simulated characteristics agree well with the experimentally measured results. Remarkable power handling capability as well as low insertion loss, high phase resolution characteristics are presented. Finally, the performance of the fabricated GaN-based phase shifters with control logic is compared with that of GaAs-based and p-i-n diode-based phase shifters.

II. Device Fabrication Process

The common-gate (CG) D-mode AlGaN/GaN HEMTs are used as switching devices in the *X*-band 5-b phase shifters. While the common-source E/D-mode AlGaN/GaN HEMTs are used in the control logic circuit to transfer the control voltages from negative to positive. Fig. 1 shows the schematic of the integrated E/D-mode AlGaN/GaN HEMTs, which were fabricated on a conventional AlGaN/GaN heterostructure grown by metal–organic chemical vapor deposition. The epitaxial structure consists of a 3-in SiC substrate, a 2-μm GaN buffer, a 1-nm AlN interlayer, a 23-nm $Al_{0.23}Ga_{0.77}N$ barrier, and a 2-nm GaN cap.

The fabrication process was compatible with conventional GaN HEMTs processes. R_{ON}, one of the most important characteristics of GaN HEMTs for switching application, should be reduced to achieve low insertion loss. Ti/Al/Ni/Au-based ohmic contacts were formed by electron-beam evaporation.

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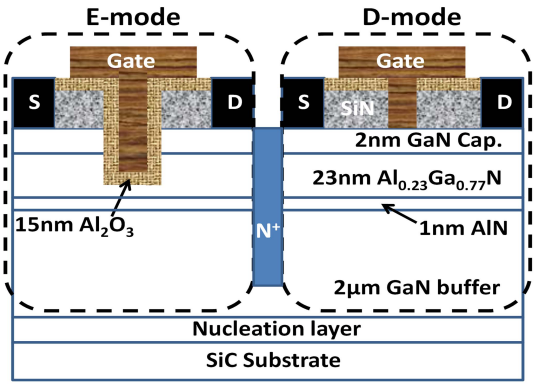

Fig. 1. Schematic of the integrated E/D-mode AlGaN/GaN HEMTs.

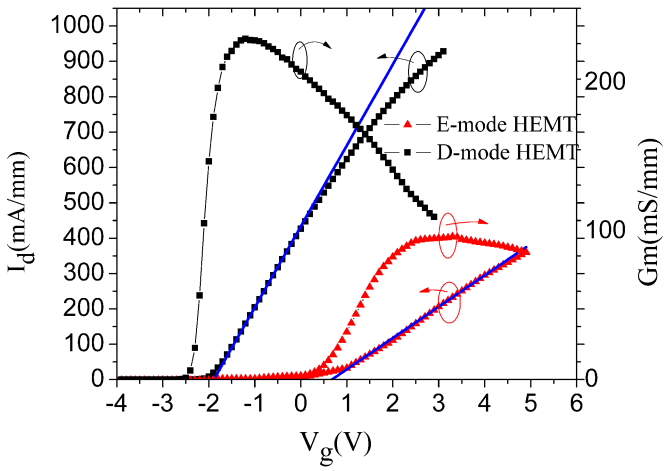

Fig. 2. Transfer characteristics of the integrated E/D GaN HEMTs.

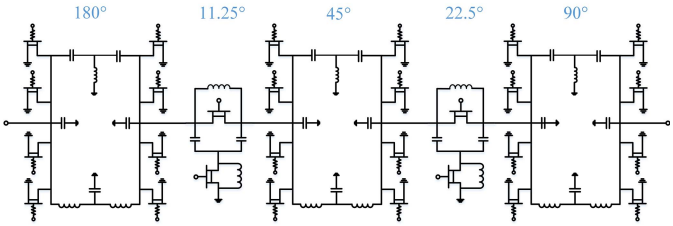

Fig. 3. Schematic of the 5-b digital phase shifters.

Annealing in vacuum condition, which can effectively avoid the Ti/Al oxidation that deteriorate the ohmic contact [9], was used to reduce the ohmic contact resistance at 870 °C for 50 s. Transmission line method test results show that the ohmic resistance of 0.2 Ω· mm and specific contact resistivity of 2×10^{-6} Ω·cm^2 were obtained, which are helpful to the low insertion loss of the GaN HEMTs switching device. The mesa isolation was made by N^+ multienergy implantation. As the E-mode GaN HEMTs were targeted to design the control logic circuit which is not used to transport the RF signal, the E-mode gate trench was formed by optical lithography instead of electron-beam lithography with a gate length of 0.5 μm. Then, the barrier thinning was done by Cl-based inductive coupled plasma etching with a depth of about 20 nm. A 15-nm Al_2O_3 was deposited by atomic layer deposition to form E-mode MOS-HEMT which can not only reduce the gate leakage current but also increase the gate voltage swing. The D-mode gate was formed by electron-beam lithography with a gate length of 0.25 μm. NH_4F:CH_3COOH:H_2O = 1:1:1 solution was used to remove the Al_2O_3 gate dielectric of the D-mode GaN HEMTs. Ni/Au contacts were evaporated to form both the E/D mode gate. The surface of the devices was passivated with 200-nm Si_3N_4 grown by plasma enhanced chemical vapor deposition. Ti/Au contacts were formed by electroplate to reduce the resistance of the metal pad. Finally, the fabrication process is concluded with back-side wafer thinning down to 90 μm, via etching and metallization for electrical grounding.

Fig. 2 shows the transfer characteristics of the integrated E/D GaN HEMTs. From the I_{ds}–V_{gs} curve, the E-mode device shows a maximum drain current density I_{max} of 400 mA/mm at a gate bias of as large as 5 V, and the saturation current of the D-mode device is >900 mA/mm. The peak transconductances and threshold voltages (usually defined by tangent extrapolation of the I_{ds}–V_{gs} curve at the V_{gs} of the peak transconductances) are 100 mS/mm, 0.75 V for the E-mode device and 230 mS/mm, −1.9 V for the D-mode device, respectively. While by strict defining ($I_{ds} = 0$), the threshold voltage of the E-mode GaN HEMTs is −0.8 V and the drain current I_{ds} = 2.5 mA/mm when V_{gs} = 0 V. This poor subthreshold characteristic may be caused by the surface damage during the gate recess etching process. Small-signal measurements show the f_T/f_{max} of 25 GHz/48.5 GHz for the E-mode device and 31 GHz/57 GHz for the D-mode device at $V_{ds} = 10$ V. The integrated E/D GaN HEMTs were used to design the X-band 5-b phase shifters and control logic circuits.

III. Circuit Design

A. Five-Bit Digital Phase Shifters Design

The 5-b digital phase shifters consist of 180°, 90°, 45°, 22.5°, and 11.25°. These digital bits are cascaded with each other and can produce 32 different phase shift states of 0° to 360° with 11.25° as step. The topology of the proposed 5-b phase shifters is shown in Fig. 3. Each bit of a phase shifter was designed and optimized to have small phase error, low insertion loss, good input and output matching, power capacity, and chip size.

For 11.25° and 22.5° phase shifters, the switched filter topology is proposed. The schematic of the switched filter network and its equivalent circuits are illustrated in Fig. 4. When V_c is −5 V, the switching device M_1 is pinched OFF and M_2 is turned ON. The circuit can be dealt as the low-pass network composed of the inductors L_1, two parallel capacitors C_p, as shown in Fig. 4(b), as long as the ON-state resistance R_{on2} of M_2 is quite small. The low-pass π-type filter network can be analyzed by ABCD matrix with neglecting the ON-state resistance of M_2, and the transmission phase can be solved as

$$L_1 = \frac{Z_0 \sin\varphi}{\omega_0} \quad C_p = \frac{\tan(\varphi/2)}{\omega_0 Z_0} \tag{1}$$

where φ is the desired phase shift, Z_0 is the characteristic impedance, and ω_0 is the center frequency.

When V_c is 0 V, the switching device M_1 is turned ON, and M_2 is pinched OFF. The inductor L_2 is sized to parallel

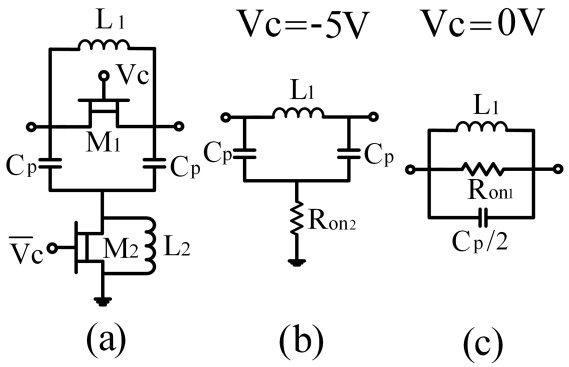

Fig. 4. (a) Topology of the switched filter. (b) Equivalent circuit when $V_c = -5$ V. (c) Equivalent circuit when $V_c = 0$ V.

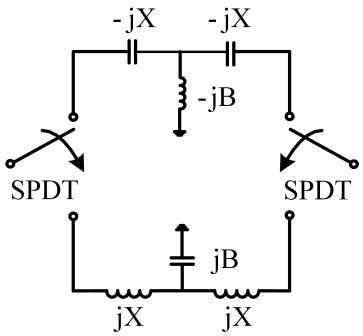

Fig. 5. Schematic of the T-type high-pass/low-pass topology.

resonate the OFF-state capacitance C_{OFF2} of M_2 at the center frequency of ω_0, preventing the RF signal leak to the ground. The equivalent circuit is shown in Fig. 4(c) and the L_2 can be obtained from

$$L_2 = \frac{1}{\omega_0^2 C_{OFF2}}. \tag{2}$$

With the control bias V_c, these two equivalent circuits in Fig. 4(b) and (c) will have a phase difference of φ at ω_0.

For 45°, 90°, and 180° circuit, the high-pass/low-pass topology was used, which consists of two single-pole/double-throw (SPDT) circuits and the high-pass/low-pass phase shifter elements. Fig. 5 shows the schematic of the T-type high-pass/low-pass configuration. Through the investigation of the ABCD matrices for the networks, the phase shift $\Delta\Phi$ caused by switching between low-pass and high-pass networks is given by

$$\Delta\phi = 2\arctan\frac{2B + X - XB^2}{2(1 - BX)}. \tag{3}$$

The X and B are the reactance and susceptance of the T structure, respectively, shown in Fig. 5. As for the SPDT, the switch transistors can either be connected in series or shunt. Since the higher drain–source capacitance of the AlGaN/GaN HEMTs, which contributes to poorer isolation for the series switch at higher frequency [10], the shunt configuration is adopted for the SPDT to achieve good insertion loss and isolation performances, as depicted in Fig. 3. After the

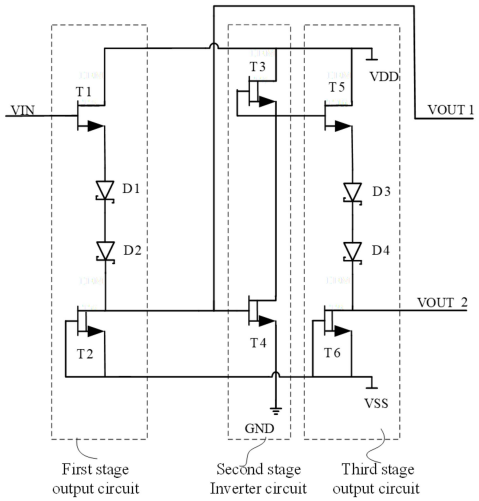

Fig. 6. Schematic of the control logic circuit.

five major bits are designed, they were connected in series and the individual bit performance can be affected by others. Therefore, it is important to optimize bits order and achieve better performances. The optimized bits order of this 5-b phase shifter is 90°, −22.5°, −45°, −11.25°, and −180°, as shown in Fig. 3.

The D-mode CG AlGaN/GaN HEMTs with a gate width of 2 × 100 μm and 4 × 100 μm and a gate length of 0.25 μm were used as switching devices in the designed 5-b digital phase shifters. The model of the switching device used to design the phase shifters was previously reported [11]. In order to prevent signal leakage, 25-kΩ TaN thin-film resistors are connected at the gate of the switching devices. All the switching devices work in two different states with gate voltages of 0 (ON-state) and −5 V (OFF-state), respectively. The simulated results of the 5-b digital phase shifters are described in Figs. 9–13.

B. Control Logic Circuit Design

Phase shifters often integrated with other components in a T/R module or system, which has single-ended (positive) control voltages to make them uncomplicated, compact, and low cost. Since most of the GaN-based microwave components and circuits are depending on D-mode GaN HEMTs with a negative bias voltage, it is significant to design and fabricate control logic circuits to transfer the positive supply voltage to negative. However, the E-mode GaN HEMTs which is essential for the control logic circuits are still facing many challenges [8]. This section describes the design of the control logic circuits. The goal of this design is to transfer the positive input voltages (0–5 V) to two complementary negative voltages (−5–0 V and 0–5 V) that can be used to control the 5-b phase shifters.

By using the integrated E/D-mode GaN HEMTs mentioned above together with the Agilent EE-HEMT device model, the control logic circuits for the proposed 5-b *X*-band GaN digital phase shifters are designed and fabricated. As depicted in Fig. 6, the control logic circuit consists of three stages with

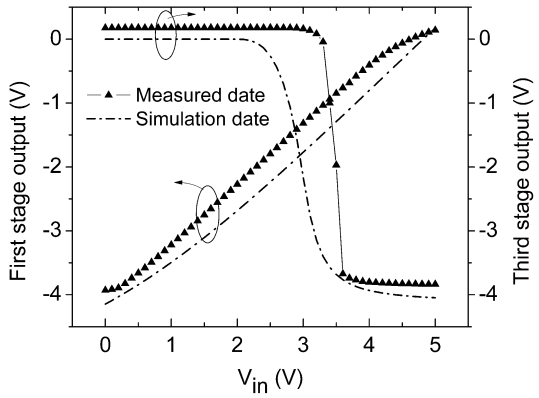

Fig. 7. Simulated and measured results of the control logic circuit.

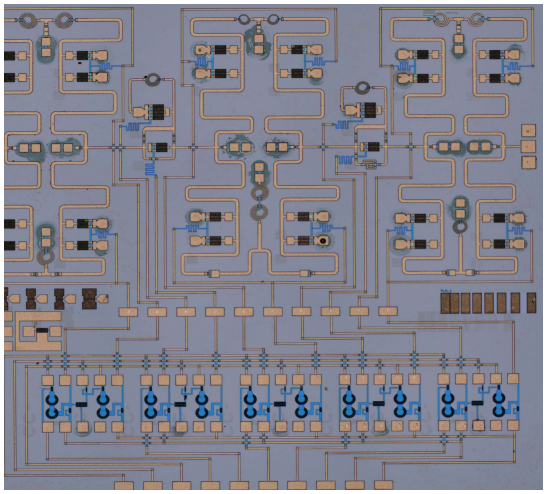

Fig. 8. Photograph of the fabricated 5-b GaN digital phase shifters with control logic circuits.

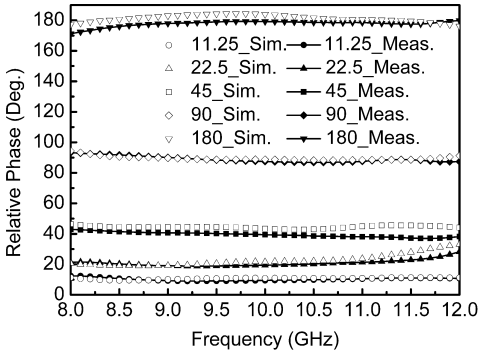

Fig. 9. Measured and simulated phase shifting performance of five major bits.

two E-mode and four D-mode GaN HEMTs, and four Schottky diodes. The input of the control logic circuit is $V_{\rm in}$ = 0–5 V, the output is expected to be two complementary negative voltages $V_{\rm out1}$ = −5–0 V and $V_{\rm out2}$ = 0–5 V which is the control voltage requirement of the 5-b GaN digital phase shifters. The first stage of the control logic circuit is consisted of an E-mode GaN HEMT T_1 (gate width = 20 μm), a D-mode GaN HEMT T_2 (gate width = 20 μm) in series with two Schottky diodes (size = 60 μm). When $V_{\rm in}$ = 0 V, $V_{\rm dd}$ = 5 V, and $V_{\rm ss}$ = −5 V, T_1 is not turned ON completely, its equivalent resistance is larger than the ON-resistance of T_2, which is always turned ON. So, most of the voltage in first stage dropped on T_1, then $V_{\rm out1}$ = −5 V. When $V_{\rm in}$ = 5 V, $V_{\rm dd}$ = 5 V, and $V_{\rm ss}$ = −5 V, T_1 and T_2 are both turned ON completely, tuning the size of the Schottky diodes to gain $V_{\rm out1}$ = 0 V. The second stage is an inverter, which is consisted of a D-mode GaN HEMT T_3 (gate width = 10 μm) and a D-mode GaN HEMT T_4 (gate width = 100 μm). When $V_{\rm out1}$ = −5 V $V_{\rm dd}$ = 5 V, T_3 is always turned ON, T_4 is pinched OFF, most of the voltage in inverter dropped on T_4, then the output voltage of the inverter is 5 V. When $V_{\rm out1}$ = 0 V, T_3 and T_4 are both turned ON, since the ON-resistance of T_3 is about ten times larger than that of T_4, most of the voltage dropped on T_3, so the output voltage of the inverter is 0 V. The input voltage and circuit elements of the third stage are the same as the first stage, which achieves a complementary output voltages $V_{\rm out2}$ (−5–0 V) as $V_{\rm out1}$ (0–5 V).

As shown in Fig. 7, the simulated and measured results of the control logic circuit agree well. When $V_{\rm in}$ = 0 V, $V_{\rm dd}$ = 5 V, $V_{\rm ss}$ = −5 V, $V_{\rm out1}$ = −4 V, and $V_{\rm out2}$ = 0 V, while when $V_{\rm in}$ = 5 V, $V_{\rm dd}$ = 5 V, $V_{\rm ss}$ = −5 V, $V_{\rm out1}$ = 0 V, and $V_{\rm out2}$ = −4 V. The output low voltage is −4 V, not reach the expected value of −5 V. The reason is when $V_{\rm in}$ = 0 V, the ON-resistance of T_2 also shares part of the voltage, the equivalent resistance of T_1 is not large enough to make $V_{\rm out1}$ to −5 V. Besides, the measured flip threshold voltage value of the inverter is positive shifted compared to the simulated. This is because the fabricated threshold voltage V_T of the D-mode GaN HEMTs is positive shifted compared to that of the model's used in simulation. As the threshold voltage of the switching D-mode GaN HEMTs in phase shifters is about $V_{\rm th}$ = −1.9 V, as shown in Fig. 2, then the high (0 V) and low (−4 V) output voltages of the control logic circuit can be used to control the 5-b phase shifters. Except the output voltages, the current consumption of the control logic circuit is also investigated. The current consumptions of the three stage are 6.9, 2.1, and 6.7 mA, respectively. The current consumptions are a little bit higher than that of GaAs-based control logic circuit [12], [13], and should be optimized in the future.

IV. Results and Discussion

The 5-b GaN digital phase shifters with control logic circuits were fabricated by the monolithic integrated E/D GaN HEMTs process. A photograph of the fabricated phase shifters is shown in Fig. 8. The chip size is 5 × 4.7 mm^2. Each bit of the phase shifter is connected with a control logic circuit, which can transfer the input positive control voltages (0–5 V) to negative voltages (−4–0 V) as mentioned above. The fabricated phase shifters were tested by Agilent Parameters Network Analyzer with RF probing on wafer.

In Fig. 9, the measured phase shifting of five major bits is compared with simulated result. It can be observed that the measured performance matches simulation value well. The measured and simulated insertion losses of all 32 states of the fabricated 5-b phase shifters are shown in Fig. 10.

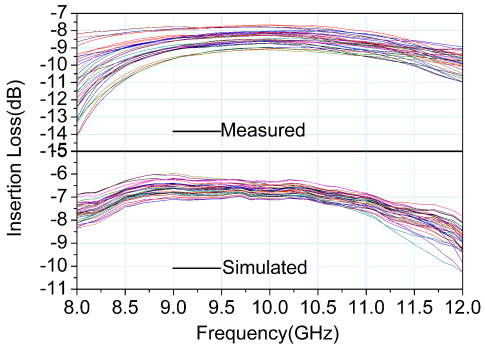

Fig. 10. Measured and simulated insertion loss of all 32 states.

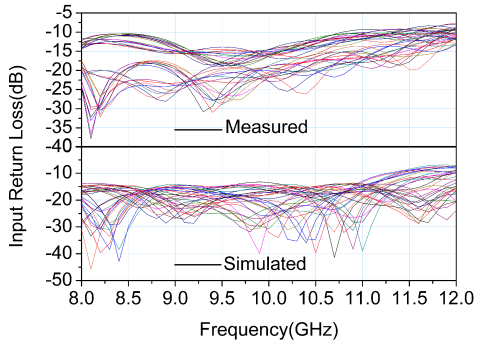

Fig. 11. Measured and simulated input return loss of all 32 states.

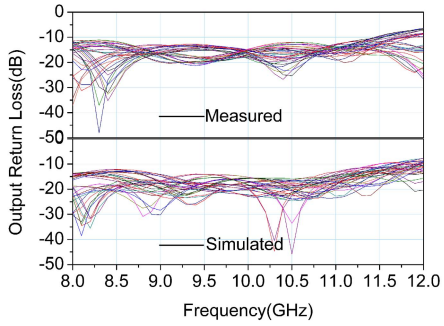

Fig. 12. Measured and simulated output return loss of all 32 states.

It shows that the measured insertion loss varies between 8 and 11 dB from 8.5 to 11.5 GHz, which is comparable to that of GaAs-based phase shifters [3], [14]. The measured and simulated input–output return losses of all 32 states of the fabricated 5-b phase shifters are shown in Figs. 11 and 12. It can be seen that the measured input and output return losses of all 32 states are almost better than −10 dB. The measured statistical rms phase error and rms amplitude error and simulated statistical rms phase error and rms amplitude error of the fabricated phase shifters are depicted in Fig. 13. It can be observed that the measured rms phase error is less than 4.5° from 8.5 to 11.5 GHz which demonstrated the high phase resolution of the phase shifters. The measured rms amplitude error is less than 0.6 dB which proves the small insertion loss variation of the phase shifters. However, there are still some points need to be optimized. For example, the deviation between the simulated and measured phase

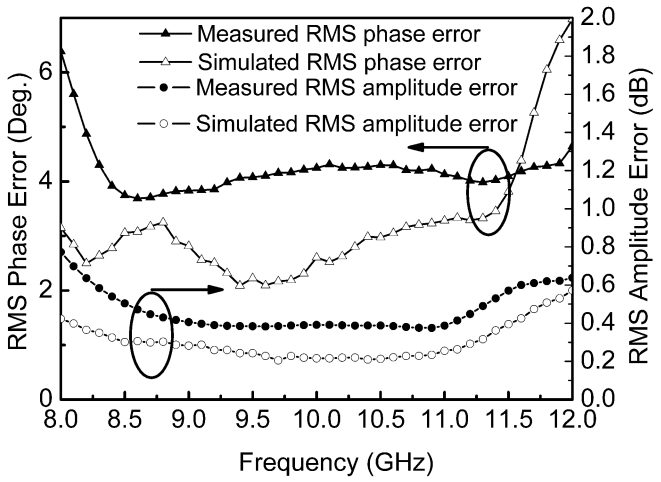

Fig. 13. Measured and simulated rms phase error and amplitude error.

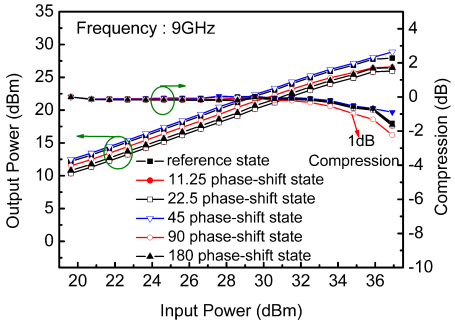

Fig. 14. Measured output power and the variation of insertion loss of five major bits.

shifting results of the 180° at 8–10 GHz and that of 45° at 11–11.5 GHz, which is mainly caused by the use of big spiral inductance as you can find in Fig. 8. Besides, the discrepancies of insertion loss and input return loss of all 32 states are also caused by the deficiency of 180° and 45°.

The output power and variation of insertion loss against input power of five major bits and reference state of the phase shifters are shown in Fig. 14. The test frequency of the continue wave signal is 9 GHz. As depicted in Fig. 14, the transfer remains linear until a input power of 30 dBm is reached. Usually, the $P_{1\ \mathrm{dB}}$ and $P_{0.1\ \mathrm{dB}}$ input power (when the insertion loss compressed 1 and 0.1 dB) is used to assess the power handling ability of the phase shifter. The measured $P_{1\ \mathrm{dB}}$ and $P_{0.1\ \mathrm{dB}}$ input power of the phase shifters is about 34.8 and 31.5 dBm, which are 8–10 dB higher than that of GaAs-based phase shifters [3], [14]. This large signal test results suggest that the GaN HEMTs are promising candidates in high power handling phase shifting application. Besides, the measured phase shifting as a function of power level of the five major bits at 10 GHz are presented in Fig. 15. The phase shifts changes a little with the variation of the input power level from −20 to 0 dBm, which proves the stability of the GaN-based phase shifters. Table I shows the performance comparison of the proposed GaN-based phase shifters with the other reported GaN, GaAs pHEMT, and GeSi p-i-n-based phase shifters. To the authors' knowledge of all,

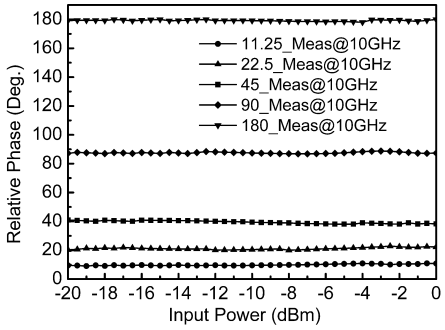

Fig. 15. Measured phase shifting with the variation of power level of five major bits.

TABLE I
PERFORMANCE COMPARISION OF THE PHASE SHIFTERS

	This work	[1]	[2]	[3]	[4]
Process	0.25μmGaN HEMT	0.5μmGaN HEMT	0.8μmGaN HEMT	0.5umGaAs pHEMT	SiGe PIN
Frequency (GHz)	8-12	7.5-13	8-12	7-12	7-11
Phase resolution (bits)	5	1	1	6	6
Insertion loss (dB)	14	5	2.5	7	14
Input return loss (dB)	7.6	11	10	10	10
Output return loss(dB)	6.5	11	10	N/A	10
RMS phase error (deg.)	6.4	N/A	N/A	8	N/A
RMS amplitude error (dB)	0.8	N/A	N/A	N/A	N/A
P_{1dB} input power (dBm)	34.8	38	N/A	22	3

it is the first time to report on the GaN-based 5-b phase shifters monolithic microwave integrated circuit (MMIC) with control logic circuits on-chip.

V. CONCLUSION

A high-power X-band GaN-based 5-b digital phase shifter with monolithic integrated E/D HEMTs control logic circuit is presented. The design of the phase shifters as well as the control logic circuit were described, and simulation results agree well with the measured results. The proposed phase shifters with control logic circuits were implemented in an integrated GaN E/D HEMTs process. From 8.5 to 11.5 GHz, all 32 states of the fabricated phase shifters exhibited an insertion loss of less than 11 dB, input–output return loss better than −10 dB, rms phase error less than 4.5°, and rms amplitude error less than 0.6 dB. Also of particular interest, the power handling capability of the phase shifters was $P_{1\ \mathrm{dB}} = 34.8$ dBm at 9 GHz. This paper implies the GaN-based MMIC has promising future in mixed signal processing application and can make T/R module more compact.

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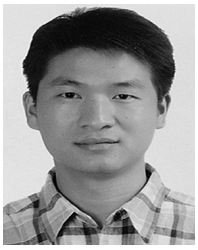

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