# A 26-GHz Vector Modulator in 130-nm SiGe BiCMOS Achieving Monotonic 10-b Phase Resolution Without Calibration

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***Abstract*— This paper presents a high-resolution (10-b) vevtor-modulator (VM) phase shifter (PS) in 130-nm SiGe BiCMOS targeting 5G applications at 26 GHz. It employs a Gilbert-cell RF core, the tail current of which is controlled by an 8-b low-power current-steering DAC and 2-b I/Q sign switches. The DAC includes an on-chip PTAT current reference with process compensation capabilities. A 2-stage RC polyphase filter (PPF) is used to generate the quadrature signals. Without any calibration or correction of PS control signals, the measured results demonstrate completely monotonic $2^{10}$ phase states, covering the full 0-360° range without any dead zones or overlapping phase states. The worst case (maximum) phase difference between any adjacent states is 0.65°. The VM exhibits an average insertion loss of 0.5 dB at 26 GHz with a 3-dB BW of 8 GHz, an rms amplitude error of 0.2 dB, $IP_{1dB}$ of 2 dBm, and 23 mW dc power dissipation. Potential applications are in RF beamforming and RF self-interference cancellation.**

***Keywords*— Vector modulator, phase shifter, SiGe, 5G**

## I. Introduction

Next-generation (5G) mobile wireless communications have challenging requirements such as peak data rate up to 20 Gbps and ultra-low user plane latency down to 1 ms. Several promising technologies such as mm-waves, small cells, phased arrays, full-duplex etc. have been investigated both by academia and industry in recent years to achieve these requirements [1].

SiGe technology has been the focus of research on 5G transceivers, due to its low cost, high integration capability, low noise and moderate output power performance, in comparison to CMOS and III-V technologies. Recently, several works on SiGe-based multi-channel RF beamforming 5G phased arrays have been reported [2]–[4].

Vector summation is a promising phase shifter topology for mm-wave 5G applications as it provides the highest bit resolution in a compact area. Despite the fact that many studies can be found in the recent literature on vector modulators [3]–[6], no work has been reported yet on high resolution vector modulators for 26 GHz 5G applications.

High resolution phase shifters are demanded to achieve precise beam steering in phased arrays, which will be crucial in overcoming increased path loss of mm-waves. For instance, 0.1° beam-steering resolution was reported in [7] using LO phase shifting. High resolution phase control is also critical in improving self-interference cancellation performance of full-duplex front-ends, widening the cancellation bandwidth, and even enabling hybrid technologies that combine full-duplex operation and beamforming [8].

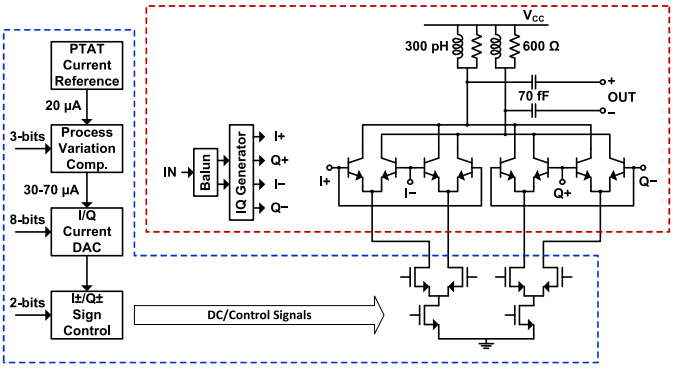


Fig. 1. The architecture of the process-compensated high-resolution (10-b) vector modulator phase shifter. Red box: RF part, blue box: dc/control part.

In this paper, we present a high resolution (10-b) vector modulator (VM) in 130 nm SiGe BiCMOS process for 5G applications at 26 GHz. The design employs a Gilbert-cell type core, an 8-b on-chip current-steering DAC to control the tail currents, a 2-b I/Q sign switches, an on-chip PTAT current reference, and a process compensation circuitry. The VM monotonically generates all the phases in 0-360° range without any dead zones, with a maximum 0.65° phase difference between any adjacent phase states. It can be configured as a state-of-the-art 8-b phase shifter with rms phase and amplitude errors of 0.2° and 0.2 dB, respectively.

## II. Circuit Design

The design of the vector modulator can be divided into RF circuitry and dc/control circuitry, as shown in Fig. 1. The RF part includes a balun, quadrature generator and Gilbert-cell type vector modulator; and the dc design part includes a PTAT current reference, process compensation circuitry, current steering DAC, and cascode tail current source.

### A. Transformer Balun

In order to achieve high linearity, the vector modulator uses a transformer balun instead of an active balun. At 26 GHz, transformer baluns are considerably small compared to transmission line based baluns. The design can be seen in Fig. 2. It converts a single-ended 50 Ω to differential 100 Ω. The 200 pH primary coil was realized by a single turn top-metal 2 trace of width 12-$\mu$m and inner diameter of 80-$\mu$m. The 440 pH secondary coil was realized by a two-turn top-metal 1 trace of width 10-$\mu$m and inner diameter of 43-$\mu$m. This

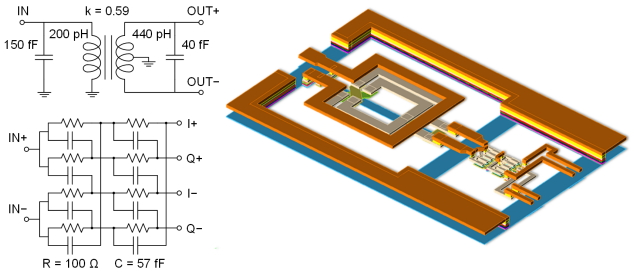


Fig. 2. The schematic and 3D layout view of the transformer balun and 2-stage RC polyphase filter.

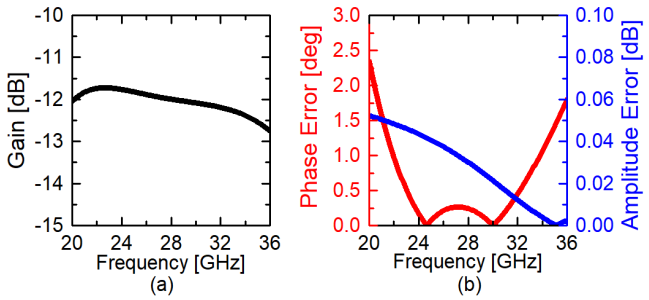


Fig. 3. The simulated (a) gain and (b) phase/amplitude imbalance of the cascaded transformer balun and 2-stage RC polyphase filter.

geometry produces a moderate magnetic coupling coefficient of $k = 0.59$ to enable a wideband matching performance. It was optimized to maximize the available power gain of the transformer. The 150 fF and 40 fF MIM capacitors tune out the coil inductances and perform the matching. Two 80 fF capacitors are used in series to ensure symmetry. The overall balun has a simulated insertion loss of 1.5 dB at 26 GHz.

### B. Quadrature Generator

The balun is followed by a 2-stage RC polyphase filter. Its advantages are good amplitude and phase balance between its outputs, high linearity, and very compact area; and its main disadvantage is insertion loss. A quadrature all-pass filter (QAPF) could have been used instead, providing significantly less insertion loss, but we preferred phase/amplitude balance advantage of the 2-stage PPF over the insertion loss advantage of QAPF. We used the constant amplitude configuration of the 2-stage RC PPF as shown in Fig. 2, where $R = 100\ \Omega$ and $C = 57$ fF. The actual layout implementation is slightly different than the schematic drawing to ensure symmetry and utilizes dummy resistors and capacitors for better device matching.

Fig. 3 shows the EM simulation results of the cascaded balun and quadrature generator. Its insertion loss is 12 dB at 26 GHz and input return loss is better than 10 dB from 20 to 36 GHz. By tuning the line lengths after the 2-stage PPF, the phase error was adjusted to exhibit two zero-crossings that were placed on separate sides of 26 GHz, as can be seen in Fig. 3(b), to maintain a good phase balance between the outputs even under process variations. The phase error is less than 1° in 22-34 GHz band and the amplitude error is negligible.

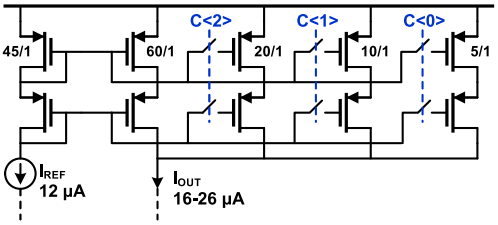


Fig. 4. Schematic view of the PMOS cascode current mirror with 3-b process compensation capability.

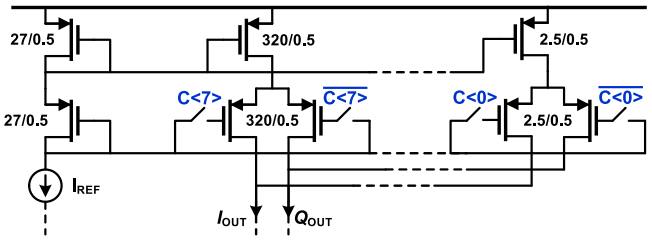


Fig. 5. Schematic view of the 8-b, PMOS, binary-weighted, current-steering DAC.

### C. Vector Modulator Core

Differential I and Q signals of the PPF are fed to the core of the vector modulator as shown in Fig. 1. The HBT sizes are $8 \times 0.48\ \mu$m and they are biased for a maximum tail current of 7.5 mA. The HBT sizes are chosen to provide a trade-off between power consumption and RF output power. The 300 pH shunt inductor and 70 fF series capacitor form the output matching network for a 100 Ω differential load, and a 600 Ω resistor is used to widen the output matching bandwidth. This type of modulator has the benefit of a constant power consumption that is independent of its setting and input drive power, unlike the current steering type modulators whose power consumption changes as a function of the phase setting. The tail current of the HBTs are provided by NMOS transistors. The bottom NMOS acts as a current source and the upper ones act as a sign switch for I and Q signal paths.

### D. DC Bias and Control Circuit

The performance of a high-resolution vector modulator strongly depends on its dc bias and control voltages. In this work, to tolerate process and temperature variations, dc bias and control voltages are generated by on-chip circuit blocks: a PTAT current reference followed by a 3-b process compensating PMOS current mirror, an 8-b current-steering DAC, and a cascode current mirror with 2-b sign switches.

The on-chip PTAT current reference has a nominal output current of 12 $\mu$A at room temperature. It draws 720 $\mu$A from a 2.5 V supply for a power consumption of 1.8 mW. To compensate for process variations, a PMOS cascode current mirror with 3-b control was used, as seen in Fig. 4. The output current of this stage is in the range of 16-26 $\mu$A, i.e. a 21 $\mu$A nominal current with $\pm 25\%$ tunable range.

The critical part of the dc/control circuitry is the current steering DAC. It is based on cascode PMOS current steering topology, as shown in Fig. 5. The sizes of PMOS transistors

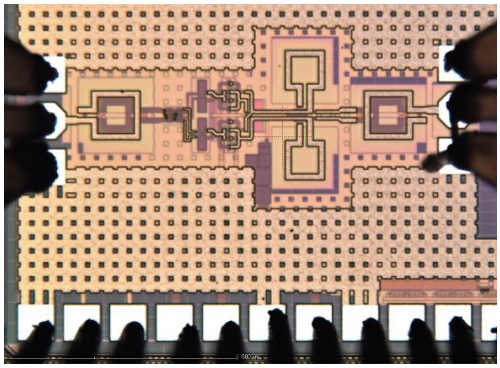

Fig. 6. Die photo.

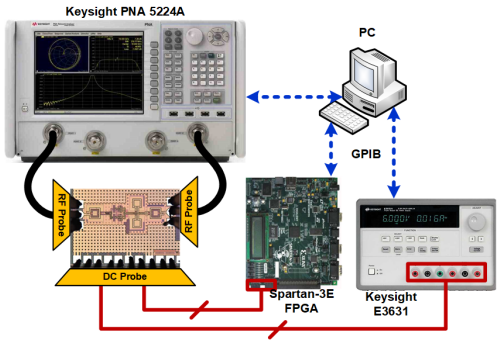


Fig. 7. Measurement setup of the vector modulator.

in each DAC cell are binary weighted between $W/L = 2.5\mu\text{m}/0.5\mu\text{m}$ and $320\mu\text{m}/0.5\mu\text{m}$. The long channel devices ($L = 0.5\ \mu\text{m}$) help increase the linearity of the DAC. The maximum output current of the DAC is 500 $\mu$A.

The final part of the dc/control circuitry is NMOS cascode current mirrors to provide the tail currents of the Gilbert-cell type vector modulator, as shown in Fig. 1. The common-source transistors are sized $10/0.5\ \mu\text{m}$ and $150/0.5\ \mu\text{m}$, and the common-gate transistors are sized $6/0.13\ \mu\text{m}$ and $90/0.13\ \mu\text{m}$, to provide a maximum tail current of $500\ \mu\text{A} \times 15 = 7.5$ mA. The common gate transistors are controlled via 2-b NMOS sign switches.

## III. Measurement Results and Discussion

The PS is fabricated in IHP SG13S BiCMOS technology. The process offers HBTs with an $f_T/f_{max}$ of 250/340 GHz, CE breakdown voltage of 1.6 V, 5 thin and 2 thick top metal layers, and 1.2 V logic and 3.3 V I/O CMOS. The chip micrograph is shown in Fig. 6. It includes input/output baluns for single-ended measurements. The IC also features a custom-designed SPI for the 10-b phase and 3-b process compensation controls. All digital pads include ESD protection circuitry. The chip area is $0.8 \times 0.6 = 0.48$ mm$^2$, excluding the pads; and the core area is $0.4 \times 0.6 = 0.24$ mm$^2$, excluding the baluns.

The pad-to-pad S-parameters are measured with a PNA N5224A network analyzer and an RF probe station, using the setup shown in Fig. 7. 100-um GSG Z-probes are used for the input/output, and the supply/digital controls are provided by a GGB dc probe.

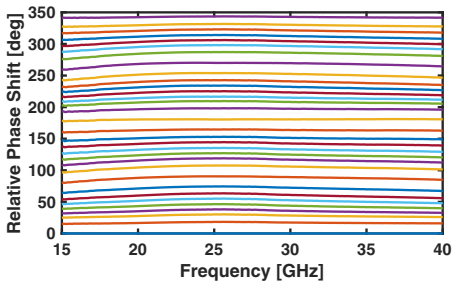


Fig. 8. Measured relative phase shifts of the VM for different states. Only 32 major states are shown for clarity.

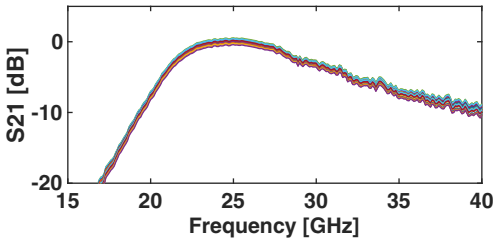


Fig. 9. Measured gain of the VM for all states.

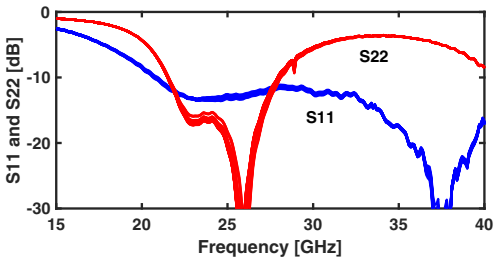


Fig. 10. Measured input and output matching for all phase states.

Fig. 8 shows the relative insertion phase across different phase settings. Here, only the 5-MSB control is swept to display the phase shifts for brevity and clarity. These results are obtained without any phase calibration. These phase shifts do not correspond to a 5-b phase shifter, since the DAC in this work was implemented in a binary fashion. Nevertheless, if these phase states are treated as the states of a 5-b phase shifter, the VM achives 4-5° rms phase error without any calibration. The other 5-LSB control can easily be used to improve the performance the phase shifter. For instance, we were able to synthesize an 8-b phase shifter with 0.2° rms phase error, which is a state-of-the-art performance.

Fig. 9 shows the measured insertion gain across different phase settings. After deembedding the combined 3 dB loss of the input/output baluns that were separately measured, the average loss is around 0.5 dB, with an rms gain error of 0.2 dB. Input/output of the PS is well-matched to 50 Ω, as seen in Fig. 10, which is predominantly determined by the baluns. The measured group delay is around 40 ps at 26 GHz center frequency.

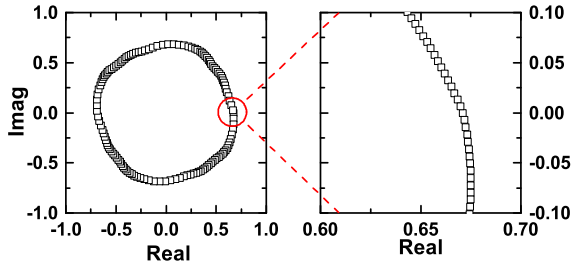


Fig. 11. Measured constellation of S21 at 26 GHz. (Left) One out of eights states is shown for brevity. (Right) Zoomed in version showing all the states.

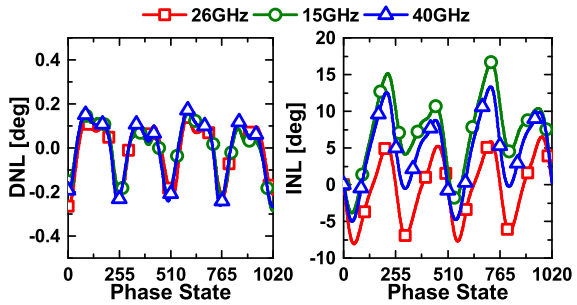


Fig. 12. Measured INL and DNL for the vector modulator.

Our aim in this work was to obtain perfectly monotonic phase states. We measured all the $2^{10} - 4$ phase states, and observed perfectly monotonic phase shifts, without any dead zones from 0 to 360°. ($-4$ is due to the four redundant phase states in $I/Q_{\pm}$ transitions). Fig. 11 shows the S21 constellation, and its zoomed-in version. The measured worst case (largest) phase difference between any adjacent states is $0.65°$. As would be expected and can be seen in the figure, these largest gaps occur around the quadrature reference vectors.

Fig. 12 shows the DNL and INL of the VM for each 1020 control code, at three different operating frequencies, treating the VM as a digital-to-phase conterter. For almost all control codes, the measured DNL is between $\pm 0.2°$ and its worst case value is $-0.3°$, meaning the phase states are completely monotonic. The best INL performance is obtained at the center frequency (between 5 and $-8°$) and it degrades further for higher/lower frequencies. This INL performance was expected, though, since the DAC cells were binary weighted. The target application of this work was adaptive self-interference cancellation in full-duplex radios, which requires good DNL but not INL.

The vector modulator core draws 7.5 mA from a 2.5 V supply. The total power consumption is 23 mW including the dc biasing and control circuitry.

For completeness, Table 1 compares state-of-the-art silicon VMs at 26-28 GHz. Two versions are included in the table for this work. The 5-b version represents the uncalibrated PS performance obtained by sweeping only the 5-MSBs, without using the other 5-b control. The 8-b version represents the PS that was synthesized after measuring all the phase states. The presented work achieves the highest resolution and linearity

Table 1. State-of-The-Art Silicon-Based Vector-Modulators at 26-28 GHz

| Reference | **This W.** | [3] | [4] | [5] | [6] |
|---|---|---|---|---|---|
| Technology | **130nm SiGe** | 180nm SiGe | 130nm SiGe | 130nm CMOS | 180nm CMOS |
| Phase Resolution | **8-b/5-b** | 6-b | 4-b | 6-b | 4-b |
| Phase Err. [°rms] | **0.2/4** | 3.4 | 5.4 | 2.6 | 1.5 |
| Gain [dB] | **−0.5** | 1 | 10.5 | −5 | −15 |
| Gain Err. [dB rms] | **0.2** | 0.5 | 0.6 | 0.31 | 0.45 |
| NF [dB] | **17** | 12 | 7 | 18 | 15 |
| $IP_{1dB}$ [dBm] | **2** | −7 | −17 | −10 | 12 |
| $P_{DC}$ [mW] | **23** | - | 136 | 27 | 0 |
| Chip Area [$mm^2$] | **0.45** | - | 0.3 | 0.3 | 0.31 |

(as [6] is fully passive), lowest rms phase/gain error, and comparable performance in other aspects.

## IV. Conclusion

A 26-GHz high-resolution (10-b) vector modulator in 130-nm SiGe have been presented. High resolution is obtained by an on-chip current steering DAC and process compensation circuitry. High linearity is achieved via a transformer balun and 2-stage RC PPF. The modulator achieved, without any calibration, completely monotonic phase states in 0-360° range without any dead zones or overlapping phase states, with a maximum $0.65°$ phase difference between any adjacent states. It has an average 0.5 dB insertion loss, 0.2 dB rms gain error, 2 dBm $IP_{1dB}$, and 23 mW dc power consumption. These state-of-the-art measured results are promising for 5G phased array transceivers and self-interference canceling circuits.

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