A Temperature Compensated Variable Gain Phase Shifter Based on GaN HEMTs

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***Abstract*— This paper presents a temperature compensated variable gain phase shifter (VGPS), composed of an active phase shifter followed by a variable gain amplifier (VGA). A temperature sensor adjusts the biasing of the phase shifter block and suppresses temperature effects on its insertion phase. Further, a self-compensation mechanism compensates the gain reduction at the VGA stage. The circuit is designed and laid out in 0.15 µm GaN HEMT technology. Post layout simulation results show that the proposed VGPS achieves over 180 °C of the relative phase shift for the frequency range of 4.5 to 5 GHz over the temperature ranging from 25 °C to 250 °C. The gain of the VGPS can be controlled from 5 dB to 17 dB.**

Keywords—high temperature, RFIC, phased array, phase shifter, GaN, variable gain amplifier (VGA).

I. Introduction

The operating temperature in high temperature applications such as oil and gas well logging, military, geothermal energy exploitation and space exploration can exceed 200 °C [1]. This necessitates high temperature electronics to reliably operate at those temperatures with adequate lifetime. The circuits on silicon do not meet the requirements at temperatures above 200 °C due to temperature runaway. The failure rate of silicon-based circuits doubles for every 10 °C increase in the temperature above 200 °C [1]. On the other hand, gallium nitride (GaN) on silicon carbide (SiC) transistors can operate reliably at temperatures up to 450 °C, thanks to their larger energy band gap compare to silicon devices [2].

Phased array transceivers are widely applied in telecommunications due to the capability of high-speed communications through fast beam steering [3]. The advantage of phased arrays may be exploited for high temperature applications. However, to our knowledge, all existing high temperature circuits and systems published in open literature are designed for traditional RF frontends (i.e. single transceivers). The power amplifiers of a phased array operating at mm-wave drastically drops in power efficiency, to result in large radiated power and hence heat.

The phase shifter is one of the main blocks of a phased array system. The performance of a phase shifter is sensitive to the overall system performance. Moreover, designing a high temperature phase shifter can be challenging, since the temperature effects can degrade main characteristics of the phase shifter (i.e., insertion phase and gain).

A phase shifter can be active or passive in its structure [4]-[7]. The active structure is usually compact in size, but it dissipates dc power [4]-[5]. On the other hand, the passive structure is highly linear and does not dissipate dc power, but it is lossy and bulky in area [6]-[7]. From the perspective of high temperature functionality, an active circuit could be more suitable, since the substrate expansion due to high temperature has little effect on its performance [8]. Further, an active circuit usually requires a smaller number of transistors compare to the number of switches used in the counterpart passive structure, which leads to easier temperature compensation.

Another important block in the transceiver chain is the variable gain amplifier (VGA). Variation in temperature can change the VGA gain by affecting the transconductance of the transistors. It has detrimental effect as the efficiency and linearity of the power amplifier is dependent on the gain from the preceding VGA. Therefore, compensation is necessary to stabilize the VGA gain over the operational temperature range and suppress the influence of the temperature on its performance.

In this paper, we propose a variable gain phase shifter composed of an active phase shifter and a VGA stage. A temperature compensation method is adopted to each block to reduce the temperature effect. To our knowledge, this is the first temperature compensated phase shifter block published in open literature.

The paper is organized as follows: Section II reviews existing phase shifters and VGAs and presents a design procedure for the proposed ones. Section III introduces the post layout simulation results. Section IV concludes the work.

II. Proposed Design

A. Phase Shifter

Sussman-Fort presented a phase shifter based on an all-pass filter with a fixed insertion phase [11]. Viveiros et al. modified the configuration, so that the circuit is able to achieve a tunable insertion phase [12]. The transmission line Z is replaced with a series of an inductor and a varactor in [12]. A pseudomorphic high electron-mobility transistor (pHEMT) is adopted as the varactor, and the source bias voltage is utilized to tune the equivalent capacitance. The compact structure can achieve the required phase shift, which is suitable for high temperature applications. However, a compensation mechanism is necessary to suppress the performance variation with temperature. Although the circuit in [12] provides a wide range of the phase shift, a tradeoff between gain and phase sensitivity limits the flexibility in design.

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The schematic diagram of the proposed phase shifter is shown in Fig. 1 (a). A close investigation of the circuit reveals that the gain of the phase shifter is proportional to (R_2/R_3), while the sensitivity of the insertion phase of the phase shifter transfer function to the varactor capacitance is proportional to (R_3/R_2). This indicates a larger variation in the varactor capacitance is required to achieve a high gain. However, a larger varactor increases parasitics and limits the minimum capacitance, resulting a smaller phase shift range.

To break the aforementioned tradeoff, Z is replaced by a parallel LC tank for the proposed circuit as shown in Fig. 1 (b). A gallium nitride (GaN) on silicon carbide (SiC) high electron mobility transistor (HEMT) is employed as the variable capacitor. Assuming matched condition at the input of the phase shifter and using the simplified transistor equivalent model in [12], the transfer function of the phase shifter can be expressed as follows.

$$S_{21} = K \cdot \frac{s^2 - \frac{R_2}{CR_1R_3}s + \frac{1}{LC}}{s^2 + \frac{1+g_{m_2}R_3}{C(R_1+R_3+g_{m_2}R_1R_3)}s + \frac{1}{LC}} \tag{1}$$

$$K = \frac{2g_{m_1}g_{m_2}R_1R_3R_L}{R_1+R_2+R_3+g_{m_2}R_2R_3} \tag{2}$$

where C is the equivalent capacitance of the varactor and g_{m_1} and g_{m_2} are the transconductance of the GaN HEMT Q_1 and Q_2, respectively. The transfer function of a second order all-pass filter is given as

$$T(s) = \frac{s^2 - \frac{\omega_0}{Q}s + \omega_0}{s^2 + \frac{\omega_0}{Q}s + \omega_0} \tag{3}$$

where ω_0 is the natural frequency of the filter and Q its quality factor. The phase shift in (3) can be expressed as

$$\phi = 2\tan^{-1}\left[Q\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right] \tag{4}$$

Comparing (1) with (3), the condition in (5) must be satisfied for (1) to behave as an all-pass transfer function.

$$R_1 = R_2 \cdot \frac{R_2+R_3}{R_3-R_2+g_{m_2}R_3(R_3-R_2)} \tag{5}$$

which leads to

$$Q = \frac{C\omega_0R_3(R_2+R_3)}{R_3-R_2+g_{m_2}R_3(R_3-R_2)} \tag{6}$$

By substituting (6) in (4), the phase variation of the circuit can be obtained as a function of design parameters. The magnitude of S_{21} and derivative of (4) (i.e. $\partial\phi/\partial C$) are plotted in Fig. 2. The hachured area is unacceptable, since R_1 becomes negative. Both gain and phase sensitivities increase by decreasing the (R_2/R_3) ratio, and the tradeoff between the gain and sensitivity no longer works. Assuming the center frequency of 5 GHz, the proposed circuit achieves around 7 dB higher gain than the proposed circuit in [12] for the same inductor, transistor transconductance, and capacitance range of the varactor.

Although the performance of the proposed circuit is satisfactory at room temperature, the temperature effects can degrade its performance at high temperatures. Fig. 3 shows the variations in g_m of the GaN HEMT with temperature. The peak of the transconductance drops by 37% from 25 ℃ to 250 ℃. The effect of the g_m variation on the phase and gain of the phase shifter can be investigated with help of (1) and (4). Fig. 4 shows the variations of the gain and the phase shift around the center frequency. The small signal gain decreases by 2.3 dB and 25% for the phase shift, assuming both transistors have the same transconductance.

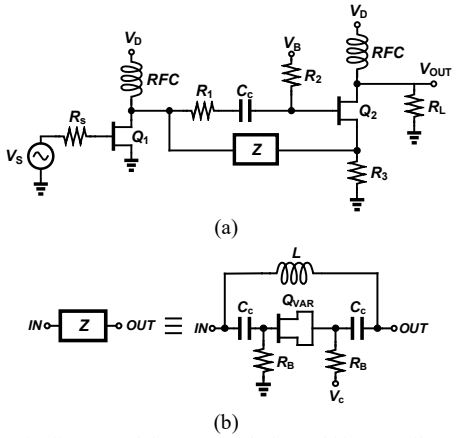

Fig. 1. Schematic diagram of the proposed phase shifter (a) all-pass filter, (b) equivalent circuit for the impedance Z.

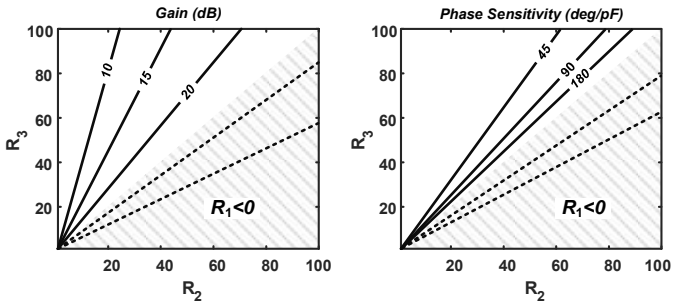

Fig. 2. Dependency on R_2 and R_3 (a) gain, (b) phase sensitivity.

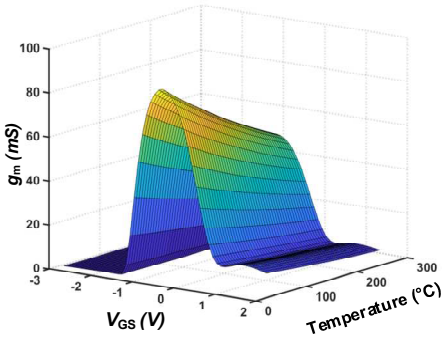

Fig. 3. Temperature effect on the transconductance of the GaN HEMT.

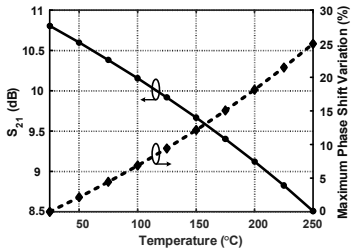

Fig. 4. Gain and phase shift with temperature.

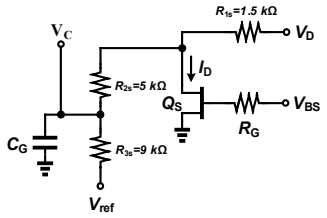

Fig. 5. Schematic of the temperature sensor.

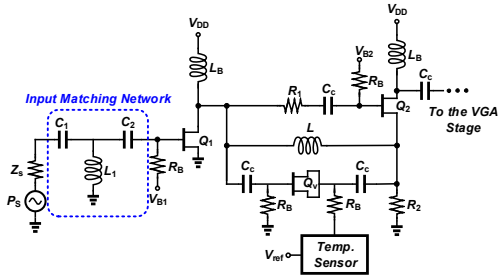

Fig. 6. Schematic of the proposed phase shifter.

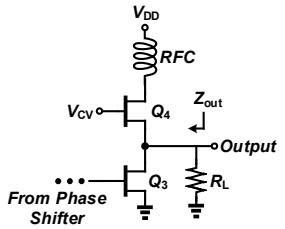

Fig. 7. Simplified schematic of the proposed VGA.

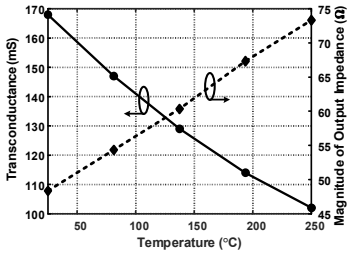

Fig. 8. Variation in the transconductance of the main transistor Q_3 and the output impedance of the VGA.

By taking a derivative from (4) and setting it equal to zero, the optimum capacitance of the varactor is obtained as

$$C_{opt} = C_0 - \alpha(T - T_0) \tag{7}$$

$$\alpha = 0.11\ fF/°C \tag{8}$$

where C_0 is the capacitance value at room temperature, α is capacitance reduction factor, T is absolute temperature and T_0 is room temperature in centigrade. α in (8) is translated to 50 mV decrease in the control voltage of the varactor for a 2×100 µm GaN HEMT.

The temperature sensor in Fig. 5 is adopted to generate the control voltage of the varactor. The transistor Q_s experiences the same temperature variations as the main transistors $Q_{1,2}$ and changes the drain current I_D accordingly. The resistors R_{2s} and R_{3s} shift the dc level of the drain voltage and store it across the capacitance C_G to provide an adaptive control voltage for the varactor. The reference voltage V_{ref} is used to sweep the capacitance of the varactor by changing the dc level of the control voltage. The sensor circuit dissipates dc power of 9 mW from the 5 V voltage supply.

Fig. 6 shows the complete schematic diagram of the temperature compensated phase shifter, where L_B is bias RF choke and C_C the coupling capacitor. The input matching network is optimized to match the input impedance to the source impedance over the frequency range from 4.5 GHz to 5 GHz. The size of the varactor Q_v is chosen to have a capacitance range from 0.4 pF to 0.75 pF.

B. VGA

The VGA gain should be set appropriately to obtain high efficiency and sufficient linearity for the power amplifier block and compensate the loss for the phase shifter block. The VGA gain is a strong function of the g_m of the main transistor, and hence the overall system performance is sensitive to g_m. Ehteshamuddin et al. proposed a high temperature VGA using GaN HEMTs that can operate at the temperature ranging from room temperature to 230 °C [14]. The transistor is biased at the near transconductance zero-temperature coefficient (GZTC) to minimize the gain variation with temperature. However, the temperature influence on the cascode transistor is ignored. which does not achieve good temperature compensation. Hussain et al. proposed a two stage VGA based on 4H-silicon carbide (4H-SiC) bipolar junction transistors (BJTs). The circuit is measured at the temperatures up to 300 °C [10]. The variation in the gain is relatively large with more than 5 dB over the entire temperature range, since temperature compensation is implemented along with the VGA.

Fig. 7 shows the simplified schematic of the proposed VGA. Transistor Q_4 (2×25µm) controls the current flowing into the drain of the main transistor Q_3 (4×100µm). Variation in the g_m of Q_3 could cause variation in the gain. However, the temperature has an opposite effect on the channel resistance of Q_4, in which g_m reduces with temperature while the channel resistance increases. The size of $Q_{3,4}$ is set appropriately, so that the g_m of Q_3 achieves the target gain and the g_m of Q_4 satisfies the compensation criteria. In addition, the g_m of Q_3 is chosen two times larger than the g_m for $Q_{1,2}$. Resultantly, only one temperature sensor for the VGA can compensate the gain variation of the phase shifter instead of two sensors necessary to adjust the bias voltages of $Q_{1,2}$. Also the required increment ratio of the sensor output voltage can be smaller than the ratio of two temperature sensors for the phase shifter, which saves power dissipation of the sensor.

Fig. 8 shows simulation results on the variation in the g_m of Q_3 and the output impedance of the VGA. As temperature increases, the gain decreases, but the impedance increases. It

leads to reduction in the gain variation of the VGA with temperature. Fig. 9 shows the schematic of the VGA. Similar to the phase shifter, the input matching network is optimized to match to the source impedance over the frequency range from 4.5 GHz to 5 GHz. To adaptively adjust the gate voltage of Q_3, a temperature sensor similar to the one in Fig. 5, but with a lower increment rate, is employed. A reference voltage V_{ref} is used for the calibration of the sensor. The sensor dissipates only 7 mW under the 5 V supply.

III. Post Layout Simulation Results

The entire circuit, including the phase shifter and the VGA, is laid out using Wolfspeed Cree GaN HEMT and is shown in Fig. 10. The process offers the minimum channel length of 0.15 µm and the minimum gate width of 25 µm. Fig. 10 shows the layout of the proposed variable gain phase shifter (VGPS) and the VGA. The die size of the circuit is 4.96 mm^2. EM simulation is performed using Keysight Momentum. Fig. 11 shows the input and output S-parameters of the VGPS. It is observed that S_{11} stays below -10 dB over the frequency range of interest (i.e. 4.5 to 5 GHz), while S_{22} exceeds -10 dB at a portion of the frequency range.

Fig. 12 (a) presents the insertion phase of the proposed circuit for the frequency range of 4.5 to 5 GHz. The maximum phase variation with temperature is below 6% for the control voltage V_C = -1 V, while it was observed about 25% for the original circuit. (Refer to Fig. 5 for the control voltage V_C.) Further, the range of the insertion phase remains above 180° over the entire frequency range. Fig. 12 (b) shows the gain of the circuit. The gain variation is below 1 dB at the low gain under V_{CV} = 0 V and increases to around 1.5 dB at the high gain under V_{CV} = 2 V (Refer to Fig. 9 for the control voltage V_{CV}.) This is mainly due to the fact that the higher gain is more sensitive to the variation of the transconductance g_m. The proposed circuit is able to control the gain over 12 dB by changing the control voltage V_{CV} from 0 V to 2 V.

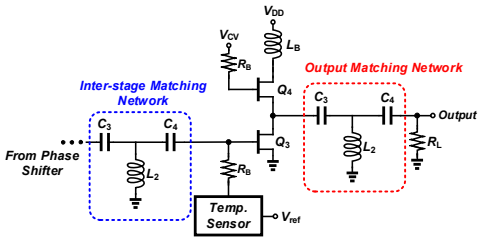

Fig. 9. Schematic of the proposed VGA.

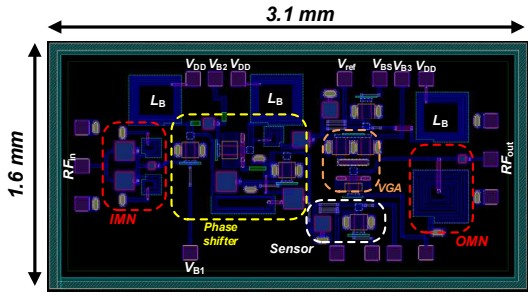

Fig. 10. Layout of the proposed variable gain phase shifter and the VGA.

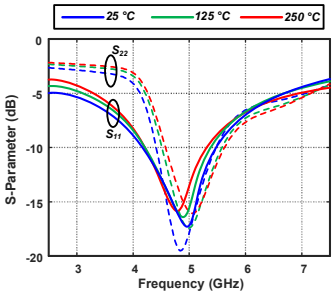

Fig. 11. Input and output S-Parameters versus frequency.

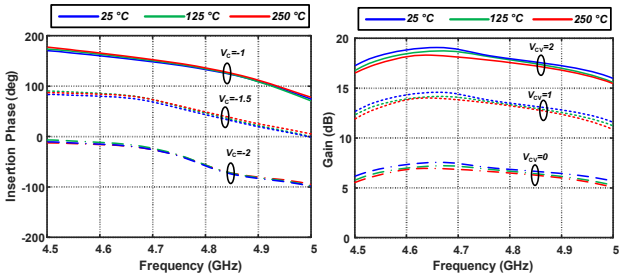

Fig. 12. Performance of the proposed circuit versus frequency at different temperatures (a) Insertion phase (b) gain.

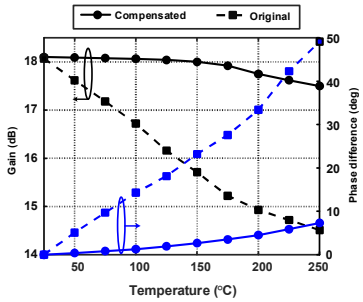

Fig. 13. Gain and phase variation of the original and compensated VGPSs at the frequency of 5 GHz.

Fig. 13 compares the variations of the gain and the insertion phase at 5 GHz against the original one without temperature compensation. The variation of the gain for the original circuit is 3.7 dB for the temperature range, while it is reduced to 0.8 dB for the compensated one. The variation of the insertion phase is 50 degrees for the original circuit, but reduced to 9 degrees for the compensated one. The noise performance of the circuit is also simulated at 5 GHz for temperature of 250 °C. The noise figure (NF) of the original circuit is 16.4 dB at 25 °C, while it is reduced to 15.7 dB at 250 °C for the compensated one. This can be attributed to the reduction of the channel noise of the main transistors by temperature due to reduction in the channel transconductance. Finally, the maximum power dissipation is about 350 mW for the phase shifter under 5 V supply and 465 mW for the VGA under 15 V supply, resulting total power dissipation of 815 mW for the proposed circuit.

IV. Conclusion

A high temperature variable gain phase shifter circuit is proposed in this paper. An effective temperature compensation method is employed at each block to compensate the temperature effects on the overall performance of the circuit. The post layout simulation results show that the performance variation due to the temperature is significantly suppressed with the proposed temperature compensation methods.

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