An Improved Wideband All-Pass I/Q Network for Millimeter-Wave Phase Shifters

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***Abstract*—This paper presents the design and analysis of an improved wideband in-phase/quadrature (I/Q) network and its implementation in a wideband phased-array front-end. It is found that the addition of two resistors (R_s) in the all-pass I/Q network results in improved amplitude and phase performance versus capacitance loading and frequency, which is essential for wideband millimeter-wave applications. A prototype 60–80-GHz phased-array front-end based on 0.13-μm SiGe BiCMOS is demonstrated using the improved quadrature all-pass filter and with 4-bit phase-shifting performance at 55–80 GHz. Application areas are in wideband millimeter-wave systems.**

***Index Terms*—Active phase shifter, beam-forming network, BiCMOS analog integrated circuit, in-phase/quadrature (I/Q) network, phase shifter, phased array, quadrature network, smart antenna.**

I. Introduction

ELECTRONIC phase shifters are essential for phased arrays, and have been implemented using passive and active networks in CMOS and SiGe technologies [1]–[19]. The active approach is based on an in-phase/quadrature (I/Q) network, and phase interpolation is achieved by adding the I/Q signals with appropriate amplitudes and polarities (Fig. 1) [11]–[19]. A low-loss accurate I/Q network is therefore an important circuit element of the active approach for precise phase shifting. To circumvent the loss in traditional *R–C*-based passive quadrature generators such as *RC–CR* bridge or *R–C* polyphase filters, a new quadrature all-pass filter (QAF) based on an *L–C* series resonator was proposed in [16]. The QAF utilizes a second-order series resonance and provides a wideband quadrature signal with maximum 3-dB voltage gain, and has been implemented in several wideband phased-array chips [14]–[19].

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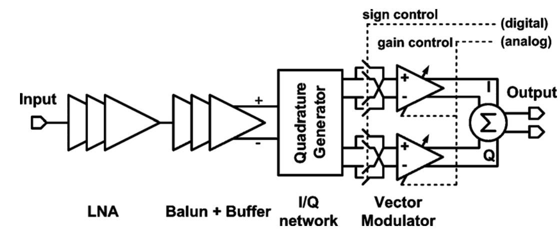

Fig. 1. Active phase-shifter architecture.

However, at millimeter waves, the QAF loading capacitance due to the vector modulator can be comparable to the internal QAF capacitance, and this results in significant I/Q errors. In fact, this problem was known in [16], and it was recommended that the loading capacitance (C_L) be chosen to be 0.1–0.2 of the filter capacitance (C) for reduced phase errors. At millimeter-wave frequencies, this is not possible in many cases, and therefore, an improved QAF network that is not sensitive to the loading capacitance is required. This paper presents the analysis of such a network, and its implementation in a wideband 60–80-GHz phased-array front-end.

II. Active Phase-Shifter Architecture

The active phase-shifter architecture is presented in Fig. 1. An I/Q network and two variable gain amplifiers (VGAs) are used in a differential mode for sign reversal, and the VGA outputs are summed in the current domain to create the final vector with arbitrary phase shift. The output phase relies on the gain *ratio* between the I- and Q-paths, and this results in a robust design against process, supply voltage, and temperature variations. Phase synthesis based on the interpolation of quadrature vectors is a linear operation and is independent of frequency, guaranteeing wideband operation. The fundamental limitation of the phase accuracy and the operating bandwidth is given by the quadrature network.

A. Analysis of Phase Synthesis Based on Signal Interpolation

To investigate the effect of the amplitude and phase errors in the quadrature network on the output phase accuracy, define a quadrature signal set as $S_{IQ} = \{V_I, V_Q\} = \{A\angle 0^\circ, A\Delta A\angle(90 + \Delta\theta)^\circ\}$, where ΔA and $\Delta\theta$ are the I/Q amplitude mismatch and phase imbalance of the basis I/Q vectors V_I and V_Q, respectively. The linear combination of the reference vectors is $V_{\text{out}} = G_I A\angle 0^\circ + G_Q A\Delta A\angle(90+\Delta\theta)^\circ$,

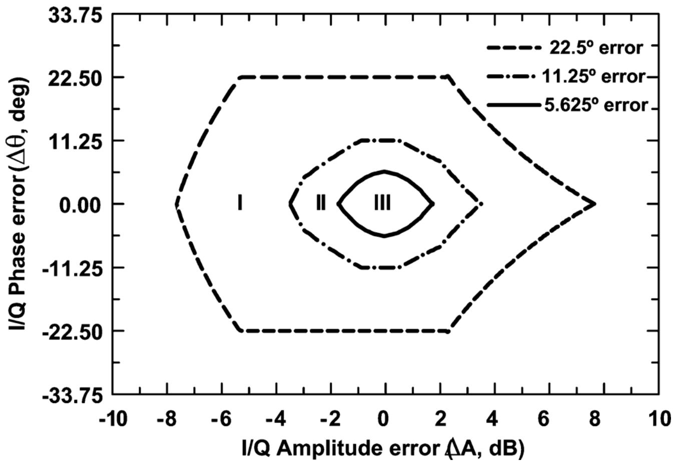

Fig. 2. Contour plot of I/Q errors (quadrature phase error, $\Delta\theta$, and amplitude mismatch, ΔA) in a quadrature network for 3-bit (region I, $\theta_{\rm error} < 360^\circ/2^4 = 22.5^\circ$), 4-bit (region II, $\theta_{\rm error} < 360^\circ/2^5 = 11.25^\circ$) and 5-bit (region III, $\theta_{\rm error} < 360^\circ/2^4 = 5.625^\circ$) operation.

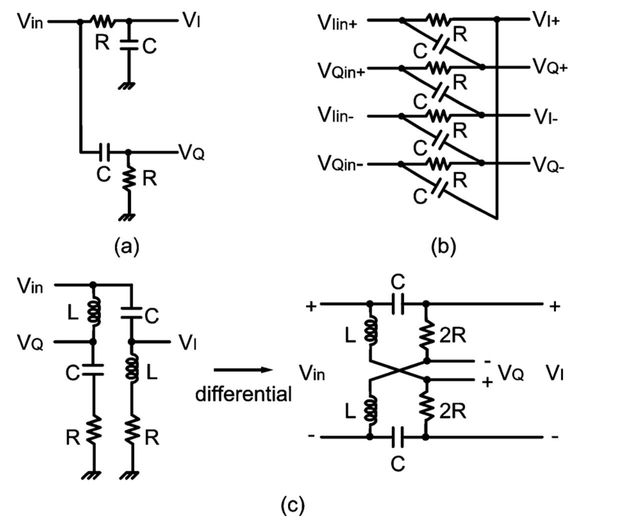

Fig. 3. (a) Typical *R–C*-based lumped passive quadrature networks: *RC–CR* network, (b) *R–C* polyphase filter (one stage), and (c) *L–C* resonance-based quadrature networks. The differential version is called the QAF filter [16].

where G_I and G_Q are amplitude weights determined by the output phase $\theta_{\rm out} = \tan^{-1}(G_Q/G_I)$. The phase error ($\theta_{\rm error}$) and amplitude error ($M_{\rm error}$) of the output signal are given by (1) and (2), respectively,

$$\theta_{\rm error}|_n = \tan^{-1} P_n - \tan^{-1}\left(\frac{P_n \Delta A \cos\Delta\theta}{1 - P_n \Delta A \sin\Delta\theta}\right) ({\rm deg}). \quad (1)$$

$$M_{\rm error}|_n = 10\log\left(\frac{1 + (P_n\Delta A)^2 - 2P_n\Delta A \sin\Delta\theta}{1 + P_n^2}\right) ({\rm dB}). \quad (2)$$

where $P_n = (G_Q/G_I)_n = \tan(n360^\circ/2^N)$ with N = number of phase bits, and $n = 0, 1, 2, \ldots, 2^N - 1$ ($0 \le P_n \le \infty$, $P_n = 0$ for $\theta_{\rm out} = 0^\circ$, $P_n = 1$ for $\theta_{\rm out} = 45^\circ$ and $P_n = \infty$ for $\theta_{\rm out} = 90^\circ$).

When $P_n = \infty$ ($+90^\circ$ phase bit), $\theta_{\rm error} = \Delta\theta$ and $M_{\rm error} = 20\log\Delta A$, respectively, consistent with intuition ($\tan^{-1} x \simeq \pi/2\text{-}1/x, \text{if } x \gg 1$). $\theta_{\rm error}$ should be $< 360^\circ/2^{N+1}$ to avoid any phase overlap between different phase bits, guaranteeing N-bit phase resolution. Fig. 2 presents contour plots of ΔA and $\Delta\theta$ for several cases of $\theta_{\rm error}$. To achieve 3-, 4-, and 5-bit accuracies, the I/Q errors should be inside regions I–III, respectively. For example, for 5-bit phase accuracy, $|\Delta\theta|$ needs to be less than 5° with a maximum of ± 1.5 dB of I/Q amplitude error in the quadrature network.

III. Quadrature Signal Generation

A. R–C-Based and L–C Resonator Quadrature Generators

The traditional *RC–CR* network has been widely used for narrowband quadrature signal generation [see Fig. 3(a)]. To extend the operation bandwidth, multistage *R–C* polyphase filter of which a single stage is shown in Fig. 3(b) has been used. However, the limitation of these I/Q networks is the loss, which tends to increase significantly with the number of stages for wideband operation. Therefore, the main applications of these networks are in high signal routes such as local oscillator (LO) or IF rather than the RF path [20]–[22].

Quadrature signals can also be generated without any voltage loss using an *L–C* resonance technique, which is shown in Fig. 3(c) for the single-ended version (where $R = \sqrt{L/C}$ $\{Q = \sqrt{L/C}/R = 1\}$ and $\omega_o = 1/\sqrt{LC}$). The transformation to a differential all-pass network having equal I and Q magnitude ($|V_{I\pm}| = |V_{Q\pm}|$) for all ω and wider bandwidth (due to lower Q factor), called a QAF, is described in [16]. The transfer function of the QAF is

$$\begin{bmatrix} V_{I\pm} \\ V_{Q\pm} \end{bmatrix} = V_{\rm in} \times \begin{bmatrix} \pm\dfrac{s^2 + \dfrac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \dfrac{2\omega_o}{Q}s + \omega_o^2} \\ \mp\dfrac{s^2 - \dfrac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \dfrac{2\omega_o}{Q}s + \omega_o^2} \end{bmatrix} \quad (3)$$

where $s = j\omega$. For practical applications with $0.8 \le Q \le 1$, the QAF results in 2–3-dB voltage gain over a wideband frequency range (3:1), which is much better than the *R–C*-based I/Q networks [16]. The QAF can generate any phase difference between two outputs by changing the resistor value (R) in Fig. 3(c): i.e., in general, the replacement of $2R$ with $2R \times \xi$ will generate $2 \times \tan^{-1}(1/\xi)$ of phase difference between the output ports.

B. Performance Comparison

Fig. 4 shows the performance comparison between the polyphase filters and the QAF, when driven by ideal voltage source and with no capacitance loading. For a fair comparison, the polyphase filters are also driven in an all-pass mode where the quadrature-phased differential input, $V_{Q{\rm in}\pm}$, is tied to the in-phase differential input, $V_{I{\rm in}\pm}$ in Fig. 3(b), resulting in equal I/Q amplitude for all ω and quadrature phase splitting at the pole frequency ($= 1/RC$) [22]. The poles of each stage in the two- and three-stage polyphase filters are also set at the

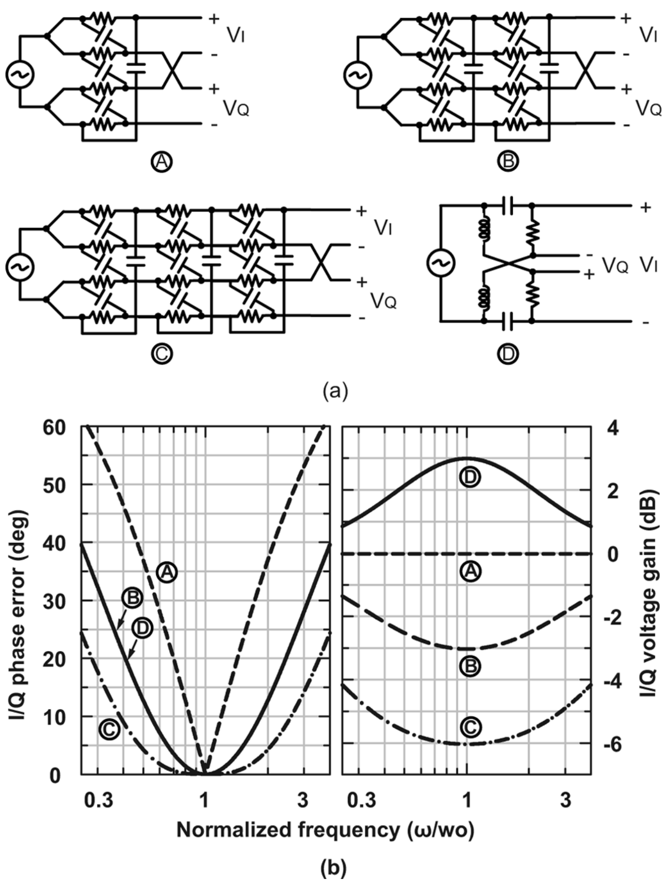

Fig. 4. Performance comparisons between quadrature networks. (a) *R–C* one-, two-, and three-stage polyphase filters (Ⓐ, Ⓑ, and Ⓒ) and QAF (Ⓓ). (b) Quadrature phase error and gain characteristics versus normalized angular frequency for the QAF and polyphase filters. $R = 20\ \Omega$, $C = 113.68$ fF, $L = 45.47$ pH, and $f_o = 70$ GHz.

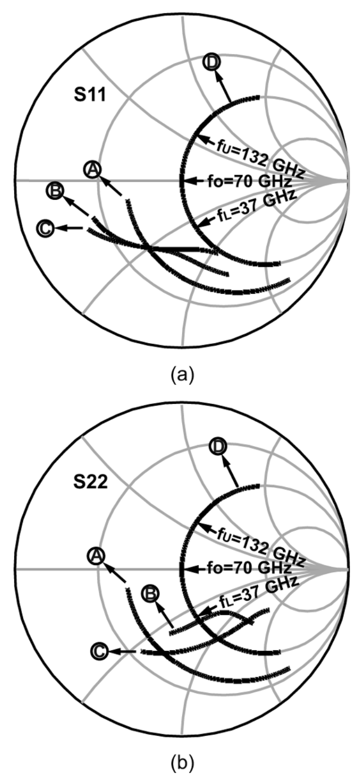

Fig. 5. Input and output impedance of the I/Q networks shown in Fig. 4. (a) Input differential impedance and (b) output differential impedance for one of the I/Q outputs. For QAF, $S_{11} < -10$ dB and $S_{22} < -10$ dB at 37 GHz ($0.53\ f_o$) to 132 GHz ($1.88\ f_o$).

same value. The three-stage polyphase filter shows the widest I/Q phase bandwidth at the expense of high loss. The I/Q phase-error characteristic of the QAF is equivalent to that of the second-order polyphase filter, but the QAF achieves 6-dB higher voltage gain than the second-order polyphase filter. The QAF can achieve more than 100% bandwidth with an I/Q phase error $<5^\circ$ and with $>$2.6 dB of voltage gain. Another difference between the polyphase filters and the QAF is that the QAF provides real input and output impedances over a wide bandwidth, while the input and output impedances of the polyphase filter are capacitive (Fig. 5) [16]. Typically input and output return losses of the QAF are $>$10 dB over more than 240% bandwidth.

C. Improvement of the QAF Under Loading Capacitance

A parasitic loading capacitance, C_L, will cause I/Q errors in the QAF and these errors are large at millimeter-wave frequencies since C_L can be comparable to the filter capacitance C. Decreasing C_L/C ratio by increasing C while C_L kept constant can relieve this problem [16]. However, at millimeter-wave frequency, this will drop the impedance of the QAF network too low; hence, making it hard for the preceding stage to drive the QAF.

The insertion of a series resistance R_s in the high-Q branches of C and L reduces the network Q and its sensitivity to the loading capacitance (Fig. 6). In this case, the I/Q transfer function of (3) is modified as (4), and R_s separates the negative real poles farther through decreasing Q by $(1+R_s/R)$. R_s does not disturb any zero location. Since the quadrature phase relation is set by the geometry of the zero positions, the I/Q phase characteristics of (4) are identical to those of (3)

$$\begin{bmatrix} V_{I\pm} \\ V_{Q\pm} \end{bmatrix} = V_{\text{in}} \times \begin{bmatrix} \pm\dfrac{s^2 + \dfrac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \dfrac{2\omega_o}{Q}\left(1+\dfrac{R_s}{R}\right)s + \omega_o^2} \\ \mp\dfrac{s^2 - \dfrac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \dfrac{2\omega_o}{Q}\left(1+\dfrac{R_s}{R}\right)s + \omega_o^2} \end{bmatrix}. \quad (4)$$

Fig. 7 presents the simulated QAF I/Q phase errors and magnitude mismatches with several values of R_s/R versus C_L/C at ω_o. The I/Q errors are suppressed with the increase of R_s and the QAF is insensitive to the parasitic capacitance when $R_s = R$ at ω_o. The penalty is loss, as shown in Fig. 8, and the maximum loss to desensitize C_L at ω_o is 6 dB when $R_s = R$ (Fig. 8 is done for $C_L/C = 0$). The added benefit of R_s is that it increases the QAF input impedance by $(1+R_s/R)$ and increases

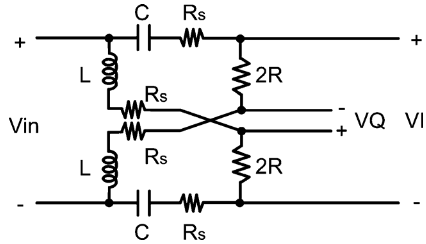

Fig. 6. Q reduction in the QAF using R_s to desensitize the loading capacitance.

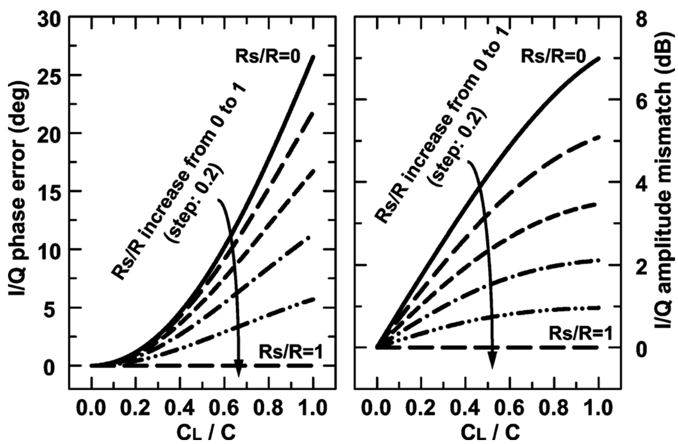

Fig. 7. I/Q errors (phase errors and amplitude mismatches) in the QAF under capacitive loading, C_L, with several values of R_s in Fig. 6.

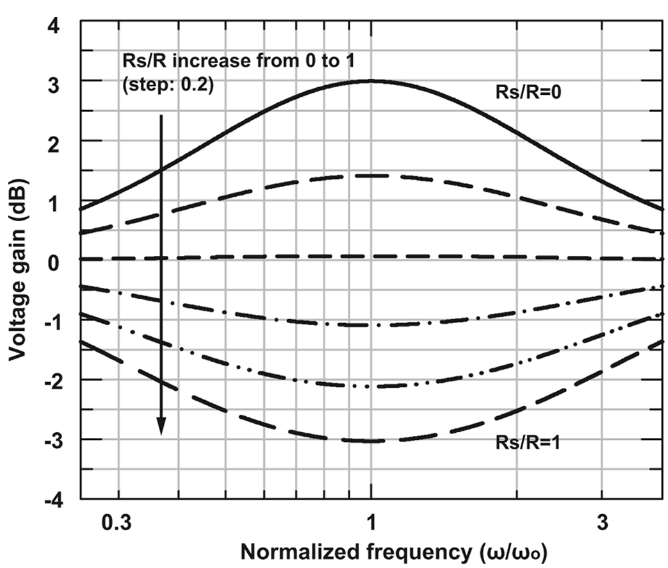

Fig. 8. Amplitude response of the improved QAF versus R_s.

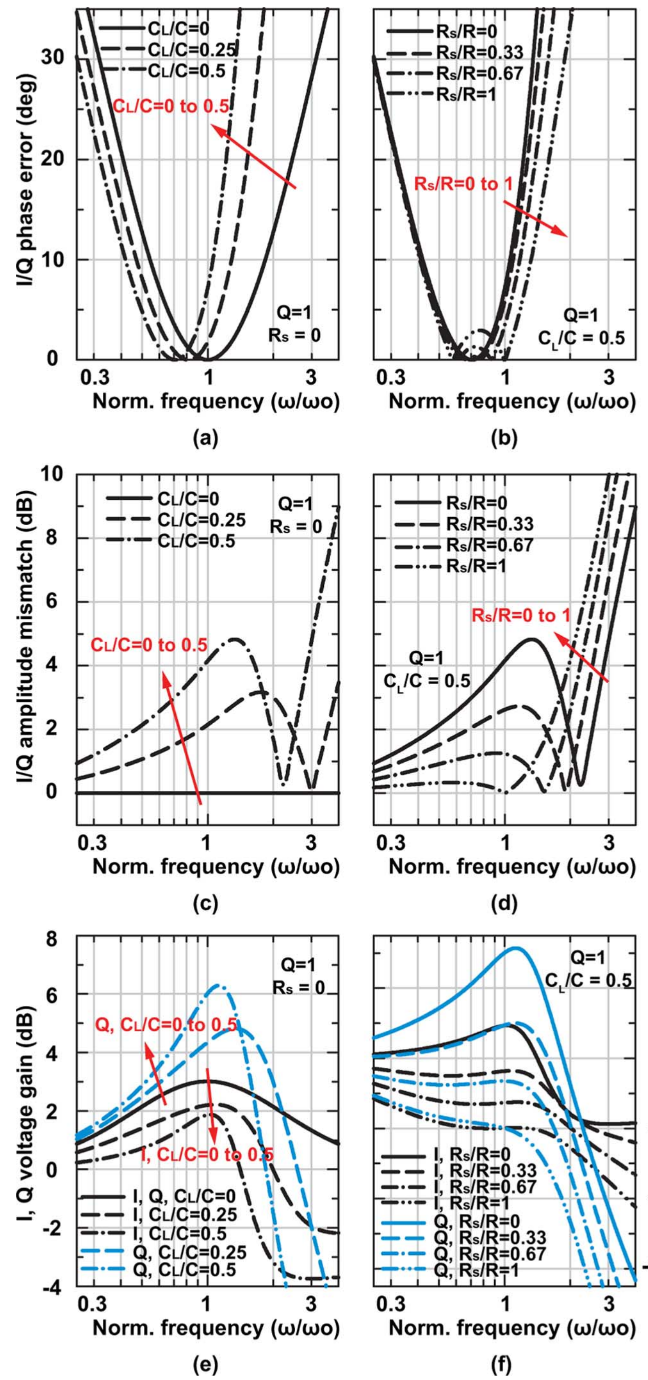

Fig. 9. (a) I/Q phase error when C_L/C increases ($R_s = 0$). (b) I/Q phase error when R_s/R increases ($C_L/C = 0.5$). (c) I/Q amplitude mismatch when C_L/C increases ($R_s = 0$). (d) I/Q amplitude mismatch when R_s/R increases ($C_L/C = 0.5$). (e) I and Q voltage gain when C_L/C increases ($R_s = 0$). (f) I and Q voltage gain when R_s/R increases ($C_L/C = 0.5$).

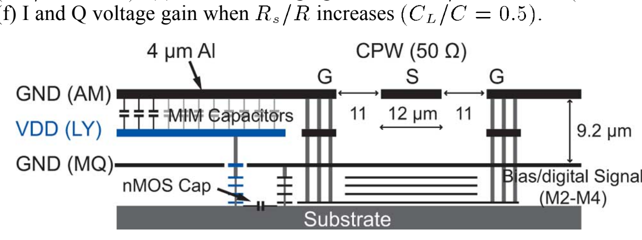

Fig. 10. IBM 8HP metal stack-up.

the load impedance on the previous amplifier stage (thus lowering its power).

An in-depth look at the frequency response of the QAF with a loading capacitance and the corresponding effect of R_s is shown in Fig. 9. The simulations are done for a QAF with a natural $Q = 1$, i.e., $C_L = 0$ and $Rs = 0$. It is seen that the phase mismatch between the I and Q outputs for $C_L = 0.5$ C is the same as $C_L = 0$, but with a shift in frequency due to the C_L loading [see Fig. 9(a)]. The addition of an R_s serves to reduce the Q factor of the network and widen the frequency response at the expense of loss, as shown in Fig. 9(b). In effect, the I/Q response can be re-centered for a specific C_L value and an R_s is not really

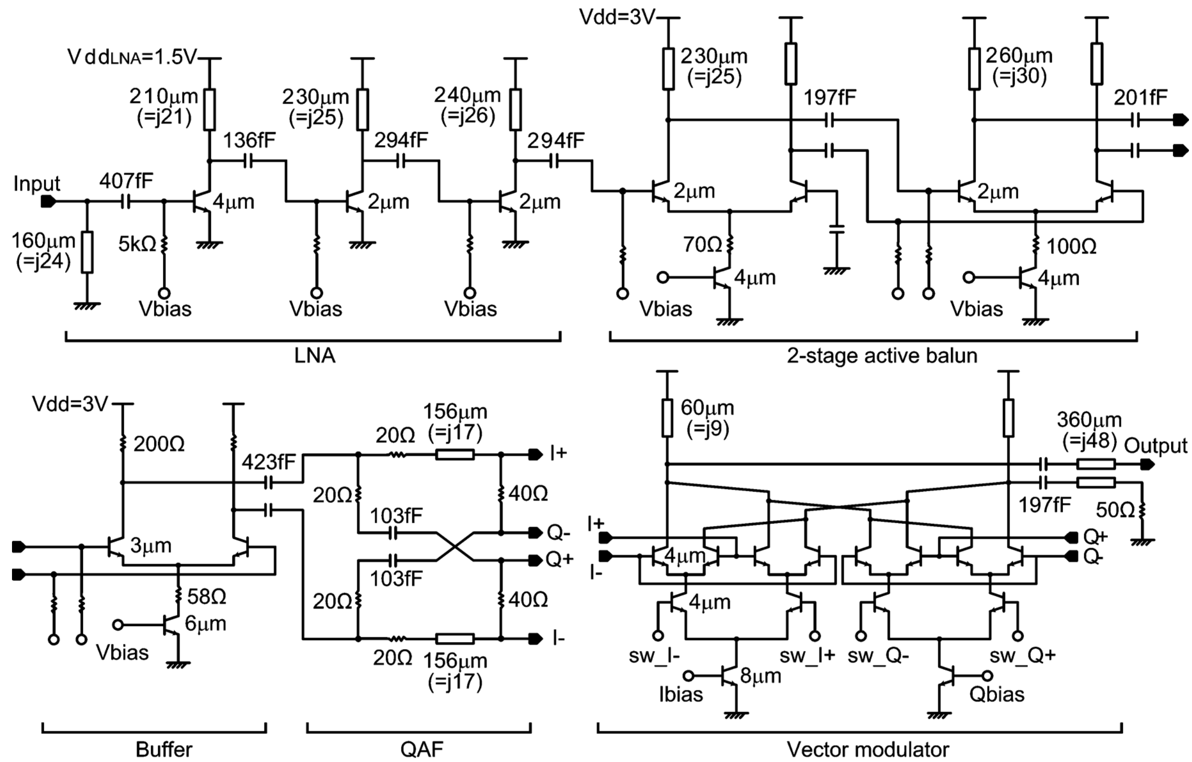

Fig. 11. Circuit schematics of the wideband millimeter-wave phase-shifter front-end.

needed. However, the amplitude mistmatch between the I and Q output is greatly affected by the C_L loading [see Fig. 9(c)] and the addition of $R_s/R = 0.67$ to the network improves the mismatch to <1.5 dB (from 4 to 5 dB) over a wide frequency range [see Fig. 9(d)], and allows the design of wideband 5-bit phase shifters. In reality, the choice of R_s depends on C_L/C and can be minimized with proper scaling of the QAF impedance together with optimizing the loading transistor size.

Finally, process, voltage, and temperature (PVT) simulations are done for the QAF with a loading capacitance of $C_L/C = 0.5$. Considering the process variations of $|\Delta R/R| \leq 10\%$, $|\Delta C/C| \leq 5\%$, and $|\Delta L/L| \leq 5\%$ and temperature range from -40° to 110°, the I/Q phase and amplitude error at the center frequency are less than 14.5° and 4.8 dB, respectively when $R_s = 0$. However, if $R_s/R = 1$, the phase error is less than 7.5° and the amplitude error is reduced to 0.2 dB at the center frequency.

IV. Wideband 60–80-GHz Phase-Shifter Design

The active phase shifter is designed using a 0.13-μm SiGe BiCMOS process (IBM 8HP). The IBM 8HP supports seven metal layers including two thick metal layers, AM ($= 4\ \mu$m) and LY ($= 1.25\ \mu$m), for low loss of the RF routing (Fig. 10). The SiGe npn transistors with a peak cutoff frequency (f_T) of 200 GHz, metal–insulator–metal (MIM) capacitors $(1\ \text{fF}/\mu\text{m}^2)$ and spiral inductors are provided in the design kit, but in this study, coplanar waveguide (CPW) transmission lines are used as the inductors using shorted stubs. The transition between the 50-Ω transmission line and the ground–signal–ground (G–S–G) pad is designed using an electromagnetic (EM) simulator (Sonnet [23]) to provide a 50-Ω impedance and <−25-dB reflection coefficient.

The active phase-shifter circuit is shown in Fig. 11. First, the single-ended RF input signal is amplified by a three-stage low-noise amplifier (LNA), and then converted to a differential signal using an active balun. Next, the differential quadrature signals are generated using a QAF loaded with Rs and the I/Q signals are sent to a vector modulator. One output of the vector modulator is terminated in 50 Ω for single-ended S-parameter measurements.

A common-emitter topology is adopted for the LNA to provide low-noise matching and 50-Ω input matching (Fig. 11). The first stage is biased at 1.0 mA/μm, which is the middle bias point between the lowest noise figure (NF) and the maximum power gain. The input matching is done using a single shunt inductor at the gate for the minimum chip area. The second and third stages are biased to maximize the gain. The LNA consumes 9.3 mA from a 1.5-V supply (14 mW) and achieves a simulated voltage gain of 19 dB at 70 GHz, and with $S_{11} < -10$ dB at 55.5–73.0 GHz. The simulated NF is 8 dB and the 1-dB compression point $(P_{1\text{dB}})$ is -19 dBm (when simulated with a 50-Ω output port).

The active balun is realized using a two-stage differential amplifier by grounding one of the differential inputs of the first stage. In order to provide additional common-mode rejection, resistors are placed at the drain of the current source transistors (Fig. 11). Simulations indicate that the output signal has an amplitude imbalance of 0.7 dB and the phase error of 2.2° at 70 GHz. The simulated balun voltage gain is 7.9 dB at 70 GHz for a current of 11.2 mA.

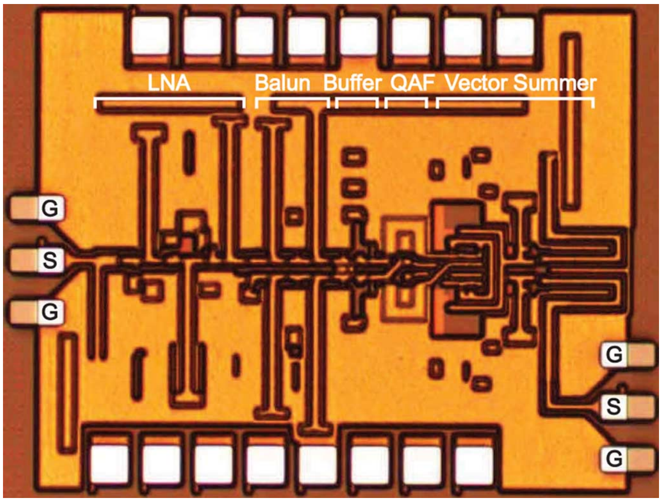

Fig. 12. Microphotograph of the wideband 60–80-GHz phase-shifter front-end (1.15×0.92 mm^2 including pads).

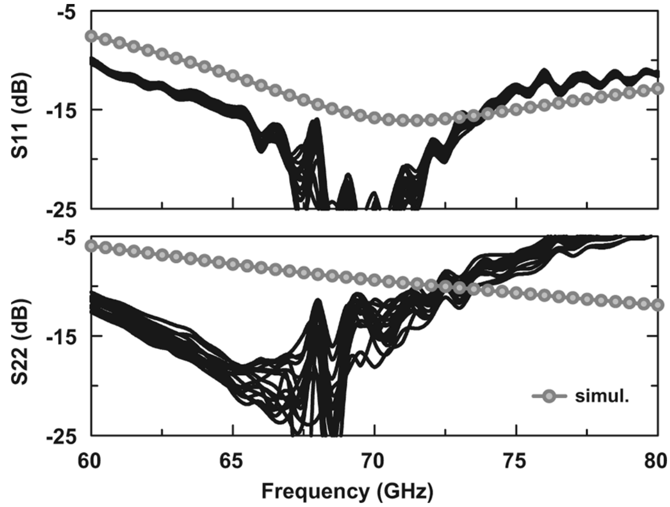

Fig. 13. Measured and simulated S_{11} and S_{22} for 16 phase states.

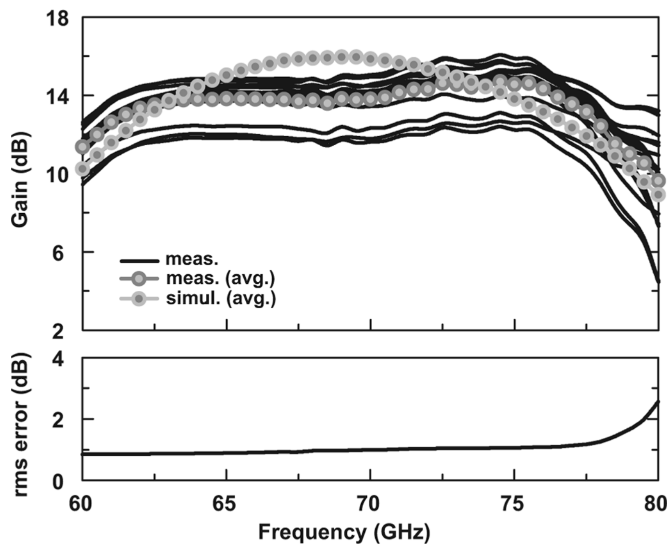

Fig. 14. Measured and simulated gain response for 16 phase states and rms gain error.

After a buffer stage with a simulated voltage gain of -1.3 dB at 70 GHz, the differential quadrature signals are generated by the improved QAF network (Fig. 11). From the desired center frequency (ω_o) and reasonable QAF impedance (R), the initial L and C values can be determined ($R = \sqrt{L/C}$ for $Q = 1$, $\omega_o = 1/\sqrt{LC}$). In this design, the estimated loading capacitance is $C_L = 50$–80 fF, which results in $C_L/C = 0.5$–0.8, which causes an I/Q phase error of 18° and an amplitude mismatch of 6 dB at the center frequency (see Fig. 7). After bandwidth extension by lowering Q [16] and EM simulation, the final optimized values of R, L, and C are $R = 20\ \Omega$, $L = 35.2$ pH, and $C = 103.4$ fF. By choosing $R_s = 20\ \Omega$ $(Rs/R = 1)$, I/Q errors are greatly minimized and the input impedance doubles to 40 Ω.

The vector modulator is composed of two Gilbert-cell type VGAs [16], [17] and the desired phase signal is synthesized by adding the current-domain I/Q signals with the proper gains at the output nodes (Fig. 11). The 180° phase shifting is done by switching the tail current (sw_$I+$/sw_$I-$ and sw_$Q+$/sw_$Q-$) and the variable gain function is done by changing the bias current of the I/Q branches (Ibias and Qbias). The vector modulator consumes 11.6 mA from a 3-V supply with a voltage gain including the QAF of -3.2 dB at 70 GHz.

V. Measurement Results

All measurements are done on-wafer using an Agilent E8361A vector network analyzer with extenders to 110 GHz. A standard short-open-load-thru (SOLT) calibration to the W-band GSG probe tips is first done using the Cascade 138–357 calibration substrate [24], and the measurements include the GSG pad transition loss. Several chips were measured and resulted in similar measurements.

Fig. 12 presents the chip microphotograph of the wideband active phase-shifter front-end. The overall chip size is 1.15×0.92 mm^2 including pads with a power consumption of 108 mW (LNA: 9.3 mA, 1.5 V, balun: 11.6 mA, 3.0 V, buffer: 8.6 mA, 3.0 V, vector modulator: 11.6 mA, 3.0 V). The power consumption is relatively high due to the wideband design of 60–80 GHz. Also, since this was a demonstration circuit for the improved QAF, low-power techniques, such as interstage transformer neutralization, were not used.

Fig. 13 presents the measured input and output matching characteristics for 16 phase states. It is seen that S_{11} is <-10 dB at 60–80 GHz, and S_{22} is <-10 dB at 60–73 GHz. The measured S_{22} does not agree well with simulations and this could be partly due to slight imbalances in the differential output port (one is internally loaded with 50 Ω and the other is connected to the GSG pad) and partly due to the inaccurate capacitance EM simulation. The measured average power gain (S_{21}) is 11.0–14.7 dB at 60–79 GHz and agrees well with simulations. The peak-to-peak gain variation is $\leq \pm$ 2.3 dB, and the root mean square (rms) gain variation is $<$1.3 dB at 60–78 GHz for the 4-bit phase states (Fig. 14). Fig. 15 presents the measured 4-bit phase responses from 60 to 80 GHz. The phase shifter results in an rms phase error of $< 9.1°$ at 60–78.5 GHz, and $< 5.6°$ at 70–77.5 GHz, showing wideband 4-bit performance.

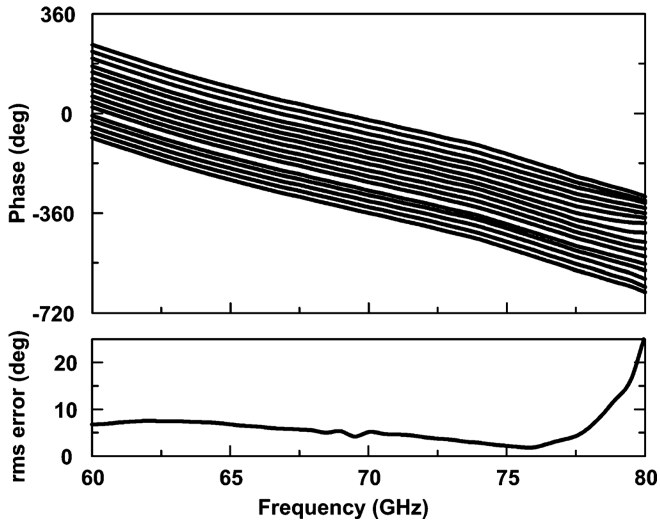

Fig. 15. Measured phase response and rms phase error.

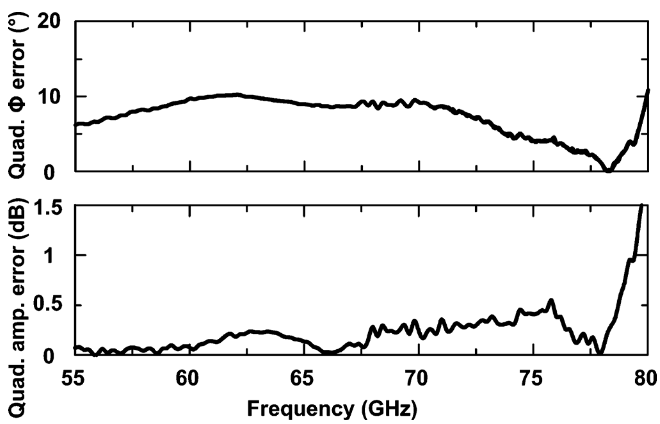

Fig. 16. Measured quadrature phase error and amplitude error.

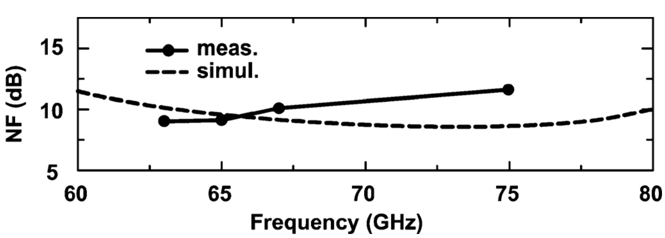

Fig. 17. Measured and simulated NF.

An accurate method to measure the QAF performance is to compare the measured 0° and 90° responses of the active phase shifter [16]. Fig. 16 shows that the I/Q phase and amplitude error of the improved QAF is $< 9.5°$ and <0.5 dB for 55–78.5 GHz, respectively, which is a proof that the improved QAF does generate accurate I/Q signals under high capacitive loading. Both follow the response predicted in Fig. 9.

The measured NF ranges is 9–11.6 dB at 63–75 GHz and agrees well with simulations (Fig. 17). The NF is nearly independent of the phase states because the LNA/active-balun gain is high enough to ignore the NF variation in the vector modulator. The measured 1-dB gain compression point ($P_{1\mathrm{dB}}$) is -27 dBm at 70 GHz (not shown).

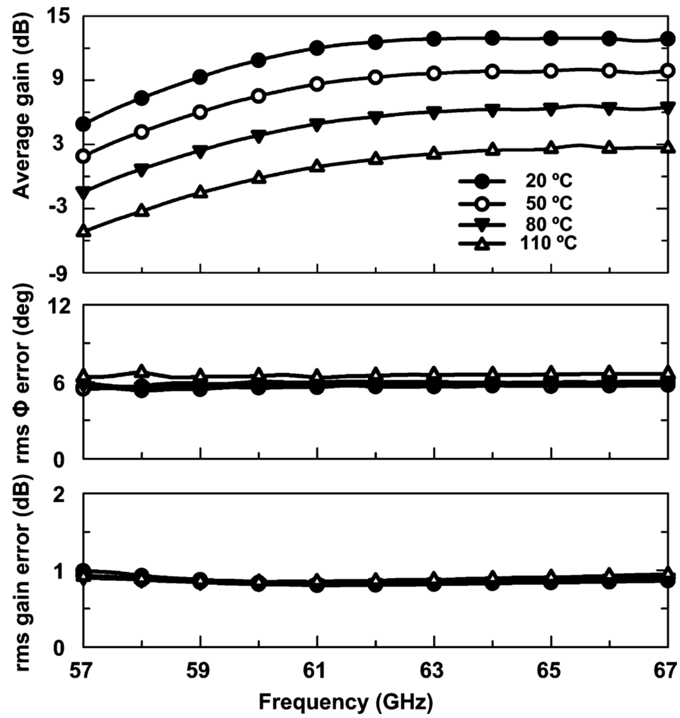

Fig. 18. Measured gain and rms errors at different temperatures.

Fig. 18 presents the measured gain and rms errors at different temperatures up to 67 GHz (limited by the test setup). The gain drops by ~ 10 dB from 20° to 110°. In the future, this gain drop can be compensated using proportional-to-absolute-temperature (PTAT) biasing circuits, as shown in [8]. On the other hand, the rms phase and gain errors remains the same, showing that the vector modulator amplifiers track each other over a wide temperature range.

VI. Conclusions

This paper has presented an improved QAF and its implementation in a 60–80-GHz active phase shifter using 0.13-μm SiGe BiCMOS technology. It has been demonstrated that with the inclusion of an $Rs/R = 0.5$-1 in the QAF, the capacitive loading problem is mitigated and the I/Q phase and amplitude errors are minimized. This technique is especially suited for wideband millimeter-wave circuits, which naturally result in high C_L/C values and cannot be tuned using narrowband techniques. A prototype wideband receiver resulted in state-of-the-art I/Q amplitude and phase balance at 55–78 GHz even with a C_L/C loading of 0.5–0.8.

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References

[1] T. M. Hancock and G. M. Rebeiz, “A 12-GHz SiGe phase shifter with integrated LNA,” *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 3, pp. 977–983, Mar. 2005.

[2] F. Ellinger, H. Jackel, and W. Bachtold, "Varactor-loaded transmission-line phase shifter at C-band using lumped elements," *IEEE Trans. Microwave Theory Techn.*, vol. 51, no. 4, pp. 1135–1140, Apr. 2003.

[3] D.-W. Kang and S. Hong, "A 4-bit CMOS phase shifter using distributed active switches," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 7, pp. 1476–1483, Jul. 2007.

[4] D.-W. Kang, J.-G. Kim, B.-W. Min, and G. M. Rebeiz, "Single and four-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3534–3543, Dec. 2009.

[5] C. F. Campbell and S. A. Brown, "A compact 5-bit phase-shifter MMIC for K-band satellite communication systems," *IEEE Trans. Microw. Theory Techn.*, vol. 48, no. 12, pp. 2652–2656, Dec. 2000.

[6] Y. Ayasli, S. W. Miller, R. Mozzi, and L. K. Hanes, "Wide-band monolithic phase shifter," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-32, no. 12, pp. 1710–1714, Dec. 1984.

[7] C.-Y. Kim, D.-W. Kang, and G. M. Rebeiz, "A 44–46-GHz 16-element SiGe BiCMOS high-linearity transmit/receive phased array," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 730–742, Mar. 2012.

[8] S. Kim and G. M. Rebeiz, "A low-power BiCMOS 4-element phased array receiver for 76–84 GHz radars and communication systems," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 359–367, Feb. 2012.

[9] S. Kim, O. Inac, C.-Y. Kim, and G. M. Rebeiz, "A 76–84 GHz 16-element phased array receiver with a chip-level built-in-self-test system," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2012, pp. 127–130.

[10] J.-L. Kuo, Y.-F. Lu, T.-Y. Huang, Y.-L. Chang, Y.-K. Hsieh, P.-J. Peng, I.-C. Chang, T.-C. Tsai, K.-Y. Kao, W.-Y. Hsiung, J. Wang, Y. A. Hsu, K.-Y. Lin, H.-C. Lu, Y.-C. Lin, L.-H. Lu, T.-W. Huang, R.-B. Wu, and H. Wang, "60-GHz four-element phased-array transmit/receive system-in-package using phase compensation techniques in 65-nm flip-chip CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 743–756, Mar. 2012.

[11] M. Chua and K. W. Martin, "1 GHz programmable analog phase shifter for adaptive antennas," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 1998, pp. 71–74.

[12] Y. Yu, P. G. M. Baltus, A. Graauw, E. Heijden, C. S. Vaucher, and A. H. M. Roermund, "A 60 GHz phase shifter integrated with LNA and PA in 65 nm CMOS for phased array systems," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1697–1709, Sep. 2010.

[13] M. Elkhouly, S. Glisic, F. Ellinger, and J. C. Schyett, "A 60 GHz four channel beamforming transmitter in 0.25 μm SiGe BiCMOS technology," in *IEEE Eur. Microw. Integr. Circuits Conf.*, Oct. 2011, pp. 25–28.

[14] M. Elkhouly, C.-S. Choi, S. Glisic, C. Scheytt, and F. Ellinger, "Millimeter-wave beamforming circuits in SiGe BiCMOS," in *IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Oct. 2010, pp. 129–132.

[15] I. Sarkas, M. Khanpour, A. Tomkins, P. Chevalier, P. Garcia, and S. P. Voinigescu, "W-band 65-nm CMOS and SiGe BiCMOS transmitter and receiver with lumped I-Q phase shifters," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 441–444.

[16] K.-J. Koh and G. M. Rebeiz, "0.13-μm CMOS phase shifters for X-, Ku-, and K-band phased arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535–2546, Nov. 2007.

[17] K.-J. Koh and G. M. Rebeiz, "An X- and Ku-band 8-element phased-array receiver in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1360–1371, Jun. 2008.

[18] K.-J. Koh, J. W. May, and G. M. Rebeiz, "A millimeter-wave (40–45 GHz) 16-element phased-array transmitter in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1498–1509, May 2009.

[19] D.-W. Kang, K.-J. Koh, and G. M. Rebeiz, "A Ku-band two-antenna four-simultaneous beams SiGe BiCMOS phased array receiver," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 4, pp. 771–780, Apr. 2010.

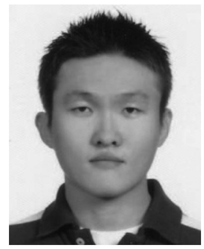
[20] M. A. F. Borremans, C. R. C. De Ranter, and M. S. J. Steyaert, "A CMOS dual-channel, 100-MHz to 1.1-GHz transmitter for cable applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1904–1913, Dec. 1999.

[21] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, Jun. 2001.

[22] K.-J. Koh, M.-Y. Park, C.-S. Kim, and H.-K. Yu, "Subharmonically pumped CMOS frequency conversion (up and down) circuits for 2-GHz WCDMA direct-conversion transceiver," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 871–884, Jun. 2004.

[23] Sonnet. ver. 11.52, Sonnet Softw. Inc., North Syracuse, NY.

[24] "Cascade impedance standard substrate," Cascade Microtech, Beaverton, OR, P/N: 138–357. [Online]. Available: http://www.cmicro.com



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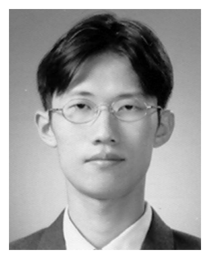

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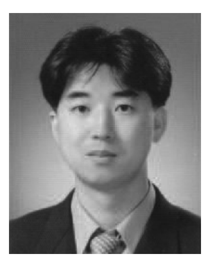

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