A 15-38 GHz Vector-Summing Phase-Shifter With 360° Phase-Shifting Range Using Improved I/Q Generator

Feng Qiu, *Graduate Student Member, IEEE*, Haoshen Zhu, *Member, IEEE*, Liang Wu, *Member, IEEE*, Wenquan Che, *Senior Member, IEEE*, and Quan Xue, *Fellow, IEEE*

***Abstract*—This brief presents a 15-38 GHz vector-summing phase shifter (VSPS) with the full 360° phase-shifting range in the 65nm CMOS process. An improved wideband quadrature all-pass filter (QAF) is designed to overcome the traditional one's capacitive loading effect and exhibits wideband I/Q performance. Analysis and comparison between the proposed QAF and the traditional one are discussed. For demonstration, a prototype VSPS with the full 360° phase-shifting range from 15GHz to 38GHz using the proposed QAF is implemented in the 65nm CMOS process. The root means square (RMS) phase and gain errors are 2° ∼ 3.5° and 0.7 dB ∼ 1 dB from 15 GHz to 38 GHz, respectively. The power consumption is 19.2mW, and the whole chip is compact with a core size of 0.16mm^2.**

***Index Terms*—Phase shifter, I/Q generator, vector-sum, capacitive loading effect.**

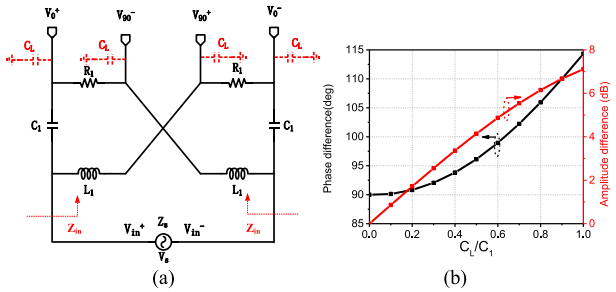


Fig. 1. (a) The schematic of the traditional QAF; (b) The Magnitude and Phase difference between ($V_0{}^+ - V_0{}^-$) and ($V_{90}{}^+ - V_{90}{}^-$) versus C_L/C_1 for the traditional QAF.

I. Introduction

PHASE shifter is a critical component in the phased array communication system for beam steering. It includes passive [1]–[5] and active types. Active phase shifters, typically based on vector-summing technique [6]–[15], feature with high gain, high phase resolution, and medium-size (typically between reflection-type and switch-type in the passive phase shifter). It consists of the I/Q generator, digital control circuit, and vector summer.

The I/Q generator is the most crucial building block in the VSPS to generate quadrature vectors. It normally adopts the quadrature all-pass filter (QAF) [6], [8], [14], or RC polyphase filter (RCPPF) [11]. The RCPPF shows good quadrature phase difference, balanced amplitude, and compact chip size but suffers from high insertion loss and narrow bandwidth in the millimeter-wave application. The bandwidth of RCPPF can be expanded by employing a multi-stage structure but leading to higher insertion loss. The QAF exhibits low phase error and balanced amplitude with less insertion loss in theory, but its loading effect strongly affects the performance, especially in wideband applications. In [6], a novel QAF with additional two resistors is introduced to overcome the loading effect. However, the insertion loss is a little high, which needs additional amplifier buffers to compensate for it.

This brief presents an improved wideband QAF as the I/Q generator, which adds a pair of serial inductors and resistors to the traditional one. The proposed QAF overcomes the capacitive loading effects while exhibiting wideband performance. For demonstration, a 6-bit VSPS with the full 360° phase-shifting range employing the proposed QAF, vector summer, and digital control circuit is implemented in the 65 nm CMOS process, performing 2.23° ∼ 3.5° RMS phase errors and 0.7 ∼ 1 dB RMS gain error across a wideband from 15 ∼ 38GHz.

Manuscript received February 11, 2021; revised March 31, 2021; accepted April 13, 2021. Date of publication April 20, 2021; date of current version September 24, 2021. This work was supported in part by the National Key Research and Development Program of China under Grant 2018YFB1802000; in part by the Guangdong Important Fields Research Program under Grant 2018B010115001; and in part by the Guangdong Innovative and Entrepreneurial Research Team Program under Grant 2017ZT07X032. This brief was recommended by Associate Editor G. Torfs. *(Corresponding author: Quan Xue.)*

Feng Qiu, Haoshen Zhu, Wenquan Che, and Quan Xue are with the Guangdong Provincial Key Laboratory of Millimeter-Wave and Terahertz, School of Electronic and Information Engineering, South China University of Technology, Guangzhou 510641, China (e-mail: qiufeng0919@126.com; zhuhs@scut.edu.cn; eewqche@scut.edu.cn; eeqxue@scut.edu.cn).

Liang Wu is with the School of Science and Engineering, the Chinese University of Hong Kong, Shenzhen 518172, China (e-mail: wuliang@cuhk.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2021.3074166.

Digital Object Identifier 10.1109/TCSII.2021.3074166

II. The Improved Quadrature All-Pass Filter

The schematic of the traditional QAF is shown in Fig. 1(a). It consists of two capacitors C_1, two inductors $L_1$and two resistors R_1. The QAF transforms the input differential signal ($V_{in}{}^+$, $V_{in}{}^-$) into two quadrature differential signals ($V_0{}^+$, $V_0{}^-$) and ($V_{90}{}^+$, $V_{90}{}^-$), which are expressed as (1) to (4) under

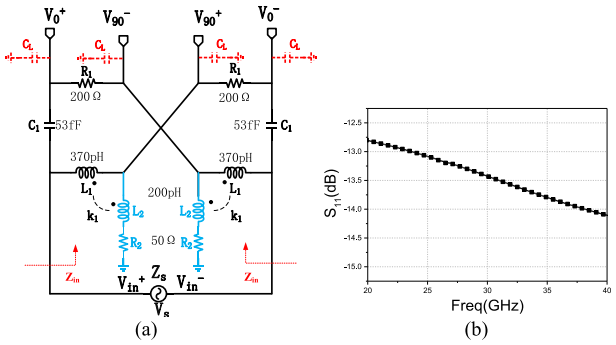


Fig. 2. (a) Schematic of the proposed QAF; (b) The EM simulated S_{11}.

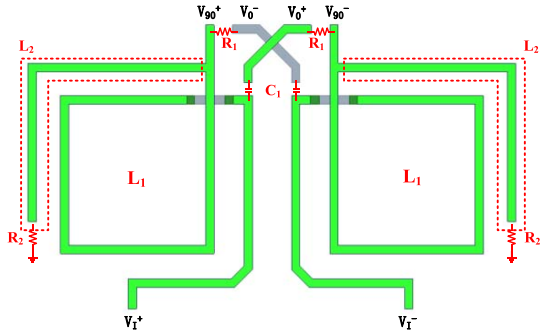


Fig. 3. The layout of the proposed QAF.

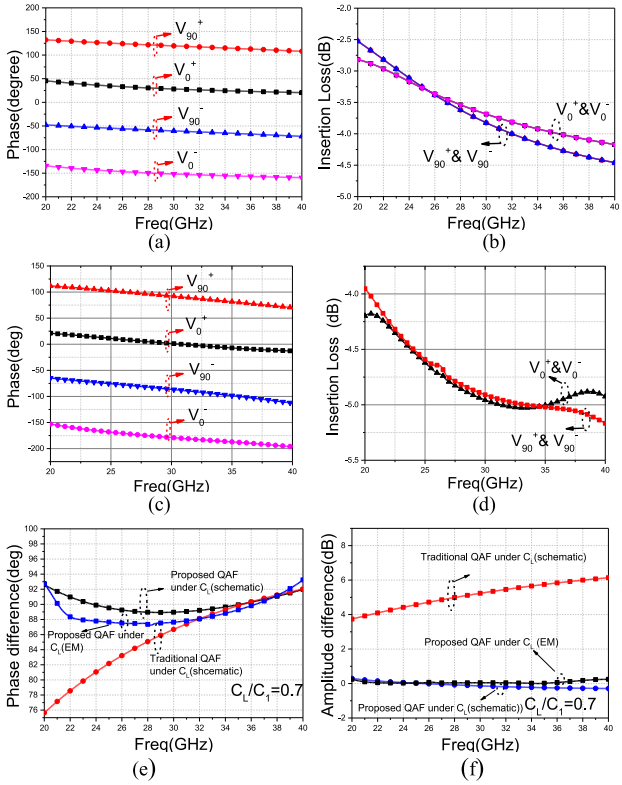


Fig. 4. Phase and Magnitude results of the proposed QAF from 20GHz to 40GHz when $C_L/C_1 = 0.7$. (a) The simulated schematic phase results of the proposed QAF. (b) The simulated schematic insertion loss of the proposed QAF. (c) The simulated EM phase results of the proposed QAF. (d) The simulated EM insertion loss of the proposed QAF. (e) The phase differences of $(V_0^+ - V_0^-)$ and $(V_{90}^+ - V_{90}^-)$ in the proposed and traditional QAFs. (f) The magnitude difference of $(V_0^+ - V_0^-)$ and $(V_{90}^+ - V_{90}^-)$ in the proposed and traditional QAFs; (C_1 = 53fF, L_1 = 530pH, R_1 = 200 Ω for the traditional QAF in 30 GHz).

ideal open loads.

$$V_0^+ = \frac{(R_1 + j\omega L_1)*V_{in}^+ + 1/(j\omega C_1)*V_{in}^-}{R_1 + j\omega L_1 + 1/(j\omega C_1)} = \frac{R_1 + j\omega L_1 - 1/(j\omega C_1)}{R_1 + j\omega L_1 + 1/(j\omega C_1)} * V_{in}^+ \quad (1)$$

$$V_{90}^- = \frac{(j\omega L_1)*V_{in}^+ + [R_1 + 1/(j\omega C_1)]*V_{in}^-}{R_1 + j\omega L_1 + 1/(j\omega C_1)} = \frac{-R_1 + j\omega L_1 - 1/(j\omega C_1)}{R_1 + j\omega L_1 + 1/(j\omega C_1)} * V_{in}^+ \quad (2)$$

$$V_{90}^+ = \frac{[R_1 + 1/(j\omega C_1)]*V_{in}^+ + (j\omega L_1)*V_{in}^-}{R_1 + j\omega L_1 + 1/(j\omega C_1)} = \frac{R_1 - j\omega L_1 + 1/(j\omega C_1)}{R_1 + j\omega L_1 + 1/(j\omega C_1)} * V_{in}^+ \quad (3)$$

$$V_0^- = \frac{1/(j\omega C_1)*V_{in}^+ + (R_1 + j\omega L_1)*V_{in}^-}{R_1 + j\omega L_1 + 1/(j\omega C_1)} = \frac{-R_1 - j\omega L_1 + 1/(j\omega C_1)}{R_1 + j\omega L_1 + 1/(j\omega C_1)} * V_{in}^+ \quad (4)$$

where $V_{in}^+ = -V_{in}^-$. The detailed derivation of the traditional QAF can be founded in [8]. The ideal QAF performs balanced magnitude and quadrature-phase differences at the resonating frequency of $\omega_0 = 1/\sqrt{L_1 C_1}$, when $R_1 = 2\sqrt{L_1/C_1}$.

However, the outputs of QAF are always connecting to the gate terminals of MOSFETs in VSPS design, which leads to small capacitive loads C_L. The influences of C_L on the amplitude and phase performances for the traditional QAF are depicted in Fig. 1 (b). It can be observed that the capacitive loading effect is negligible when $C_L << C_1$, But as C_L gets larger, it deteriorates the phase and amplitude balance. Particularly, when $C_L/C_1 > 0.7$, the phase and amplitude errors are larger than 12.5 degrees and 5.5dB, respectively.

To weaken this loading effect, a large capacitance of C_1 is needed to be assigned, which leads to a small resistance of R_1 in the millimeter-wave band as $R_1 = 2\sqrt{L_1/C_1}$ and $\omega_0 = 1/\sqrt{L_1 C_1}$. However, the resistance R_1 is related to the input impedance matching. The input impedance of the QAF Z_{in} at the operating frequency of $\omega_0 = 1/\sqrt{L_1 C_1}$ is expressed as:

$$Z_{in} = (R_1 + j\omega L_1 + 1/j\omega C_1)/2 = \frac{R_1}{2} \text{ at } \omega = \omega_0 \quad (5)$$

In [8], the resistor R_1 is set to be 96.4Ω for 50Ω differential input impedance matching. In the proposed design, the resistance of R_1 is set to be 200Ω for 100Ω differential input impedance matching. A small resistance of R_1 will deteriorate the input matching performance and decrease the input voltages of $(V_I^+ - V_I^-)$ when considering source impedance Z_s, as shown in equation (6).

$$V_{in}^+ - V_{in}^- = V_s * \frac{R_1/2}{Z_s + R_1/2} \text{ at } \omega = \omega_0 \quad (6)$$

$$V_0^+ = -V_0^- = \frac{[j\omega L_1 // \frac{1}{j\omega C_L} // (j\omega L_2 + R_2) + R_1] // \frac{1}{j\omega C_L}}{[j\omega L_1 // \frac{1}{j\omega C_L} // (j\omega L_2 + R_2) + R_1] // \frac{1}{j\omega C_L} + \frac{1}{j\omega C_1}} * V_{in}^+ + \frac{\frac{1}{j\omega(C_1+C_L)}}{[\frac{1}{j\omega(C_1+C_L)} + R_1] // \frac{1}{j\omega C_L} // (j\omega L_2 + R_2) + j\omega L_1} * V_{in}^- \quad (7)$$

$$V_{90}^- = -V_{90}^+ = \frac{j\omega L_1 // \frac{1}{j\omega C_L} // (j\omega L_2 + R_2)}{[j\omega L_1 // \frac{1}{j\omega C_L} // (j\omega L_2 + R_2) + R_1] // \frac{1}{j\omega C_L} + \frac{1}{j\omega C_1}} * V_{in}^+ + \frac{[\frac{1}{j\omega(C_1+C_L)} + R_1] // \frac{1}{j\omega C_L} // (j\omega L_2 + R_2)}{[\frac{1}{j\omega(C_1+C_L)} + R_1] // \frac{1}{j\omega C_L} // (j\omega L_2 + R_2) + j\omega L_1} * V_{in}^- \quad (8)$$

TABLE I
LOGIC MAPPING TABLE FOR THE DIGITAL CIRCUIT

$B_4B_3B_2B_1B_0$	VG_1	VG_2	Target Phase(deg)	$B_4B_3B_2B_1B_0$	VG_1	VG_2	Target Phase(deg)	B_5B_6	K_1	K_2	K_3	K_4	Section
00000	0.6V	0V	0	10000	0V	0.6V	90	00	1	0	1	0	I
00001	0.6V	0.255V	5.625	10001	0.255V	0.6V	84.375	01	1	0	0	1	III
00010	0.6V	0.297V	11.25	10010	0.297V	0.6V	78.75	10	0	1	1	0	II
00011	0.6V	0.325V	16.875	10011	0.325V	0.6V	73.125	11	0	1	0	1	IV
00100	0.6V	0.35V	22.5	10100	0.35V	0.6V	67.5						
00101	0.6V	0.367V	28.125	10101	0.367V	0.6V	61.875						
00110	0.6V	0.390V	33.75	10110	0.390V	0.6V	56.25						
00111	0.6V	0.422V	39.375	10111	0.422V	0.6V	50.625						
01XXX	0.6V	0.6V	45	11XXX	0.6V	0.6V	45						

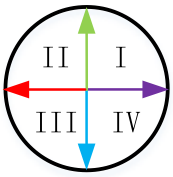
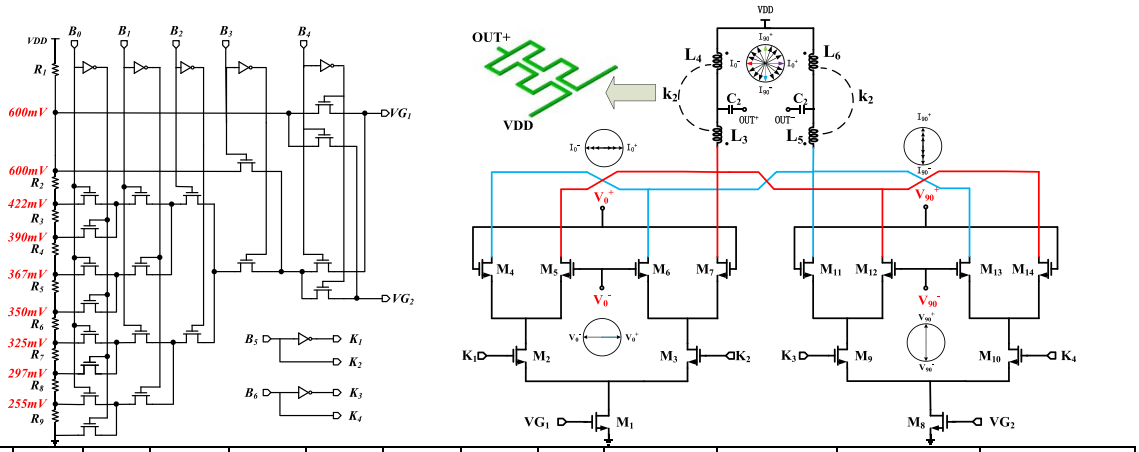


TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Ref	Technology	Freq (GHz)	Phase Resolution	RMS Phase error(deg)	Gain (dB)	RMS Gain error(dB)	Power Consumption(mW)	Chip Size(mm^2)
TMTT 2012[6]	0.13um BiCMOS	60-80	22.5°	9.1°	-	1.3	34.8	-
TMTT 2013 [10]	0.18um BiCMOS	15-35	22.5°	4.2°-13°	-13.5-5	1-2.2	25.2	0.19*
TMTT 2016[7]	90nm CMOS	57-64	22.5°	2.3°-7.6°	1.1	0.75-1.6	19.8	0.61
JSSC 2017 [9]	28nm FDSOI CMOS	80-96	22.5°	<11.9°	2.3	<2	21.6	0.12*
MWCL2018[13]	40nm CMOS	52-57	5.625°	2.8°-3.76°	-19~-9	2.07-2.23	14.3	0.15*
ISSC 2019 [14]	65nm bulk CMOS	25-30	5.625°	<1.5°	-	<0.25dB	-	-
ACCESS2020[15]	0.18um CMOS	13.4-15.5	5.625°	<2.3°	3.8**	<1	29.7	1.305
This work	**65nm CMOS**	**15-38**	**5.625°**	**2°-3.5°**	**-4.7~ -1.7**	**0.7-1**	**19.2**	**0.16***

* without PADs ** peak gain



Resistors	R_1	R_2	R_3	R_4/R_6	R_5	R_7	R_8	R_9	Transistors	M_1/M_8	$M_2/M_3/M_9/M_{10}$	M_4-M_7/M_{11}-M_{14}
Value(Ω)	10.9k	2.6k	0.63k	0.45k	0.36k	0.54k	0.82k	5k	W/L	64um/60nm	40um/60nm	32um/60nm

(a) (b)

Fig. 5. The schematic of the proposed vector summer and digital control circuit. (a) The digital control circuit; (b) The Gillerbert circuit for vector summing.

It should be noted that the loading effect in the traditional QAF is challenging to be removed by optimizing the parameters of lumped elements, especially for wideband.

To overcome the capacitive loading effect and obtain wideband performance, the improved QAF is proposed, as shown in Fig. 2 (a). A pair of serial inductors L_2 and resistors R_2 are added to the traditional QAF design. The inductors L_2 are added parallel to C_L to realize a parallel resonance. As the parallel resonance is narrowband responses, additional resistors R_2 are added to decrease the Q factor to enhance the wideband performance. Fig. 2(b) shows the EM simulated S_{11} of the proposed QAF, which performs 12.7dB input return loss across 20 to 40GHz. The

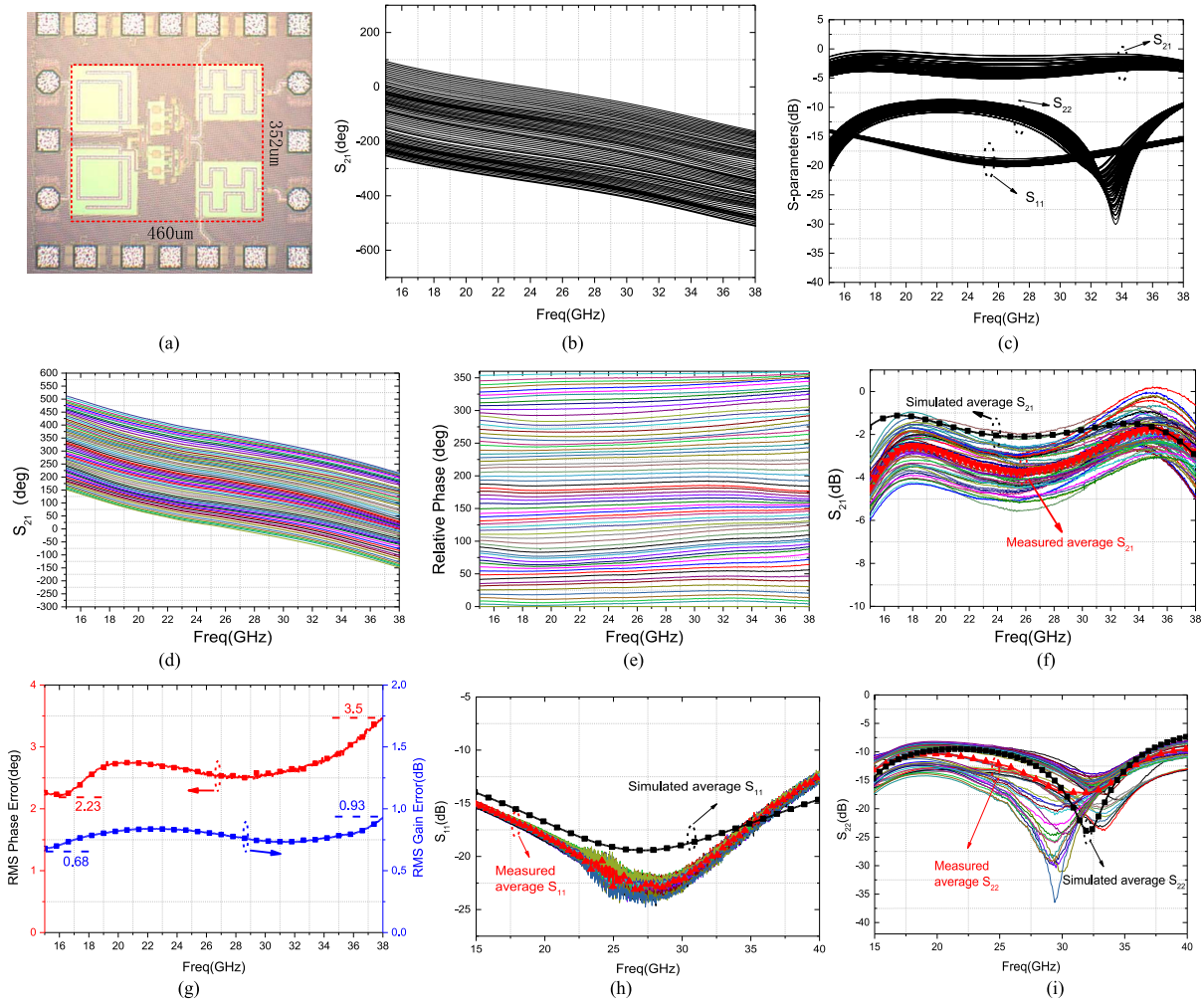


Fig. 6. The results of the proposed phase shifter; (a) The micrograph of the proposed phase shifter. (b) The simulated 64 insertion phase states; (c) The simulated S-parameters. (d) The measured 64 insertion phase states; (e) The 64 relative phase states; (f) The measured S_{21} for 64 phase states and the simulated average S_{21}; (g) The results of RMS phase error and gain error. (h) The measured S_{11} for 64 phase states and the simulated average S_{11}; (i) The measured S_{22} for 64 phase states and the simulated average S_{22}.

wideband input impedance matching is due to the resistors added in the QAF. The resistors reduce the quality factor of the input matching network, which enhances the input matching bandwidth.

Fig. 3 shows the layout of the proposed QAF with lumped elements. It should be noted that the inductors L_1 and L_2 are designed to be folded for saving chip size. The coupling between inductors L_1 and L_2 is weak and considered in the EM simulation.

The output voltages of the proposed QAF under loading capacitors C_L are expressed at the bottom of the p. 2. As the equations in (7) and (8) are too complicated and the equation analysis for canceling the loading effect is hard to be observed. So, this brief shows the comparison of simulation results between the proposed QAF and traditional QAF under the loading capacitor C_L. Fig. 4 (a) to (d) show the schematic and EM simulation results of the proposed QAF working at the central frequency of 30GHz under 30 fF capacitive loading effect ($C_L/C_1 = 0.7$), respectively. The schematic simulation results, as shown in Fig. 4 (a) and (b), exhibit $89° \sim 92°$ phase differences and $-0.28 \sim 0.29$ dB magnitude differences between $(V_0^+ - V_0^-)$ and $(V_{90}^+ - V_{90}^-)$ for a wideband from 20 GHz to 40 GHz, respectively. The insertion loss is acceptable from 2.5$\sim$ 4.5dB. The I/Q performance in EM simulation results degrades slightly, as shown in Fig. 4 (c) and (d). Fig. 4 (e) and (f) compare the simulated results between the proposed QAF and the traditional one under the same loading effect ($C_L/C_1 = 0.7$). The proposed one exhibits the better performance of quadrature-phase difference and balanced amplitude across a wideband from 20GHz to 40GHz.

III. The Proposed Vector Summer With Digital Control Circuit

The vector summer and digital controller are the other critical blocks in VSPS design. Fig. 5 shows the schematics of the vector summer and digital controller in the proposed VSPS.

An analog differential vector summer, as shown in Fig. 5(b), is designed to be a Gillebert circuit. Transistors M_4 to M_7 and M_{11} to M_{14} in the circuit transform the output differential

voltage signals (V_0^+, V_0^-) and (V_{90}^+, V_{90}^-) from QAF to currents signals as (I_0^+, I_0^-) and (I_{90}^+, I_{90}^-). The magnitude of currents vectors are adjusted by the voltage VG_1 and VG_2 on the gate terminals of transistors M_1 and M_8. Transistors M_2, M_3, M_9, and M_{10} are designed to switch, which select current vectors from I_0^+, I_0^- I_{90}^+, and I_{90}^- for vector summing by controlling the voltage of K_1 to K_4. Inductors L_3 to L_6 and capacitors C_2 are designed for output matching. The inductor pairs of (L_3, L_4) and (L_5, L_6) are designed to construct the multi-resonance transformers to expand the bandwidth while still keep a compact size, as shown in Fig. 5(b). The voltages of VG_1, VG_2, and K_1 to K_4 in the vector summer are controlled by the digital control circuits, as shown in Fig. 5(a). The bit of B_0 to B_4 controls the voltage pair of (VG_1, VG_2), and bit B_5 and B_6 control the phase sections in the rectangular coordinate system. The logic mapping table for the digital circuit is shown in Table I.

IV. Measured Results of the Proposed Phase Shifter

Based on the QAF mentioned above, vector summer, and digital control circuit, a 15-38 GHz VSPS with a full 360° phase shift range is implemented in the 65nm CMOS process. The fabricated die micrograph of the proposed VSPS is shown in Fig. 6 (a) with a compact size of 0.16mm^2 for the core area. It consumes 16mA current at most from a 1.2V voltage supply.

Fig. 6 (b) and (c) show the simulation results of the whole VSPS. Fig. 6 (d) and (e) depict the 64 measured insertion phase states and relative phase states, respectively. Fig. 6(f) shows the measured voltage gain for the 64 phase states and their average voltage gain. The 3dB bandwidth of the average voltage gain ranges from 15GHz to 38GHz. The RMS errors of phase and gain are presented in Fig. 6(g), which exhibits 2.23-3.5° RMS phase error and 0.7-1 dB RMS gain error from 15 GHz to 38 GHz, respectively.

Fig. 7(h) and (i) illustrate the measured return loss of input and output in the proposed VSPS, which is higher than 12dB for input return loss and 8dB for the output return loss from 15 GHz to 38 GHz, respectively.

Table II summary the performance of the proposed design and compares it with state-of-art. The proposed VSPS exhibits wideband, high phase resolution.

V. Conclusion

This brief reports a wideband vector-sum phase shifter in the 65nm CMOS process. An improved QAF is designed to overcome the loading effect and obtain wideband performance. The digital circuit and vector summer are also included in the design. The proposed phase shifter exhibits good performance for millimeter-wave communication application.

References

[1] C.-W. Wang, H.-S. Wu, and C.-K. C. Tzuang, "CMOS passive phase shifter with group-delay deviation of 6.3 ps at *K*-band," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 7, pp. 1778–1786, Jul. 2011, doi: 10.1109/TMTT.2011.2146267.

[2] M. Meghdadi, M. Azizi, M. Kiani, A. Medi, and M. Atarodi, "A 6-bit CMOS phase shifter for *S*-band," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3519–3526, Dec. 2010, doi: 10.1109/TMTT.2010.2086310.

[3] J.-C. Wu, T.-Y. Chin, S.-F. Chang, and C.-C. Chang, "2.45-GHz CMOS reflection-type phase-shifter MMICs with minimal loss variation over quadrants of phase-shift range," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 10, pp. 2180–2189, Oct. 2008, doi: 10.1109/TMTT.2008.2003527.

[4] F. Ellinger, R. Vogt, and W. Bachtold, "Ultracompact reflective-type phase shifter MMIC at C-band with 360° phase-control range for smart antenna combining," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 481–486, Apr. 2002, doi: 10.1109/4.991386.

[5] C.-Y. Chen, Y.-S. Wang, Y.-H. Lin, Y.-H. Hsiao, Y.-C. Wum, and H. Wang, "A 36–40 GHz full 360° ultra-low phase error passive phase shifter with a novel phase compensation technique," in *Proc. 47th Eur. Microw. Conf. (EuMC)*, Nuremberg, Germany, 2017, pp. 1245–1248, doi: 10.23919/EuMC.2017.8231076.

[6] S. Y. Kim, D.-W. Kang, K.-J. Koh, and G. M. Rebeiz, "An improved wideband all-pass I/Q network for millimeter-wave phase shifters," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3431–3439, Nov. 2012, doi: 10.1109/TMTT.2012.2212027.

[7] Y. Yu *et al.*, "A 60-GHz 19.8-mW current-reuse active phase shifter with tunable current-splitting technique in 90-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 5, pp. 1572–1584, May 2016.

[8] K.-J. Koh and G. M. Rebeiz, "0.13-μm CMOS phase shifters for X-, Ku-, and *K*-band phased arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535–2546, Nov. 2007, doi: 10.1109/JSSC.2007.907225.

[9] D. Pepe and D. Zito, "Two mm-wave vector modulator active phase shifters with novel IQ generator in 28 nm FDSOI CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 344–356, Feb. 2017, doi: 10.1109/JSSC.2016.2605659.

[10] S. P. Sah, X. Yu, and D. Heo, "Design and analysis of a wideband 15–35-GHz quadrature phase shifter with inductive loading," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 3024–3033, Aug. 2013, doi: 10.1109/TMTT.2013.2267749.

[11] Y.-Y. Huang, H. Jeon, Y. Yoon, W. Woo, C.-H. Lee, and J. S. Kenney, "An ultra-compact, linearly-controlled variable phase shifter designed with a novel RC poly-phase filter," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 2, pp. 301–310, Feb. 2012, doi: 10.1109/TMTT.2011.2177856.

[12] A. Asoodeh and M. Atarodi, "A full 360° vector-sum phase shifter with very low RMS phase error over a wide bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1626–1634, Jun. 2012, doi: 10.1109/TMTT.2012.2189227.

[13] X. Quan *et al.*, "A 52–57 GHz 6-bit phase shifter with hybrid of passive and active structures," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 3, pp. 236–238, Mar. 2018, doi: 10.1109/LMWC.2018.2802706.

[14] J. Park, S. Lee, D. Lee, and S. Hong, "9.8 A 28GHz 20.3%-transmitter-efficiency 1.5°-phase-error beamforming front-end IC with embedded switches and dual-vector variable-gain phase shifters," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2019, pp. 176–178.

[15] T. Wu *et al.*, "A Ku-band 6-bit vector-sum phase shifter with half-quadrant control technique," *IEEE Access*, vol. 8, pp. 29311–29318, 2020, doi: 10.1109/ACCESS.2020.2966277.