A SiGe-BiCMOS Wideband Active Bidirectional Digital Step Attenuator With Bandwidth Tuning and Equalization

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***Abstract*— A 6-bit active digital step attenuator (DSA), which simultaneously achieves wide bandwidth, flat gain characteristics, and bidirectional operation, is proposed for wideband phased-array antennas. In addition, it supports bandwidth tuning and equalization function to reduce complexity and physical size of systems. The proposed circuit utilizes an active double-pole double-throw switch, which provides positive gain with four-way switching and bidirectional operation. In addition, the simplified switched T-type topologies are applied to improve the insertion loss and save on chip area for low-attenuation states (0.5, 1, and 2 dB). Implemented in a 130-nm SiGe-BiCMOS technology platform, the proposed active DSA provides the advantages of seamless integration with digital control blocks and wide operational bandwidth due to its low parasitic capacitance. The active DSA exhibits flat in-band gain of >7 dB and the input/output return losses <9 dB from 2 to 20 GHz, which covers S-, C-, X-, and Ku-bands. In addition, it shows the root-mean-square amplitude and phase errors of <0.3 dB and <3.4°, respectively. The measured output 1-dB compression point is −3.6 dBm with a dc power consumption of 75 mW. The chip area of the active DSA is 1.43 × 1.23 mm^2, including pads.**

***Index Terms*— Active switch, BiCMOS, bidirectional amplifier (BDA), bidirectional operation, digital step attenuator (DSA), SiGe HBT, wideband phased-array antennas.**

I. Introduction

IT IS well known that wideband amplitude control circuits are key components for realizing various applications, such as high data rate wireless communications, temperature compensation, automatic gain control of transmitter/receiver systems, and wideband phased-array antenna systems [1]–[3]. To meet recent high-level system demands, such as low cost, high yield, high integration level, and low system complexity, designers need to consider additional functionality over the conventional designs. To satisfy these recent demands, wideband amplitude control circuits require gain or loss flatness with bidirectional operation as well as wide operational bandwidth and compact chip size. In addition, such systems need to support highly accurate and wide amplitude control range with low phase/amplitude errors to reduce system complexity by minimizing phase/amplitude calibration and data errors [4], [5]. Since the high-level systems require passive-based circuits such as power dividers/combiners, radio frequency (RF) switches, and control circuits, an insertion loss (IL) and a frequency dependent loss characteristic can affect the performance, complexity, and physical size of the system. Therefore, the system configuration can be further simplified if additional functions such as bandwidth tuning and equalization function can be added to the amplitude control circuit.

In order to realize the amplitude control circuits, variable gain amplifiers (VGAs) and passive-based attenuators

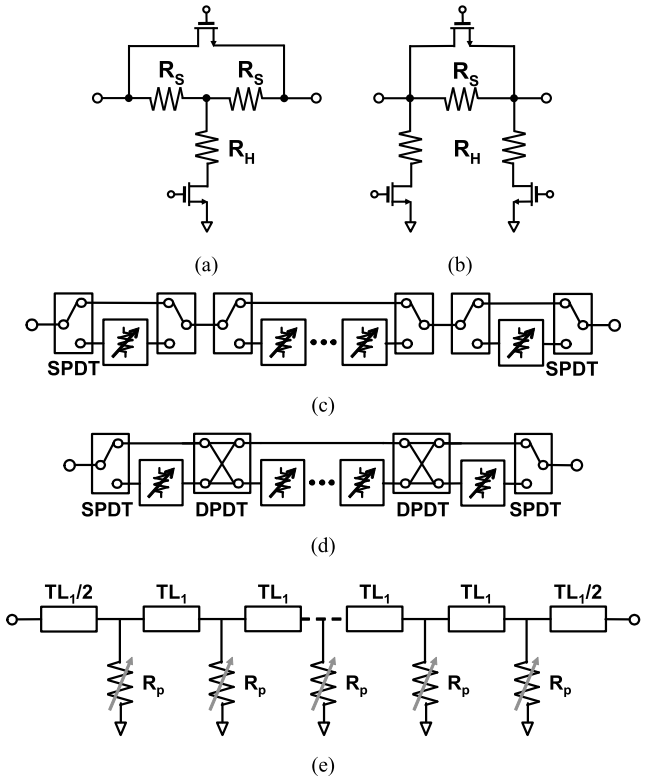

Fig. 1. Conventional topology DSA. (a) Switched T-type. (b) Switched Pi-type. (c) SPDT-based switched path. (d) DPDT-based switched path. (e) Distributed step attenuator with variable resistors after [15].

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(analog and digital types) have been widely used for RF and millimeter-wave applications. While VGAs provide gain with amplitude control functionality unlike passive-based attenuators, it must be separately added in both receive and transmit paths due to its uni-directional operating characteristics. In addition, it has limitations such as bandwidth, high phase variation during amplitude control, dc power consumption, and low power-handling capability [6], [7]. On the other hand, passive-based digital step attenuators (DSAs) provide advantages such as low-power consumption, high linearity, and simple control, as shown in Fig. 1 [8]–[14]. However, the switched T-/Pi-type attenuators provide low IL and small chip size, as shown in Fig. 1(a) and (b), but exhibit large phase variations under amplitude control and have limited bandwidth [8], [9]. The switched path attenuators [see Fig. 1(c) and (d)] have been introduced to minimize the phase variation and extend bandwidth [10]–[13]. However, they show high IL and frequency dependent loss characteristics, which dramatically degrades depending on the amplitude control range. On the other hand, low IL and relatively flat transmission response over a wide frequency range and an attenuation range can be provided by the distributed attenuators [14], as shown in Fig. 1(e). However, a large chip area is required to achieve wide attenuation range with high resolution due to a large number of variable resistors and quarter-wave transmission lines. Therefore, the additional loss compensation amplifiers (LCAs) and equalizers are essential components in the passive-based DSAs in order to compensate their high IL and frequency dependent loss characteristics which are generated by many passive RF switches and quarter-wave transmission lines. From a system perspective, these components can increase the overall system size, dc power consumption, and system complexity and consequently limit the power-handling capability. Therefore, ideal wideband amplitude control circuits should support wideband operation, simple control, and small chip size. In addition, they should provide bidirectional operation and positive flat in-band gain without additional LCAs and equalizers, in order to minimize system complexity and configure a high-level system.

The proposed DSA was briefly introduced in [15] to provide the circuit configuration and small-signal measurement results under major attenuation states. In this paper, we propose a wideband active bidirectional 7-bit DSA including 0.5-dB tuning bit to overcome the limitations associated with the previous active and passive-based amplitude control circuits. In addition, a detailed description related to bandwidth, bandwidth tuning, and equalization function of the bidirectional amplifier (BDA) core are provided to describe the additional benefits of the proposed wideband active DSA. In the proposed design, a combination of a wideband active double-pole double-throw (DPDT) switch [16] and a simplified switched T-type attenuator [13] techniques provide a positive flat in-band gain response, bidirectional operation, and small chip size by eliminating the additional LCAs and equalizers. In addition, since SiGe HBTs show small parasitic capacitance under the same transconductance compared to the CMOS technology, a SiGe BiCMOS platform is chosen in this design. In Section II, we describe the design and bandwidth tuning capability including equalization function of the wideband active DPDT switch. Section III provides the configuration and the optimization of the proposed wideband active bidirectional DSA. The measured results are presented in Section IV. The analysis of the advantages and the potential limitations of the proposed DSA and the future work are discussed in Section V. Finally, we will summarize this paper in Section VI.

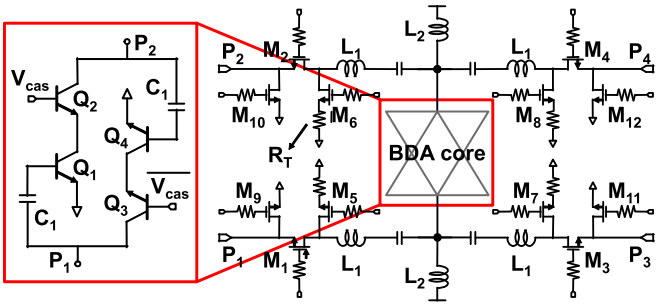

Fig. 2. Schematic of the wideband active bidirectional SiGe DPDT switch with BDA core and series–shunt switches after [16].

II. Design of the Active DPDT Switch

Fig. 2 shows the schematic of the wideband active DPDT switch with BDA and series–shunt switch techniques. The active DPDT switch design and measured RF performance were previously discussed in [16] (excluding circuit analysis). However, to illustrate the operation, a brief description is included here and a detailed circuit analysis of the bandwidth tuning and equalization function of the wideband active DPDT switch are provided.

A. Wideband Active DPDT Switch

To simultaneously provide four-way switching function, bidirectional operation, and positive gain response with equalization function, the wideband active DPDT switch consists of a single-stage BDA core and four series–shunt switches. The single-stage distributed amplifier using the BDA core provides positive in-band flat gain response and bidirectional operation over the wide operational bandwidth. To support the four-way switching function, the four series–shunt switches are applied in this design. However, since the IL of the series-shunt switch can degrade circuit performances (e.g., output power and gain), floating-body and N-well techniques are applied to improve the IL [17]. In addition, the two shunt transistors are added at both source and drain terminals of the series transistors to improve port-to-port isolation characteristic. On the other hand, since the leakage signal through the substrate from the series-shunt switch and the BDA core can potentially affect circuit performance, the P- substrate, P+, and N-well guard ring techniques are applied to prevent undesirable RF leakage signals [18].

B. BDA Core Structure

The simplified circuit schematic of the BDA core for forward direction from P_1 to P_2 is shown in Fig. 3(a). To provide bidirectional operation without supply voltage control [19],

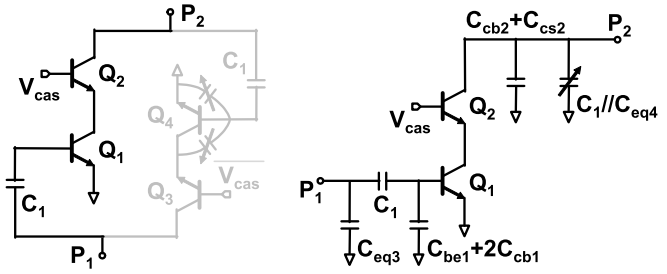

Fig. 3. (a) Simplified circuit schematic of BDA core for the P_1-to-P_2 mode (forward operation). (b) Equivalent circuit of the forward operation.

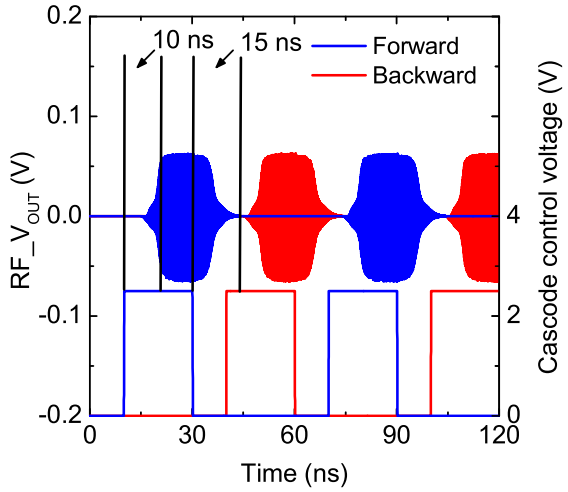

Fig. 4. Simulated mode selection of the active DPDT switch depending on cascode bias control at 10 GHz under the −20-dBm input power.

two cascode pairs (Q_1/Q_2 and Q_3/Q_4) are connected through the capacitors (C_1s) [16]. To amplify the signal from P_1 to P_2, the base terminal of Q_2 is "HIGH (2.5 V)" and Q_3 is "LOW (0 V)" while both Q_1 and Q_4 are biased by an external current source through current mirrors. Under this bias condition, the BDA core becomes a single-stage cascode amplifier [see Fig. 3(a)]. In addition, the voltage at base terminal of Q_2 and $Q_3(V_{cas})$ can provide high-speed mode switching between forward and backward operations compared to the supply voltage switching approach [19]. However, the V_{cas} should be carefully controlled because the BDA core requires settling time for mode selection. If the voltages at the base terminals of Q_2 and Q_3 are turned ON and OFF simultaneously, the BDA core may show an unstable behavior because of a positive feedback loop. As shown in Fig. 4, it takes about 10 and 15 ns to stabilize the BDA core by control signals of rising and falling for mode selection, respectively. Therefore, the required minimum switching time is about 10 ns to select the forward and backward operations.

The capacitance C_1 is the key component in the BDA core for achieving high-speed mode selection by isolating the dc bias between the base terminal of Q_1 and Q_4 from the supply voltage (V_{CC}). In addition, it can optimize the total capacitance of the P_1 and P_2 nodes of the BDA core [16]. Since the total capacitance of the P_1 and P_2 nodes is key parameter to determine the bandwidth of the active DPDT switch, the capacitance value of C_1 should be carefully selected depending on the system requirement. In addition, the inductance value (L_1) is important to obtain a desired bandwidth and good matching characteristics [see Fig. 2] because the operational bandwidth of the active DPDT switch is determined by the 3-dB cutoff frequency (f_c) of an artificial transmission line, given as

$$f_{\text{c, input, output}} = \frac{1}{\pi\sqrt{L_{\text{input, output}} C_{\text{parasitic, input, output}}}}. \quad (1)$$

In addition, the characteristic impedance of the artificial transmission line for the input and output of the active DPDT switch can be calculated as follows:

$$Z_o = \sqrt{\frac{L_1}{C_{\text{par, BDAs}} + C_{\text{par, INDs, Lines}}}}. \quad (2)$$

Therefore, the bandwidth of the active DPDT switch is a primary contribution to determine the bandwidth of the proposed active bidirectional DSA. The equivalent circuit including all parasitic capacitances is shown in Fig. 3(b). The total capacitance of the P_1 and P_2 nodes can be calculated by equation. Equations (1)–(4) for forward operation under fixed dc bias condition and device size

$$C_{\text{total, input, forward}} = C_{\text{eq3}} + \left(\frac{C_1 \times (C_{\text{be1}} + 2C_{\text{bc1}})}{C_1 + (C_{\text{be1}} + 2C_{\text{bc1}})}\right) \quad (3)$$

$$C_{\text{total, output, forward}} = C_{\text{bc2}} + C_{\text{cs2}} + \left(\frac{C_1 \times C_{\text{eq4}}}{C_1 + C_{\text{eq4}}}\right) \quad (4)$$

where C_{be} and C_{bc} are the base–emitter and the base–collector capacitances, respectively. The collector-substrate capacitance is C_{cs}. The equivalent capacitances of C_{eq3} and C_{eq4}, including the parasitic capacitance of the OFF-state cascode pair, are defined as follows:

$$C_{\text{eq3}} = C_{\text{bc3}} + C_{\text{cs3}} \quad (5)$$

$$C_{\text{eq4}} = C_{\text{be4}} + \left(\frac{C_{\text{bc4}} \times (C_{\text{cs4}} + C_{\text{be3}})}{C_{\text{bc4}} + (C_{\text{cs4}} + C_{\text{be3}})}\right). \quad (6)$$

Based on (3)–(6), the capacitance of C_1 is a critical parameter under the same dc bias condition and device size. The total capacitance in backward operation can be calculated similarly as forward operation. The parasitic capacitance and the size of transistors of both operations are summarized in Table I.

TABLE I
PARASITIC CAPACITANCE AND SIZE OF TRANSISTOR IN BDA CORE

Parameter	Q_1		Q_2		Q_3		Q_4	
	P_1 TO P_2	P_2 TO P_1	P_1 TO P_2	P_2 TO P_1	P_1 TO P_2	P_2 TO P_1	P_1 TO P_2	P_2 TO P_1
W_E (μm)	0.12		0.12		0.12		0.12	
L_E (μm)	8.0		8.0		8.0		8.0	
C_{bc} (fF)	13.9	316.5	16	12.8	12.8	16	316.5	13.9
C_{be} (fF)	129.2	51.2	125.1	21.6	21.6	125.1	51.2	129.2
C_{cs} (fF)	7.3	11.3	6.8	6.7	6.7	6.8	11.3	7.3

TABLE II
PARASITIC CAPACITANCE OF Q_4 UNDER VARYING BIAS CONDITION

Para-meter	Q_4					
W_E (μm)	0.12					
L_E (μm)	12.0					
I_b (uA)	0	2.3	5.7	13.2	27.5	59.2
C_{bc} (fF)	22.3	107	188.8	344.5	580.1	975.1
C_{be} (fF)	32.5	52.9	58.2	68.0	94.1	283.4
C_{cs} (fF)	18.5	18.5	18.5	18.5	18.5	18.5
Total Cap. (fF)	P_1: 149 P_2: 73	P_1: 149 P_2: 97	P_1: 149 P_2: 102	P_1: 149 P_2: 109	P_1: 149 P_2: 121	P_1: 149 P_2: 169

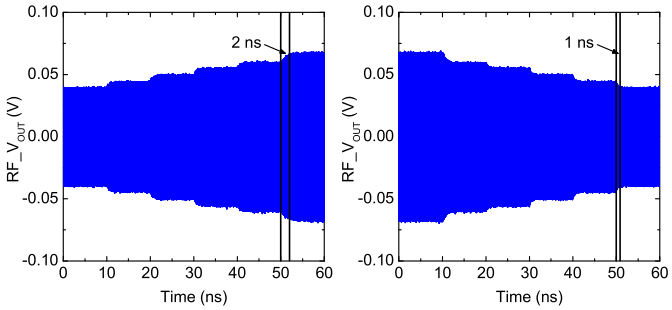

Fig. 5. Simulated transient signal of the active DPDT switch for bandwidth (a) increasing and (b) decreasing cases depending on the base current of Q_4 at 23 GHz under the −20-dBm input power.

On the other hand, C_{be4} and C_{bc4} can be controlled by the base current of Q_4 in the forward operation case [see Fig. 3(a)]. The V_{cas} of Q_3 is "LOW" and the supply voltage from P_1 is delivered to the collector node of Q_3, but the node voltage between Q_3 and Q_4 is close to 0 V under this conditions. While the supply voltage from P_2 is isolated from the base node of Q_4 by C_1, the base current of Q_4 is controlled by the external current source through the current mirror. Under this operation condition, the bandwidth of the active DPDT switch can be controlled because the total parasitic capacitance of P_2 node can be changed by the base current of Q_4 in the forward operation. The parasitic capacitances depending on the base current of Q_4 and the calculated total capacitances by (3)–(6) are summarized in Table II. Since forward-biased junction for Q_4 forms diffusion capacitances, it can support fast bandwidth tuning of the active DPDT switch. Fig. 5 shows simulated transient signals at the output port (RF_V_{out}) depending on the base current of Q_4 for bandwidth tuning at 23 GHz. For this transient 0simulation, the base current of Q_4 is controlled every 10 ns using the external current source. Under the condition of increasing bandwidth, the switching time for the bandwidth tuning is about 2 ns [Fig. 5(a)], and 1-ns switching time is approximately required to control the bandwidth reduction [Fig. 5(b)]. In addition, the active DPDT switch shows constant performance except for the bandwidth and the gain in the enhanced bandwidth because the base current of Q_4 does not affect the operation of the other transistors

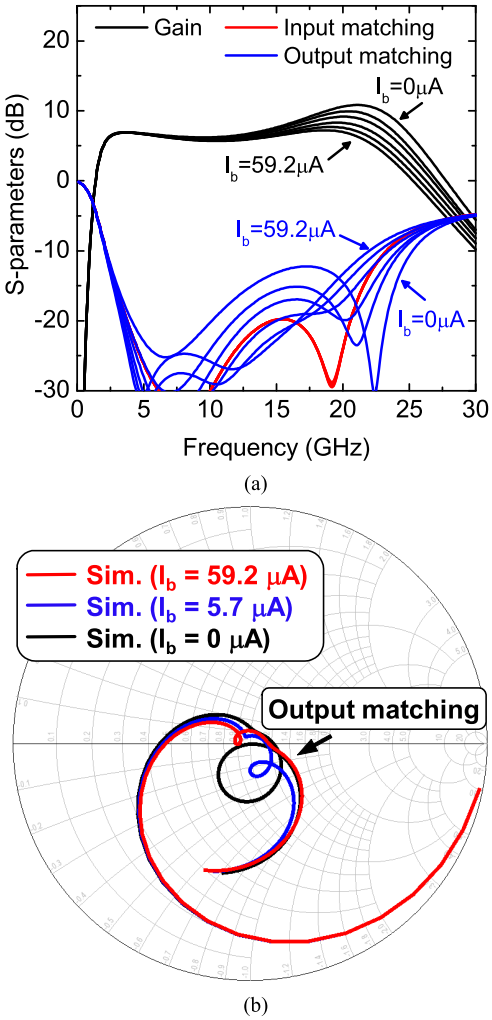

Fig. 6. (a) Simulated S-parameters and (b) output matching characteristics of the active DPDT switch with varying current at base terminal of Q_4 for bandwidth tuning (forward operation).

in the forward operation, as shown in Fig. 6(a). In addition, it can support an equalization function without additional components. The gain of the active DPDT switch is enhanced from 7 to 10.7 dB at 20 GHz and the bandwidth increases from 20 to 25 GHz. In the backward operation from P_2 to P_1, the base current of Q_1 should be controlled for bandwidth tuning and equalization. As shown in Fig. 6(b), the optimum output matching characteristic was achieved when the base current of Q_4 was 59.2 μA. By reducing the base current of Q_4, the output matching characteristic shifts from the 50-Ω point, which means that the characteristic impedance of the artificial transmission line increased. However, it exhibited better than 10-dB return loss over the desired frequency range of 2–20 GHz. In addition, since the 3-dB cutoff frequency of the artificial transmission line was extended, it provided bandwidth tuning and equalization functions. Fig. 7 presents the measured and simulated S-parameters of the active DPDT switch. The measured gain was degraded about 1 dB due to unexpected layout parasitic elements.

The BDA core is used in the active DPDT switch for two main purposes. The first priority of BDA core is bidirectional operation. Since it provides bidirectional operation without

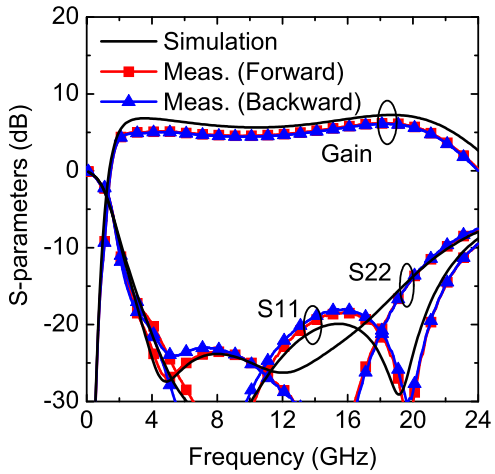

Fig. 7. Measure and simulated S-parameters of the active DPDT switch.

additional switches, it can save the chip area by eliminating the need to place it in each of the TX and RX paths separately. In addition, it can support competitive switching time (10 ns) compared to commercial switches (20 ns) [20]. Second, it provides positive gain with the bandwidth tuning and equalization function. From a system perspective, where many passive circuits (e.g., control circuits, power dividers/combiners, and switches) are used for wideband applications such as large-scale phased-array antennas, wideband switch matrices, and switched beamforming, bandwidth tuning and equalization function are required to compensate for the IL and frequency dependent loss characteristics generated from them. Therefore, the proposed active DSA using active DPDT switch provides bidirectional operation, bandwidth tuning, and equalization as well as amplitude control, positive gain and wideband characteristics.

III. Proposed Wideband Active Bidirectional DSA

For achieving wide attenuation range, low phase/amplitude errors, simple control, and compensating IL, the proposed wideband active bidirectional DSA is implemented by combining the topologies of the switched path and switched T-type in Fig. 8. In addition, the internal digital control circuit is applied to the proposed DSA for simplifying attenuation control. The control voltage of 1.2 V is chosen for the switched T-type and path attenuators to be compatible with the internal digital circuitry. Since the switched path topology shows the identical parasitic elements of the reference and attenuation path in all attenuation states, this topology was applied to the high attenuation of 4, 8, and 16 dB to achieve for low phase variation. For the low attenuation levels, switched T-type attenuators are used to save chip area and improve the IL. However, as described in the introduction, since both topologies have disadvantages (e.g., IL, phase variation, and frequency dependent loss characteristics), new design approaches are applied to the proposed DSA to overcome these disadvantages.

A. Simplified Switched T-Type Attenuator

As shown in Fig. 9(a), the conventional switched T-type attenuator is composed of series and shunt transistors and resistive T-network. To design the conventional switched T-type attenuator with desired attenuation, the size of the transistors and resistance values need to be determined considering the IL, return loss, attenuation level, and bandwidth, etc. To select the desired attenuation state, the series and shunt transistors should be turned ON or OFF. In addition, since the number of series transistor is decided by the required attenuation range, it exhibits high IL and frequency dependent loss characteristic due to the series transistors. If the series transistor can be removed while achieving the desired attenuation state, it can improve the IL and frequency dependent loss characteristics of the switched T-type attenuator. To eliminate the series transistor, we need to pay attention to the resistive T-network. For the low attenuation, the small series and large shunt resistances are required in the resistive T-network. For example, the series and shunt resistances are 2.9 and 433.3 Ω for 1-dB attenuation, respectively. Therefore, by properly adjusting the shunt resistance, the series resistors and transistor can be eliminated while satisfying other parameters such as return loss and phase variations for general requirements, simultaneously, as shown in Fig. 9(b) [13]. As a result, the simplified switched T-type attenuator improves the IL and frequency loss characteristics and provides simple layout. Fig. 10 shows comparison of the IL between the conventional and simplified designs for the switched T-type attenuator for 1-dB attenuation. The simplified T-type attenuator exhibits excellent IL and frequency dependent loss characteristic compared to the conventional designs. The simulated return loss of both designs is better than 10 dB from dc to 30 GHz. However, this design is not suitable for the high attenuation due to the high series resistance of the resistive T-network. Therefore, as described above, the switched path attenuator is applied for the high attenuation states.

B. Switched Path Attenuator With Active DPDT Switch

The conventional attenuators (e.g., switched T-type and VGA) exhibit the high phase variation in the high attenuation states during the amplitude control, except for the switched path topology. Therefore, the switched path topology is chosen for high attenuation of 4, 8, and 16 dB in the proposed wideband active bidirectional DSA. However, the conventional switched path attenuators show the high IL and frequency dependent loss characteristics due to many passive-based RF switches. In addition, based on the discussion in Section III-A, the IL of the simplified switched T-type attenuators is improved by eliminating the series transistor and resistors but cannot be negligible. Therefore, the proposed switched path attenuator requires a novel circuit configuration to compensate the IL and frequency dependent loss characteristics which are generated from switched T-type attenuators and passive RF switches without additional components. The proposed switched path attenuator consists of the active DPDT switches, the single-pole double-throw (SPDT) switches, and resistive T-networks. The active DPDT switches in the proposed switched path attenuator not only provide switch functionality by replacing existing passive RF switches such as SPDT and DPDT switches, but also support the positive in-band

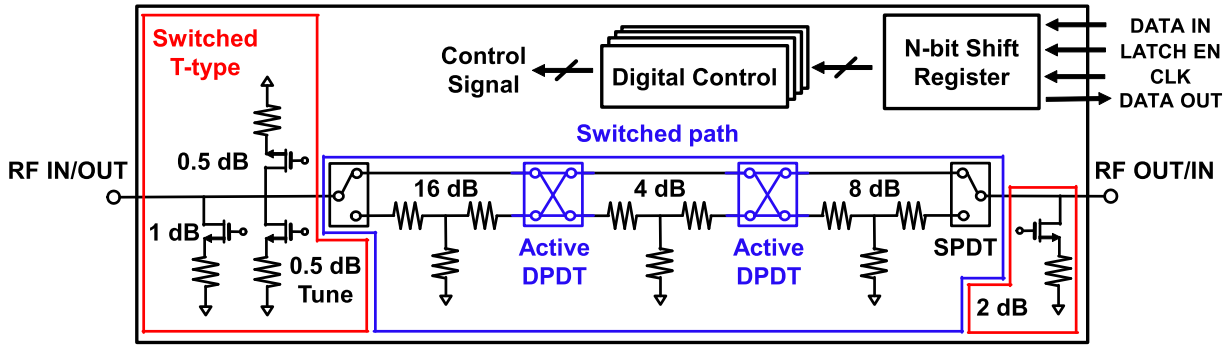

Fig. 8. Block diagram of the proposed wideband active bidirectional SiGe DSA.

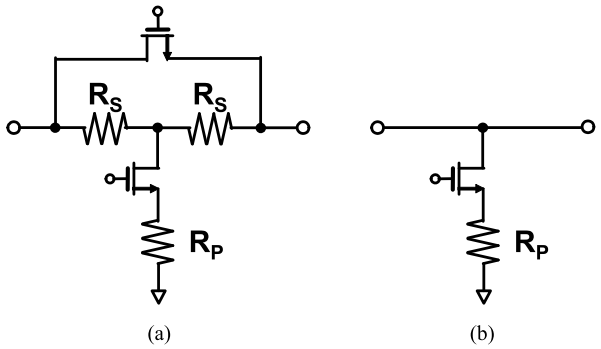

Fig. 9. Schematic of (a) conventional switched T-type attenuator and (b) simplified switched T-type attenuator.

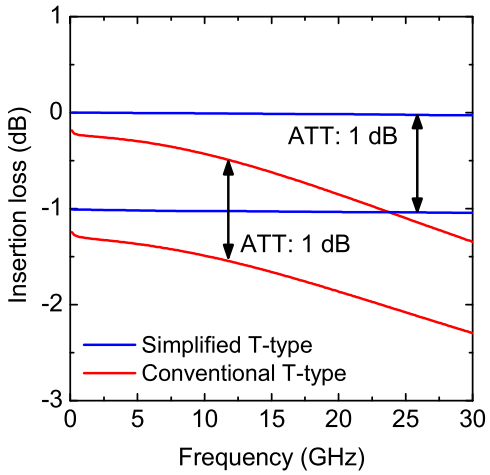

Fig. 10. Simulation of the IL between conventional and simplified switched T-type attenuators.

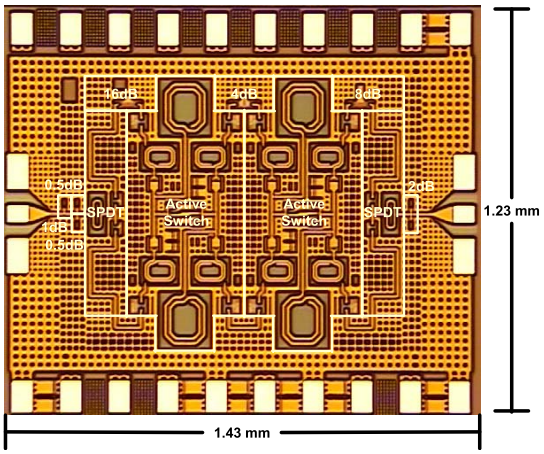

Fig. 11. Microphotograph of the proposed wideband active bidirectional SiGe DSA after [15].

flat gain response, bidirectional operation, bandwidth tuning, and equalization functionality without additional LCAs and equalizers. As a result, the proposed wideband active bidirectional DSA can reduce system complexity and physical size by eliminating additional LCAs and equalizers which are required for passive-based attenuators. In addition, this configuration supports a wide attenuation range with low phase/amplitude errors. Although the power-handling capability may be lower than the passive-based attenuators, the proposed DSA can be suitable for various systems because the passive-based attenuators require additional LCAs and equalizers when considering the entire system requirement.

The passive components, such as inductors, interconnections, and RF GSG pads in the proposed DSA were simulated and optimized. To achieve accurate circuit performance, minimizing unexpected signal coupling and leakage are critical in wideband circuits. Therefore, the interconnections are designed using grounded coplanar waveguide structures to minimize signal coupling and leakage that may occur between adjacent signal lines. In addition, since a symmetric layout and topology is critical to achieve the identical circuit performance, all subcomponents such as active DPDT switches, SPDT switches, switched T-type attenuators, and resistive T-network were carefully placed and simulated with an electromagnetic solver (Sonnet [21]).

IV. Measurements

Fig. 11 shows the microphotograph of the fabricated wideband active bidirectional DSA and the chip area, excluding the pads, was 1.14 × 0.86 mm^2 (0.98 mm^2). The circuit was implemented in Global Foundries 130-nm SiGe HBT BiCMOS technology (GF 8HP). From a supply voltage of 2.5 V, the circuit draws a bias current of 30 mA, which amounts to the total dc power consumption of 75 mW. The small-signal performance of the proposed DSA was measured with on-wafer probing using a network analyzer (Agilent PNA E8364B).

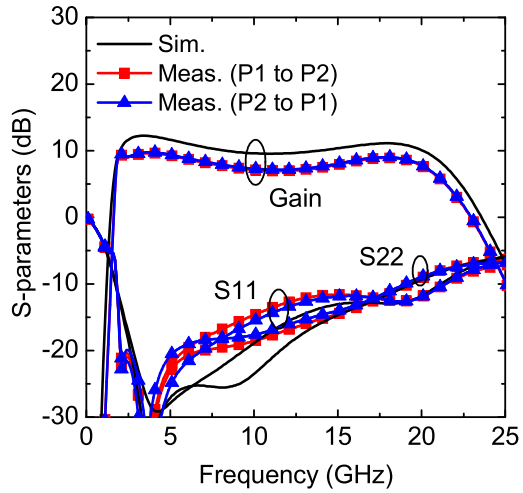

Fig. 12. Measured and simulated S-parameters of the proposed wideband active bidirectional DSA at the reference state under the bidirectional operation.

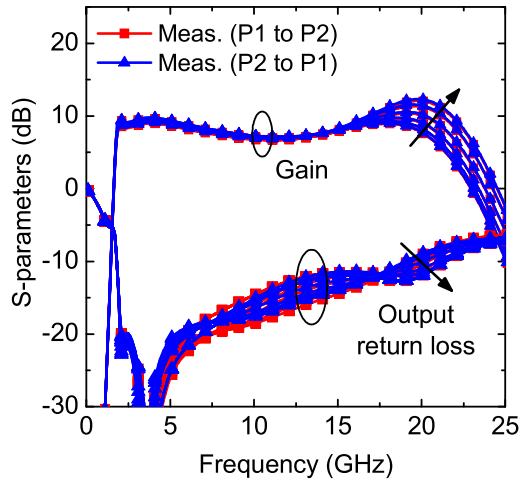

Fig. 13. Measured gain and output return losses of the proposed DSA with varying current at base terminals for the bandwidth tuning and equalization.

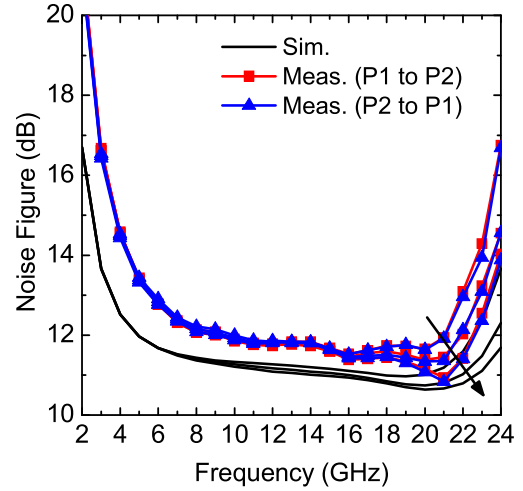

Fig. 14. Measured and simulated NF of the proposed DSA under with varying current at base terminals for the bandwidth tuning and equalization.

Fig. 12 shows the measured and simulated S-parameters at the reference state of the proposed DSA. In the measurement results, the proposed DSA provided a positive gain

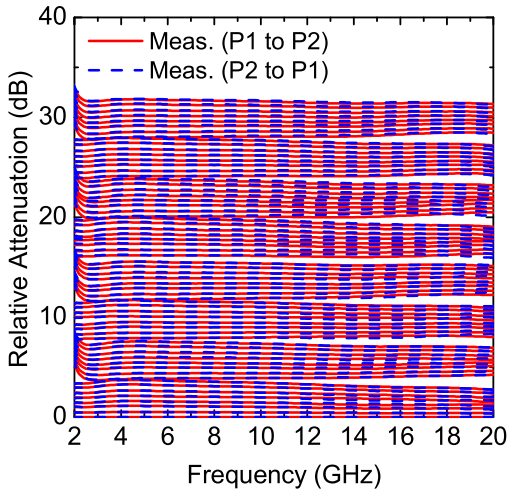

Fig. 15. Measured relative attenuation of the proposed wideband active bidirectional DSA under the bidirectional operation.

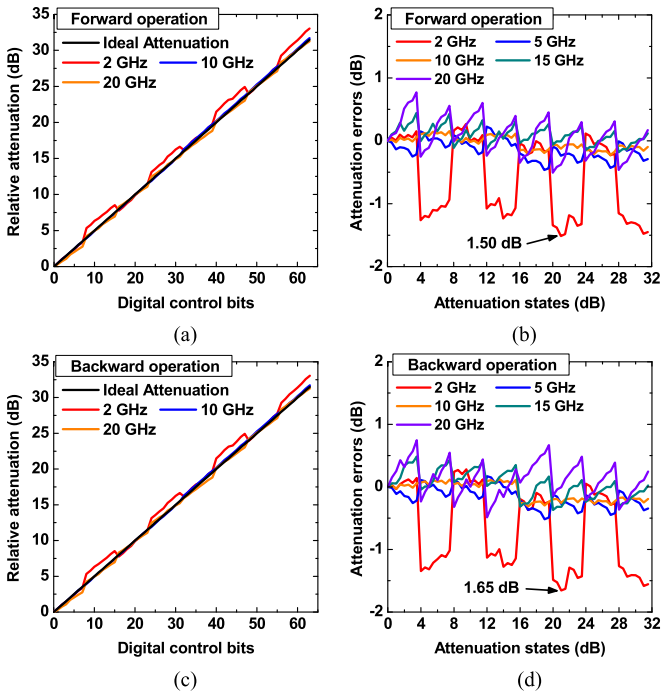

Fig. 16. Measured (a) relative attenuation and (b) attenuation errors of the forward operation, and (c) relative attenuation and (d) attenuation errors of the backward operation over the 64 states.

(7.7–9.6 dB) instead of the IL compared to a typical passive-based design. The input and output return losses were better than 9 dB at 2–20 GHz. As described above, the measured gain was slightly reduced compared to the simulation results because the gain of the active DPDT switch was degraded by about 1 dB. Both direction of the forward and the backward operations showed identical circuit response because of symmetric layout and topology.

As described in Section II, the bandwidth tuning and equalization function can be controlled by the base current of the common emitter transistors (Q_1 or Q_4) depending on the required directions. The S-parameters of the proposed DSA for the bandwidth tuning and equalization function at the

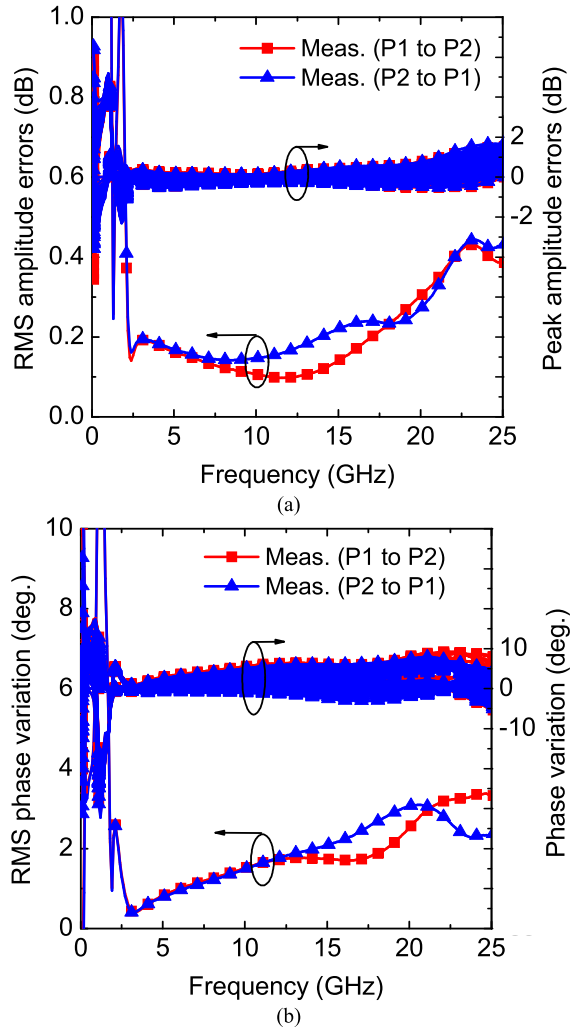

Fig. 17. Measured rms. (a) Amplitude errors. (b) Phase variations over the 64 attenuation states.

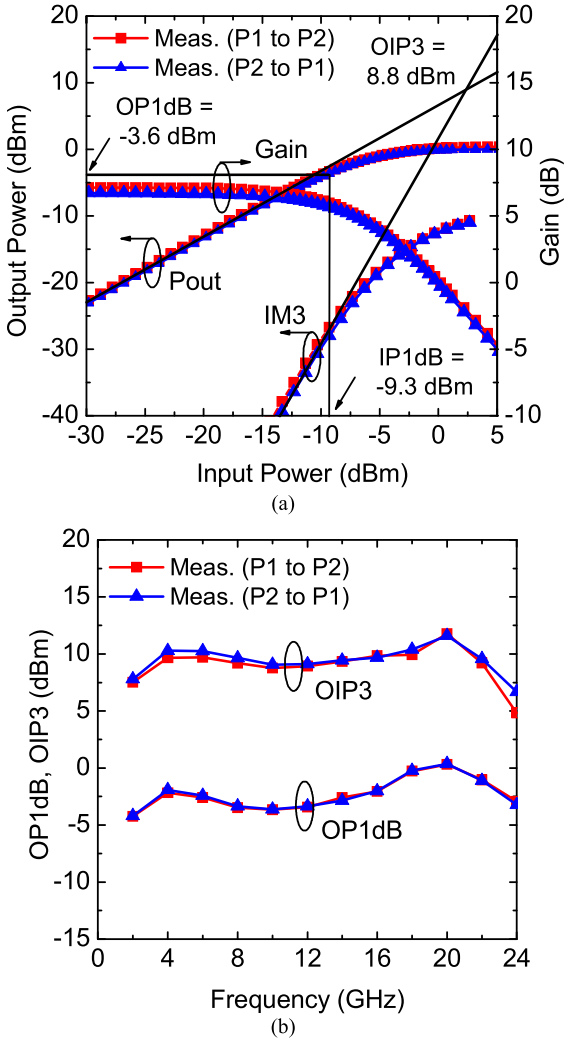

Fig. 18. (a) Measured large-signal responses of the proposed wideband active bidirectional DSA at 10 GHz and (b) measured OP1dB and OIP3 versus frequency.

reference state are shown in Fig. 13. The gain was enhanced from 7.7 to 12.3 dB at 20 GHz and the gain bandwidth was improved from 20 to 23 GHz based on 7.7-dB gain. In addition, output return loss was enhanced 20 to 22.5 GHz based on the output return loss of 9 dB while maintaining input return loss response. The proposed DSA exhibited the identical response for bidirectional operations (forward and backward) in bandwidth tuning and equalization function as the reference state (see Fig. 12). In addition, since the attenuation through the resistive T-networks shows a constant characteristic in the wideband, the bandwidth tuning, and equalization function depending on the attenuation state showed a similar tendency to the response at the reference state.

The measured and simulated noise figure (NF) versus frequency depending on bandwidth tuning and equalization function is presented in Fig. 14. To confirm the NF performance, the PXA signal analyzer (N9030A) and the noise source (N4002A) were used with on-wafer probing. Under normal operating conditions, the minimum NF was 11.5 dB at 15 GHz and the overall NF was better than 12.7 dB at 5–20 GHz. The minimum NF was 10.8 dB at 20 GHz under maximum bandwidth and equalization conditions. From a system perspective, since the NF of the receiver signal path is decided by a front-end circuit (LNA), the NF of whole system can be improved compared with receivers with passive-based DSAs. In addition, the proposed DSA provides competitive NF when compared with [22] and [23].

Fig. 15 shows the measured relative attenuation over the operational frequency. The maximum attenuation range was 31.5 dB and a least significant bit (LSB) was 0.5 dB. When the resistive T-network for the 4-dB attenuation was selected, the attenuation errors were occurred at low and high frequencies. The attenuation error is the difference between ideal attenuation (from 0 to 31.5 dB with 0.5-dB LSB) and the measured relative attenuations. To observe the relative attenuation and attenuation errors in various frequencies in detail, the relative attenuation and attenuation errors for forward operation are shown in Fig. 16, along with the digital control bits. The worst error of the forward operation was 1.5 dB at 2 GHz, and the attenuation errors were less than 0.5 dB, except 2 and 20 GHz, as shown in Fig. 16(b). On the other hand, the backward operation had a peak error of 1.65 dB at 2 GHz and the overall

TABLE III
COMPARISONS OF THE RECENTLY PUBLISHED AMPLITUDE CONTROL CIRCUIT WITH THIS PAPER

Ref.	[6]	[7]	[10]	[11]	[13]	[14]	**This work**
Tech	SiGe HBT	0.13 μm SiGe BiCMOS	0.18 μm CMOS	GaAs	0.18 μm CMOS SOI	0.12 μm BiCMOS	**0.13 μm SiGe BiCMOS**
Bandwidth tuning / Equalization function	None / None	None / None	None / None	None / None	None / None	None / None	**Support / Support**
Topology	VGA	VGA	Switched Pi/T w/ phase correction	Switched T	Switched path and T w/ DPDT switch	Distributed	**Switched path and T w/ active switch**
Freq. [GHz]	10 – 14.4	26 – 30	0 – 14	0 – 40	0 – 20	10 – 50	**2 – 20 / 2 – 23**
Attenuation range [dB]	22.0 (14-states) (LSB=1.50 dB)	18.0	31.5 (6-bit) (LSB=0.50 dB)	23.0 (5-bit) (LSB=1.00 dB)	31.0 (5-bit) (LSB=1.00 dB)	11.0 (11-states) (LSB=0.90 dB)	**31.5 (6-bit) (LSB=0.50 dB)**
Gain [dB]	11.5±1.5	18	-7.0±3.0	-4.5±3.5	-5.3±2.2	-2.5±0.5	**8.6±1.0**
Return loss [dB]	> 11	N/A	> 9	> 14	> 12	> 19	**> 9**
RMS Amp. error [dB]	N/A	< 0.5	< 0.5	N/A	< 0.5	N/A	**0.63 @ 2 GHz < 0.3 (2.2-25 GHz)**
RMS phase variation [degree]	$\leq 2^{\#}$	$< 5^{\#}$	< 4.2	N/A	< 2.5	< 3	**< 3.4**
Noise Figure [dB]	< 7	7.4 @ 28 GHz*	-	-	-	-	**< 12.7 (5-20 GHz)**
IP1dB / IIP3 [dBm]	-17 / -3 @ 12 GHz	-13 / - @ 28 GHz	13 / 28 @ 10 GHz	N/A	10 / - @ 10 GHz	4 / - @ 35 GHz	**-9.3 / 2.3 @ 10 GHz**
P_{dc} [mW]	83	35	0	0	0	0	**75**
Die area [mm^2]	1.3	-	0.5^{+}	4.48	0.63	0.15^{+}	**0.98^{+} / 1.76**

*: Simulation. +: active area. #: phase variation

performance was similar to the forward operation, as shown in Fig. 16(d). The resistive T-network for the 4-dB attenuation used tantalum nitride (TaN) resistors for series and parallel resistance while N diffusion and TaN resistors were applied for parallel and series resistance in resistive T-network of the 8 and 16 dB, respectively. Therefore, as shown in Fig. 16, it shows a relatively high attenuation error when the resistive T-network for the 4-dB attenuation was selected.

Fig. 17 shows the measured root-mean-square (rms) amplitude error and phase variation of all 64 attenuation states. The maximum rms amplitude error was 0.63 dB at 2 GHz, but less than 0.3 dB from 2.2 to 20 GHz. The rms phase variation was less than 3.4° at 2–25 GHz for both bidirectional operations. The measured group delay was 163 ± 19 ps across 4–24 GHz and the maximum group delay variation over the 64 attenuation states was about 4 ps at 20 GHz. As described above, the 4-dB resistive T-network is the main contribution to the amplitude error at 2 GHz. In addition, since imperfect RF-choke inductors and dc-blocking capacitors were applied to the active DPDT switch without the use of external bias tees, in order to achieve high-level system integration, the amplitude errors, phase variations, group delays, and NF were degraded in the low-frequency range.

The measured large-signal performance of the proposed DSA at reference state is presented in Fig. 18. The input and output 1-dB compression point (IP1dB and OP1dB) and output third-order intercept point (OIP3) at 10 GHz are shown in Fig. 18(a). The OP1dB was about −3.6 dBm and the corresponding IP1dB was −9.3 dBm. In addition, the third-order intermodulation distortion (IM3) was measured with two different signals which had 50-MHz spacing. The measured OIP3 was roughly 8.8 dBm at 10 GHz. The measured OP1dB and OIP3 versus frequency were shown in Fig. 18(b). It exhibited −4.4 and 0.4 dBm of the OP1dB at 2 and 20 GHz, respectively. The OIP3 was found to be 7.6 and 11.7 dBm at 2 and 20 GHz, respectively. The measurement results show almost identical performance for both forward and backward operations.

The comparisons with other recent state-of-the-art designs are summarized in Table III. The proposed active bidirectional SiGe DSA achieves positive in-band flat gain with wide operational frequency instead of IL, and frequency dependent loss characteristics compared to the passive-based attenuators due to the new design approach utilized (simplified T-type attenuator and switched path attenuator with the active DPDT switch). In addition, it can support controllable

bidirectional operation (TX/RX modes), bandwidth tuning capability, and equalization functionality by using the active DPDT switch. Other parameters (e.g., impedance matching, amplitude error, and phase variation) also can be compatible with other state-of-the-art designs.

V. Discussion

The proposed wideband active bidirectional DSA presented in this paper provides positive in-band flat gain response, bidirectional operation, wide attenuation range, low amplitude error, and relevant phase variation. In addition, it supports bandwidth tuning and equalization function to compensate for IL and frequency dependent loss characteristics of the passive-based circuits which are required in the systems. In order to achieve positive gain with wide operation frequency, a SiGe-BiCMOS technology was selected in this paper because it exhibits lower parasitic capacitance compared to other technologies (e.g., CMOS and CMOS SOI) under the same transconductance. In addition, the small amplitude errors and phase variations of the proposed DSA can minimize the required amplitude/phase calibration circuitries in the systems and reduce data errors. However, in comparison with the passive-based attenuators, it has the drawbacks such as the dc power consumption and low power-handling capability. Despite these drawbacks, since the passive-based attenuators require LCAs and equalizers to compensate for the IL and frequency dependent loss characteristics for the system configuration, the proposed DSA can save the physical size of the system and significantly reduce the complexity of the system. Therefore, the proposed DSA can be applied to various systems without additional LCAs and equalizers.

For future work, additional optimization is required to improve the amplitude errors at the low- and high-frequency range caused by the resistive T-network for 4-dB attenuation. In addition, further studies are needed to improve the power-handling capability of the active DPDT switch.

VI. Summary

This paper has introduced the wideband active bidirectional DSA with bandwidth tuning and equalization function. To provide the positive in-band flat gain response and the wide attenuation range with low amplitude errors and phase variations, the proposed DSA consists of the simplified switched T-type attenuators and the switched path attenuator with the active DPDT switch using the 130-nm SiGe BiCMOS platform. In addition, the proposed DSA focuses on the effects of bandwidth tuning and equalization function as well as the wide attenuation range with low amplitude errors and phase variations based on the BDA applied to the active DPDT switch. Therefore, the proposed DSA is expected to be applicable to various wideband applications.

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