A 3–6-GHz Wideband Compact 6-Bit Phase Shifter in 0.5-μm GaAs Technology

Jiahui Chen, Shouxian Mou, Kaixue Ma, *Senior Member, IEEE*, and Fanyi Meng

***Abstract*— This letter presents a 3–6-GHz wideband compact 6-bit phase shifter (PS) in 0.5-μm GaAs pHEMT process. It combines a 3-bit enhanced high-pass/low-pass topology, a 2-bit modified low-pass/resonator topology, and a 1-bit switched-filter structure, with optimized cascade order to achieve a bandwidth (BW) up to 66.7%. Since the proposed PS consists of lumped elements and minimized the number of switches and inductors, it achieves a compact core size of 1.214 mm^2. The 64-output state PS exhibits high phase resolution of 5.625° with an rms phase error (PE) of less than 4°, and an insertion loss (IL) less than 6.7 dB at 3–6 GHz. To the best of our knowledge, this PS achieves the largest BW with the smallest chip size among the published 5-bit/6-bit GaAs/GaN PSs over a similar band.**

***Index Terms*— 0.5-μm GaAs, broadband, compact, low loss, monolithic microwave integrated circuit (MMIC), phase shifter (PS), phased array.**

I. Introduction

As THE core module of the phased array, the phase shifter (PS) is widely used in satellite communication, mobile communication, radar, etc., [1]–[10]. Promoted by increasing demands of these applications, the PS is continuously improving toward high phase resolution, wide bandwidth (BW), miniaturization, and low cost. This is particularly true for complex phased array applications where thousands of such PSs are required [1]. The development of monolithic microwave integrated circuit (MMIC) has made it possible to realize low cost and miniaturized chips. Correspondingly, there have been many efforts to realize this kind of PS. In [2], the PS adopted high-pass low-pass topology and a technique of embedding FETs into a phase-shifting circuit, which achieved 40% BW and chip size of 2.6 mm^2 but has a low phase-resolution (4-bit). Basically, as the phase-resolution increases, system performance will achieve incremental improvement while the contradiction between BW and chip size is getting more intense. The 5-bit PS based on the all-pass network in [3] has a small size of 1.63 mm^2, however, with a BW of only 10%. The 5-bit PS in [4] demonstrates 40% BW but occupies a large footprint of 23.5 mm^2.

In this letter, we propose a 3–6 GHz 6-bit PS, which has a good tradeoff of wide BW, miniaturization, low cost, and high phase resolution. The circuit adopting optimal topology for each bit and several chip miniaturization technologies is cascaded in an optimal order. The proposed PS based on 0.5-μm GaAs pHEMT process exhibits a compact size of 1.8 mm^2 (with pads) with 66.7% BW, which has a higher phase resolution and a 24.7% increase in BW comparing with the PS in [2].

Manuscript received May 1, 2020; revised June 17, 2020; accepted July 1, 2020. Date of publication July 17, 2020; date of current version August 7, 2020. This work was supported by the National Natural Science Foundation of China for Distinguished Young Scholar under Grant 61625105. *(Corresponding author: Shouxian Mou.)*

Jiahui Chen and Shouxian Mou are with the School of Physics, University of Electronic Science and Technology of China, Chengdu 610054, China (e-mail: sxmou@uestc.edu.cn).

Kaixue Ma and Fanyi Meng are with the School of Microelectronics, Tianjin University, Tianjin 300072, China.

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Digital Object Identifier 10.1109/LMWC.2020.3007836

TABLE I
PERFORMANCE SUMMARY OF SWITCHING DEVICES FROM FOUNDRY

Devices	IL (dB)	isolation (dB)	IP1dB (dBm)
Single gate switch	>0.5	>18	49*
Dual gate switch	>0.7	>21	45
Triple gate switch	>1.0	>23	38
D-mode CPW FET	>0.5	>1.6	28

* Gain compression = 0.5 dB.

II. Circuit Design

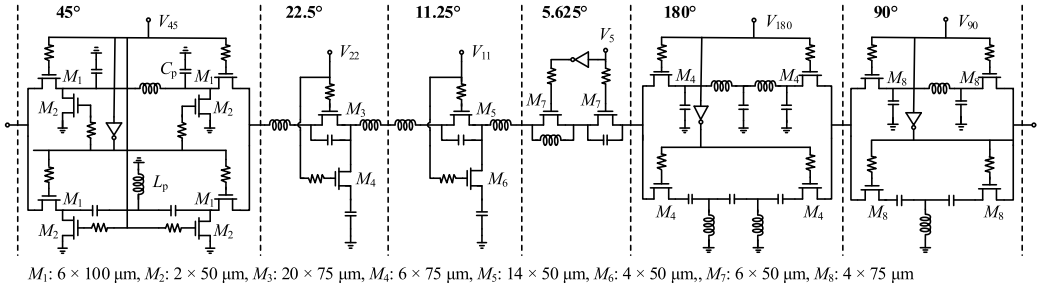
It is difficult for microwave PS to achieve ultrabroadband operation and harder to realize chip miniaturization design in low microwave frequency. Basically, three types of PS, including distributed PS, reflective-type PS (RTPS), and switched-type PS (STPS), are extensively employed in broadband PS designs.

The RTPS exhibits a wide BW, but with limited phase range [8], and the coupler inside occupies a large chip area at low microwave frequency. The distributed PS has the same issue for containing the quarter-wavelength transmission line [9]. However, the STPS based on lumped elements has the potential to realize the miniaturized design and wideband performance. Therefore, in this letter, an optimized STPS comprising a 3-bit enhanced high-pass/low-pass topology using a hybrid T/π network, a 2-bit modified low-pass/resonator topology, and a 1-bit switched-filter structure, is adopted for broadband and compact design. Fig. 1 shows the simplified schematic of the proposed 3–6 GHz 6-bit PS.

A. Switching Devices

The switches in PS design involves the tradeoff between isolation, insertion loss (IL), and linearity. Since the foundry provides several switching devices, simulation of these devices with 300-μm width is carried out from 1 to 8 GHz. The performance of these devices is compared in Table I, the single gate switch is utilized in this design based on overall consideration.

The threshold voltage of the switching FET is −1.2 V, a gate bias voltage of 0 V for ON-state, and −5 V for OFF-state is used in this letter. The gate bias voltage is applied through a large series resistor to reduce IL by minimizing signal leakage between the power supply and the RF path. A 10-kΩ mesa resistor is selected as a tradeoff between chip size, isolation, and switching speed. For the switching FETs



M_1: 6 × 100 μm, M_2: 2 × 50 μm, M_3: 20 × 75 μm, M_4: 6 × 75 μm, M_5: 14 × 50 μm, M_6: 4 × 50 μm,, M_7: 6 × 50 μm, M_8: 4 × 75 μm

Fig. 1. Simplified schematic of the proposed 3–6 GHz 6-bit PS.

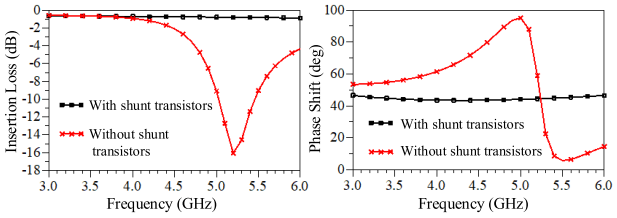


Fig. 2. Simulation results of the 45° bit section with/without shunt transistors.

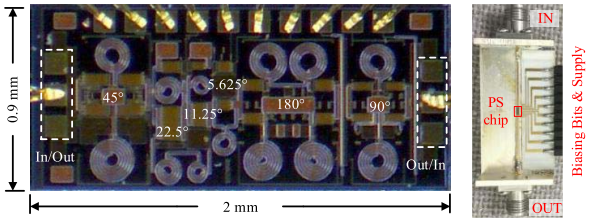


Fig. 3. Chip photo of the proposed 3–6 GHz 6-bit PS and evaluation board.

over 3–6 GHz, the normalized ON-state resistance is approximately 1.52 Ω·mm, and OFF-state capacitance is 0.11 pF/mm.

B. PS Design

The flat phase response and wide phase range of low-pass/high-pass PS have become the perfect choice for the design of 180°/90°/45° bits sections [11]. This topology can realize larger BW and better matching by increasing the order of the low-pass/high-pass filter. Considering the tradeoff between BW, performance, and area, the 45°/90° bits adopt third-order filters and the 180° bit adopts fifth-order filters. For the compact implementation purpose, series-type single-pole/double-throw (SPDT) switches and an improved hybrid topology that combines a high-pass T-network and a low-pass π-network are utilized. With the same performance to the all T/π high-pass/low-pass topology, the improved hybrid topology reduces the number of inductors from 3 to 2. Besides, the values of inductors in high-pass T/π-network satisfy

$$L_\pi / L_T = 2\cos^2(\Delta\Phi/4) \tag{1}$$

where the L_T and L_π are inductors in T/π-network, and $\Delta\Phi$ is the desired phase shift. For phase shift like 45°/90°, the ratio of L_π to L_T is more than 1.7, so the improved hybrid topology exhibits lower loss and smaller size compared to the all-π topology.

It must be noted that the limited isolation of SPDT switches has triggered C_p and L_p of the 45° bit section to be resonant over the band of interest. Owing to different device parameters, there is no resonance in 180°/90° bits. To avoid unwanted resonance, an enhanced SPDT switch with two shunt transistors (M_1) is applied in the 45° bit part as shown in Fig. 1. The simulation results of the 45° bit section with/without shunt transistors are shown in Fig. 2.

The low-pass/resonator PS is suitable for 22.5°/11.25° bits, where wide BW and compact size are required. However, SPDT switches inside the PS reduce BW from 88% to 54% [12]. Hence, an improved low-pass/resonator PS is used in our 11.25° and 22.5° bits, which realizes BW expansion by incorporating the switches into the phase-shifting circuit. The low-pass T-network and series *LC* resonator share two series inductors as shown in Fig. 1. Such PS achieves miniaturization by minimizing the number of inductors and transistors. There are only two transistors and two inductors in this structure while there are eight transistors and ten inductors in [12]. The size of the 22.5° bit is 0.1 mm^2, which is ten times smaller than [12] with a half operating frequency of [12].

For the 5.625° bit, a switch/inductor topology containing only one transistor and one small inductor is usually adopted for small size [10]. However, such topology exhibits large phase error (PE) and amplitude imbalance. To reduce these kinds of impact, a switched L/C structure is adopted for 5.625° in this letter as shown in Fig. 1. This structure achieves size reduction by embedding the switches into the phase-shifting circuit, which has the advantages of a high-pass/low-pass PS as the phase shift circuit can be equivalent to a first-order filter. Also, this structure has one series transistor in both operating states, so an equal amplitude response can be achieved by appropriately adjusting the transistor size. Simulation results show that the proposed PS achieves a greatly reduced PE of ±0.4°, compared with the PE of normal switch/inductor PS of ±2.4°.

III. Implementation and Measurements

All phase-shifting units above are designed with an S_{11}/S_{22} of lower than −17 dB during the electromagnetic (EM) simulation stage, ensuring minimal interaction between each unit and the S_{11}/S_{22} of the entire PS less than −10 dB. Since the PS is formed by cascading 6 bits in series, and the performance of each bit could be degraded by loading of adjacent bits, so the cascading order of phase-shifting units is optimized. Owing to a low return loss (RL) indicates less signal reflection, bits with worse RL are shielded by bits with better RL to reduce the influence of adjacent bits. RL consideration is an important basis for cascade optimization. The dedicated optimal order used in this design is shown in Fig. 3. The FET peripheries of each unit are optimized for better performance and compact area. The information of the corresponding FET sizes can be found in Fig. 1.

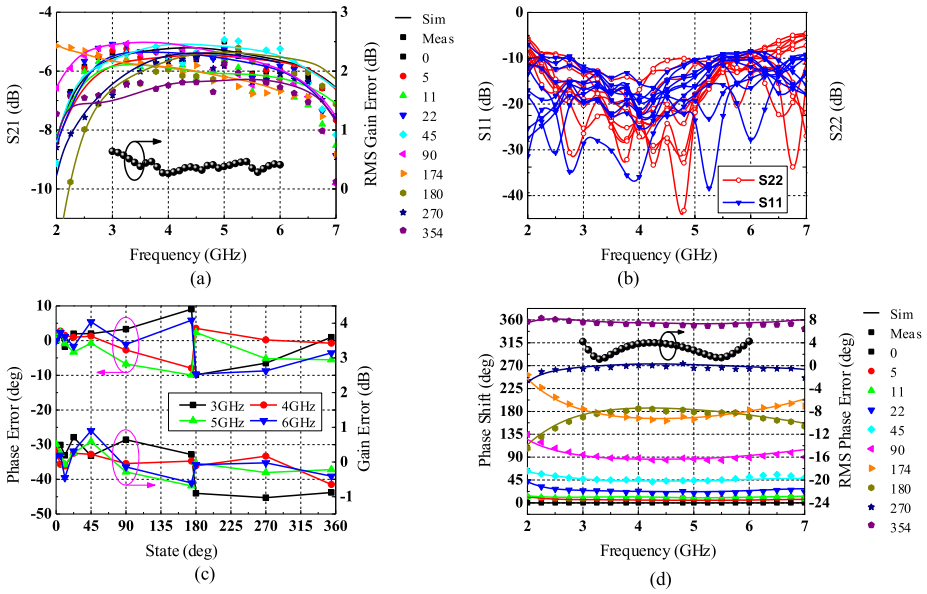


Fig. 4. Measured results of major state. (a) Measured and simulated S_{21}, and rms gain error. (b) Measured S_{11} and S_{22}. (c) Measured PE and gain error versus phase state. (d) Measured and simulated phase shift and simulated rms PE results.

TABLE II
SUMMARY OF SIMILAR BAND MMIC PSS

Ref	BW (GHz)	Bits	BW (%)	IL (dB)	RMSPE	Process	Area (mm^2)
[2]	2.3-3.8	4	42	<4.7	<3°	0.4-μm GaAs	2.6
[3]	S band	5	10	<6.7	<2.8°	0.5-μm GaAs	1.63
[4]	8-12	5	40	<14	<6.4°	0.5-μm GaN	23.5
[6] *	5-6	6	18	<6.2	<10°	0.18-μm SOI	1.03
[7] *	2.5-3.2	6	25	13**	<2°	0.18-μm CMOS	3.1***
This work	**3-6**	**6**	**66.7**	**<6.7**	**<4°**	**0.5-μm GaAs**	**1.8**

* Si process, for reference only ** .Without amplification *** The area is estimated from the die photo, with the amplifier excluded.

The proposed 3–6 GHz 6-bit PS was fabricated in 0.5-μm GaAs pHEMT technology with a substrate thickness of 100-μm. The process provides metal–insulator–metal (MIM) capacitors with capacitance density of 600 pF/mm^2 and three layers of metal (1.1-μm-thick metal 1, 2.1-μm-thick metal 2, 4-μm-thick metal 3), which helps to reduce chip size and loss of passive components. The MIM capacitors used in this PS have a range from 0.2 to 9 pF; and the inductors have a range from 0.2 to 3.5 nH, with a Q value of 15–24. Fig. 3 shows the chip photo of the proposed PS with a compact chip size of 0.9 mm $\times$ 2 mm including pads.

For the measurement, the chip was wire bonded to an evaluation board as shown on the right side of Fig. 3. The diameter and length of the gold bonding wire are 25 μm and 300 μm, respectively. The microstrip 50 Ω line is built on the Rogers 4350 substrate with a dielectric constant of 3.55 and a dissipation factor of 0.004. The S-parameters were measured using the Keysight N9918A FieldFox analyzer.

Fig. 4 depicts the measured results of the PS over the frequency range of 3–6 GHz. The IL of the evaluation board is 0.76–1.2 dB over the range of 3–6 GHz, and the PS exhibits an IL of 5–6.7 dB after subtracting the board loss, with an rms gain error of 0.3–0.6 dB over 3–6 GHz as shown in Fig. 4(a). The measured and simulated IL results agree well, with a fluctuation of about 0.4 dB. Fig. 4(b) depicts the measured S_{22} is better than -10 dB over 3–6 GHz, and S_{11} is better than -8 dB. The measured PE is $-10°$ to 9° over the operating frequency range and the maximum gain error was -1 dB at 3 GHz, as illustrated in Fig. 4(c). The phase shift measurement results of major states are demonstrated in Fig. 4(d). The PS has a simulated rms PE less than 4°. This work exhibits a measured input P1dB around 29 dBm benefited from the high linearity switching FETs.

Table II compares this work with similar operating band PSs in literature. Generally, the proposed PS has a high phase-resolution with compact chip size, and its IL, rms PE, and operation BW are better than that of the previously reported works. The PS is significantly smaller in size and has 20.7% more extension in BW compared with the 0.15-μm GaAs pHEMT based PS product design [5], making MMIC PSs practical for broadband applications.

IV. CONCLUSION

In this letter, a 3–6 GHz wideband and compact 6-bit PS using 0.5-μm GaAs pHEMT process is presented. Modified high-pass/low-pass topology and low-pass/resonator topology is applied in different bits for broadband and compact design. The PS achieves an rms PE of less than 4°, and an IL less than 6.7 dB in 66.7% BW with a compact chip size of 1.8 mm^2, demonstrating the effectiveness of the modified topologies and methodologies used in this work.

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