E-Band Reflection-Type Phase Shifter with Uniform Insertion Loss

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***Abstract* — An 81-86 GHz reflection-type phase shifter (RTPS) with uniform insertion-loss (IL) for E-Band phased array transceivers is reported in this paper. The RTPS is based on two loaded couplers and implemented in 120 nm SiGe BiCMOS process. The 6-bit phase shifter achieves >195° phase variation across the upper E-band with less than ±0.5 dB insertion loss variation over all phase states. The measured IL at 84 GHz is 7.4±0.15 dB. Measured RMS gain and phase error are less than 0.2 dB and 2°, respectively, across 81–86 GHz. The IC occupies area of 350 x 700 μm².**

***Index Terms* — Reflection type phase shifter; E-band; phased array;**

I. Introduction

SiGe BiCMOS technologies have been demonstrated to be excellent candidates for the design of E-band and W-Band phased arrays thanks to their high breakdown voltage, HBT's cutoff frequencies and technology maturity. [1], [2]. Passive phase shifters are often preferred in such systems, as they consume zero DC and linear. The most prevalent topologies are switched LC branches [2], capacitive-loaded transmission line [3], and RTPS [4], [5]. Since many BiCMOS technologies are built on 130 nm CMOS node, the first two topologies suffer from high IL variation and low phase resolution, stemming from the high insertion loss associated with CMOS switches. The RTPS typically incorporates only two varactors and hence exhibit lower IL, but requires a non-linear, process sensitive control to maintain a uniform IL [1], which complicates the calibration procedure.

In this paper, we present a RTPS operating at E-Band that is based on two couplers rather than only one. This technique was proposed in [6] as a bandwidth extension method and is utilized here and in [7] to minimize IL variation by means of pole-zero placement. It enables the RTPS to attain low IL variation in the presence of a low-Q varactor while achieving more than 195^0 phase shift.

II. Circuit Design

The phase shifter was designed and fabricated in Global-Foundries 120 nm 5 metal levels SiGe8XP technology. The thin oxide MOS varactors achieves simulated C_{max}/C_{min} of ~3 for a bare (unwired) device.

The standard RTPS topology comprises a hybrid coupler, loaded by reactive network. Fig. 1 depicts such C-L-C load with resistance parasitic associated with each component.

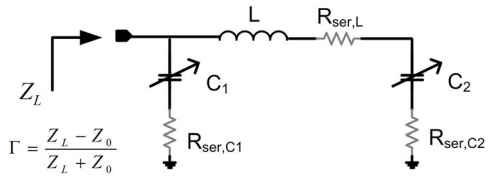

Fig. 1. C-L-C network load

Eq. 1 gives the input impedance of a lossless C-L-C network which has complex pole and zero at $_p$ and $_z$, respectively:

$$Z_L = \frac{1 + s^2 LC_2}{s(C_1 + C_2) + s^3 LC_1 C_2} \quad (1)$$

$$\omega_P = \frac{1}{\sqrt{LC_1 \parallel C_2}} \quad \omega_Z = \frac{1}{\sqrt{LC_2}}$$

The phase at the output of the RTPS and its IL can be expressed as [3]:

$$IL_{dB} = |\Gamma| + 2IL_{coupler} = 20\log\left(\frac{(R_L - Z_0)^2 + X_L^2}{(R_L + Z_0)^2 + X_L^2}\right) + 2IL_{coupler} \quad (2)$$

$$\theta = -90^0 - \angle\Gamma$$

where is load reflection coefficient, X_L and R_L are the load's imaginary and real parts, respectively, and Z_0 is the system's characteristic impedance. At lower frequencies, the components' high-Q values result in near ideal resonances (series-R_L<<Z_0, parallel-R_L>>Z_0) and therefore $|\Gamma|$~1 despite the variations in R_L near resonances (Eq .2). That gives a degree of freedom in the pole and zero placement, which can be chosen in-band or close to maximize the phase shift contributed by both. However, at E-Band, the varactor's Q is ~5 and R_L is typically limited to 10-100 , which turns $|\Gamma|$ highly dependent in the value of R_L across different settings of the varactor near resonances. In this design, C_1 and C_2 are chosen to be small enough (C_1=44-132 fF, C_2=22-63 fF) to push up $_p$ out of band and minimize the effect of its variable location on IL variation. Similarly, the position of $_z$ is set below 75 GHz for all varactor's settings. The main drawback of this approach is the significant decrease of phase tuning range, and to achieve 180^0 phase shift two cascaded loaded couplers are required. Fig. 2 depicts the reflection coefficient of two loads optimized for 180^0 and 90^0 degrees phase shift with minimal IL variation at 83 GHz.

Note that the later (used in this work) aligns with the constant -3.5 dB IL circle almost perfectly (within 0.2 dB), while the first deviates from the constant -7 dB IL circle by 2 dB. Therefore, the IL is not doubled by using the proposed technique and the only penalty is the IL of a second coupler (0.7 dB) and its additional silicon area.

Fig. 3(a) shows the schematic of the phase shifter. Lange couplers (3 dB) are used, as they more compact than hybrid couplers and exhibit wider bandwidth. The 4 traces microstrip is realized at the top metal over M1 ground plane, as shown in Fig 3(b). The simulated IL is 0.7 dB, while return loss and isolation are better than 19 dB. Simulated phase difference between direct and coupled ports is 90±0.5^0 at E-Band.

The couplers are loaded with identical C-L-C loads designed to provide total phase shift of at least 180° (90^0 for each stage) with minimal IL variation over different phase settings. All the varactors are controlled by a single linear 6-bit voltage DAC, but biased with a different reference voltage, optimized uniform IL. The loads' inductors are implemented as 70 Ω microstrip lines with simulated Q of 15 at E-Band.

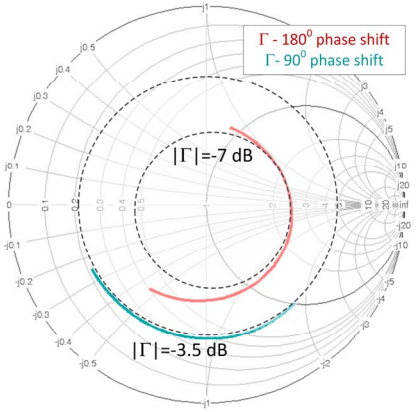

Fig. 2. Simulated Γ of loads designed for 180^0 phase shift (single coupler) and 90^0 phase shift (two couplers)

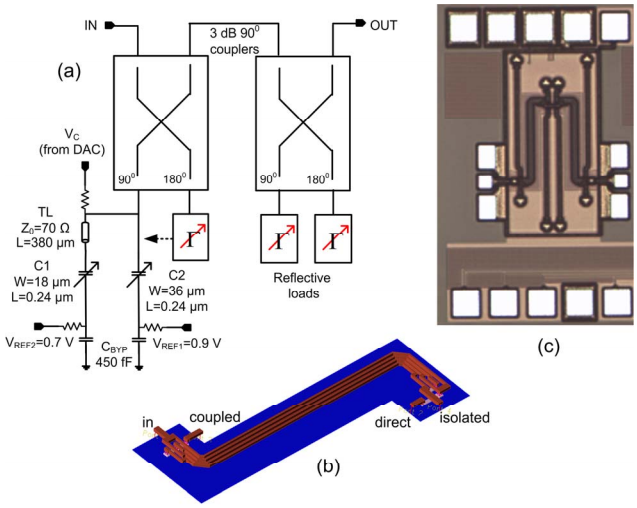

Fig. 3. Phase shifter schematic (a), coupler layout (b) and chip photograph (c)

III. Measured Results

The IC, shown in Fig. 3(c) occupies area of 350×700 µm^2, excluding pads, and was measured with on-wafer probing using Keysight PNA-X N9030A. Fig. 4(a) shows the measured insertion loss for all 64 phase states. The IL is better than 8.4 dB at 81-86 GHz and at 84 GHz is 7.4±0.15 dB across all phase states. The input (and output –due to symmetry) matching exhibit a very wideband behavior with S11<-12 dB at 75-100 GHz, as can be seen in Fig. 4(b).

Fig 5(a) presents the phase shift achieved at different frequencies vs. the DAC bit settings. Across the frequency of interest, the minimum phase shift is 197^0 (at 86 GHz). The IL vs. phase shift in different frequencies is plotted in Fig. 5(b), which shows that the IL variation across phase states is below ±0.5 dB.

The measured and simulated IL at -40,25 and 85^0 (DAC bit word=0) are presented in Fig. 5(c). Amplitude variation is 1 dB IL across temperature extremes, with good agreement with simulation. The phase variation across temperature in each phase state is lower than ±2.5 degrees.

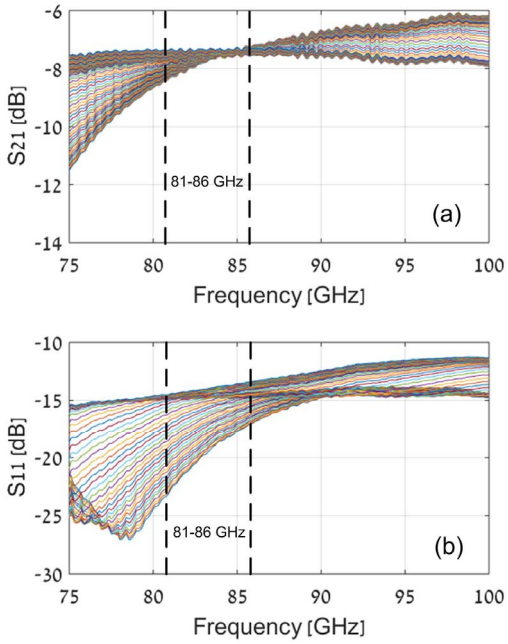

Fig. 4. Measured IL (a) and input return loss (b) for all 64 DAC states

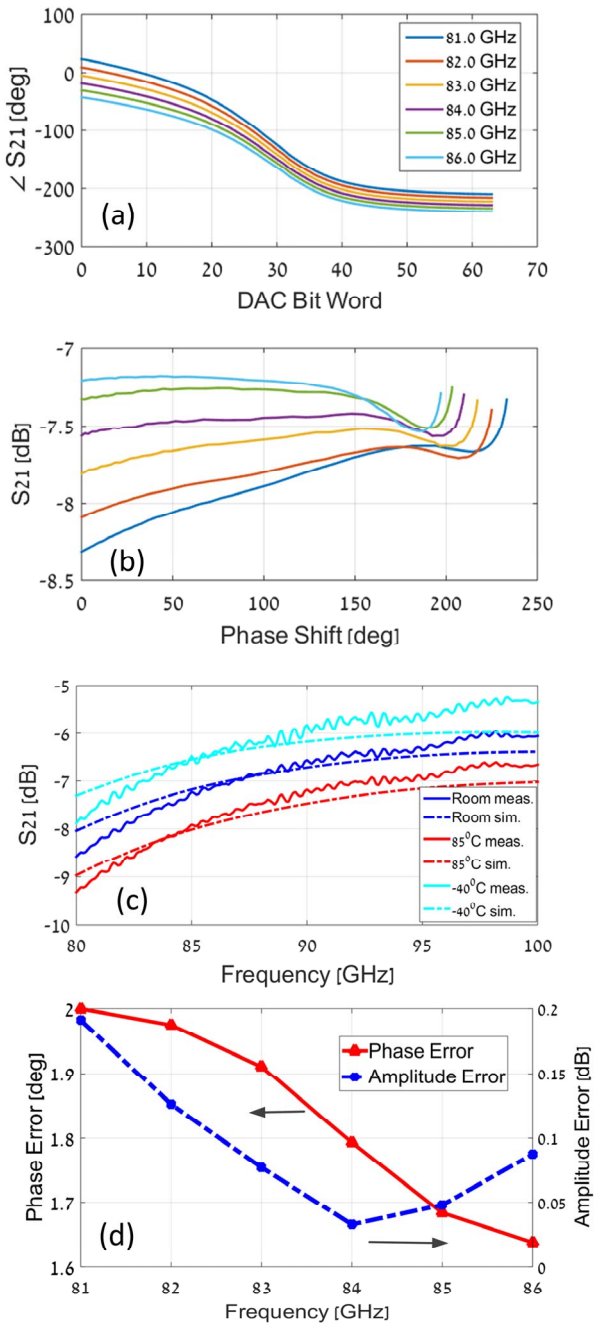

Fig. 5. Measured phase vs. DAC bit (a), IL vs. phase shift (b), IL variation in temperature (c) and phase/amplitude errors (d)

RMS phase and amplitude error are shown in Fig. 5(d) for a 6-bit operation. In the intended phased array system, a calibration is performed in 6 frequency points (81,82...86 GHz) and for each frequency a set of DAC settings optimized for lowest phase error is stored in the memory. The optimized DAC settings result in RMS phase error better than 2^0, while the RMS amplitude error is better than 0.2 dB at 81-86 GHz. IIP3 was measured using two Analog devices frequency sources (HMC-T2240) at 100 MHz relative offset which were multiplied by SAGE frequency triplers to E-Band and summed by magic-Tee. The IM3 products and fundamental E-Band tones were measured using Keysight N9030A PXA equipped with W-Band harmonic mixer. Fig. 6 shows the worst-case Input-referred IP3 over all phase states, which is >12 dBm across temperature and frequency. Table I summaries the results with comparison to previously reported Si passive mm-wave phase shifters.

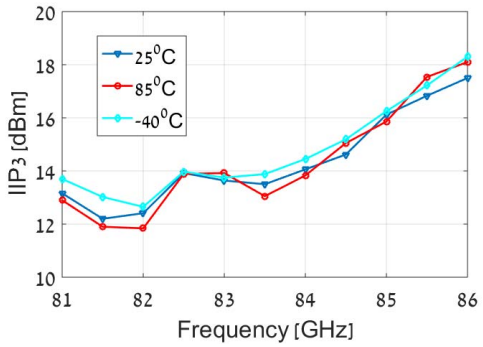

Fig. 6. Measured IIP3 over frequency and temperature

IV. Conclusion

In this paper we propose a new design approach for reflection-type phase shifter, based on resonance free reflective loads, optimized for a flat IL response and two cascaded couplers to span >180^0 phase shift. The fabricated E-Band RTPS demonstrates state of the art performance in terms of IL variation while achieving >195^0 phase shift tuning range.

TABLE I.
RESULTS SUMMARY AND COMPARISON

	This work	[2]	[4]	[3]	[5]
Process	SiGe 0.12µm	SiGe 0.12µm	CMOS 65nm	CMOS 32nm	SiGe 0.12µm
Type	RTPS	LP delay	RTPS	Loaded T-Line	RTPS
Frequency (GHz)	81-86	76- 84	55-65	55-65	57-64
Min phase shift (^{0})	197	349	180	165	180
Max IL (dB) 25^{0}C	8.3	22.3	8.3	8.7	7.5
Max IL var. (dB)	1	4.3	3.3	2	3.3
RMS phase error [^{0}]	2	7.2	-	3.2	4
Chip size (mm^2)	0.245	0.135	0.031	0.1	0.18

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