A Fully Integrated X-Band Multifunction Core Chip in 0.25 μm GaN HEMT Technology

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***Abstract*—This paper presents the design of a wide band and highly compact multifuction core chip Monolithic Microwave Integrated Circuit (MMIC) using WIN Semiconductor's 0.25 μm Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) process design kit for the first time. The core chip is designed for use in GaN based X-band Transmit Receive (T/R) modules of Active Electronically Scanned Antenna (AESA) radars. Core chip operates in the frequency band of 9 to 11 GHz and provides multiple functions that includes 6-bit Digital Phase Shifter (DPS) for beam steering, 6-bit Digital Step Attenuator (DSA) for amplitude correction, interstage Low Noise Amplifiers (LNAs) and Single Pole Double Throw (SPDT) T/R switches. The Electromagnetic Simulation (EM) shows that MMIC exhibits a transmit gain of 19 dB and receive gain of 17 dB at 9 GHz. Transmit path Root Mean Square (RMS) gain and phase error are better than 1.15 dB and 4.7° respectively. The RMS attenuation and insertion phase shift error are also better than 0.75 dB and 7.25° respectively. The receive path has a maximum noise figure of 5.8 dB at 11 GHz. This core chip occupies die area of 15.36 mm^2 (6.65 mm x 2.31 mm). The compact size, low receiver noise figure and high transmit/receive gain makes this core chip suitable for integration in T/R modules of X-band AESA radars.**

***Index Terms*—GaN, T/R module, core-chip, digital phase shifter, digital attenuator, SPDT switch**

I. Introduction

T/R modules for AESA applications are required to fulfill certain performance requirements due to their operation under challenging electrical and environmental conditions. These requirements include efficiency, accurate phase and amplitude control, low noise figure, excellent thermal conductivity and most important is miniaturization through high integration [1]. To be competitive in the market and in order to meet these performance requirements, the selection of an appropriate fabrication technology and the level of integration that can be achieved are the key elements for cost reduction. Fig. 1 shows a simplified block diagram of a modern TRM. For core chip design and fabrication, Gallium Arsenide (GaAs) and Silicon Germanium (SiGe) based technologies are dominating the marker so far. Several GaAs based highly integrated multifunction core chips have been reported [2]–[7]. These core chips are only able to handle limited input/output power of up to 20 dBm with high receiver noise figure. In past few years, the performance evaluation of SiGe technology over microwave frequencies makes it a promising candidate for low power mixed signal functionalities. Although SiGe is not able to outperform GaAs in terms of RF performance but,

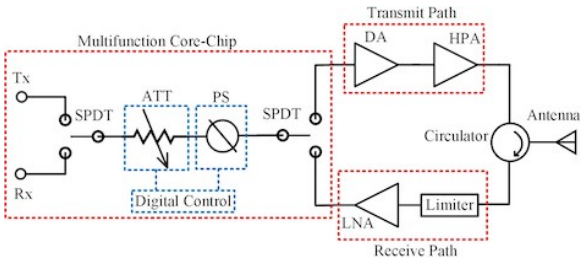

Fig. 1. Simplified block diagram of a T/R Module

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higher integration can be achieved that eventually leads to reduced size and cost [8]–[12]. Additionally, high yield and integration with low fabrication cost can also be achieved by using silicon based complementary metal oxide semiconductor (CMOS) process with the expense of high insertion loss, low power and poor noise figure [13]–[15].

Recent technological advancements in the high electron mobility wide band gap semiconductors like Gallium Nitride (GaN) enables it to operate on higher frequencies (∼300 GHz), improved power densities (∼8 W/mm^2), high temperature (∼600° C) and voltages of up to 100 V [16]. High power density of GaN would result in 5 times greater power production as compared to conventional GaAs based process in same mm^2 die area. This leads to the 1/4 times reduced size requirement for producing same amount of power. This would eventually results in overall size and cost reduction of entire system. High frequency operation and greater power density enable one to design wide band MMICs with low noise figure [17]. GaN technology has replaced GaAs process for designing high power MMICs for front end of T/R module that includes driver amplifiers (DAs), high power amplifiers (HPAs), roboust low noise amplifiers in receive path and SPDT T/R switches [18]. The design and fabrication of back end mixed signal MMICs for phase and amplitude control using GaN technology would result in compact size, less number of interconnects, lower integration cost, improved heat transfer to the back of MMIC and simple routing of T/R module.

This work contributes to the design and development of a GaN based X-band T/R module for airborne AESA platform. A multifunction core chip with 6-bit phase and amplitude control is designed in Keysight Advance Design System (ADS). The designed core chip occupies a die area of 15.36 mm^2 without pads which is comparable to most of GaAs based chips. The multifunction chip contains single 6-bit digital phase shifter and attenuator, six interstage amplifiers and three SPDT T/R switches. It shows good RF performance with a receive path noise figure better than 5.8 dB.

II. Multifunction Core Chip Design Process

The block diagram of GaN multifunction core chip is shown in Fig. 2. Common leg architecture is used in order to have a trade off between noise figure and power handling capability [4]. This topology results in a compact design as compared to separate Tx/Rx path architecture because the digital phase shifter and step attenuator are shared in both transmit and receive operation. The designed core chip contains one 6-bit digital phase shifter for beam steering, one 6-bit digital step attenuator for amplitude correction through antenna pattern tailoring, six interstage amplifiers having same RF characteristics and three SPDT T/R switches. Both transmit and receive path contain four amplifiers. In common leg path, one amplifier is placed before digital phase shifter to compensate its negative gain slope and one amplifier is also placed after digital step attenuator for further loss compensation. No amplifier is placed between digital phase shifter and attenuator in order to maintain phase linearity and to get minimum

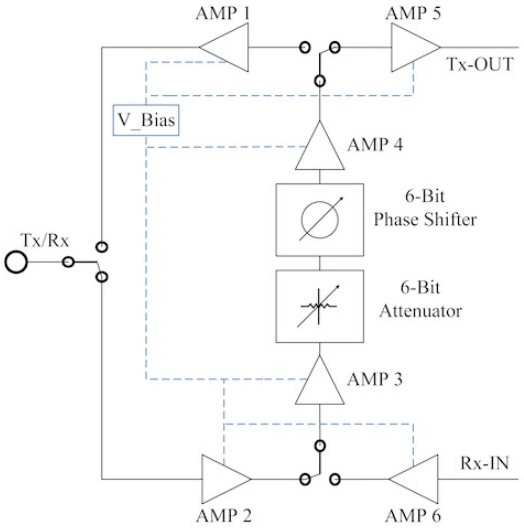

Fig. 2. Block diagram of GaN multifunction core chip with 6-bit phase and amplitude control

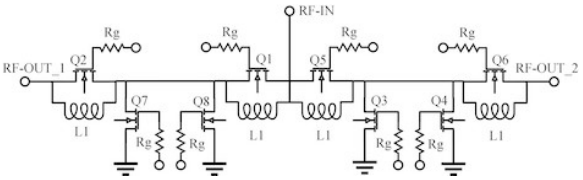

Fig. 3. Schematic of GaN SPDT switch.

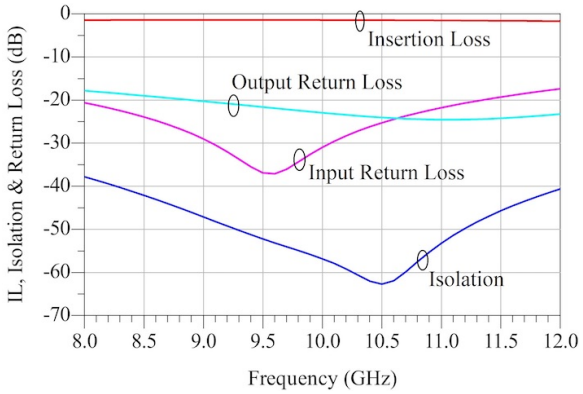

Fig. 4. Simulated insertion loss, isolation and input/output return loss of GaN SPDT switch.

insertion phase change in both transmit and receive mode of operation. High isolation SPDT T/R switches are designed for signal control and operating mode selection. Each component of the core chip is separately designed and optimized in order to have compact size and good RF performance. The operating voltages for inter stage low noise amplifiers are selected to be +12 V and for ON/OFF control of SPDT switches, 0 V and -24 V are used respectively. The design of individual components of core chip is described in the following sections.

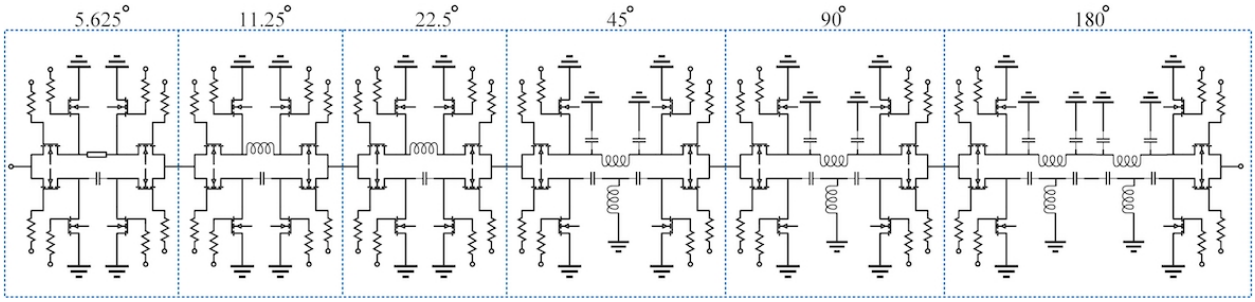

Fig. 5. Schematic design of GaN 6-bit phase shifter.

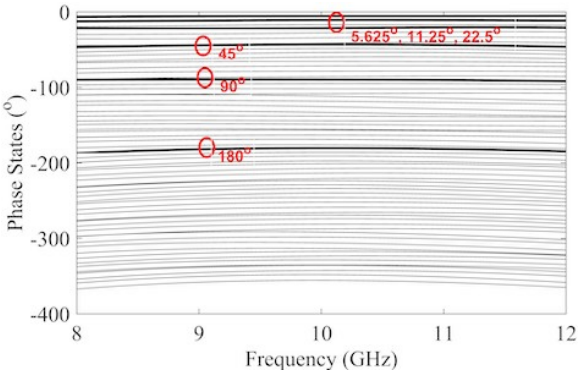

Fig. 6. Simulated 64 phase states of GaN 6-bit phase shifter (thick black lines are major phase states).

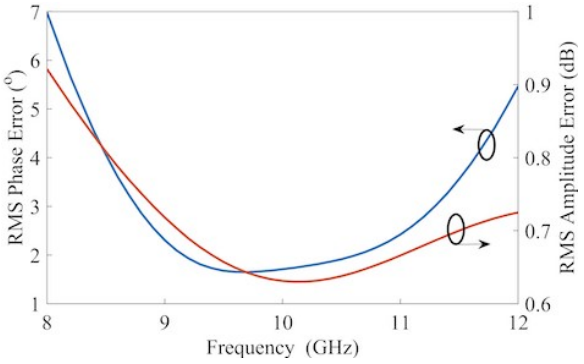

Fig. 7. RMS phase and amplitude error of GaN 6-bit phase shifter.

A. SPDT Switch

A reflective, high power and high isolation SPDT switch is designed using the design considerations presented in [19]. The schematic design of proposed switch is shown in Fig. 3. A gate control voltage of 0 V and -24 V is used to switch from on-state and off-state operation. Simulation results in Fig. 4 shows that it exhibits an insertion loss less than -1.7 dB and isolation better than -38 dB over the entire X-band. The input and output match for a 50 Ω impedance are better than -18 dB from 8 to 12 GHz.

B. 6-Bit Digital Phase Shifter

A 6-bit digital phase shifter is designed having 360° coverage with incremental step of 5.625°. Hybrid high pass low pass filter topology [20] is used to design 45°, 90° and 180° bit sections for compact size and wide band operation. To design lower bits, a single inductor and capacitor is used for reference and phase shift path respectively. The schematic diagram of digital phase shifter is shown in Fig. 5. EM simulation results show that it exhibits an insertion loss of -13±1.7 dB, RMS phase error less than 4° and P1 dB compression point of 36 dBm. Fig. 6 and Fig. 7 shows all 64 phase states and RMS phase and amplitude error respectively.

C. Interstage Low Noise Amplifier

To compensate insertion losses associated with SPDT switches, DPS and DSA, a single stage low noise interstage amplifier is designed using source degeneration topology shown in Fig. 8 to get a flat gain and good input/output match over the entire X-band. The source degeneration is achieved by connecting a microstrip line between source of HEMT and and ground via, whereas the LC network is used for input matching and a resistive network is used to match the output to a 50 Ω impedance. A 116 Ω mesa resistance designed using sheet of high resistivity having dimensions of 100 x 25 μm is used for output matching as well as to decrease the over all noise figure of amplifier. The amplifier is biased to operate in the linear region by using a shunt inductor at gate which also a part of input matching network. A single drain bias voltage of 12 V is used to drive the amplifier. The small signal gain and noise figure of designed amplifier are shown in Fig. 9. It can be seen that it provides a maximum gain of 9.8 dB at 9 GHz and minimum gain of 8 dB at 12 GHz. The noise figure is also less than 1.6 dB over the entire X-band.

D. 6-Bit Digital Step Attenuator

A 6-bit digital step attenuator having maximum attenuation range of 31.5 dB with LSB of 0.5 dB is designed for amplitude correction and antenna pattern tailoring. A combination of switched T and pi topology with inductive phase compensation is used to have low insertion phase change [21]. One major advantage of using switched pi/T attenuator topology is the requirement of less number of switches. Less number of transistors also results in lower die area. To design 0.5 and 1 dB attenuator bits, a combination of single transistor and single resistor is used. The value of resistance is varied to obtain desired attenuation level. Switched path topology is used to

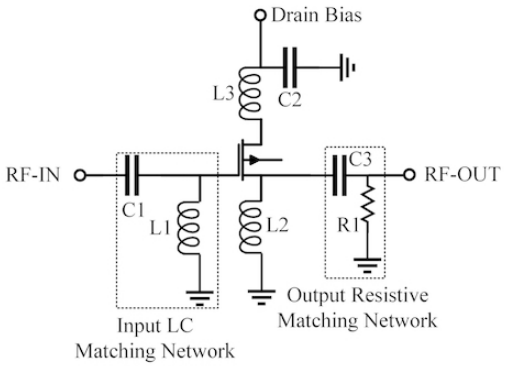

Fig. 8. Schematic design of GaN inter-stage amplifier.

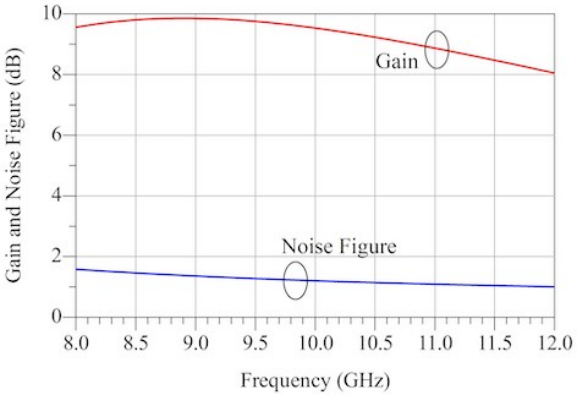

Fig. 9. Small signal gain and noise figure of GaN inter-stage amplifier.

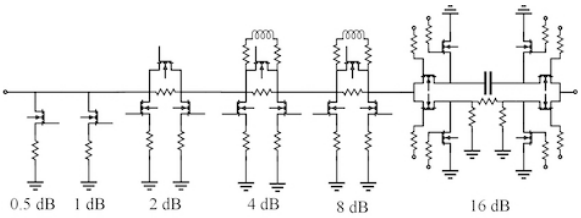

Fig. 10. Schematic design of GaN 6-bit digital step attenuator.

design 16 dB attenuator bit. A pi resistive network is chosen for attenuation path and a single capacitor is inserted in the reference path to compensate the phase change of attenuation network. Two SPDT switches are connected on both sides of the 16 dB bit to switch from reference to attenuation path. After design and optimization of each attenuator bit, all bits are cascaded together to have a 6 bit digital attenuator. Bit order can change the overall RF performance of designed MMIC, therefore, those bits having poor return losses are cascaded in the middle. The optimum bit order is shown in schematic design of 6-bit digital step attenuator in Fig. 10.

The simulation result of all 64-attenuation states is shown in Fig. 11. It shows a broadband response of designed attenuator. Fig. 12 shows the RMS attenuation error which is less than 0.27 dB from 8 to 12 GHz.

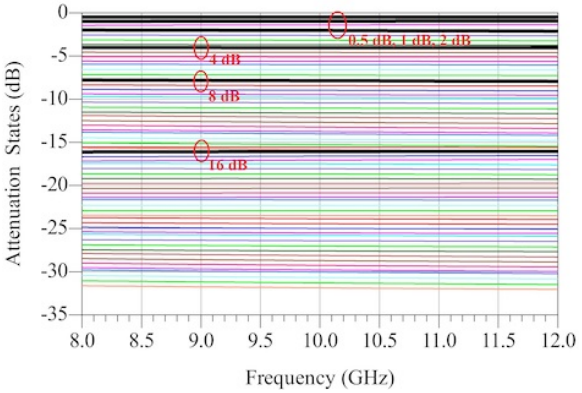

Fig. 11. Simulated all 64-states of GaN digital step attenuator (thick black lines are major attenuation states).

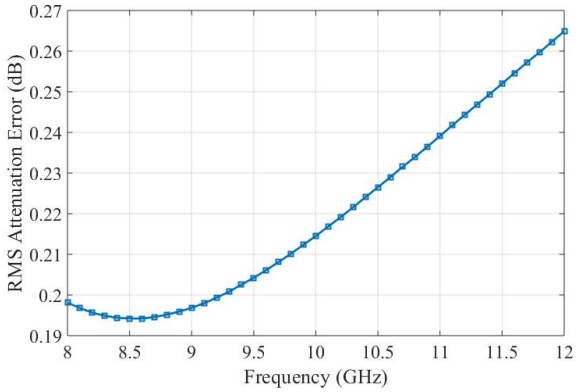

Fig. 12. RMS attenuation error of GaN digital step attenuator.

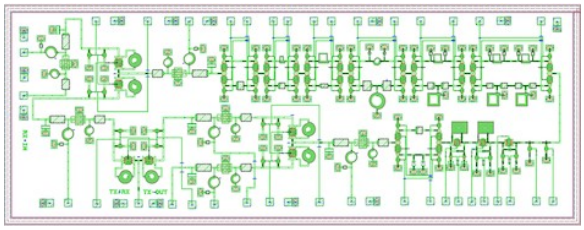

Fig. 13. Layout of multifunction core-chip (chip size: 6.65 mm x 2.31 mm)

III. Simulation Results and Discussion

After design and optimization of each subsystem explained in previous section, they are connected to from a multifunction core chip as shown in Fig 2. The GaN MFC is simulated in Keysight Advanced Design System (ADS) software and its overall layout is shown in Fig. 13. It occupies a chip area 15.36 mm^2.

The gain and phase shift characteristics of all 64 phase states of core-chip relative to the reference state versus frequency during transmit mode of operation is shown in Fig. 14 and 15 respectively. The attenuator is set to be in the reference state of operation. It can be seen that the gain varies from 19 dB to 12 dB from 9 to 11 GHz. The variation in gain is due

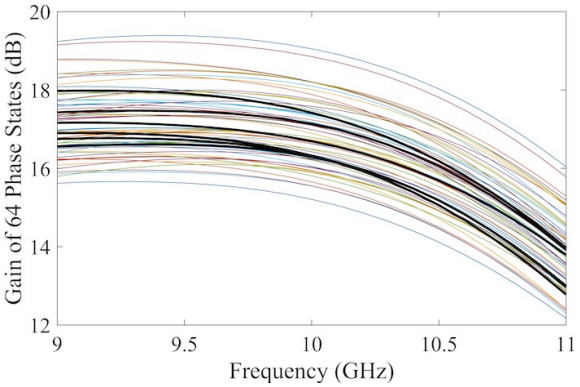

Fig. 14. Gain of 64-phase states during Tx state operation (thick black lines are major phase states)

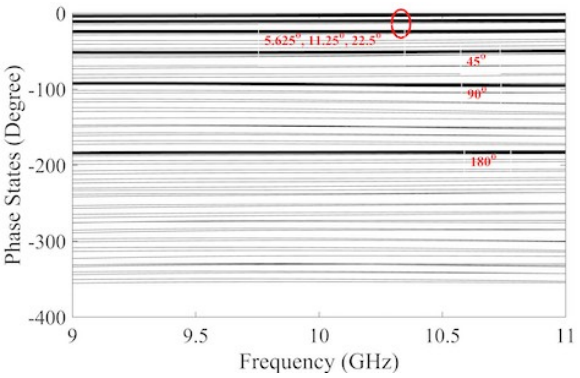

Fig. 15. Phase shift characteristics 64-phase states during Tx state operation (thick black lines are major phase states)

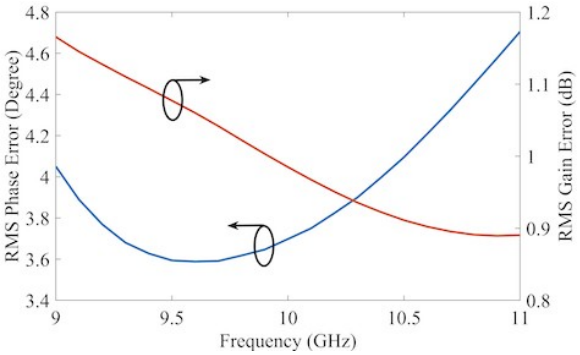

Fig. 16. RMS gain and phase error of transmit path during reference state operation of attenuator

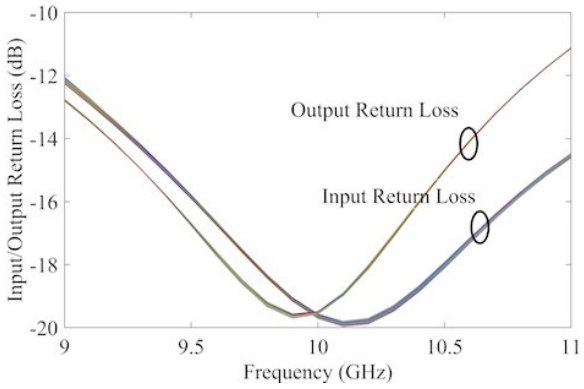

Fig. 17. Input and output return losses of 64-phase states during reference state operation of attenuator

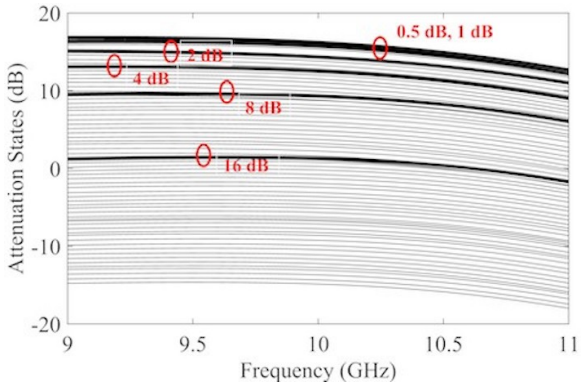

Fig. 18. Attenuation characteristics of 64-attenuation states during reference state operation of phase shifter (thick black lines are major attenuation states)

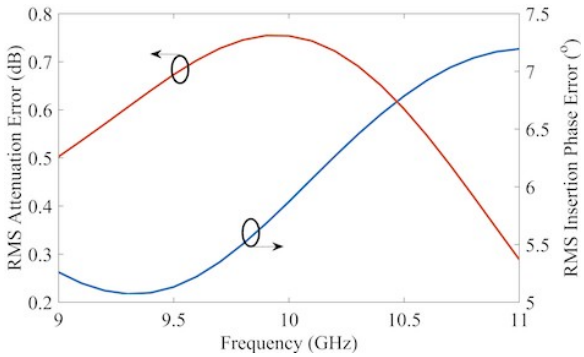

Fig. 19. RMS attenuation and insertion phase error of 64-attenuation states during reference state operation of phase shifter

to the variation of insertion loss of different phase states of digital phase shifter. Fig. 15 shows the wide band flat phase shift characteristics of MFC from 9 to 11 GHz.

The RMS gain and phase error of transmit path during reference state operation of attenuator is shown in Fig. 16. It can be seen that the RMS gain and phase error is less than 1.2 dB and 4.7° respectively from 9 to 11 GHz. The input and output return losses off all 64-phase states during reference state operation of attenuator is shown in Fig. 17 and are better than -11 dB.

The attenuation characteristics in transmit path of core-chip during reference state operation of digital phase shifter is shown in Fig. 18. It can be seen that the gain varies from 18 dB to -14 dB covering the range of 6-bit attenuator (0 to 31.5 dB). The RMS attenuation and insertion phase error of 64-attenuation states during reference state operation of digital phase shifter is shown in Fig. 19 and are less than 0.75 dB and 7.25° respectively from 9 to 11 GHz.

To analyze the receiver gain and noise figure, the major phase states are simulated during reference state operation of

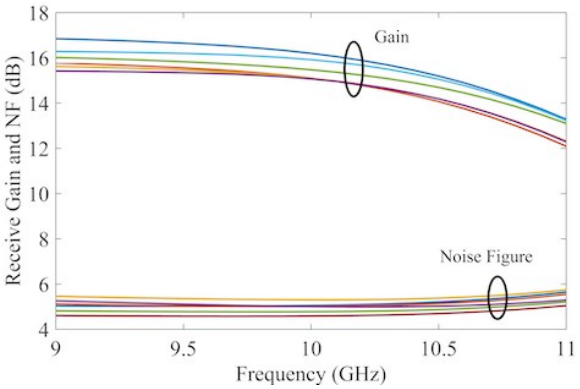

Fig. 20. Receiver gain and noise figure of major phase states during reference state operation of digital attenuator

TABLE I
PERFORMANCE COMPARISON WITH AVAILABLE SIMULATION RESULTS

Ref.	This Work	[15]	[11]	[3]
Process	GaN	CMOS	SiGe	GaAs
Frequency (GHz)	9-11	7-12	9-10	6-18
Tx Gain (dB)	<20	<20	<25	<15
Rx Gain (dB)	<17	<20	<20	-
Rx NF (dB)	<6	-	<8	<20
Return Loss (dB)	<-10	<-5	<-5	<-10
Chip Size (mm^2)	15.36	12.76	4.9	20

attenuator and are shown in Fig. 20. It can be seen that the gain varies from 17 to 12 dB and noise figure varies from 5.8 to 4.8 dB from 9 to 11 GHz. A performance comparison of designed GaN multifunction chip with available simulation results of recently published work is presented in Table I.

IV. CONCLUSION

A Gallium Nitride (GaN) based multi-function chip is designed using a 0.25 μm GaN HEMT process design kit. The designed chip shows good RF performance exhibiting a transmit gain of 19 dB and receive gain of 17 dB at 9 GHz. Transmit path root mean square (RMS) gain and phase error are better than 1.15 dB and 4.7° respectively during reference state operation of DSA. The RMS attenuation and insertion phase shift error during reference state operation of DPS are also better than 0.75 dB and 7.25° respectively. The receive path has a maximum noise figure of 5.8 dB at 11 GHz. This MFC occupies die area of 15.36 mm^2 (6.65 mm x 2.31 mm). The compact size, low receiver noise figure and high transmit/receive gain makes this MFC suitable for integration in T/R modules of X-band AESA radars.

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