AlGaN/GaN-based Variable Gain Amplifiers for W-band Operation

S. Diebold[1], D. Müller[1], D. Schwantuschke[2], S. Wagner[2], R. Quay[2], T. Zwick[1], I. Kallfass[3]

[1] *Karlsruhe Institute of Technology (KIT), Institut für Hochfrequenztechnik und Elektronik (IHE)*
Kaiserstrasse 12, D-76131 Karlsruhe, Germany

[2] *Fraunhofer Institute for Applied Solid-State Physics (IAF)*
Tullastrasse 72, D-79108 Freiburg, Germany

[3] *University of Stuttgart, Institute of Robust Power Semiconductor Systems*
Pfaffenwaldring 47,D-70569 Stuttgart, Germany

***Abstract*— In this paper three versions of a variable gain amplifier (VGA) monolithic millimetre-wave integrated circuit (MMIC) are presented. They make use of 100 nm gate-length AlGaN/GaN-based high electron mobility transistors (HEMTs) grown on SiC. The MMICs operate in the 75 to 110 GHz band and have a centre-frequency of 94 GHz. Different phase compensation techniques, which are proposed in literature are applied and their suitability for millimetre-wave (mmW) frequency application is evaluated. We propose an additional phase compensation means leading to our best VGA version providing a gain tuning range from -17.2 to 7 dB with a phase variation of only 12.6 °.**

***Index Terms*— gain control, Gallium nitride, GaN, HEMTs, MMICs, phase control, phase shifters, Power amplifiers, variable gain amplifier, VGA**

I. Introduction

A VGA is a device that serves to modify the amplification of a signal by means of a control voltage. They are key components in antenna beam-forming and automatic gain control (AGC) systems. In beam-forming applications the VGA phase has to be insensitive to the steering of the amplifier gain to avoid a deformation of the beam. AGC systems are employed in receiver and transmitter front-ends, too, where they provide a stable RF power level for linearity improvement. In this scenario a constant phase versus gain is not crucial. Both applications demand for low cost and small size solutions. Moreover, the VGA must be capable to handle high RF power levels. It has to be robust in terms of maximum (peak) input power, provide a high power linearity and secure operation even under the influence of interferer or reflected signals.

In the frequency band around 94 GHz, these requirements only are fulfilled by MMICs exploiting AlGaN/GaN-based HEMTs. They have a linearity potential due to the high output power handling capability of the wide band-gap material, superior to their MMIC competitors like GaAs-based or Si-based transistors.

To compare different published VGAs, the gain-variation per phase-variation value ($GPV = {}^{\Delta gain}/_{\Delta phase}$) can be used. In literature silicon-based [1]–[4] and III-V compound semiconductor based [5] VGAs can be found. Their *GPV* ranges from 1.1 dB/deg [2] to 4.1 dB/deg [5]. A *GPV* of 4 and 3.3 dB/deg was presented in [1] where a low noise amplifier (LNA)/VGA in SiGe HBT technology operating at 5.2 to 5.9 GHz was presented providing a gain control range of 12 and 20 dB with a phase variation of 2 and 6 deg, respectively. An other LNA/VGA in SiGe HBT technology at 60 GHz with a phase variation of 12 deg and a gain variation of 13 dB was presented in [2] resulting in a *GPV* of 1.1 dB/deg. A LNA/VGA in CMOS technology at 60 GHz with a gain control range of 13 dB and a phase variation of 5 deg causing a *GPV* of 2.6 dB/deg was published by [3]. In [4] a 71 GHz to 76 GHz CMOS VGA with 30 dB gain control range and 4 dBm saturated output power was presented. They did not publish the phase dependency of signal. A D-Band (110 to 170 GHz) VGA realised in 100 nm GaAs mHEMT technology with 16.4 dB gain variation and less than 4 deg phase variation at 161 GHz leading to a *GPV* of 4.1 dB/deg has been published by [5].

In this paper three versions of a AlGaN/GaN-based variable gain amplifier are presented, which offer the superior power robustness and linearity compared to other technology candidates such as GaAs or Si based transistors. They make use of the phase compensation technique presented in [1] with small variations to analyse the suitability of the proposed techniques for mmW application. The means are evaluated by measurements of the fabricated MMICs. Moreover, we found an additional circuit parameter allowing for further minimisation of the phase variation. The here presented VGA versions provide a gain tuning range from 16.7 dB to 30.3 dB with an associated parasitic phase variation ranging from 10.8 deg to 23.5 deg. The *GPV* ranges from 1.29 dB/deg to 1.92 dB/deg.

II. Technology Description

Due to the high electron mobility $\mu_e = 1.800\,\mathrm{cm^2/(V\,s)}$, the large saturation velocity $v_{\mathrm{sat}} = 2.7 \times 10^7$ cm/s and the high breakdown voltage $V = 3 \times 10^6$ V/cm of GaN HEMTs, they are perfect candidates for high speed and high power operation. The VGAs presented in this paper make use of 100 nm gate-length AlGaN/GaN HEMTs grown on SiC. With a drain-source voltage of 7 V they provide a current gain cut-off frequency f_T higher than 80 GHz and a maximum frequency of oscillation $f_{\max}$ of about 200 GHz in small gate-width devices.

The employed HEMTs yield a maximum drain current of greater than 1.6 A/mm and a maximum DC transconductance g_m of greater than 550 mS/mm. More detailed information on this technology can be found in [6].

III. Circuit Topology and Measurement

A cascode formed by a transistor in common-source (CS) configuration and a second in common-gate (CG) configuration is the key component of the phase compensation technique presented in [1]. There the authors analysed the phase change occurring during tuning of the CS and CG stage amplification. They found that the stages can be tailored to provide opposite phase behaviour versus gain leading to a stable phase by superposition of both stages. In addition to that, the parasitic phase variation can be reduced by adding an inductive feedback at the source of the CS stage, i.e. by source degeneration. It can be further reduced by optimisation of the capacitance located at the gate connection of the CG stage. Usually this value is chosen to be high to provide a RF short at the gate. By choosing a smaller value they have shown that the phase variation significantly can be reduced.

In this paper we add another degree of freedom to minimise the phase unwanted phase variation occurring while tuning the VGA gain. In a cascode the CS and CG stages are connected by a short piece of transmission line having strong influence on amplifier bandwidth, matching and stability. This line is utilised to minimise the phase variation even further.

Fig. 1 shows the schematic representation, which in principle is common to all three VGA versions. The employed transistors all make use of four finger devices with a single finger width of 45 µm, which adds up to a total gate-width of 180 µm. To reduce the chip-size of the VGAs, capacitors to ground (C_p) are located at the input and output T-junctions. The matching is done by these capacitors, the parallel transmission lines (L_{pi}, L_{po}) and the series transmission lines (L_{si}, L_{so}). The biasing of the CS gate and the CG drain is done via L_{pi} and L_{po}, too. To provide DC-decoupling, series capacitors (C_s) are located at the input and output of the circuit. A resistive voltage divider (R_1, R_2) is employed to simplify the system and only one control voltage V_{ctrl} is required to steer the VGA gain. The negative voltage V_{neg} can be set individually for each device to compensate for technology variations.

A fixed negative voltage V_{neg} of -34 V and a fixed drain voltage V_d of 15 V are applied to the VGAs. The control voltage V_{ctrl} is varied from 6 to 9.5 V for all VGA versions. The given voltages result in a CS stage gate voltage of -1.2 V and 1.6 V for $V_{neg} = 6$ V and $V_{neg} = 9.5$ V, respectively. These are typical values for the employed GaN technology. The variation of V_{ctrl} leads to a variation of the VGA gain and phase, which is shown for all VGA versions in Fig. 2. This figure shows phase versus gain performance at a frequency of 94 GHz and is determined by S-parameter measurements.

It can be seen that the first version has the smallest phase variance due to the source inductance. This is in accordance to the theory proposed in [1]. The gain can be swept from -13.6 to 3.1 dB leading to a phase variation of only 10.8°. The chip

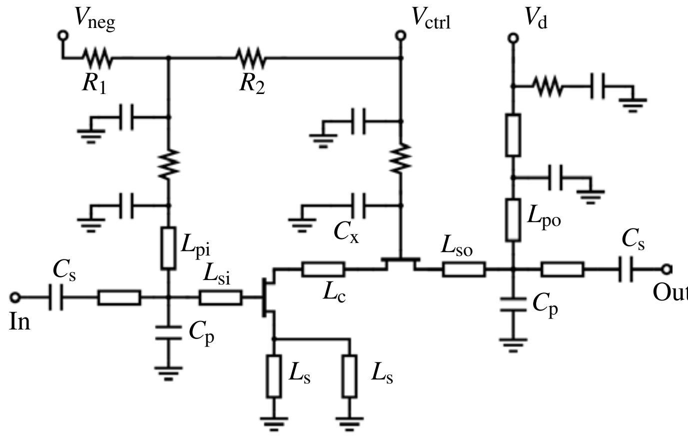


Fig. 1: Schematic representation of all VGA versions.

photograph of the first VGA is shown in Fig. 3a. The chip size is $1.25 \times 1.0\,\mu m^2$. The VGA makes use of a symmetric source degeneration set up by the shorted transmission lines L_s with a length of 110 µm each. The line L_c connecting the CS and CG stage has a length of 60 µm and the two capacitors C_x have a value of 120 fF.

The downside of the source inductance lines L_s is the limited gain control range being significantly higher with the second version not using source degeneration. There a gain variation from -17.2 to 7 dB with a phase variation of 12.6° can be obtained. In the second VGA version, which is shown in Fig. 3b the source degeneration lines L_s are omitted to provide a higher gain. The chip measures $1.25 \times 1.0\,\mu m^2$, too. The CG-capacitors C_x have a value of 530 fF and the line L_c has a length of 60 µm.

An even higher control range can be realised with the third version with a gain control span from -22.3 to 8 dB and an associated phase variation of 23.5°. Here the connection line L_c is omitted to form a dual-gate transistor topology being popular

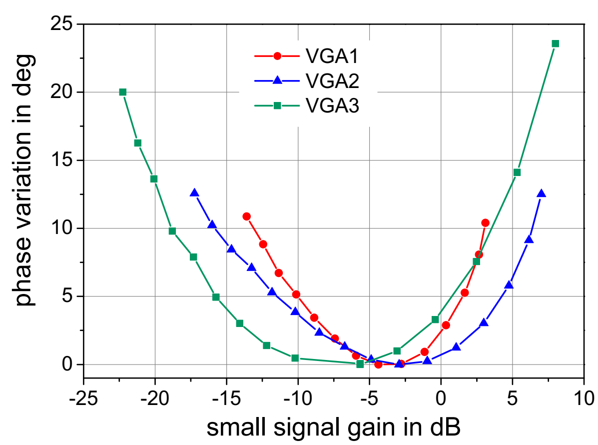


Fig. 2: Phase variation versus VGA gain for the three VGA versions. The plot shows the VGA performance at 94 GHz.

with GaN power amplifier design. With this configuration the CS and CG transistor fingers are parallel, which can be seen in the chip photograph shown in Fig. 3c. The chip has a size of $1.0 \times 1.0\,\mu m^2$.

In the W-Band (75 to 110 GHz) the scattering parameters are measured and shown in Fig. 4 for $V_{ctrl} = 6.0$ V and $V_{ctrl} = 9.5$ V resulting in maximum and minimum VGA gain, respectively. It can be seen that the second version has with about 7 dB at 94 GHz the highest gain and a very large bandwidth when biased for maximum gain. This makes this version favourable over the first and third version having either much lower gain or lower bandwidth. When biased for minimum gain, the third version has with about -20 dB at 94 GHz the lowest gain making this the version with the highest gain control range. The first and second version have a similar minimum gain value of about -15 dB. As can be seen in e.g. [5], the down-side of steering the VGA gain with voltage divider voltages is the average matching quality changing with the control voltage. For all versions the matching is better than 3 dB and goes up to 20 dB.

The analysis of Figs. 2 and 4 shows that VGA version two provides the best performance. Its *GPV* is 1.92 dB/deg compared to 1.55 dB/deg and 1.29 dB/deg for the first and third stage, respectively. The source degeneration used in the first version leads to the smallest phase variation but results in a limited gain control capability. The second version, which does not make use of source degeneration has a higher gain tuning range with still a very good phase stability. This proves that source degeneration is not advantageous in high mmW frequency range VGA design. In this paper we have shown that the transmission line L_c has a strong influence on the phase stability. This transmission line is omitted in the third version resulting in a high phase variation. To the authors' knowledge this behaviour has not been shown yet in VGA designs.

The large-signal behaviour of the VGAs is presented in Fig. 5 and is investigated by one-tone measurements. For measurement a signal generator drives a commercially available source module, which drives an in-house designed, developed and packaged power amplifier. This amplifier is followed by a variable attenuator and a RF-probe, succeeded by the output RF probe, a 10 dB attenuator and a diode-based power meter. The 10 dB attenuator is used to secure linear operation of the power meter. The input power is calibrated to the probe-tip plane and can be changed by appropriate setting of the variable attenuator.

The linear input power $P_{in,-1dB}$, i.e. the input power where the output signal is compressed by 1 dB is of great importance to guarantee linear operation of e.g. communication systems. The $P_{in,-1dB}$ of the first, second and third VGA version are +10 dBm, +7 dBm and +4 dBm, respectively, when the VGAs are biased for maximum gain, i.e. with $V_{ctrl} = 6$ V. The associated linear output power values $P_{out,-1dB}$ are 11.8, 11.6 and 10.7 dBm, respectively. The measurement results are shown in Fig. 5. Again, the second version is favourable over the first and third version since it provides high gain, high linearity and a high output power. The saturated output power of the VGAs could not be measured with the given measurement equipment due to its limited power to drive the amplifiers. With an input power value of $P_{in} = 15$ dBm the output power of the first, second and third VGA version is 13.5, 14 and 15.1 dBm, respectively. The $P_{in,-1dB}$, $P_{out,-1dB}$ and P_{out} values shown in this paragraph demonstrate the superior power handling capability of GaN devices in the mmW frequency range.

IV. Conclusion

Three AlGaN/GaN-based 100 nm gate-length HEMT VGA versions have been presented and different phase compensation techniques presented in literature have been investigated. We supplemented the existing methods by showing that the transmission line connecting the CS and CG stage in a cascode device has a strong influence on phase stability. Our best VGA version makes use of the most suitable combination of phase stabilisation means and provides a large gain control range of 24.2 dB with a high maximum gain of 7 dB and small phase variation of 12.6 °. By measuring the large-signal performance of the VGAs at 94 GHz, the superior power handling capability of GaN-based devices has been demonstrated by showing a linear behaviour up to an input power of 7 dBm and an linear output power of 11.6 dBm.

V. Acknowledgement

We express our gratitude to our colleagues in the IAF technology department for their excellent contributions during epitaxial growth and wafer processing. This work partly was supported by the Deutsche Forschungsgesellschaft.

References

[1] F. Ellinger, U. Jorges, U. Mayer, and R. Eickhoff, "Analysis and Compensation of Phase Variations Versus Gain in Amplifiers Verified by SiGe HBT Cascode RFIC," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 1885 –1894, aug. 2009.

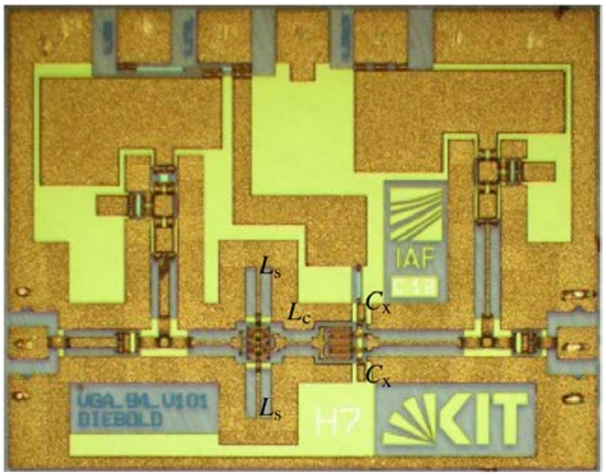
[2] S. Hauptmann, F. Ellinger, F. Korndoerfer, and C. Scheytt, "V-band variable gain amplifier applying efficient design methodology with scalable transmission lines," *IET Circuits, Devices & Systems*, vol. 4, no. 1, pp. 24 –29, jan. 2010.

[3] Y. Kim and Y. Kwon, "A 60 GHz Cascode Variable-Gain Low-Noise Amplifier With Phase Compensation in a 0.13 um CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 7, pp. 372 –374, july 2012.

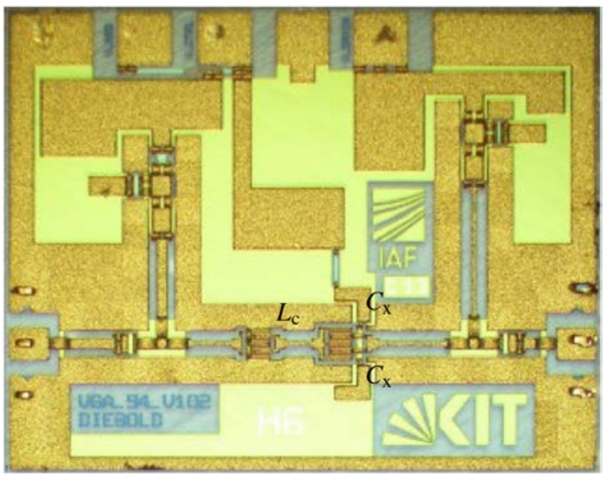
[4] C.-C. Kuo, Z.-M. Tsai, J.-H. Tsai, and H. Wang, "A 71 - 76 GHz CMOS variable gain amplifier using current steering technique," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, apr. 2008, pp. 609 –612.

[5] D. Müller, S. Diebold, H. Massler, A. Tessmann, A. Leuther, T. Zwick, and I. Kallfass, "A D-band phase compensated variable gain amplifier," in *Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*, sept. 2012, pp. 1 –3.

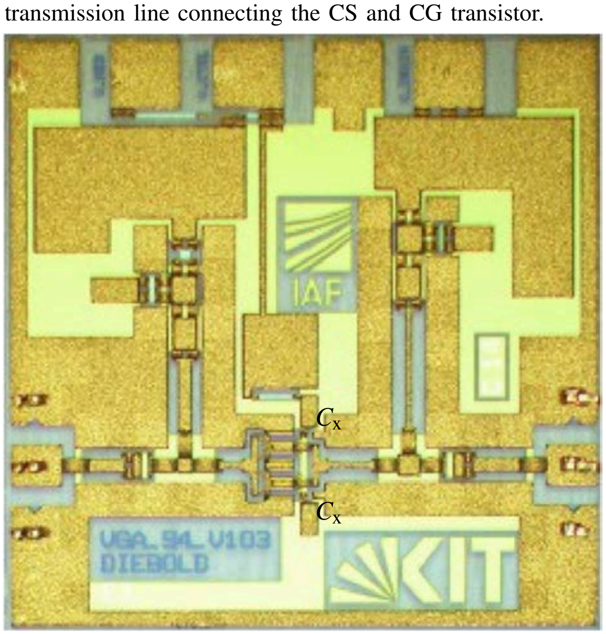
[6] C. Haupt, S. Maroldt, R. Quay, W. Pletschen, A. Leuther, and O. Ambacher, "Development of a high transconductance GaN MMIC technology for millimeter wave applications," *physica status solidi (c)*, vol. 8, no. 2, pp. 297–299, feb. 2011.



(a) Version 1 with source degeneration and a long transmission line connecting the CS and CG transistor.



(b) Version 2 without source degeneration but with a long transmission line connecting the CS and CG transistor.



(c) Version 3 using a dual-gate transistor without source degeneration

Fig. 3: Chip photographs of all three VGA versions. The elements, which are typical for each version are labelled in the photograph.

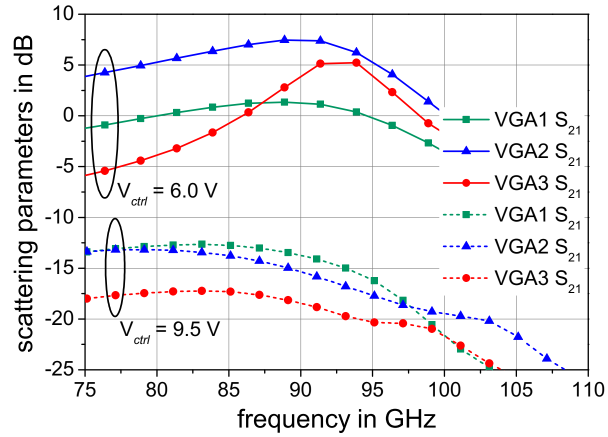


Fig. 4: Small signal gain for all VGA versions biased with $V_{\text{ctrl}} = 6.0\,\text{V}$ and $V_{\text{ctrl}} = 9.5\,\text{V}$ for maximum and minimum gain, respectively.

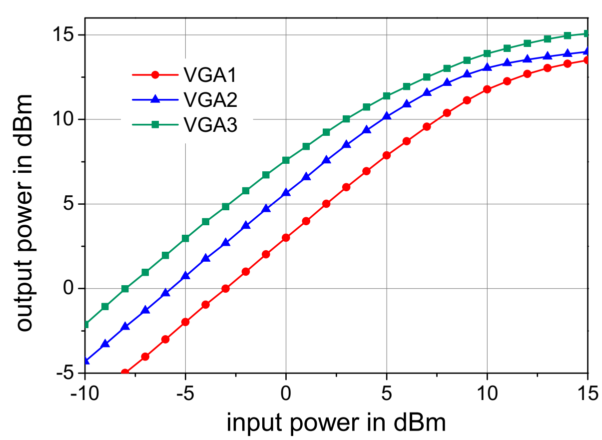


Fig. 5: Output power versus input power for all VGA versions at 94 GHz and $V_{\text{ctrl}} = 6\,\text{V}$.