Chapter 4
Differential Amplifiers

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教材：模拟CMOS集成电路设计

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4.1 single-ended and differential operation

- 单端信号：参考电位为一固定电位（ fixed potential）,通常为地。
- 差动信号：两个节点电位之差。该两节点直流电位相对某一固定电位（即共模电平）大小相等，交变小信号电压方向相反。并要求该两节点与固定电位（=交流地）节点的阻抗相等（电路对称）。

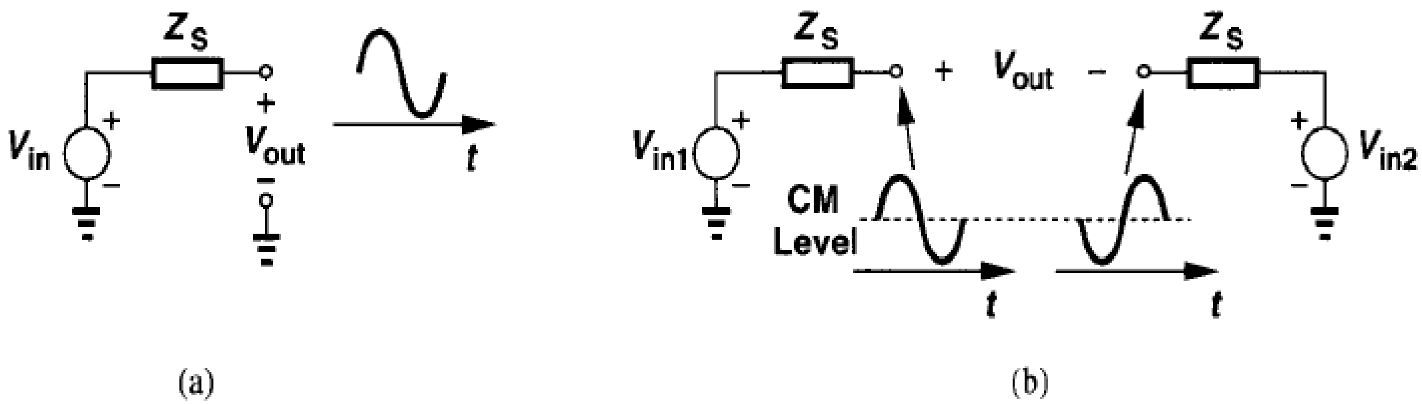


Figure 4.1 (a) Single-ended and (b) differential signals.

差动（或称差分）工作方式的优点

（1）对共模噪声（外部环境电磁噪声，如电源和地噪声）的强抑制能力;

共模噪声：2输入端或输出端相同大小的噪声

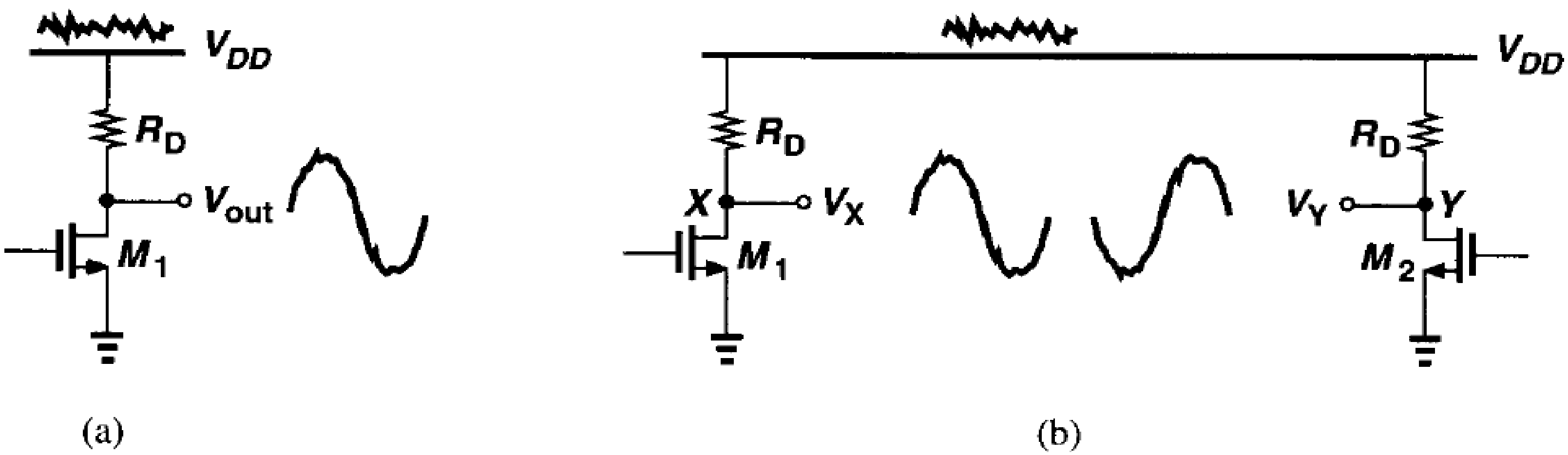


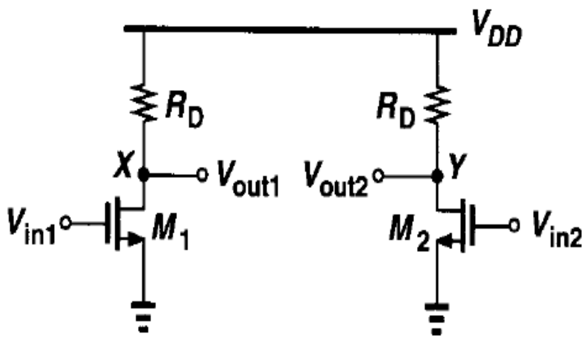
Figure 4.3 Effect of supply noise on (a) a single-ended circuit, (b) a differential circuit.

两单端放大器组成差动对

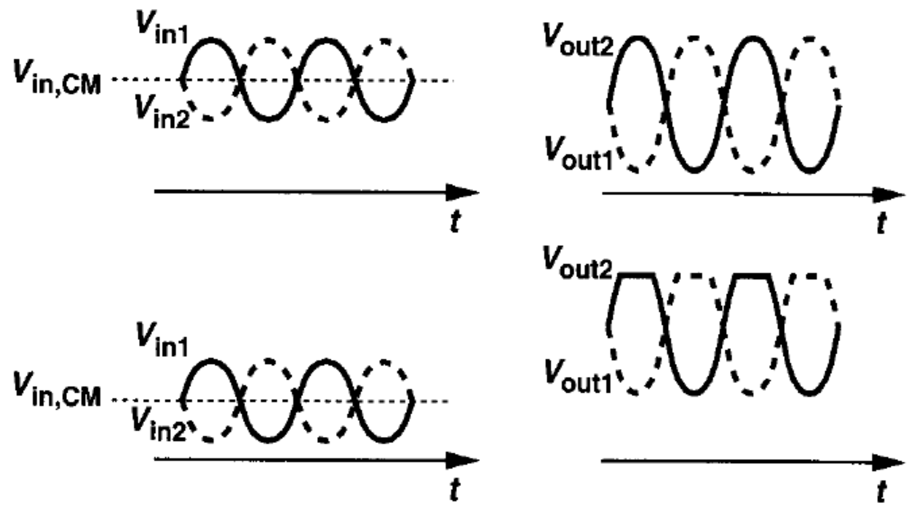
（2）Vout=VX-VY,增大了输出电压摆幅

（3）提高线性范围（差分）

两单端放大器组成差动对的缺点



(a)



(b)

Figure 4.5 (a) Simple differential circuit, (b) illustration of sensitivity to the input common-mode level.

输入共模电平影响输出摆幅。

共模CM电平：
2输入端或输出端的相同电平。

4.2 Basic Differential Pair

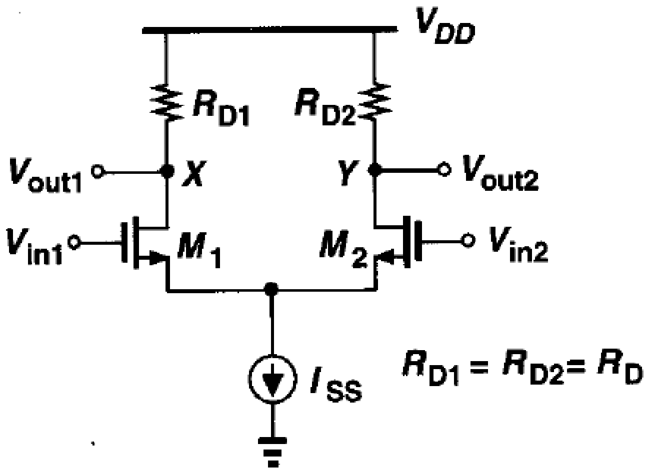


Figure 4.6 Basic differential pair.

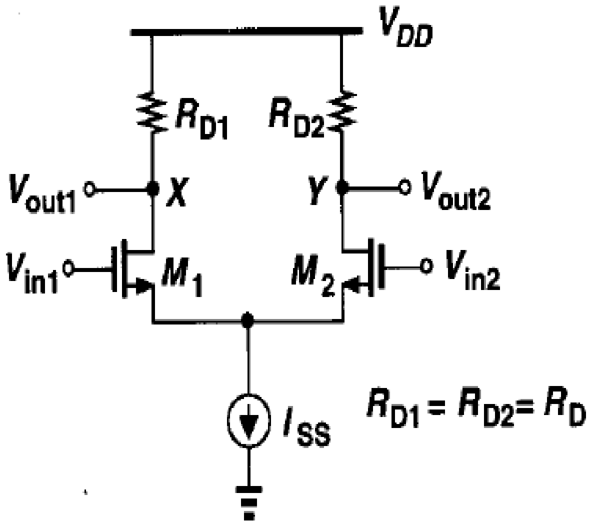
$I_{SS}=I_{D1}+I_{D2}$不依赖V_{iCM}。

设M1、M2非截止区，尾电流源M3处于饱和区，

当$V_{in1}=V_{in2}$（大信号）时,

输出共模电平$V_{oCM}=V_{DD}-R_D*I_{SS}/2$

4.2.1 Qualitative analysis



$I_{SS}=I_{D1}+I_{D2}$

当$V_{in1}=V_{in2}$,
$V_{out1}= V_{out2}= V_{DD}-R_D*I_{SS}/2$

- V_{in1} 电位很低时 M1 截止， $I_{D2}=I_{SS}$, $V_{out1}=V_{DD}$, $V_{out2}= V_{DD}-R_D*I_{SS}$,

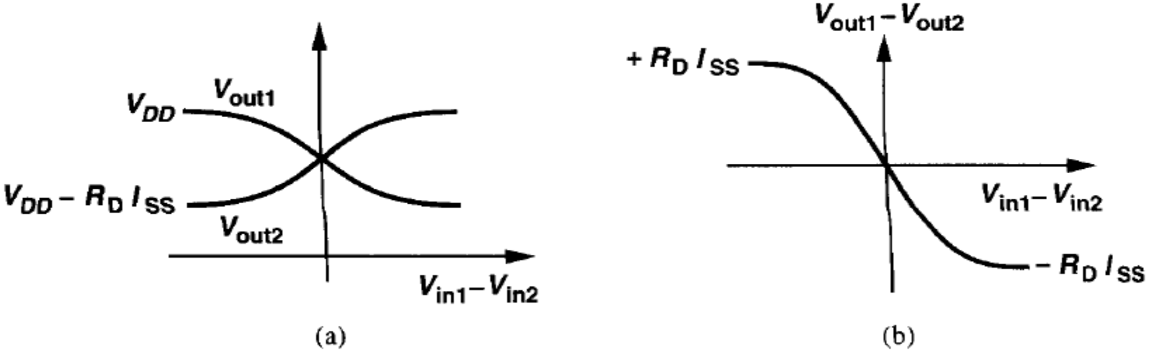


Figure 4.7 Input-output characteristics of a differential pair.

具有尾电流源的差动对重要特性：

（1）输出端的最大和最小电平是完全确定的（V_{DD}和 $V_{DD}-R_D*I_{SS}$），与共模输入电平无关（尾电流源的作用）,前提：负载不是电流源，尾电流源在饱和区

（2）小信号增益当$V_{in1}=V_{in2}$时（平衡状态equilibrium）最大，且随|Vin1-Vin2|的增大而减小，即有非线性

common-mode （CM）behavior

Vin1=Vin2=VinCM, Vout1=Vout2

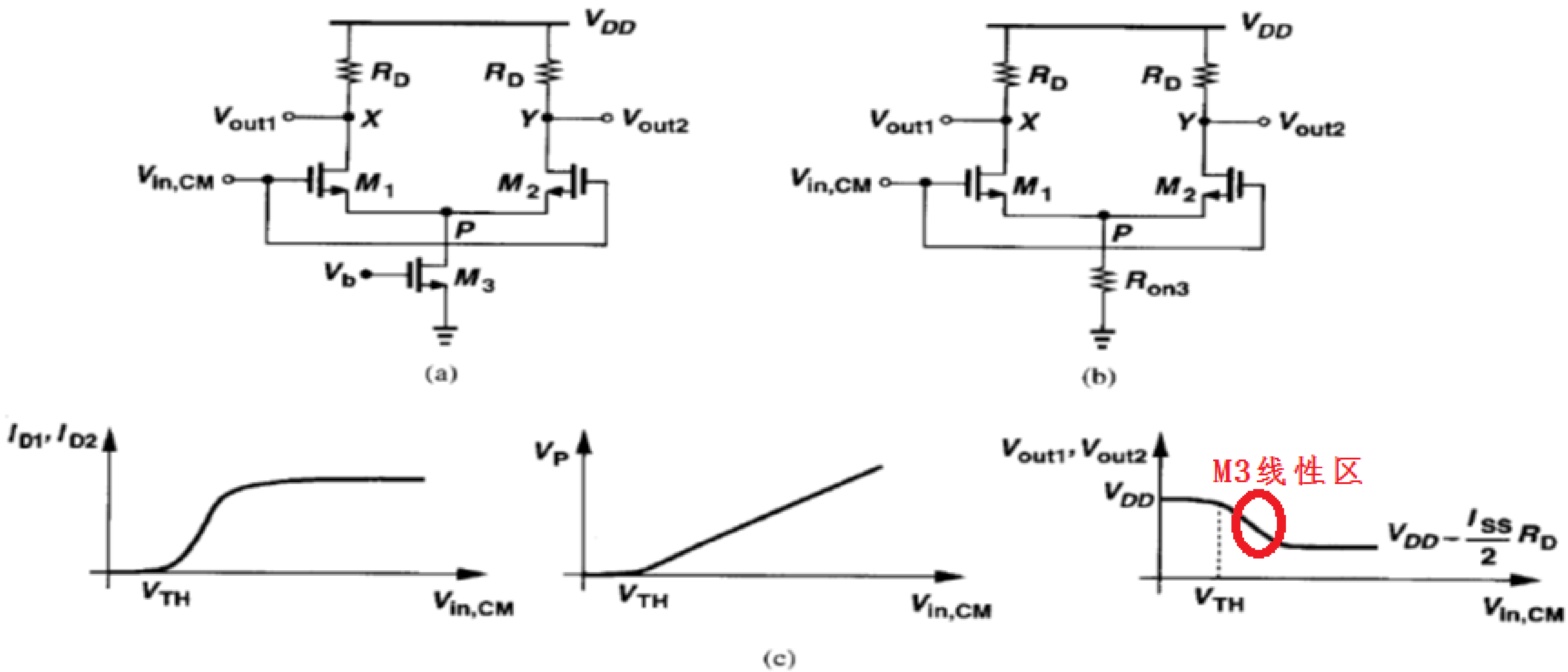
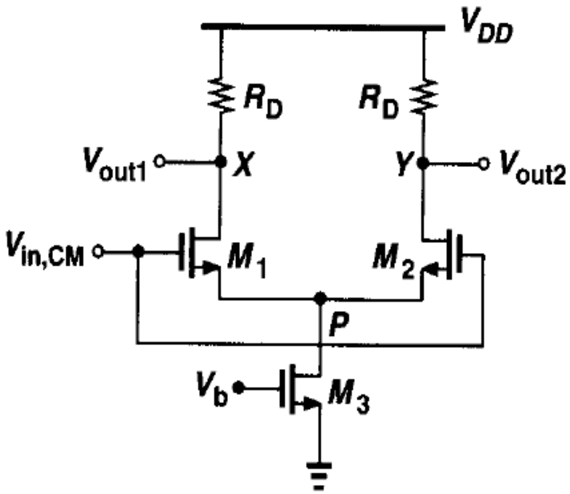


Figure 4.8 (a) Differential pair sensing an input common-mode change, (b) equivalent circuit if M_3 operates in deep triode region, (c) common-mode input-output characteristics.

CM输入范围：$V_{DD} - R_D I_{SS}/2 + V_{TH1} \ge V_{in,CM} \ge V_{TH1} + V_{OD1} + (V_b - V_{TH3})$

M1、M2饱和区 M3饱和区,VOD:过驱动电压

共模增益：应很小



共模输入时，两边并联合并为带源极负反馈的共源级。

当沟道长度调制效应可忽略时：

$$A_{vCM}(\text{或记}A_{vc}) = \frac{\partial V_{out}}{\partial V_{inCM}} = \frac{-R_D/2}{1/2g_m + R_S} = \frac{-g_m R_D}{1+2g_m r_o} \approx \frac{-R_D}{2r_o}$$

共模CM“变化信号”实为噪声：
地噪声、输入共模噪声、
电源噪声（下一级的输入共模噪声）、输入（温度）漂移，两端相同！

Output voltage swing of a differential pair

单端输出范围（RC上拉负载）：

$$V_{DD} > V_{oCM} > V_{in,CM} - V_{TH1}$$

$$V_{in,CM} \geq V_{GS1} + (V_{GS3} - V_{TH3})$$

较大的共模输入变化会扰乱偏置点、改变小信号增益，并限制输出电压摆幅。

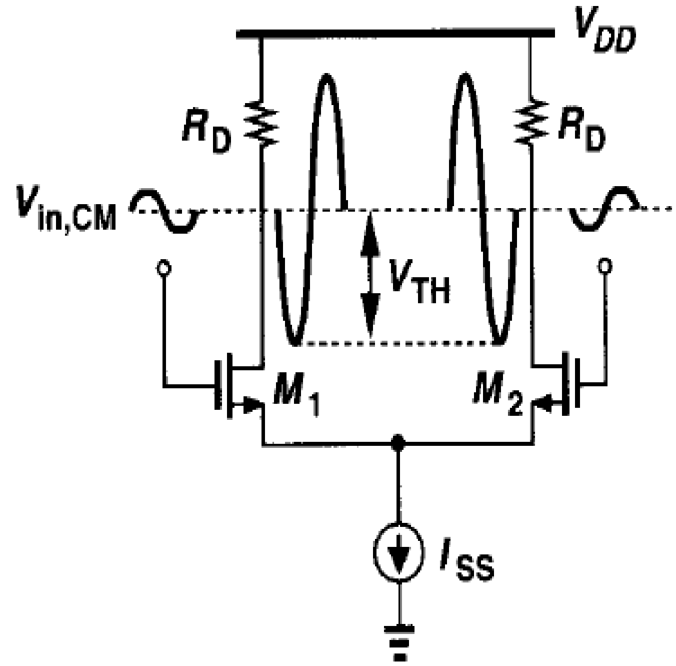


Figure 4.10 Maximum allowable output swings in a differential pair.

4.2.2 quantitative analysis

求：差动增益A_{vd}（或记A_v）$= \dfrac{\partial(V_{out1}-V_{out2})}{\partial(V_{in1}-V_{in2})}$

定义差分电路跨导：$G_m = \dfrac{\partial(I_{D1}-I_{D2})}{\partial(V_{in1}-V_{in2})} = \dfrac{\partial\Delta I_D}{\partial\Delta V_{in}}$

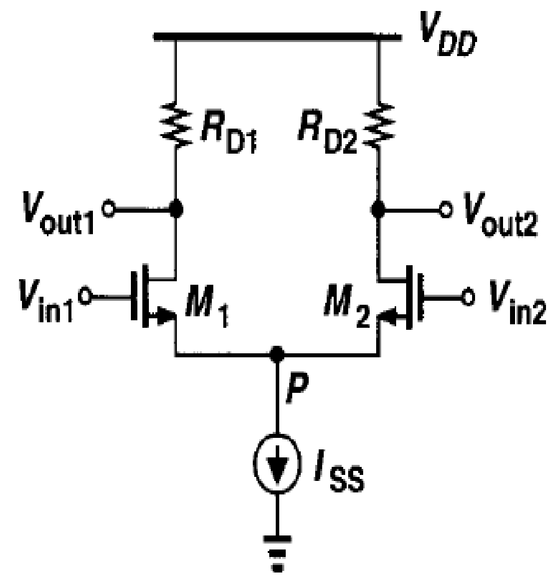


Figure 4.11 Differential pair.

公式解析法：

$$\Delta V_{out} = V_{out1} - V_{out2} = (V_{DD} - R_{D1}I_{D1}) - (V_{DD} - R_{D2}I_{D2})$$

$$= -R_D(I_{D1} - I_{D2}) = -R_D\Delta I_D$$

$$R_{D1} = R_{D2} = R_D$$

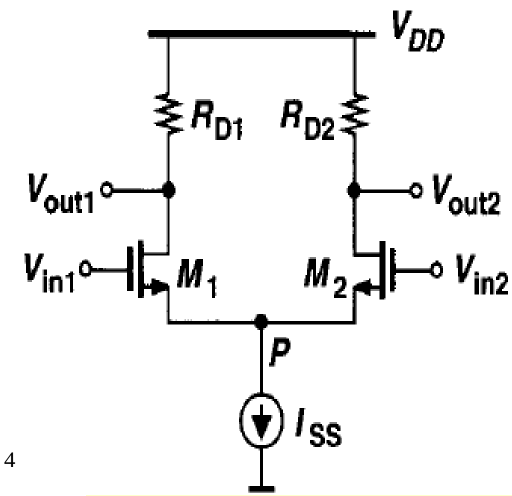
$\because V_P = V_{in1} - V_{GS1} = V_{in2} - V_{GS2} \quad \therefore \quad V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$

由$I_D = \dfrac{1}{2}\mu_n C_{ox}\dfrac{W}{L}(V_{GS}-V_{TH})^2$得$V_{GS} = \sqrt{\dfrac{2I_D}{\mu_n C_{ox}\dfrac{W}{L}}} + V_{TH}$

设M1、M2工作在饱和区，沟道长度调制效应可忽略

$\therefore \quad V_{in1} - V_{in2} = \sqrt{\dfrac{2I_{D1}}{\mu_n C_{ox}\dfrac{W}{L}}} - \sqrt{\dfrac{2I_{D2}}{\mu_n C_{ox}\dfrac{W}{L}}}$，式（4.5）

以下利用I_{SS}计算$I_{D1}-I_{D2}$



由$I_{D1}+I_{D2}=I_{SS}$和公式（4.5）得$(V_{in1}-V_{in2})^2=\dfrac{2}{\mu_n C_{ox}\frac{W}{L}}(I_{SS}-2\sqrt{I_{D1}I_{D2}})$

$$\longrightarrow\quad 2\sqrt{I_{D1}I_{D2}}=I_{SS}-\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2$$

$$\longrightarrow\quad 4I_{D1}I_{D2}=I_{SS}{}^2-I_{SS}\left(\mu_n C_{ox}\frac{W}{L}\right)(V_{in1}-V_{in2})^2+\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1}-V_{in2})^4$$

差分对VI线性比单管MOSFET好！

$$\text{又}\because 4I_{D1}I_{D2}=(I_{D1}+I_{D2})^2-(I_{D1}-I_{D2})^2=I_{SS}^2-(I_{D1}-I_{D2})^2$$

$$\therefore (I_{D1}-I_{D2})^2=I_{SS}^2-4I_{D1}I_{D2}=I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2-\frac{1}{4}(\mu_n C_{ox}\frac{W}{L})^2(V_{in1}-V_{in2})^4$$

$$=\frac{1}{4}【\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})】^2\times【\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}-(V_{in1}-V_{in2})^2】$$

$$\therefore \Delta I_D=I_{D1}-I_{D2}=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}-(V_{in1}-V_{in2})^2}=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\Delta V_{in}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}-\Delta V_{in}{}^2}\text{式（4.9）}$$

quantitative analysis (cont.)

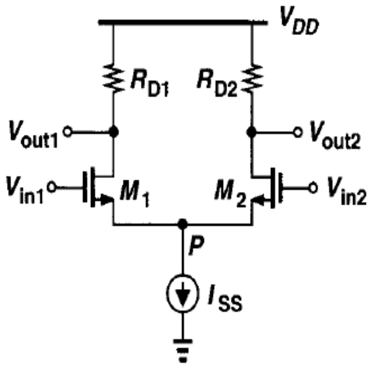
$$G_m = \frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2} - \frac{\Delta V_{in}}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}\right) = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}$$

$\Delta V_{in} = 0$平衡状态时，达最大跨导（最大增益）：$G_m = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}} = g_m$

差动增益$A_{vd} = \frac{\partial\left(V_{out1} - V_{out2}\right)}{\partial\left(V_{in1} - V_{in2}\right)} = -G_m R_D = -g_m R_D$，前提条件？

当全部Iss流过其中一个MOS时，另一个FET截止。最大差模输入：

由式（4.5） $\Delta V_{inMAX} = V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$



问题：由式（4.9）$\Delta V_{in} = \sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$时， $\Delta I_D = 0$ 对吗?

推论：若输入管W/L小或尾电流源 Iss大，则 差动输入变化范围可以较大

Transconductance of differential pair

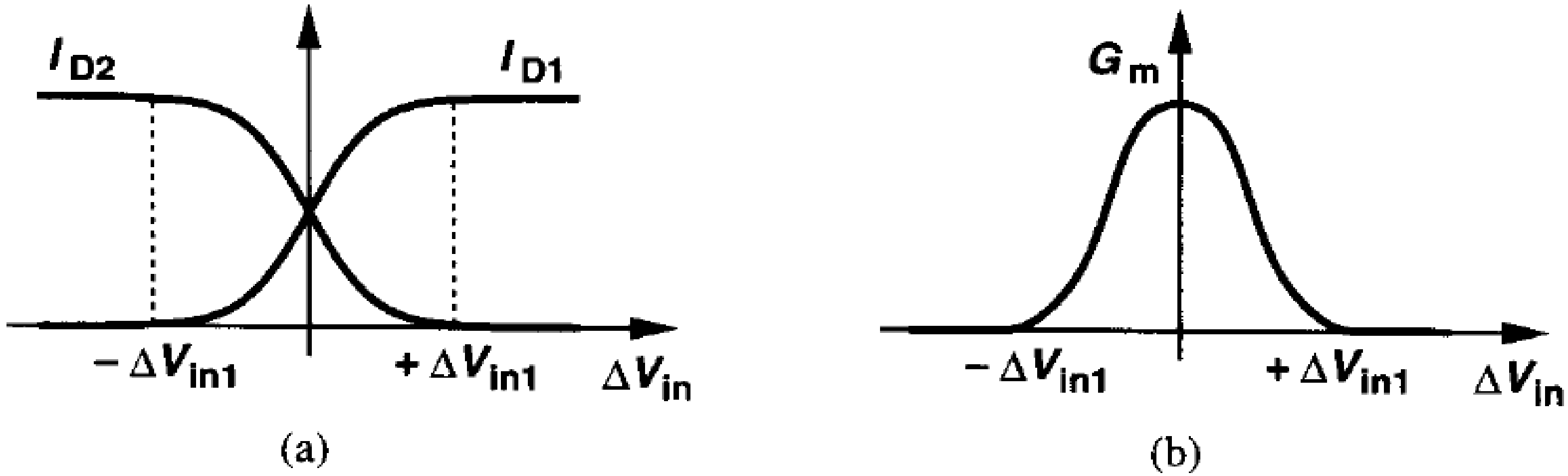
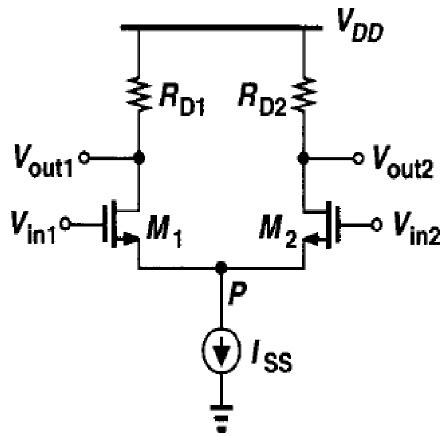
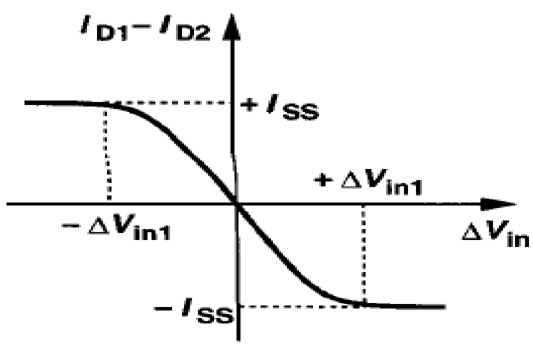


Figure 4.12 Variation of drain currents and overall transconductance of a differential pair versus input voltage.

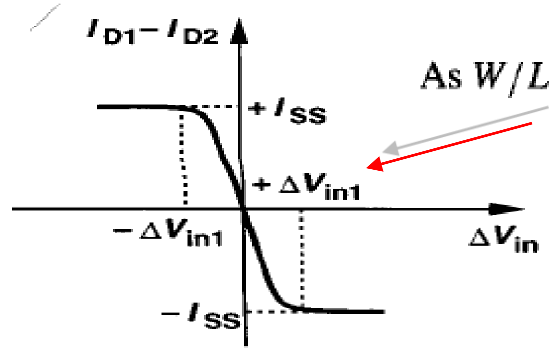


Example 4.2

- Plot the input-output characteristic of a differential pair as the device width and the tail current vary.



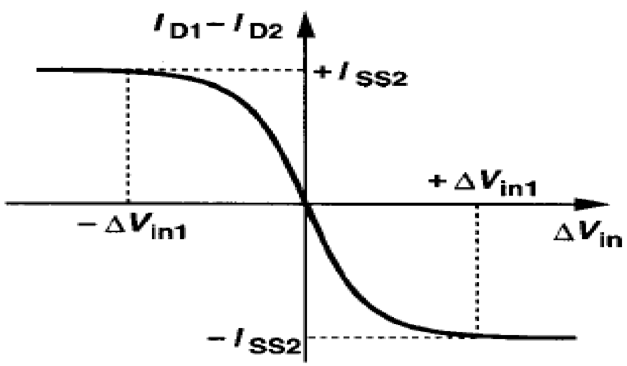
(a)



(b)

As W/L increases, ΔV_{in1} decreases,

$$\Delta V_{inMAX} = \Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$



(c)

Figure 4.13

较大的最大差模输入范围好处是：
线性范围大！

As Iss increases, both the input range and output current swing increase. 图(c)

Small-signal behavior of differential pairs

- Method 1:superposition(叠加法)

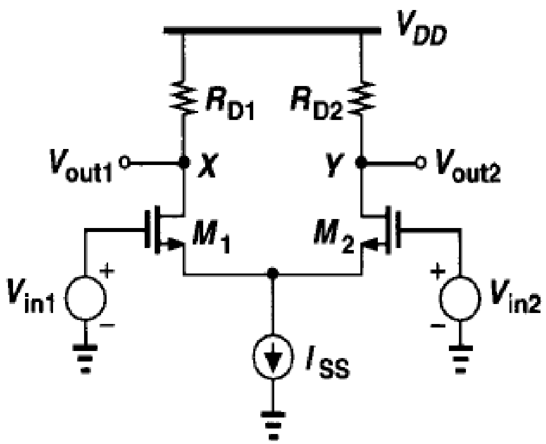
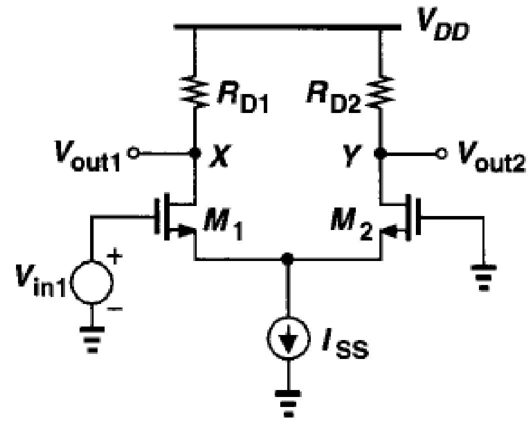


Figure 4.14 Differential pair with small-signal inputs.



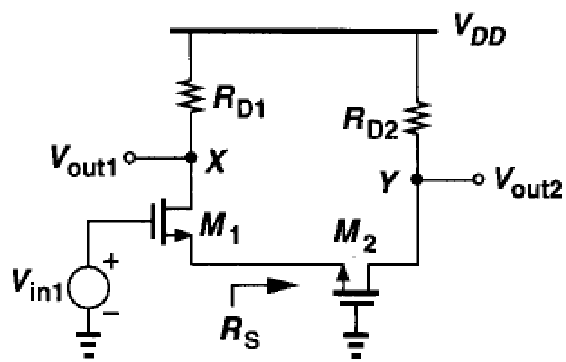
set V_{in2} to zero

(a)

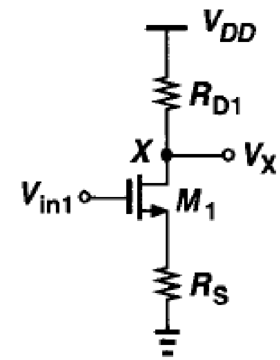
计算Vx

由$I_{D2}=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS2}-V_{TH})^2$ 忽略λ和γ

$$R_S=\partial V_S/\partial I_S=\frac{1}{\partial I_S/\partial V_S}=\frac{1}{-\partial I_{D2}/-\partial V_{GS2}}=\frac{1}{g_{m2}}$$



(b)



(c)

由式（3.57） $$\frac{V_{X1}}{V_{in1}}=-\frac{R_D}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}}$$

Figure 4.15 (a) Differential pair sensing one input signal, (b) circuit of (a) viewed as a CS stage degenerated by M_2, (c) equivalent circuit of (b).

Set Vin2 to zero: 计算VY

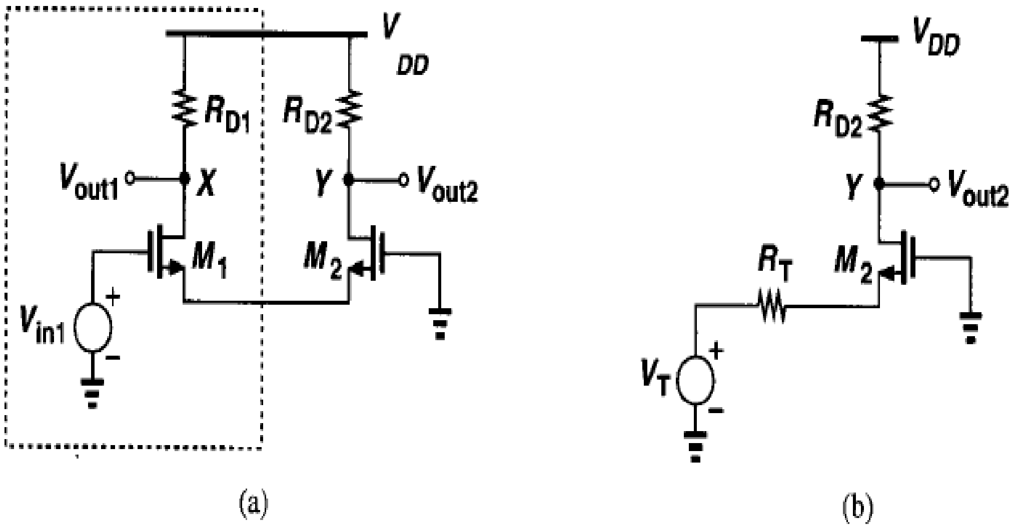
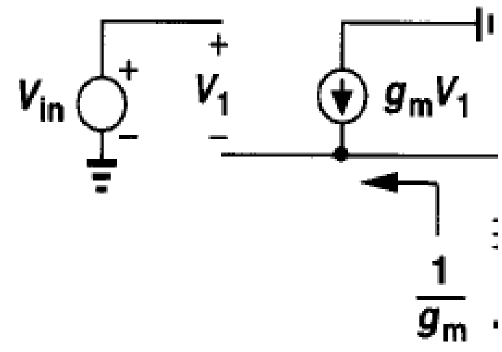


Figure 4.16 Replacing M_1 by a Thevenin equivalent.



令$V_{in1} = 0$

$$R_T = \frac{-V_1}{-g_{m1}V_1} = \frac{1}{g_{m1}}$$

开路电压:$V_T = I_{SC} * R_T = V_{in1}$

小信号 $\frac{V_{Y1}}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$

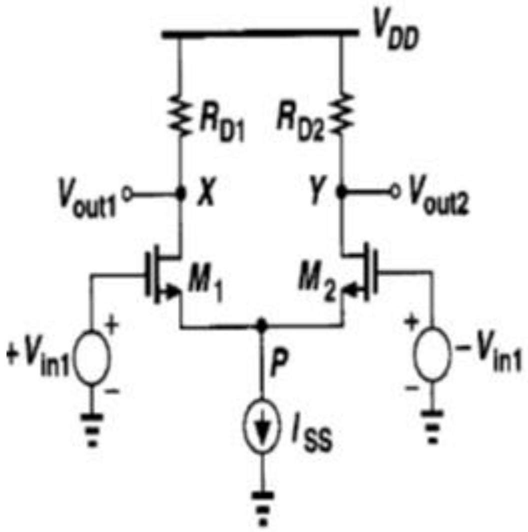
设 $V_{in2} = 0,\quad g_{m1} = g_{m2} = g_m$，则$V_{X1} - V_{Y1} = 2\frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}V_{in1} = -g_mR_DV_{in1}$

Superposition叠加法

Set Vin1 to zero，同理得：$V_{X2} - V_{Y2} = g_m R_D V_{in2} = -g_m R_D V_{in1}$

$$差动增益：A_{vd} = \frac{V_X - V_Y}{V_{in1} - V_{in2}} = \frac{(V_{X1} + V_{X2}) - (V_{Y1} + V_{Y2})}{2V_{in1}} = -g_m R_D$$

- 单边输出，增益减半。



差分对与共源级的比较

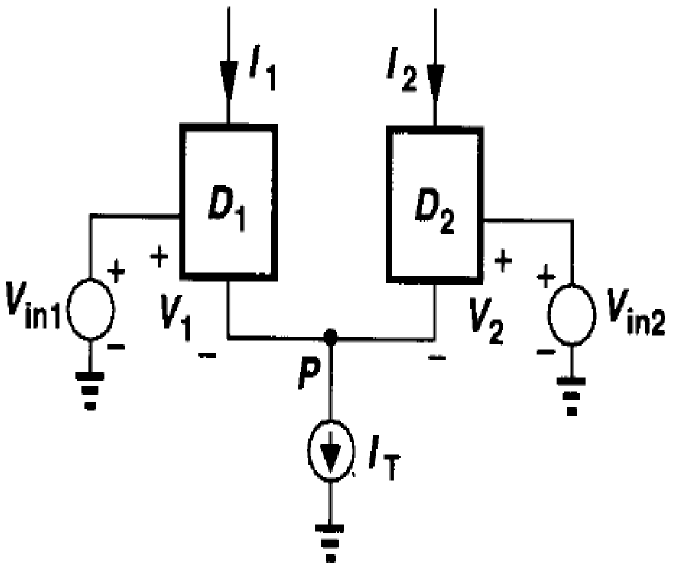
- 设总偏置电流相同，为I_{SS}.
- 平衡状态下，差分对中单管M1（M2）偏置电流$I_{D1}=I_{SS}/2$

- 差分对 $$g_m=\sqrt{2\mu_n C_{ox}\frac{W}{L}I_{D1}}=\sqrt{2\mu_n C_{ox}\frac{W}{L}\frac{I_{SS}}{2}}$$

  - 差分对增益为单管共源级放大器的$1/\sqrt{2}$

Method 2: concept of half circuit

- 对称电路的“虚地”点概念。



- 设差分输入：

$$V_{in1}=V_{CM}+\Delta V$$
$$V_{in2}=V_{CM}-\Delta V$$

- VCM 共模输入电压
- 如果电路保持线性，保证2个管gm相同

$$g_m\Delta V_1+g_m\Delta V_2=0$$

$$\Delta V_1=-\Delta V_2$$

- 则P点电位不变, 交流虚地！

适合幅度变化小的信号！

半边电路概念的应用

- 半边电路概念适合分析全差动输入的对称差动对。

小信号 $\frac{V_X}{V_{in1}} = -g_m R_D$

$$\frac{V_Y}{V_{in2}} = \frac{V_Y}{-V_{in1}} = -g_m R_D$$

$$\text{差动增益}A_v = \frac{V_X - V_Y}{V_{in1} - V_{in2}} = \frac{V_X - V_Y}{2V_{in1}} = -g_m R_D$$

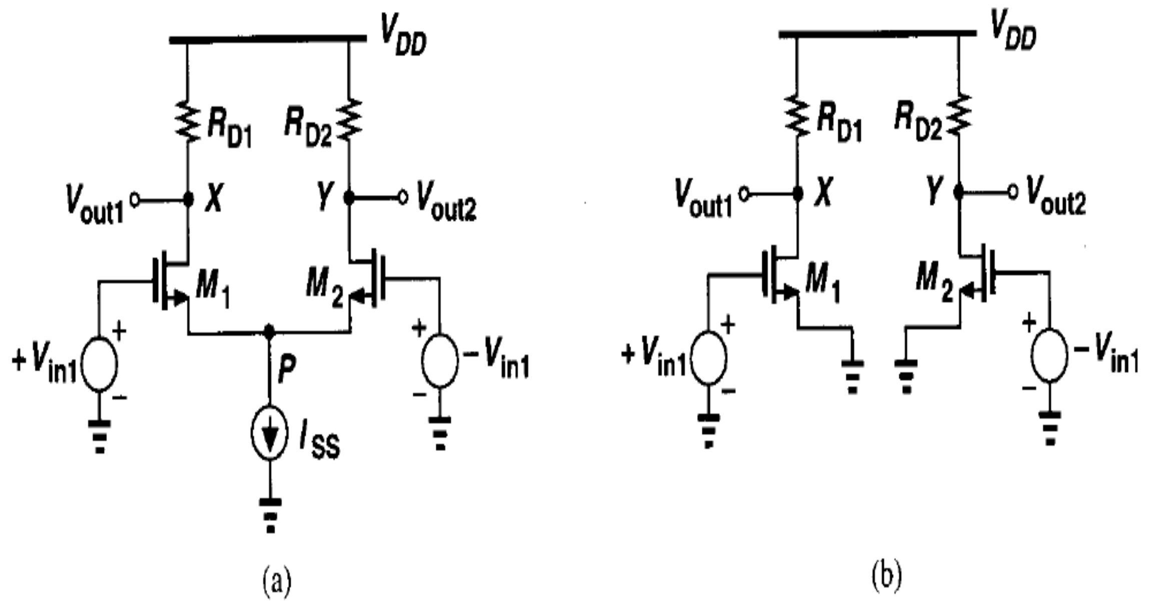


Figure 4.20 Application of the half-circuit concept.

半边电路计算简单（全差分结构、输入信号变化幅度小）

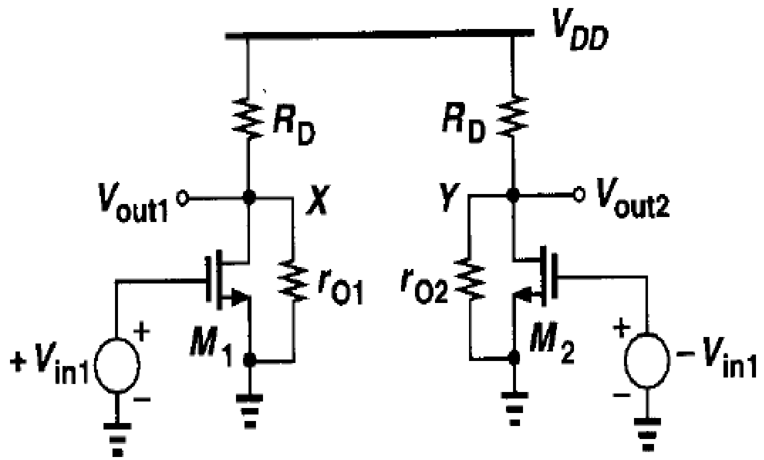
Example 4.4 计算差动增益

设 $r_{o1} = r_{o2} = r_o$

$$\frac{V_X}{V_{in1}} = -g_m(R_D \parallel r_o)$$

$$\frac{V_Y}{V_{in2}} = \frac{V_Y}{-V_{in1}} = -g_m(R_D \,||\, r_o)$$

$$A_{vd} = \frac{V_X - V_Y}{V_{in1} - V_{in2}} = \frac{V_X - V_Y}{2V_{in1}} = -g_m(R_D \,||\, r_o)$$



$\lambda \neq 0 \quad \Leftrightarrow r_o \neq \infty$

考虑沟道长度调制效应

任何输入可分解成差模信号分量+共模信号分量

$$V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2}$$

$$V_{in2} = -\frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2}$$

对所有V_{in}均成立

实际电路需要保证两边直流电压工作点一致，否则gm失配

差动信号无直流分量，无论大小均视为变化量。

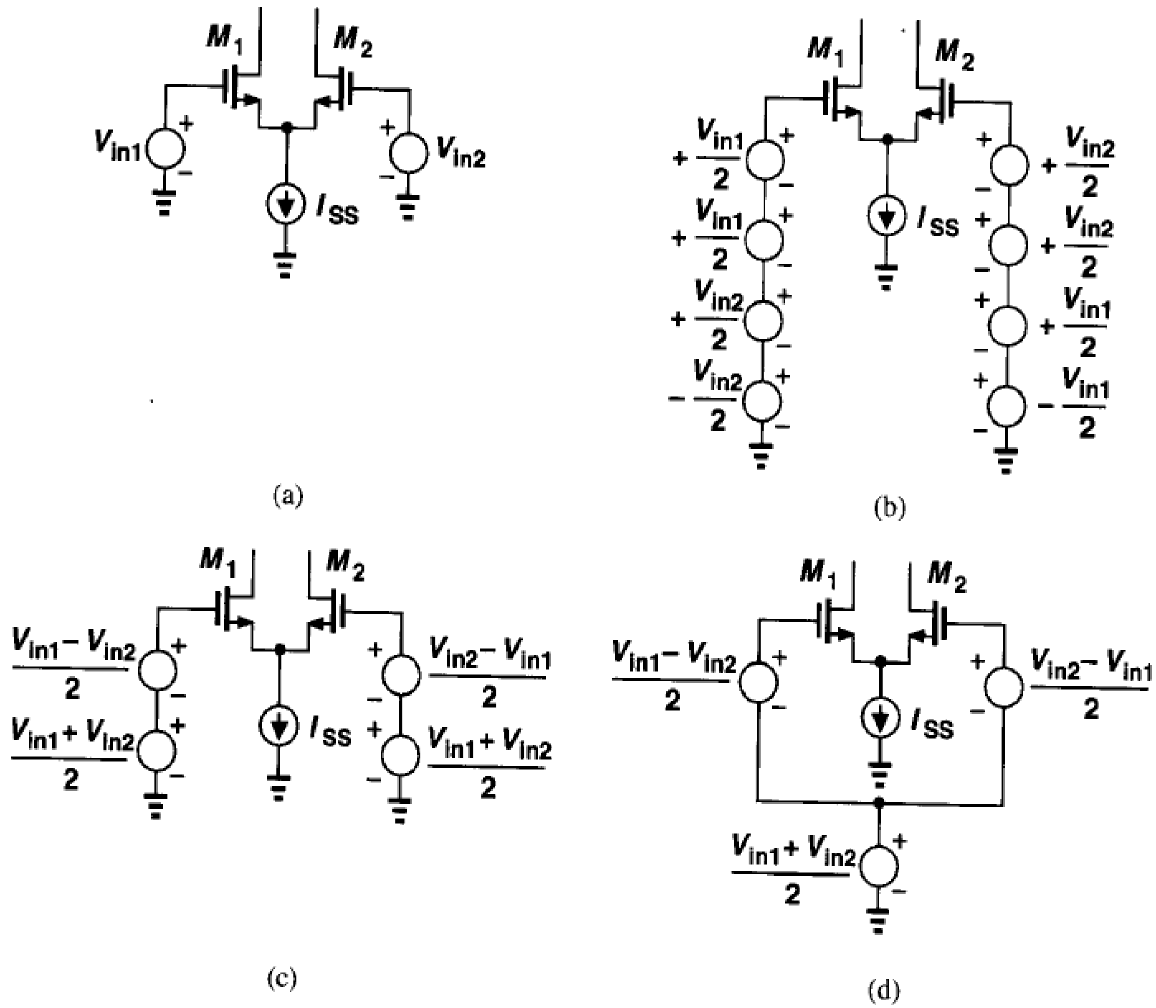
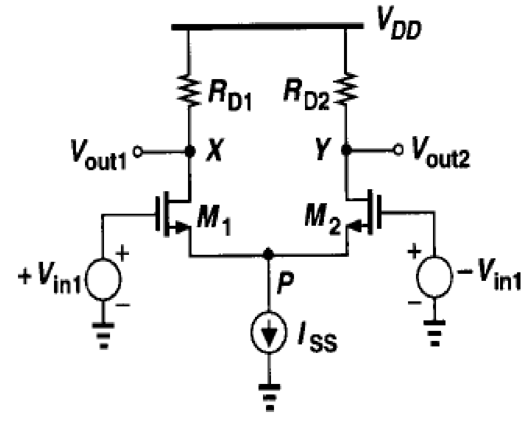


Figure 4.22 Conversion of arbitrary inputs to differential and common-mode components.

Example 4.5

In the circuit of Fig. 4.20(a), calculate V_X and V_Y if $V_{in1} \neq -V_{in2}$ and $\lambda \neq 0$.



(a)

- 差模小信号：图4.24(a)

$$V_X = -g_m(R_D \,||\, r_o)\frac{V_{in1} - V_{in2}}{2}$$

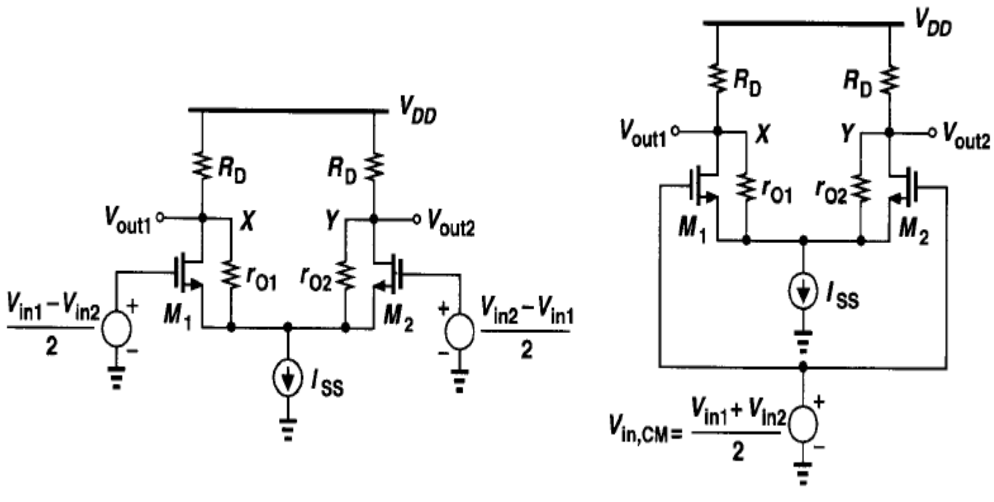
$$V_Y = -g_m(R_D \,||\, r_o)\frac{V_{in2} - V_{in1}}{2}$$

$$V_X - V_Y = -g_m(R_D \,\|\, r_o)(V_{in1} - V_{in2})$$

•共模小信号（交变）：图4.24(b)

M1和M2的漏电流均为Iss/2，Vx和Vy不变。共模抑制！

实际电路中若Vincm=1/2(Vin1+Vin2)上升，则VGS和VP均会上升，Iss稍微上升（沟道长度调制）。



(a) (b)

Figure 4.24

4.3 common mode response

- 差动放大器的重要特点是对共模噪声的抑制。
- 设电流源输出电阻Rss（理想值为无穷大）

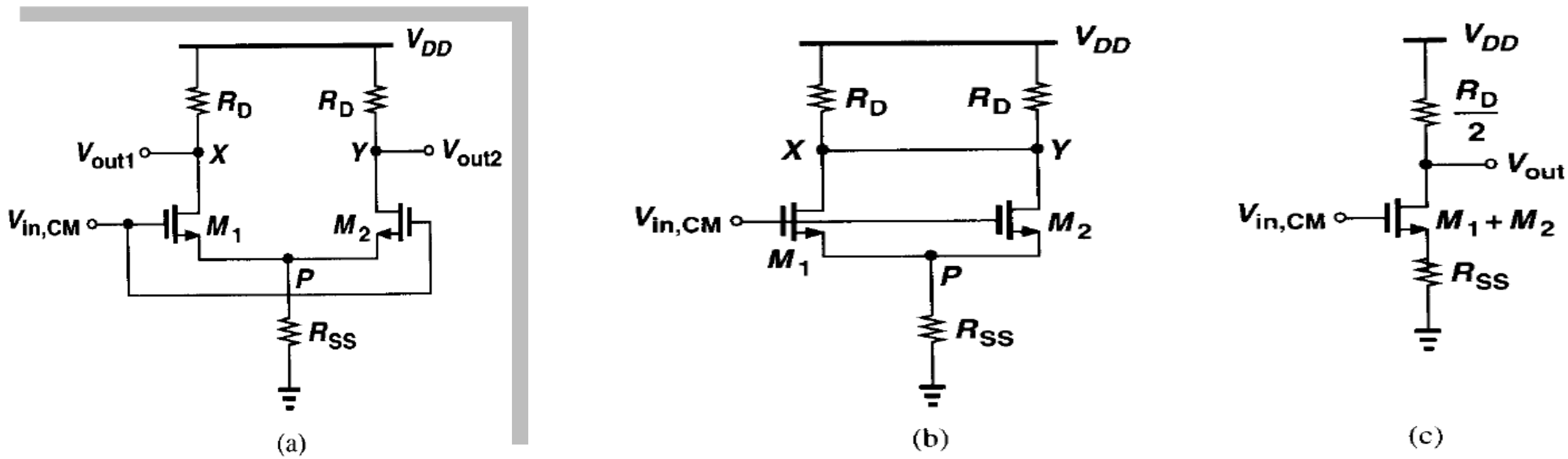


图4.25(a) 共模输入的差动对电路；图(a)的简化电路；图(b) 的等效电路(gm为单管的2倍)

$$A_{v,CM}=\frac{\partial V_{out}}{\partial V_{in,CM}}=-\frac{R_D/2}{\frac{1}{2g_m}+R_{SS}}，\quad 式（4.28）$$

增大R_{SS}，减小$A_{v,CM}$

Example 4.6

已知：$I_{SS} = 1mA,\ \left(\frac{W}{L}\right)_{1,2} = \frac{2.5}{0.5},\ \mu_n C_{ox} = 50\mu A/V^2,$

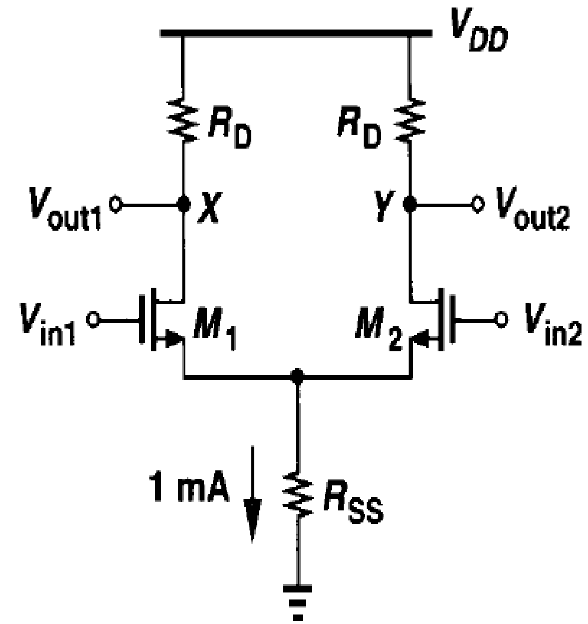
$V_{TH} = 0.6V,\ \lambda = \gamma = 0,\ V_{DD} = 3.3V$

(a) V_{Rss}=0.5V,输入共模电压应是多少？

（b）差模增益=5时R_D=?

（c）输出共模电平？最低单端输出电平？

（d）输入共模增加50mV，输出变化多大？



解（a）$V_{in,CM} = V_{GS} + V_{RSS}$

$$R_{SS} = \frac{0.5V}{1mA} = 500\Omega$$

$$I_{D1} = I_{D2} = 0.5mA$$

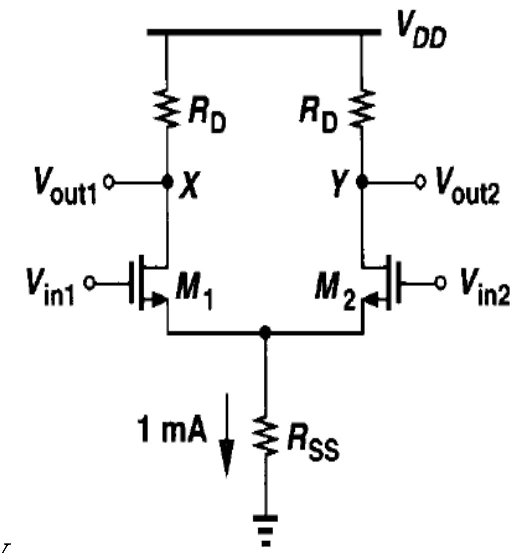
$$V_{GS1} = V_{GS2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} + V_{TH1} = 1.23V$$

设$\lambda = \gamma = 0$

$$V_{in,CM} = V_{GS} + V_{RSS} = 1.23V + 0.5V = 1.73V$$

Example 4.6 (cont.)

(b)：已知 $|A_v| = \left|\frac{\Delta V_{out}}{\Delta V_{in}}\right| = \sqrt{\mu_n C_{ox}\frac{W}{L}I_{SS}}R_D = g_{m1}R_D = 5$



$$g_{m1} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_{D1}} = \sqrt{\mu_n C_{ox}\frac{W}{L}I_{SS}} = \frac{1}{632\Omega}$$

$$R_D = \frac{5}{g_m} = 3.16k\Omega \;\therefore$$

(c)：共模输出 $V_X = V_{DD} - I_{D1}R_D = 3V - 0.5 * 3.16V = 1.42V$

$$V_{in1} - V_{TH1} \le V_X$$

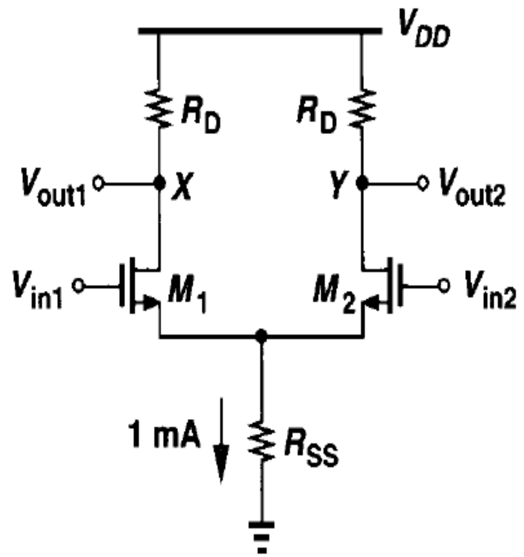
$$V_{X\min} = V_{in,CM} - V_{TH} = 1.73V - 0.6V = 1.13V$$

若输出电压减小1.42-1.13=0.29V晶体管就会进入线性区，RD不可较大。

Example 4.6 (cont.)

$$(d):\ \Delta V_{o,CM} = A_{v,CM}\Delta V_{in,CM} = -\frac{R_D/2}{\frac{1}{2g_m}+R_{SS}}\Delta V_{in,CM}$$

$$= -\frac{3160/2}{632/2+500}\times 50mV = -96.8mV$$



结果表明该结构不好，共模抑制差。

原因是Rss阻值太小（电流随输入电平变化）。

差分电路的问题：失配！

差分电路要求电路严格对称！

$$\text{小信号}A_{v,CM} = \frac{\partial V_{out}}{\partial V_{in,CM}} = -\frac{R_D/2}{\frac{1}{2g_m}+R_{SS}}$$

设负载失配ΔR_D：

$$\Delta V_X \approx -\frac{R_D}{\frac{1}{g_m}+R_{SS}}\Delta V_{in,CM} \qquad \Delta V_Y \approx -\frac{R_D+\Delta R_D}{\frac{1}{g_m}+R_{SS}}\Delta V_{in,CM}$$

导致共模输入产生差动输出，共模噪声对输出影响很大。

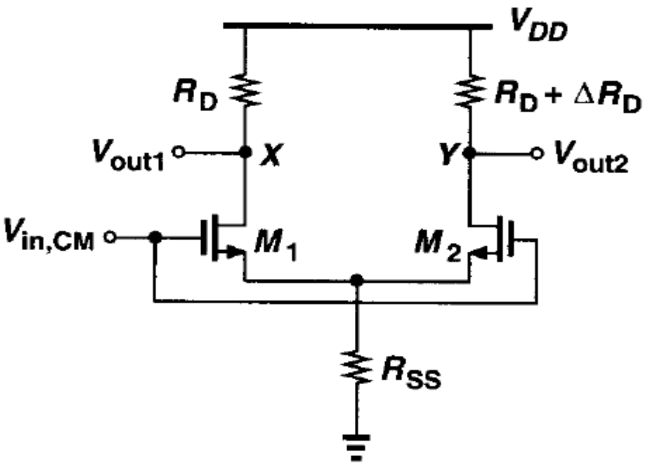


Figure 4.27 Common-mode response in the presence of resistor mismatch.

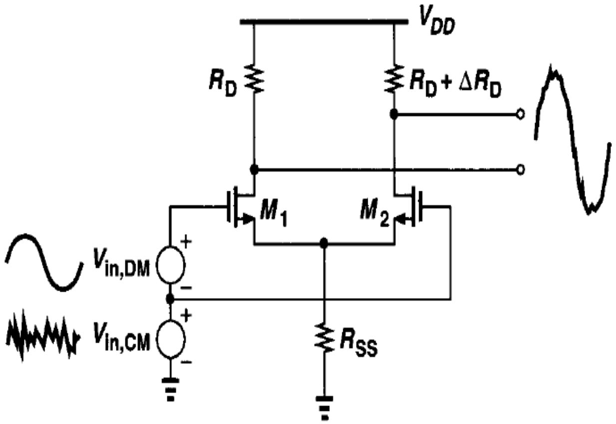


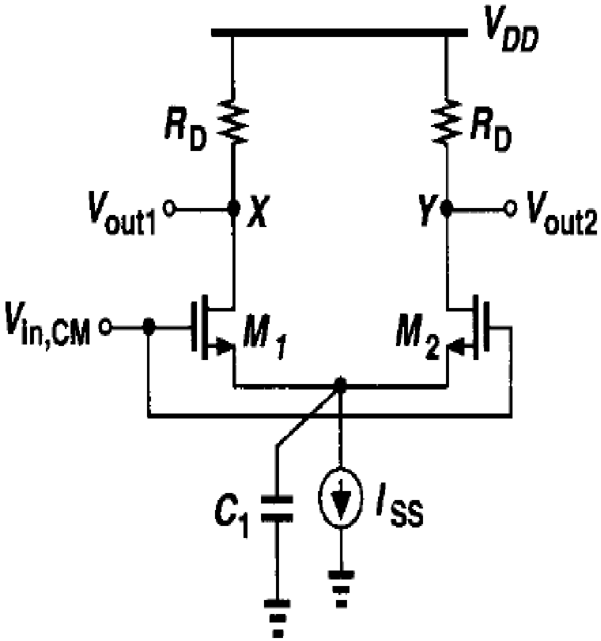
Figure 4.28 Effect of CM noise in the presence of resistor mismatch.

总结：差动电路的共摸响应取决于尾电流源和电路非对称性。

失配导致输入共模信号在输出端产生差模分量。

失配导致共模噪声转换为差模噪声“信号”

实际差分电路的不对称性产生失配，主要来自输入晶体管，工艺误差造成的阈值电压和尺寸（包括版图不平衡）不一致，体现为gm不同、电流不同。



差动结构缺点：对工艺质量（失配）敏感，功耗稍大，版图要求对称。

共模输入噪声影响：输入管不匹配情况讨论

交变小信号

$$I_{D1} = g_{m1}(V_{in,CM} - V_P) \qquad I_{D2} = g_{m2}(V_{in,CM} - V_P)$$

$$V_P = (I_{D1} + I_{D2})R_{SS} = (g_{m1} + g_{m2})(V_{in,CM} - V_P)R_{SS}$$

$$\therefore V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM}$$

$$V_X = -I_{D1}R_D = -g_{m1}(V_{in,CM} - V_P)R_D$$

$$= -g_{m1}\frac{1}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM} R_D$$

$$V_Y = -I_{D2}R_D = -g_{m2}(V_{in,CM} - V_P)R_D$$

$$= -g_{m2}\frac{1}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM} R_D$$

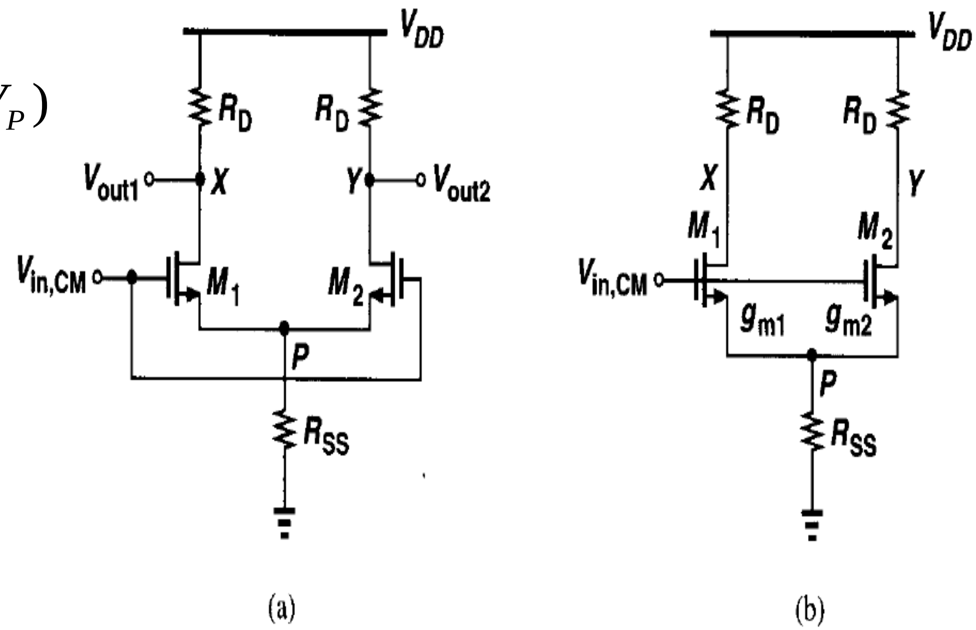


Figure 4.30 (a) Differential pair sensing CM input, (b) equivalent circuit of (a).

由失配产生的差动输出： $V_X - V_Y = -\dfrac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM} R_D$

应当极小

共模噪声转化成差动小信号误差：

$$A_{CM-DM} = \frac{V_X - V_Y}{V_{in,CM}} = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D = -\frac{\Delta g_m}{(g_{m1} + g_{m2})R_{SS} + 1} R_D,\ \text{式 (4.43)}$$

Example 4.7

M3和M4的跨导失配Δg_m。多大比例的电源噪声以差动分量的形式出现在输出端？

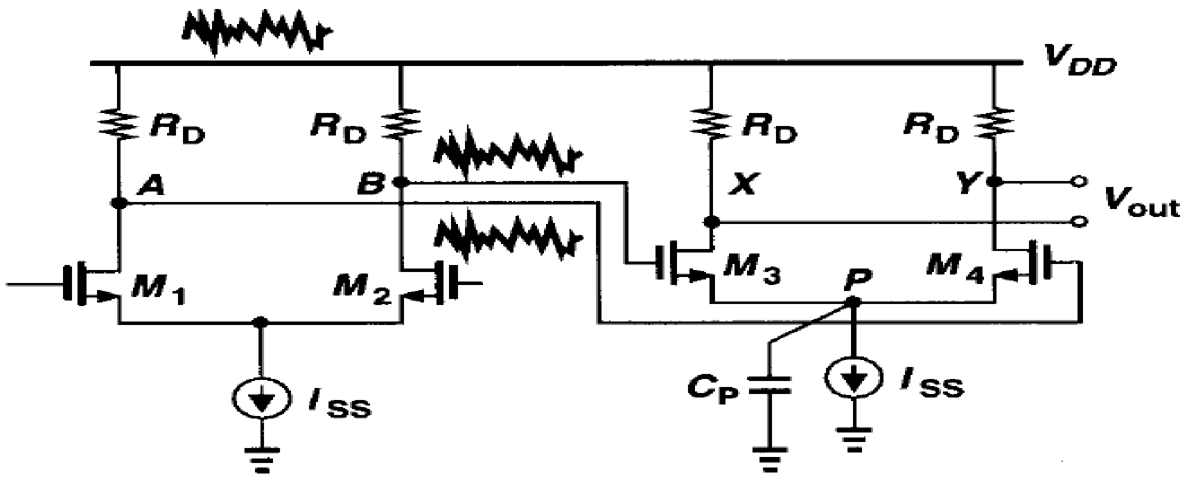


Figure 4.31

Assume $\lambda = \gamma = 0$.

解：电源噪声是共模噪声。尾电源源的交流阻抗很大，因此电源噪声全部加到A点和B点成为M3和M4的共模输入（交变小信号）。由(4.43)

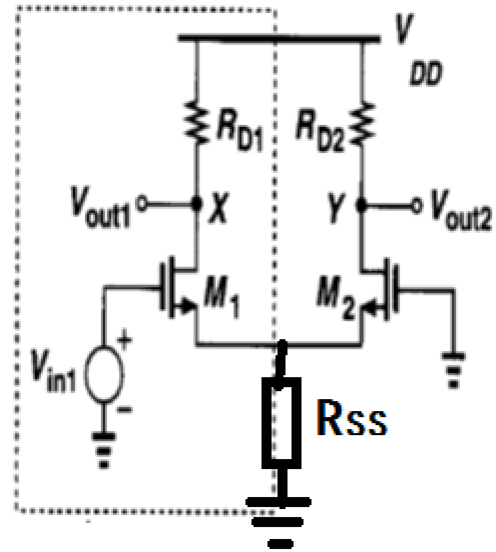
$$A_{\text{CM-DM}} = \frac{V_X - V_Y}{V_{in,CM}} = -\frac{\Delta g_m}{(g_{m3}+g_{m4})\frac{1}{j\omega C_p}+1} R_D \longrightarrow |A_{\text{CM-DM}}| = \left| \frac{\Delta g_m}{\sqrt{(g_{m3}+g_{m4})^2\left|\frac{1}{\omega C_p}\right|^2+1}} R_D \right|$$

共模抑制比Common-mode rejection ratio

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

注意区别 $\left| \frac{A_{DM}}{A_{CM}} \right|$

设MOS失配：$g_{m1} \neq g_{m2}$， I_{SS}的$R_{SS} \neq \infty$



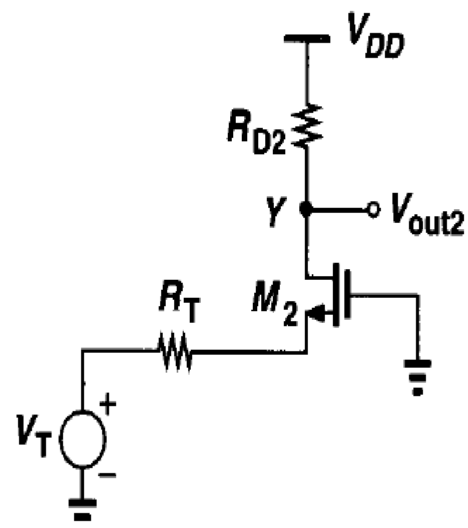
- 参考图4.15采用叠加定律

（失配时半边电路分析不成立）

令$V_{in2} = 0$，$\frac{V_X}{V_{in1}} = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}} \,||\, R_{SS}}$

$$R_T = \frac{1}{g_{m1}} \,||\, R_{SS} = \frac{\frac{1}{g_{m1}} R_{SS}}{\frac{1}{g_{m1}} + R_{SS}} = \frac{R_{SS}}{1 + g_{m1} R_{SS}}$$

$$V_T = V_{in} g_{m1} \left(\frac{1}{g_{m1}} \| R_{SS} \right) = V_{in} \frac{g_{m1} R_{SS}}{1 + g_{m1} R_{SS}}$$



Common-mode rejection ratio (cont.)

- 由共栅级增益公式：$$\frac{V_{out2}}{V_T}=\frac{R_{D2}}{\frac{1}{g_{m2}}+R_T}$$

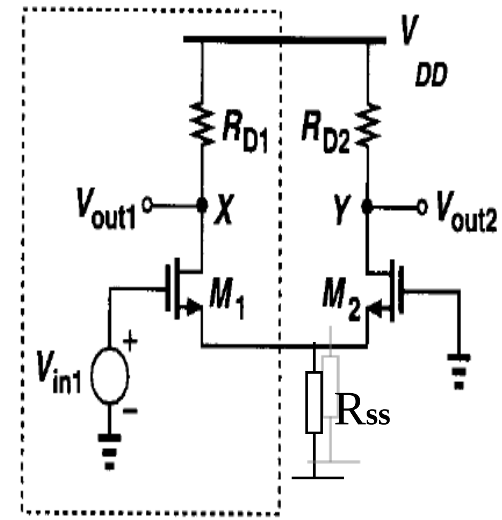
得 $$\frac{V_y}{V_{in1}}=\frac{V_y}{V_T}\frac{V_T}{V_{in1}}=\frac{R_D}{R_T+\frac{1}{g_{m2}}}*\frac{g_{m1}R_{SS}}{1+g_{m1}R_{SS}}=\frac{R_D}{\frac{1}{g_{m1}}\parallel R_{SS}+\frac{1}{g_{m2}}}*\frac{g_{m1}R_{SS}}{1+g_{m1}R_{SS}}$$

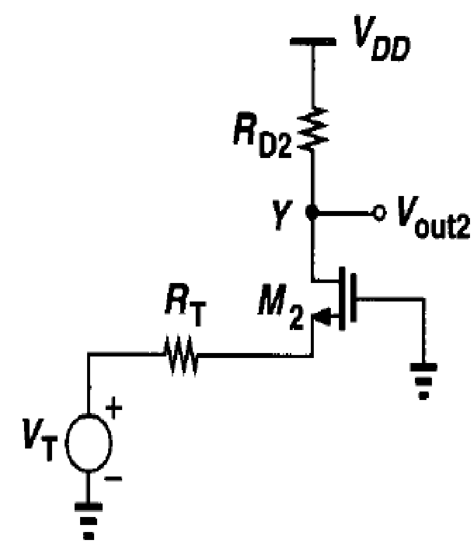
$$(V_X-V_Y)_{Vin1}=\left(\frac{-R_D}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\parallel R_{SS}}-\frac{R_D}{\frac{1}{g_{m1}}\parallel R_{SS}+\frac{1}{g_{m2}}}*\frac{g_{m1}R_{SS}}{1+g_{m1}R_{SS}}\right)V_{in1}$$

同理 $$(V_X-V_Y)_{Vin2}=\left(\frac{R_D}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\parallel R_{SS}}*\frac{g_{m2}R_{SS}}{1+g_{m2}R_{SS}}+\frac{R_D}{\frac{1}{g_{m1}}\parallel R_{SS}+\frac{1}{g_{m2}}}\right)V_{in2}$$

$$V_{in1}=-V_{in2}\qquad A_{DM}=\frac{(V_X-V_Y)_{tot}}{V_{in1}-V_{in2}}=\frac{(V_X-V_Y)_{in1}+(V_X-V_Y)_{in2}}{V_{in1}-V_{in2}}$$

$$=-\frac{R_D}{2}\frac{g_{m1}+g_{m2}+4g_{m1}g_{m2}R_{SS}}{1+(g_{m1}+g_{m2})R_{SS}}\qquad(4.46)$$





CMRR (cont.)

当$g_{m1}=g_{m2}=g_m$

$A_{DM}=-g_m R_D$

即得(4.19) $\frac{(V_X-V_Y)_{tot}}{V_{in1}-V_{in2}}=-g_m R_D$

当$g_{m1}\neq g_{m2}$

$$\mathrm{CMRR}=\left|\frac{A_{\mathrm{DM}}}{A_{\mathrm{CM\text{-}DM}}}\right|=\left|\frac{-\dfrac{R_D}{2}\dfrac{g_{m1}+g_{m2}+4g_{m1}g_{m2}R_{SS}}{1+(g_{m1}+g_{m2})R_{SS}}}{-\dfrac{\Delta g_m}{(g_{m1}+g_{m2})R_{SS}+1}R_D}\right|$$

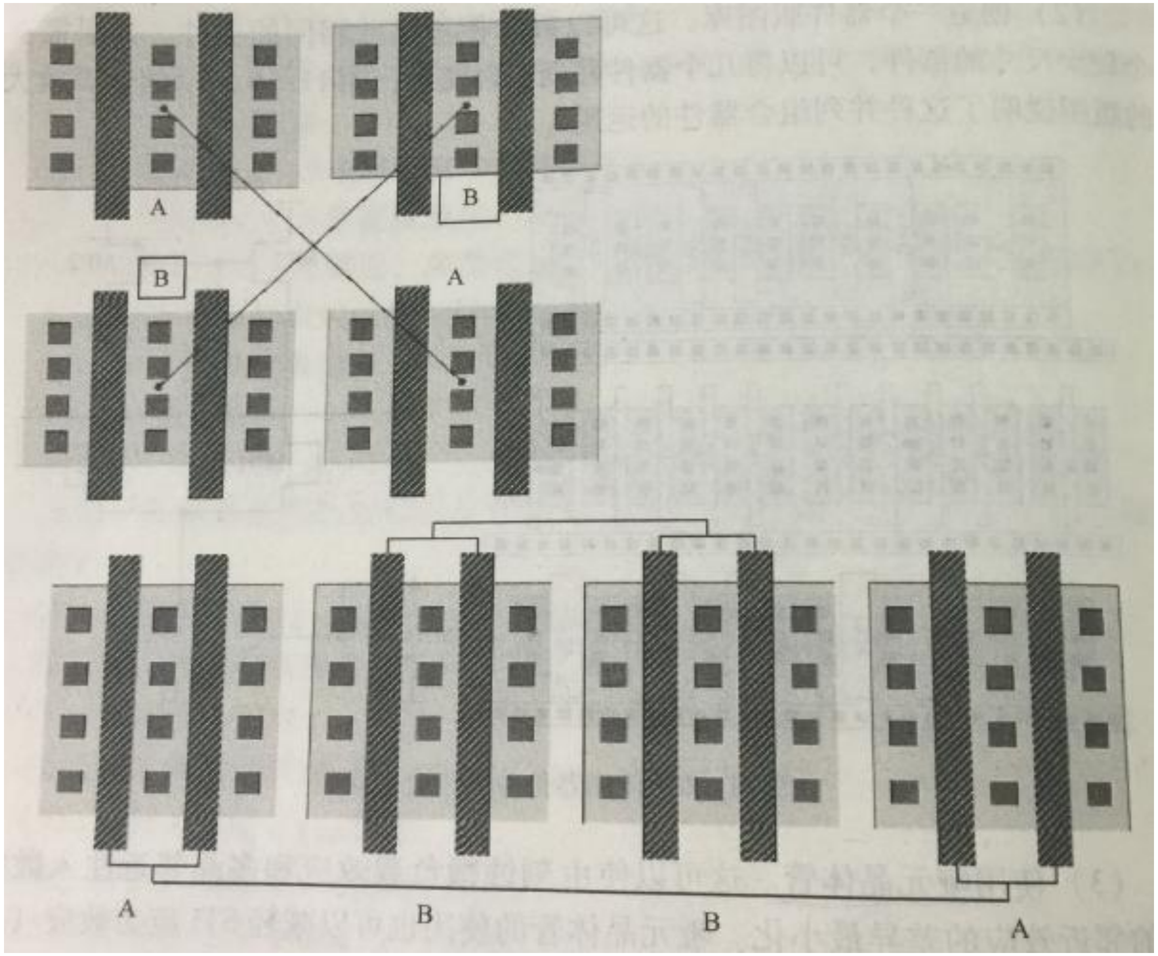
$$=\left|\frac{g_{m1}+g_{m2}+4g_{m1}g_{m2}R_{SS}}{2\Delta g_m}\right|$$

版图设计：质心法（对称）

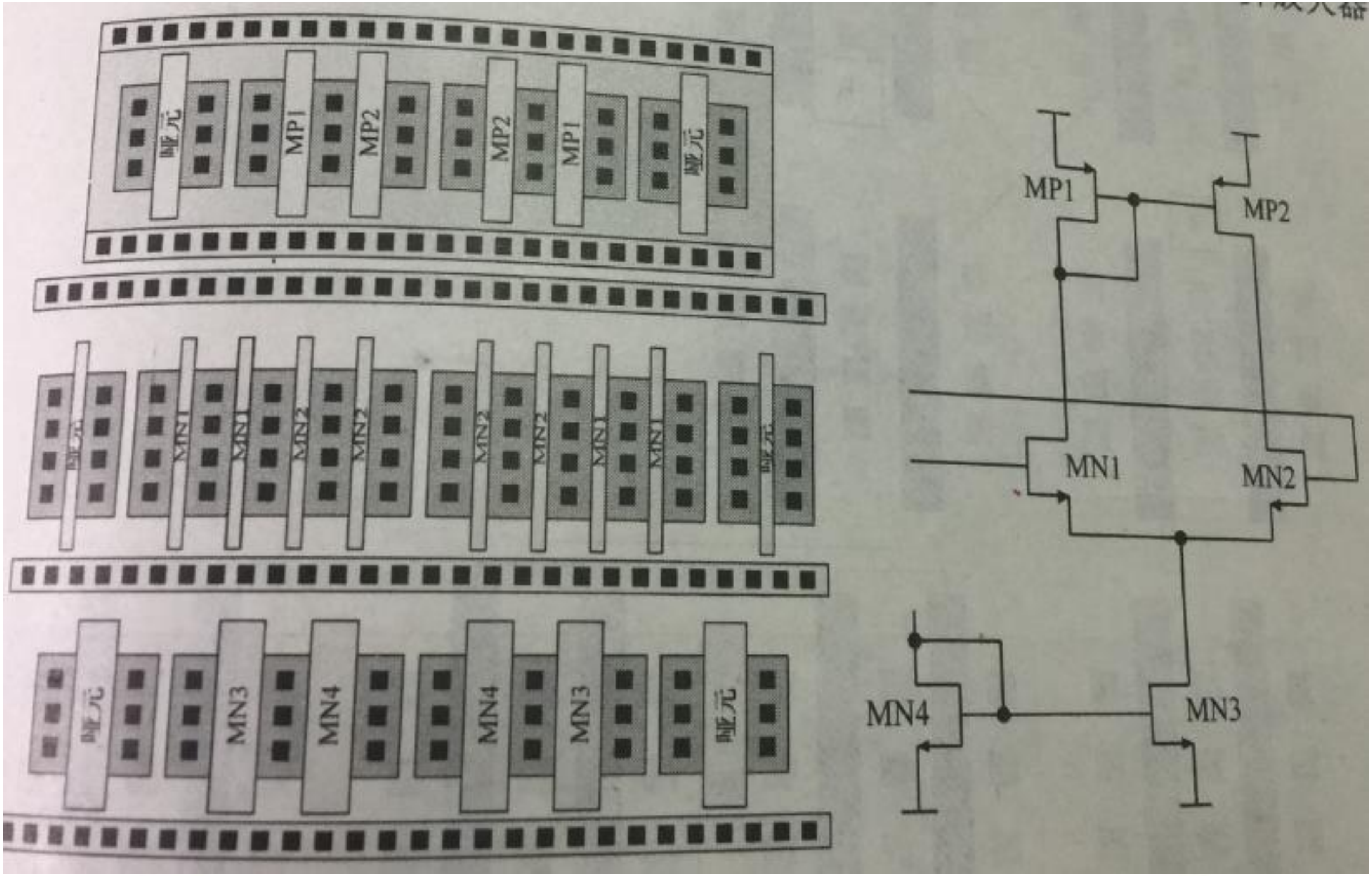
- 质心法布局W/L大的MOS

交叉
对角

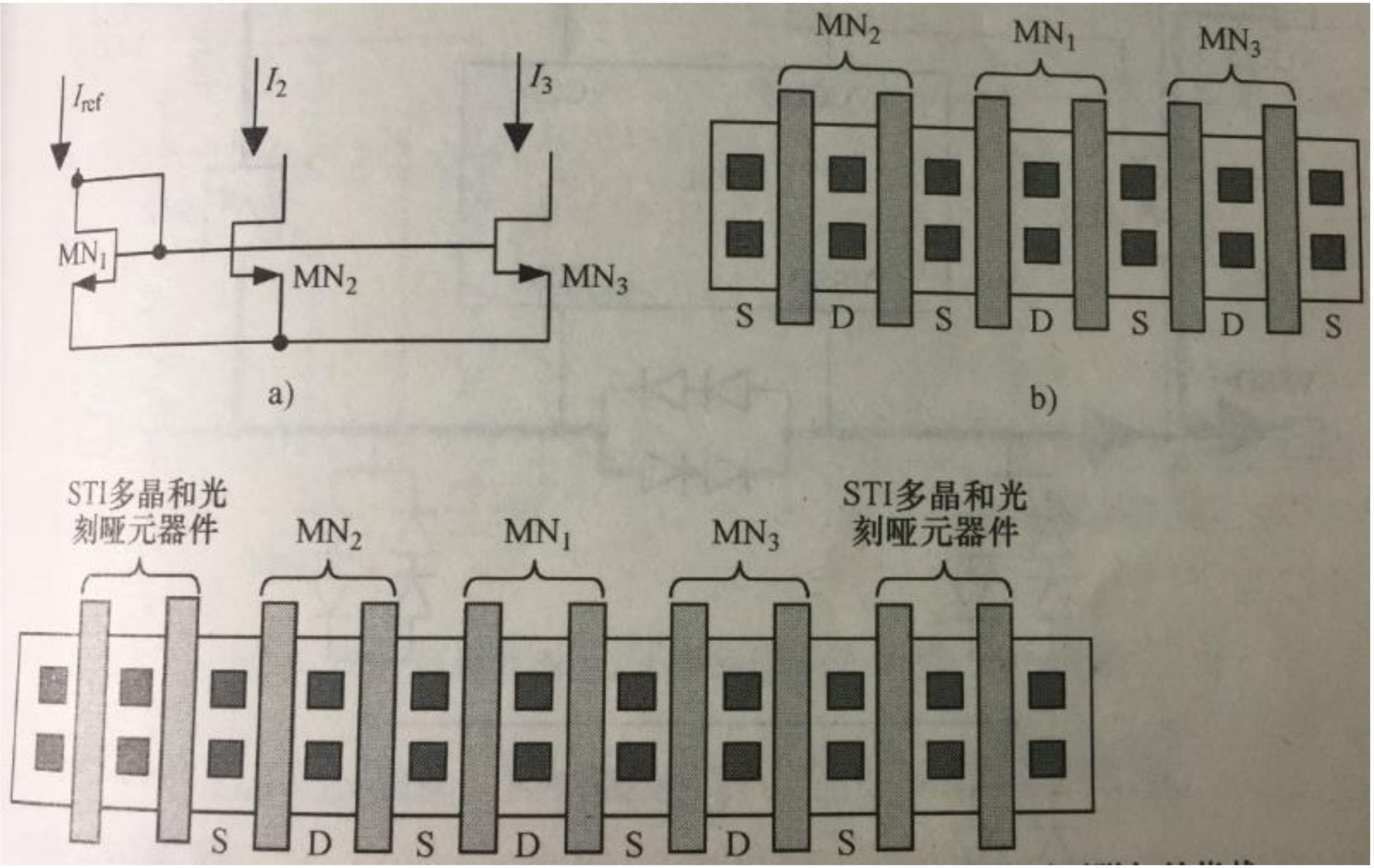
分割
对称



哑元器件（改善临近注入效应）

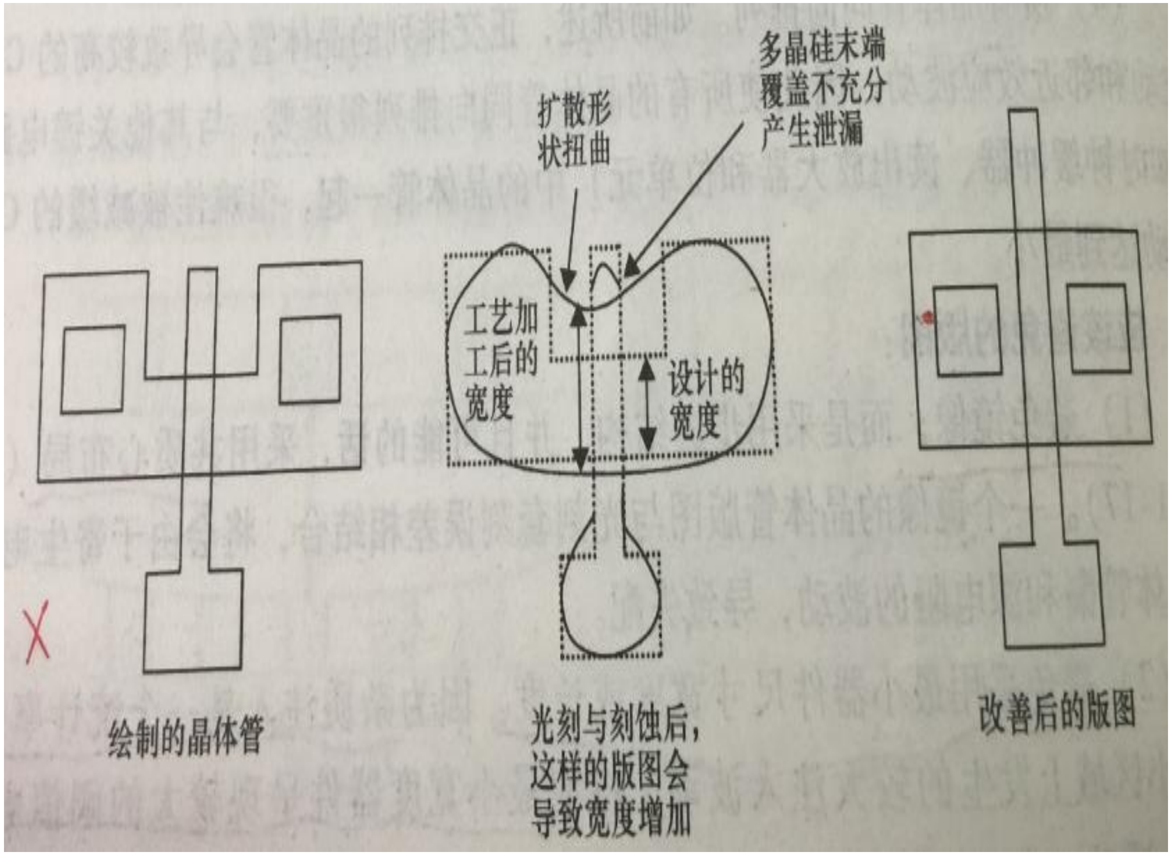


例：镜像电流源

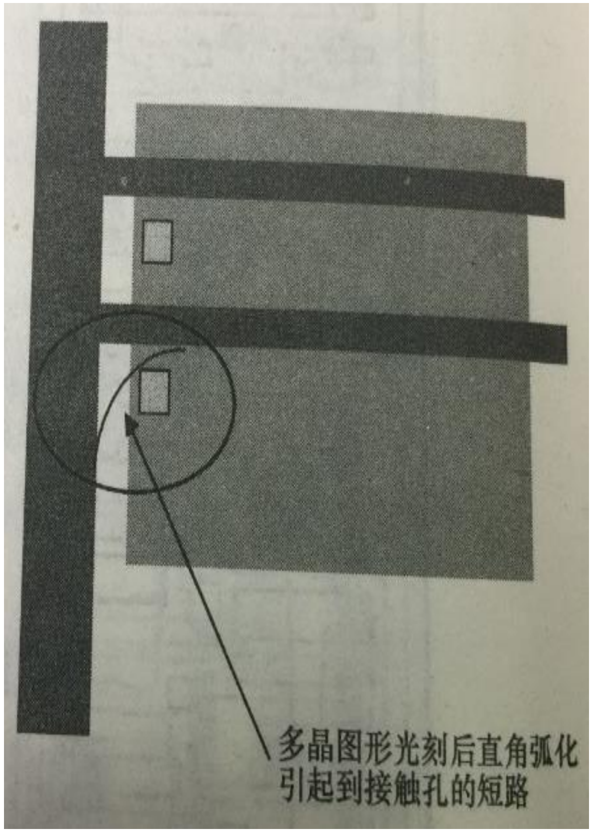


I_{ref}
I_2
I_3
MN_1
MN_2
MN_3
a)
MN_2
MN_1
MN_3
S D S D S D S
b)
STI多晶和光刻哑元器件
MN_2
MN_1
MN_3
STI多晶和光刻哑元器件
S D S D S D S

应避免的版图画法

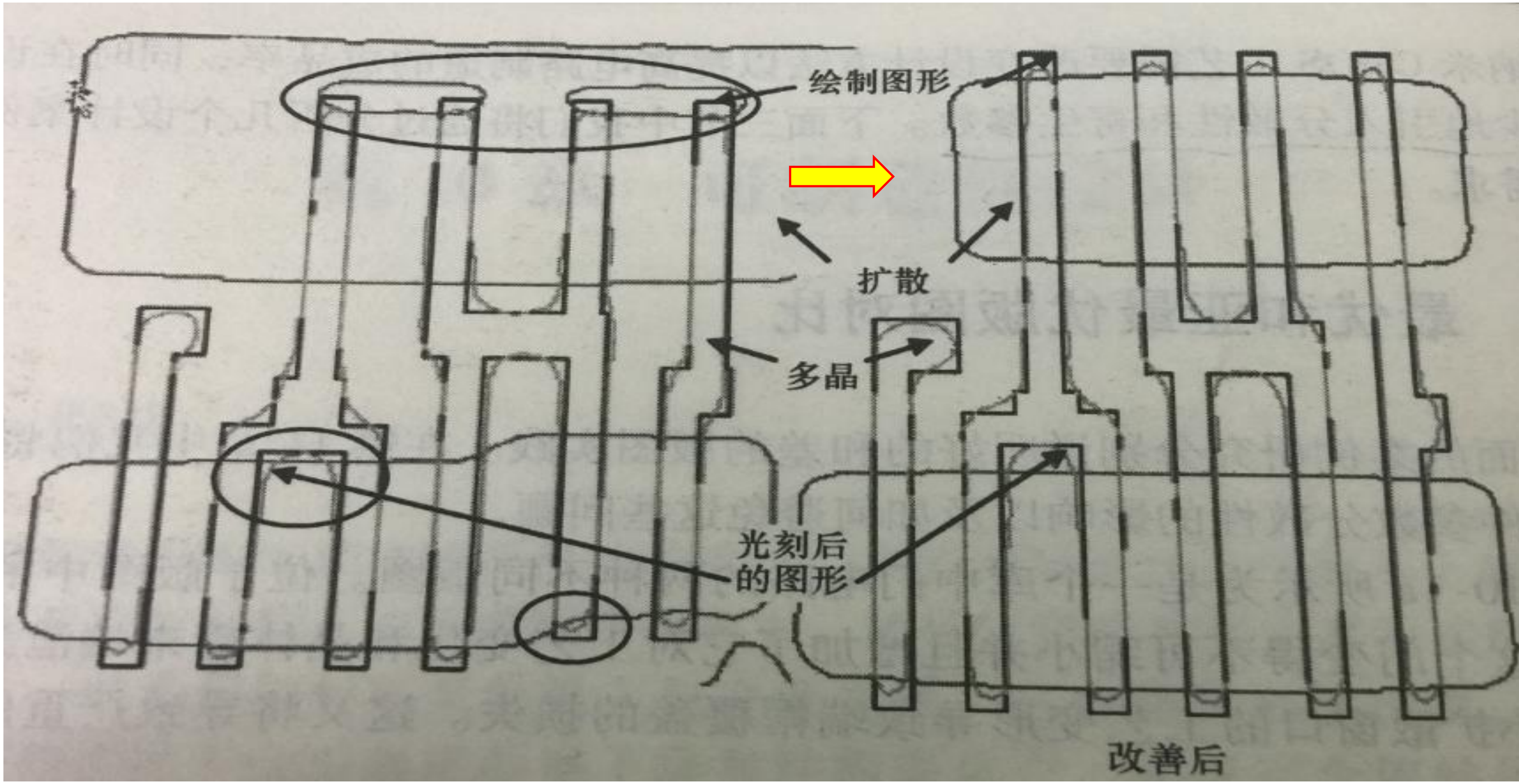


多晶硅末端
覆盖不充分
产生泄漏
扩散形
状扭曲
工艺加
工后的
宽度
设计的
宽度
绘制的晶体管
光刻与刻蚀后，
这样的版图会
导致宽度增加
改善后的版图

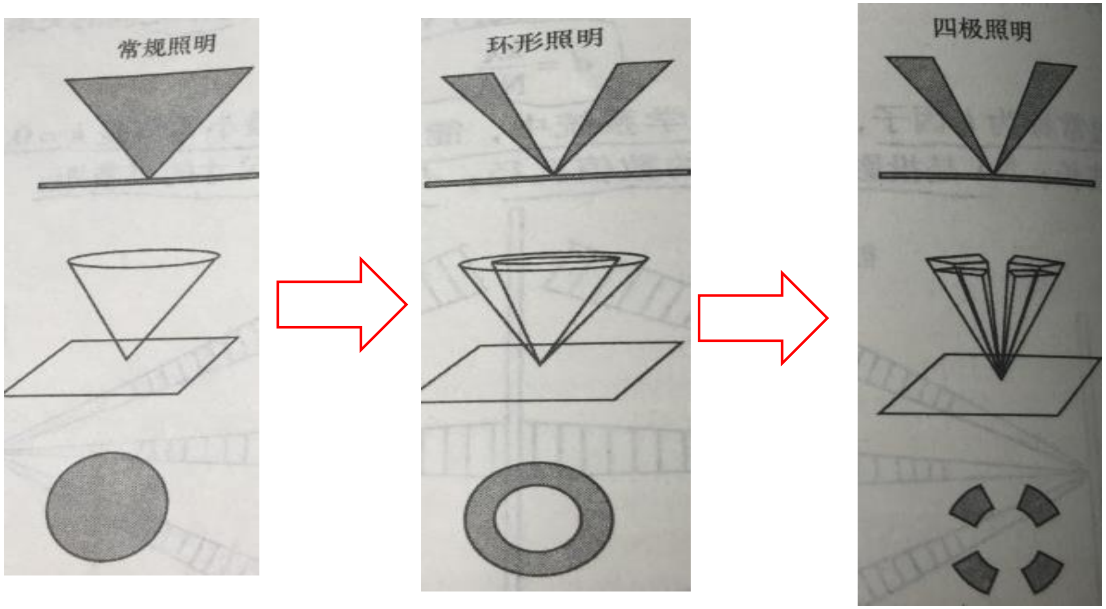


多晶图形光刻后直角弧化
引起到接触孔的短路

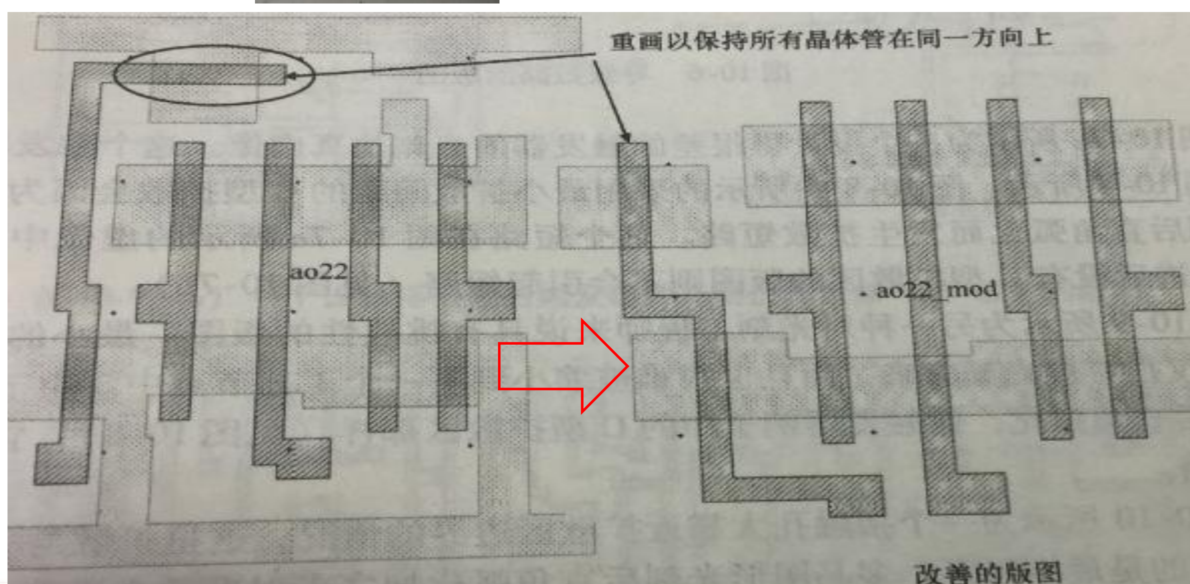
版图改善：例



四极照明：100nm工艺光学分辨率增强

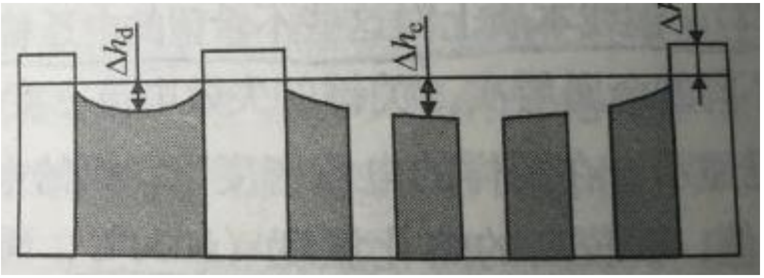


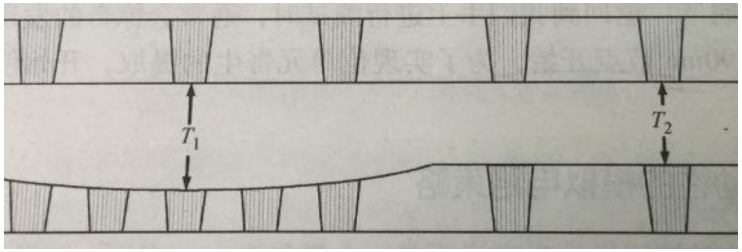
消除对图形形成没有贡献的光线，增加对比度



四极照明要求MOS版图摆放方向一致

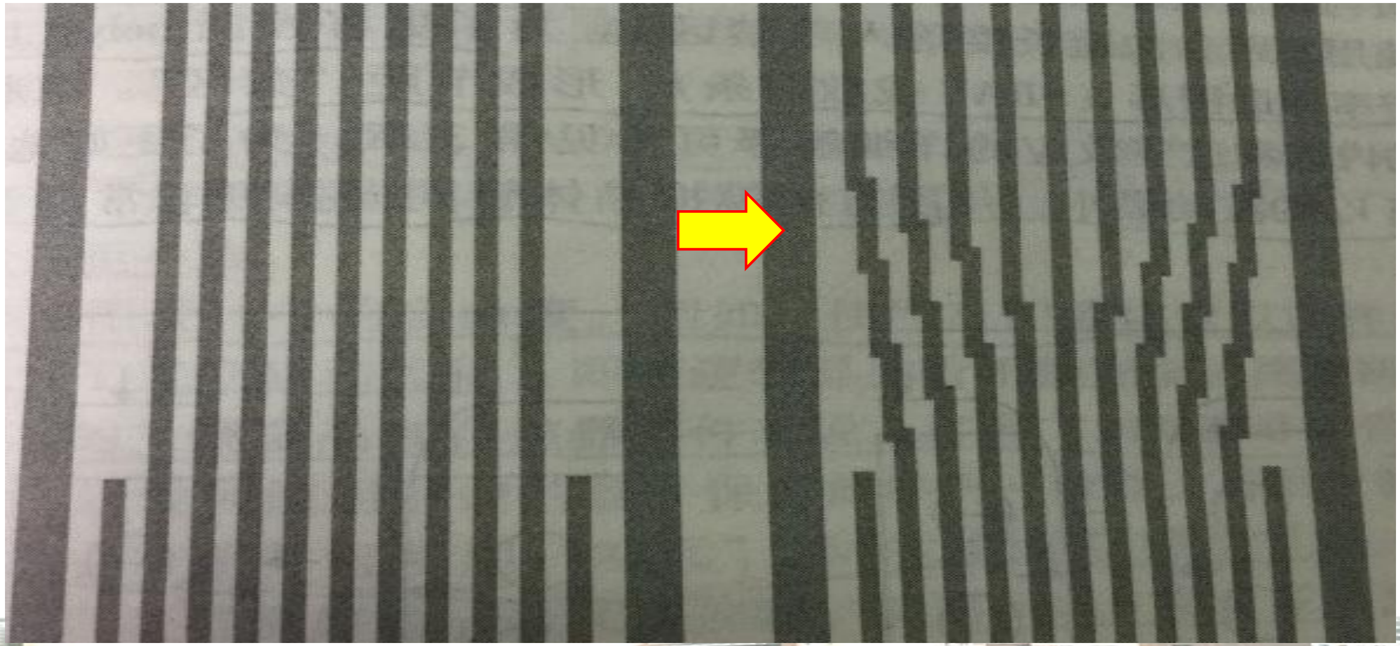
铜工艺（0.13um工艺后)金属层连线





化学机械抛光CMP后铜厚度损失

版图改进



最 优 线 宽
3~5um

4.4 MOS为负载的差动对

- 差动增益可用半边电路（参考图3.12和式3.42）

$$A_{DM} = -g_{mN}\left(\frac{1}{g_{mP}} \| r_{oP} \| r_{oN}\right) \approx -\frac{g_{mN}}{g_{mP}}$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_{D1}}$$

- 平衡点附近

$$A_{DM} \approx -\frac{g_{mN}}{g_{mP}} = \sqrt{\frac{\mu_{n\,ox}\left(\frac{W}{L}\right)_N}{\mu_n\left(\frac{W}{L}\right)_P}} \qquad (4.51)$$

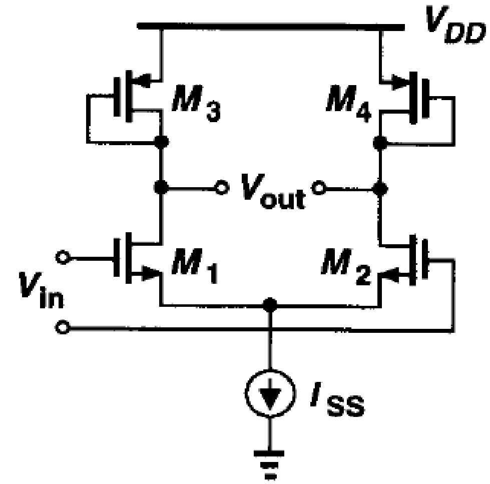


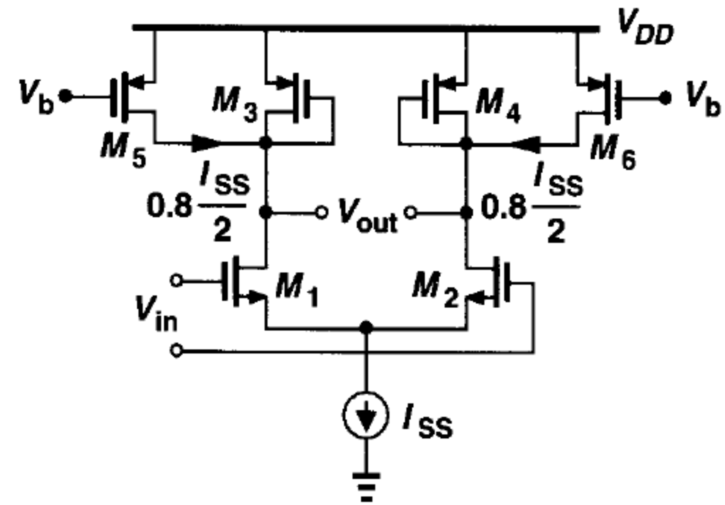
图4.32(a)以二极管为负载的差动对

注意增益方向：输入输出同侧为-，异侧为+

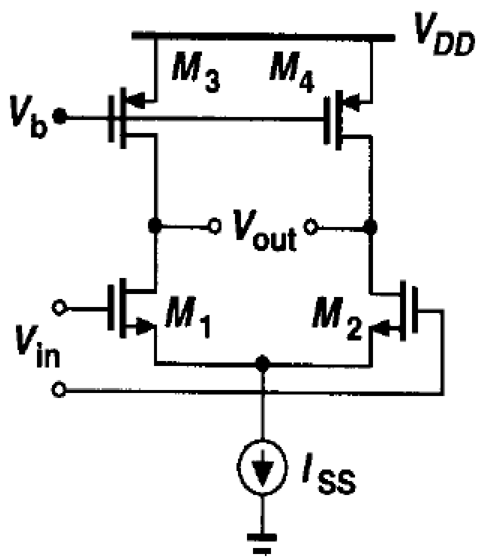
- 二极管负载减少了输出电压余度。
- 要增大增益，需减小(W/L)p，从而|VGSP-VTHP|增大，X和Y点允许的共模电平下降。

MOS为负载的差动对

Figure 4.33 Addition of current sources to increase the voltage gain.



采用减少电流而不是减少宽度的方法减小负载PMOS的 gm,见（式4.51）



由式（3.43）

$$A_{DM} = -g_{mN}(r_{oP} \parallel r_{oN})$$

图4.32(B)电流源负载差动对

以电流源为负载的差动对的小信号增益

$$A_{DM} = -g_{mN}(r_{oP} \parallel r_{oN})$$

一般为几十，可用cascode增大增益（实质是增大输出阻抗,注意后级的输入阻抗要大）。

采用cascode差动对提高增益

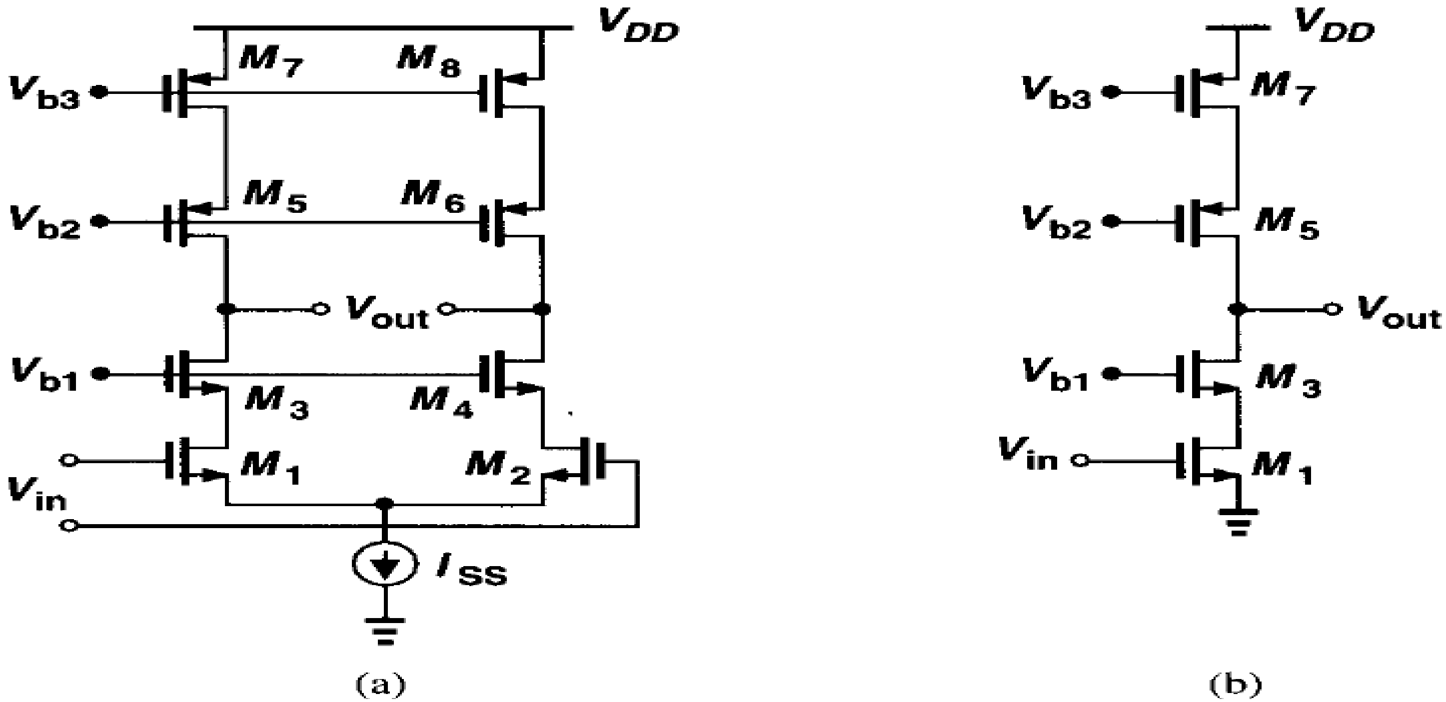


Figure 4.34 (a) Cascode differential pair, (b) half circuit of (a).

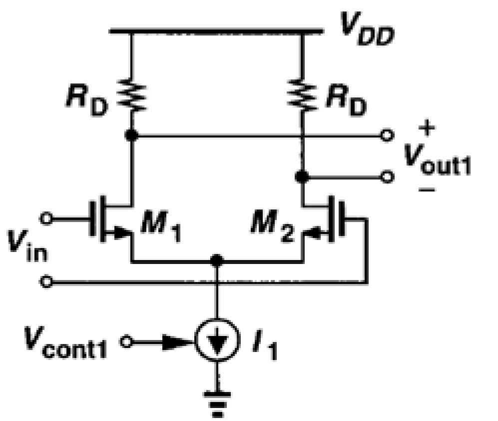
- 缺点是减少了输出电压余度，只适合小信号放大。
- 注意：电流源负载差动放大必须用某种方法确定输出共模电平;
- 二极管负载结构的图4.32(a)和图4.33输出共模电平是确定的，为

$$V_{DD}-V_{SGP}$$

吉尔伯特单元 Gilbert cell：乘法器

实现$\Delta V_{out} = k\Delta V_{cout}\Delta V_{in} = k(V_{cont\,2} - V_{cont\,1})\Delta V_{in}$

考察



$$小信号\ g_m = \sqrt{\mu C_{ox}(\frac{W}{L})_1 I_1}$$

$$= \sqrt{\mu C_{ox}(\frac{W}{L})_1 \times \frac{1}{2}\mu_n C_{OX}(\frac{W}{L})_{cont\,1}(V_{cont\,1} - V_{TH})^2}$$

$$= \mu C_{ox}\sqrt{\frac{1}{2}(\frac{W}{L})_1(\frac{W}{L})_{cont\,1}}(V_{cont\,1} - V_{TH})$$

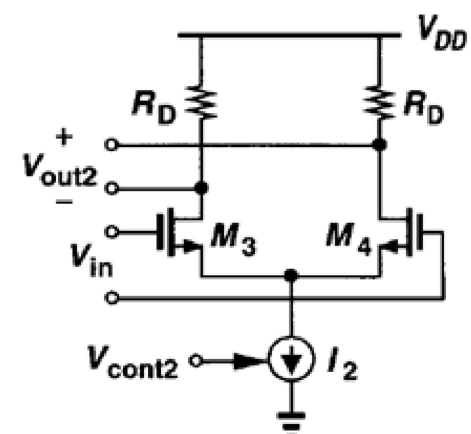
$$A_1 = -g_m R_D = -k(V_{cont1} - V_{TH})$$

小信号增益是尾电流的函数，
Vcont控制尾电流

$$\Delta V_{out} = k(V_{cont\,2} - V_{cont\,1})\Delta V_{in}$$

$$= k(V_{cont\,2} - \mathrm{V_{TH}} - V_{cont\,1} + \mathrm{V_{TH}})\Delta V_{in}$$

$$= -k(V_{cont\,1} - \mathrm{V_{TH}})\Delta V_{in} + k(V_{cont\,2} - \mathrm{V_{TH}})\Delta V_{in}$$



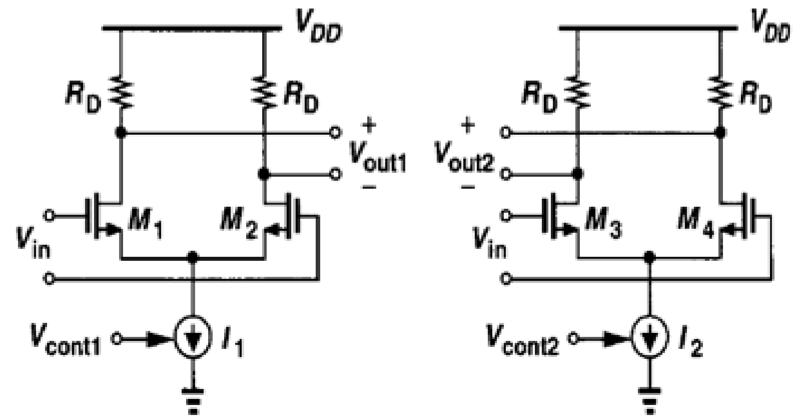
Gilbert cell：电路演变

如何实现 $\Delta V_{out} = k(V_{cont2} - V_{cont1})\Delta V_{in}$

$= -k(V_{cont1} - V_{TH})\Delta V_{in} + k(V_{cont2} - V_{TH})\Delta V_{in}$

注意 V_{out2}方向

差动输出Vout= Vout1+ Vout2



Vin相同， Vout1和 Vout2反相

大信号分析：

差动输出 $V_{out1} = [V_{DD} - R_D I_{D1}] - [V_{DD} - R_D I_{D2}]$

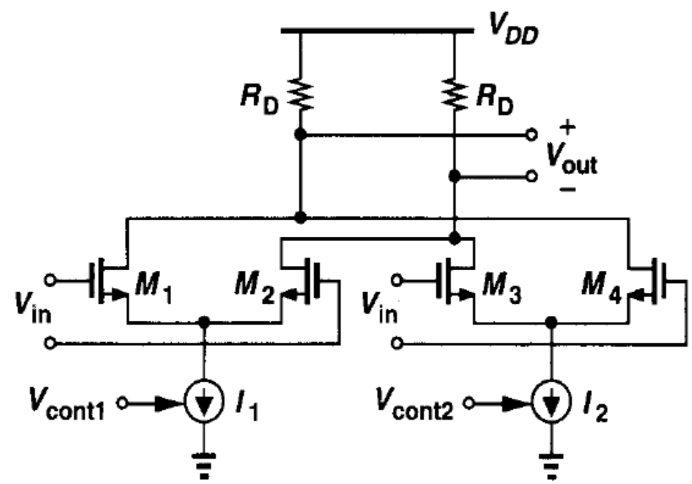
$= R_D(I_{D2} - I_{D1})$

差动输出 $V_{out2} = [V_{DD} - R_D I_{D4}] - [V_{DD} - R_D I_{D3}]$

$= R_D(I_{D3} - I_{D4})$

$V_{out} = V_{out1} + V_{out2} = R_D(I_{D2} - I_{D1}) + R_D(I_{D3} - I_{D4})$

$= R_D(I_{D2} + I_{D3}) - R_D(I_{D1} + I_{D4})$，如何实现？



$V_{out} = [V_{DD} - R_D(I_{D1} + I_{D4})] - [V_{DD} - R_D(I_{D2} + I_{D3})]$

$= R_D(I_{D2} - I_{D1}) + R_D(I_{D3} - I_{D4}) = V_{out1} + V_{out2}$

Gilbert cell 电路结构

交变信号$\Delta V_{out} = V_{out} = k(V_{cont2} - V_{cont1})\Delta V_{in} = k\Delta V_{cont} \times \Delta V_{in}$

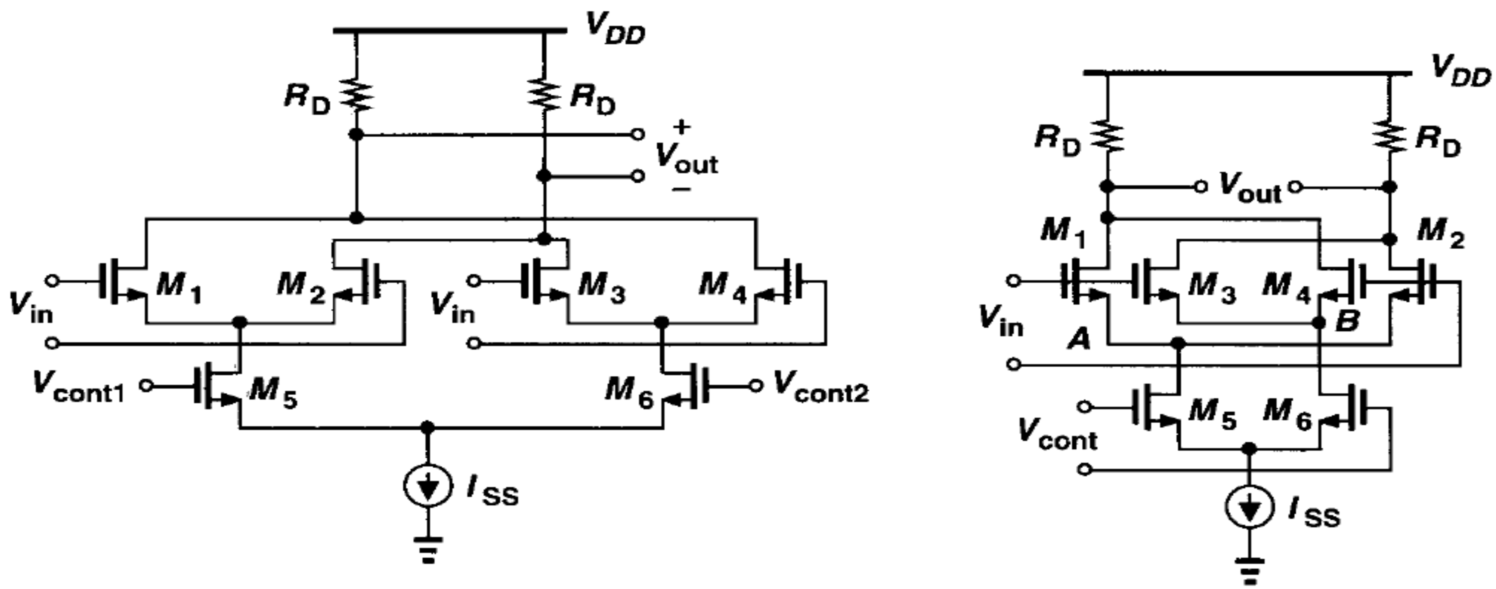


Figure 4.36 (c) use of M_5-M_6 to control the gain, (d) Gilbert cell.

- 吉尔伯特单元 可作为乘法器和Mixer，什么信号之间隔离较好？
- 输入交变信号很大时，输出中含有其它非理想混频信号和杂散信号