# A W-Band 6-Bit Phase Shifter With 7 dB Gain and 1.35° RMS Phase Error in 130 nm SiGe BiCMOS

Huanbo Li, Jixin Chen, *Member, IEEE*, Debin Hou, *Member, IEEE*, and Wei Hong, *Fellow, IEEE*

***Abstract*—This brief presents a W-band 6-bit active phase shifter fabricated in 0.13 $\mu$m SiGe BiCMOS process. A wideband quadrature signal generator composed of a 90-degree hybrid and a pair of transformers is exploited for low insertion loss and superior balance. Conventional architecture used in gain control unit is replaced by a novel phase inverter-embedded variable gain amplifier to achieve a high gain and low complexity. In addition, a balun-first combiner with symmetrical layout is utilized at the output to keep as low the imbalance of I/Q paths as possible. The proposed phase shifter exhibits a record average gain of 7 dB at 79 GHz with a 3-dB bandwidth from 71.5 to 84.5 GHz. The variation of gain remains below 2.1 dB over 64 phase states. The measured RMS phase error is 1.35° at 78 GHz and remains below 3.5° from 72 to 82 GHz. The RMS gain error is measured to be 0.46 dB at 75 GHz and keeps less than 0.76 dB from 71 to 82 GHz. The measured input 1dB compression point amounts to −10 dBm. To the best of the author's knowledge, this brief presents the lowest RMS phase error (1.35°) and the highest gain (7 dB) compared with the reported silicon-based W-band active phase shifters.**

***Index Terms*—Millimeter wave (mm-wave), phase shifter, quadrature coupler, SiGe, variable gain amplifier, vector synthesis, W-band.**

## I. Introduction

In RECENT years, phased array technique has been an attractive solution to various millimeter-wave applications, such as 5G cellular communication and autonomous radar [1]–[11]. By controlling the direction of wave beams, phased arrays can achieve higher data rate transmission and higher detection precision with wider detection area. Digital beam forming architecture is not appropriate for large-scale antenna array due to high power consumption and considerable computation load at the baseband [2]–[4]. Therefore, phase shifting in the RF path is more feasible to implement and have been widely applied in phased array system.

Phase shifters are crucial components in phased-array systems to provide phase shifting, which can be classified into passive form and active form. Passive structures typically exhibit high linearity and low power consumption, at the expense of high loss and large area [1], [2]. Active phase shifters based on vector summing exhibit higher gain, smaller area and full phase shifting range [3]–[10], [12]. Small phase-shifting steps can be realized by controlling the gains of I/Q paths through high resolution DACs. However, active structures have defects in poor linearity performance and high power consumption. Several active phase shifters operating in V-band or W-band have been reported [3]–[7], [9], [10]. However, most of them exhibit a low gain, typically smaller than 0 dB, with a large RMS phase error comparable to that of passive counterparts.

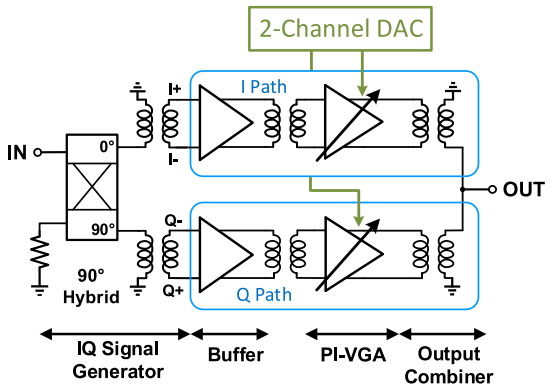


Fig. 1. Block Diagram of the W-band 6-bit phase shifter.

In this brief, a new architecture named as phase inverter-embedded variable gain amplifier (PI-VGA) is proposed to control the gain of I/Q paths. Compared with conventional control units, PI-VGA achieves a larger available gain with over 18.6-dB gain tuning range. In addition, Phase inverter-embedded architecture reduces the design complexity because no extra phase-selecting circuit in the RF path is required. Based on the proposed PI-VGA, our work devises a 6-bit phase shifter with over 7-dB gain and a small RMS phase error of 1.35° around 78 GHz.

This brief is organized as follows. In Section II, the detailed circuit design of all blocks is addressed. Section III shows the measurement results and the comparison with other reported designs. The conclusions are drawn in Section IV.

## II. Design of W-Band Phase Shifter

The proposed phase shifter is fabricated in 0.13 $\mu$m SiGe BiCMOS process, featuring a $f_T/f_{MAX}$ of 200 GHz/250 GHz. Fig. 1 depicts the block diagram of the circuit, consisting of an I/Q signal generator, a pair of PI-VGAs with buffers and an output combiner. A 2-channel digital-to-analog convertor (DAC) with 8-bit resolution is implemented to carefully control the gain of I/Q paths.

### A. IQ Signal Generator

As we know, the phase error and amplitude imbalance of the quadrature signals have significant impacts on the overall

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The authors are with the State Key Laboratory of Millimeter Waves, Southeast University, Nanjing 210096, China (e-mail: jxchen@seu.edu.cn).

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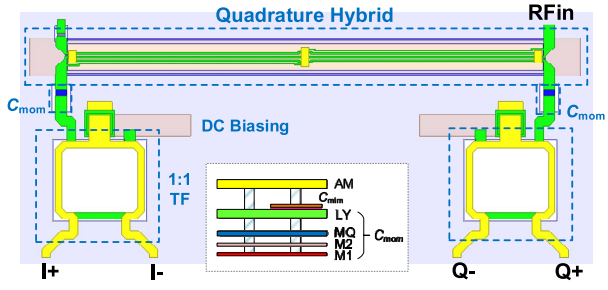



Fig. 2. 3D Layout of the I/Q signal generator.

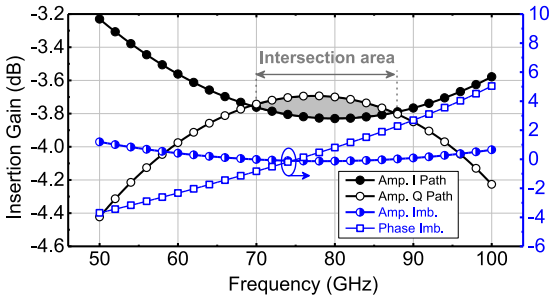



Fig. 3. Simulated (a) insertion again and (b) insertion phase of the separate lange coupler.

performance including phase resolution, RMS phase error and gain deviation [7], [10]. To achieve 6-bit accuracy, the phase error and amplitude imbalance have to be restricted to 2.5° and 1 dB, respectively.

The I/Q signal generator utilized in this brief is composed of a 90° hybrid and two transformers (TFs), as shown in Fig. 2. Lange coupler is selected over spiral coupler for its symmetrical layout and ultra-wideband characteristic. Fig. 3 shows the EM simulation results of the separate lange coupler. It can be seen that there exists a flat intersection area between the gain curves of I and Q paths, which leads to a wide operating bandwidth. The separate lange coupler achieves a insertion gain of −3.8 dB with over 20-GHz available bandwidth. The amplitude and phase imbalances are less than ±0.1 dB and ±2.5° from 65 to 90 GHz, respectively.

A pair of TFs, together with two customized capacitors, is exploited to transform the single-ended source impedance (50 Ohm) to the differential input impedance ($Z_{in,diff}$) of the following stage (27-$j$42 Ohm). It is noteworthy that $Z_{in,diff}$ varies with different phase states, therefore the I/Q signal generator should bear load variation. Fig. 4(a) shows the simulated average gain and RMS amplitude imbalance of the 4-way quadrature outputs with ±20% variation of $Z_{in,diff}$. The RMS phase error of the four outputs is plotted in Fig. 4(b). It can be clearly seen that changes in $Z_{in,diff}$ have minor impacts on the loss and signal balance, which reveals that the proposed I/Q signal generator exhibits robust performance.

### B. Gain Control Unit

Gain control unit is the key cell in active phase shifter. The four topologies of gain control unit shown in Fig. 5 are analyzed to compare their pros and cons. The first architecture called Gilbert-based analog adder has been widely applied in numerous reported designs [5], [9], [10], as shown in Fig. 5(a). In I path, the amplitude of vectors is controlled by the tail current in the lower transistor ($I_{t\_I}$) and the polarities are inverted by a SPDT digital switch (SI and SIN) at

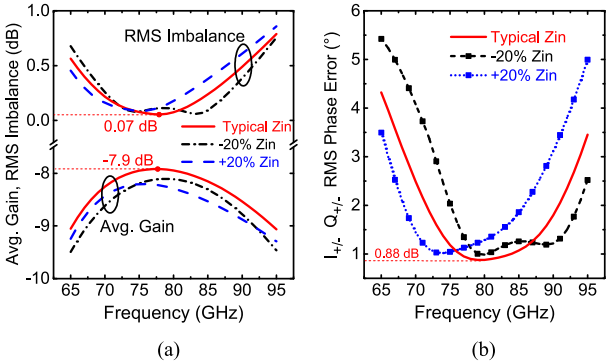



Fig. 4. Simulated characteristics of the IQ signal generator with ±20% variation of $Z_{in,diff}$. (a) Average gain and RMS amplitude imbalance. (b) RMS phase error.

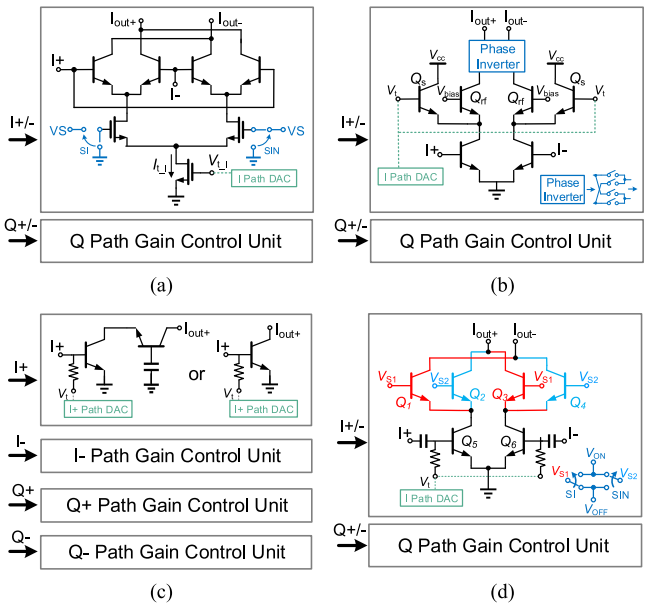



Fig. 5. Gain control units comparison. (a) Gilbert-based analog adder. (b) current steering VGA with phase inverter. (c) 4-way single-ended VGA with 4-channel DACs. (d) Proposed PI-VGA.

the middle transistor pair. This classical architecture with only one stage is compact, whereas it suffers from low gain, low isolation and huge variation of input and output impedance with different gain states. Current steering technique [4], [6], as shown in Fig. 5(b), is operated by tuning the current through the cascode (CC) transistor $Q_s$, so that the gain is changed. Although current steering exhibits superior gain and low input impedance variations, an extra phase inverter is required to implement polarity switching [6]. The architecture in Fig. 5(c) consists of four independent units. The gains of four quadrature paths are tuned separately by four identical single-ended VGAs. This architecture requires 4-channel high resolution DACs, which considerably increases the complexity of digital units.

In this brief, a new architecture named as phase inverter-embedded variable gain amplifier (PI-VGA) is proposed, as shown in Fig. 5(d). PI-VGA consists of a pair of differential CC amplifiers to achieve gain tuning and 180° phase reversal. The CE stage is shared while the upper two pairs of common-base (CB) transistors work alternately. By switching $V_{S1}$ and $V_{S2}$ to $V_{ON}$ ($V_{OFF}$) and $V_{OFF}$ ($V_{ON}$), respectively, we can enable either pair of CB transistors to operate and

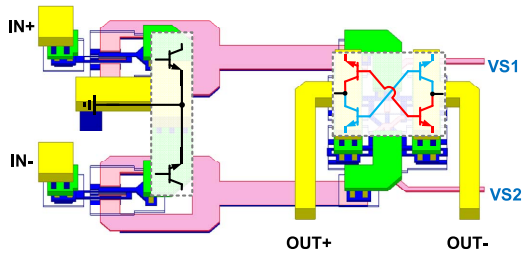
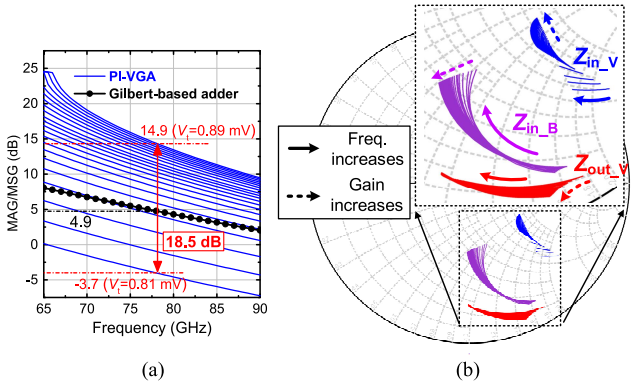



Fig. 6. 3D Layout of PI-VGA.




(a) (b)

Fig. 7. Simulated (a) MAG/MSG, (b) $Z_{in\_V}$, $Z_{in\_B}$ and $Z_{out\_V}$ with changing $V_t$.

further realize full 360° phase shifting. For instance, if $V_{S1}$ and $V_{S2}$ are equal to $V_{ON}$ and $V_{OFF}$, respectively, $Q_1$ and $Q_3$ are active while the currents through $Q_2$ and $Q_4$ are negligible, thus $Q_1$, $Q_3$, together with $Q_5$ and $Q_6$ comprise a differential CC amplifier with a negative amplification coefficient. PI-VGA does not demand an extra phase inverter in the RF path, which simplifies the system complexity. The gain tuning is operated by controlling the base voltage of $Q_5$ and $Q_6$, through an 8-bit DAC. All the transistors in PI-VGA are sized to be 5×0.13 $\mu$m$^2$and each PI-VGA consumes 8 mA from a 3.3 V supply. Fig. 6 shows the 3D layout of PI-VGA.

From the principle of vector synthesis, the required dynamic range of the VGA ($R_v$) to achieve N-bit phase resolution can be expressed as, $R_v = \tan(2\pi/2^N)$. Therefore, for a 6-bit phase resolution, the gain tuning range of VGA should exceed 10 dB. Fig. 7(a) shows the maximum available (stable) gain (MAG/MSG) of PI-VGA with changing $V_t$. It is evident that PI-VGA can achieve over 18-dB gain tuning range which is enough to achieve 6-bit resolution. In addition, the simulated highest MSG that conventional Gilbert-based adder architecture can achieve is plotted in Fig. 7(a). It can be derived that PI-VGA exhibits higher MSG (14.9 dB at 77 GHz) compared with Gilbert-based adder (4.9 dB at 77 GHz), thanks to its CC configuration. Another notable issue, as mentioned earlier, is the variation of the input impedance. As shown in Fig. 7(b), the differential input impedance of a separate PI-VGA ($Z_{in,V}$) exhibits quite large variations, which causes deterioration in phase synthesizing accuracy. Thus, a buffer stage with 5-dB gain in CE configuration is inserted before PI-VGA, as shown in Fig. 7(b). The transistors in buffer are scaled as the same width as those in PI-VGA and biased in AB-class under 1.5 V supply. A transformer with 1:1 turn ratio is adopted to connect the two blocks and implement impedance transforming. The input impedance looking at the buffer ($Z_{in,B}$) and the output impedance ($Z_{out\_V}$) of PI-VGA are plotted in Fig. 7(b).

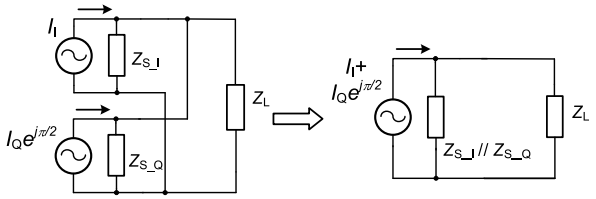
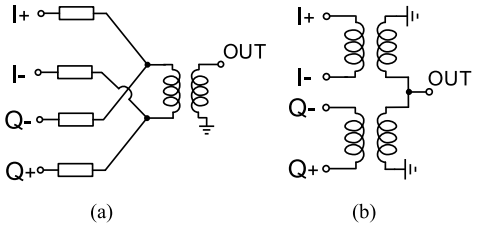



Fig. 8. Schematic of I/Q signals combining.




(a) (b)

Fig. 9. (a) Conventional TL-first combiner. (b) Proposed TF-first combiner.

Compared with $Z_{in,V}$, $Z_{in,B}$ is more stable with different gain states, at the expense of bandwidth. $Z_{out\_V}$ is insensitive to gain variation, thus output buffer is dispensable.

### C. Output Combiner

4-way modulated I/Q vectors are summed at the output and converted to a single-ended signal. The optimum load impedance of the I/Q sources and the transmission coefficient are worth investigating. According to Norton's theorem, two orthogonal sources can be simplified to one source, as shown in Fig. 8, and the power at ZL can be expressed as

$$P_L = \frac{1}{2}|I_L|^2\mathrm{Re}(Z_L) = \frac{1}{2}|I_S|^2\left|\frac{Z_S}{Z_S+Z_L}\right|^2\mathrm{Re}(Z_L)$$
$$= \frac{1}{2}\left(I_I^2+I_Q^2\right)\left|\frac{Z_S}{Z_S+Z_L}\right|^2\mathrm{Re}(Z_L) \quad (1)$$

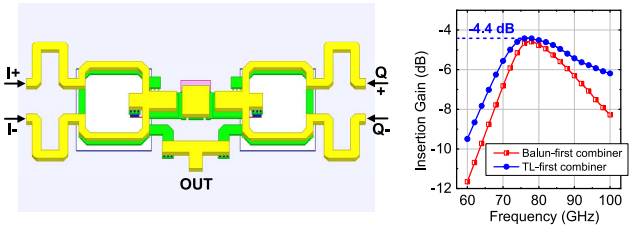
where $I_S$ represents the overall source current, equal to $I_I$+$I_Q e^{j\pi/2}$, and $Z_S$ is the equivalent source impedance, equal to $Z_I$//$Z_Q$. Therefore, the maximum power delivered to the load is obtained when $Z_L = Z_S^*$, which is known as the conjugate matching. The ratio of the maximum transmission coefficient of two quadrature sources to two in-phase sources can be expressed as $R_{mt} = (I_I^2+I_Q^2)/(I_I^2+I_Q^2+2I_II_Q)$ which means that quadrature combining induces a 3-dB loss when the amplitude of $I_I$ and $I_Q$ are the same.

In most of the state-of-the-art active phase shifters, the 4-way vectors are added at first and the acquired differential signal is converted to single-ended output by a balun [4]–[10], [12] as shown in Fig. 9(a). However, this structure suffers from asymmetrical layout because the transmission lines (TLs) usually intersect [5]–[8], [12]. In this brief, a balun-first combiner is adopted, as shown in Fig. 9(b), for the following reasons.

1) Contrive a layout-symmetrical output network to keep as low as possible the imbalance of the I/Q paths, and hence improve the accuracy of phase shifting.

2) Long TLs used for connecting the balun and PI-VGA can be removed or meandered, and hence save the area and extend the bandwidth.

Fig. 10(a) shows the 3D-layout of the proposed output combiner, which occupies an area of 300×150 $\mu$m$^2$. The simulated insertion gains of both the balun-first combiner




(a) (b)

Fig. 10. (a) 3D Layout and (b) simulated insertion gains of output combiner.

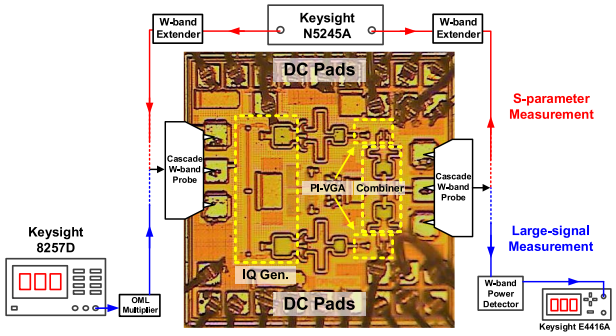



Fig. 11. Micrograph of the W-band phase shifter and measurement setup.

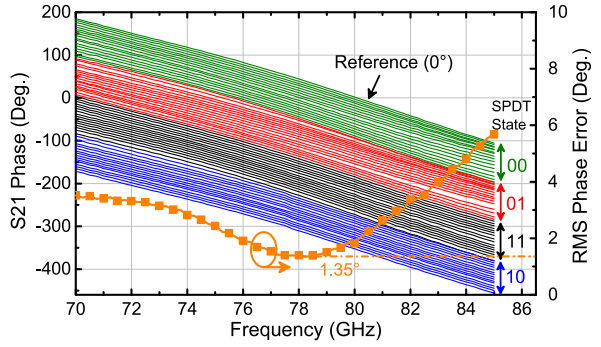



Fig. 12. Measured phase shifts over 64 phase states and RMS phase error.

and TLs-first combiner are plotted in Fig. 10(b) (the power of I and Q sources is the same), the balun-first combiner exhibits a smaller loss of 4.4 dB with a larger bandwidth.

## III. Fabrication and Measurement

Fig. 11 shows the micrograph of the fabricated phase shifter, occupying an area of 910 $\mu$m×900 $\mu$m. The core area excluding pad is only 0.31 mm$^2$ and the dc power consumption is 60 mW.

The measurement setup is demonstrated in Fig. 11. The S-parameter measurement involves a Keysight N5245A vector network analyzer with OML W-band (75-110 GHz) extenders. The dc pads are bonded to a printed circuit board (PCB) and then connected to a voltage source or a microcontroller, whereas the mm-wave pads are probed. Large-signal characteristic measurement is implemented by Keysight 8257D signal source (followed by an OML multiplier) and a Keysight E4416A power meter.

The measured phase shifts for the 64 phase states are shown in Fig. 12. The phase shifter provides a phase tuning range of 360° with 6-bit resolution. Different quadrants shifting is implemented by four combination states of SPDT, labeled as "00", "01", "11", "10". The RMS phase error is 1.35° at 78 GHz and remains below 3.5° from 72 to 82 GHz.

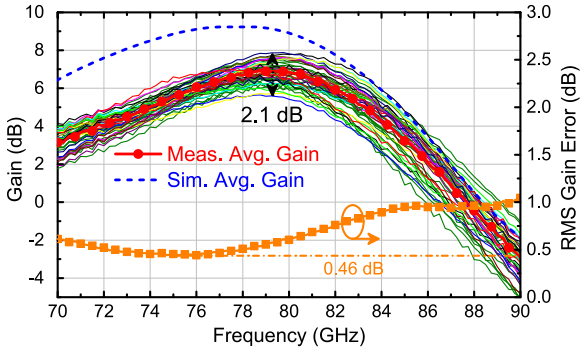
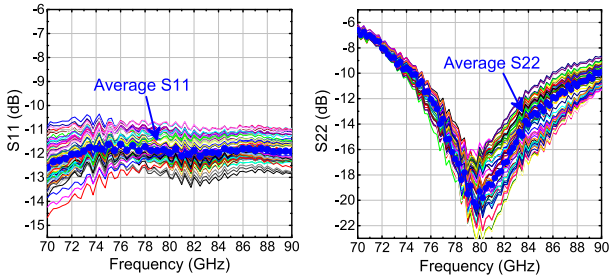



Fig. 13. Measured insertion gain over 64 phase states and RMS gain error.




(a) (b)

Fig. 14. Measured (a) $S_{11}$ and (b) $S_{22}$ over 64 phase states.

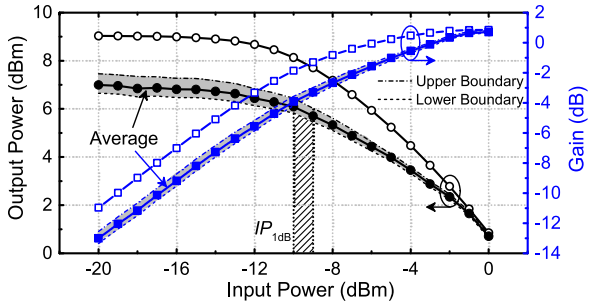



Fig. 15. Measured $P_{\text{out}}$, conversion gain and $IP_{1\text{dB}}$.

The measured 16-state gain and their average value are plotted in Fig. 13. The proposed phase shifter exhibits a peak average gain of 7 dB at 79 GHz with a 3-dB bandwidth from 71.5 to 84.5 GHz. The conversion gain varies by only 2.1 dB across all phase states. A 2.5-dB difference is observed between the measured and simulated gain from 70 to 78 GHz, which may results from the model inaccuracy and process variation. The RMS gain error amounts to 0.46 dB at 75 GHz and is less than 0.76 dB from 71 to 82 GHz.

Fig. 14(a) and Fig. 14(b) show the measured $S_{11}$ and $S_{22}$, respectively. $S_{11}$ remains below than −10 dB over the entire interested frequency range, benefiting from the wideband I/Q generator. $S_{22}$ is better than −10 dB from 74.5 to 90 GHz. The simulated average noise figure is 14.2 dB at 75 GHz and remains below 16 dB from 64 to 85 GHz.

The measured output power ($P_{\text{out}}$) and conversion gain as a function of the input power ($P_{\text{in}}$) are presented in Fig. 15. The measured input-referred 1 dB compression point ($IP_{1\text{dB}}$) amounts to −10 dBm at 79 GHz and varies less than ±0.5 dB with different phase states.

The comparison with other state-of-the-art silicon-based phase shifters operating in V-band or W-band is summarized in Table I. Considering the power consumption, we modify the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER STATE-OF-THE-ART SILICON-BASED PHASE SHIFTERS

| Reference | [4] | | [5] | [6] | [7] | [8] | [9] | **This Work** |
|---|---|---|---|---|---|---|---|---|
| Technology | 28 nm FDSOI | 28 nm FDSOI | 0.13 μm SiGe | 40 nm CMOS | 90 nm CMOS | 40 nm CMOS | 45nm SOI CMOS | **0.13 μm SiGe** |
| Architecture | Vector Modulator | Vector Modulator | Vector Modulator | Vector Modulator | Vector Modulator | Hybrid | Vector Modulator | **Vector Modulator** |
| Frequency (GHz) | 78.8-92.8 | 80.2-96.8 | 74-92 | 58-62 | 57-64 | 52-57 | 57.7-84.2 | **71.5-84.5** |
| Phase Resolution (bits) | 4 | 4 | 5 | 7 | 4 | 6 | 5 | **6** |
| Peak Average Gain (dB) | 2.3 | 0.83 | -4 | -0.4 | 1.1 | -9 | -4 | **7** |
| RMS Gain error (dB) | 1.68-2 | 1.46-2 | 1.5 | 0.13-0.5 | 0.75-1.6 | 2.07-2.23 | 0.8-1.1 | **0.46-0.76 @ 71-82 GHz** |
| RMS Phase error (°) | 9.4-11.9 | 11.2-11.9 | 8-11 | 1.4-2.7 | 2.3-7.6 | 2.8-3.76 | 2.7-10.1 | **1.35-3.5 @ 72-82 GHz** |
| $S_{11}$ (dB) | <-10.5 | <-11.5 | - | <-10 | <-10 | <-8 | <-10 | **<-10** |
| $S_{22}$ (dB) | <-7 | <-7 | - | <-9 | <-10 | <-4 | <-5 | **<-10 @ 74.5-90 GHz** |
| Noise Figure (dB) | 10.8 | 11.9 | 15 | - | - | - | - | **14.2*** |
| Input $P_{1dB}$ (dBm) | -7 | -6 | 4* | -6.9 | 9.7 | >10 | 5 | **-10** |
| Power Consumption (mW) | 21.6 | 21.6 | 28 | 38 | 19.8 | 14.3 | 17 | **60** |
| FOM | 20.4 | 17.6 | 6.7 | 34.9 | 40 | 3.2 | 20.4 | **99.7** |
| FOM1 | 440.7 | 380.2 | 186.8 | 1327 | 792 | 46 | 346 | **5983** |
| FOM2 | 0.37 | 0.31 | 0.39 | - | - | - | - | **0.39*** |
| Area ($mm^2$) | 0.12[a] | 0.06[a] | - | 1.13 | 0.61 | 0.15[a] | 0.11[a] | **0.82(0.31[a])** |

$$\text{FOM1}=\frac{f_0(\text{GHz})\cdot G(\text{abs})\cdot B_{3\text{dB}}(\text{GHz})\cdot \text{Resolution(bits)}}{\text{RMS Phase Error in } B_{3\text{dB}}(\text{deg.})\cdot \text{RMS Gain Error in } B_{3\text{dB}}(\text{abs})} \qquad \text{FOM}=\text{FOM1}/P_{\text{DC}}(\text{mW})$$

* simulation, [a] core area

$$\text{FOM2}=\frac{f_0(\text{GHz})\cdot G(\text{abs})\cdot B_{3\text{dB}}(\text{GHz})\cdot IP_{1\text{dB}}(\text{mW})\cdot \text{Resolution(bits)}}{\text{RMS Phase Error in } B_{3\text{dB}}(\text{deg.})\cdot \text{RMS Gain Error in } B_{3\text{dB}}(\text{abs})\cdot P_{\text{DC}}(\text{mW})\cdot (NF(\text{abs})-1)}$$

figure of merit (FOM) based on FOM1, referred in [4]. FOM1, FOM2 in [4] and FOM are all listed to weigh the performance of phase shifters. The proposed phase shifter exhibits excellent FOMs among all the works in Table I. It is noteworthy that the design in this brief achieves the highest average peak gain of 7 dB with a 13 GHz bandwidth. Furthermore, the 6-bit phase shifter demonstrates the lowest RMS phase error and quite small RMS gain error while consuming an acceptable chip area.

## IV. CONCLUSION

This brief presents a 6-bit W-band active phase shifter fabricated in 0.13 $\mu$m SiGe BiCMOS process. A 90° hybrid and a pair of transformers are adopted to form a wideband I/Q signal generator. The gain control unit is composed of a pair of novel PI-VGAs for high gain and low complexity. A balun-first combiner with a symmetrical layout is utilized at the output. The proposed phase shifter exhibits a record average insertion gain of 7 dB at 79 GHz with a 3-dB bandwidth of 13 GHz. The minimum RMS phase error and gain error are measured to be 1.35° at 78 GHz and 0.46 dB at 75 GHz, respectively. With excellent performance and a competitive size, the presented circuit is appropriate for mm-wave communication system and W-band autonomous radar.

## ACKNOWLEDGMENT

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## REFERENCES

[1] H.-S. Lee and B.-W. Min, "W-band CMOS 4-bit phase shifter for high power and phase compression points," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 1, pp. 1–5, Jan. 2015.

[2] S. Y. Kim and G. M. Rebeiz, "A low-power BiCMOS 4-element phased array receiver for 76–84 GHz radars and communication systems," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 359–367, Feb. 2012.

[3] T. Shimura, Y. Ohashi, and T. Ohshima, "A 76–81 GHz active phase shifter for phased array automotive radar in 65nm CMOS," in *Proc. Eur. Microw. Integr. Circuits Conf.*, Nuremberg, Germany, Oct. 2013, pp. 252–255.

[4] D. Pepe and D. Zito, "Two mm-wave vector modulator active phase shifters with novel IQ generator in 28 nm FDSOI CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 344–356, Feb. 2017.

[5] B.-H. Ku, O. Inac, M. Chang, H.-H. Yang, and G. M. Rebeiz, "A high-linearity 76–85-GHz 16-element 8-transmit/8-receive phased-array chip with high isolation and flip-chip packaging," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2337–2356, Oct. 2014.

[6] B. Wang, H. Gao, M. K. Matters-Kammerer, and P. G. M. Baltus, "A 60 GHz 360° phase shifter with 2.7° phase resolution and 1.4° RMS phase error in a 40-nm CMOS technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Philadelphia, PA, USA, Jun. 2018, pp. 144–147.

[7] Y. Yu *et al.*, "A 60-GHz 19.8-mW current-reuse active phase shifter with tunable current-splitting technique in 90-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 5, pp. 1572–1584, May 2016.

[8] X. Quan *et al.*, "A 52–57 GHz 6-bit phase shifter with hybrid of passive and active structures," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 3, pp. 236–238, Mar. 2018.

[9] N. Hosseinzadeh and J. F. Buckwalter, "A compact, 37% fractional bandwidth millimeter-wave phase shifter using a wideband lange coupler for 60-GHz and E-band systems," in *Proc. IEEE Compd. Semicond. Integer. Circuits Symp.*, Miami, FL, USA, Oct. 2017, pp. 1–4.

[10] S. Y. Kim, D.-W Kang, K.-J. Koh, and G. M. Rebeiz, "An improved wideband all-pass I/Q network for millimeter-wave phase shifters," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3431–3439, Nov. 2012.

[11] D. Huang, L. Zhang, D. Li, L. Zhang, Y. Wang, and Z. Yu, "A 60-GHz 360° 5-bit phase shifter with constant IL compensation followed by a normal amplifier with ±1 dB gain variation and 0.6-dBm OP-1dB," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 12, pp. 1437–1441, Dec. 2017.

[12] J. Xia and S. Boumaiza, "Digitally assisted 28 GHz active phase shifter with 0.1 dB/0.5° RMS magnitude/phase errors and enhanced linearity," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 6, pp. 914–918, Jun. 2019.