Compact and Wideband MMIC Phase Shifters Using Tunable Active Inductor-Loaded All-Pass Networks

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***Abstract*— To address the challenging needs of small size, wide bandwidth, and low-frequency applicability, a novel phase shifter implementation is introduced that utilizes tunable active differential inductors within all-pass networks. The inductor tuning is used to achieve phase shifts up to 180°. A switchable active balanced-to-unbalanced transition (balun) circuit is included in front of the all-pass network to complement its phase shift capability by another 180°. In addition, the all-pass network is followed by a variable-gain amplifier to correct for gain variations among the phase shifting states and act as an output buffer. Although active inductors have previously been used in the design of various components, to the best of our knowledge this is the first time that they have been used in an all-pass phase shifter. The approach is demonstrated with an on-chip design and implementation exhibiting wideband performance for S- and L-band applications by utilizing the 0.5-μm TriQuint pHEMT GaAs monolithic microwave integrated circuits (MMIC) process. Specifically, the presented phase shifter 1×3.95 mm^2 die area and operates within the 1.5–3-GHz band (i.e., 2:1 bandwidth) with 10-dB gain, less than 1.5-dB root-mean-square (rms) gain error and less than 9° rms phase error. Comparison with the state-of-the-art MMIC phase shifters operating in S- and L-bands demonstrates that the presented phase shifter exhibits a remarkable bandwidth performance from a very compact footprint with low-power consumption. Consequently, it presents an alternative for the implementation of wideband phase shifters where all-passive implementations will consume expensive die real estate.**

***Index Terms*— Active balun, active inductor, all-pass network, L-band, monolithic microwave integrated circuits (MMIC), phase shifter, S-band, tunable inductor.**

I. Introduction

PHASE shifters are key components of electronically scanned antenna arrays (ESAs). Their phase resolution capabilities and phase/amplitude errors affect the precision achieved in radiation beam direction and the magnitude of the side lobes [1]. The high number of tightly spaced antenna elements within an ESA dictates the use of compact, low-cost, and power efficient phase shifter components. On the other hand, emerging applications operating across multiple frequency bands or over wide frequency ranges impose a new challenges for phase shifters due to the well-known tradeoffs among cost, size, performance, and bandwidth. Achieving wide bandwidth operation from a compact and low-cost on-chip phase shifter is especially challenging in the lower microwave band due to the size of inductors and any distributed components. To address the miniaturization needs, many phase shifter designs in the past decade have been done at the chip level. These implementations have mostly been carried out with GaAs processes and provided monolithic microwave integrated circuits (MMICs) capable of achieving complete 360° phase shifts. The design techniques for these MMICs include utilization of digital high-pass/low-pass [2] and all-pass [3] passive networks, performing vector summations [i.e., amplitude and phase control by changing the amplitude of I/Q signals using variable gain amplifiers (VGAs)] [4]–[10] and using switchable [11] and variable [2] delay lines. More recently, silicon (Si)-based phase shifters have attracted interest due to cost advantages. The majority of these designs have been primarily based on the techniques previously established with the GaAs implementations. For example, a 360° phase shifter is presented in [12] that use a varactor-tuned ladder network to operate at 8 GHz. A 6-b digital phase shifter covering the 7–11 GHz band has been implemented in SiGe [13]. A 4-b dual-band phase shifter for 5.2/2.4-GHz applications is introduced in [14]. The design combines two single-band phase shifters that utilize VGAs to perform vector summations.

For wideband phase shifter applications, high-pass/low-pass and all-pass network-based phase shifters are mostly preferred due to their ability to provide constant phase shift over an octave or more [3]. Fully integrated versions of these passive phase shifters are quite common. They have minimal power consumption and high linearity but suffer from high insertion loss [15]. In addition their wideband design necessitates the use of higher order networks with an increased number of passive inductor/capacitor components, penalizing the insertion loss further. Most importantly, realizing such wideband phase shifters at low microwave frequencies (e.g., below 10 GHz) contradicts with the miniaturization need–an attribute not desirable for on-chip implementations.

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On the other hand, vector summation techniques reduce chip area but do not provide the wideband characteristics of high-pass/low-pass phase shifters. Vector-sum phase shifters also require the use of a quadrature splitter at the input. This splitter is usually implemented using resistor/capacitor polyphaser filters which consist of cascaded resistor/capacitor–capacitor/resistor networks to extend the bandwidth and minimize amplitude variation between the in-phase and quadrature-phase paths. At lower gigahertz frequencies the resistor and capacitor values would be prohibitively large and require many stages to achieve wideband performance. Quadrature-phase accuracy is also determined by component matching between in-phase and quadrature-phase paths, and these paths require large layout areas for the resistors and capacitors.

To address the challenging needs of small size, wide bandwidth, and low-frequency applicability, this paper introduces a novel phase shifter implementation that combines the wide bandwidth performance of all-pass networks with tunable active differential inductors. The implementation also utilizes an active balanced-to-unbalanced (balun) transition-based 180° phase shifting circuit block and a VGA to provide a complete 360° phase shift range with low root-mean-square (rms) gain and phase error. Although active inductors have been previously used in the design of filters, power dividers [16], voltage controlled oscillators [17], and artificial transmission lines [18], to the best of our knowledge this is the first time that they have been used to implement all-pass network-based phase shifters. The feasibility of the approach is demonstrated with an on-chip design and implementation by utilizing a 0.5-μm TriQuint pHEMT GaAs process for S- and L-band applications. Specifically, the presented phase shifter 1×3.95 mm^2 die area and operates within the 1.5–3-GHz band (i.e., 2:1 bandwidth) with 10-dB gain, less than 1.5-dB rms gain error and less than 9° rms phase error.

This paper is organized as follows. Section II presents the functional block diagram of the phase shifter. Section III discusses the design of the active balun-based 180° phase shifting block. The design considerations regarding the active inductors and utilizing them within the all-pass network are detailed in Section IV. Section V explains the design of the VGA block that is also utilized as the output buffer. The experimental verification of the phase shifter is presented in Section VI. This is followed by the concluding remarks in Section VII.

II. Functional Block Diagram

The functional block diagram of the phase shifter is shown in Fig. 1. The first stage is composed of an active balanced-to-unbalanced (balun) circuit followed by a single-pole double-throw switch. The balun is designed to provide a wideband 50-Ω impedance match at the RF input and reduce the insertion loss of the phase shifter by providing gain. The balun functions as a switched 180° phase shifter bit to complement the phase shift that is attained in the second stage. Therefore, accuracy in both phase and amplitude performance of the balun is crucial as it directly contributes to the overall performance of the phase shifter.

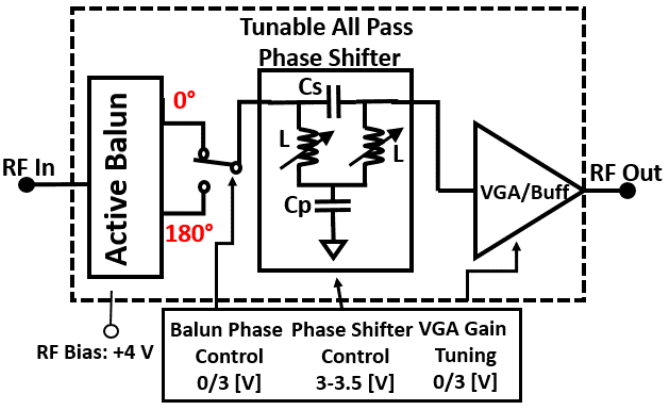


Fig. 1. Functional block diagram.

The second stage of the phase shifter is an all-pass network implemented using active inductors. All-pass networks are attractive for large phase shift bandwidths. It is typical to use them in digital implementations by including two switchable all-pass network blocks to form a phase shift bit [3] (e.g., a 22.5° bit). The complete phase shifter generally includes 4–6 such bits. However, implementation of this type of phase shifter causes the circuit area to be dominated by passive inductors, not only by the physical size of each inductor but also the spacing needed between them to reduce mutual coupling to an acceptable level. Therefore, the all-pass network utilized in this paper is based on an active tunable inductor that is compact and eliminates the need for several all-pass network blocks. The shunt inductor all-pass configuration (see Fig. 1) requires identical inductance values for its inductors and is therefore chosen over the shunt capacitor design. As detailed in Section IV, the selected active inductor-based all-pass network implementation provides continuous adjustment of the phase shift within 0°–180° from 1.5 to 3 GHz through a control voltage.

The third and final component of the functional block diagram comprises a two stage VGA that also acts as an output buffer. The first stage of the VGA is a common-gate (CG) amplifier that provides a constant load impedance to the output of the active all-pass network. The second stage is another CG amplifier with a variable bias resistor network in order to adjust the amplifier gain to balance the gain variations among the phase shift values. The output buffer at the end of the circuit is designed to provide a wideband 50-Ω match at the output. The following sections detail the design of each of the blocks within the proposed phase shifter with specific emphasis on the tradeoffs between tunability, bandwidth, and achievable phase shift associated with inclusion of active inductors within the all-pass network.

III. Active Balun-Based 180° Phase Shifter

The single-to-differential circuit topology shown in Fig. 2(a) has been extensively used to implement an active balun as documented in [19]–[21]. This circuit shows reliable performance with moderate noise figure (<3.8 dB), good linearity (Pin1dB ≈ 0 dBm), wideband input match (1.5–3 GHz), and balanced outputs. The circuit functions by taking an input signal and

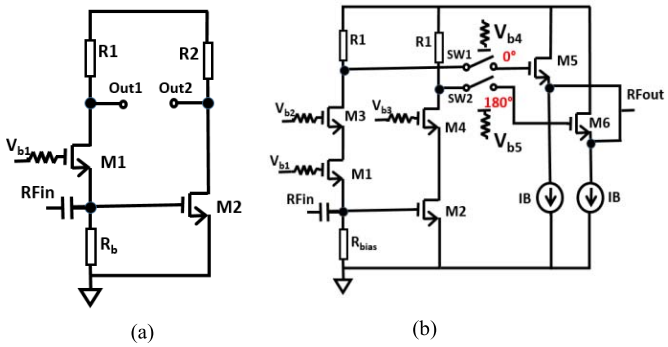


Fig. 2. (a) CG CS active balun and (b) its switched implementation for the proposed phase shifter.

splitting it into two equal amplitude signals that are ideally 180° apart in phase. It uses a CG transistor M1 and a common-source (CS) transistor M2 to provide a wideband input impedance (R_{in}) given as

$$R_{\text{in}} = \frac{1}{\text{gm}_1} \Big\| R_b \tag{1}$$

where R_b and gm_1 are the source resistor and transconductance of M1, respectively. R_b also serves to provide a bias voltage to M2. Selecting a large R_b value results in an R_{in} value that is dominated by the $1/\text{gm}_1$ term. In addition, for this case, the voltage gains of the two branches (Av_{CG} and Av_{CS}) are simplified as

$$\text{Av}_{\text{CG}} = \text{gm}_1 \times R1 \qquad \text{Av}_{\text{CS}} = -\text{gm}_2 \times R2 \tag{2}$$

where gm_2 represents the transconductance of M2. $R1$ and $R2$ are the load resistors of M1 and M2, respectively. Equation (2) shows that for this topology to function as a balun, M1 and M2 must have identical transconductance and load resistor products. For this, the load resistors are selected to be equal as $R1 = R2 = 500\ \Omega$. Since large values of R_b in the 400–700 Ω range imply $R_{\text{in}} \approx 1/\text{gm}_1$, gm_1 is selected as 27 ms to achieve a 50-Ω input impedance. Consequently gm_2 is selected to be identical with gm_1 to achieve equal powers at the outputs with 180° phase difference.

Fig. 2(b) depicts the active balun implementation within the proposed phase shifter. Transistors M3 and M4 form a cascode topology which provides higher isolation from output to input by eliminating the Miller effect with bias voltages V_{b1}, V_{b2}, and V_{b3} set to 1.3, 1.8, and 1.8 V, respectively. To utilize only one of the outputs based on the desired phase shift, switches SW1 and SW2 are placed on each of the output branches. The switches are implemented using large single enhancement mode transistors with width/length (W/L_t) of 100/0.5 μm and two fingers to minimize series resistance. The gates of the switches are biased with 1.5-kΩ resistors to improve isolation. Simulation results show a worst case insertion loss of 1.1 dB and isolation of 26.8 dB at 1.5 GHz. Unlike existing similar designs, switching the balun output does not result in input impedance variation as none of the transistors get completely shutoff. Specifically, both branches are always active since M1–M4 are kept in saturation and phase change are controlled by switches at the output. This results in higher

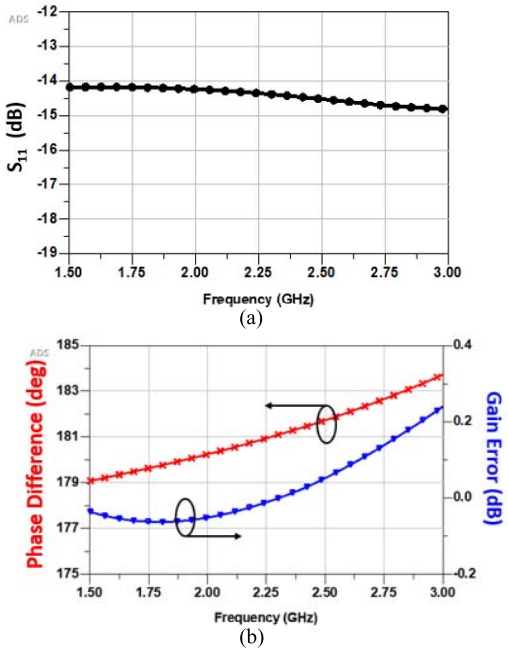


Fig. 3. Simulated performance of the active balun. (a) S_{11}. (b) Phase difference and gain error between the 0° and 180° states.

current consumption (~4.5 mA) but averts the critical issues of input impedance matching variations between different phase states. The buffers are implemented to isolate the balun from the input of the active all-pass phase shifter stage where bias currents (IB) are implemented using current mirrors. Keysight ADS schematics and full-wave momentum layout simulations were utilized in combination with post layout tuning to obtain the S_{11}, gain error, and phase difference performances shown in Fig. 3. Specifically, the gains of the two phase shift states were equalized by tuning the load resistors. In addition, although transistors M1–M4 were initially sized the same (W/L 30/0.5 μm with two fingers), the sizes of M2 and M4 were subsequently decreased (W/L 26/0.5 μm with two fingers). This strategy works well for compensating the lack of symmetry between the two signal paths. As seen, the circuit is well matched and S_{11} is maintained below −14 dB. The gain error between the two phase shift states is between −0.1 and 0.25 dB with the average gain being 10 dB. The phase error is below 4° across the 1.5 to 3 GHz frequency of interest. The active balun has a worst case switching time of 2.3 ns that was not affected by sweeping the inductance value of active inductor-loaded all-pass network.

IV. Active Inductor-Loaded All-Pass Network

The gyrator-C network shown in Fig. 4 consists of a back-to-back connection of two transistors and operates as a floating active inductor. In this network, $C_i (i = 1, 2)$ and Goj $(j = 7, 8)$ represent the total parasitic capacitance and conductance at the input–output and output/input nodes of the transistors M7/M8, respectively. Fig. 4 also depicts the RF equivalent circuit model corresponding to the gyrator-c network. The finite values of these conductance result in loss and limit the frequency range over which the network acts

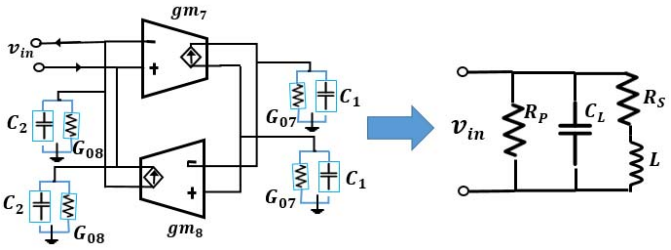


Fig. 4. Floating gyrator-c active inductor and its RF equivalent circuit model.

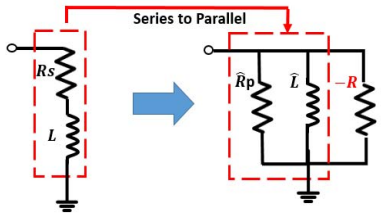


Fig. 5. Series RL to RL transformation in the RF equivalent circuit model of the gyrator-c network.

as an active inductor. The RF equivalent circuit consists of parasitic parallel resistance (R_p), parallel capacitance (C_L), series resistance (R_s), and inductance (L).

A Bode plot of this impedance shows that the inductance response of the network is frequency limited and dictated by the parasitic resistance of the network. Specifically, for a typical condition of $R_p \gg R_s$ the pole and zero frequencies (i.e., ωp and ωz) occur at

$$\omega p \approx \sqrt{\frac{1}{C_L L}} \qquad \omega z = \frac{R_s}{L}. \tag{3}$$

These denote the upper and lower bounds of the frequency range, respectively. Due to $R_p \gg R_s$, the quality factor (Q) of the active inductor also becomes

$$Q = \frac{\omega L}{R_s}. \tag{4}$$

Specifically, ωz is minimized by decreasing R_s which also serves to increase Q. This can be achieved by properly sizing transistors or using cascode transistors to reduce output conductance $Go7$. Additional operational frequency range can be obtained by using a feedback resistor as demonstrated in [24]. This feedback resistor introduces an additional zero to cancel the dominant pole. The approach allows for large values of capacitors C_L without limiting the maximum range of frequency where the system behaves like an inductor. The Q of the active inductor can be further increased by introducing a shunt negative resistor to the input of the gyrator-c network to cancel out the parasitic resistance seen in its RF equivalent circuit. This can be seen from the circuit model in Fig. 5 that revises the RF equivalent circuit of the gyrator-c network by replacing the series $R_S - L$ branch with parallel $\hat{R}p$ and $\hat{L}$ branches. To implement the negative R that will be used to cancel $\hat{R}p$, two cross coupled equally sized transistors can be employed as shown in Fig. 6 [25]. The negative resistance and

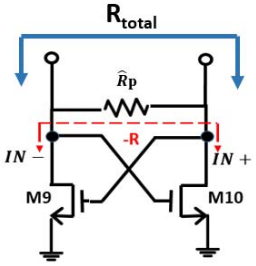


Fig. 6. Negative resistance cross-coupled transistors.

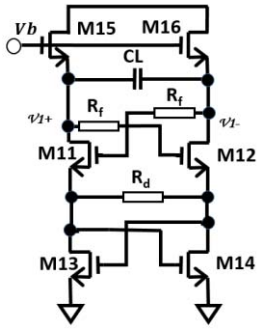


Fig. 7. DAI-based on cross-coupled transistors with feedback.

total resistance of this network are given by

$$-R = -\left(\frac{1}{\mathrm{gm}_9} + \frac{1}{\mathrm{gm}_{10}}\right)$$
$$R_{\text{total}} = \hat{R}p \| - R. \tag{5}$$

Fig. 7 depicts the schematic of the active inductor circuit introduced by [26] for implementing the aforementioned strategies for improved quality factor and frequency range. This schematic also represents the circuit that constitutes the active inductors of the all-pass network employed within the phase shifter of this paper. This source-degenerated differential active inductor (DAI) design comprises two cross-coupled E-mode PHEMT transistors M11 and M12 to realize the gyrator-c network. Feedback resistors R_f enlarge the frequency range, reduce the series RF resistance, and increase the inductance. Transistors M13 and M14 form the negative resistance circuit to improve the quality factor. Inductance tunability is achieved by varying the gm_{11} and gm_{12} values of the cross-coupled transistors M11 and M12, respectively. To do so, tuning voltage (V_b) on transistors M15 and M16 are utilized for current adjustment. Due to the feedback resistors, the RF equivalent circuit parameters of the active inductor becomes [26]

$$L = \frac{C_L}{\alpha(\mathrm{gm}_{11}\mathrm{gm}_{12})} \tag{6}$$

$$R_s = \frac{\frac{1}{R_T} - \omega p^2 \cdot \mathrm{Cgs}_{11,12} \cdot C_L \cdot R_f}{\mathrm{gm}_{11} \cdot \mathrm{gm}_{12}} \tag{7}$$

$$R_T = R_f \| R_d \| \mathrm{ro}_{11,12} \| \mathrm{ro}_{13,14} \tag{8}$$

where α represents the voltage attenuation factor (between 0 and 1) introduced by the feedback resistors, ωp is the frequency in (3), $\mathrm{ro}_{11,12}$ is the output resistance of transistors M11 and M12, $\mathrm{ro}_{13,14}$ is the net negative resistance of

M13 and M14 and C_L is the load capacitor. $Cgs_{11,12}$ is the sum of the gate to source capacitances of M11 and M12. In the case R_s becomes negligible because of the negative resistance network, the quality factor of the active inductor is determined by the parallel resistance R_p in Fig. 4, and (4) becomes

$$Q \approx \frac{R_p}{\omega L}. \tag{9}$$

Active inductors implemented using the gyrator-c topology are negative feedback systems and stability should also be considered. Classifying the gyrator-c active inductor shown in Fig. 4 as a second-order system, the damping factor is given by [22]

$$\xi = \frac{1}{2\sqrt{gm_7 gm_8}}\left(\sqrt{\frac{C_2}{C_1}} + \sqrt{\frac{C_1}{C_2}}\right). \tag{10}$$

Increasing gm_7 or gm_8 will lead to a decrease in the damping factor resulting in a decrease in stability. Resistor R_d in Fig. 7 thus becomes mandatory for unconditional stability ensuring that the resistance of the system stays positive.

To utilize the active inductor circuit shown in Fig. 7 within the all-pass network for phase shifting purposes, the first step is to determine the inductance variation required to achieve a 180° phase shift range within the frequency band of interest. For this, the following design equations reported in [3] can be employed:

$$L = \frac{p \cdot Z_0}{\omega}$$
$$p = \frac{1}{2}\tan\left(\frac{\phi}{4}\right) + \sqrt{1 + \frac{1}{4}\tan\left(\frac{\phi}{4}\right)^2} \tag{11}$$

where Z_0 is the characteristic impedance and ϕ denotes the phase shift in radians. Equation (11) shows that there is a linear relationship between the value of the characteristic impedance Z_0 and the inductance value L. For 1.5-GHz operation and 180° phase shift, a 50-Ω characteristic impedance results in an inductance tuning range from 3.2 to 8.6 nH. However, trying to implement an active inductor with this tuning range by following the approach outlined in the following paragraphs, fails due to the large inductance value and inductance variation ratio. Since, the active inductor-loaded all-pass network is preceded by the active balun and followed by the output VGA/buffer, it does not directly interact with the external 50-Ω connections and allows the freedom of choosing a lower characteristic impedance to minimize the required active inductance tuning range. Based on the inductance values obtainable from the active inductor, the impedance of the all-pass network was reduced. Consequently, buffers were needed at the output of the balun to provide the required impedance. Increased power consumption was therefore unavoidable when implementing this approach with a reduced characteristic impedance. Nevertheless, the quality factor was improved by including the shunt negative resistor network as described above and shown in Fig. 6. The desired inductances were achievable when the all-pass network was designed with a 25-Ω impedance with the required inductance tuning range being 1.6 to 4.3 nH and 0.9 to 2.2 nH at 1.5 and 3 GHz, respectively. The achievable

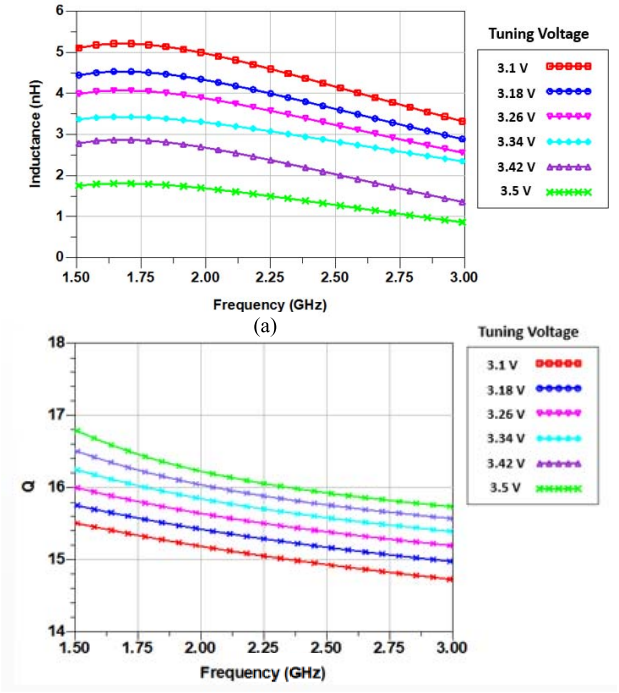


Fig. 8. (a) Inductance tuning range and (b) quality factor variation of the designed DAI circuit layout.

TABLE I
EFFECTS OF VARYING TRANSCONDUCTANCE AND FEEDBACK RESISTANCE ON PERFORMANCE OF THE TUNABLE ACTIVE INDUCTOR

gm	L	R_s	ωp	ωz
↑	↓↓	↓↓	↑	↓
↓	↑↑	↑↑	↓	↑
R_f	L	R_s	ωp	ωz
↑	↓	↓	↑	↓↓
↓	↑	↑	↓	↑↑

tuning range was designed, as seen in Fig. 8(a), to exceed that the minimum required range was to be able to accommodate potential manufacturing related variations.

Having determined the required inductance variation range, (3)–(7) are used as a starting point in the initial stages of the inductor design. M11 and M12 are the most critical transistors forming the core of the gyrator-c network-based active inductor concept. Table I summarizes how the transconductance variation of these transistors affects the active inductance, series resistance, and frequency range. The well-known equation $gm = (2K(W_{11,12}/L_{t11,12})I)^{1/2}$ (where K is the process transconductance parameter, W is transistor width, L_t is transistor length, and I is the IB) relates transconductance to the transistor size and IB. Changing the IB to change transconductance for inductance tuning also affects the operational frequency range of the inductor and therefore the frequency range needs to be adjusted by properly sizing the M11 and M12 transistors.

It is also assumed that the series and parallel capacitances of the all-pass network, denoted by Cs and Cp in Fig. 1, are in parallel with the parasitic capacitances of the transistors and contribute to C_L thereby impacting the inductance. (The values of Cs and Cp are 1.8 and 6.8 pF, respectively, as determined from [3] at the center frequency of 2.25 GHz.) In estimating the transconductance range, the transistor sizing and achievable inductance tuning range via IB control must be investigated by utilizing circuit and layout models associated with the fabrication process to account for critical parasitic effects. In doing so, the quality factor and operational frequency range of the active inductor must also be considered since the transistor sizes can be reduced to increase L but this in turn impacts R_s and ωz as indicated in (3). Consequently, the M11 and M12 sizes are best determined through circuit and layout modeling. In these modeling steps, the inductance value is extracted from the S-parameters of the entire all-pass network. Specifically, these transistors exhibited $gm_{11,12} = 0.9$ mS and $gm_{11,12} = 2.8$ mS at the 850 μA and 2.7 mA IB levels. Transistors M15 and M16 serve as current mirrors to vary the gm of M11 and M12 to tune the inductance.

Once M11 and M12 sizes are determined to achieve the necessary inductance values, the next design step is to minimize the series resistance of the equivalent RF network in an effort to further increase the quality factor of the active inductor. In the DAI network shown in Fig. 7, transistors M13 and M14 form the negative resistance network and they are customarily sized to be identical with equal transconductance. Since sources of the active inductor transistors and drains of the negative resistance transistors are connected to each other (e.g., M11 and M13), they are biased with the same current. Therefore, the smallest IB (i.e., 850 μA) used to tune the inductor results in the largest absolute value of negative resistance as can be observed in (5) with the opposite occurring for the largest IB (i.e., 2.7 mA). Hence, transistors M13 and M14 are sized to produce a negative resistance to minimize the series resistance of the network under the 850-μA IB condition. Specifically, the transistor sizes were determined in a way to keep the total series resistance of the entire all-pass network slightly above zero ($\sim$5 Ω) in order to increase the quality factor while retaining a positive resistance margin to prevent the occurrence of oscillations due to fabrication tolerances. Stability simulations were also conducted and R_d of 100 Ω was added to the network to ensure unconditional stability. It is important to note that addition of R_d does not impact the Q performance as it is in parallel with the total series resistance. Since, the negative resistance circuit is also in parallel with the active inductor, it has a minimal impact on the inductance value and its frequency behavior.

The phase shifter was verified as being unconditionally stable and this was achieved by the inclusion of R_d in Fig. 7. This ensures that the total resistance of the inductor stays positive. Not including this resistor also makes the inductor stability more susceptible to the total transistor resistance fluctuations due to process variations. Total parasitic capacitance variations of the transistors due to process variations can be accounted for in (6)–(8) as they affect the value of R_s. However, such impact is minimal since the inclusion of the negative resistance network makes Rs negligible as explained in (5) and Fig. 6. Additional effects of process variations and sensitivity on design specifications could be implemented in a design of experiments setup to identify the most sensitive components in the design.

TABLE II
TRANSISTOR SIZES OF THE OPTIMIZED TUNABLE ACTIVE INDUCTOR

Transistor	W/L$_t$, µm/µm	Number of Fingers
M11, M12	130/0.5	2
M13, M14	50/0.5	2
M15, M16	100/0.5	2

Once the above procedure is completed for achieving the inductance tuning range at the center frequency, the entire tunable active inductor circuit must be investigated for its frequency-dependent behavior. This observation reveals that the frequency range should be enhanced by introducing the feedback resistors R_f shown in Fig. 7 as described in [25]. Since, the feedback resistors change the voltage attenuation factor α, the achievable inductance tuning range is also impacted as indicated by (6). Moreover, the desired inductance tuning per control voltage is not identical across the frequency band as already mentioned. This necessitates parametric studies and optimizations to achieve the desired inductance tuning across the operation bandwidth while maintaining the quality factor and stability performance. The interrelationship among the key circuit parameters utilized in the parametric studies and optimizations performed for this paper are summarized in Table I. The value of R_f was determined as 70 Ω from simulation. The appropriate value was selected by running a simulation and sweeping the value of R_f while trying to remain within the limits of inductance value that were previously determined for the phase shifter. Table II shows the transistor sizes of the optimized circuit. Full-wave layout simulations were performed using the Keysight ADS Momentum suite to account for parasitic effects. Optimization of the transistor size as mentioned previously resulted in achievement of the desired tuning range of inductance over a frequency range from 1.5 to 3 GHz as shown in Fig. 8(a) for tuning voltage varying from 3.1 to 3.5 V. Unconditional stability was achieved with a stability factor >1 and stability measure >0 across the entire frequency range. The quality factor is shown in Fig. 8(b). It ranges from 14.8 to 17.5. These simulation results demonstrate that this approach can be used as an alternative to passive inductors in applications where inductance tunability is advantageous, such as in the design of tunable all-pass or matching networks.

V. OUTPUT VGA/BUFFER

The last stage of the functional block diagram consists of VGA/buffer circuits as shown in Fig. 9. The first block of the circuit is a CG amplifier that provides a constant 25-Ω load impedance to the output of the active tunable inductor-loaded all-pass network. The first cascade and emitter follower

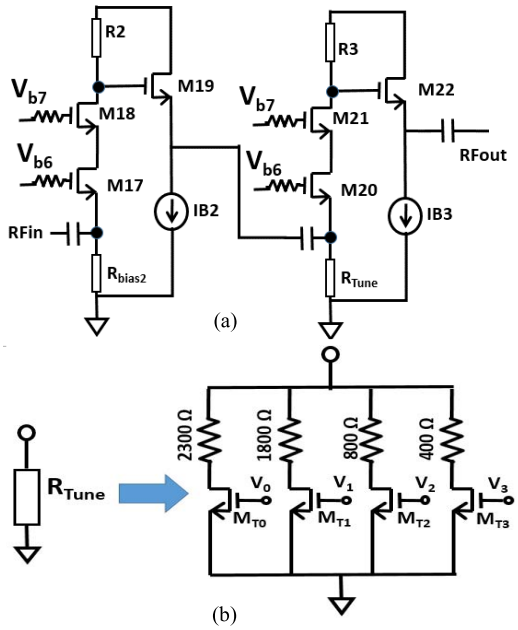


Fig. 9. (a) Circuit schematics of the output VGA/buffer. (b) Resistive tuning network.

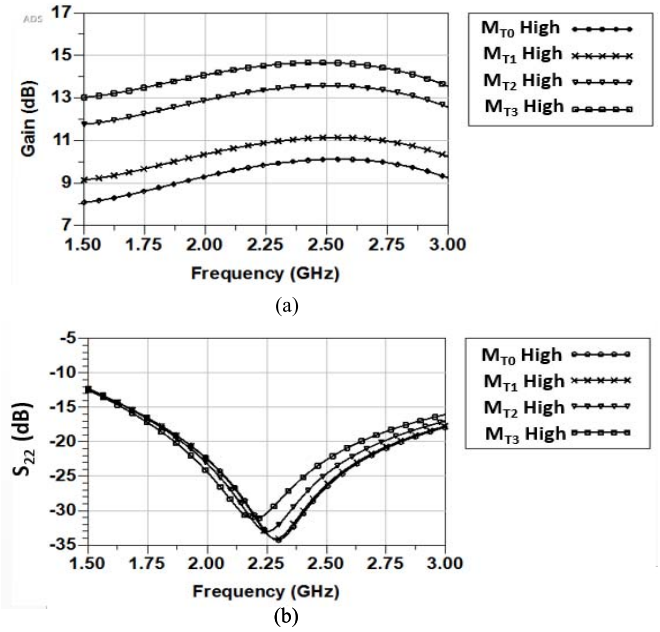


Fig. 10. (a) Simulated gain and (b) S_{22} of the designed VGA/buffer circuit.

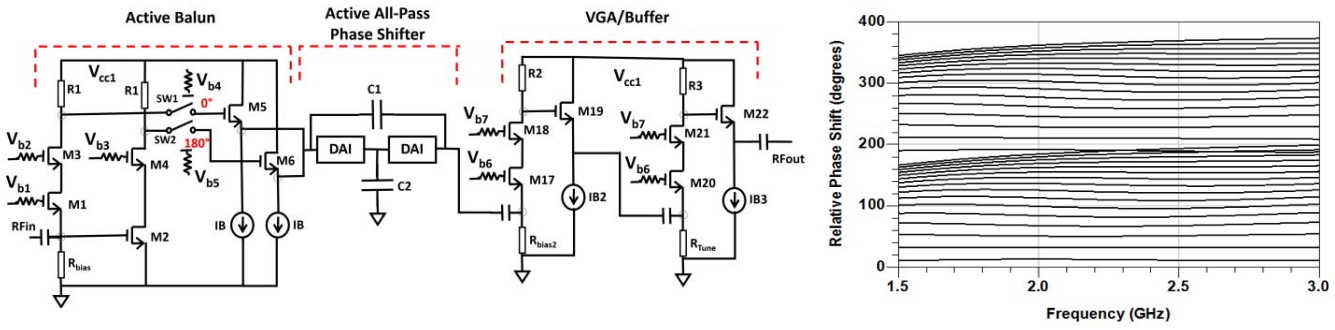
(M17, M18, and M19) serve as a buffer to isolate the active all-pass network from the actual VGA (M20, M21, M22, and R_{Tune}) so phase shift is not affected as gain is adjusted. Given that the input impedance of the CG amplifier M17 is approximately equal to $1/\text{gm}_{17}$ the impedance value can be set by adjusting IB and/or transistor size. The operating point is adjusted using the bias at the source terminal which in this case is implemented by using a resistor $R_{\text{bias}2}$ that sets the IB of M17. The transistor size used was $W/L_t = 33/0.5\ \mu$m with two fingers. $R_{\text{bias}2}$ is selected as 700 Ω for a IB of 1.2 mA. M18 and M19 are sized the same as M17 with V_{b6} set to 1.4 V and V_{b7} set at 2.5 V. The second block of the circuit is another CG amplifier similar to the first but with a variable resistance at the source (i.e., source of transistor M20) to tune the gain for compensating the S_{21} variations across the different phase shift values. The resistive tuning network is shown in Fig. 9(b) and consists of four parallel resistors that can be used as R_{Tune} by activating appropriate switches M_{T0}–M_{T3} ($W/L_t = 50/0.5\ \mu$m with number of fingers = 2). The different resistor values vary the IB through the CG amplifier M20 and can be used to vary the voltage gain, which in a first-order approximation becomes

$$\text{Av} \approx \text{gm}_{20} \times R3. \tag{12}$$

Based on the resistor value chosen, the IB varies from 0.4 to 3.5 mA for a voltage gain variation from 8 to 15 dB. Within this range, using the four resistor network, 15 discrete gain steps are available with ∼0.5 dB steps. The output buffer is designed to provide a wideband 50-Ω output match using the same approach pursued at the input of the CG amplifier. However, transistor M22 is sized as $W/L_t = 20/0.5\ \mu$m with number of fingers = 2 and a IB of 3 mA to achieve a 50-Ω output impedance. Bias current sources IB2 and IB3 are implemented using CS transistors (15/0.5 μm, number of fingers = 2) with external voltage applied to the gate, both providing 3-mA IB. The simulated performance of the VGA/buffer layout is shown in Fig. 10. The complete schematic of the entire phase shifter is shown in Fig. 11(a) where all components and interconnects are implemented on chip. The simulated phase shift performance of the design layout is shown in Fig. 11(b). Greater than 360° phase shift is achieved across the entire frequency range with a mean gain of 13 dB. The simulated input- and output-return losses are >13 dB across the entire frequency range. In Fig. 11(a), the simulated voltage gain of the active balun is 10 dB while the active all-pass phase shifter has an average simulated loss of 5 dB with the VGA/Buffer providing an average voltage gain of 8 dB. The all-pass network as a stand-alone unit is bidirectional which with implementation of double-pole double-throw switches could also be used in a transceiver. The success achieved with the simulated performance motivated the experimental verification of the designed phase shifter as detailed in the following section.

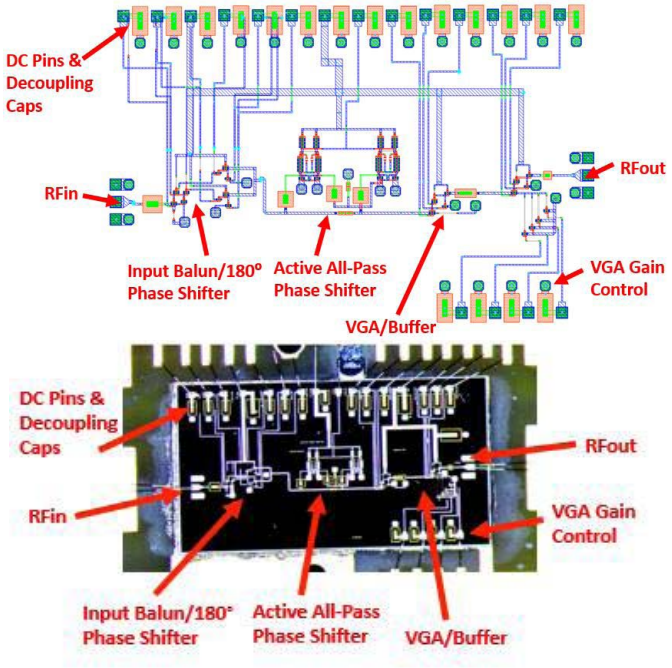
VI. Experimental Verification

The phase shifter was implemented in the 0.5-μm TriQuint TQPED GaAs process with a chip size of 2.7 × 4.5 mm^2 including all bias lines and bond pads (1 × 3.95 mm^2 without the bond pads [see Fig. 12(a)]. The chip is mounted on a test board [see Fig. 12(b)] that utilizes grounded coplanar waveguides for input–output RF excitations and narrower conductive traces for dc bias and control. The test board is an 8.1 × 4.8 cm^2 0.79-mm-thick FR4 board. All traces on the test board were fabricated using 1 oz. copper with Electroless Nickel Electroless Palladium Immersion Gold surface finish to allow for the addition of wire bonds. The RF input and output pads of the chip are wedge wire bonded to the test board with two parallel 18-μm-diameter gold wires to minimize the

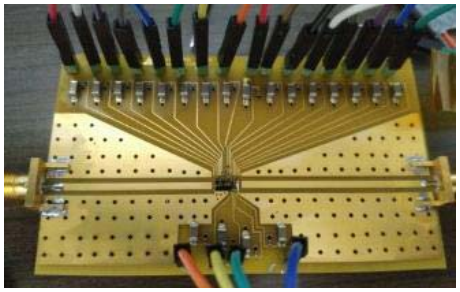


(a) (b)

Fig. 11. (a) Expanded circuit schematic of the phase shifter. (b) Simulated phase shift performance from the designed layout. DAI schematic is given in Fig. 7.



(a)



(b)

Fig. 12. Fabricated phase shifter. (a) Design layout and microphotograph. (b) Test board.

parasitic series inductance associated with the wire bonds. The 20-pF decoupling capacitors of the circuit are implemented on chip. The test board also utilizes 1-μF 0603 and 0.1-μF 0201 sized surface mount decoupling capacitors in order to provide low-frequency filtering and a low impedance path to ground for any high-frequency signals on the dc bias lines. The 50-Ω SubMinature version A (SMA) connectors are attached to both the input and output RF ports to facilitate the measurements while the four wire connectors V_{0-3} [Fig. 9(b)] on the bottom are used to vary the gain of the VGA. The top part of the board consists of dc bias connections used to bias V_{b1-9} and V_{cc1} in Fig. 11(a) as well as to vary the tuning voltage V_b of the active inductor (Fig. 7). The gain is varied via the VGA to minimize gain errors around the center frequency of 2.25 GHz. The VGA settings used for each phase shift state are derived from the circuit and layout simulations and depend on the gain variation between reference and phase state.

Fig. 13(a) shows the measured phase response covering the entire 360° range as well as the rms phase error. The input balun/180° phase shifter was set to the 0° phase shift option by activating switch SW1 in Fig. 11. The tuning voltage of the active inductor (V_b Fig. 7) was varied in 30 mV increments from 3.1 to 3.5 V for phase shifts up to 180°. To achieve the next consecutive 180° phase shift for a full 360°, switch SW2 of 180° phase shifter was activated instead of SW1. The rms phase error is calculated using [19]

$$\theta_{\Delta,\mathrm{RMS}} = \sqrt{\frac{1}{N-1}\sum_{i=2}^{N}|\theta_{\Delta i}|^2} \tag{13}$$

where N is the number of phase states used to achieve a 360° phase shift and $\theta_{\Delta i}$ is the phase difference between simulated and measured phase shift for 32 distinct phase states equivalent to a 5-b phase shifter. The rms phase error ranges from 5° to 9° over the entire frequency range. Results observed in Fig. 13(a) show that phase shift is not uniform across the entire frequency range. For instance, from 1.5 to 2 GHz there is not coverage from approximately 150° to 180°. However, it should be remarked that the presented design is a continuous phase shifter and finer phase tuning can be achieved with smaller voltage increments. In addition, it is important to note that a more robust solution could also be achieved by cascading another all-pass network stage and designing these all-pass networks for different center frequencies within the 1.5- to 3-GHz frequency range. This cascading approach would decrease the inductance requirements and result in

TABLE III
PERFORMANCE COMPARISON

	[28]	[29]	[30]	[31]	[32]	This work
Technology	0.5 um pHEMT	0.5 um pHEMT	0.5 um pHEMT	0.18 um CMOS	SiGe	0.5 um pHEMT
Frequency (GHz)	1.8 – 3.2	2.5 – 3.5	0.85 – 1.15	3.4-3.5	10-13	1.5 - 3
Phase Control	360°/6 bits	360°/6 bits	360°/5 bits	360°/6 bits	360° /4 bits	360° /5 bits
Gain (dB)	26	26	-6.5	-5.4	3.7	10
RMS Phase Error (deg.)	< 6	< 3	< 7	3	-	< 9
RMS Gain Error (dB)	<1	-	< 1.5	-2	-	< 1.5
Power (mW)	500	not reported	not reported	-	54	78
P_{out}1dB (dBm)	12	13	21	-	-27.3	12
Fractional Bandwidth (%)	56	22	10	3	6	67
Size (mm^2)	4 × 4	5.5 × 5.5	1.87 × 0.87	1.2 x 2.3	1.92 x .78	2.7 × 4.5

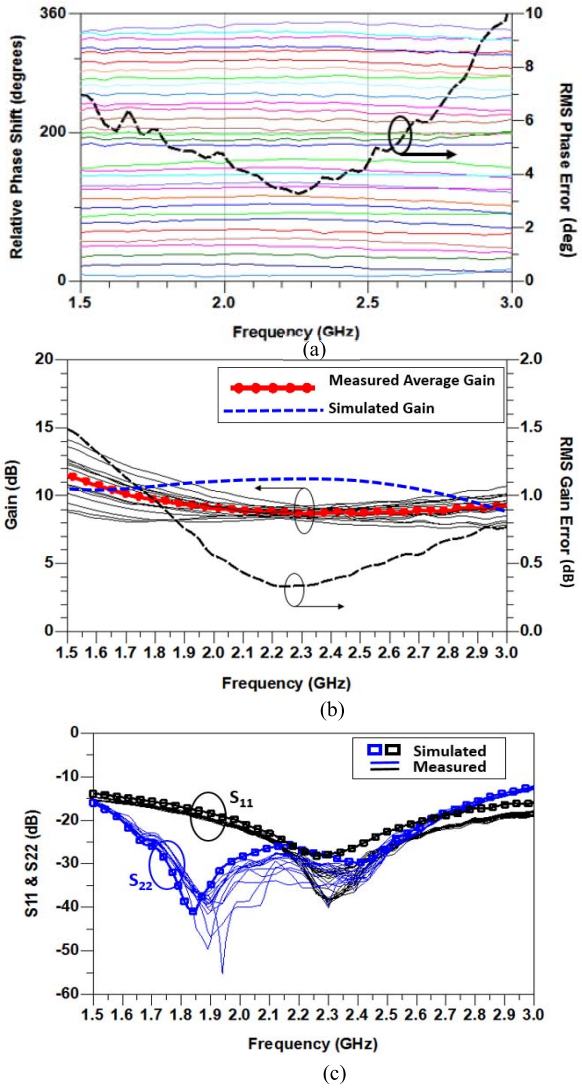


Fig. 13. Measured performance of the fabricated phase shifter. (a) Phase response and rms phase error. (b) Gain and rms gain error. (c) S_{11} and S_{22}.

a flatter phase response, but would also require larger chip area and power consumption. Fig. 13(b) shows the measured gain for the different measured phase shift states depicted in Fig. 13(a) along with the average gain. The measured rms gain error, calculated using

$$A_{\Delta,\mathrm{RMS}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}|A_{\Delta i}|^2} \tag{14}$$

is also shown in Fig. 13(b) where $A_{\Delta,\mathrm{RMS}}$ is the RMS amplitude error. RMS gain error <1.5 dB was obtained. Fig. 13(c) presents the measured S_{11} and S_{21} performances of the phase shifter. The difference between measured and simulated gain can be attributed to additional losses of RF traces on the test board, as these were not accounted for in simulation. These data demonstrate that impedance matching is satisfied with >15 dB return losses across the frequency range and are independent of the phase shifter state due to the functionalities of the active balun acting as an input buffer and VGA cascaded with an output buffer. Measured results show an input 1-dB compression point (P1dB) of −1 and −2 dBm at 1.5 GHz for the low and high gain settings of the VGA, respectively. At 3 GHz, the measured P1dB is −1 and 0 dBm for the low and high gain settings of the VGA, respectively. As an example, Fig. 14 presents the measured P1dB performance at 3 GHz for the high gain setting of the VGA and demonstrates a P1dB value of 0 dBm. The total current consumption of the active balun, active tunable inductor-loaded all-pass network, and output VGA/buffer is 8, 3.4, and 8 mA, respectively. The dc supply voltage is 4 V and results in a total power consumption of 78 mW for the phase shifter.

Table III summarizes the measured performance of the phase shifter and compares it with performances of the previously published state-of-the-art MMIC phase shifters that are tailored toward L- and S-band applications. The 67% fractional bandwidth of the presented design outperforms that of the others given in Table III. Its footprint is larger than the phase shifter presented in [30]–[32]. However, as compared to these, the presented phase shifter 10-dB gain in addition to its significantly larger bandwidth. The rms gain error is on-par with the other phase shifters. The rms phase shift error is larger than desired but can potentially be reduced in the future iterations with the addition of a 90° phase shifter in conjunction with the 180° balun already used. This design change would require less tuning range in the active inductor.

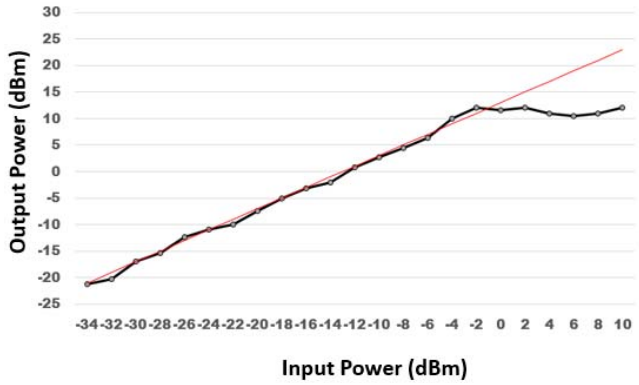


Fig. 14. Measured P1dB performance at 3 GHz for high gain setting.

The phase shifters presented in [28] and [29] provide large gains; however, they also occupy more chip area than the presented design. In addition, power consumption of the phase shifter in [28] is 500 mW, which is more than six times the consumption of the presented design. Measured results show an output P1dB of 12 dBm which is similar to [28] and [29], but less than the passive design in [30] which has 6.5-dB insertion loss. Reference [32] has an output P1dB of −27.3 dBm but operates at a higher frequency.

VII. Concluding Remarks

A novel compact and wideband phase shifter concept based on tunable active inductor-loaded all-pass networks has been introduced and experimentally verified for potential S- and L-band applications. Specifically, the presented phase shifter has 1×3.95 mm^2 die area without bond pads and operates within the 1.5 to 3 GHz band with 10-dB gain, less than 1.5-dB rms gain error and less than 9° rms phase error. A comparison with the state-of-the-art MMIC phase shifters operating in S- and L-bands demonstrates that the presented phase shifter exhibits a remarkable bandwidth performance from a very compact footprint with low-power consumption. Although the phase shifter is implemented using a GaAs MMIC process, the concept is suitable to be implemented on silicon processes as the functionality of the active inductors has already been successfully verified. Linearity performance might be the only advantage in using GaAs over a silicon process such as CMOS since the limiting factor for linearity in this network could be that of the active inductors. In addition, the compact circuit area of the presented concept is promising to include additional all-pass network segments within the design to further increase the bandwidth performance, potentially to cover a decade or more. The utilized GaAs process includes both enhancement and depletion mode pHEMT devices which can be facilitated to design digital serial to parallel converter to reduce number of interfaces for phase control similar to that of CMOS.

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