Single-Ended and Differential Ka-Band BiCMOS Phased Array Front-Ends

Byung-Wook Min, *Student Member, IEEE*, and Gabriel M. Rebeiz, *Fellow, IEEE*

***Abstract*—Single-ended and differential phased array front-ends are developed for Ka-band applications using a 0.12 μm SiGe BiCMOS process. The phase shifters are based on CMOS switched delay networks and have 22.5° phase resolution and <4° rms phase error at 35 GHz, and can handle +10 dBm of RF power ($P_{1\mathrm{dB}}$) with a 3rd order intermodulation intercept point (IIP3) of +21 dBm. For the single-ended design, a SiGe low noise amplifier is placed before the CMOS phase shifter, and the LNA/phase shifter results in 11 ± 1.5 dB gain and < 3.4 dB of noise figure (NF), for a total power consumption of only 11 mW. For the differential front-end, a variable gain LNA is also developed and shows 9-20 dB gain and < 1° rms phase imbalance between the eight different gain states. The differential variable gain LNA/phase shifter consumes 33 mW, and results in 10 ± 1.3 dB gain and 3.8 dB of NF. The gain variation is reduced to 9.1 ± 0.45 dB with the variable gain function applied. The single-ended and differential front-ends occupy a small chip area, with a size of 350 × 800 μm^2 and 350 × 950 μm^2, respectively, excluding pads. These chips are competitive with GaAs and InP designs, and are building blocks for low-cost millimeter-wave phased array front-ends based on silicon technology.**

***Index Terms*—Ka-band, low-noise amplifier (LNA), phase error, phase shifter, phased array, SiGe BiCMOS integrated circuit, variable gain amplifier.**

I. Introduction

PHASED-ARRAY systems have been used since the 1950's to achieve electronic beam control and fast beam scanning [1], [2]. They require a receiver front-end per antenna element which includes a low-noise amplifier (LNA), a phase shifter, and a variable gain amplifier (VGA). These have been implemented with GaAs- or InP-based discrete modules especially at millimeter-wave frequencies, resulting in relatively high cost and low integration density. However, with recent developments in silicon technologies, it is possible to build Si-based phased array on a single chip [3], [4], and the number of GaAs components can be drastically reduced.

Fig. 1 shows the block diagram of a phased array receiver front-end. The electronic phase shifters vary the insertion phase of the incoming signal and this results in the antenna beam scanning. The VGA can weight the RF signals to tailor the beamwidth and sidelobe level and also compensate for the gain variation of the phase shifter. The RF phase-shifting architecture has been used since the 1950s and has several advantages over the LO or IF phase-shifting architecture [3]. 1) The possible interferer is canceled before the mixer/receciver, and this greatly relaxes the mixer linearity and overall dynamic range requirement (since the Wilkinson power combiner is a linear passive circuit [5], [6]). 2) There is no need to distribute a local oscillator signal over the chip, which is important for large element systems. 3) The power consumption is reduced since only one mixer is needed for the entire array. There are four basic types of phase shifters [7]: switched delay [8]–[10], loaded reflection [11], [12], loaded line [13], [14], and vector modulation [15], [16], and all can be designed using either distributed or lumped-elements, but the lumped element design is preferable on silicon for high integration density. The phase shifter can either be analog-based (continuous phase shift) or digital-based (step phase shift). The digital passive phase shifter has advantages of simple control circuits and immunity to noise in the control lines.

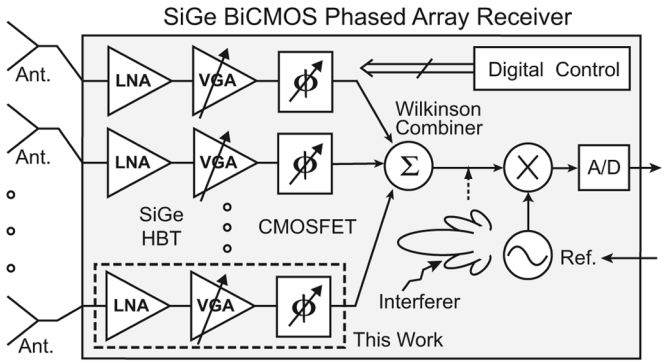

Fig. 1. Block diagram of a SiGe BiCMOS receiver front-end for an RF phase-shifting phased-array system.

A 4-bit digital-type phase shifter with 22.5° phase resolution (a maximum phase error of ±11.25°) is the most specified design for satellite communications and radar systems. This is because, with ±11.25° phase delay resolution, the phased arrays can scan the antenna beam with negligible decrease of the array gain or increase in the sidelobe levels. Fig. 2 presents the array factor of a linear uniformly excited 16-element phased array with an element-to-element spacing of $d = \lambda/2$ and scanning every 3° with 4-bit phase shifters. The required delay for each element is rounded to the nearest phase delay available in the

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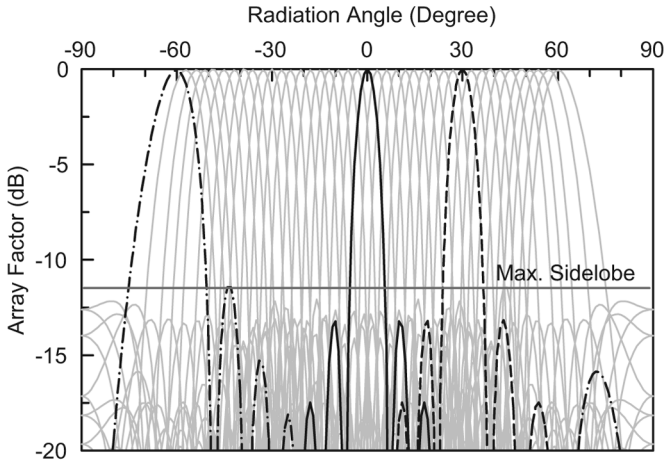

Fig. 2. Array factor of a 16-element phased array scanning every 3° from −60° to 60° with 4-bit phase shifters ($d = \lambda/2$).

4-bit phase shifter. The loss at the scanning direction due to the 4-bit phase resolution is < 0.1 dB for all scan angles.

In this paper, single-ended and differential versions of SiGe BiCMOS front-ends are presented for a 35-GHz phased array receiver system (Fig. 1). The application areas are in Ka-band defense and high-data-rate satellite communication systems. The LNA and VGA (for the differential version only) is based on the SiGe heterojunction bipolar transistor (HBT), and the 4-bit switched-delay-type phase shifters are designed using CMOS transistors. In Section II, the SiGe BiCMOS process and phase shifter design are described, followed by the measured results in Section III. Section IV reports the LNA and VGA design, and the measured results of the entire receiver front-end modules (single-ended and differential) are presented in Section V.

II. Phase Shifter Design

A. SiGe BiCMOS Process, Transmission Line, and RF Pads

The Ka-band receiver front-ends are designed using a 0.12 μm SiGe BiCMOS process (IBM 8HP) [17]. The peak cutoff frequency (f_T) of a SiGe HBT is about 200 GHz at a collector current density of 12 mA/μm^2, and the minimum noise figure $(\mathrm{NF}_{\min})$ of a common-emitter amplifier is about 1.8 dB at 35 GHz with a current density of 1.5 mA/μm^2. Hyper-abrupt junction diodes are also available and used as varactors (HAVAR) [18]. Metal–oxide–metal (MIM) capacitor and spiral inductor models are supported in the process design kit, but, in this work, these are designed using a commercial electromagnetic software (Sonnet[1]) since the design-kit layout is not optimal for high density Ka-band circuits.

The IBM 8HP process supports seven metal layers including top two thick metal layers. A 50 Ω transmission line is designed as shown in Fig. 3(a). The bottom and side ground planes shield the signal line from the lossy substrate. A measured 50 Ω line results in a impedance (Z_o) of ∼48.5 Ω, a loss (α) of 0.4 dB/mm, and an effective permittivity $(\epsilon_{\mathrm{eff}})$ of 3.9 at 35 GHz [Fig. 3(b)]. The transition between the transmission line and G-S-G pad is also designed using Sonnet to provide a 50-Ω impedance, and is

[1]Sonnet, ver. 10.53, Sonnet Software Inc., Syracuse, NY, 1986–2005.

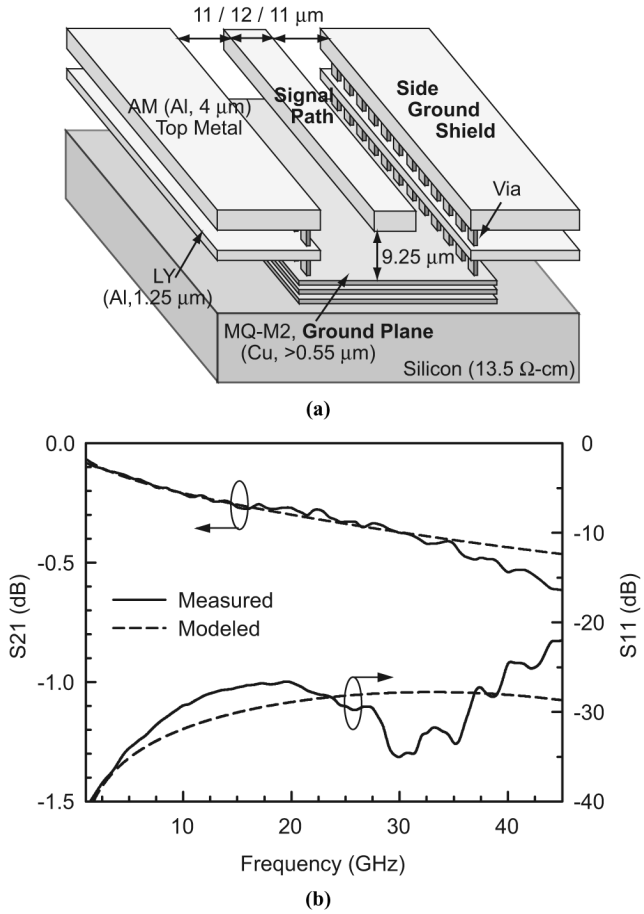

Fig. 3. (a) Shielded 50 Ω microstrip line structure using the seven-metal-layer profile (IBM 8HP) and (b) measured and modeled S-parameters of the transmission lines ($Z_o = 48.5\ \Omega$, $\alpha = 0.4$ dB/mm and $\epsilon_{\mathrm{eff}} = 3.9$).

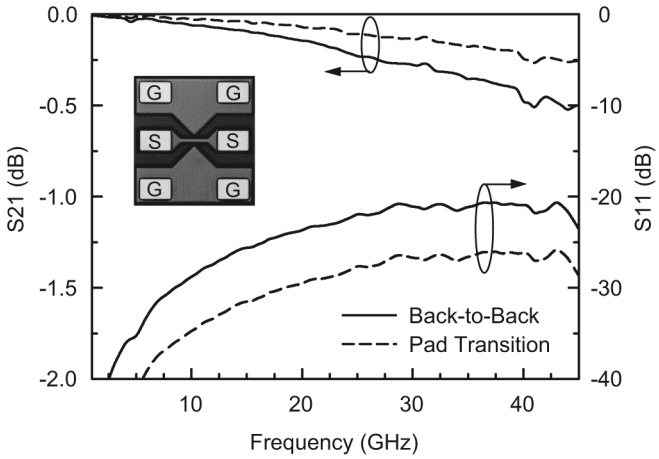

Fig. 4. Measured S-parameters of the pad transitions.

measured in a back-to-back configuration (Fig. 4). The performance of a single transition is then obtained using a symmetrical ABCD matrix, and results in a return loss of <-25 dB up to 45 GHz, and an insertion loss of 0.2 dB at 35 GHz.

B. CMOS Switches

The phase shifters are based on 0.12 μm CMOS transistors (Fig. 5). The CMOS transistor is a four-port device with a body node of the substrate contact. The CMOS gate is biased using a

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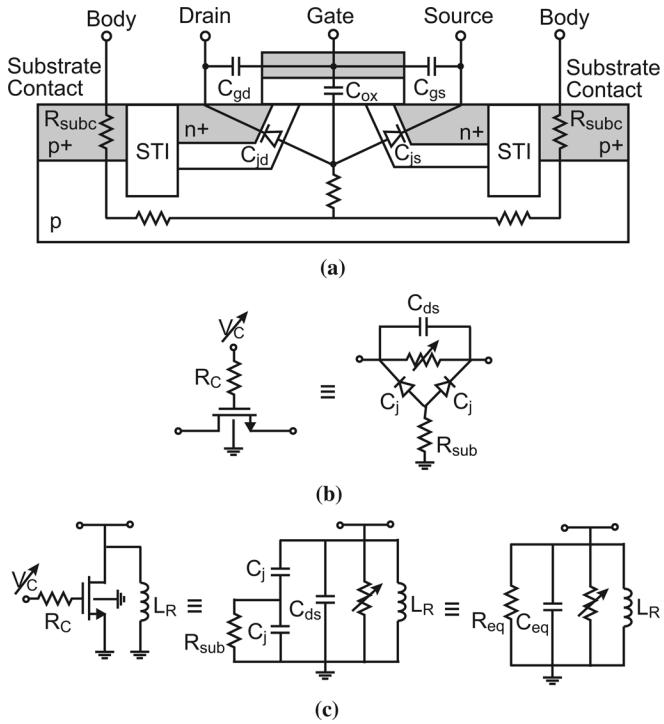

Fig. 5. (a) Cross sectional view of a CMOS transistor and simplified circuit models of (b) a series switch and (c) a shunt switch with a parasitic-resonating inductor.

large resistor, $R_C = 20$ kΩ, in order to prevent signal leaking and oxide breakdown. Fig. 5(b) shows the simplified circuit model of an nMOS series switch, where C_{ds} is the series capacitance between the drain and source and C_j is the drain and source junction capacitance. $R_{\rm sub}$ is the series resistance from the junction to the ground node, and therefore includes the substrate resistance and substrate contact resistance $(R_{\rm subc})$. $R_{\rm sub}$ highly depends on the size and distance (from the transistor) of substrate contacts, and even the transistor shape [19]. Therefore, large substrate contacts (35×50 μm^2) are placed very closely all around each nMOS transistor to minimize this uncertainty, and $R_{\rm sub}$ is assumed to be 50 Ω [20]. Minimizing $R_{\rm sub}$ with large substrate contacts also increases the isolation of the CMOS switch because it reduces the input signal leakage through the junction capacitance to the output port.

The on-state resistance of CMOS switches can usually be reduced by enlarging the gate width in low frequency application. However, at Ka-band frequencies, capacitive coupling to the substrate due to the junction capacitances C_j results in an increased signal loss. This means that there is an optimum value for the gate width in order to minimize the insertion loss at a given frequency and a specific input/output impedance [21]. Fig. 6 shows that the insertion loss is minimized when the gate width is 20-26 μm (optimal $w = 23$ μm). The simplified model values of the switch are also shown for $w = 23$ μm.

The CMOS shunt switch and its equivalent circuit is also shown in Fig. 5(c). The gate width of the shunt switch can be larger than the series switch because the junction capacitances do not degrade the on-state switch performance due to the already grounded source. A low on-state resistance is more important for the shunt switch so as to minimize the impedance

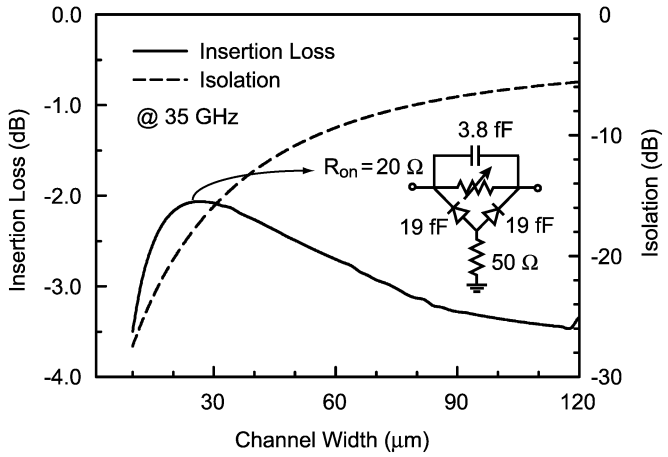

Fig. 6. Simulated insertion loss and isolation of CMOS series switch at 35 GHz versus channel width. The simplified model of 23 μm wide CMOS switch is also shown.

to the ground. However, the junction capacitances degrade the off-state isolation (to ground) and this limits the transistor size. A shunt inductor $(L_R = 1/\omega^2 C_{\rm eq})$ can be connected in parallel with the shunt switch to resonate out the parasitic capacitance $(C_{\rm eq})$ at a desired frequency and this allows an increase in the transistor size. In Fig. 5(c), $C_{\rm eq}$ and $R_{\rm eq}$ of the equivalent circuit are

$$R_{\rm eq} = \frac{4\omega^2 R_{\rm sub}^2 C_j^2 + 1}{\omega^2 R_{\rm sub} C_j^2} > \frac{4}{\omega C_j} \tag{1}$$

$$C_{\rm eq} = \frac{C_j + 2\omega^2 R_{\rm sub}^2 C_j^3}{4\omega^2 R_{\rm sub}^2 C_j^2 + 1} + C_{ds} \tag{2}$$

and $R_{\rm eq}$ is usually large (> 500 Ω) unless the transistor is extremely large. Therefore the off-state isolation depends mostly on the quality factor (Q) of L_R. In the phase shifter design, the gate width of the shunt switch is enlarged to 34 μm considering the inductor value and the isolation bandwidth at 35 GHz.

C. Single-Ended Switched-Delay Phase Shifter

For a switched-delay phase shifter, low-pass or high-pass Π and T networks provide up to 90° of phase delay or advance while being matched at a desired frequency [8], [14]. The inductor and capacitor values for the low- or high-pass networks are calculated to provide ϕ phase delay or advance using

$$|\angle {\rm S}_{21}| = |\angle {\rm S}_{12}| = \phi \tag{3}$$

$$ {\rm S}_{11} = {\rm S}_{22} = 0 \tag{4}$$

and are summarized in Fig. 7. The low-pass Π network is preferred on silicon since it requires a single inductor.

Fig. 8 shows the switched-delay phase shifter using CMOS switches and the simplified circuit model of the bypass and phase delay states. With T_1 off and T_2 on, L_S and C_P form a low-pass Π network with a delay given by $\phi = \sin^{-1}(\omega_o L_S / Z_o)$. When T_1 is on and T_2 is off, L_R resonates with the parasitic capacitance of T_2, and L_S and

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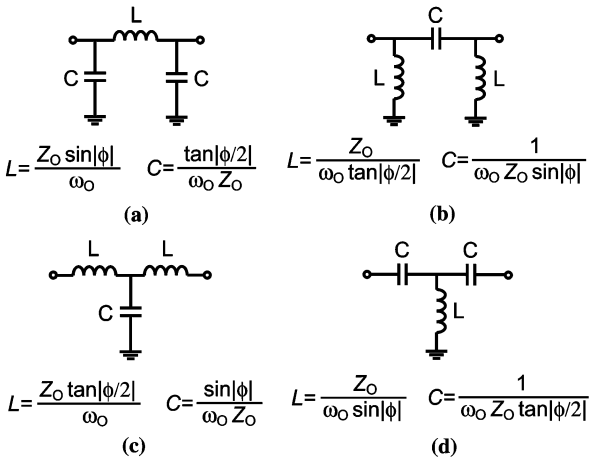

Fig. 7. (a) Low-pass Π. (b) High-pass Π. (c) Low-pass T and (d) high-pass T networks with $|\phi|<90^\circ$ insertion phase and perfect matching to Z_o at ω_o.

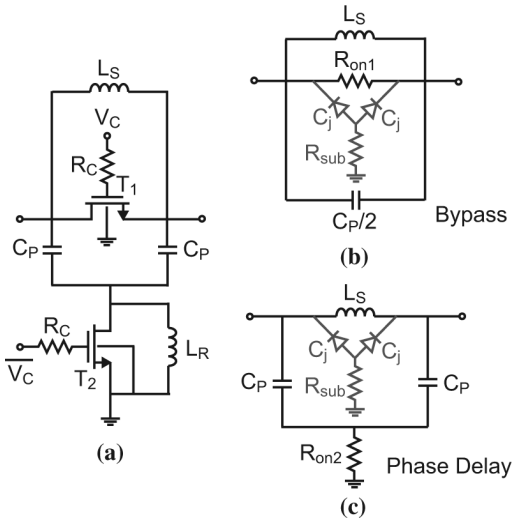

Fig. 8. (a) Single-ended CMOS 1-bit phase shifter and the simplified circuit model of the (b) bypass and (c) phase delay states.

$C_P/2$ are in parallel with the on-state resistance $(R_{\rm on1})$ of T_1. The total reactance of L_S and $C_P/2$ is

$$X_P = \frac{1}{\frac{1}{j\omega_o L_S + j\omega_o 2C_P}} \tag{5}$$

$$= \frac{Z_o}{\frac{1}{j\sin|\phi| + j2\tan\left|\frac{\phi}{2}\right|}} \tag{6}$$

$$= j\,2Z_o \tan\left|\frac{\phi}{2}\right| \tag{7}$$

and has minimal impact on the insertion phase of the bypass state as long as $X_P \gg R_{\rm on1}$. When X_P is comparable with $R_{\rm on1}$, the bypass state also results in a small phase delay, but the low-pass network can be designed to provide an extra phase delay so as to achieve the desired phase difference between the bypass and phase-delay states. Fig. 9 shows the simulated insertion phase of the 90° CMOS phase shifter. The bypass and phase delay states have 0° and − 90° insertion phase at 35 GHz. The insertion phase of the low-pass Π network is linear up to

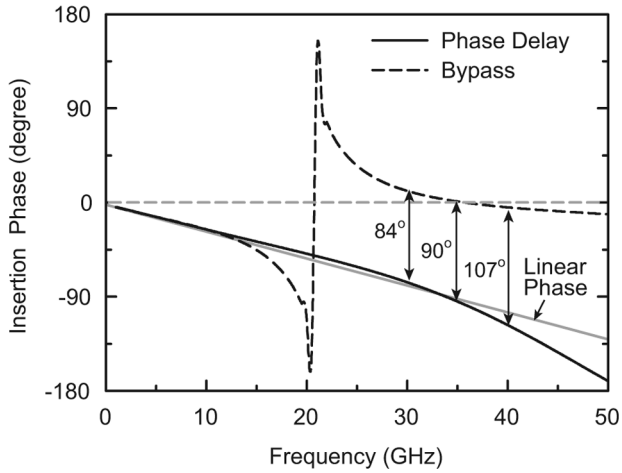

Fig. 9. Simulated insertion phase of the 1-bit CMOS 90° phase shifter.

35 GHz and the bypass state has a parasitic resonant frequency at $\omega = 1/\sqrt{L_R(C_{\rm eq}+2C_P)} = \omega_o/\sqrt{2C_P/C_{\rm eq}+1}$ due to C_P. Still, one can achieve good performance at 28-40 GHz.

The 4-bit phase shifter is designed using five stages of switched-delay networks (Fig. 10). The first two stages are 90° phase shifters and are tied together to become the 180° bit. The 22.5°, 45°, and 90° phase bits are cascaded in series afterwards using 50 Ω lines. Each stage can operate in either a bypass or low-pass (delay) mode. The values of the spiral inductors (L_S and L_R) and MIM capacitors (C_P) are optimized using full-wave electromagnetic simulations and take into account the parasitics of T_1 and T_2. The 45° phase bit is designed with two shunt capacitors (C_{P2}) in series due to the minimum available MIM capacitor value. In the case of the 22.5° phase shifter bit, the parasitic capacitances of L_{S2} and T_1 are large enough to effectively become the shunt capacitor of the low-pass network, and L_M matches the junction capacitance for the bypass states. The L and C values are summarized in the table of Fig. 10.

The chip photograph of the single-ended phased shifter is shown in Fig. 11. A tapered transition from G-S-G pads to the microstrip line provides a 50 Ω input and output impedance. Inductors are surrounded closely by ground planes to reduce their distance and cross-coupling, and the parasitics are taken into account. The chip size is 530×220 μm^2 $(<0.12$ mm$^2)$ without pads. The CMOS phase shifter does not consume any static power, and results in a simulated average insertion loss of 12 dB at 35 GHz.

D. Differential 4-Bit Phase Shifter

The differential phase shifter is also designed using the low-pass Π networks. Fig. 12(a) presents a single bit and its differential series switch model. Since the switches operate differentially, the RF virtual ground of the substrate nodes are formed inside the substrate. This decreases $R_{\rm sub}$ of the differential switch compared to the single-ended switch since the substrate contact resistance $(R_{\rm subc})$ can be ignored and also the substrate resistance itself is decreased by a factor of 2. For the differential shunt switch, $R_{\rm sub}$ can be completely ignored in the design due to the virtual ground at the junction. The equivalent circuit models for the bypass and phase delay states are shown in Fig. 12(b)–(c), where C_{ds} is ignored since it is small.

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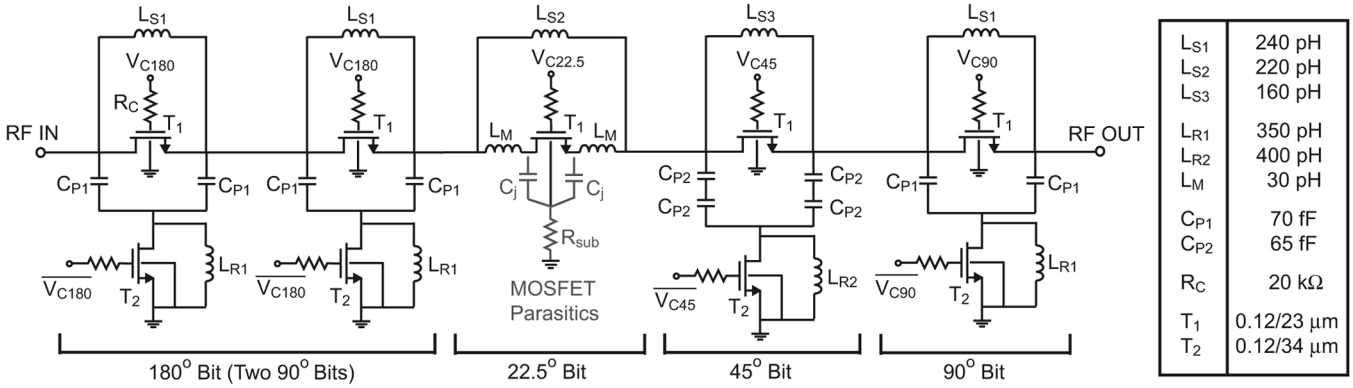

Fig. 10. Schematic of the single-ended Ka-band 4-bit CMOS phase shifter.

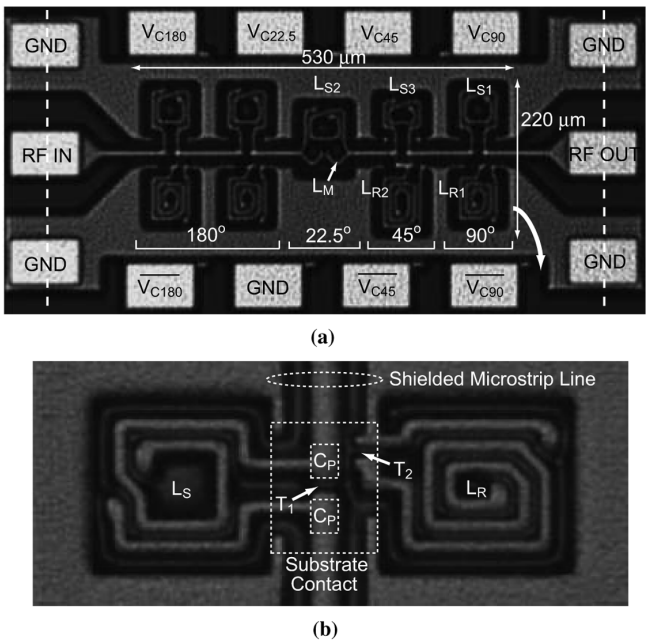

Fig. 11. Chip photographs of (a) the single-ended Ka-band phased shifter, and (b) a blow-up view of the 90° phase bit.

Because $R_{\rm sub}$ for the differential switch is small, the junction capacitances (C_j) of the series and shunt switches can be matched with input and output inductors, L_M, and therefore the gate width of the CMOS transistor can be enlarged. Also, the differential shunt switch can be designed without the resonating inductor. Fig. 12(b)–(c) also show the simplified differential half-circuit models for the bypass and phase delay states, and explain how the inductor and capacitor values are calculated. L_M is first designed to match the two junction capacitances of the series switch and the series combination (C_x) of $2C_P$ and C_j (of the shunt switch). C_x is almost C_j if $2C_P$ is large enough. Then, L_M and $1.5C_j$ can be considered as an impedance transformer between Z_o and Z_X, where $Z_X = Z_o(1+Q^2) = Z_o + \omega^2 L_M^2/Z_o$. Therefore, L_S and C_P of the low-pass Π network are calculated using the equations in Fig. 7 with Z_X instead of Z_o. In this case, the loss due to $R_{\rm on}$ becomes quite small because Z_X is larger than Z_o.

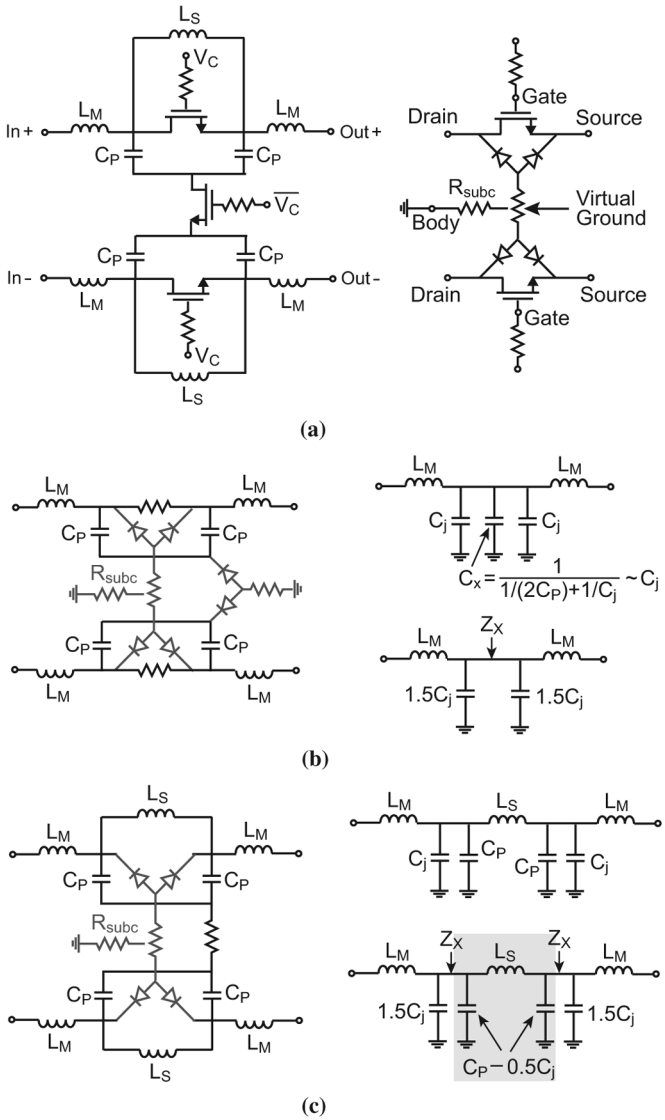

Fig. 12. (a) Differential CMOS 1-bit phase shifter with the differential CMOS switch, and the equivalent circuit and simplified half-circuit of (b) bypass and (c) phase delay states.

The 4-bit differential phase shifter is shown in Fig. 13. The 90° and 45° phase bits are based on the switched-delay networks using differential CMOS switches. The 180° phase bit is

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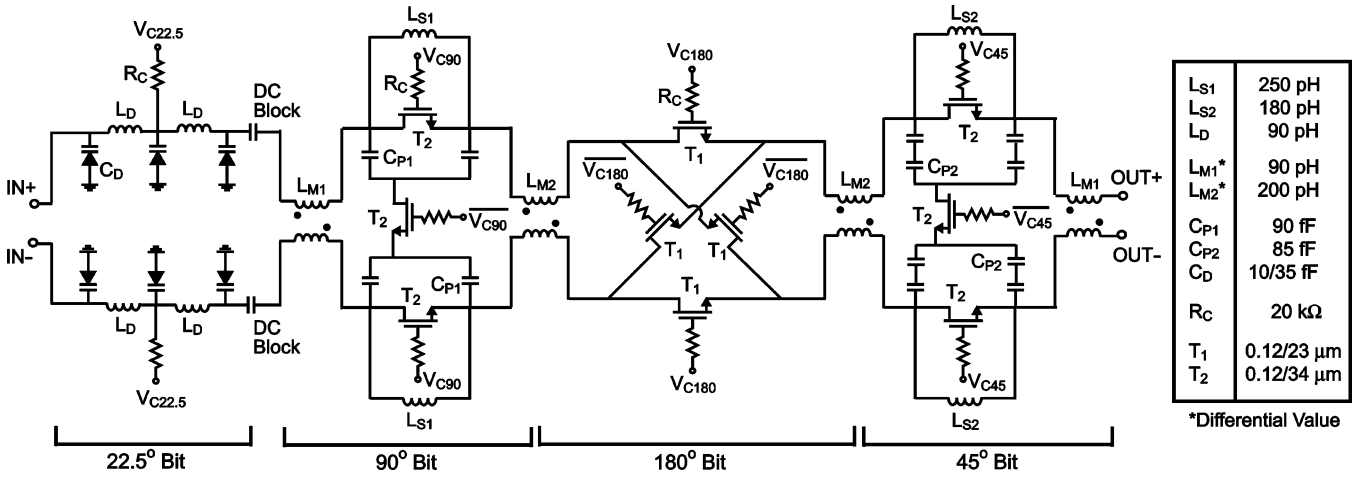

L_{S1}	250 pH
L_{S2}	180 pH
L_D	90 pH
L_{M1}*	90 pH
L_{M2}*	200 pH
C_{P1}	90 fF
C_{P2}	85 fF
C_D	10/35 fF
R_C	20 kΩ
T_1	0.12/23 μm
T_2	0.12/34 μm

Fig. 13. Schematic of the differential Ka-band 4-bit CMOS phase shifter.

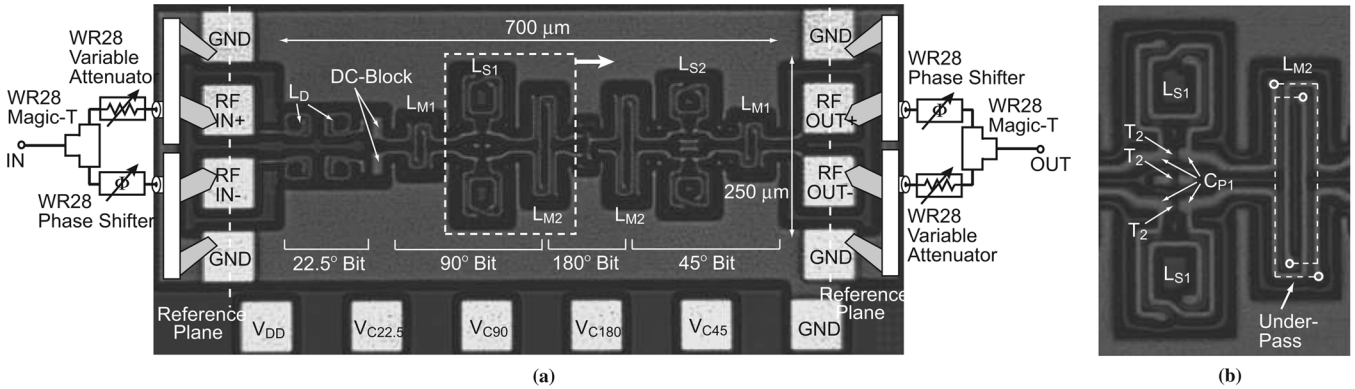

Fig. 14. Chip photograph of (a) the differential Ka-band phased shifter, and (b) the blow-up view of the 90° phase bit and L_{M2}. The Ka-band differential measurement setup is also shown together.

based on a differential CMOS quad switch with input and output matching inductors. The 180° phase bit is placed between the 90° and 45° phase bit and their input and output matching inductors are combined together. The matching inductors, L_M, for the differential paths are reversely coupled to each other so as to take advantage of the mutual coupling. The 22.5° phase bit is a loaded-line phase shifter using varactor diodes (HAVAR) [22]. The loaded line is composed of L_D and C_D, and has an impedance of 60 Ω for $C_D = 10$ fF ($V_{C22.5} = 2.5$ V) and 40 Ω for $C_D = 35$ fF ($V_{C22.5} = 0$ V) considering all the parasitics. The diode is operated in the digital mode ($V_{C22.5} = 0/2.5$ V) resulting in 22.5° phase difference. The junction area of the diode is $4 \times 4\ \mu\text{m}^2$, and the Q is 4-11 for the reverse bias voltage of 0-2.5 V. The final L and C values of the differential phase shifter are obtained using full-wave simulation and summarized in Fig. 13.

Fig. 14 presents the chip photograph of the differential phase shifter. Inductors are also surrounded closely by ground planes, and all parasitics are taken into account using full-wave simulation. The differential matching inductors (L_M) are designed using the two top metal layers to maximize the mutual coupling and the under-pass of the inductors is shown in Fig. 14(b). The CMOS switches are placed very close to each other to take the advantage of the differential switch topology by reducing the substrate resistance between the transistors. The chip size is $700 \times 250\ \mu\text{m}^2$ ($< 0.18\ \text{mm}^2$) without pads. The Ka-band 4-bit differential phase shifter also does not consume any static power, and results in an average insertion loss of 10 dB at 35 GHz.

III. Phase Shifter Measurements

A. Single-Ended 4-bit Phase Shifter

The single-ended phase shifter was measured on-chip using an Agilent E8364B network analyzer using SOLT calibration to the probe tips. Fig. 15 presents the measured S-parameters for the 16 different phase states. A input/output match of <-10 dB is obtained from 30-40 GHz. The combined input and output losses for the pad transitions (0.35-0.45 dB from 30 to 40 GHz) are not taken out of the measurements. The measured loss is 13 ± 1.1 dB at 34 GHz (12.6 ± 1.1 dB without pad losses), and agrees well with simulations. The rms gain error of the 16 different phase states is about 1 dB at the design frequency (35 GHz).

Fig. 16 presents the measured absolute phase performance of the single-ended phase shifter. The phase shifter is designed based on true time-delay networks, and therefore the phase steps increase with frequency. The rms phase error ($\Delta_{\text{rms}}\phi$) is calculated from a standard deviation of $\Delta\phi_n = \angle S_{21.n} - 22.5° \times n$,

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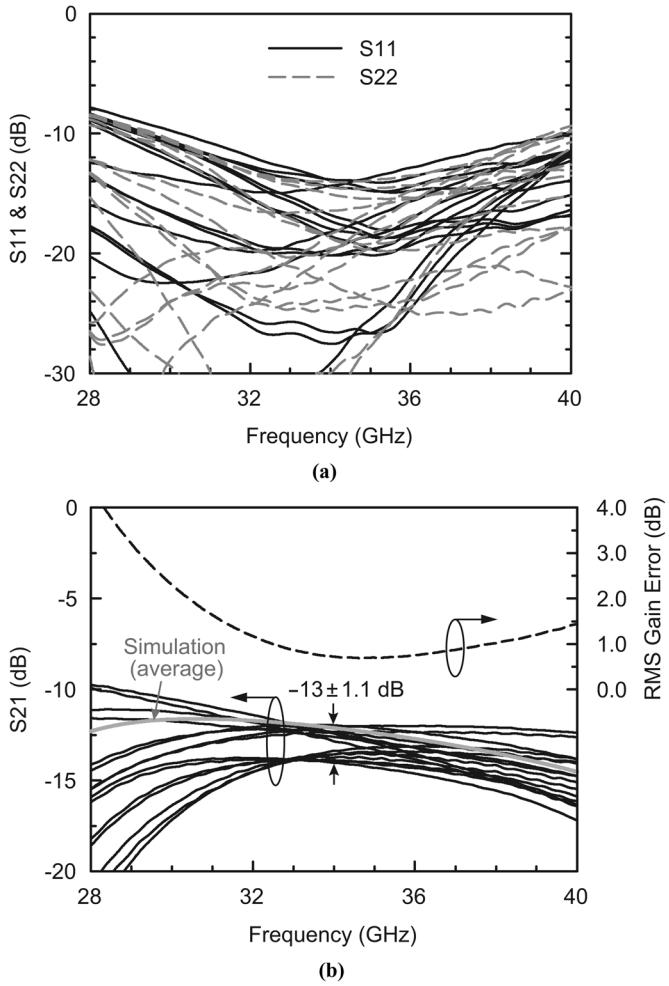

Fig. 15. Single-ended phase shifter: Measured (a) input and output return loss, and (b) insertion loss of 16 different phase states and the rms gain error.

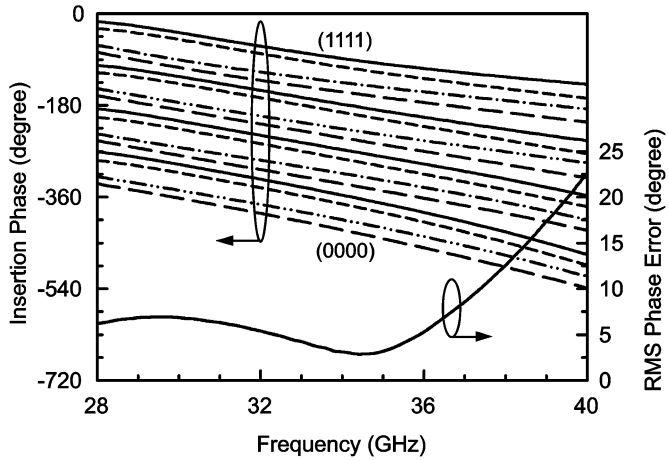

Fig. 16. Single-ended phase shifter: Measured insertion phase of 16 different phase states and the rms phase error.

and is 4° at 35 GHz. The rms phase error at 28-38 GHz is still less than 11.25°, which is the fifth significant bit and this has virtually no detrimental effect on the phased array performance.

Fig. 17 presents the insertion loss of each bit of the phase shifter versus the input power (measured separately). The power

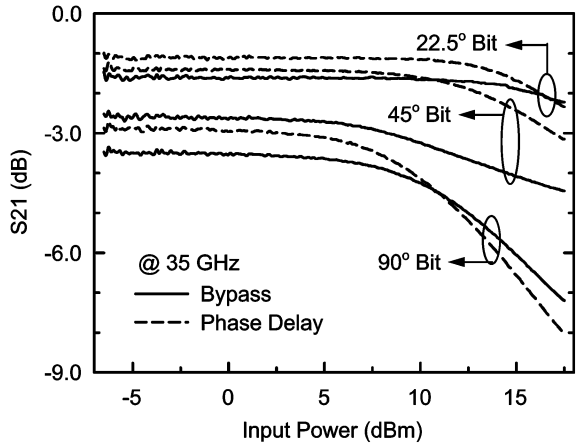

Fig. 17. Single-ended phase shifter: Measured insertion loss of the each phase bit versus input power. The input and output pad transitions are de-embedded.

handling capability of the phase shifter is limited by the junction diode of the CMOS switch since this diode is forward biased when the peak signal voltage is >0.7 V in the negative swing. The $P_{1\mathrm{dB}}$ of the 90° phase bit is $+10$ dBm, and this sets the power handling limit. The 45° and 22.5° phase bit have a higher $P_{1\mathrm{dB}}$ since they are not as resonant as the 90° phase bit. The measured IIP3 at 35 GHz is $+21$–22 dBm depending on the phase state. This shows that passive CMOS phase shifters are very linear and can be placed after high-gain LNAs.

B. Differential 4-Bit Phase Shifter

The differential phase shifter was measured on-chip using an Agilent E8364B network analyzer and off-chip baluns [Fig. 14(a)]. A waveguide magic-T is used for the single-to-differential conversion, and a waveguide phase shifter and variable attenuator are also used for fine tuning the phase and amplitude imbalance. The system is then calibrated using a differential calibration substrate and the measured results are referenced to the input and output G-S-S-G pads.

The measured S-parameters for the 16 different phase states are shown in Fig. 18. The input return loss is less than -8 dB and the output return loss is less than -12 dB at 28-40 GHz. The input return loss is a bit high since the loaded-line phase shifter (22.5° phase bit) is not a perfectly matched phase shifter. The measured loss is 10 ± 1.2 dB at 34 GHz and is less than the single-ended phase shifter since the 180° phase bit is much more compact and contains a single series switch in each path. The rms gain error is <1 dB at 28-40 GHz [Fig. 18(b)]. This is lower and more constant versus frequency than the single-ended phase shifter because the differential design minimizes the effect of R_{sub} (due to the virtual ground).

Fig. 19 presents the measured absolute phase performance of the differential phase shifter and the rms phase error. The 90°, 45°, and 22.5° phase bits of the phase shifter are designed based on true time-delay networks, but the 0/180° phase bit is a constant-phase design. This results in a larger phase step at 28 GHz, and a slight phase overlap at 40 GHz. However, the phase steps are still relatively constant around the design frequency of 35 GHz, and the rms phase error is still $<15°$ over the 28-40 GHz range and only 4° at 35 GHz. The measured IIP3

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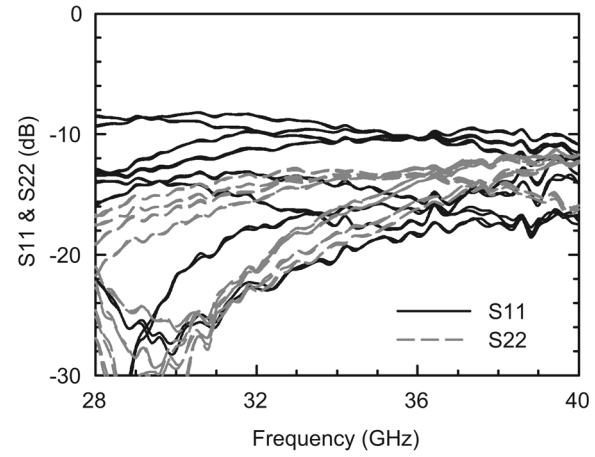

Fig. 18. Differential phase shifter: Measured (a) input and output return loss, and (b) insertion loss of 16 different phase states and the rms gain error.

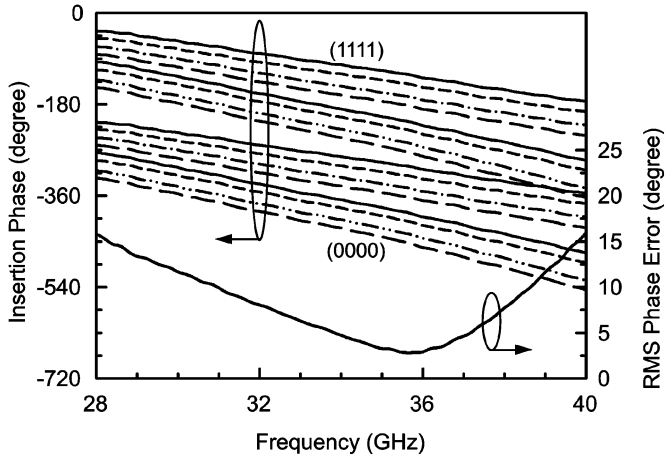

Fig. 19. Differential phase shifter: Measured insertion phase of 16 different phase states and the rms phase error.

is +16–17 dBm depending on the phase state and is limited by the 22.5° phase bit which is based on HAVAR diodes. The differential phase shifter with an all CMOS transistor implementation should have an IIP3 $>$ 23 dBm.

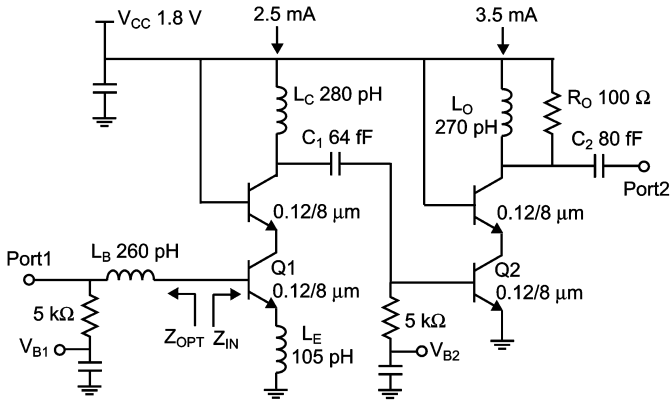

Fig. 20. Schematic of the single-ended Ka-band HBT low-noise amplifier.

IV. Low-Noise SiGe Amplifier and Gain Control

The single-ended and differential phase shifters have low phase errors, but have a loss of 10-13 dB. Therefore, it is important to build an LNA to improve the phased array gain and noise figure. The phase shifters can handle a high input power ($P_{1\mathrm{dB}} = 10$ dBm), and therefore the total system linearity is not limited by the phase shifter even with a high gain LNA.

A. Single-Ended LNA

A compact two-stage LNA is designed for the receiver front-end and has been presented in [23] (Fig. 20). The first stage of the LNA is based on an inductively degenerated cascode amplifier [24]. The emitter length (ℓ_E) of Q_1 is scaled so that the optimal (noise-matching) resistance ($R_{\mathrm{OPT}} = \mathrm{real}(Z_{\mathrm{OPT}})$) equals to about 75 Ω and results in $\ell_E = 8$ µm and a collector current $I_C = 2.5$ mA. The degeneration inductor, L_E minimizes the difference between the optimal (noise-matching) impedance (Z_{OPT}) and the input impedance ($Z_{\mathrm{IN}}{}^*$). The base inductor, L_B (and its parasitics), is the input matching network transforming the input impedance Z_{IN} to $Z_o = 50\ \Omega$.

The second amplifier stage is a duplicate of the first stage without L_E and is biased at $I_C = 3.5$ mA. The output of the LNA needs to be well matched to the following phase shifter and the output resistance ($R_O = 100\,\Omega$) increases the matching bandwidth. The LNA core area is less than 0.1 mm^2, and the measured gain and noise figure are 23.5 dB and 2.9 dB, respectively. The LNA consumes 11 mW (6 mA, 1.8 V), and the measured input $P_{1\mathrm{dB}}$ and IIP3 at 35 GHz are −28 dBm and −19 dBm , respectively. A 10-50 GHz CMOS variable attenuator was also developed for the gain control of the single-ended receiver and is reported in [25].

B. Differential Variable Gain LNA

A differential variable gain LNA (VG-LNA) is designed for the differential phase shifter (Fig. 21). The first stage of the VG-LNA is a differential version of the first stage of the single-ended LNA with a slightly lower bias current (1.5 mA for a half-circuit) to reduce the power consumption. The $\mathrm{NF}_{\mathrm{min}}$ increases only by 0.1 dB due to the low bias current. The emitter degeneration inductor (L_E) and base inductor (L_B) provide simultaneous input optimum noise and power matching. The second stage is a 3-bit VGA, and using x2 and x4 larger transistors for 3-bit operation (eight different gain states) [26]. The

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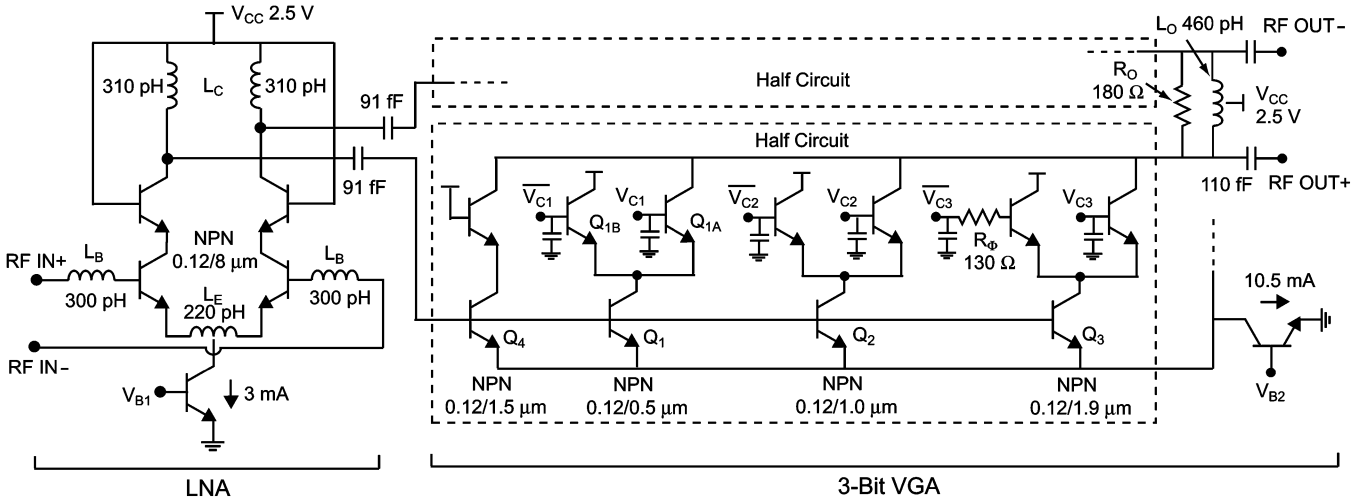

Fig. 21. Schematic of the differential Ka-band variable-gain low-noise amplifier (VG-LNA).

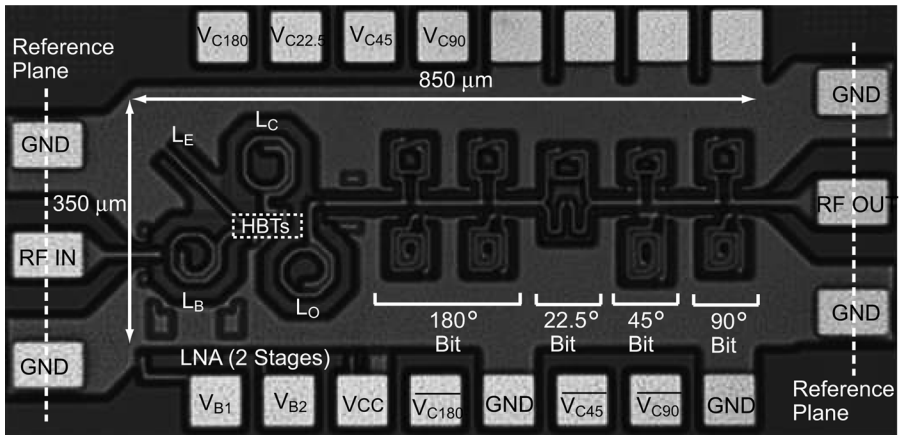

Fig. 22. Chip photograph of the single-ended Ka-band phased array BiCMOS front-end.

VGA stage can be controlled linearly in magnitude, and the minimum gain is defined by the cascode amplifier (Q_4) which always amplifies the signal.

The 3-bit VGA is designed such that the transistors $(Q_1$–$Q_4)$ are biased with a constant current, and therefore its input impedance does not change over the different gain states. This is important because the insertion phase of the VG-LNA varies significantly if the 3-bit VGA impedance is not constant. As is well known, the VG-LNA must have a very low insertion phase variation over the different gain states (phase imbalance) to avoid a complex phase/amplitude calibration for the phased-array system [1]. The resistor R_Φ for $\overline{V_{C3}}$ control line minimizes the phase imbalance further by changing the insertion phase slightly when V_{C3} is low. The VG-LNA core area is less than 0.15 mm^2 and consumes 33 mW (13.5 mA, 2.5 V). The simulated input and output return loss are < -13 dB at 30-40 GHz with a maximum/minimum gain of 23/11 dB at 35 GHz.

V. Front-End Measurements

A. Single-Ended LNA/Phase Shifter

The single-ended front-end is shown in Fig. 22. The matching inductor L_M of the 22.5° phase bit is increased a bit ($L_M =$ 70 pH) for better input and output matching. The total chip size 850×350 μm^2 and is <0.3 mm^2. The gain and phase of the front-ends were measured on-chip using SOLT calibration to the probe tips. The noise figure was measured using an Agilent 346CK01 noise source and the noise figure measurement personality of the Agilent E4448A spectrum analyzer. Two Ka-band preamplifiers are used in front of the spectrum analyzer and result in a 0.2 dB noise figure uncertainty.

The measured gain and noise figure for all 16 different phase states are shown in Fig. 23(a). The single-ended front-end results in 11 $\pm$ 1.5 dB of gain at 34 GHz with an associated noise figure of <3.4 dB. The input return loss for all 16 different phase states is very close to the LNA input characteristics due to the high reverse isolation of the LNA ($S_{11}< -$ 15 dB at 30-40 GHz). The output return loss of the single-ended front-end is similar to the single-ended phase shifter [$S_{22} < -10$ dB at 30-40 GHz, see Fig. 15(a)]. These results agree very well with simulations. The measured input $P_{1\mathrm{dB}}$ and IIP3 at 35 GHz are -28 dBm and -22 dBm , respectively, and are limited by the LNA rather than the phase shifter.

Fig. 23(a) presents the measured absolute phase performance and rms phase error of the the single-ended front-end. Two different rms phase errors are calculated using a constant-phase

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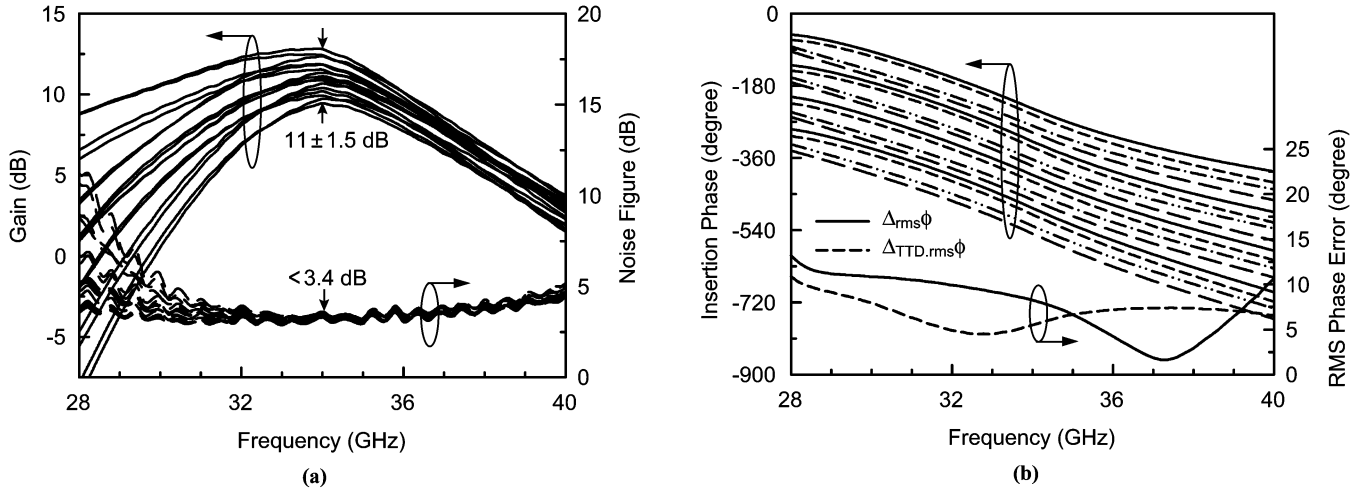

Fig. 23. Single-ended front-end: Measured (a) gain and noise figure, and (b) insertion phase and rms phase error of 16 different phase states.

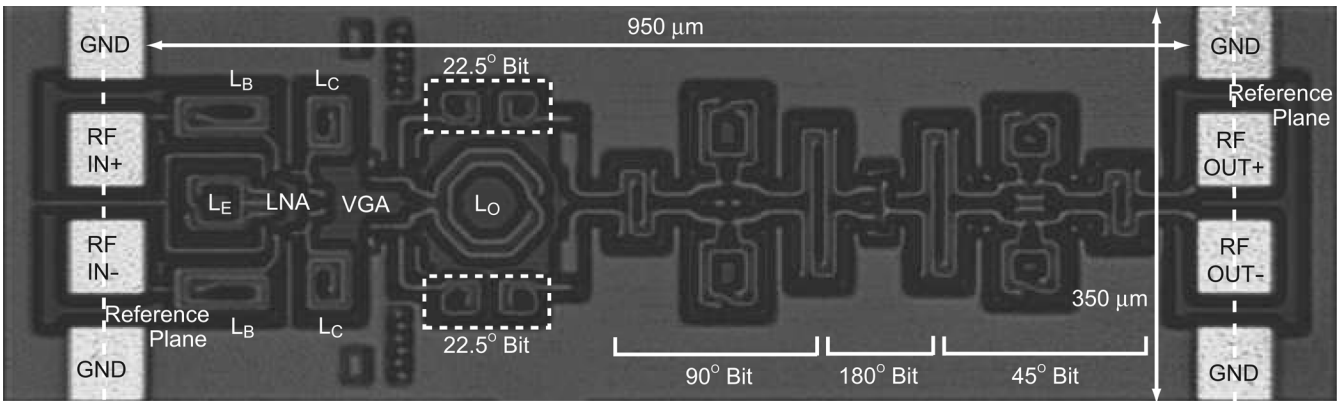

Fig. 24. Chip photograph of the differential Ka-band phased array BiCMOS front-end (bias pads are not shown).

phase shift and a true time-delay (TTD) phase shift assumption. The phase steps of the true time-delay phase shifter increase linearly versus frequency and the rms error $(\Delta_{\mathrm{TTD.rms}}\phi)$ is based on $\Delta\phi_{\mathrm{TTD.n}} = \angle \mathrm{S}_{21.n} - (f/f_o) \times 22.5^\circ \times n$. It is seen that the single-ended front-end results in $<12.5^\circ$ of rms phase error at 28-40 GHz for either model ($\Delta_{\mathrm{rms}}\phi$ and $\Delta_{\mathrm{TTD.rms}}\phi$).

B. Differential VG-LNA/Phase Shifter

The chip photograph of the differential front-end is shown in Fig. 24. The entire chip size is $950 \times 350\ \mu\mathrm{m}^2$ and is $< 0.34\ \mathrm{mm}^2$. The gain and phase of the front-end were measured on-chip using the same method for the differential phase shifter (see Fig. 14). The noise figure was also measured using the Agilent 346CK01 noise source and the noise figure measurement personality of Agilent E4448A spectrum analyzer with two Ka-band preamplifiers. The loss of the off-chip balun and the G-S-S-G probes are measured using the back-to-back configuration and are subtracted from the measurement.

Fig. 25(a) presents the measured gain and noise figure of the differential front-end. The gain is 10 ± 1.3 dB at 33 GHz for the maximum gain state of the VG-LNA. The noise figure is measured for the 0° and 337.5° phase states because these represent the highest and lowest loss states of the differential phase shifter. The noise figure is < 3.8 dB for the maximum gain state of the VG-LNA.

Fig. 25(b) presents the measured absolute phase performance and rms phase error of the differential front-end. Both $\Delta_{\mathrm{rms}}\phi$ and $\Delta_{\mathrm{TTD.rms}}\phi$ are 4° at 35 GHz, and less than 20° at 28–40 GHz. $\Delta_{\mathrm{rms}}\phi$ and $\Delta_{\mathrm{TTD.rms}}\phi$ of the differential front-end are very similar since the phase shifter is composed of both a true-time delay phase bit (90°, 45°, and 22.5°) and a constant phase bit (180°). All the measurements agree well with simulations.

The gain variation of the VG-LNA is 9-20 dB with a constant gain step in magnitude, and the rms phase imbalance of the VG-LNA is $< 2.5^\circ$ at 28-40 GHz and only 0.7° at 32-34 GHz. Therefore, the gain imbalance of the phase shifter can be compensated without increasing the phase error. Fig. 26 presents the differential front-end gain with gain-error compensation, and the compensated gain is 9.1 ± 0.45 dB at 33 GHz (rms gain error of < 0.35 dB). This is sufficient for phased arrays with very low sidelobe levels. Fig. 26 also shows the input and output return loss of the differential front-end over all phase states. The input return loss is set by the VG-LNA and is < -13 dB and the output return loss is < -10 dB. The measured input $P_{1\mathrm{dB}}$ is -28 dBm at 35 GHz for all eight different gain states and the measured input IIP3 at 35 GHz is -20 dBm. Again, the

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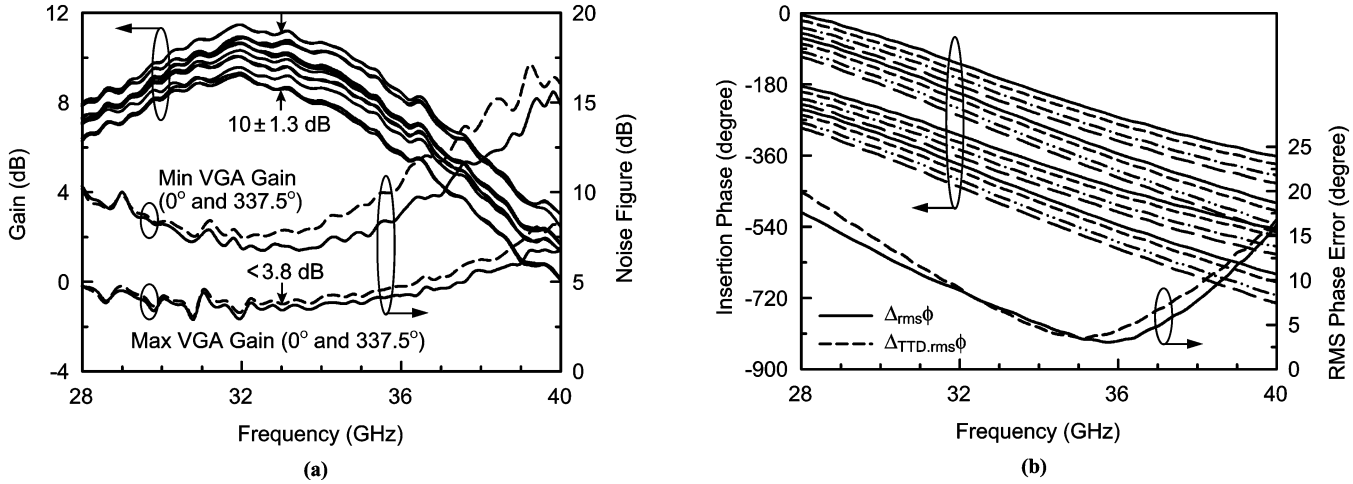

Fig. 25. Differential front-end: Measured (a) gain and noise figure, and (b) insertion phase and rms phase error of 16 different phase states.

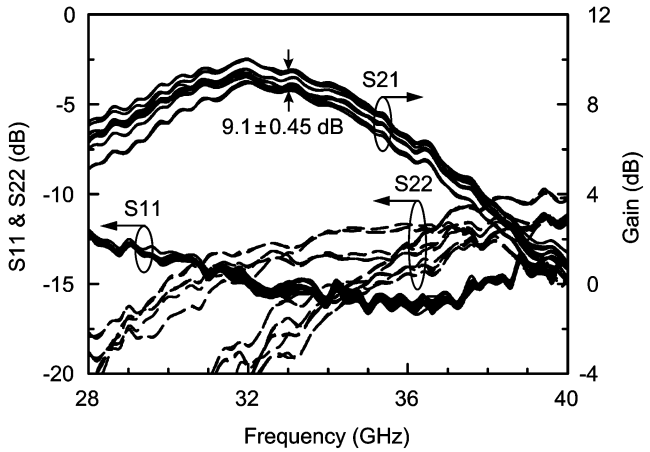

Fig. 26. Differential front-end: Measured compensated gain and return loss for 16 different phase states.

$P_{1\mathrm{dB}}$ and IIP3 are limited by the VG-LNA and not by the phase shifter.

VI. Conclusion

There is no doubt that GaAs and InP technologies have dominated the phased array front-ends for the past twenty years, and this paper shows that it is possible to obtain state-of-the-art passive phase shifters and LNA/phase shifters at the Ka-band frequency range using a standard silicon BiCMOS technology. The passive phase shifters have high linearity (IIP3 $> +21$ dBm) and can be placed after high-gain high-linearity GaAs/InP amplifiers for high interference systems. The phased array front-end has also been implemented in a differential design, which is beneficial for high density (multiple-element) integration and low on-chip coupling. The silicon front-ends occupy a very small area, and can be arrayed in 4–16 elements on a single silicon chip for compact Ka-band phased-array modules. The silicon modules will not replace the GaAs/InP power amplifier and very low noise amplifier (NF of 1-2 dB at 35 GHz) but can significantly reduce the cost of the back-end (phase shifters, VGA, combiner, etc.) in defense-based and satellite communication systems.

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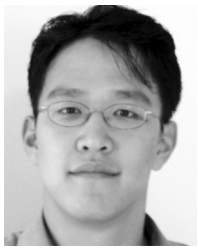

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