# 60 GHz 7-Bit Passive Vector-Sum Phase Shifter With an X-Type Attenuator

Geon-Ho Park, Chul Woo Byeon, *Member, IEEE*, and Chul Soon Park, *Fellow, IEEE*

***Abstract*—This brief presents the design of a 60 GHz passive vector-sum phase shifter with 7-bit phase resolution. An analog X-type attenuator with complementary voltage control was used for vector modulation. The proposed attenuator is suitable for high-resolution phase shifter design because it is capable of phase inversion and shows a large attenuation range with low-phase variation. The prototype phase shifter fabricated through the 65 nm CMOS process occupies an area of 0.24 mm$^2$ (excluding the bonding pads). The measurement results show that the proposed phase shifter achieves a phase resolution of 2.815° while exhibiting an average insertion loss of 14 dB without DC power consumption. The calculated RMS gain and phase error were below 0.55 dB and 0.83–2.36°, respectively, in the range of 57–67 GHz.**

***Index Terms*—60 GHz, bidirectional, CMOS, millimeter wave, phase shifter, vector modulation, vector-sum phase shifter, X-type attenuator.**

## I. Introduction

THE PHASED array technique is essential in millimeter-wave band communication systems, wherein the phase shifter is the principal component in implementing a phased array [1]. The phase shifter controls the phase state of the phased array channel and consequently forms a beam. Therefore, the phase resolution of the phase shifter determines the beam-steering resolution of the phased array system, and a high phase resolution is necessary to achieve adequate performance for a large-sized phased array system [2], [3].

Phase shifters are classified into active and passive structures, each having its advantages and disadvantages. However, the passive structure is superior in terms of wideband design, DC power consumption, linearity, and bidirectionality. Thus, a passive phase shifter is more suitable for implementing a millimeter-wave-band, low-power, wideband, time-division-duplexed phased array transceiver [4], [5], [6], [7], [8], [9], [10], [11], [12].

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Switched filter-type phase shifters (STPSs) [4], [5], [6] and reflective-type phase shifters (RTPSs) [8] are the most popular passive phase shifter topologies. However, STPS requires gain compensation, so additional power consumption by variable gain amplifier (VGA) [4] or additional loss due to loss compensation [6] is required, and RTPS has a limitation in that it is difficult to achieve a 360° phase shift range in a wide bandwidth.

By contrast, the vector-sum phase shifter (VSPS) shifts the phase through gain control of the in-phase (I) and quadrature (Q) signals [9]. Thus, a 360° phase shift range can be easily achieved, and the gain error between the phase states is small. While the VSPS is usually implemented as an active structure, it can also be implemented as a passive structure by using an attenuator rather than a VGA. Step [10], reflective-type [11], and digital X-type [12] attenuators have been used for passive vector modulation. The step-attenuator-based VSPS requires an additional block for phase inversion and exhibits large IL. The reflective-type attenuator is phase-invertible and has a wide gain control range; however, it occupies a large area and exhibits high IL. The digital X-type attenuator occupies a small area, enables phase inversion, and has a wide gain control range. However, because many bits of transistor switches are required in high-resolution phase shifter design, the IL increases, and the layout becomes complicated.

Herein, a 60 GHz 7-bit passive VSPS is proposed for achieving high phase resolution with low loss; to this end, an X-type attenuator with complementary voltage control was used in the VSPS. The proposed attenuator can precisely control the gain and invert the phase while minimizing impedance and phase variation. To further reduce the loss, a body-floating technique was adopted. Therefore, the proposed scheme is suitable for high-resolution passive VSPSs.

## II. Circuit Design

### A. X-Type Attenuator With Complementary Voltage Control

Fig. 1(a) shows a core schematic of the proposed X-type attenuator. It consists of four n-MOS transistors serving as variable resistors instead of multiple digital transistor switches to achieve high resolution with low loss. To further decrease the IL, a body-floating technique was adopted for all transistors [5]. In the proposed attenuator, the sum of the two control voltages, $V_{C1}$ and $V_{C2}$, is always constant; in this brief, this sum was set to 1 V.

As shown in Fig. 1(b), a body-floated n-MOS resistor can be modeled as parallel resistance and capacitance. Using the

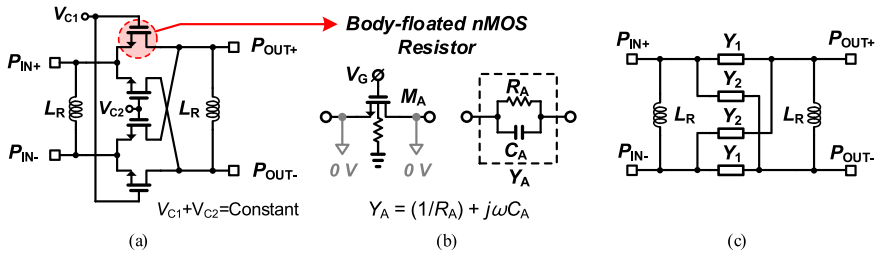


Fig. 1. (a) Schematic of the proposed X-type attenuator. (b) Simplified equivalent model of body-floated n-MOS as a variable resistor. (c) Equivalent model of X-type attenuator.

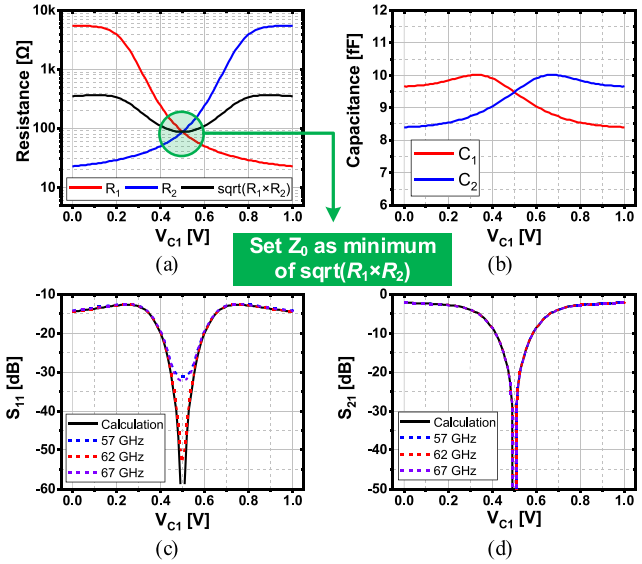


Fig. 2. (a) $R_1$, $R_2$ and $\sqrt{R_1R_2}$ with respect to $V_{C1}$. (b) $C_1$ and $C_2$ with respect to $V_{C1}$. (c) Calculated and simulated $S_{11}$. (d) Calculated and simulated $S_{21}$.

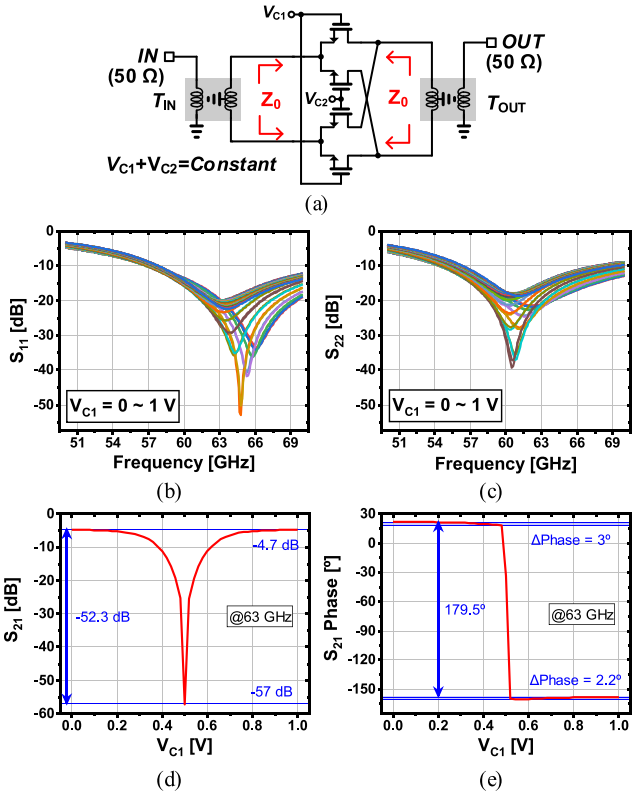


Fig. 3. (a) Complete schematic of the proposed attenuator. (b) Simulated $S_{11}$. (c) Simulated $S_{22}$. (d) Simulated $S_{21}$ with respect to $V_{C1}$ at 63 GHz. (e) Simulated $S_{21}$ phase with respect to $V_{C1}$ at 63 GHz.

model in Fig. 1(b), an equivalent model of the X-type attenuator is shown in Fig. 1(c). $Y_1$ and $Y_2$ are the equivalent admittances of body-floated n-MOS resistor controlled by $V_{C1}$ and $V_{C2}$, respectively, and can be summarized as follows:

$$Y_1 = (1/R_1) + j\omega C_1, \tag{1}$$

$$Y_2 = (1/R_2) + j\omega C_2, \tag{2}$$

where $R_1$, $R_2$, $C_1$, and $C_2$ are the equivalent resistances and capacitances controlled by $V_{C1}$ and $V_{C2}$, respectively.

Fig. 2(a) and 2(b) show the $R_1$, $R_2$, $C_1$, and $C_2$ values corresponding to $V_{C1}$ of an n-MOS resistor with size 15 µm. Fig. 2(b) shows insignificant change in $C_1$ and $C_2$ with respect to $V_{C1}$, therefore $C_1 \cong C_2 = C_P$. Assuming that shunt inductor $L_R$ resonates with $C_P$ and the input/output impedance is $Z_0$, S-Parameters of X-type attenuator are expressed as [12]:

$$S_{11} = S_{22} = \frac{R_1R_2 - Z_0^2}{(R_1 + Z_0)(R_2 + Z_0)}, \tag{3}$$

$$S_{21} = S_{12} = \frac{(R_2 - R_1)Z_0}{(R_1 + Z_0)(R_2 + Z_0)}. \tag{4}$$

Fig. 2(a) shows the complimentary change in values of $R_1$ and $R_2$ such that the sum of $V_{C1}$ and $V_{C2}$ is maintained constant. This control scheme provides two advantages. First, by minimizing the change in the value of $R_1R_2 - Z_0^2$ in (3), the input and output return loss can be maintained below −10 dB regardless of the gain state. Second, as shown in (4), because the gain is determined by $R_2 - R_1$, it can be controlled. The results of calculating (3) and (4) using the values of $R_1$ and $R_2$ are shown in Fig. 2(c) and 2(d). In addition, simulated $S_{11}$ and $S_{21}$ of the X-type attenuator are also shown in Fig. 2(c) and 2(d). In (3) and (4), $Z_0$ was set to 87 Ω, which is the minimum value of $\sqrt{R_1R_2}$. Fig. 2(c) and 2(d) show a good agreement between the calculated and simulation results. In particular, Fig. 2(c) shows that even at 57 and 67 GHz, outside the resonant frequencies of $C_P$ and $L_R$ of 62 GHz, the proposed attenuator still exhibited a return loss of less than −10 dB regardless of the gain state because $C_P$ is small [12]. The proposed attenuator has a small $C_P$ for two reasons. First, the use of multiple transistor switches was avoided. Second, the body-floating technique was adopted. Another advantage of the proposed attenuator is that because

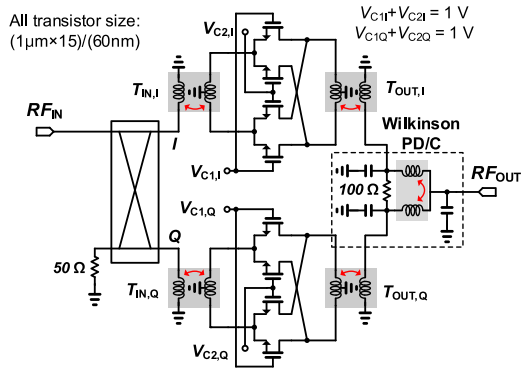


Fig. 4. Schematic of the proposed VSPS.

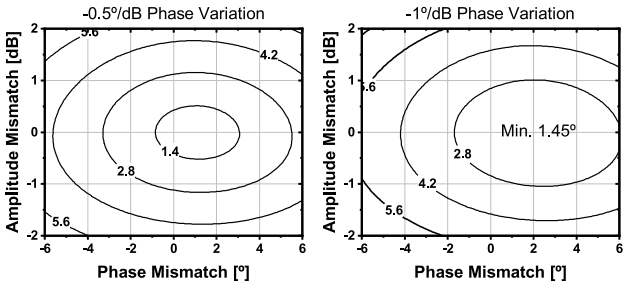


Fig. 5. Calculated RMS phase error for the I/Q amplitude and phase mismatch of the 7-bit VSPS when an attenuator with phase variations of −0.5 and −1 °/dB is used as the vector modulator.

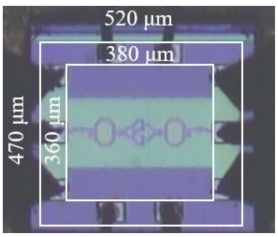


Fig. 6. Chip micrograph of the X-type attenuator.

(4) consists only of real parts, it exhibits phase-invariant gain control characteristic.

Fig. 3(a) shows the complete schematic of the proposed X-type attenuator. Transformers were inserted at the input and output to convert the impedance from a differential $Z_0$ to single-ended 50 Ω and to obtain $L_R$ as shown in Fig. 1(a). Fig. 3(b)–(e) show simulation results of proposed X-type attenuator. The simulation also reflected the effects of routing in the attenuator and parasitic components of the transistor. The simulation results indicate that the analog X-type attenuator with complementary voltage control has a wide gain control range with low phase and impedance variation. The simulated lowest IL of the X-type attenuator is 4.7 dB.

### *B. Proposed 7-Bit Passive VSPS*

Fig. 4 shows a schematic of the proposed 7-bit passive VSPS. A transformer-based quadrature coupler was used to generate the I and Q signals. Unlike polyphase filters, transformer-based couplers can generate I/Q signals with low

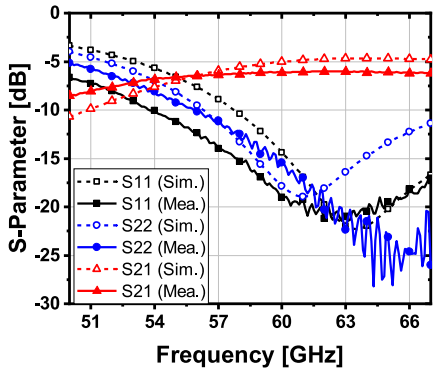


Fig. 7. Simulated and measured S-Parameter of the X-type attenuator at the lowest IL state.

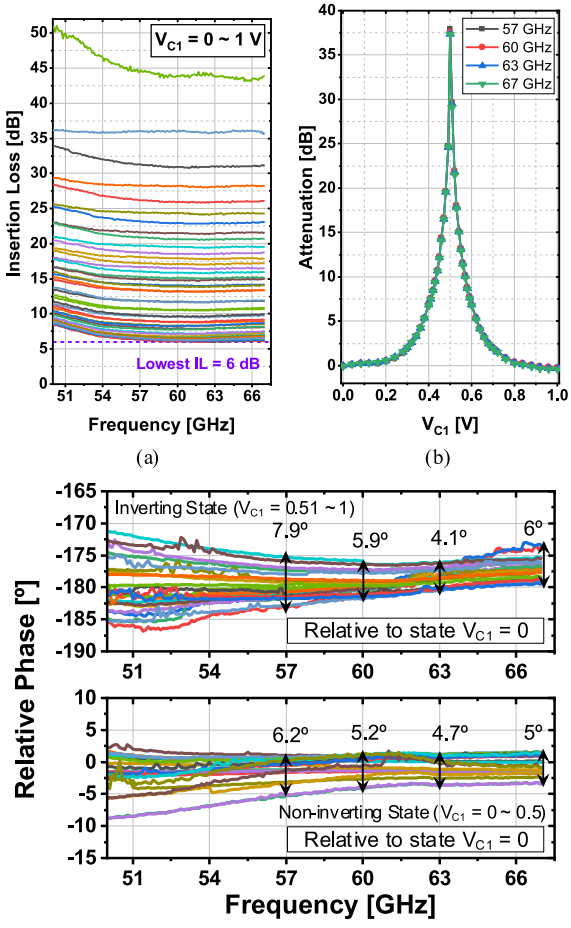


Fig. 8. Measured IL (a) as a function of frequency and (b) as a function of control voltage at 57, 60, 63, and 67 GHz. (c) Measured relative phase.

losses. The simulated I/Q gain and phase mismatch are less than 0.69 dB and 0.3° in the 57–67 GHz range, respectively.

Fig. 5 shows the calculated RMS phase error contours for the I/Q gain and phase mismatch when the attenuator has a phase variation of –0.5 and –1 °/dB in a 7-bit VSPS. The graph illustrates that the RMS phase error increases as the phase variation of the attenuator increases. The proposed X-type attenuator overcomes this limitation as it exhibits a wide gain control range with low-phase variation, as shown in Fig. 3(d) and 3(e) (3° phase variation for 52 dB gain control). Finally,

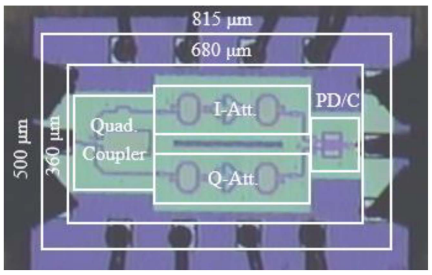


Fig. 9. Chip micrograph of the 7-bit passive VSPS.

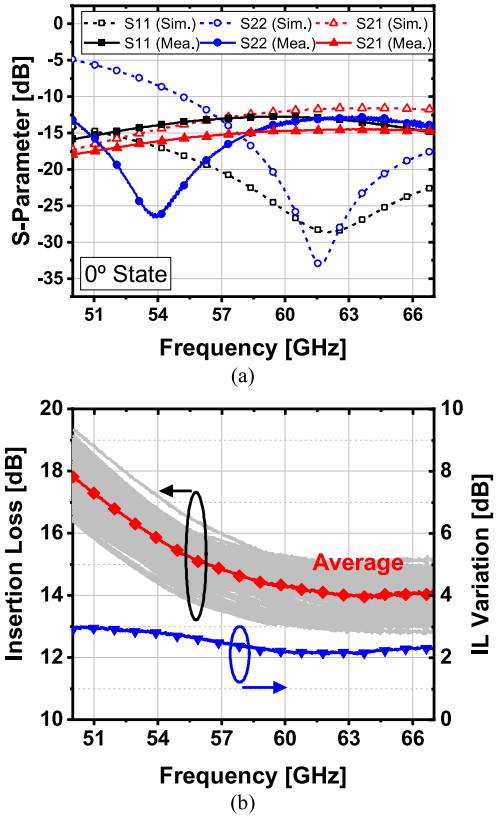


Fig. 10. (a) Measured S-Parameter (b) Measured IL and IL variation for all phase states.

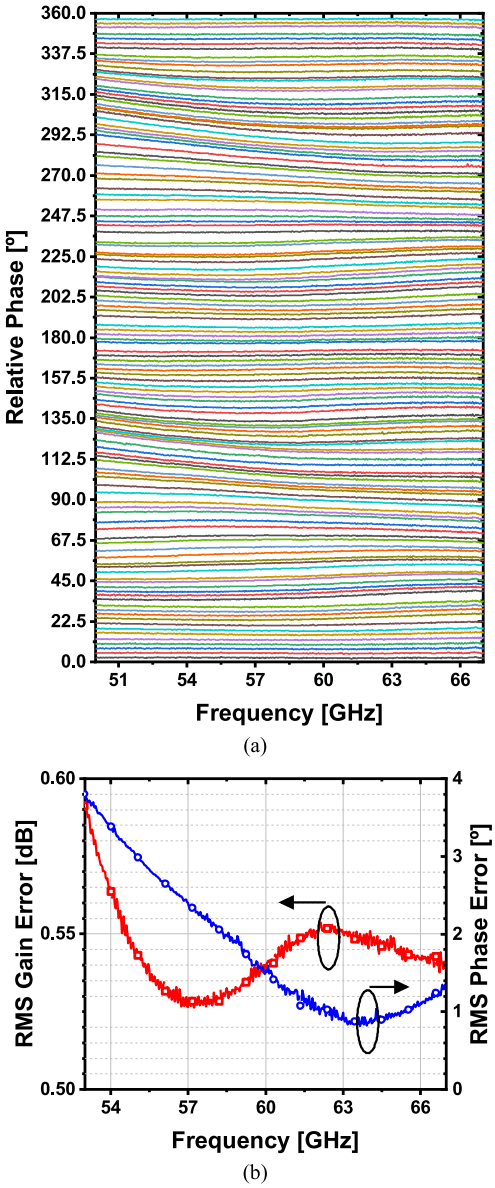


Fig. 11. (a) Measured S-Parameter (b) Measured IL and Measured RMS phase/gain error.

the gain-controlled I and Q signals are combined using a Wilkinson combiner [13]. The Wilkinson combiner provides a higher isolation between the two ports than the directly combined structure. Therefore, the gain and phase errors due to impedance variations during gain control in the I and Q paths are minimized.

## III. Experimental Results

### A. X-Type Attenuator

Fig. 6 shows a micrograph of an X-type attenuator fabricated for testing purposes, with a core size of 0.38 × 0.36 mm$^2$. Fig. 7 shows the simulated and measured S-Parameters of the attenuator in the highest gain state. Clearly, $S_{11}$ was less than −10 dB from 54 to 67 GHz, $S_{22}$ was less than −10 dB from 56 to 67 GHz, and the lowest measured IL was 6 dB, which is degraded compared with the lowest simulated IL of 4.7 dB. This might be because of the difference in the on-resistance of the transistor. Fig. 8(a) and 8(b) show the gain corresponding to frequency and control voltage at the four frequencies, respectively. The measurement results indicate that the proposed attenuator has an attenuation range of 37 dB in the 60 GHz band. Fig. 8(c) shows the phase response of the attenuator. In the plots, the state $V_{C1} = 0$ V was defined as the reference state. In the range of 57–67 GHz, the phase variation of the attenuator was less than 7.9° and 6.2° in the inverted and non-inverted states, respectively. The phase variation increased compared with the simulation, which might be due to the mismatch between the transistors and the increase in parasitic capacitance.

### B. 7-Bit Passive VSPS

Fig. 9 shows a micrograph of the fabricated 7-bit passive VSPS. The proposed VSPS, with a core size of 0.68 × 0.36 mm$^2$, was fabricated through a 65 nm CMOS process.

TABLE I
PERFORMANCE COMPARISON OF 60 GHZ BAND PASSIVE PHASE SHIFTERS

| | [4] | [5] | [6] | [7] | [8] | **This Work** |
|---|---|---|---|---|---|---|
| Process | 90 nm CMOS | 65 nm CMOS | 65 nm CMOS | 65 nm CMOS | 130 nm BiCMOS | 65 nm CMOS |
| Topology | STPS | STPS | STPS | STPS+RTPS | RTPS | VSPS |
| Frequency (GHz) | 57–64 | 57–66 | 57–66 | 57–64 | 59–64(1) | 57–67<br>60.4–67(4) |
| Phase Resolution (°) | 11.25 | 22.5 | 11.25 | 11.25 | <5(2) | 2.815 |
| Insertion Loss (dB) | 14.6±3 | 8.7±1.7 | <18.5 | 14.3±2 | 9.6–10.3(3) | 14±1.05 |
| RMS Gain Error (dB) | < 1.8 | 0.37–1.17 | <0.23 | 0.5–1.1 | N/A | < 0.55 |
| RMS Phase Error (°) | 2.2–10 | 2.1–5.5 | <8 | 4.4–9.5 | N/A | 0.83–2.36<br>< 1.4(4) |
| IP1dB (dBm) | N/A | 7.4 | 13 | >9.5 | 13.6 (Sim.) | 10.5 (Sim.) |
| Core Size ($mm^2$) | 0.34 | 0.092 | 0.44 | 0.094 | 0.16 | 0.24 |

(1) 360° phase shift possible, (2) not fixed, (3) at 62 GHz (4) RMS Phase Error < 1.4° range

Fig. 10(a) shows the simulated and measured S-Parameters in the 0° phase state. $S_{11}$ and $S_{22}$ show shapes different from the simulation results because of the effect of the pad; however, they still satisfy the $< -10$ dB condition from 50 to 67 GHz. The lowest measured IL was 14.6 dB, which is approximately 3 dB higher than the lowest simulated IL of 11.6 dB. This was mainly due to the increased IL of the X-type attenuator. Fig. 10(b) shows the measured IL for all phase states and the IL variation with the phase states. The lowest average IL for the 128 phase states was 14 dB, and the IL variation between phase states in the 60 GHz band was ∼2.1 dB. Fig. 11(a) shows the measured relative phase of the proposed VSPS, indicating that a phase shift of 360° was possible with a phase resolution of 2.815°. Fig. 11(b) shows the measured RMS phase and gain errors of the proposed VSPS. From 57 to 67 GHz, the RMS phase and gain errors were 0.83°–2.36° and <0.55 dB, respectively. Table I summarizes the performance of the proposed VSPS and compares it with the published 60 GHz band passive phase shifters. Table I shows that the proposed VSPS can achieve a phase shift of 360° with the lowest phase resolution and an RMS phase error of 57–67 GHz. This is due to the low phase variation and fine gain control of the proposed attenuator used as the vector modulator.

## IV. CONCLUSION

A 7-bit passive VSPS in the 60 GHz band was fabricated through a 65 nm CMOS process. The proposed VSPS uses an analog X-type attenuator with complementary voltage control as the vector modulator. The proposed vector modulator exhibits the advantages of a wide attenuation range, phase reversal capability, and small size, rendering it suitable for high-resolution VSPS design. The measurement results showed that the fabricated circuit had an average IL of 14 dB, and that it covered a phase shift range of 360° with a phase resolution of 2.815°. Further, the RMS phase and gain errors were 0.83°–2.36° and <0.55 dB, respectively. Compared with other reported 60 GHz band passive phase shifters, the proposed VSPS has the lowest phase resolution and RMS phase error owing to wide low phase variation gain control range of the proposed attenuator; hence, it is suitable for implementation in large-scale bidirectional phased array systems.

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