A 160–190-GHz Vector-Modulator Phase Shifter for Low-Power Applications

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***Abstract*— This letter presents a vector-modulator phase shifter for low-power and broadband applications operating from 160 to 190 GHz. The component is implemented in a 130-nm SiGe BiCMOS technology featuring a maximum oscillation frequency of 450 GHz. Phase-control methods, inductive peaking, and circuit architecture minimize both the dissipated power (P_{dc}) for a given insertion loss (IL) and the silicon footprint of the component. A 360° control of the insertion phase is demonstrated for a root-mean-square (rms) IL of 5.5 dB, and a maximum rms error of 1 dB, when the power consumption is 12.4 mW. The core area of the circuit is 0.07 mm^2. To the best knowledge of the authors, the presented solution achieves the smallest core area together with one of the lowest power consumptions for comparable IL among designs operating above 100 GHz in any fabrication process.**

***Index Terms*— Inductive peaking, low power, millimeter-wave integrated circuits, phase shifters, SiGe BiCMOS integrated circuits, vector modulators (VMs), WR-5 band.**

I. Introduction

VECTOR-MODULATOR (VM) phase shifters offer compact footprints, low insertion losses (ILs), and continuous 360° phase control at the cost of moderate power consumption (P_{dc}) [1]–[6]. A common approach for the design of these components is to use a Gilbert cell applying the control voltages to the transistors Q_1 [4], as shown in Fig. 1. The amplitudes of the four signals that combine at nodes $Y^{\pm}$ are controlled by steering the bias currents of Q_0 among the Q_1 transistors. Thanks to passive structures, such as baluns and couplers, these signals reach the phase shifter output with a 90° relative phase shift, and their combination, weighted via the control voltages $V_{c1,2}$, enables the generation of any insertion phase between 0° and 360°. The main drawback of this approach is that in the majority of the selected insertion phases, the signal current of Q_0 is partitioned between the Q_1 transistors, and their output common-mode signals are rejected by the balun, used to generate 180° phase shift, and, thereby, not contributing to the output power. Several designs tried to mitigate this limitation by varying the total bias current of the variable gain amplifiers (VGAs) instead of steering it, and modified Gilbert cells have been proposed at the cost of increased circuit complexity, silicon footprint, and early phase distortions when the gain is in compression [8], [9].

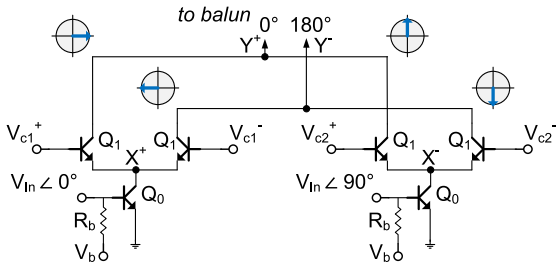

Fig. 1. Core section of a Gilbert-cell VM phase shifter [4]. $V_{c1\text{-}2}{}^{\pm}$ tune the steering of the Q_0 bias collector currents between the Q_1 transistors to dynamically control the amplitude of the signals at node $Y^{\pm}$.

In this letter, the total VGA's bias current tuning is achieved via the control voltages to the transistors Q_0. With respect to the previous demonstration of this technique [8], [9], layout complexity and silicon footprint are reduced by using a single-end architecture, while early phase distortion effects are still possible for sufficiently large input power levels. Moreover, an inductively peaked triple-cascode VGA is employed to further increase the efficiency in terms of IL per power consumption. This letter is structured as follows: the analysis and design of the component are given in Section II, while the experimental results are presented in Section III. Finally, Section IV concludes the work with a comparison of the obtained results against the state of the art.

II. Analysis and Design

Fig. 2 illustrates the schematic of the presented phase shifter. An on-chip Lange coupler splits the single-ended input and inserts a 90° phase delay between the output signals [11]. The quadrature signals drive two pairs of VGAs, whose outputs are gathered by the out-of-phase branches of an on-chip balun. This passive structure adds a relative phase shift of 180° to achieve 360° control of the insertion phase. The balun and the coupler operating between 160 and 200 GHz ensure a broadband frequency response of the circuit. For four particular insertion phases, spaced by 90°, only one VGA is needed, while for all the other insertion-phase states, only two VGAs, driven in quadrature, are necessary. The proposed architecture is, thus, more efficient than the conventional Gilbert cell, where the total bias current and the dissipated power are

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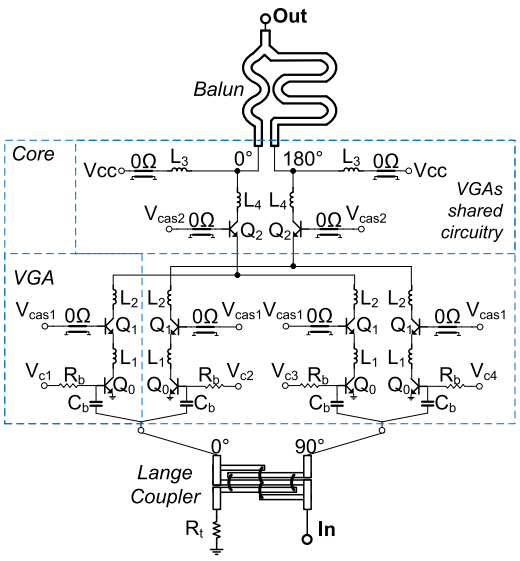

Fig. 2. Circuit schematic of the presented phase shifter.

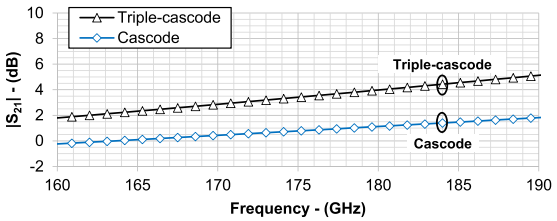

Fig. 3. Simulated $|S_{21}|$ of inductively peaked cascode and triple-cascode VGAs for the same operation point and design parameters used in this letter.

constant and steered between the four Q_1 transistors (Fig. 1), which generate both useful quadrature and rejected-by-the-balun common-mode signals [4]. The resistors R_b of 25 kΩ isolate the input ac signals from the control voltages $V_{c,1\text{-}4}$, which, in turn, are decoupled by capacitors C_b (Fig. 2). The capacitance of C_b was set to 50 fF, a value obtained as the tradeoff between the gain of the VGAs, and the variations of $|S_{11}|$, both increasing with C_b, which is in series with the Q_0 base. The triple inductively peaked cascode VGA [10] improves the small-signal gain for a given power consumption, thanks to a double-inductive peaking between the Q_2 and Q_1 parasitic capacitances and the inductances L_2 and L_1 [10], as illustrated by the simulation in Fig. 3. The inductances $L_{1\text{-}4}$ with an average value of 15 pH in the frequency band of interest have been achieved with electrically short segments of transmission lines as in [6] and [10]. Transmission lines with characteristic impedance close to 0 Ω, referred to as *zero-ohm* lines (0 Ω in Fig. 2) [10], provide a reliable ac ground while feeding the Q_1 base bias signal. The emitter area of the $Q_{0\text{-}2}$ transistors is 4 μm × 0.9 μm × 0.07 μm. Finally, the single-ended architecture in conjunction with the compact Lange coupler reduced the silicon footprint of the design.

III. Measurement Results

Fig. 4 shows the chip photographs of the phase shifter implemented in an HBT SiGe technology with a feature size of 130 nm and a maximum oscillation frequency of 450 GHz. The introduced approach allows for a core area as low as

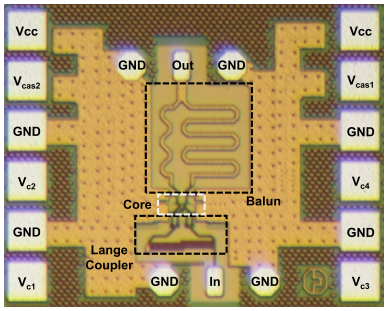

Fig. 4. Chip photograph of the presented phase shifter. The chip dimensions are 750 μm × 570 μm.

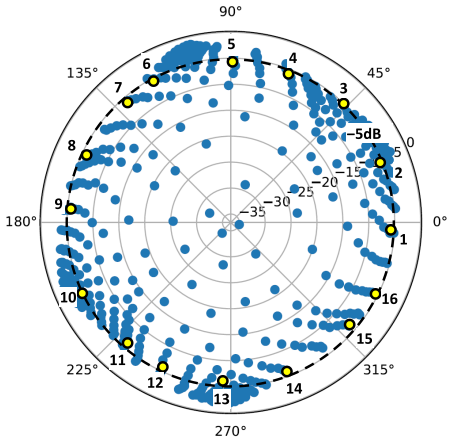

Fig. 5. Measured S_{21} polar plot at 180 GHz for a 1.8-V V_{CC}, and I_{CC} ranging from 0 to 12.5 mA in 16 steps. The best matches to 16 equidistant insertion-phase responses are annotated with yellow dots.

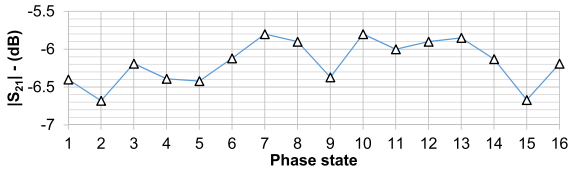

Fig. 6. Measured at 180-GHz $|S_{21}|$ versus the 16 states highlighted in Fig. 5.

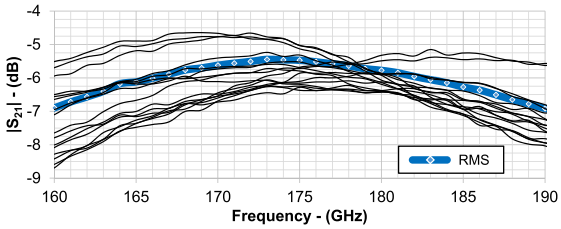

Fig. 7. Measured $|S_{21}|$ of the 16 states highlighted in Fig. 5.

0.07 mm^2. The characterization was performed on-chip with a voltage supply V_{CC} of 1.8 V, and a total collector current I_{CC} swept from 0 to 12.5 mA in 16 steps. Fig. 5 shows the measured polar diagram at 180 GHz. For an average I_{CC} of 6.9 mA, corresponding to a P_{dc} of 12.4 mW, the component provided an average IL of 6.2 dB. Fig. 6 shows the measured $|S_{21}|$ over the 16 states highlighted in Fig. 5, and calibrated to have a resolution of 22.5°: the gain variation over the whole phase tuning range is limited to 0.9 dB. Fig. 7 illustrates the frequency response of the selected phase states. The $|S_{21}|$ of

TABLE I
STATE OF THE ART OF VM PHASE SHIFTERS OPERATING AT MILLIMETER-WAVE FREQUENCIES ABOVE 100 GHz

Ref.	Tech.	Area‡ (mm^2)	BW* (GHz)	IL (dB)	$P_{DC}{}^a$ (mW)	$P_{DC}{}^b$ (mW)	IL/P_{DC}** (1/mW)	iP_{1dB} (dBm)	RMS Amp. Error (dB)	RMS Phase Error (degree)	$\|S_{11}\|^{**}$, $\|S_{22}\|^{**}$ (dB)
[3]	130 nm SiGe	0.12	220–240	8	105	n.a.	0.004	–5†	<1.0	n.a.	n.a.
[4]	250 nm InP	0.14	220–320	14	32	22–42	0.008	–0.7	<1.2	<12	–20, –5
[5]	50 nm GaAs	0.45	240–270	4.5	13.7	n.a.	0.042	n.a.	<1.8	<12	n.a.
[6]	130 nm SiGe	0.07	160–200	9.5	8.6	7.2–16.2	0.035	–8.4†	<0.9	<15	–10, –10
This work	130 nm SiGe	0.07	162–190	6.2	12.4	9.9–15.3	0.041	–13.5†	<1	<8	–10, –10

‡: core area, *: –3 dB bandwidth from minimum IL, **: worst matching, **: IL in natural scale, †: simulated, ^{a}: average, ^{b}: min–max.

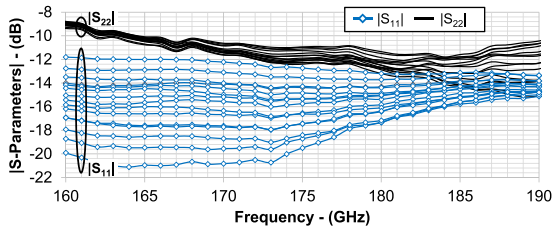

Fig. 8. Measured $|S_{11}|$ and $|S_{22}|$ of the 16 states highlighted in Fig. 5.

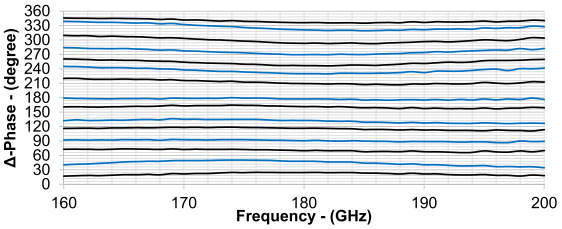

Fig. 9. Measured insertion phase-to-phase difference (Δ-Phase) of the 16 states highlighted in Fig. 5 versus frequency.

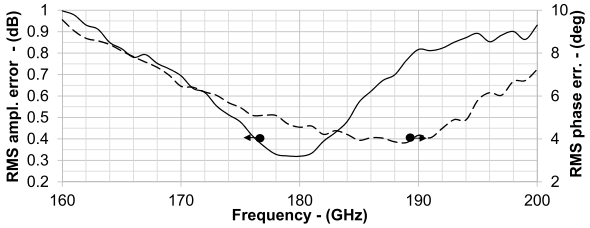

Fig. 10. Measured amplitude and phase rms errors of the 16 states highlighted in Fig. 5 versus frequency.

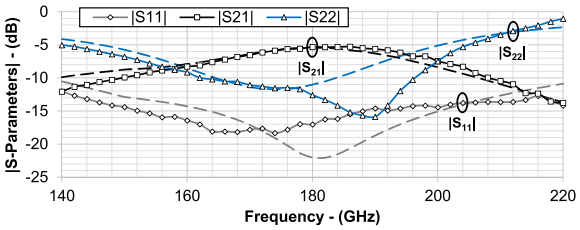

Fig. 11. Measured (solid) and simulated (dashed) S-parameters magnitude of the presented phase shifter for phase-state 7 (Fig. 5).

each state is within 3 dB from the maximum value over the frequency band of 162–190 GHz, while the minimum root-mean-square (rms) IL is 5.5 dB reached at 174 GHz. The difference in the $|S_{21}|$ frequency responses (Fig. 7) arises from different bias conditions of the VGAs, which together with asymmetries of layout, shared circuitry, and passive structures, resonate at slightly distinct frequencies. To minimize this effect, the collector bias current has been adjusted in the range between 5.5 and 8.5 mA, corresponding to a dissipated power between 9.9 and 15.3 mW. Fig. 8 presents the measured $|S_{11}|$ and $|S_{22}|$ of the 16 states: a matching always below -10 dB is observed. Again, the variation of the matching versus the phase states is due to different combinations of biased VGAs, which correspond to distinct impedances attached at the coupler and balun ports. Fig. 9 shows the measured insertion phase-to-phase difference response of the 16 states versus frequency. The rms amplitude and phase error versus frequency, with respect to the average response, is calculated from these measurements as in [4]. The minimum rms amplitude error is 0.3 dB, while the minimum rms phase error is 3° (Fig. 10). Fig. 11 shows the comparison of the small-signal measurements and simulations (only one state for clarity), showing agreement for the IL, while differences for input and output matching are due to the difficulties in modeling the pads. Finally, the simulated input and output power in 1-dB gain compression at 180 GHz for the worst linearity (state 7) are -13.5 and -20 dBm.

IV. CONCLUSION

A VM phase shifter for low-power and broadband applications at millimeter-wave frequencies has been presented. The component is based on a modified Gilbert-cell single-ended architecture, where the VGAs are controlled via the input transistor in place of the stacked one. Continuous 0°–360° phase control in the frequency band from 160 to 190 GHz has been demonstrated, implementing the circuit in a 130-nm SiGe BiCMOS technology. The core area of the component is 0.07 mm^2, mostly set by the integrated on-chip balun and coupler used to generate quadrature and out-of-phase signals. An inductively peaked triple-cascode VGA has been used to improve the circuit efficiency in terms of small-signal gain over power consumption. Experimental results demonstrated an rms IL of 5.5 dB, with a maximum rms error of 1 dB, for an average P_{dc} of 12.4 mW. Table I gathers the obtained results and compares them against the state of the art. The presented solution achieves one of the best performances in terms of IL per power consumption together with the smallest silicon footprint.

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