A DC–*Ka*-Band 7-Bit Passive Attenuator With Capacitive-Compensation-Based Bandwidth Extension Technique in 55-nm CMOS

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***Abstract*— This article presents a 7-bit wideband passive attenuator with low insertion loss (IL) and high attenuation accuracy in 55-nm CMOS technology. The π-type and bridge-T-type attenuation units utilize an effective capacitive compensation technique, whose bandwidth extension mechanism is detailed in a single-unit pole–zero analysis. The matching-induced performance deterioration is investigated to minimize amplitude and phase errors at the chip level. The fabricated attenuator demonstrates a 32.4-dB attenuation range with a 0.255-dB resolution and a 3.5–8.4-dB IL from dc to 32 GHz. The measured root-mean-square (rms) amplitude and phase errors are below 0.32 dB and 5.33°, respectively. The attenuator occupies a 0.054-mm^2 core area and consumes negligible power.**

***Index Terms*— Bandwidth extension, bridge-T type, capacitive compensation, high resolution, low insertion loss (IL), π type, wideband passive attenuator.**

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I. Introduction

THE arising low-Earth-orbit (LEO) satellite communication exploits silicon technologies to achieve low form factor and cost while suffering from temperature-related gain variations. Passive attenuators demonstrate low-temperature dependence and are suitable for digital temperature compensation. Compared with variable-gain amplifiers [1]–[3], passive attenuators provide wide tuning range, high resolution, low phase variation, high linearity, and wideband operation with negligible power consumption. Hence, beamformers often employ attenuators with a wide gain tuning range (i.e., 32 dB) to realize amplitude weighting with extra margin and a high resolution (i.e., $\leq$0.25 dB) to minimize beam jitter [4], [5]. In addition, analog beamforming prefers independent gain and phase control to reduce implementation complexity, imposing low insertion phase variation of the attenuator [6].

There are three passive attenuator topologies in the prior arts: distributed, switch-path, and switch π-/T-/bridge-T-type attenuators [4], [5], [7]–[20]. Distributed step attenuators can provide a wide bandwidth with a low insertion loss (IL) [7]–[10] but cannot achieve a large attenuation range (e.g., $>$16 dB) and a high resolution (e.g., $<$0.5 dB) concurrently. Besides, the use of transmission line increases chip area. The switch-path topology with identical number of series switches between the reference and attenuation paths facilitates wideband operation and low phase error [5], [11], [12]. However, it suffers from high IL due to a large number of series switches. In contrast, the switch π-/T-/bridge-T-type attenuator can achieve fine amplitude control and low IL simultaneously. Some recent developed techniques further broaden the operation bandwidth and minimize the phase variations among different attenuation states [4], [13]–[20]. Inductive compensation was proposed in [13] and utilized in [14] and [15] to mitigate the insertion phase variation. Capacitive compensation can also improve the attenuator performance with a smaller chip area. The tail-capacitor compensation demonstrated in [19] and [20] can minimize the phase error in a relatively narrowband. Sim *et al.* [4], Sun *et al.* [16], Song *et al.* [17], and Gu *et al.* [18] utilize capacitive

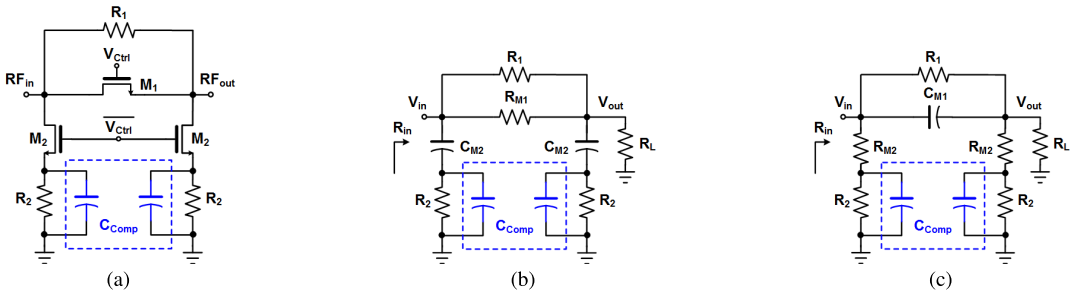


Fig. 1. (a) Schematic of the π-type attenuation unit with capacitive compensation and simplified equivalent circuits for (b) reference state and (c) attenuation state. Without C_{Comp}'s, the schematic and simplified equivalent circuits are converted to that of a conventional π-type unit.

compensation to broaden bandwidth by manipulating the poles and zeros of each attenuation unit with either low resolution or small bandwidth. For instance, Gu *et al.* [18] achieve a dc-50-GHz operation with only a 15.5-dB attenuation range and a 5-bit resolution. Song *et al.* [17] achieve a 31.5-dB attenuation range but can only support frequencies below 20 GHz.

This article expands on [21] and presents a 7-bit wideband attenuator covering from dc to *Ka*-band with the capacitive compensation technique. The detailed pole–zero analysis on π- and bridge-T-type units reveals the mechanism of the bandwidth extension in the single-unit level. However, the performance enhancement comes at the cost of matching deterioration, which limits the accuracy of the whole attenuator. Hence, this article further analyses the placement order of the attenuator units based on the cascaded S-parameter calculation and provides an optimization method to reduce the amplitude and phase errors. The article is organized as follows. Section II investigates π- and bridge-T-type units with and without capacitive compensation. Section III illustrates the matching deterioration problem and the optimization method. Section IV proposes a design flow of wideband attenuators and introduces the fabricated 7-bit wideband attenuator of this work. Section V shows the measurement results. Section VI summarizes this article.

II. Circuit Design

A. Limitations of π-Type Attenuation Unit

The conventional π-type attenuation unit is generally used for high attenuation bits, such as 8 and 16 dB, whose schematic is shown in Fig. 1(a), excluding the additional capacitors (C_{Comp}'s) highlighted inside the dotted box. In the reference state, the series transistor (M_1) turns on and two shunt transistors (M_2's) turn off. In the attenuation state, all the transistors operate oppositely. In order to analyze the impact of each component on the amplitude and phase errors, each transistor can be simplified as a resistor in the ON-state or as a capacitor in the OFF-state. Fig. 1(b) and (c) presents the equivalent circuits of the two states, where R_{M1} / R_{M2} and C_{M1} / C_{M2} represent ON- and OFF-state transistors, respectively.

Generally, the highest-attenuation unit introduces the largest amplitude and phase errors. Hence, the 16-dB attenuation unit is used to clarify the limitation of the π-type unit. Defined as (3), the transfer functions of the two working states are derived as (1) and (2), as shown at the bottom of the next page,

TABLE I
Parameters for the 16-dB Attenuation Unit

R_1	169.3 Ω	R_2	57.3 Ω
R_{M1}	10.2 Ω	C_{M1}	23.46 fF
R_{M2}	9.6 Ω	C_{M2}	25.2 fF
R_L	50 Ω	C_{Comp}	100 fF

where R_B is defined as the bypass resistance ($R_1 \parallel R_{M1}$) in the reference state and R_P is defined as the shunt brunch's total resistance ($R_{M2} + R_2$). The zeros and poles of both working states can be derived from the transfer functions and are detailed as (4)–(8)

$$T(s) = (1 + S_{11})\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{2R_{\text{in}}}{R_{in} + R_L} \cdot \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} \tag{3}$$

$$f_{\pi,w/o\ \text{Cc,Ref},z+,-} = \frac{1}{2\pi C_{M2} R_2} \tag{4}$$

$$f_{\pi,w/o\ \text{Cc,Ref},p1} = \frac{1}{2\pi C_{M2}(R_2 + R_L)} \tag{5}$$

$$f_{\pi,w/o\ \text{Cc,Ref},p2} = \frac{2R_L + R_B}{2\pi C_{M2}[2R_2 R_L + R_B(R_2 + R_L)]} \tag{6}$$

$$f_{\pi,w/o\ \text{Cc,Att},z} = \frac{1}{2\pi C_{M1} R_1} \tag{7}$$

$$f_{\pi,w/o\ \text{Cc,Att},p} = \frac{R_1(R_P + R_L) + 2R_L R_P}{4\pi C_{M1} R_1 R_L R_P}. \tag{8}$$

Table I provides the major parameters of the 16-dB attenuation unit in the used 55-nm CMOS. The values of R_1 and R_2 are calculated by (9) and (10) [22], where A is the attenuation level defined by the ratio of the input and output voltage, and R_{M2} is chosen to be 1/6 of R_2 to reduce the voltage swing across M_2 and improve the linearity. The dimension of M_2 is determined by R_{M2}, and the dimension of M_1 is chosen by trading off IL and bandwidth [17]

$$R_1 = R_L \cdot \frac{A^2 - 1}{2A} \tag{9}$$

$$R_2 = R_L \cdot \frac{A + 1}{A - 1} - R_{M2}. \tag{10}$$

Fig. 2 shows the analytical amplitude and phase responses of the 16-dB π-type attenuation unit without the C_{Comp}'s calculated by (1) and (2) with the values in Table I. In the reference

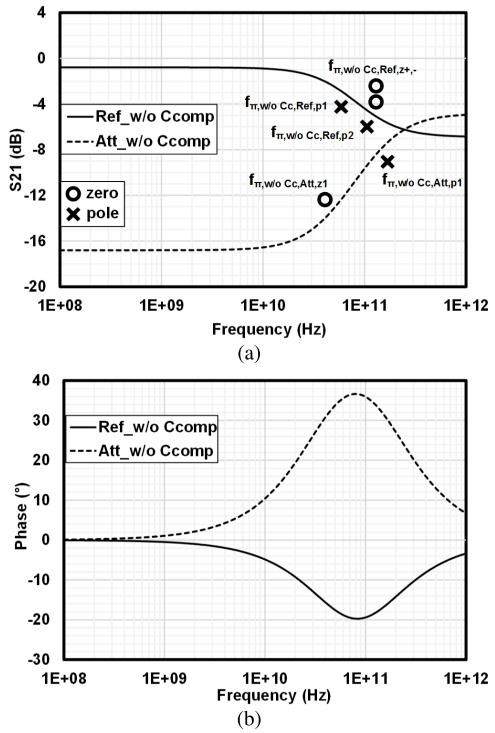


Fig. 2. Analytical (a) amplitude response and (b) phase response for the 16-dB π-type attenuation unit without C_{Comp}'s. The poles and zeros for both states are marked in (a).

state, two poles ($f_{\pi,w/o\ \text{Cc,Ref},p1/2}$) appear at 59/102 GHz, and two co-located zeros ($f_{\pi,w/o\ \text{Cc,Ref},z+,-}$) appear at 110 GHz. The amplitude response in Fig. 2(a) keeps nearly constant up to 15 GHz since the poles and zeros locate at relatively high frequencies. However, in the attenuation state, a zero ($f_{\pi,w/o\ \text{Cc,Att},z}$) shows up at 40 GHz and changes the slope of amplitude response around 10 GHz. The pole ($f_{\pi,w/o\ \text{Cc,Att},p}$) at 159 GHz has negligible influence on the frequencies under the millimeter wave. The zero and the pole are far apart such that the zero limits the working bandwidth of the π-type unit. The frequency of the zero ($f_{\pi,w/o\ \text{Cc,Att},z}$) is inversely proportional to the value of the OFF-state capacitance C_{M1}, as indicated by (7). In order to minimize the IL of the π-type unit, the ON-state resistance R_{M1} should be as small as possible. Consequently, the OFF-state capacitance C_{M1} becomes larger leading to a smaller zero. The phase responses in Fig. 2(b) show similar trends with the amplitude response, and the phase variation increases rapidly as the frequency increases.

B. Π*-Type Unit With Capacitive Compensation*

Fig. 1(a) shows the proposed π-type attenuation unit with capacitive compensation. To tackle the challenge of high amplitude and phase variation in *Ka*-band, two compensation capacitors (C_{Comp}'s) are added symmetrically in the shunt branches to extend the working bandwidth. The transfer functions for the equivalent circuits of the compensated π-type unit [as shown in Fig. 1(b) and (c)] can be derived as (11) and (II-A), as shown at the bottom of this page. Fig. 3 shows the amplitude and phase responses with C_{Comp}'s calculated by (11) and (II-A) with the values in Table I. The poles and zeros of two working states are also marked in Fig. 3(a) with cross and circle, respectively.

In the reference state, the frequencies of zeros and poles are calculated from (11) with the parameters in Table I. Two co-located zeros ($f_{\pi,w/\ \text{Cc,Ref},z+,-}$) locate at 22 GHz, and the first two poles ($f_{\pi,w/\ \text{Cc,Ref},p1/2}$) locate at 21 and 22 GHz, respectively. They cancel out each other, making the third pole ($f_{\pi,w/\ \text{Cc,Ref},p3}$) at 165 GHz dominant. The fourth pole at 1.8 THz falls far apart from the interested frequency band. Through this way, the capacitive compensation extends the bandwidth with flat amplitude response in the reference state.

In the attenuation state, the zeros and poles can be calculated as (13)–(15) with two other poles ($f_{\pi,w/\ \text{Cc,Att},p1/3}$) derived from (16)

$$f_{\pi,w/\ \text{Cc,Att},z1} = \frac{1}{2\pi C_{M1} R_1} \tag{13}$$

$$f_{\pi,w/\ \text{Cc,Att},z+,-} = \frac{R_P}{2\pi C_{\text{Comp}} R_2 R_{M2}} \tag{14}$$

$$f_{\pi,w/\ \text{Cc,Att},p2} = \frac{R_P + R_L}{2\pi C_{\text{Comp}} R_2 (R_{M2} + R_L)} \tag{15}$$

$$R_1 \left\| \frac{1}{sC_{M1}} + 2\left(R_{M2} + R_2 \| \frac{1}{sC_{\text{Comp}}} \right) \right\| R_L = 0. \tag{16}$$

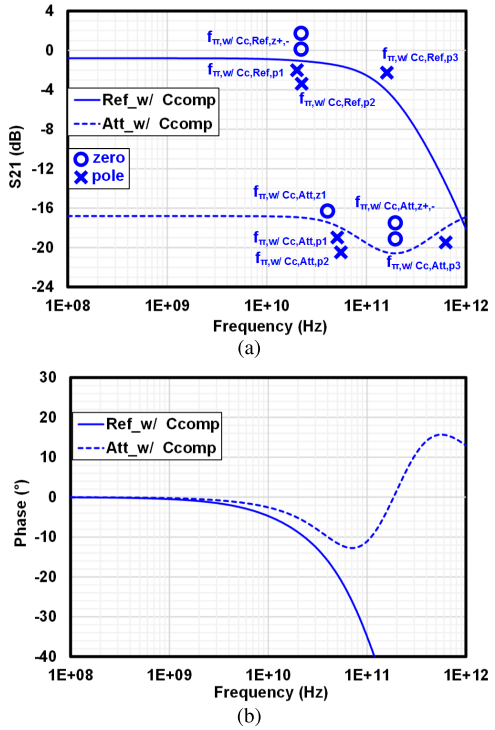
The first zero ($f_{\pi,w/\ \text{Cc,Att},z1}$) also appears at 40 GHz since it shares the same expression with (7). The poles ($f_{\pi,w/\ \text{Cc,Att},p1,2}$) located at 51 and 55 GHz cancel the first zero and change the slope of phase and amplitude responses

$$T(s)_{\pi,w/o\ \text{Cc,}Ref} = \frac{2R_L(1 + C_{M2}R_2 s)^2}{[1 + C_{M2}(R_2 + R_L)s]\{2R_L + R_B + C_{M2}[2R_2R_L + R_B(R_2 + R_L)]s\}} \tag{1}$$

$$T(s)_{\pi,w/o\ \text{Cc,}Att} = \frac{2R_L R_P^2(1 + C_{M1}R_1 s)}{(R_P + R_L)[R_1(R_P + R_L) + 2R_L R_P + 2C_{M1}R_1 R_L R_P s]} \tag{2}$$

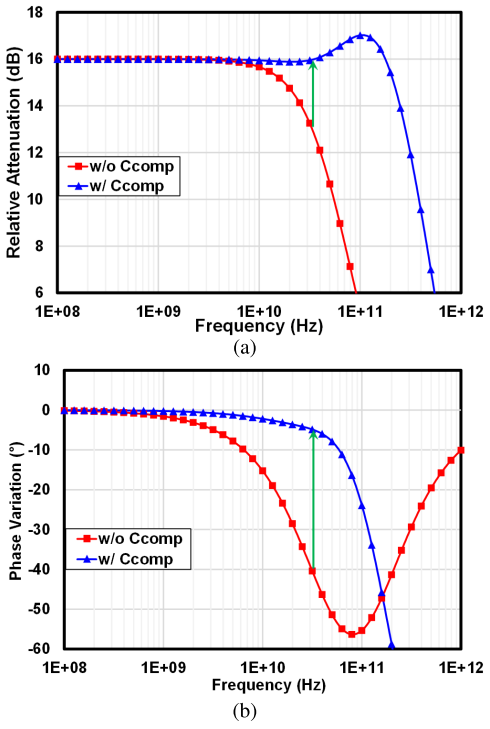
$$T(s)_{\pi,w/\ \text{Cc,Ref}} = \frac{2R_L\left[1+\left(C_{M2}+C_{\text{Comp}}\right)R_2 s\right]^2}{\left\{1+\left[\left(C_{M2}+C_{\text{Comp}}\right)R_2+C_{M2}R_L\right]s+C_{M2}C_{\text{Comp}}R_2R_L s^2\right\}\left\{2R_L+R_B+\left[\left(C_{M2}+C_{\text{Comp}}\right)R_2(2R_L+R_B)+C_{M2}R_L R_B\right]s+C_{M2}C_{Comp}R_BR_2R_L s^2\right\}} \tag{11}$$

$$T(s)_{\pi,w/\ \text{Cc, Att}} = \frac{2R_L\left(R_P + C_{\text{Comp}}R_2R_{M2}s\right)^2(1 + C_{M1}R_1 s)}{\left[R_P + R_L + C_{\text{Comp}}R_2(R_{M2} + R_L)s\right]\left\{R_1(R_P + R_L) + 2R_L R_P + \left[C_{\text{Comp}}R_2(R_1R_{M2} + R_1R_L + 2R_LR_{M2}) + 2C_{M1}R_1R_LR_P\right]s + 2C_{M1}C_{Comp}R_1R_2R_{M2}R_L s^2\right\}} \tag{12}$$



(a) (b)

Fig. 3. Analytical (a) amplitude response and (b) phase response for the 16-dB π-type attenuation unit with compensation capacitor. The poles and zeros for both the reference state and attenuation state are marked in (a).

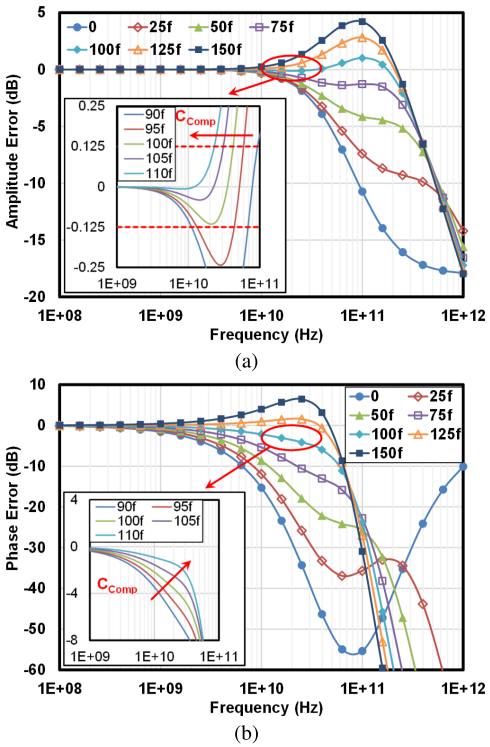


(a) (b)

Fig. 4. Comparisons of (a) relative attenuation and (b) phase variation show the effect of the additional compensation capacitor.

into negative, while the next two zeros ($f_{\pi,w/\ Cc,\mathrm{Att},z+,-}$) at 193 GHz slow down this trend. The third pole ($f_{\pi,w/\ Cc,\mathrm{Att},p3}$) appears at 604 GHz out of the interested frequencies. By adding the C_{Comp}'s, the original pole is replaced by two new poles ($f_{\pi,w/\ Cc,\mathrm{Att},p1/3}$). At the same time, two additional zeros ($f_{\pi,w/\ Cc,\mathrm{Att},z+,-}$) and a pole ($f_{\pi,w/\ Cc,\mathrm{Att},p2}$) independent of C_{M1} are inserted after the unchanged zero ($f_{\pi,w/\ Cc,\mathrm{Att},z1}$). These poles and zeros interact each other and extend the operation bandwidth at the attenuation state compared with the structure without the C_{Comp}'s, as shown in Fig. 3. Specifically, the capacitive compensation modifies the response of the π-type attenuation unit so that the amplitude and phase errors deteriorate at much higher frequencies. Fig. 4 compares the performance of π-type attenuation unit with and without C_{Comp}'s. The analysis shows the compensation technique reduces the maximum amplitude error from 2.8 to 0.12 dB and the maximum phase error from 40.7° to 4.9° from dc to 32 GHz.

The two poles ($f_{\pi,w/\ Cc,\mathrm{Att},p1/3}$) are complicated to formulate; hence, the value of C_{Comp} is hard to derive and determined from the simulated amplitude and phase errors by sweeping C_{Comp}, as shown in Fig. 5. The amplitude error is the difference between the realized relative attenuation and the target attenuation level. The frequencies of the two zeros ($f_{\pi,w/\ Cc,\mathrm{Att},z+,-}$) and a pole ($f_{\pi,w/\ Cc,\mathrm{Att},p2}$) decrease with the increase in C_{Comp} according to (14) and (15), which changes the amplitude and phase errors. In Fig. 5(a), the optimal value of C_{Comp} is 100 fF to achieve the lowest amplitude error from dc to 32 GHz. However, a 125-fF capacitor is needed for the lowest phase error till 32 GHz, as shown in Fig. 5(b). These two different values demand further tradeoffs. The



(a) (b)

Fig. 5. Simulation of (a) amplitude error and (b) phase error sweeping the value of C_{Comp}. The insets at the left bottom show a finer sweep with a step of 5 fF and magnify the curve inside the circle.

insets of Fig. 5(a) and (b) provide the amplitude and phase curves with C_{Comp} between 90 and 110 fF in a 5-fF step. Considering a resolution of 0.25 dB, the amplitude error is

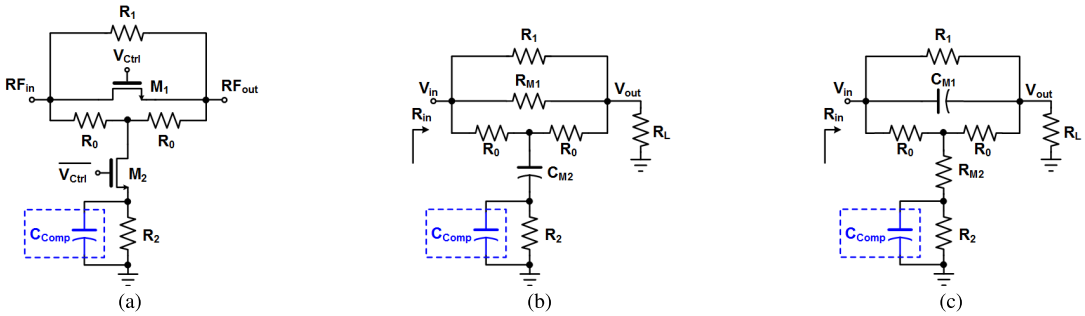


Fig. 6. (a) Schematic of the bridge-T-type unit with the C_{Comp} and simplified equivalent circuits for (b) reference state and (c) attenuation state.

limited between ±0.125 dB to ensure a monotonic control. Given this constraint, the operation bandwidth is about 10 GHz when the value of C_{Comp} is below 100 fF, as shown in Fig. 5(a). When the value of C_{Comp} is larger than 100 fF, the operation bandwidth decreases rapidly. As a comparison, the inset of Fig. 5(b) only shows a 1.2°/step variation at 32 GHz. It is obvious that a change of C_{Comp} has a larger influence on the amplitude error than the phase error. As a result, the value of C_{Comp} is chosen to be 100 fF.

C. Bridge-T Type Unit With Capacitive Compensation

The accumulated amplitude and phase errors can be considerably large when the number of bits reaches seven. Although the compensated π-type attenuation structure proposed in Section II-B reduces the errors of high-attenuation units, low-attenuation units still need to be optimized. Fig. 6(a) shows the proposed bridge-T-type attenuation unit. Similar to the modified T-type structure proposed in [17], a compensation capacitor C_{Comp} is connected in parallel with the resistor R_2. Fig. 6(b) and (c) presents the equivalent circuits at the reference and attenuation states, respectively. By using the definition of (3), the transfer functions corresponding to the two working states with and without the C_{Comp} are derived as (17)–(20), as shown at the bottom of this page.

To demonstrate the improvement brought by the capacitive compensation, the 4-dB attenuation unit is analyzed in detail with major parameters summarized in Table II. The values of R_1 and R_2 are calculated by (21) and (22) [22], where A is the attenuation level. The transistor parameters are determined in the same way as the π-type unit, as illustrated in Section II-A. The analytical amplitude and phase response with and without C_{Comp} calculated by (17)–(20) with the values in Table II are shown in Fig. 7

TABLE II
PARAMETERS FOR THE 4-dB ATTENUATION UNIT

R_1	34.9 Ω	R_2	61.4 Ω
R_{M1}	9.9 Ω	C_{M1}	24.14 fF
R_{M2}	10.2 Ω	C_{M2}	23.46 fF
$R_0 = R_L$	50 Ω	C_{Comp}	55 fF

$$R_1 = R_L \cdot (A-1) \tag{21}$$

$$R_2 = R_L \cdot \frac{1}{A-1} - R_{M2}. \tag{22}$$

Without C_{Comp}, the zeros and poles of the reference and attenuation states can be derived as (23)–(26) from (17) and (18)

$$f_{\text{BT},w/o\ \text{Cc,Ref},z} = \frac{R_B + 2R_0}{2\pi C_{M2}\left(R_0^2 + 2R_0R_2 + R_2R_B\right)} \tag{23}$$

$$f_{\text{BT},w/o\ \text{Cc,Ref},p} = \frac{1}{\pi C_{M2}(R_0 + R_L + 2R_2)} \tag{24}$$

$$f_{\text{BT},w/o\ \text{Cc,Att},z} = \frac{R_P(2R_0 + R_1) + R_0^2}{2\pi C_{M1}R_0R_1(R_0 + 2R_P)} \tag{25}$$

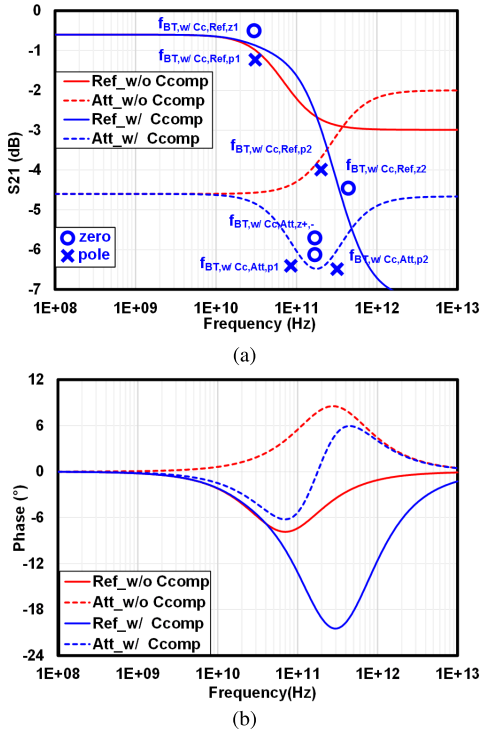
$$f_{\text{BT},w/o\ \text{Cc,Att},p} = \frac{R_0R_1 + 2R_0R_L + R_1R_L}{4\pi C_{M1}R_0R_1R_L}. \tag{26}$$

$$T(s)_{\text{BT},w/o\ \text{Cc,Ref}} = \frac{2R_L\{R_B + 2R_0 + C_{M2}[R_0(R_0 + 2R_2) + R_2R_B]s\}}{[R_B(R_0 + R_L) + 2R_0R_L][2 + C_{M2}(R_0 + R_L + 2R_2)s]} \tag{17}$$

$$T(s)_{\text{BT},w/o\ \text{Cc,Att}} = \frac{2R_L\left[(2R_0 + R_1)R_P + R_0^2 + C_{M1}R_0R_1(R_0 + 2R_P)s\right]}{(R_0 + R_L + 2R_P)(R_0R_1 + 2R_0R_L + R_1R_L + 2C_{M1}R_0R_1R_Ls)} \tag{18}$$

$$T(s)_{\text{BT},w/\text{Cc,Ref}} = \frac{2R_L\left\{R_B + 2R_0 + \left\{C_{M2}[R_0(R_0 + 2R_2) + R_2R_B] + C_{\text{Comp}}(2R_0R_2 + R_2R_B)\right\}s + C_{M2}C_{\text{Comp}}R_0^2R_2s^2\right\}}{[R_B(R_0 + R_L) + 2R_0R_L]\left\{2 + \left[C_{M2}(R_0 + R_L + 2R_2) + 2C_{\text{Comp}}R_2\right]s + C_{\text{Comp}}C_{M2}R_2(R_0 + R_L)s^2\right\}} \tag{19}$$

$$T(s)_{\text{BT},w/\text{Cc,Att}} = \frac{2R_L\left\{(2R_0+R_1)R_P+R_0^2+\left[C_{M1}R_0R_1(R_0+2R_P)+C_{\text{Comp}}R_2\left(R_0^2+R_1R_{M2}+2R_0R_{M2}\right)\right]s+C_{M1}C_{\text{Comp}}R_0R_1R_2(R_0+2R_{M2})s^2\right\}}{\left[R_0 + R_L + 2R_P + C_{\text{Comp}}R_2(R_0 + R_L + 2R_{M2})s\right](R_0R_1 + 2R_0R_L + R_1R_L + 2C_{M1}R_0R_1R_Ls)} \tag{20}$$



(a) (b)

Fig. 7. Analytical (a) amplitude response and (b) phase response for the 4-dB bridge-T-type unit with and without C_{Comp}. The poles and zeros of the unit with C_{Comp} are marked in (a).

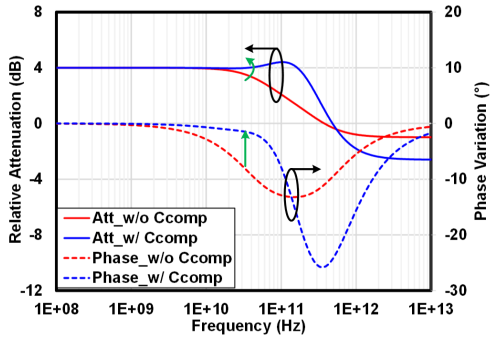


Fig. 8. Comparisons of relative attenuation and phase variation show the improvement due to the capacitive compensation technique.

In the reference state, a pole ($f_{\text{BT},w/o\ \text{Cc,Ref},p}$) and a zero ($f_{\text{BT},w/o\ \text{Cc,Ref},z}$) appear at 61 and 80 GHz, respectively. In the attenuation state, a zero ($f_{\text{BT},w/o\ \text{Cc,Att},z}$) and a pole ($f_{\text{BT},w/o\ \text{Cc,Att},p}$) appear at 238 and 321 GHz, respectively. All the poles and zeros fall out of the *Ka*-band, but the curves at *Ka*-band are already affected by the pole of the reference state and the zero of the attenuation state, which results in large amplitude and phase errors.

By adding the compensation capacitor, the amplitude and phase responses are changed, as shown in Fig. 7. In the reference state, the first pole ($f_{\text{BT},w/\ \text{Cc,Ref},p1}$) appears at 30 GHz, and the first zero ($f_{\text{BT},w/\ \text{Cc,Ref},z1}$) appears at 32 GHz. They cancel out each other and make the next pole ($f_{\text{BT},w/\ \text{Cc,Ref},p2}$) at 210 GHz dominant. The second zero ($f_{\text{BT},w/\ \text{Cc,Ref},z2}$) is located at 432 GHz. In the attenuation state, the poles and

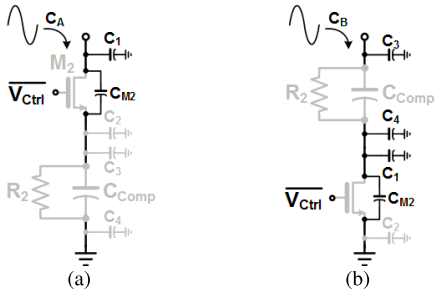


Fig. 9. Analysis for two orders of the shunt brunch: (a) order A and (b) order B.

zeros can be derived from (20), as shown in (27)–(29)

$$f_{\text{BT},w/\ \text{Cc, Att},p1} = \frac{R_0 + R_L + 2R_2 + 2R_{M2}}{2\pi C_{\text{Comp}} R_2 (R_0 + R_L + 2R_{M2})} \tag{27}$$

$$f_{\text{BT},w/\ \text{Cc, Att},p2} = \frac{R_0 R_1 + 2R_0 R_L + R_1 R_L}{4\pi C_{M1} R_0 R_1 R_L} \tag{28}$$

$$f_{\text{BT},w/\ \text{Cc, Att},z+,-} = \frac{1}{2\pi}\left[\frac{(2R_0 + R_1)(R_2 + R_{M2}) + R_0^2}{C_{M1} C_{\text{Comp}} R_0 R_1 R_2 (R_0 + 2R_{M2})}\right]^{\frac{1}{2}} \tag{29}$$

$$C_{\text{Comp}} > \frac{C_{M1} R_0 R_1 (R_0 + 2R_{M2})}{R_2\left[(2R_0 + R_1)(R_2 + R_{M2}) + R_0^2\right]} \times \left(\frac{R_0 + R_L + 2R_2 + 2R_{M2}}{R_0 + R_L + 2R_{M2}}\right)^2. \tag{30}$$

By using the value in Table II, the first pole ($f_{\text{BT},w/\ \text{Cc,Att},p1}$) at 95.2 GHz and two co-located zeros ($f_{\text{BT},w/\ \text{Cc,Att},z+,-}$) at 175 GHz are derived. The second pole ($f_{\text{BT},w/\ \text{Cc,Att},p2}$) has the same equation as (26) and appears at 321 GHz. Equations (27)–(29) indicate that C_{Comp} introduces the first pole into the responses and changes the position of the zero. If the value of C_{Comp} satisfies the relationship of (30), the first pole ($f_{\text{BT},w/\ \text{Cc,Att},p1}$) would appear before the zeros ($f_{\text{BT},w/\ \text{Cc,Att},z+,-}$), as same as the reference state. In general, an appropriate C_{Comp} can make the pole dominate at lower frequencies in both the reference and attenuation states such that the amplitude and phase errors can be decreased. The simulated relative attenuation and phase variation show that the capacitive compensation reduces the amplitude error from 0.45 to 0.05 dB and the phase error from 7.93° to 1.44° from dc to 32 GHz, as shown in Fig. 8.

D. Shunt Branch Design

The shunt branch of both the π- and bridge-T-type units consists of a transistor M_2 and an RC pair ($R_2 \parallel C_{\text{Comp}}$). The placement order of these two parts does not affect the theoretical analysis in Sections II-A, B, and C, while it does change the distribution of parasitic capacitance. Here, order A denotes the case when the transistor is on the top of the RC pair, and order B denotes the case when the RC pair is on the top of the transistor. The widely adopted floating-body and floating-gate techniques minimize the grounded parasitic capacitance of the transistor [23]. Both ends of the transistor and the RC pair have a small parasitic grounded capacitance

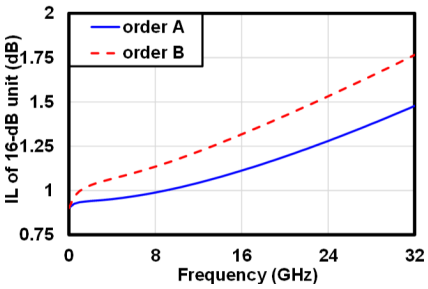


Fig. 10. Simulated IL of the 16-dB attenuation unit for the two orders with the practical layout.

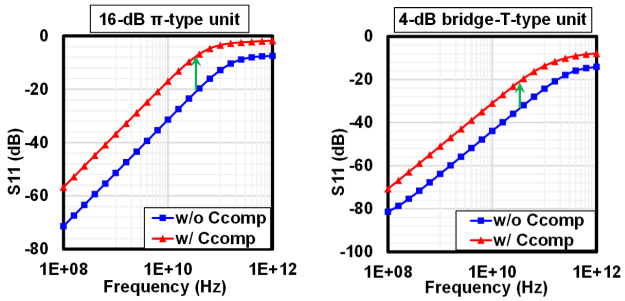


Fig. 11. Simulated S_{11} of (a) 16-dB π-type unit and (b) 4-dB bridge-T-type unit in the attenuation state with and without C_{Comp}.

(C_1–C_4) mainly introduced by the metal wiring, as shown in Fig. 9.

In the reference state of the 16-dB attenuation unit, the OFF-state transistor is equivalent to a small capacitor (25.2 fF), whose impedance is far greater than the RC pair (57.3 Ω ‖ 100 fF) at 32 GHz. Therefore, in order A, the RC pair can be neglected, and the parasitic capacitors C_2, C_3, and C_4 are then shorted to the ground, as shown in Fig. 9(a). The total capacitance C_A connecting to the signal is $C_{M2} + C_1$. In contrast, only the parasitic capacitor C_2 is shorted to the ground in order B, as shown in Fig. 9(b). The total capacitance C_B connecting to the signal is $C_{M2} + C_1 + C_3 + C_4$ and is larger than C_A, which results in a higher IL. In the postlayout simulation, C_A and C_B in the 16-dB attenuation unit are 17 and 22.4 fF, respectively. Fig. 10 shows the simulated IL of a 16-dB attenuation unit for both orders. The IL of order A is 0.29 dB lower than that of order B at 32 GHz.

III. Matching Considerations and Attenuator Optimization

A. Matching Deterioration

Sections II-B and II-C show that the capacitive compensation improves the amplitude and phase performances in the single-unit level. Unfortunately, it degrades the matching.

In the reference state of both π- and bridge-T-type units, S_{11} is mainly determined by R_{M1} and is better than 20 dB with and without the compensation capacitors at low frequencies. However, with the increase in frequency, C_{M2} cannot provide adequate isolation for the shunt brunch thus exacerbating S_{11}.

Fig. 11(a) shows the simulated S_{11} of a 16-dB π-type unit in the attenuation state. When without C_{Comp}, S_{11} can be derived as (31), as shown at the bottom of the next page, where the constant term of the numerator equals to zero, as shown in (33), by substituting R_1 and R_P using (9) and (10). S_{11} deteriorates with a slope of 20 dB/decade at low frequencies and becomes −21.45 dB at 32 GHz. When with C_{Comp}, S_{11} has a similar trend. S_{11} at low frequencies can be approximately derived as (33), as shown at the bottom of the next page. By comparing (31) and (33), S_{11} further deteriorates with C_{Comp}. The deterioration degree Δ of the matching can be defined as (34). Calculated with the value in Table I, S_{11} deteriorates 14.59 dB in the 16-dB unit. Δ at 32 GHz shown in Fig. 11(a) is 13.39 dB, and the return loss of 8.06 dB is inferior

$$(R_1 + 2R_P)R_L^2 - R_1R_P^2 = 0 \tag{32}$$

$$\Delta = \frac{S_{11}(s)_{\pi,w/\ \text{Cc,Att}}}{S_{11}(s)_{\pi,w/o\ \text{Cc,Att}}} = 1 + \frac{C_{\text{Comp}}}{C_{M1}} \cdot \frac{{R_2}^2}{{R_L}^2} \cdot \frac{A^2+1}{(A+1)^2}. \tag{34}$$

Fig. 11(b) shows the simulated S_{11} of a 4-dB bridge-T-type unit in the attenuation state. The approximate S_{11}'s of the bridge-T-type unit with and without C_{Comp} are derived as (35) and (36). The curves of both cases have a slope of 20 dB/decade at low frequencies, and the values of S_{11} are −21.23 and −33.8 dB when with and without C_{Comp} at 32 GHz. By comparing (35) and (36), C_{Comp} is still the source of the deterioration. The deterioration degree is defined as

$$\Delta = \frac{S_{11}(s)_{\text{BT},w/\ \text{Cc,Att}}}{S_{11}(s)_{\text{BT},w/o\ \text{Cc,Att}}} = 1 + \frac{C_{\text{Comp}}}{C_{M1}} \cdot \frac{{R_2}^2}{{R_L}^2}. \tag{37}$$

By using the value in Table II, S_{11} has a deterioration of 12.94 dB at low frequencies.

To investigate the relationship between input matching and attenuation level, S_{11} of both π- and bridge-T-type units without the C_{Comp}'s in the attenuation state is derived as (38) from (31) and (35). It is easy to prove that S_{11} gets worse with the increase in the attenuation level A. In conclusion, the high attenuation level in the 16-dB unit leads to a poorer matching performance, and the additional C_{Comp}'s further deteriorate it

$$S_{11}(s)_{w/o\ \text{Cc,Att}} = -\frac{(A-1)^2 C_{M1} R_L s}{2A[A + (A-1)C_{M1}R_L s]}. \tag{38}$$

B. Multiunit Cascading Analysis

To quantitatively evaluate the impact of matching on attenuation performance, the S-parameters for cascaded two-port networks shown in Fig. 12 need to be derived. Gupta *et al.* [24] and Sadiku and Akujuobi [25] utilize the transfer scattering parameters or T-parameters to analyze the cascaded two-port networks, which is defined as follows:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix}. \tag{39}$$

S-parameters and T-parameters can be directly converted to each other. For the same character impedance, the overall T-parameters of cascaded two-port networks can be obtained

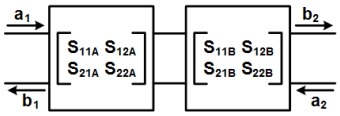


Fig. 12. Block diagram of the cascaded two-port networks.

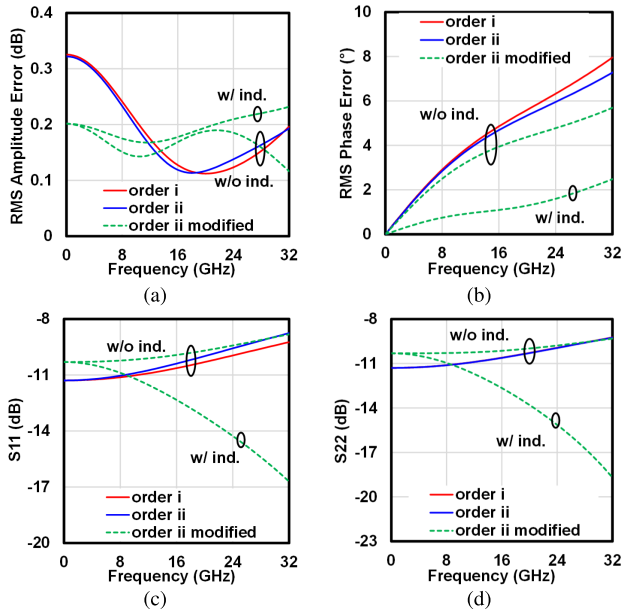


Fig. 13. Analytical (a) rms amplitude errors, (b) rms phase errors, (c) S_{11} of the reference state, and (d) S_{22} of the renference state for order i (0.5-2-16-8-4-1-dB order) and order ii (0.5-16-2-4-8-1-dB order). The dotted lines show the performance of order ii after parameter adjustment. Additional interunit series inductors can reduce the rms phase error by improving the matching condition at high frequencies.

by multiplying individual T-matrices [24]. The S-parameters of cascaded two-port networks can be derived as follows:

$$\begin{cases} S_{11} = S_{11A} + \dfrac{S_{11B}S_{12A}S_{21A}}{1 - S_{22A}S_{11B}} \\ S_{12} = \dfrac{S_{12A}S_{12B}}{1 - S_{22A}S_{11B}} \\ S_{21} = \dfrac{S_{21A}S_{21B}}{1 - S_{22A}S_{11B}} \\ S_{22} = S_{22B} + \dfrac{S_{22A}S_{12B}S_{21B}}{1 - S_{22A}S_{11B}}. \end{cases} \tag{40}$$

The equations indicate that S_{12} and S_{21} are related with S_{11} and S_{22}, which means that the attenuation accuracy can be influenced by the single-unit matching performance. Furthermore, the cascaded S_{11} and S_{22} are also influenced by the attenuation level, especially when the attenuation units are in their reference states.

TABLE III
S-PARAMETERS FOR DIFFERENT ATTENUATION UNITS

Unit	$S_{11(22)}$ ref.	$S_{21(12)}$ ref.	$S_{11(22)}$ att.	$S_{21(12)}$ att.
16-dB	0.02153 -0.20136i	0.84644 -0.198i	-0.20346 -0.33922i	0.13707 -0.01992i
8-dB	0.02821 -0.128i	0.89569 -0.12681i	-0.06871 -0.21258i	0.35461 -0.05133i

TABLE IV
S-PARAMETERS FOR 16-8-dB CASCADED NETWORKS

Att. Level (dB)	S_{11} (dB)	S_{22} (dB)	$S_{21(12)}$ (dB)	Relative Att. (dB)
0	-10.605	-10.844	-2.303	0
8	-9.612	-12.109	-10.508	8.205
16	-8.010	-8.111	-18.459	16.156
24	-7.968	-11.460	-26.594	24.291

Take the cascading of 16- and 8-dB units as an example, the S-parameters in the complex form of the two units at 32 GHz are specified in Table III. The S-parameters of the cascaded network can be calculated by (40) and are summarized in Table IV. The maximum relative attenuation is 24.29 dB at 32 GHz, which is 0.29 dB larger than the ideal value. The matching performance of all states is further deteriorated compared with the single-unit condition. It is identified that the interunit matching introduces considerable attenuation error and limits the achievable resolution.

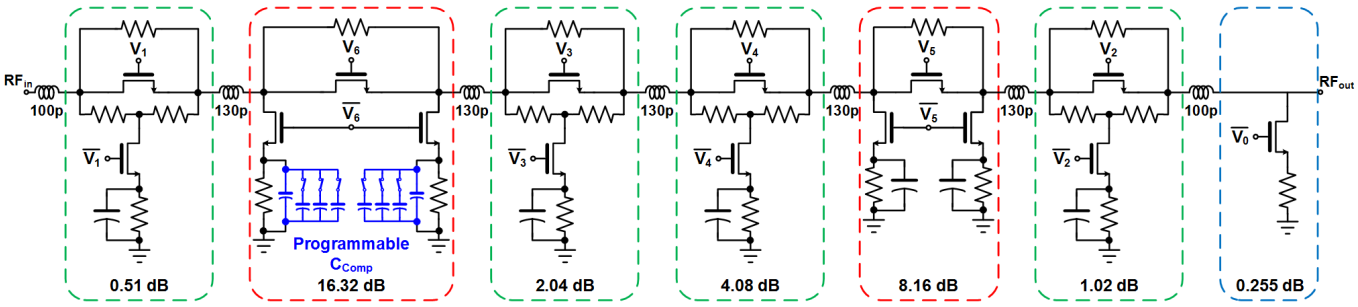
To fully characterize the matching-induced performance deterioration, different arrangements of the entire attenuator design are investigated. First, the 16- and 8-dB units adopt π-type attenuation structure, and 4-, 2-, 1-, and 0.5-dB units adopt bridge-T-type structure since π-type structure performs better at large attenuations [18]. Second, the S-parameters versus frequency of every single unit are calculated. Then, the root-mean-square (rms) amplitude/phase errors and S_{11}/S_{22} of the reference state are evaluated for different arrangements. Fig. 13 shows the results of two typical arrangements: 1) 0.5-2-16-8-4-1-dB order as order i and 2) 0.5-16-2-4-8-1-dB order as order ii. The two orders demonstrate similar

$$S_{11}(s)_{\pi,w/oCc,Att} = -\frac{(R_1 + 2\ R_P)R_L^2 - R_1R_P^2 + 2\ C_{M1}R_1R_PR_L^2 s}{(R_P + R_L)[R_1(R_P + R_L) + 2\ R_PR_L + 2\ C_{M1}R_1R_PR_Ls]} \tag{31}$$

$$S_{11}(s)_{\pi,w/Cc,Att} \approx -\frac{2\ C_{M1}R_1R_PR_L^2 s + 2\ C_{Comp}R_2^2(R_1R_P - R_L^2)s}{(R_P + R_L)[R_1(R_P + R_L) + 2\ R_PR_L]} \tag{33}$$

$$S_{11}(s)_{BT,w/oCc,Att} = -\frac{2C_{M1}R_0R_1R_L^2 s}{(R_0 + 2R_P + R_L)(R_0R_1 + 2R_0R_L + R_1R_L + 2C_{M1}R_0R_1R_Ls)} \tag{35}$$

$$S_{11}(s)_{BT,w/Cc,Att} \approx -\frac{2C_{M1}R_0R_1R_L^2 s + 2C_{Comp}R_0R_1R_2^2 s}{(R_0 + 2R_P + R_L)(R_0R_1 + 2R_0R_L + R_1R_L)} \tag{36}$$



Attenuation (dB)	M_1 (W/L)	M_2 (W/L)	R_1 (Ω)	R_2 (Ω)	C_{Comp} (fF)
0.255	/	5.7 μm / 60 nm	/	1000	/
0.51	46.5 μm / 60 nm	16.5 μm / 60 nm	9.4	984.5	0
1.02	65.1 μm / 60 nm	16.5 μm / 60 nm	12.2	400.3	5
2.04	73.5 μm / 60 nm	16.5 μm / 60 nm	24	218.9	12
4.08	46.5 μm / 60 nm	16.5 μm / 60 nm	49	70.5	28
8.16	65.1 μm / 60 nm	16.5 μm / 60 nm	66.1	97.1	28
16.32	46.5 μm / 60 nm	32.3 μm / 60 nm	249.2	84.9	64–82

Fig. 14. Schematic of the proposed 7-bit wideband attenuator. The C_{Comp}'s in the 16.32-dB unit are two 3-bit programmable capacitor arrays. The parameters of each unit are summarized in the table.

performance in all aspects. In this article, order ii is adopted for its slightly better phase performance than order i.

As shown in Fig. 13(a), the rms amplitude errors of both orders rise at low frequencies, which is also induced by the different matching performances at the reference and attenuation states for each unit. To address this problem, viable schemes include: 1) to reduce the dimension of M_1 and 2) to increase the values of R_1 and R_2. Both schemes require smaller C_{Comp} (i.e., the optimum value of the C_{Comp} in the 16-dB attenuation unit is reduced from 100 to 75 fF) and improve the amplitude and phase accuracy at the cost of a larger IL and a further degraded matching performance. Taking the latter scheme as an example, after parameter adjustment, the rms amplitude error of order ii can be significantly improved [as shown in Fig. 13(a)], while, with S_{11} and S_{22}, it worsened at low frequencies [as shown in Fig. 13(c) and (d)].

As shown in Fig. 13(b), the rms phase errors of both orders rise at high frequencies. Although the parameter adjustment reduces the rms phase error by 1.6° at 32 GHz, the remaining error is still large. Additional interunit series inductors can further reduce the phase variation [as shown in Fig. 13(b)] by improving the matching at high frequencies [as shown in Fig. 13(c) and (d)]. It is worth noting that the interunit series inductors cannot improve the attenuation accuracy, as shown in Fig. 13(a).

IV. Wideband Attenuator Implementation

Based on the above analysis, a design flow for wideband attenuators can be summarized as follows. First, given the design specification, the number of units and the corresponding structures are determined. Second, the proposed capacitive compensation technique is applied in every single unit to minimize the amplitude and phase errors. The parameters of the resistors and transistors are calculated and optimized according to IL, attenuation level, and operation bandwidth. The pole–zero analysis can provide an intuitive understanding of the bandwidth extension effect. Third, a proper cascading order needs to be determined to achieve smaller rms amplitude and phase errors. In addition, parameter values, such as the dimension of M_1, the values of R_1 and R_2, and the size of C_{Comp}, are optimized to reduce the matching-induced amplitude and phase errors.

To demonstrate the effectiveness of the proposed design flow, a wideband attenuator with seven binary-weighted units was implemented, as shown in Fig. 14. Due to the inaccurate substrate model of the switches and the actual parasitic effect, the realized attenuation range is 32.4 dB, slightly larger than the designed value (31.75 dB), and the corresponding step size is 0.255 dB. The 16.32- and 8.16-dB units employ the π-type topology with capacitive compensation to achieve wideband and accurate amplitude control at high attenuation levels. The 4.08-/2.04-/1.02-/0.51-dB units utilize the bridge-T-type topology with capacitive compensation to minimize the accumulated errors. The reduced-T-type topology proposed in [17] is exploited in the 0.255-dB unit to reduce the IL. The placement order and the parameters of each unit are optimized according to Section III-B. Serial inductors isolate adjacent units and improve the input and output matching of the attenuator. A serial peripheral interface (SPI) configures the attenuator.

To adapt to the process variation, the two C_{Comp}'s in the 16.32-dB unit are replaced by two identical 3-bit programmable capacitor arrays ranging from 64 to 82 fF. Fig. 15 shows the simulated rms amplitude errors at fast and slow process corners. The dashed lines present the results simulated using the standard control bits of the capacitor arrays, and the solid lines show that the attenuation accuracy can be effectively optimized by increasing the compensation capacitance at the fast corner and decreasing it at the slow corner.

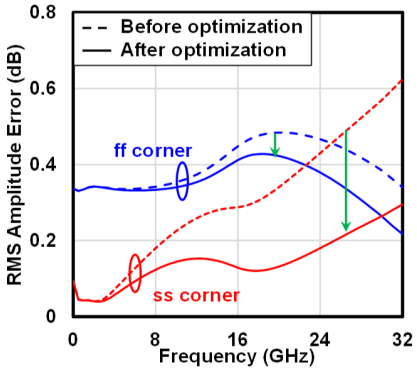


Fig. 15. Simulated attenuation accuracy at fast and slow process corners before and after tuning the programmable capacitor arrays.

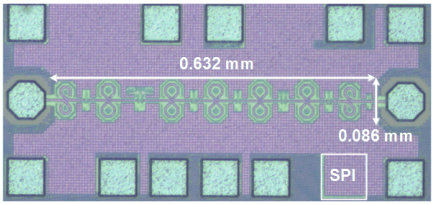


Fig. 16. Chip micrograph of the 7-bit wideband attenuator. The core area is 0.054 mm^2 (0.632 mm $\times$ 0.086 mm) excluding pads, SPI, and nonactive area.

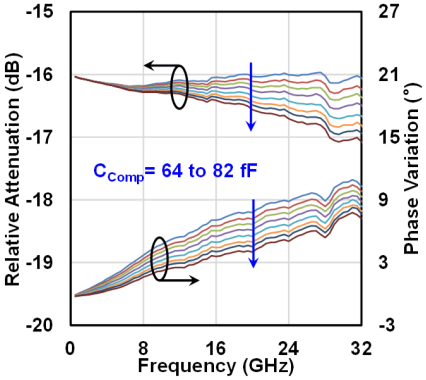


Fig. 17. Measurement results of the compensation capacitors' effect on relative attenuation and phase variation of 16.32-dB attenuation.

V. Measurement Results

The proposed wideband 7-bit digital-step attenuator is fabricated in a 55-nm CMOS process, and the micrograph is shown in Fig. 16. It occupies 0.054 mm^2 (0.632 mm $\times$ 0.086 mm), excluding pads, SPI, and nonactive area. The on-chip probing test characterizes the performance of the attenuator. The S-parameters are measured with an Agilent PNA 5224A network analyzer.

Fig. 17 shows the measurement results of the compensation capacitors' effect on relative attenuation and phase variation of 16.32-dB attenuation. As the value of C_{Comp} increases, smaller phase variation can be achieved at the cost of larger attenuation error, which agrees with the analysis in Section II-B. The value of C_{Comp} is tuned to guarantee a better rms amplitude error with an acceptable rms phase error.

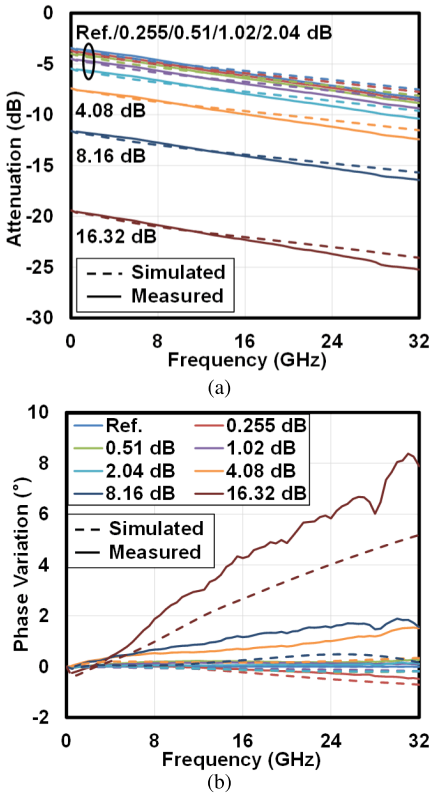


Fig. 18. Simulated and measured (a) attenuation results and (b) phase variations of major states.

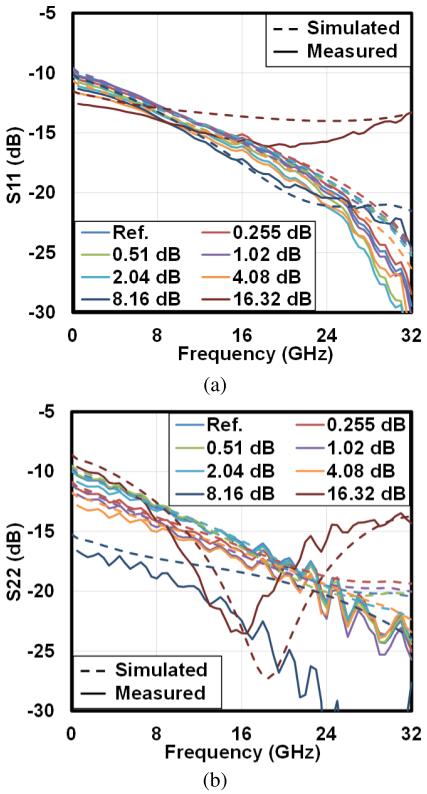


Fig. 19. Simulated and measured (a) S_{11} and (b) S_{22} of major states.

Fig. 18(a) shows the simulated and measured attenuation results of eight major states. The measured IL at the reference state is from 3.5 to 8.4 dB at 0–32 GHz, slightly larger

TABLE V
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART ATTENUATORS

Reference	TMTT'10 [13]	JSSC'18 [17]	RFIC'17 [5]	TMTT'18 [12]	TCAS-II'20 [15]	TCAS-I'20 [20]	This work
Process	0.18 μm CMOS	0.13 μm SiGe BiCMOS	65 nm CMOS	0.25 μm GaAs pHEMT	0.25 μm SiGe BiCMOS	65 nm CMOS	**55 nm CMOS**
Bandwidth (GHz)	0–14	0–20	26–32	6–18	6.6–12.8	37–40	**0–32**
Att. range (dB)	31.5	31.5	31	31.75	28.575	31	**32.4**
Number of bits	6	6	5	7	7	5	**7**
LSB (dB)	0.5	0.5	1	0.25	0.225	1	**0.255**
IL (dB)	3.7–10	1.7–7.2	N/A	<9	8.9–12.4	7[a]	**3.5–8.4**
Return loss (dB)	>9	>12	N/A	>12	>13	>12	**>9.6**
RMS amp. error (dB)	0.5	0.37	0.5	0.6	0.225	0.27	**0.32**
RMS phase error (°)	4.2	4	5	7[b]	2.3–3.3	3.7	**5.33**
IP1dB (dBm)	15 @10 GHz	10 @1 GHz	N/A	N/A	13.5 @10 GHz	12[a]	5.1@5 GHz **9.1@30 GHz**
Core area (mm^2)	0.5	0.14	N/A	5.4	0.71	0.21	**0.054**

[a] Simulation result.
[b] Maximum phase error.

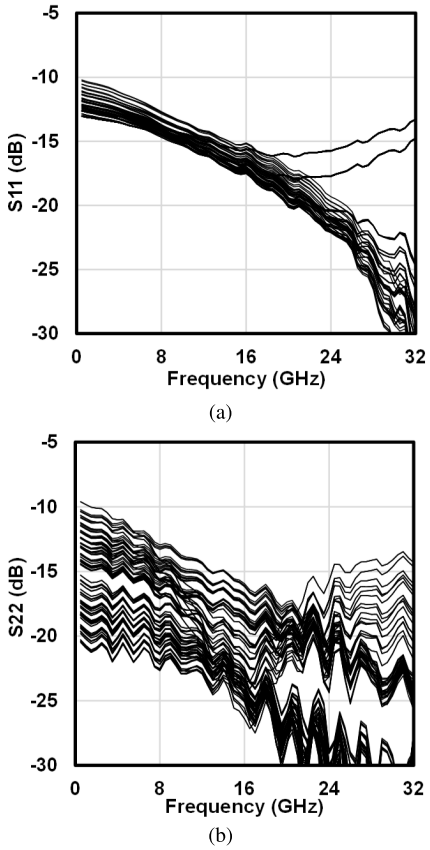


Fig. 20. Measured (a) S_{11} and (b) S_{22} over frequencies for all the 128 states.

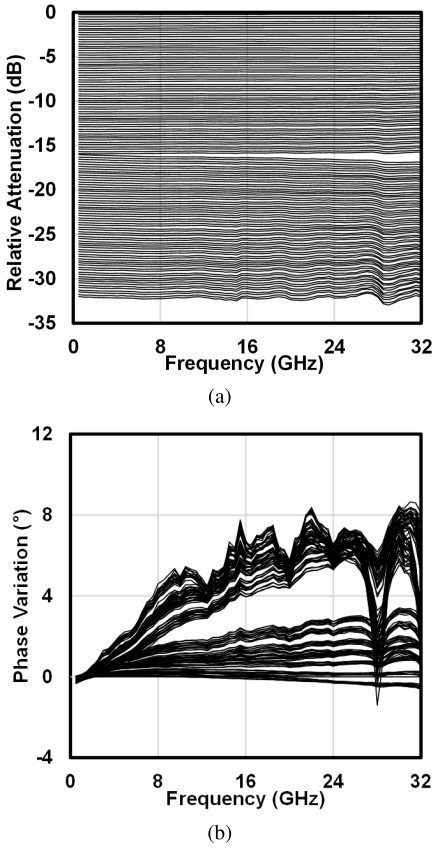


Fig. 21. Measured (a) relative attenuation and (b) phase variation versus frequency for all the 128 attenuation states.

than the simulated one (3.4 to 7.5 dB). Fig. 18(b) shows the simulated and measured phase variations of these states. The results demonstrate a similar trend between simulation and measurement, and the 16.32-dB attenuation state has a 3.3° maximum difference at 31 GHz. The transistors adopt the triple-well NMOS structure and the double-well body floating technique to reduce the IL [23]. For each transistor, the N-well (NW) and the deep-NW (DNW) guarding it are connected to 1.2 V with a large poly resistor (e.g., 16 kΩ), and the P-well (PW) where the transistor dwells in is connected to 0 V also with a large resistor. The inaccurate P-substrate model affects

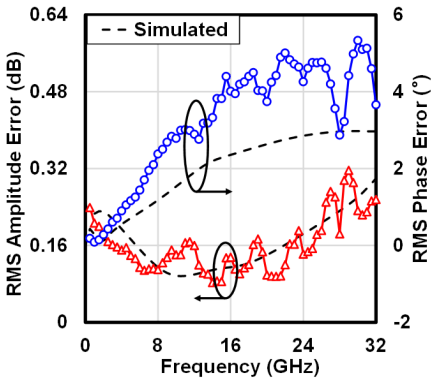


Fig. 22. Simulated and measured rms amplitude and phase errors versus frequency across 128 attenuation states.

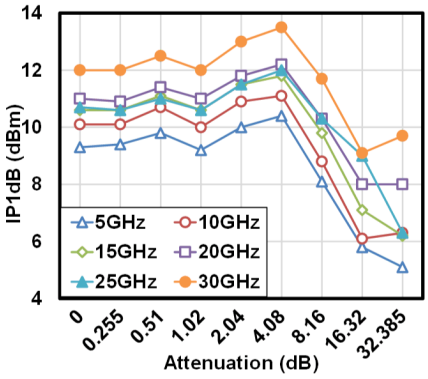


Fig. 23. Measured IP1dB for major states of the attenuator at different frequencies.

the quality factors of the reversed-biased PW-DNW and DNW-P-substrate diodes and may account for the difference between the simulation and measurement results.

Fig. 19 shows the simulated and measured S_{11} and S_{22} of eight major states. The matching performance is worse at the low frequencies than that at the high frequencies because of the optimization procedure mentioned in Section III-B. The measured S_{11} and S_{22} of all the attenuation states are better than -10.2 and -9.6 dB across 0–32 GHz, respectively, as shown in Fig. 20. Fig. 21(a) presents the measured relative attenuation for all states from 0 to 32.4 dB. The attenuation is monotonic without any crossover between adjacent states. The measured phase error varies from $-1.62°$ to $8.65°$ over 0–32 GHz, as shown in Fig. 21(b). The unshielded input and output pads create a coupling path through the substrate and may cause the amplitude and phase variation around 28 GHz. As the attenuation level rises, this coupling effect becomes more obvious. Fig. 22 shows the simulated and measured rms amplitude and phase errors. The rms amplitude error is less than 0.32 dB at 0–32 GHz, and the worst rms phase error is $5.33°$ at 30 GHz.

The IP1dB is defined as the input-referred 1-dB compression or expansion point. Fig. 23 summarizes the measurement results of the IP1dB for major states at different frequencies. Note that the gain increases with the input power in the 16.32- and 32.385-dB attenuation states due to the limited isolation of the OFF-state series transistor in the 16.32-dB attenuation unit. The measured worst case IP1dB at 5/30 GHz is 5.1/9.1 dBm.

Table V summarizes the performances of the proposed wideband attenuator and compares it with the state-of-the-art attenuators. The proposed attenuator achieves the largest operation bandwidth and the smallest area compared to the digital-step attenuators with a similar attenuation range. It also achieves state-of-the-art rms amplitude and phase errors.

VI. Conclusion

This article presents a thorough pole–zero analysis on the capacitive-compensation-based π-type and bridge-T-type attenuation units and shows that the proposed technique can extend the operation bandwidth to the *Ka*-band in the single-unit level. However, the performance enhancement comes at the cost of matching deterioration, which limits the accuracy of the whole attenuator. To address this problem, the attenuator is optimized based on the cascaded S-parameter calculation to minimize the rms amplitude and phase errors at the chip level. The 7-bit wideband attenuator has been designed and fabricated in a 55-nm CMOS process. The attenuator achieves a wide bandwidth covering dc-*Ka*-band and demonstrates a 32.4-dB attenuation range with a 0.255-dB resolution, an rms amplitude error of <0.32 dB, and an rms phase error of $<5.33°$ at 0–32 GHz. The attenuator features wide bandwidth and compact size compared with the state-of-the-art attenuators with a similar attenuation range.

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