Design of 6-bit 28GHz Phase Shifter in 65nm CMOS

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***Abstract* — This paper presents a 6-bit 28GHz phase shifter in 65nm CMOS technology. The phase shifter is composed of switching-type phase shifters to achieve low power consumption, low insertion loss, and bidirectionality. The relative phase shift varies from 0° to 354.375° with a step of 5.625°. The result of EM simulation shows that the phase shifter has the insertion loss less than 8.63dB over a frequency range of the 26.5 to 29.5GHz. The return loss is smaller than -10.5dB and the RMS phase error is 3.11°. The core size of the phase shifter is 0.38×0.98mm^2**

Keywords — Beam steering, CMOS intergrated circuits, Millimeter wave circuits, Millimeter wave phase shifters, Phased arrays, Phase shifters

I. Introduction

Mobile communication systems have been developed for a long time and reached 5G through several generations. 5G technology is expected to realize a transmission rate above 1 Gbps and therefore millimeter wave is studied around world as a way to implement such a high-speed communication with a large bandwidth [1-3]. However, because these waves are easily absorbed or scattered due to the very high frequency [4-5], beamforming technology with a phased arrays steering the radio wave to a desired direction attracts many attention these days [6]. One of necessary parts of the phased array is a phase shifter. It controls the phase of a wave, and the phase-shifted waves from different phase shifters are spatially combined in a constructive way to a specific direction, providing high directivity.

In the present paper, a 6-bit phase shifter at 28GHz is designed using a 1.2V 65-nm CMOS process evaluated by simulation. The circuit structure and basic operation principle for each phase-shift bit are described.

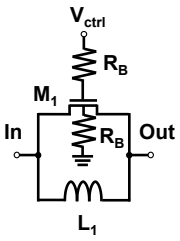
II. Phase Shifter Design

There are several methods to design phase shifters. Active phase shifters combine quadrature signals with different amplitudes to make a desired phase. This type of phase shifters doesn't have bidirectionality [7] and consumes a large power [8]. Reflective phase shifters using quadrature hybrids have a lower power consumption but its size and insertion loss become large in the CMOS technology in the millimeter wave band [9]. However, a switching-type phase shifter, in which the phase of the signal is changed by switching one of two different paths with two different fixed phases, ideally does not consume power, have low insertion loss, and can be implemented in a smaller area compared to the reflective phase shifter [8], [10]. Therefore, a switching type phase shifter is adopted in this work.

The 6-bit phase shifter consists of 180°, 90°, 45°, 22.5°, 11.25°, and 5.625° phase shift bits and each bit has reference state and phase shifting state.

A. 5.625°bit and 11.25°bit

Fig.1 shows the schematic of the 5.625° and 11.25°-bit phase shifters. Phase delay of 5.625° and 11.25° is easily realized by a single inductor. When V_{ctrl}, the control signal, is 1.2V, the phase shift bit is in reference state and the input and output ports are shirted through M_1. To reduce the insertion loss of the reference state, the body-floating technique is exploited for M_1, which in turn reduces the parasitic capacitances to the bulk substrate. When V_{ctrl} is 0V, it becomes phase shifting state and a signal passing through the phase-shifter experiences the designated phase by L_1.



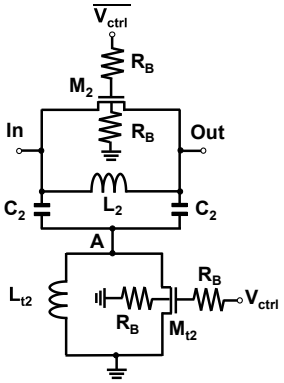
	5.625° bit	11.25° bit
M_1	80μm/60nm	
L_1	69.4pH	122pH
R_B	10kΩ	

Fig. 1. Schematic of 5.625° and 11.25° bit

B. 22.5°bit and 45°bit

As the required amount of phase shift in the phase shifter becomes bigger, the inductance of L_1 needs to be larger. A large inductance makes the pass impedance of phase-shifting state deviate from Z_0, which is the characteristic impedance of transmission line, and increases the return loss. Therefore low-pass filters are used for 22.5° bit and 45° bit as shown in Fig. 2. π-network-based low-pass filter is chosen to keep the bidirectionality and reduce the number of inductor, thereby decreasing the chip area.

In the reference state, transistor M_{t2} and M_2 is on and off respectively. The phase shifter operates as a low-pass filter consisting of C_2-L_2-C_2. In phase shifting state, M_{t2} is off and M_2 is on. M_{t2} and L_{t2} work as LC tank and provide a high impedance at node A, and signals pass through M_2.

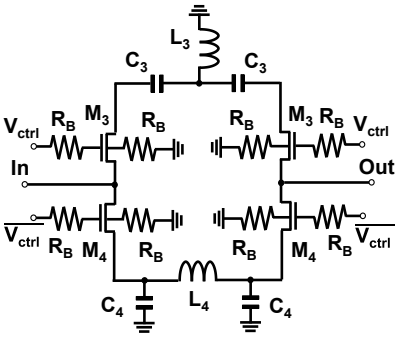


	22.5° bit	45° bit
M_2	192µm/ 60nm	110µm/ 60nm
L_2	96.0pH	120pH
C_2	34.3fF	50.1fF
M_{t2}	192µm/ 60nm	168µm/ 60nm
L_{t2}	500pH	339pH
R_B	10kΩ	

Fig. 2. Schematic of 22.5° and 45° bit

C. 90°bit and 180°bit

For 90° bit and 180°, high-pass filter is used for the reference state rather than utilizing a transistor switch as shown in Fig. 3. The reason is for this is to reduce the phase error between the reference and phase-shifting states. The amount of the phase shift of the filter is not constant with frequency and the phase error between the center and the end of the frequency band is negligible. As $d\theta/df$ is proportional to $tan\theta$ where θ is the phase shift of the filter and f is frequency, the phase error at the end of the frequency band of interest becomes bigger when the phase shift of the filter becomes bigger in the circuit shown in Fig. 2. However, as $d\theta/df$ of the high and low-pass filters are positive and negative respectively, the phase errors of the two filters cancel each other in the circuit in Fig.3. This contributes to reduce the phase error of the phase shifter. To reduce the number of inductors, T-network high-pass filter is used.



	90° bit	180° bit
M_3	192µm/ 60nm	60µm/ 60nm
L_3	244pH	256pH
C_3	9.34fF	111fF
M_4	40µm/ 60nm	80µm/ 60nm
L_4	280pH	280pH
C_4	311fF	125fF
R_B	10kΩ	

Fig. 3. Schematic of 90° and 180° bit

D. 6-bit Phase Shifter

The all aforementioned phase shifters are combined in cascade to form a 6-bit phase shifter. Although these bits are designed for their ports at Z_0, it is not perfectly matched and the port impedances vary with frequency. Therefore, the optimum sequence for the phase shifters exists to maximize the performance of the composite 6-bit phase shifter. In this work, they are arranged in the order of 45°, 11.25°, 180°, 90°, 5.625°, and 22.5° phase shifters.

III. Simulation Results

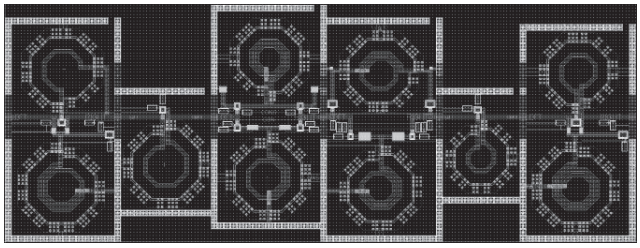


Fig. 4. Layout of 6-bit phase shifter

Fig. 4 shows the layout design of 6-bit phase shifter. The size of core area is 0.38×0.98mm^2. The EM model for each bit is generated respectively from layout of its core part. The 6-bit phase shifter is analyzed with cascaded EM models, using simulation software.

Fig. 5 and Fig. 6 represent S11 and S21 of all 64 states. The return loss is smaller than -10.5dB in the frequency range from 26.5GHz to 29.5GHz. The insertion loss is between -8.63dB and -5.65dB in the same range.

The phase shift over 64 states is represented in Fig. 7 and the RMS phase error over frequency is plotted in Fig. 8. The simulated RMS phase error is less than 3.11° in the desired operating frequency range of 26.5 to 29.5 GHz

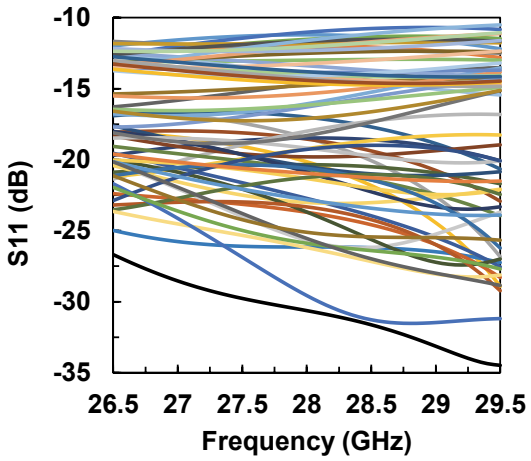


Fig. 5. Simulated S11 of the circuit

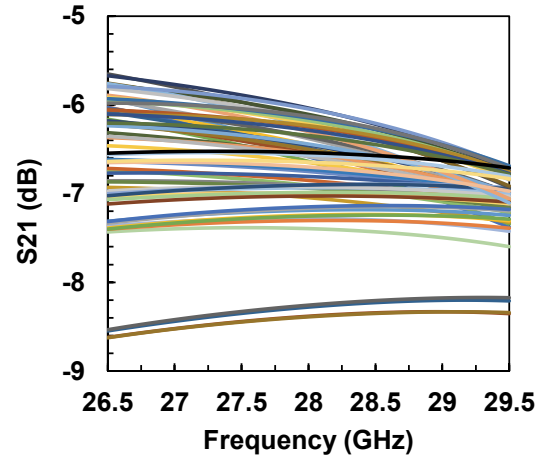


Fig. 6. Simulated S21 of the circuit

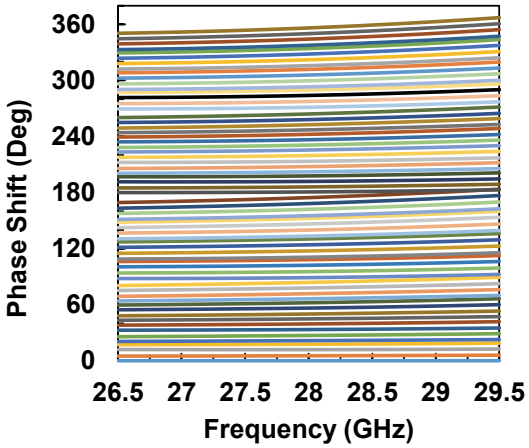


Fig. 7. Phase shift over 64 states

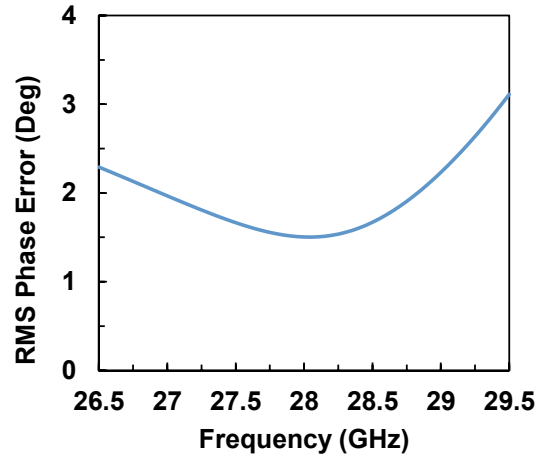


Fig. 8. RMS phase error

IV. Conclision

This paper has presented the development of a 6-bit 28GHz phase shifter in 65nm CMOS technology. It has a core area of $0.38\times0.98mm^2$. The phase-shift range is 360° by the resolution of 5.625°. The phase shifter has a simulated insertion loss less than 8.63dB and The RMS phase error smaller than 3.11° in the operating frequency.

Acknowledgement

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