A Compact and High-Linearity 140–160 GHz Active Phase Shifter in 55 nm BiCMOS

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***Abstract*— This letter presents the design of a 140–160 GHz vector-modulator-type phase shifter, integrated in a 55-nm BiCMOS technology. The circuit is optimized to minimize the occupied area and maximize the linearity, facilitating its integration in D-band phased arrays. Test results show an average insertion loss of 4.5 dB, an OP 1 dB of −3.7 dBm, and rms gain/phase errors lower than 1.4 dB and 7.5°. The circuit core occupies 0.05 mm^2, consuming less than 66 mW of dc power.**

***Index Terms*— BiCMOS, millimeter-wave (mmW), phase shifter (PS), radio frequency integrated circuit (RFIC).**

I. Introduction

In THE last few years, the *D*-band (130–170 GHz) is being investigated as a candidate to support the very high capacity backhaul links required for 5G and beyond [1], [2]. An advantage of operating in the high millimeter-wave (mmW) region is that compact phased-arrays can be built to provide beam-steering functionality and enable new flexible use of spectrum and network solutions [3].

A widespread approach in mmW phased arrays is to perform RF-level beamforming [4]–[6]: a single up(down)-converter chain is employed and each antenna element is driven by a phase shifter (PS) and a power amplifier (PA)/LNA. This way, the system can be made scalable by grouping into a single chip PS+PA or several LNA+PS chains [4], [7]. The main specs for PSs are usually phase range, resolution, and phase/gain errors. They have a direct impact both on the system gain and on the immunity to interferers due to sidelobe rejection [8], [9]. However, for *D*-band applications, size, gain, and linearity are crucial as well. To achieve a low-loss connection between the antennas and chips at mmW frequencies, the ICs can be placed on top of the antenna array and connected using Cu pillars or solder bumps [10], [11]. However, the chip size is strongly limited by the $\lambda/2$ distance between antenna elements: 1 mm at 150 GHz. Therefore, it is important that all the building blocks within the antenna driver chips occupy a small area, especially PSs and amplifiers.

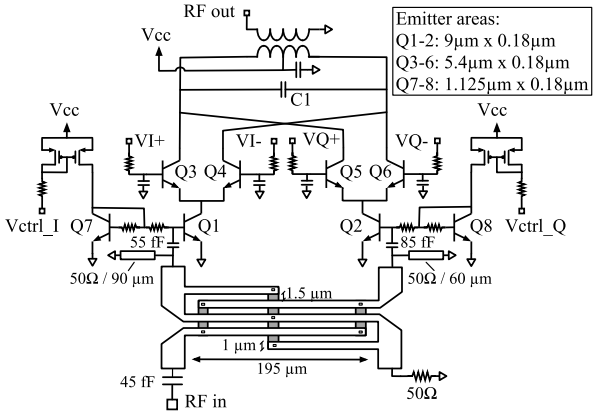

Fig. 1. Schematic of the PS circuit.

On the other hand, to deliver enough power to the TX antennas and relax the required gain for the PA, which can cause stability issues when several large stages are cascaded, the PS must exhibit high linearity and low loss as well. At the RX side, having a linear PS allows more robustness against interferers and more balanced gain and noise requirements for other building blocks.

To address the tradeoff between phase range/resolution, insertion loss, and occupied area, active PSs are usually preferred over their passive counterparts. Vector-modulator-type PSs are widely employed [12], [13], as they allow independent control of the output amplitude and phase with very high resolution. However, they commonly show a reduced output power capability due to technological limitations and to the use of several stacked transistors, requiring a very careful design when high linearity is also desired.

This letter presents a BiCMOS vector-modulator phase-shifter for *D*-band phased-arrays. It presents a very compact design, low loss, and high linearity to facilitate the integration in a phased-array system.

II. Design Description

A vector-modulator architecture is employed in this work, due to its well-known balance between area, gain, linearity, and phase resolution [5], [12]–[15]. The schematic of the circuit is depicted in Fig. 1. A Gilbert-cell summation structure with single-ended inputs and four transistors in the upper part is chosen [13], [14], at the cost of a slightly different gain at different quadrants due to a nonhomogeneous feeding

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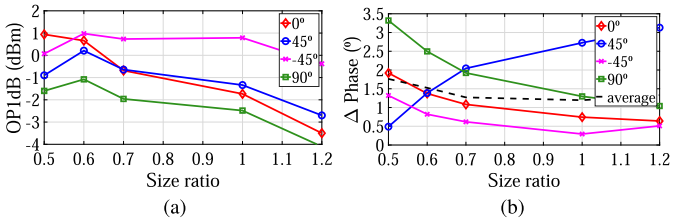

Fig. 2. Simulated linearity versus size ratio between the CB and CE transistors, for $Le_{CE} = 9$ μm. (a) OP1dB. (b) Phase distortion for Pin = 3 dBm.

of the output, as opposed to fully differential architectures that employ eight transistors for the summation [5], [12]. In turn, it allows having a more compact layout and a lower output capacitance, which improves the overall behavior at mmW frequencies. The output currents are summed by an integrated octagonal balun transformer. With an outer diameter of only 36 μm, it provides a much more compact layout than other structures such as Marchand baluns [15]. To maintain the optimal operation of the output transformer over a wide bandwidth, an array of bypass capacitors is placed at its center tap. This center tap is also used to connect the Vcc voltage. A custom-made method of moments (MOM) capacitor (C1) using the top ultrathick metal is placed at the transformer input to match the PS output to 50 Ω at 150 GHz. Electromagnetic (EM) simulations of the balun show an amplitude imbalance lower than 1 dB, Q-factors higher than 7.5, an insertion loss lower than 1.6 dB, a phase imbalance lower than 4.5° and a common-mode rejection ratio higher than 24 dB across 140–160 GHz.

The output quadrant is selected by turning Q3–Q6 on/off through their base voltages. To control the amplitude of the 0° and 90° branches of the vector modulator, Q1 and Q2 are biased using pMOS current mirrors. The pMOS transistors of this current mirror can be substituted by a current steering digital to analog converter (DAC) in an eventual fully integrated phased array [16]. With the proposed biasing structure, no extra tail current sources are required in the design and the number of stacked HBT transistors is minimized as much as possible, allowing more voltage headroom. The sizes of the transistors in the circuit core (Q1–Q6) have been selected to present a moderate output capacitance and an acceptable insertion loss at 150 GHz, while at the same time providing high output power and low phase distortion. The ratio between the common-base (CB) transistors (Q3–Q6) and the common-emitter (CE) transistors (Q1–Q2) has been optimized to maximize the circuit linearity. Fig. 2 shows the simulated OP1dB and phase distortion at 150 GHz as a function of the emitter area ratio, where the parasitics of the transistor layouts and the interconnections are taken into account by means of parasitic extraction and EM simulation. As observed, the selected size ratio of 0.6 provides the best performance in terms of OP 1 dB, for the selected bias current density. As for the phase distortion, the selected transistor sizes provide a phase variation below 2.5° for an input power of 3 dBm. The impact of the size ratio on the phase variation is smaller than on the OP1dB, as the output phase is mainly dependent on

TABLE I
COMPARISON OF 90° COUPLERS

Type	Branch line coupler	Lange coupler	Coupled TLs	Spiral coupler	Tandem coupler
Avg. ΔGain (dB) in 120-160 GHz	2	0.5	<0.2	<0.2	<0.2
Avg. ΔPhase (°) in 120-160 GHz	87.5	87.3	92	97	90.5
Size (μm^2)	205x205	35x250	4x250	60x60	120x115
Symmetrical outputs	Yes	Yes	No	No	No

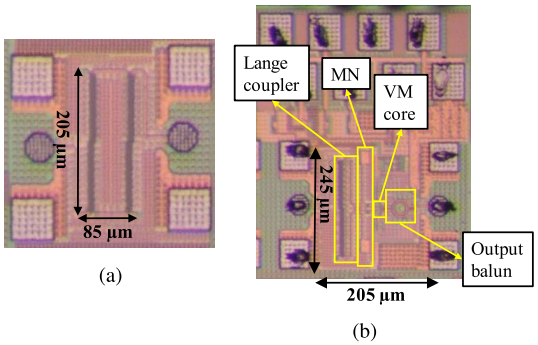

Fig. 3. Chip pictures. (a) Lange coupler back-to-back (size: 280 μm × 310 μm). (b) Complete PS (size: 430 μm × 530 μm, core: 205 μm × 245 μm).

the bias points of Q1–Q2, to whose bases the input signal is applied, rather than on the upper CB transistors.

One of the most critical parts of vector-modulator type PSs is the quadrature coupler at its input, due to its impact on the size, loss, bandwidth, and amplitude/phase imbalance of the final circuit. Table I shows a comparison of different transmission-line (TL)-based coupler structures designed for this purpose, all with a similar core insertion loss of around 1.5–2 dB at 150 GHz. The Lange coupler shows the best relationship between aspect ratio and performance, while providing symmetrical outputs that minimize the imbalances due to connections to the vector modulator core. When all the connections are taken into account, it provides an EM simulated insertion loss of 2.6 dB, a gain difference of 0.3 dB, and a phase difference of 90.8° between its outputs at 150 GHz. Matching networks consisting of a grounded stub and a series MIM capacitor are placed between the Lange coupler and the Q1–Q2 transistor inputs, to ensure an homogeneous gain response in all four quadrants and at the same time an input reflection coefficient better than −10 dB for all PS configurations. A series MIM capacitor is placed at the circuit input to provide dc decoupling. The simulated noise figure of the PS at a constant gain of −6.5 dB is between 19 and 20.5 dB, depending on the phase.

III. TEST RESULTS

A test circuit with the Lange couplers in back-to-back configuration and the whole PS circuit have been manufactured in the 55-nm BiCMOS process of STMicroelectronics, which provides HBT transistors with $f_T/f_{\max}$ of 320 GHz/370 GHz and nine metal layers (5 thin, 2 thick, 1 ultrathick, and 1 Al layer). Die pictures are shown in Fig. 3. The PS occupies only 0.05 mm^2, without pads. The circuits are measured using

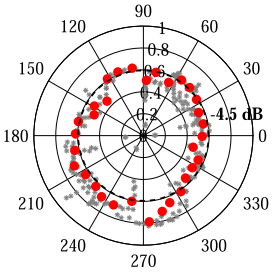

Fig. 4. Polar diagram.

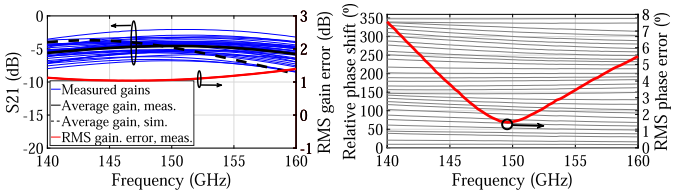

Fig. 5. (a) Simulated and measured gain and rms gain error. (b) Measured phase response.

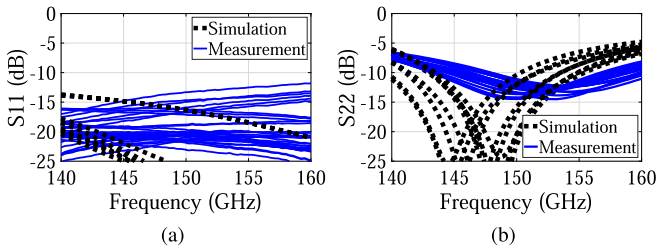

Fig. 6. (a) Input matching. (b) Output matching.

on-wafer probes and a Keysight N5245A network analyzer with Virginia Diodes Inc (VDI) 110–170 GHz frequency extenders. For power compression measurements, the input power is swept using the internal attenuator of the extenders and the output power is measured using an Erickson Instruments PM2 power meter. Two separate power supplies are used to control the gain of the 0°/90° paths, applying control voltages in a range of 1.3–3.3 V, with a resolution of 100 mV. On/off voltages of 2.5 V/0 V are applied at the bases of Q3–Q6 to select the quadrant. The maximum dc power consumption is 66 mW from a Vcc supply of 3.3 V.

The measured insertion loss of the coupler is 3.6 dB at 150 GHz, only 1 dB worse than the simulated value. The PS has been tested in 255 different configurations. For the results presentation, 32 states with similar amplitude and 11.25° spacing have been selected. Fig. 4 shows the amplitude and phase shift of the circuit in all the tested configurations at 150 GHz, where the 32 selected points are highlighted in red. It is observed that a consistent gain of −4.5 dB can be achieved for all angles in the 360° circle. The gain and phase shift for those reference 32 states are shown in Fig. 5. The average gain is −4.5 dB, centered at 150 GHz. The rms gain and phase errors are only 1.1 dB and 1.6° at 150 GHz, and lower than 1.4 dB and 7.5° between 140 and 160 GHz. Fig. 6 shows the measured and simulated S11 and S22 parameters of the complete PS for the 32 selected states. As observed, the input is well matched (S11 $<$ −10 dB) in all cases. The output matching is slightly up-shifted in frequency with

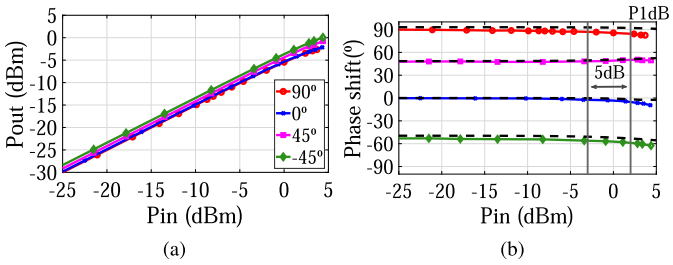

Fig. 7. (a) Pout versus Pin. (b) Phase versus Pin.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Reference.	**This work**	[18]	[14]	[5]	[13]	[15]
Technology	**55nm BiCMOS**	120nm BiCMOS	130nm BiCMOS	130nm BiCMOS	250nm InP	250nm BiCMOS
Architecture	**Vector Modulator**	Inverter + Reflect. Type	Vector Modulator	Vector Modulator	Vector Modulator	Vector Modulator
Phase range(°)	**360**	360	360	360	360	360
Gain (dB)	**-4.5**	-5.8	-6.2	12.6(1)	-13.7	-10(1)
Freq. (GHz)	**140-160**	116-128	162-190	112.5-123	220-320	110-130
IP_{1dB} (dBm)	**2**	N.A.	-13.5(2)	-13.1(1)	-0.7	2(1)
OP_{1dB} (dBm)	**-3.7**	N.A.	-20(2)	0.7(1)	-15.4	-9(1)
Max. RMS gain error (dB)	**1.4**	0.4	1	N.A.	1.2	N.A.
Max. RMS phase error (°)	**7.5**	12.5	8	N.A.	10.2	N.A.
P_{DC}(mW)/Vcc(V)	**50/3.3**	30/2.5	15.3/1.8	225(1)/2.5	42/4	74(1)/3.3
Core area(mm^2)	**0.05**	0.405	0.07	0.05(3)	0.08(4)	0.167(4)

(1)Complete chain including amplifiers. (2)Simulation.
(3)Without output balun. (4)Estimated from chip picture.

respect to simulations, but S22 is still lower than −6.5 dB over 140–160 GHz. As for the linearity, the measured Pout versus Pin curves for four different representative angles at 150 GHz are plotted in Fig. 7(a). An IP_{1dB} higher than 2 dBm is exhibited, while the OP_{1dB} is higher than −3.7 dBm. The best-case IP_{1dB} and OP_{1dB} are 4.4 and 0 dBm, respectively. Fig. 7(b) shows the simulated (dotted lines) and measured (solid lines) output phase as a function of the input power. Certain variation at high input power is observed, due to self-biasing of the input transistors, input capacitance variation, and coupling through the base-collector capacitances [17]. The maximum phase distortion at P1dB is 9°, while it stays below 3° when a 5-dB back-off is applied with respect to the P1dB.

These results are summarized in Table II, together with those of other reported PSs working above 100 GHz.

As shown, the presented PS provides an excellent ratio between OP_{1dB} and occupied area, while keeping state-of-the-art gain and phase imbalances.

IV. CONCLUSION

A 140–160 GHz PS has been presented in this letter, suitable for use in integrated *D*-Band-phased arrays. By employing the proposed circuit architecture and techniques, this circuit outperforms other state-of-the-art active PSs in terms of linearity and occupied area.

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