Digitally Assisted 28 GHz Active Phase Shifter With 0.1 dB/0.5° RMS Magnitude/Phase Errors and Enhanced Linearity

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***Abstract*—This brief presents a new digitally assisted vector-summing phase shifter (DA-VSPS) featuring high accuracy and enhanced linearity. It begins by highlighting the RF performance degradation of traditional DA-VSPSs operating at millimeter-wave frequencies due to the large number of unit-cells and the significant underlying parasitics. Then, a new DA-VSPS topology is proposed to mitigate this source of performance degradation using analog variable-gain amplifiers with digitally assisted current sources. A study of the accuracy and linearity of the proposed DA-VSPS is conducted to inform the choice of the optimal parameters (number of unit-cells and load impedance) that maximize the RF performance while minimizing the implementation complexity. A proof-of-concept prototype was implemented in 45 nm silicon-on-insulator CMOS technology. The measurement results demonstrated a 1-dB RF bandwidth from 27 to 33 GHz, root-mean-square magnitude and phase errors of 0.1 dB and 0.5° to 0.6°, respectively, while covering 360° of phase shifts at 5° resolution. Furthermore, the measured group delay and input 1dB compression point are maintained within ± 4 ps and >2.2 dBm, respectively, at any phase shift settings.**

***Index Terms*—Vector-summing, phase shifter, millimeter-wave.**

I. Introduction

THE HIGHLY sought after fifth generation (5G) wireless networks will form the information infrastructure to connect billions of people and devices with uniform quality of experience and low latency. For that, they are expected to include ultra-densely packed base-stations with large-scale antenna systems to minimize the interferences and maximize the spatial multiplexing. However, the practical implementation of the 5G radio hardware will be very challenging because of the very stringent requirements introduced by 3GPP release 15. In particular, it will be difficult to satisfy the required error vector magnitude (EVM) when transmitting millimeter-wave (mm-wave) vector modulated signals with a modulation bandwidth of up to 1.2 GHz [1].

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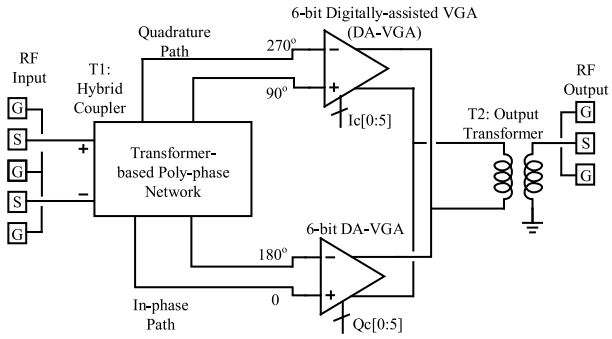

Fig. 1. Block diagram of the proposed digitally assisted vector-summing phase shifter (DA-VSPS).

The successful deployment of 5G large-scale antenna systems require RF phase shifters to achieve low insertion loss, group delay variation, and phase error across the targeted modulation bandwidth, while minimizing DC power consumption and nonlinear distortions. In the literature, a variety of passive phase shifters, including switched [2], reflective [3] or true-time delay [4] were reported. While high-linearity and zero power consumption are attractive features of passive phase shifters, they tend to exhibit large variations of the ILs, input and output impedances and group delay with the phase setting. In contrast, vector-summing phase shifters (VSPS) have prompted growing interests as they allow simultaneous control of the magnitude and phase and exhibit lower group delay variation. Yet, the application of VSPS to mm-wave frequencies faces significant challenges due to the worsening circuit parasitics that limit the performance of the constituent components, namely, the 90° hybrid coupler and the VGAs. Research in [5]–[9] suggested different active or passive monolithically integrated 90° hybrid couplers with enhanced performance. However, the various digitally-assisted VGA topologies recently reported in [7]–[9] tend to suffer from low magnitude and phase accuracy due to the large number of unit-cells and the underlying significant parasitic. They also yield low input 1dB compression point (IP1dB) power of maximum -6 dBm [5]–[7], [9], which makes them more tailored to the receiver side and not for the transmitters.

In this brief, a new digitally-assisted VSPS (DA-VSPS) operating in the 28 GHz band is presented. It relies on a new digitally-assisted VGA (DA-VGA) topology where an analog VGA and a digitally-assisted current source were suitably devised to harness the accuracy of digitally-controlled analog

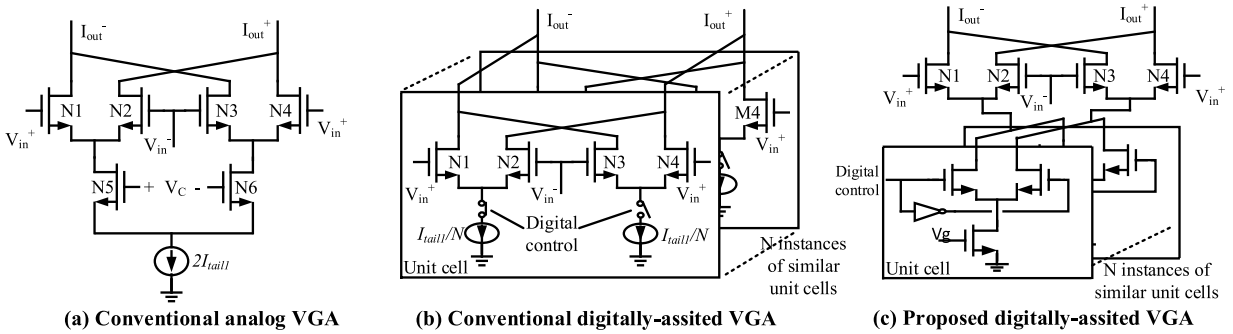

Fig. 2. Schematic of (a) conventional analog VGA (b) conventional DA-VGA and (c) the proposed DA-VGA.

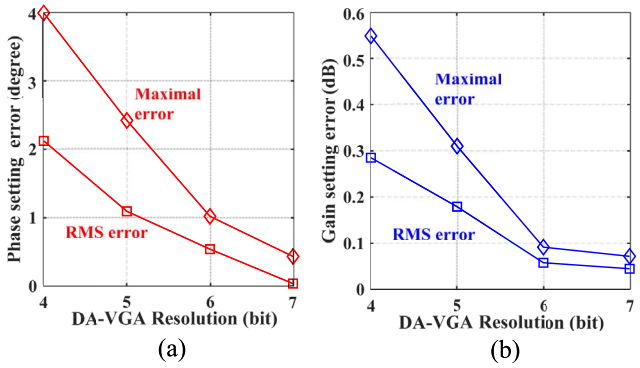

Fig. 3. Calculated DA-VSPS (a) phase and (b) gain setting errors when its two DA-VGAs have finite gain control resolution.

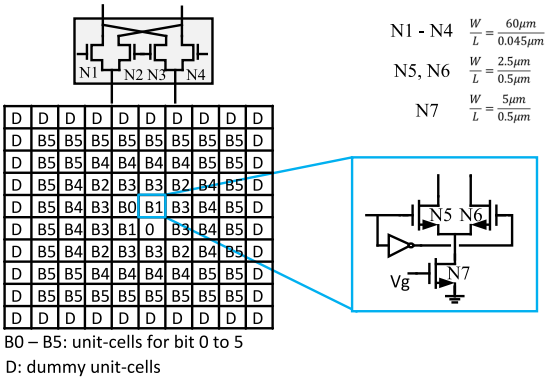

Fig. 4. Schematic and floor plan of the proposed 6-bit DA-VGA.

circuits while minimizing the effects of the parasitics on the VGA block.

II. Proposed DA-VSPS Circuit Topology and Implementation

Fig. 1 shows the block diagram of the proposed DA-VSPS, which consists of a 90° hybrid coupler (T1, transformer-based poly-phase network [10]), two digitally-assisted variable-gain amplifiers (DA-VGAs) and an output transformer (T2). Ideally, the hybrid coupler splits the RF input signal into in-phase (I_{RF}) and quadrature-phase (Q_{RF}) signals with equal magnitude and 90° relative phase difference. The I_{RF} and Q_{RF} signals are then weighted by the gains of the two corresponding VGAs, which are set by control signals I_C and Q_C. Finally, the combining of the VGAs output signals yields an output signal, which is equal to magnitude and phase adjusted version of the input RF signal.

To maximize the performance of the VSPS, the VGAs need to exhibit a linear-in-magnitude gain control response while maintaining minimal phase variation versus different values of I_C and Q_C. Among the various VGA topologies used in VSPS [5]–[7], [9], [11], the Gilbert-cell based one, which is shown in Fig. 2a, has the advantage of producing low phase variation, due to the double-balanced transconductance stage ($N_1 - N_4$). However, the nonlinearity in the tail current soruces ($N5$ and $N6$) translates into a nonlinear VGA gain control. To mitigate this issue, Fig. 2b depicts an example of digitally-assisted VGA [8]. Here, the Gilbert-cell based analog VGA in Fig. 2a is partitioned into multiple smaller unit-cells, which are switched on or off depending on the digital control word. This allows an improved gain control linearity compared to the one in Fig. 2a. Yet, the significant parasitics associated with the large number of unit-cells needed for achieving the desired resolution leads to a poor matching between $N1$ to $N4$, which degrades the RF performances in the resulting DA-VSPS. To address this performance limitation, this brief proposes a new DA-VGA topology shown in Fig. 2c. The proposed topology includes a single transconductance stage (N1-N4) that can be optimized to minimize the impact of the parasitics and mismatch between the four matched transistors using suitable layout strategies such as common-centroid and inter-digitization. The gain control is achieved digitally by switching the appropriate number of unit-cells depending on the control codeword. As explained in the following two sub-sections, a study of the accuracy and linearity is conducted on the proposed DA-VSPS in order to inform the choice of the optimal design parameters using the proposed DA-VGA in Fig. 2c while minimizing the implementation complexity.

A. DA-VSPS Accuracy Enhancement

In the following, the minimum number of control bits, N, needed to provide a phase control over 360° with a step $\theta = 5°$ is carefully determined. Assuming that each of the DA-VGA in Fig. 2c is controlled using a codeword of N bits, the total number of possible settings of the DA-VSPS is consequently equal to $M = 2^{2N}$. The magnitude and phase errors of the DA-VSPS are computed when N is varied between 4 and 7. As per Fig. 3, when $N = 4$, the RMS and maximal phase error of an ideal DA-VSPS are as high as 2.1° and 4°, respectively. In addition, the error reduces below 1° for $N = 6$ or higher. In this brief the number of control bits is fixed to 6.

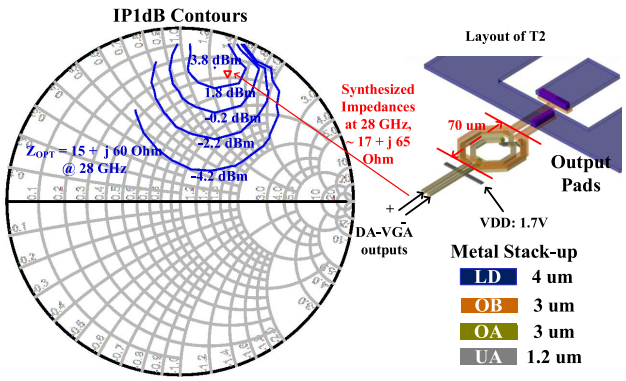

Fig. 5. Load-pull results of the optimal impedance needed for maximizing the IP1dB.

Fig. 4 illustrates the schematic and floor plan of the proposed 6-bit DA-VGA. The transconductance stage (N1-N4) are implemented using n-type transistors each with a gate width and length of 60μm and 45nm, respectively. Then, the remaining circuitry of the DA-VGA is segmented into 63 equally-sized unit-cells. To minimize the mismatches among the unit-cells due to process variations, they were designed with n-type transistors of much wider channel width and length (see Fig. 4). Moreover, they were arranged around a common centroid. It is to note these accuracy-enhancement layout techniques are not applicable to the conventional DA-VGA topology depicted in Fig. 2b, due to the large number of unit-cells (63 in this case) and the incurred routing parasitics at the mm-wave frequency. In contrast, the proposed DA-VGA topology separates N1-N4 from the gain-control unit-cells, hence increasing the number of unit-cells is made possible and consequently both accuracy and RF performance (e.g., bandwidth, IL and linearity) can be maximized.

B. DA-VSPS Linearity Enhancement

Traditionally, VSPS has been designed using linear circuit theory, where the RF performance are optimized assuming small-signal operation. While this assumption can be satisfied in the receiver-side, it is critical to extend the design methodology of the VSPS to maximize its performance under large-signal excitation conditions that are likely to occur in the transmitter-side. In particular, in this extended design methodology, it is critical to determine the optimal load impedance presented to the DA-VGAs in the VSPS to maximize the large-signal performance. This was achieved using load-pull technique where the IP1dB of VSPS was determined while sweeping the load impedance presented to the output terminals of DA-VGAs. This analysis was conducted while the gain and phase of DA-VSPS are set to peak gain and 0°, respectively. This setting was chosen as it is expected to yield the lowest IP1dB, since the first and second VGAs are configured to achieve the maximum and minimum gains, respectively. As shown in Fig. 5, an optimal load impedance (Z_{opt}) of $\sim 15 + j60$ ohm allowed for an 3.8dBm IP1dB at 28 GHz. Subsequently, this optimal impedance was realized by transforming the 50 ohm termination using a transformer-based matching network (T2 in Fig. 1). This transformer has a turns-ratio of 2 to 1 and is implemented using the two top-most copper layers (OA/OB) offered in 45nm SOI-CMOS process,

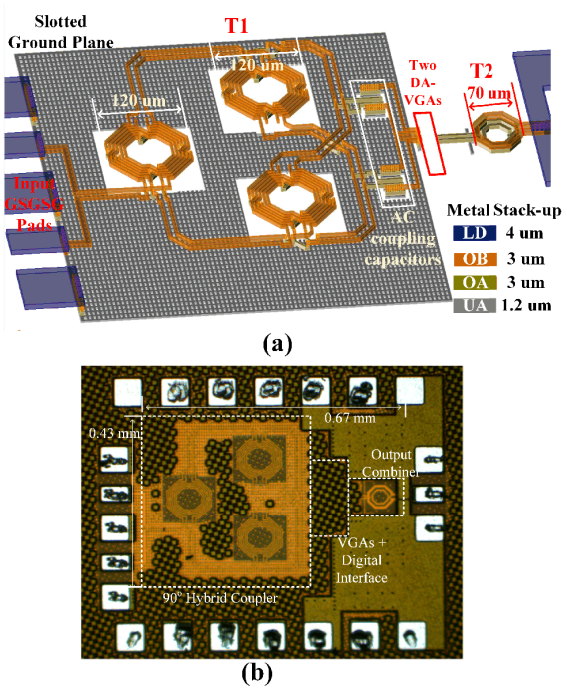

Fig. 6. (a) three-dimensional view of the overall floorplan of the proposed DA-VSPS. (b) microphotograph of a fabricated DA-VSPS prototype.

as shown in Fig. 5. The transformer's electro-magnetic (EM) simulations revealed a primary and secondary self-inductances of 420 pH and 180 pH, a coupling factor of 0.59 and an insertion loss of 1.8 dB in T2 at 28 GHz. The simulation confirmed also a transformed impedance equal to $\sim 17 + j65$ ohm at 28 GHz, which is very close to the desired Z_{opt}.

Fig. 6(a) shows an overall three-dimensional view of the proposed DA-VSPS. In addition to the two instances of DA-VGAs and T2, the proposed DA-VSPS includes an on-chip 90° hybrid coupler (T1), which is synthesized using a two-stage transformer-based poly-phase network [10] to broaden its bandwidth. EM simulation revealed that T1 maintained a meager insertion loss variation of -1 ± 0.5dB, a magnitude and phase imbalance of < 0.3 dB and 1.2°, respectively, between 20 to 40 GHz.

III. Measurement Results

Fig. 6(b) shows the microphotograph of the proposed DA-VSPS prototype fabricated in GlobalFoundries 45 nm SOI-CMOS process. The characterization of the fabricated chip was conducted using a vector network analyzer (Keysight N5247A) along with a FPGA which is programmed to produce the digital codewords. During these experiments, the DA-VSPS has been configured in three different operating conditions, namely:

a) *Test One:* In this test, one of the two DA-VGAs is turned-on while the other one is turned off. Fig. 7 shows a good agreement between the simulated and measured gains of the DA-VGA (G_{VGA}) at 28 GHz for all the values of the digital codewords (i.e., 6-bit resolution). According to Fig. 7, the magnitude of G_{VGA} can be varied from 0.032 to 1 (normalized gain) and a phase variation of ±2° is achieved for a gain control range of 24 dB.

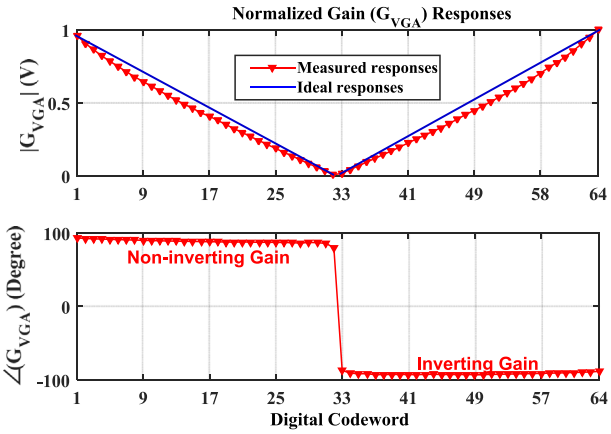

Fig. 7. Measured (a) gain and (b) phase from one unit of DA-VGA.

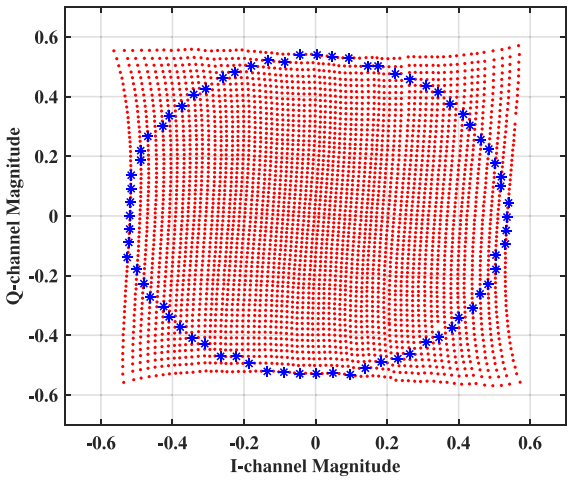

Fig. 8. Measured constellation plot (in red dot) and the selected 72 settings (in blue) for the LUT.

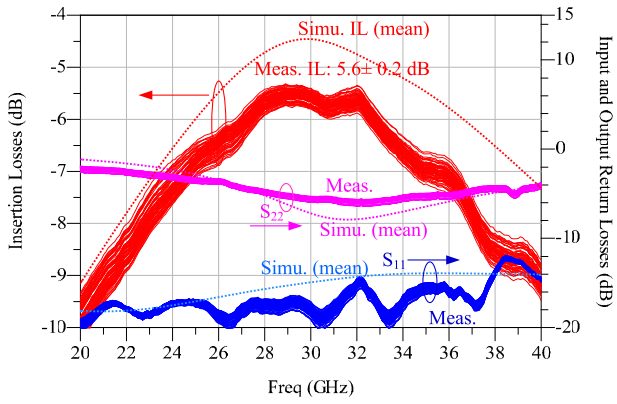

Fig. 9. Measured insertion losses, input and output return losses of the proposed phase shifter.

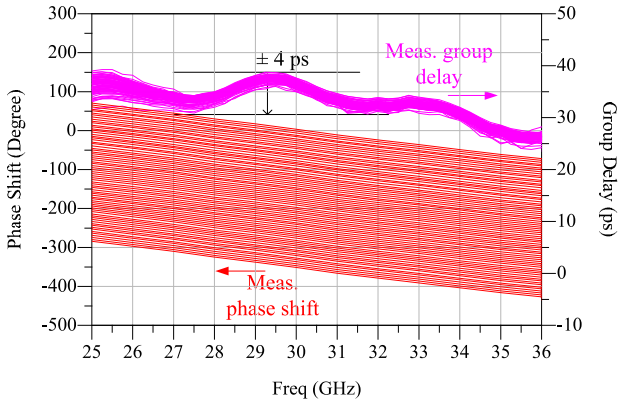

Fig. 10. Measured phase shifts and group delays of the proposed phase shifter.

b) *Test Two:* In this test, both DA-VGAs were turned on and the complex gain (G_{PS}) of the DA-VSPS was characterized at 28 GHz for all possible values of the codewords. The measured G_{PS} is depicted in Fig. 8. It reveals a relatively uniform distribution of the measured data points, which is used to form a look-up table (LUT) with 72 entries that stores the codewords needed to achieve phase shifts over 360° in a step of 5° while maximizing the phase accuracy and minimizing the magnitude variation.

Fig. 9 shows the simulated and measured small-signal performances (ILs, input and output return losses, S_{11} and S_{22}, respectively) corresponding to the 72 LUT entries when the frequency of the input signal is varied from 20 to 40 GHz. According to Fig. 9, the proposed DA-VSPS has an average IL of -5.6 dB at 28 GHz with an IL variation of only $\pm 0.2dB$. Furthermore, a 1dB RF bandwidth of between 27 - 33GHz was achieved. Moreover, the proposed DA-VSPS maintained relatively constant values of S_{11} and S_{22} across 360° of phase shifts. This is an important consideration in designing the RF beamforming system, as the variation of S_{11} and S_{22} will induce magnitude and phase errors when the VSPS is cascaded with the other building blocks in the transmitter.

Fig. 10 confirms the proposed DA-VSPS achieving constant group delays ($\pm 4ps$ between 27–33 GHz) and consequently linear phase variation versus frequency over the entire 360° of phase shift range.

Fig. 11 depicts the RMS phase and magnitude errors of the proposed DA-VSPS versus frequency. According to Fig. 11, at 28 GHz which corresponds to the frequency used to construct the LUT entries, the lowest RMS magnitude and phase errors of $0.1dB$ and 0.5°, respectively, were achieved. As the frequency deviates from 28 GHz, the RMS magnitude error remained at 0.1 dB and the RMS phase error had a maximum value of 0.8° at 36 GHz. The phase error can be lowered at a given frequency if the LUT entries were determined at that frequency.

c) *Test Three*: In this test, the IP1dB of the proposed DA-VSPS was evaluated for all 360° of phase shift settings between its 1dB RF bandwidth (27 - 33GHz). According to Fig. 12, the proposed DA-VSPS achieved a measured IP1dB of 2.2 - 4.7 dBm at all 360° phase settings. To further assess linearity of the proposed DA-VSPS, the amplitude-to-phase modulation (AM-PM) and phase accuracy were measured for input power levels spanning from -10 dBm to IP1dB and shown in Fig. 13(a) and (b), respectively. As one can deduce from Fig. 13(b), a phase error of $< 2.6°$ or below was maintained over the entire power range and for all phase shift settings.

Table I summarizes the measured performance of the fabricated DA-VSPS and compares them with recently reported VSPSs operating at similar frequencies. According to Table I,

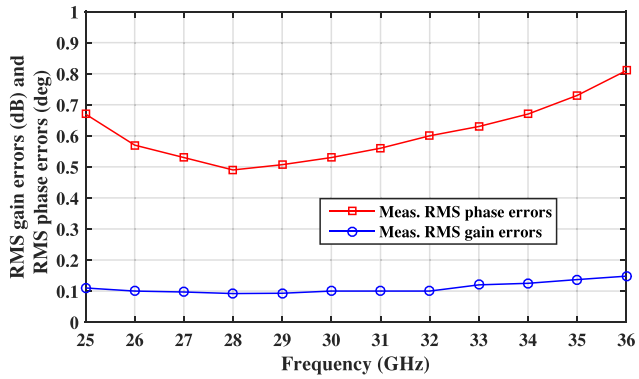

Fig. 11. Measured RMS phase errors and gain errors of the proposed phase shifter.

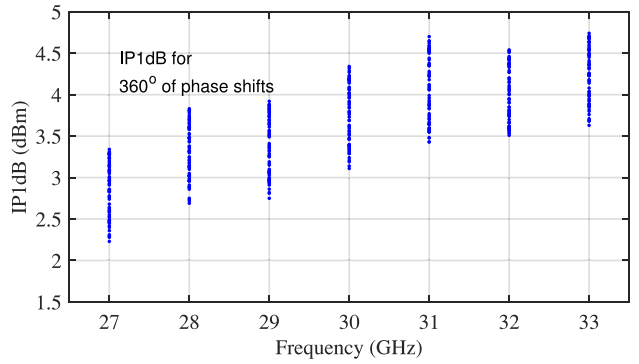

Fig. 12. Measured IP_{1dB} for all phase shift settings.

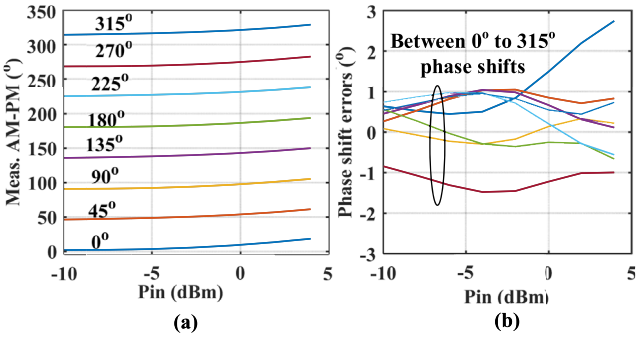

Fig. 13. Measured (a) AM-PM and (b) phase errors covering 360° of phase shifts at 28 GHz.

the proposed DA-VSPS demonstrated the best overall accuracy in terms of RMS phase errors (0.5°) and magnitude variation (±0.2dB). Furthermore, it significantly outperforms the previous works in terms of IP1dB (2.2*dBm*) while consuming comparable DC power (25 mW) and occupying similar chip size (0.27 mm^2). This confirms the validity of the proposed accuracy and linearity enhancement methodology for designing the mm-Wave DA-VSPS.

IV. Conclusion

This brief presented a new digitally-assisted vector-summing phase shifter (DA-VSPS) with enhanced magnitude and phase accuracy and linearity at millimeter-wave frequencies. The proposed DA-VSPS is built upon a newly devised digitally-assisted VGA topology, where an analog VGA is augmented with digitally-assisted tail current sources to realize linear-in-magnitude gain control while minimizing circuit parasitics due to the large number of unit-cells. Measurement results of the DA-VSPS prototype fabricated using 45nm SOI-CMOS technology revealed RMS magnitude and phase errors of 0.1dB and 0.5°, respectively, between 27 - 33 GHz. Furthermore, a relatively high IP1dB of >2.2 dBm was obtained over the targeted bandwidth. These results confirm the accuracy and linearity enhancement of the proposed DA-VSPS and suggest its promising application for realizing RF phase shifting in the massive-MIMO transmitters.

TABLE I
Comparison of Recent VSPSs

	This work	[5]	[7]	[8]	[6]
CMOS Tech.	**45 nm SOI**	130 nm	130nm SiGe	65nm	180nm SiGe
Freq. (GHz)	**27-33**(1)	24.5-27.4(2)	20.5-26.5(2)	2-20(2)	15-35(3)
Avg. IL (dB)	**-5.8**	-6.1	-1	-4.3	-6
Mag. Variation (dB)	**±0.2**(5)	±1.5(5)	±0.8(6)	±0.8(6)	±2(7)
RMS phase error (deg)	**0.5-0.8**(5)	<2.6(5)	1.2(6)	1.22(6)	4.2-13(7)
Phase resolution	**5°**	Cont.	5°	5°	Cont.
IP1dB (dBm)	**2.2**	-9.2	-16	-	-7
DC Power (mW)	**25**	27	10	92	25.2
Area (mm^2)	**0.27**	0.25	0.12	0.9(4)	0.19
Control	**Digital**	Analog	Digital	Digital	Analog

(1) 1-dB RF bandwidth (2) 3-dB RF bandwidth (3) Bandwidth of quadrature phase shifter only
(4) estimated from figure (5) over 3dB RF bandwidth (6) at the center freq. (7) between 15 – 35 GHz

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