A 45–75 GHz Vector Modulator MMIC With Built-In Voltage Converter

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***Abstract*— This letter presents a 45–75 GHz balanced vector modulator (VM) with a built-in voltage converter for quadrature phase shift keying modulation. With embedded voltage converter, the design becomes less sensitive to threshold voltage variation. The effect of the Lange coupler's coupling factor and cold FET's total gate width on wideband symmetry performance of the modulator is investigated. A 30-GHz operation bandwidth centered at 60 GHz is achieved by using a 0.15-μm GaAs pHEMT process. On-wafer measurement results of the VM show that, from 58 to 67 GHz, the amplitude and phase errors are better than ±0.45 dB and ±2°, respectively. Within a wide frequency range of 45–67 GHz, for all modulation states, the amplitude and phase errors are within ±0.9 dB and ±4°, respectively, while the insertion loss is less than 11.5 dB and return loss is better than 10 dB.**

***Index Terms*— 60 GHz, BPSK, microwave monolithic integrated circuit (MMIC), QPSK, vector modulator (VM), wideband.**

I. Introduction

VECTOR modulator (VM) plays increasingly an important role in millimeter-wave direct carrier modulation [1] and phased-array transceiver [2] applications due to its capacity of direct multilevel amplitude and 360° phase control at millimeter-wave frequencies.

A general approach for VM, which is composed by the in-phase combination of two orthogonal bi-phase amplitude modulators (BM), was developed in [3]. The single-reflection BM in [3] utilizes GaAs FET as variable resistance reflection termination. However, this termination is not ideal "ON" and "OFF" due to parasitics at millimeter-wave frequencies. In [4], a method by adding shunt resistor to the variable termination is proposed to correct the asymmetry caused by parasitics. However, this compensation technique is only suitable for narrowband applications. To solve this problem, a balanced or a push-pull structure VM [5]–[7] has been proposed, in which bi-phase function is realized by combining two conventional single-reflection BMs in an out-phase connection. Performance of the balanced topology is not affected by parasitics since it will be canceled in the out-phase combination realized by two Lange couplers. In [1], theoretical analysis of design equations of the balanced VM is presented, but the analysis is based on only center frequency of the Lange coupler. In [2], an H-band VM is implemented in 50-nm GaAs mHEMT process, in which branch-line hybrid is utilized to generate orthogonal signal, and variable gain amplifiers (VGAs) are used to control each signal's amplitude. A 360° phase shifter [8] implemented in CMOS process is realized based on VM formation, but only phase modulation is employed. VGAs are also utilized to control the magnitude of each BM. However, under different gain settings of the VGA the phase varies [2], especially within a wide frequency range, which will limit the bandwidth of these designs. Therefore, the bandwidth of VMs can be further improved.

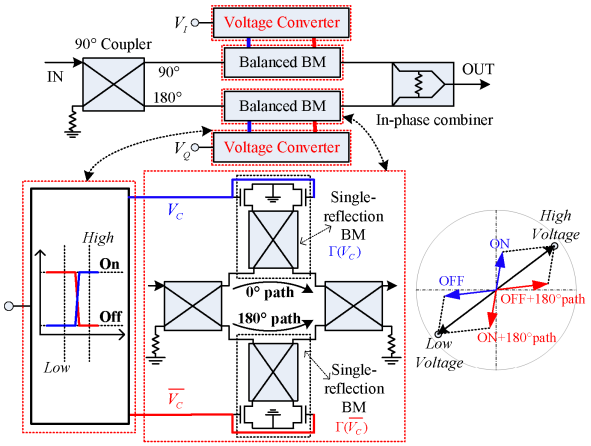

Fig. 1. Proposed configuration of 45–75 GHz balanced VM with built-in voltage converter.

In this letter, a wideband 60-GHz balanced VM microwave monolithic integrated circuit (MMIC) with the built-in voltage converter is proposed, as the architecture shown in Fig. 1. Wideband behavior of balanced VM is investigated, and a method to improve wideband symmetry performance by adjusting parameters of FET termination and Lange coupler is illustrated. The proposed design is verified experimentally using the on-wafer measurement. The built-in converter is designed to control "ON" and "OFF" states of FETs in each BM according to input signal, as illustrated in Fig. 1. The proposed converter can also avoid the variation due to the threshold voltage change.

II. 60-GHz Balanced Vector Modulator Design

As illustrated in Fig. 1, two single-reflection BMs in out-phase connection are controlled by complementary voltages V_C and $\overline{V_C}$ generated by embedded voltage converter from high or low input signal, either V_I or V_Q.

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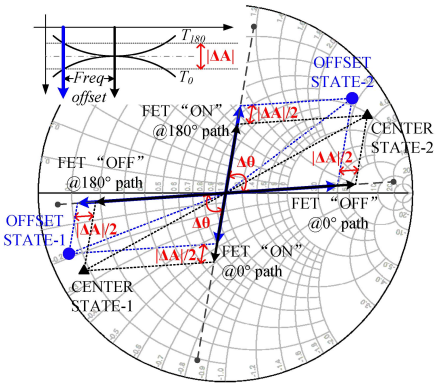

Fig. 2. Vector diagram of balanced BM.

A. Wideband Design Technique

To realize wideband performance with minimized phase and amplitude error, it is crucial to minimize the imbalance from the BM when frequency is offset from center frequency. The transmission coefficient at any frequencies for the balanced BM can be written as follows:

$$S_{21}^{\mathrm{BM}} = T_0 \cdot \Gamma(V_C) - T_{180} \cdot \Gamma(\overline{V_C}) \tag{1}$$

where Γ is the response of single-reflection BM; T_0 and T_{180} are the transmission coefficient of 0° and 180° paths. To evaluate both phase and amplitude error, we introduce an evaluation factor based on [1]

$$K_B = \frac{\left|S_{21}^{\mathrm{HIGH}} - S_{21}^{\mathrm{LOW}}\right|}{\left|S_{21}^{\mathrm{HIGH}} + S_{21}^{\mathrm{LOW}}\right|} \tag{2}$$

From (1) and (2), K_B can be calculated by

$$\begin{aligned} K_B &= \left|\frac{T_0 + T_{180}}{T_0 - T_{180}}\right| \cdot \frac{|\Gamma_{\mathrm{ON}} - \Gamma_{\mathrm{OFF}}|}{|\Gamma_{\mathrm{ON}} + \Gamma_{\mathrm{OFF}}|} \\ &= \frac{T_0 + T_{180}}{|\Delta A|} \cdot \sqrt{\frac{A_{\mathrm{mp}} + 2\cos\Delta\theta}{A_{\mathrm{mp}} - 2\cos\Delta\theta}} \end{aligned} \tag{3}$$

where

$$A_{\mathrm{mp}} = |\Gamma_{\mathrm{ON}}|/|\Gamma_{\mathrm{OFF}}| + |\Gamma_{\mathrm{OFF}}|/|\Gamma_{\mathrm{ON}}| \tag{4}$$

$$|\Delta A| = |T_0 - T_{180}| \tag{5}$$

$$\Delta\theta = \angle\Gamma_{\mathrm{ON}} - \angle\Gamma_{\mathrm{OFF}} - 180° \tag{6}$$

$|\Delta A|$ is the amplitude difference between 0° and 180° paths which is due to the intrinsic imbalance of Lange coupler when frequency is offset from center frequency. $\Delta\theta$ refers to the phase deviation from perfect symmetry of single-reflection BM's "ON" and "OFF" states, of which the existence has been investigated due to parasitic ON-state resistance R_{ON} and pinch-off capacitance C_{OFF} [6] at millimeter-wave frequencies. As revealed in (3), to make this evaluation factor K_B larger, value of $|\Delta A|$ and $|\Delta\theta|$ must be as small as possible. The symmetry performance at center and offset frequency is illustrated in the vector diagram of balanced BM in Fig. 2, which also suggests that both $\Delta\theta$ and $|\Delta A|$ induce unsymmetrical characteristic of two modulation states of the balanced BM at offset frequency.

For wideband symmetrical operation of balanced BM, both $|\Delta A|$ and $|\Delta\theta|$ should be minimized in operation frequency band. $|\Delta A|$ can be tuned by changing the coupling factor of Lange coupler; $|\Delta\theta|$ highly depends on FET parasitics, which can be tuned by changing FET geometry. Therefore, based on the 0.15-μm GaAs pHEMT process, we investigate the minimum K_B within the frequency range of 45–75 GHz, with total gate width between 50 and 150 μm, and coupling factor of Lange coupler ranging from −2.5 to −3.2 dB, as shown in the contour in Fig. 3. Since minimum K_B suggests the worst unsymmetrical case in the frequency range, the larger value of "minimum K_B" means the better wideband symmetry performance. Thus, in this design, we choose Lange coupler with coupling factor of −2.8 dB and cold FET size of 2×40 μm.

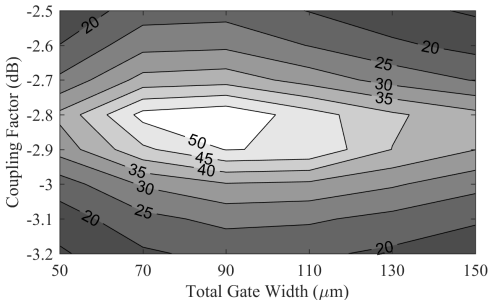

Fig. 3. Minimum evaluation factor within 45–75 GHz.

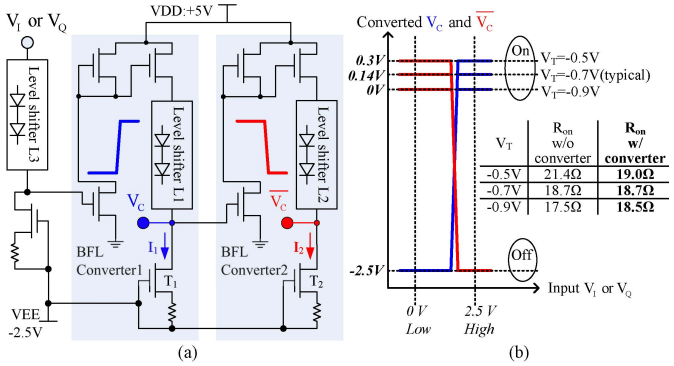

Fig. 4. Built-in control voltage converter. (a) Schematic. (b) Response.

B. Built-In Voltage Converter

The proposed on-chip voltage converter is composed of two sets of converters which utilize GaAs buffered FET logic for the inversion function, as illustrated in Fig. 4(a).

One advantage of the proposed converter is that threshold voltage (V_T) variation effects on R_{ON} can be reduced. Normally R_{ON} will become larger if V_T increases; hence, "ON" voltage should be raised accordingly to guarantee same R_{ON} for the cold FET termination. In the proposed configuration, when V_C is of "ON" control state, if V_T increases current I_1 will drop thus the voltage shift from the level shifter L1 will be smaller. Therefore "ON" voltage V_C will increase with V_T, and the same analysis is also applicable for $\overline{V_C}$. For this design, the low and high input signals are 0 and 2.5 V, and generated "ON" and "OFF" voltages are 0.14 and −2.5 V at typical V_T of −0.7 V. Converted voltages and comparison of R_{ON} under three sets of V_T are illustrated in Fig. 4(b). With V_T increasing from −0.9 to −0.5 V, "ON" voltage increases from 0 to 0.3 V, making R_{ON} more constant compared to the

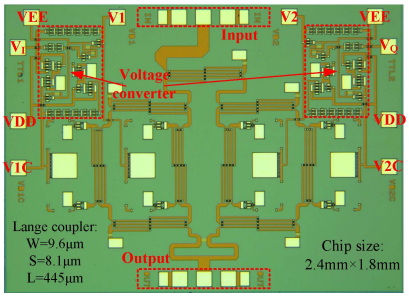

Fig. 5. Chip photograph of fabricated 45–75 GHz VM.

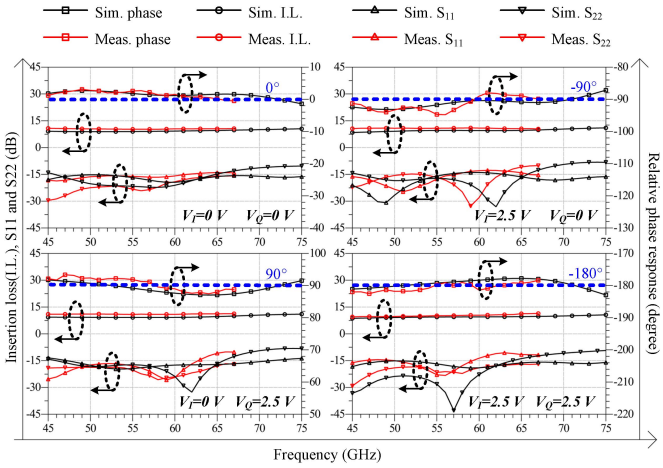

Fig. 6. Measured and simulation response under four modulation states.

case without proposed converter. Thus, with proposed voltage converter, it is less sensitive to threshold voltage variation.

III. Measurement Results

The proposed 45–75 GHz VM is fabricated in 0.15-μm GaAs pHEMT process. The chip photograph is shown in Fig. 5; the VM can also be directly controlled using the interface of V1, V2, V1C, and V2C without the converter. Static on-wafer small signal measurement has been performed from 45 to 67 GHz due to constraints of measurement facilities. Built-in converter is used to control the four states of QPSK during measurement. Once symmetry result is achieved for QPSK modulation, symmetric performance for higher-level modulation can be obtained by a control voltage calibration procedure [2], [6], [7].

Comparison of simulation and measurement result is illustrated in Fig. 6. Under four modulation states within tested frequency range, average insertion loss is 10 dB with amplitude error less than 0.9 dB (rms error < 0.6 dB), while input and output return losses are better than 10 dB. Relative phase response is calculated by the difference of absolute phase response and average value of four modulation states. Based on the measured phase response, phase error is within ±2° from 58 to 67 GHz and better than ±4° (rms error < 3°) in whole measured band. A good agreement between measurement and simulation results is achieved.

The performance comparison is summarized in Table I. Compared to other designs, the designed VM achieves 30-GHz bandwidth with low amplitude and phase error at 60 GHz, and avoids the additional requirement on digital-to-analog converter (DAC) for QPSK modulation with the built-in converter.

TABLE I
Performance Summary of Reported VM

Ref.	[1]	[2]	[6]	[8]	This work
Tech.	0.15-μm HEMT	50-nm HEMT	0.25-μm HEMT	90-nm CMOS	0.15-μm HEMT
Freq. (GHz)	40	240-270	55-65	50-70	45-75
Phase Error (°)	±1.5	RMS* <12.5	<±2	<±5.1	±1.5@60GHz <±2(58~67GHz) <±4(45~67GHz) RMS*<3
Amp. Error (dB)	±0.3	RMS* <1.8	<±0.3	<±0.6	±0.3@60GHz <±0.45(58~67GHz) <±0.9(45~67GHz) RMS*<0.6
Modu-lation#	Voltage Sweep &CVC†	4-bit$ PS &CVC†	Voltage Sweep &CVC†	5-bit$ PS	QPSK (2-bit$ PS)
DAC Req.	Yes	Yes	Yes	No	No

Modulation condition specified for measured static symmetry result.
$ n-bit phase shift can be treated as 2^n PSK concerning static symmetry result.
* Root-Mean-Square (RMS). † Control Voltage Calibration (CVC).

IV. Conclusion

In this letter, a wideband 60-GHz balanced VM MMIC with embedded voltage converter implemented in 0.15-μm GaAs pHEMT process is presented. Design technique which highlights the effect of coupler's coupling factor and FET's total gate width on wideband symmetry performance is proposed and verified experimentally. With the proposed voltage converter, DAC requirement for QPSK modulation is avoided and sensitivity problem due to threshold voltage variation is mitigated. The proposed design will be suitable for various millimeter-wave applications in the wide operation frequency range.

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