A 10 MHz - 6 GHz High Power High Linearity 35 dB Digital Step Attenuator MMIC Using GaN HEMTs with TaON Passivation

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***Abstract*—This paper describes a 10 MHz - 6 GHz high power high linearity 35 dB digital step attenuator monolithic microwave integrated circuit (MMIC) for radio frequency automated test equipment (RF ATE) systems. The digital step attenuator MMIC is fabricated using a novel Schottky gallium nitride high electron mobility transistor (GaN HEMT) process that is characterized in very low gate leakage current with tantalum oxy nitride (TaON) passivation technology. Owing to the characteristic of the developed GaN HEMT, circuit topologies for improving large signal performance in wideband from lower frequency can be employed, and the MMIC shows input 1 dB compression point (IP1dB) of more than +40 dBm and input 3rd order intercept point (IIP3) of more than +55 dBm.**

Keywords—ATE, MMICs, GaN HEMTs, step attenuators

I. Introduction

For measurement instruments including radio frequency automated test equipment (RF ATE) systems, digital step attenuators have an essential role to maximize their dynamic ranges. High attenuation accuracy and fast settling time are very important to the digital step attenuator for RF ATE systems because of accomplishing higher RF test throughput. Moreover, with the increase in output power level and modulation bandwidth for a test of RF integrated circuits (RFICs), higher power handling capability and linearity are also demanded. Thus, a gallium nitride high electron mobility transistor (GaN HEMT) is one of suitable devices to realize the digital step attenuator monolithic microwave integrated circuit (MMIC), because it exhibits higher settling time, higher power handling capability and lower distortion characteristic. However, a conventional GaN HEMT using silicon nitride (SiN) passivation films has large gate leakage current [1] – [3]. Hence, large signal performance for the RF ATE cannot be satisfied because a circuit topology using large gate isolation resistor, as described in next section, cannot be employed. In order to solve this problem, we developed a very low gate leakage current Schottky GaN HEMT based on tantalum oxy nitride (TaON) passivation technology instead of conventional SiN passivation [4], [5].

In this paper, a 10 MHz - 6 GHz high power high linearity 35 dB digital step attenuator MMIC for RF ATE using the Schottky GaN HEMTs with TaON passivation technology is described. The MMIC shows fast settling time, high input 1 dB compression point (IP1dB) and high input 3rd order intercept point (IIP3).

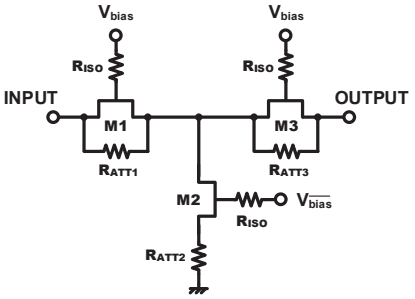

Fig. 1. Schematic of the T-type attenuator cell.

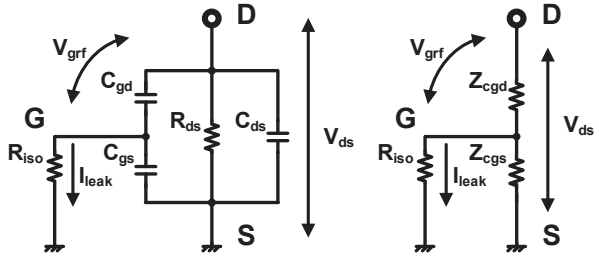

Fig. 2. Equivalent circuits for the shunt FET in the off state. (a) RF equivalent circuit. (b) Simplified equivalent circuit.

II. Improvement in Large Signal Performance

A T-type attenuator cell configuration that is one of typical attenuator cells is shown in Fig. 1. For the configurations, a major factor in degradation of the large signal performance is a shunt FET, because the shunt FET cannot maintain the off state when input RF signal becomes larger. Fig. 2-(a) shows an RF equivalent circuit for the shunt FET in the off state and Fig. 2-(b) shows a simplified schematic of Fig. 2-(a) by neglecting R_{ds} and C_{ds} in the off state. In Fig. 1, the shunt FET M2 needs to maintain the off state when the attenuator cell is through state. Thus, the shunt FET in the off state requires $V_{gs} < V_{th}$,and V_{gs} can be expressed as

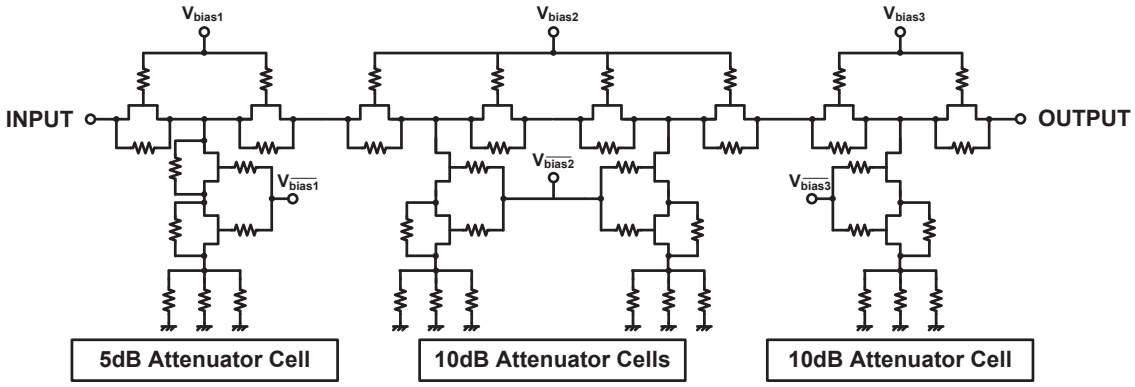

Fig. 3. Schematic of the 35 dB digital step attenuator.

$$V_{gs} = V_{bias} + I_{leak} \times R_{iso} + V_{grf} \quad (1)$$

$$V_{grf} = V_{ds} \times \frac{Z_{cgd}}{Z_{cgd} + Z_{cgs} // R_{iso}} \quad (2)$$

$$Z_{cgd} = 1 / j\omega C_{gd} \quad (3)$$

$$Z_{cgs} = 1 / j\omega C_{gs} \quad (4)$$

where V_{bias} is a DC voltage applied by a bias circuit, I_{leak} is a gate leakage current, R_{iso} is a gate isolation resistor and V_{grf} is a RF voltage applied to C_{gd}. V_{ds} is a RF voltage applied between a symbol D and a symbol S shown in Fig. 2. As expressed in (1), it can be found that V_{gs} exceeds V_{th} when V_{grf} becomes larger. Thus, the shunt FET in the off state transits to the on state, and the large signal performance degrades.

From the above description, V_{grf} must be decreased in order to improve the large signal performance. Thus, on the basis of (2), the shunt FET is stacked [6] and large gate isolation resistor is used for decreasing V_{grf} in wideband from lower frequency. However, as expressed in (1), the large R_{iso} causes large voltage drop by I_{leak}. Hence, we developed a novel Schottky GaN HEMT based on TaON passivation technology that is characterized in very low gate leakage current [4], [5]. Using the HEMT, large voltage drop caused by large R_{iso} can be avoided. Therefore, the developed HEMT enables to employ the large gate isolation resistor, and the large signal performance for the attenuator cell can be substantially improved in wideband.

III. Device Design and Characteristics

In order to reduce the gate leakage current, we employ TaON [4] as the passivation films instead of conventional SiN [1]-[3]. The TaON films are deposited by RF magnetron sputtering with no damage to the sheet resistance for fast settling time [5].

The n-GaN/AlGaN/GaN HEMT structure is grown on a SiC substrate by metal organic vapor phase epitaxy (MOVPE). The Schottky GaN HEMT has a gate length of 0.5 μm, a source-gate spacing of 1 μm, and a drain-gate spacing of 1 μm.

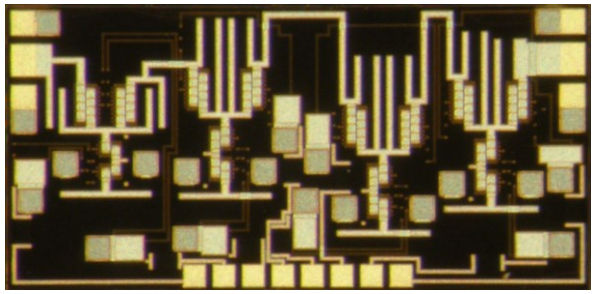

Fig. 4. Photograph of the fabricated MMIC.

Typical characteristics of the fabricated HEMT exhibit a saturation current I_{dss} of 0.6 A/mm, a threshold voltage of −3 V and a breakdown voltage of more than 50 V. The HEMT exhibits the gate leakage current of less than 10 nA/mm up to the gate voltage of −50 V that is considerably low leakage current compared with HEMT using SiN. The epitaxial resistor is used as the gate isolation resistor, and the thin film resistor with Ni/Cr is used as the attenuation resistor. The through substrate via is fabricated in the 100 μm thinned substrate.

IV. Circuit Design

The circuit schematic is shown in Fig. 3. The digital step attenuator consists of 4 stage cascade connection using one 5 dB attenuator cell and three 10 dB attenuator cells. Thus, the maximum attenuation ratio is 35 dB with 5 dB step. A stacked FET for the shunt FET and large gate isolation resistor that is more than 300 KΩ are used for improving the large signal performance. Fig. 4 shows a fabricated bare chip photograph. The die size is 2.4 mm × 1.8 mm.

V. Measurement Results

The digital step attenuator MMIC is measured in bare chip form. The control voltage V_{bias} corresponding to on and off states is set to 0 V and -15 V, respectively. Fig. 5 shows measured return loss and insertion loss in through state. Both input and output return losses in through state are better than 14 dB, and both the input and output return losses in attenuation state from 5 dB to 35 dB are also better than 14 dB. The insertion loss is lower than 2.7 dB up to 6 GHz. Measured attenuation accuracy for each state is shown in Fig. 6. The

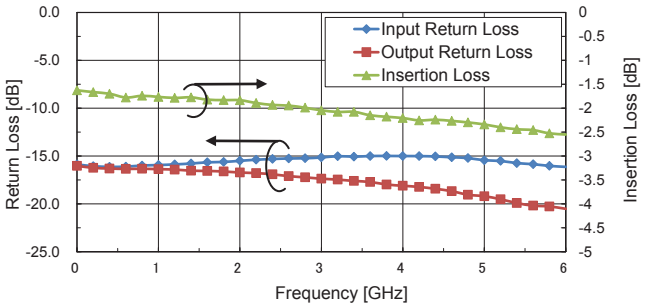

Fig. 5. Measured return and insertion losses in thru state.

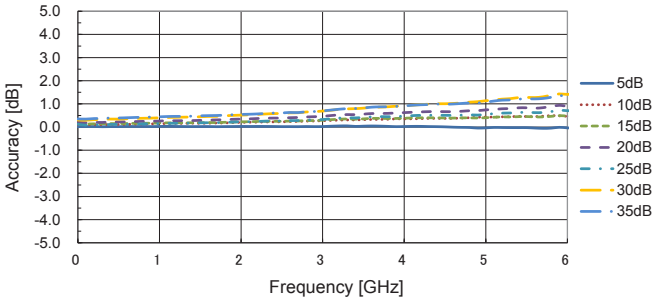

Fig. 6. Measured attenuation accuracy for each state.

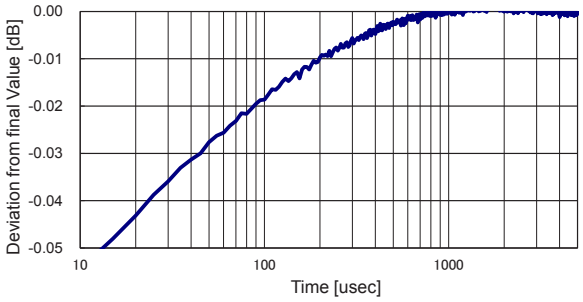

Fig. 7. Measured settling time for state transition.

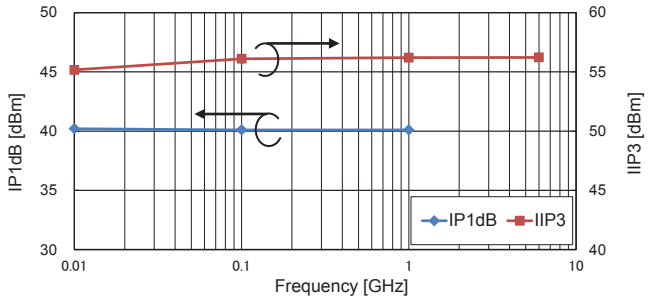

Fig. 8. Frequency responses of measured IIP3 and IP1dB.

attenuation accuracy of less than 2 dB across 10 MHz to 6 GHz is achieved. Fig. 7 shows measured settling time for state transition from attenuation state to through state. The settling time is less than 50 µs within 0.05 dB that satisfies with the RF ATE requirement for higher test throughput [7], [8]. The frequency responses of measured IP1dB and IIP3 are shown in Fig. 8. The IP1dB was measured across 10 MHz to 1 GHz and the IIP3 was measured across 10 MHz to 6 GHz. As results, the IP1dB is more than +40 dBm and the IIP3 is more than +55 dBm.

VI. Conclution

The 10 MHz - 6 GHz high power high linearity 35 dB digital step attenuator MMIC for RF ATE using the novel GaN HEMTs with TaON passivation has been developed. Owing to the very low leakage current characteristic of the developed HEMT, the large signal performance for the digital step attenuator can be substantially improved in wideband from lower frequency. The fabricated digital step attenuator shows the return loss of better than 14 dB, the insertion loss of less than 2.7 dB and the attenuation accuracy of less than 2 dB up to 6 GHz. The fast settling time of less than 50 µs within 0.05 dB is obtained. The digital step attenuator has the superior large signal performance, and the IP1dB and the IIP3 are more than +40 dBm and +55 dBm, respectively. These measured results can be satisfied with the RF ATE requirements.

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