A 60-GHz Low-Power Active Phase Shifter With Impedance-Invariant Vector Modulation in 65-nm CMOS

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***Abstract*— This study presents the design and analysis of a 60-GHz low-power active vector-sum phase shifter with 5-bit phase resolution. An impedance-invariant variable gain amplifier (VGA) is proposed and applied to the vector modulator. The proposed VGA not only demonstrates low phase and impedance variations during gain control but also high linearity under low supply voltage. Moreover, it reduces the gain/phase error in vector modulation. In addition, the transformer-based current-reuse technique is adopted to enhance the gain of the phased array channel while consuming low dc power. The prototype circuit implemented in 65-nm CMOS technology consumes only 5 mW of dc power and occupies an area of 0.3 mm^2 (excluding pads). The measurement results of the prototype circuit reveal that the proposed phase shifter achieves an average gain of −3.8 dB (including a 2-dB loss of the measurement balun), an rms gain error of 0.25–0.72 dB, and an rms phase error of 3°–7° in the 3-dB bandwidth from 51 to 66.3 GHz. The measured input 1-dB compression point is observed to be higher than −1.1 dBm at 60 GHz.**

***Index Terms*— CMOS, current-reuse technique, impedance invariant, millimeter wave (mm-wave), phased array, phase shifter, 60 GHz, variable gain amplifier (VGA), vector modulation, vector-sum phase shifter (VSPS).**

I. Introduction

RECENTLY, the demand for high-data-rate wireless communication, in technologies such as wireless 4K streaming and wireless virtual reality head-mounted displays (VR HMDs), has been increasing. Wireless communication using the 60-GHz unlicensed band can realize data rates of tens of Gb/s due to its wide bandwidth. For this reason, 60-GHz band transceivers with multiple tens of Gb/s over short distances have been researched [1]–[3]. However, due to significant path loss, the communication distance of 60-GHz radio is severely limited. This issue can be overcome by the use of the phased array technique that supports electrical beam steering in a 60-GHz wireless transceiver because the technique improves the effective isotropic radiated power (EIRP) of the transmitter and signal-to-noise ratio (SNR) of the receiver [4].

An RF phase shifter is one of the most important building blocks for realizing an RF beamforming system, and it can be implemented with either a passive or an active structure. A passive phase shifter is typically implemented as a switched filter type [5]–[11] or reflective type [12]–[14], which shows good linearity and nearly 0-mW dc power consumption. However, it exhibits a high insertion loss. In contrast, an active phase shifter, typically implemented with a vector-sum structure [15]–[25], not only exhibits low insertion loss and a compact circuit size but also easily achieves high resolution and simple calibration. For these reasons, an active vector-sum phase shifter (VSPS) is more suitable for a high-performance integrated phased array system. However, an active VSPS has a large dc power consumption with limited gain and linearity. These disadvantages need to be overcome because they increase the power consumption of the phased array receiver and degrade the power efficiency and linearity of the phased-array transmitter.

In this study, we propose a low-power VSPS with an impedance-invariant variable gain amplifier (IIVGA) and a transformer-based current-reuse technique. Analysis of the vector modulator (VM) reveals that the proposed IIVGA minimizes the phase and impedance variations during gain control, which in turn reduces the gain/phase error of the VSPS. Moreover, the IIVGA demonstrates better linearity than that of the conventional VM structures. The transformer-based current-reuse technique at the VM enhances the gain and hence reduces the dc power consumption of each channel in the phased-array system. It is worth noting that the proposed IIVGA can be used not only for VM of VSPS but also for other phase-invariant gain control applications.

The remainder of this article is organized as follows. In Section II, the impedance-invariant vector modulation technique is presented and analyzed. A detailed circuit implementation and its measurement results are described and discussed in Section III and Section IV, respectively. Finally, the conclusions are presented in Section V.

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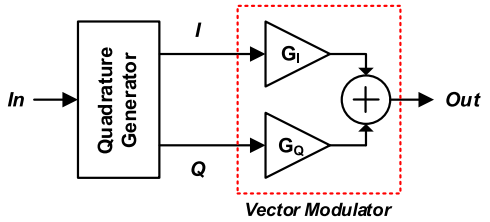


Fig. 1. Block diagram of a conventional VSPS.

II. Impedance-Invariant Vector Modulation

As shown in Fig. 1, the VSPS is typically composed of a quadrature generator and a VM. The quadrature generator produces two signals called the I and Q signals with a phase difference of 90°. The VM performs two operations: 1) it modulates the I and Q signals by the gain weights of G_I and G_Q, respectively, and 2) it synthesizes the desired phase by combining the two modulated signals. In addition, as the VM is located at the end in this configuration, it has a crucial effect on the linearity of the entire VSPS. Therefore, for designing a low-error VSPS with high linearity, a VM with high accuracy and linearity is required. In this section, we will discuss several reported VM structures and their limitations. Then, an improved VM structure is proposed.

A. Reported VM Structures

Fig. 2 shows three reported VM topologies in the 60-GHz band. The Gilbert cell structure [15], [17], [18], [20] in Fig. 2(a) is one of the most popular topologies, even in the millimeter-wave (mm-wave) regime. This structure controls the gain by adjusting the bias current through the current source of the first stack from the bottom and reverses the phase by switching the current source of the second stack. The use of multiple transistor stacks, which limit linearity under limited supply voltage or cause large power consumption under high supply voltage, is one of the drawbacks of this structure.

The cascode current-steering structure [16], [22], [24], [25] in Fig. 2(b) is another classical VM topology. It adjusts the gain by diverting the current along the dummy path. This method enables almost constant input impedance, but a certain amount of current is always discarded when the vector is modulated. Thus, it is not suitable for low-power structures.

To overcome the drawback of the Gilbert cell structure, as shown in Fig. 2(c), Song *et al.* [19] eliminated the use of differential structure and current sources and used VGA with a simple single-ended common source (CS) structure as the VM. In this structure, the gain is controlled by adjusting the gate bias, and the sum of the currents flowing in the I and Q paths is always kept constant. Unlike the Gilbert cell and cascode current-steering structures, this structure requires only one transistor stack.

A common feature of these VM structures is that they control the gain by adjusting the bias current. This bias current control scheme has two disadvantages. First, as the operating point of the transistor varies with the bias current, a parasitic capacitance variation occurs. This not only causes variations in the input and output impedances (except the input impedance of the current-steering structure) but also phase variation during gain control. Variations in the input impedance affect the quadrature generator, resulting in additional gain/phase error, where phase variation degrades the accuracy of vector modulation. Therefore, for precise phase synthesis, both impedance and phase variation should be minimized during gain control. Second, at low gain, the bias current in the signal path is reduced, limiting the linearity of the amplifier. As a result, the compression point can be varied considerably depending on the phase states in the VSPS in which the VM with the bias current control scheme is used.

B. Proposed Vector Modulation Technique

We propose the IIVGA to overcome the aforementioned issues, as shown in Fig. 3. The proposed IIVGA applies three techniques to eliminate impedance and phase variations during gain control.

First, to remove transistor parameter variation except g_m with the bias point, the transistor width is digitally controlled instead of the bias current, for the purpose of gain control. To this end, one large transistor is divided into N unit transistors to form a digitally controlled transistor array, as shown in Fig. 3(a) [16], [37], [38]. Thus, the transistor size can be adjusted simply by each unit transistor being turned on and off. In this scheme, the operating point of the ON-state transistor is kept constant during gain control.

Second, the signal path is divided into two paths, and the unit transistors of the transistor array located in the two paths are digitally controlled by an inverter and turned on and off in a complementary manner. Therefore, for all gain states, the effective width of the ON (or OFF) state transistor located at the input node is always kept constant. For example, as shown in Fig. 3(b), assuming that there are N_1 ON-state transistors in one path and N_2 ON-state transistors in the other path, the sum of N_1 and N_2 is always kept constant. For convenience, the path where N_1 transistors are turned on is called the N_1-path. In this configuration, the input impedance and the dc current remain constant for all gain states.

Third, the positive and negative signals are cross-coupled, as shown in Fig. 3(c), to finally complete the proposed IIVGA structure. This keeps both the input and output impedance constant during gain control and helps to achieve a wider gain control range. In IIVGA, there are N ON-state and OFF-state transistors at the input and output nodes, regardless of the gain state. Thus, the input and output impedances are kept constant for all gain states. In addition, by cross-coupling the N_1-path and the N_2-path with opposite phase, the gain is rendered proportional to the difference between N_1 and N_2. Moreover, a combination of these techniques eliminates phase variation during gain control and neutralizes the parasitic capacitance between the input and output nodes. These effects can be observed through small-signal analysis.

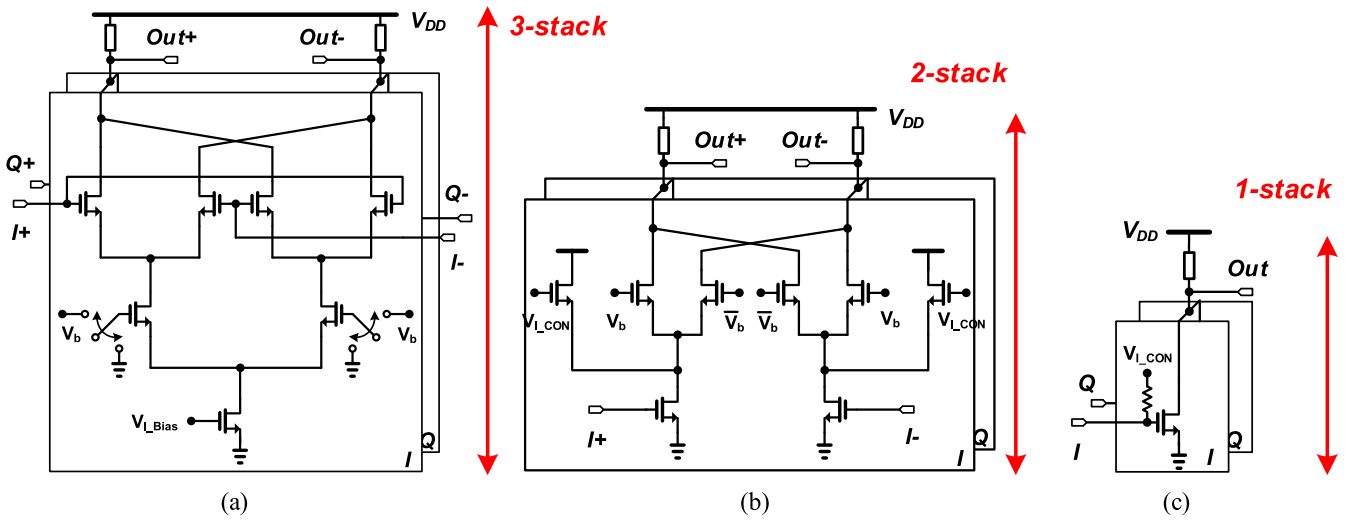


Fig. 2. (a) Gilbert cell-based VM. (b) Cascode current-steering VM. (c) Vector adder in [19].

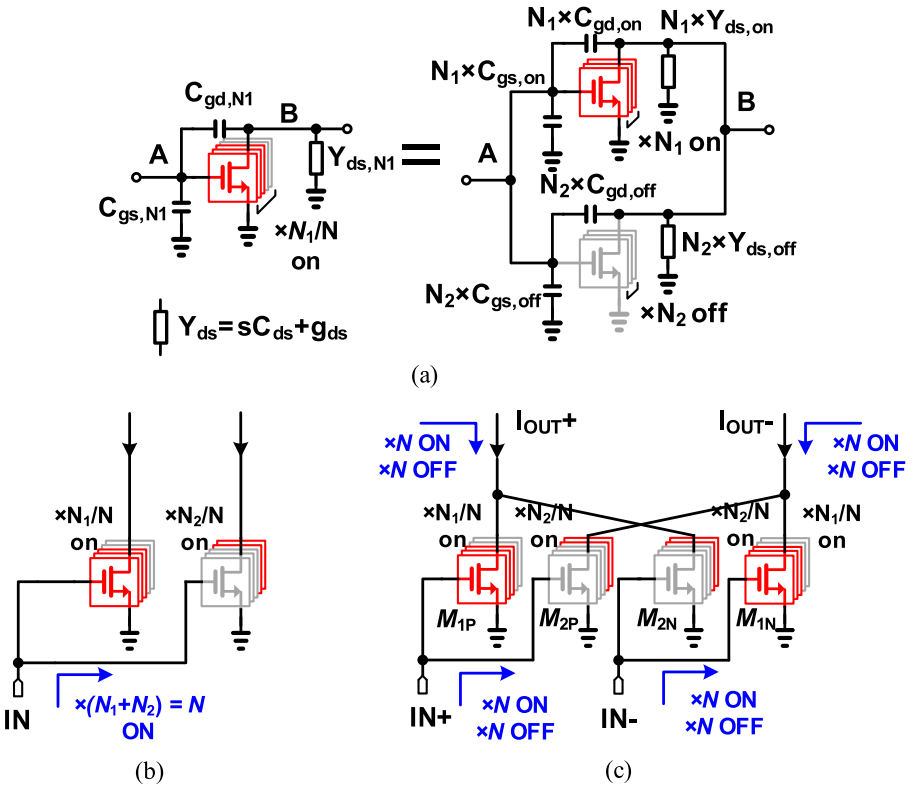


Fig. 3. (a) Digitally controlled transistor array with N_1 ON-state transistors. (b) Two signal paths consisting of complementary ON and OFF digitally controlled transistor arrays. (c) Simplified block diagram of proposed IIVGA.

C. Small-Signal Analysis of IIVGA

To analyze the small-signal characteristic of the IIVGA, it is necessary to investigate the effective transistor parameters of the digitally controlled transistor array. For simplicity, in this study, rather than writing drain–source capacitance C_{ds} and drain–source resistance g_{ds} separately, we express them as the combined admittance Y_{ds} defined as $sC_{ds} + g_{ds}$. As shown in Fig. 3(a), the digitally controlled transistor array in the N_1-path consists of N_1 ON-state transistors and N_2 OFF-state transistors. Therefore, the parasitic elements of the digitally controlled transistor located in the N_1-path are expressed as follows:

$$C_{gs,N1} = N_1 \times C_{gs,ON} + N_2 \times C_{gs,OFF} \quad (1)$$

$$C_{gd,N1} = N_1 \times C_{gd,ON} + N_2 \times C_{gd,OFF} \quad (2)$$

$$Y_{ds,N1} = N_1 \times Y_{ds,ON} + N_2 \times Y_{ds,OFF} \quad (3)$$

where $C_{gs,ON}$, $C_{gs,OFF}$, $C_{gd,ON}$, $C_{gd,ON}$, $Y_{ds,ON}$, and $Y_{ds,OFF}$ are the ON-state C_{gs}, OFF-state C_{gs}, ON-state C_{gd}, OFF-state C_{gd}, ON-state Y_{ds}, and OFF-state Y_{ds} of unit transistor, respectively.

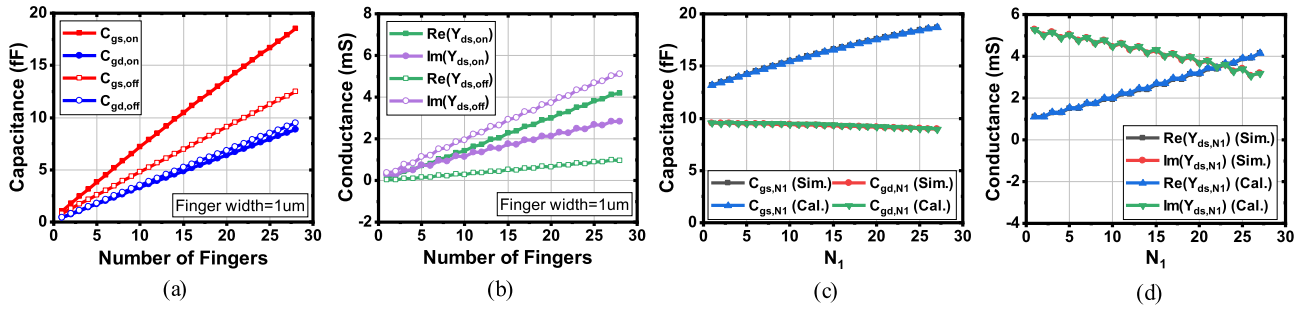


Fig. 4. (a) C_{gs} and C_{gd} on transistor width. (b) Y_{ds} depending on transistor width. (c) Calculated and simulated $C_{gs,N1}$ and $C_{gd,N1}$ in a digitally controlled transistor array. (d) Calculated and simulated $Y_{ds,N1}$ in a digitally controlled transistor array.

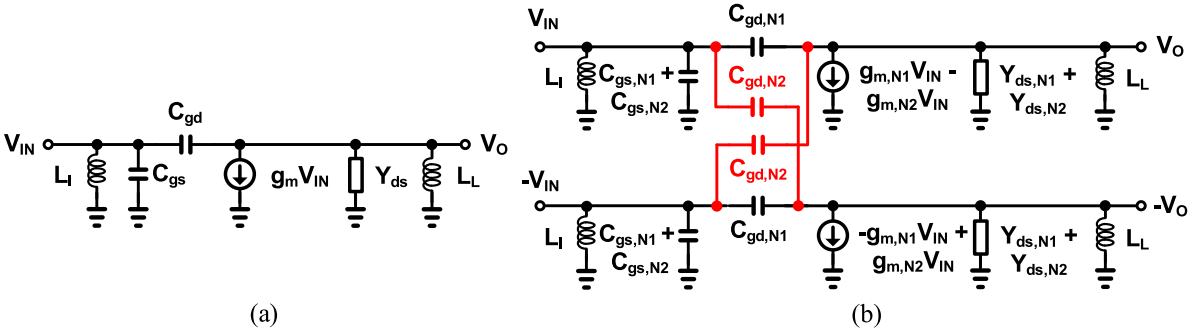


Fig. 5. Simplified small-signal equivalent circuit of (a) conventional CS structure and (b) proposed IIVGA.

The simulation results of C_{gs}, C_{gd}, and Y_{ds} according to the width of the RF nMOS are shown in Fig. 4(a) and (b). These transistor parameters were calculated from the Y-parameters [32]. Through (1)–(3), the effective transistor parameters $C_{gs,N1}$, $C_{gd,N1}$, and $Y_{ds,N1}$ of a digitally controlled transistor array with a size of N_1 can be calculated. A comparison of the calculated $C_{gs,N1}$, $C_{gd,N1}$, and $Y_{ds,N1}$ values and the corresponding values obtained through the simulation are shown in Fig. 4(c) and (d). The simulations were conducted with a unit transistor size of 1 μm while maintaining $N_1 + N_2$ at 28. As there is no difference between the calculated and simulated values, it is indicated that a digitally controlled transistor array can be analyzed by the small-signal model in Fig. 3(a) and (1)–(3).

Fig. 5(a) and (b) shows the simplified small-signal equivalent circuit of the CS amplifier and the proposed IIVGA, respectively. The gain of the CS amplifier is expressed as

$$A_{v,\mathrm{CS}} = -\frac{\overbrace{(g_m - \mathrm{s}C_{\mathrm{gd}})}^{\text{complex } G_m}}{sC_{\mathrm{gd}} + sC_{\mathrm{ds}} + g_{\mathrm{ds}} + \frac{1}{sL_L}} \tag{4}$$

where L_L represents the load inductance. It can be seen from (4) that the CS amplifier has a complex G_m value of $g_m - \mathrm{s}C_{\mathrm{gd}}$ because of the gate–drain capacitance effect in the CS amplifier. This complex G_m causes phase variation during gain control. As the change in the parasitic component with the bias current is not large, the phase variation according to the gain state change $\Delta\varphi$ is expressed as

$$\Delta\varphi \approx \tan^{-1}\left(-\frac{\omega C_{\mathrm{gd}}}{\Delta g_m}\right) \tag{5}$$

where Δg_m represents the g_m variation. As (5) suggests, to eliminate the phase variation that occurs during gain control in the CS amplifier, the imaginary part of the numerator should disappear to have a real G_m value.

By means of using the Miller theorem, the input admittance of the CS amplifier is given by

$$Y_{\mathrm{in,CS}} = \frac{1}{sL_I} + sC_{\mathrm{gs}} + [1 + A_{v,\mathrm{CS}}(\omega)]sC_{\mathrm{gd}}. \tag{6}$$

Adjusting the bias current to control the gain changes both the gain and the C_{gs} value. Because C_{gd} does not vary considerably with the bias current, the change in input admittance according to the gain state is expressed as

$$\Delta Y_{\mathrm{in}} \approx s(\Delta C_{\mathrm{gs}}) + \Delta A_{v,\mathrm{CS}} sC_{\mathrm{gd}}. \tag{7}$$

Therefore, the input impedance of the CS amplifier varies depending on the gain states. In contrast, in the case of IIVGA, as shown in Fig. 5(b), $C_{gd,N2}$ is cross coupled between the opposite phases. The graph in Fig. 4(a) suggests that the C_{gd} values of the ON-state and OFF-state transistors are almost equal. Therefore, it can be expressed as

$$C_{\mathrm{gd},N1} \cong C_{\mathrm{gd},N2}. \tag{8}$$

Therefore, $C_{gd,N1}$ is neutralized by $C_{gd,N2}$ for all gain states, indicating that IIVGA has better stability and reverse isolation compared with the conventional CS structure.

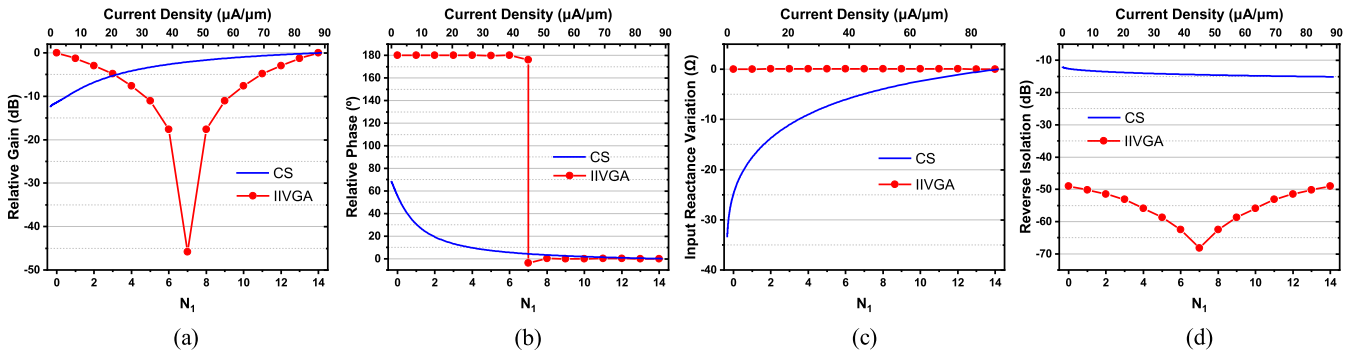


Fig. 6. Simulated (a) relative gain (or gain variation), (b) relative phase (or phase variation), (c) input impedance variation, and (d) reverse isolation.

The small-signal circuit shown in Fig. 5(b) and (1)–(3) and (8) is used to derive the gain of IIVGA as

$$A_{v,II} = \frac{-(g_{m,N1} - g_{m,N2} + sC_{\mathrm{gd},N2} - sC_{\mathrm{gd},N1})}{sC_{\mathrm{gd},N1} + sC_{\mathrm{gd},N2} + Y_{\mathrm{ds},N1} + Y_{\mathrm{ds},N2} + \frac{1}{sL_L}} \approx \frac{-(N_1 - N_2)g_{m0}}{D} \tag{9}$$

$$D = (N_1 + N_2)(sC_{\mathrm{gd,ON}} + sC_{\mathrm{gd,OFF}} + sC_{\mathrm{ds,ON}} + sC_{\mathrm{ds,OFF}} + g_{\mathrm{ds,ON}} + g_{\mathrm{ds,OFF}}) + \frac{1}{sL_L} \tag{10}$$

where g_{mN1}, g_{mN2}, and g_{m0} are the transconductances of the N_1-path, N_2-path, and unit transistor, respectively. As expected, the gain of the IIVGA is determined only by the difference between the number of ON-state transistors in the N_1-path and N_2-path. Equation (9) indicates that unlike (4), the proposed IIVGA does not contain complex terms in the numerator and (10) is a constant regardless of the gain state so that no phase variation will occur during gain control. In addition, the IIVGA has a positive gain when $N_1 > N_2$, a negative gain when $N_1 < N_2$, and ideally a zero gain when $N_1 = N_2$.

Similarly, the input admittance of the IIVGA is derived as

$$Y_{\mathrm{in,II}} \approx (N_1 + N_2)(sC_{\mathrm{gs,ON}} + sC_{\mathrm{gs,OFF}} + sC_{\mathrm{gd,ON}} + sC_{\mathrm{gd,OFF}}) + \frac{1}{sL_1}. \tag{11}$$

If the sum of N_1 and N_2 is considered to be constant, then (11) indicates that the input impedance of IIVGA is approximately constant regardless of the gain state.

Fig. 6 shows the simulated relative gain, relative phase, input reactance variation, and reverse isolation for the single-ended CS VGA and the proposed IIVGA according to the gain state. The CS VGA used a 14-μm transistor and variable gain was achieved by adjusting the bias current with the gate voltage. The proposed IIVGA uses a 4-bit transistor array composed of 1, 2, 4, and 7 μm transistors to control the total size of a 14-μm transistor. Here, the electromagnetic (EM) simulation was reflected in this simulation, thereby also reflecting the effect of layout-dependent parasitic components by the additional feeding line in the 4-bit transistor array. This layout-dependent parasitic effect leads to a gain degradation of up to 1.7 dB compared with the CS VGA. In the simulation, the two structures were biased to have the same current density at the highest gain state.

Fig. 6(a) shows the simulated relative gain at 60 GHz. The IIVGA shows approximately 46 dB of gain control range. In contrast, the CS structure shows approximately 12.5 dB of limited gain control range. From (9), the IIVGA gain is zero for $N_1 = N_2$. Hence, it should ideally have an infinite gain control range but is restricted to 46 dB due to the layout-dependent parasitic components.

Fig. 6(b) shows the simulated relative phase of the two structures at 60 GHz. The CS structure showed a 68.6° phase variation. Conversely, IIVGA showed a phase variation of less than 3.7° in both the phase inversion and the noninversion state. In particular, except for the lowest gain state, only phase variations of less than 0.2° were observed.

Fig. 6(c) shows the simulated input reactance of the two structures at 60 GHz. In IIVGA, the input reactance is constant with gain because there is no capacitance variation. In the CS structure, a large impedance variation of approximately 33 Ω was observed in the imaginary part.

Fig. 6(d) shows the simulated reverse isolation of the two structures at 60 GHz. The proposed IIVGA shows less than −49 dB reverse isolation for all gain states, but the CS structure shows reverse isolation of −15 dB. This is because the gate–drain capacitance is neutralized for all gain states, as can be seen from (8). These simulation results indicate that the proposed IIVGA not only has a wider gain control range than the conventional CS structure but also has a significantly low phase and impedance variation and better reverse isolation.

D. Comparison to Gilbert Cell Structure

To explore how the improvements in the IIVGA affect the accuracy and linearity of VM, vector synthesis simulations of 11.25° resolution were performed for IIVGA. We also performed the same simulation on Gilbert cell structures, which are widely used in the VSPS design, to compare the vector modulation performance. We exclusively simulated the phase states of one quadrant (0–90 states) because the remaining quadrants can be achieved by inverting the phase of the I or Q signal, thus leading to duplicate results. In this simulation, we used ideal components to create the quadrature signal by a transformer-based quadrature coupler and to match both the IIVGA and Gilbert cell structures to 50 Ω. The total

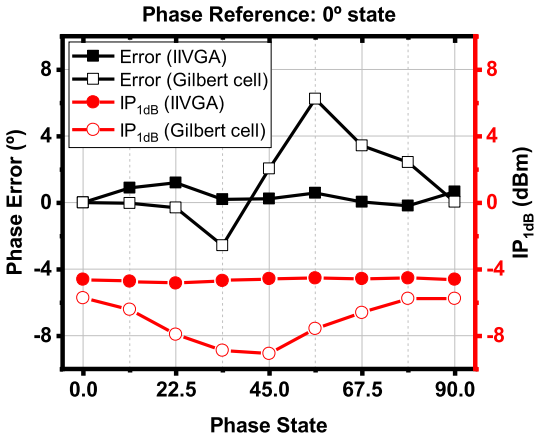


Fig. 7. Vector synthesis simulation for IIVGA and Gilbert cell structure: phase error and input $P_{1\,\mathrm{dB}}$ according to the phase state.

current consumption of the IIVGA-based VM and Gilbert cell was matched, and the supply voltages were set to 0.5 and 1.5 V, respectively.

Fig. 7 shows the simulation results of the phase error and input $P_{1\,\mathrm{dB}}$ according to the phase state. The IIVGA-based VM has a phase error of less than 1.2° for a phase state from 0° to 90°, mainly due to quantization error caused by digital control through transistor size. In contrast, for the Gilbert cell, a phase error of up to 6.2° occurs, especially in the phase state of 33.75° to 78.75°. As previously mentioned, this is due to two reasons: 1) phase variation during gain control and 2) input impedance variation during gain control. This is because the difference between the $x°$ phase state and the 90-$x°$ phase state indicates that only the bias currents of the I and Q paths are interchanged. Therefore, the only factor that can cause phase error is a non-ideality occurring in the VM.

According to the simulation results of the input $P_{1\,\mathrm{dB}}$, IIVGA-based VM indicates a nearly constant $\mathrm{IP}_{1\,\mathrm{dB}}$ depending on the phase state. In contrast, the Gilbert cell structure represents different values of $\mathrm{IP}_{1\,\mathrm{dB}}$ depending on the phase state. Moreover, although the supply voltage of the Gilbert cell is three times higher than that of IIVGA-based VM, the Gilbert cell structure presents −5.75 dBm of maximum $\mathrm{IP}_{1\,\mathrm{dB}}$, whereas the IIVGA-based VM shows −4.84 dBm of minimum $\mathrm{IP}_{1\,\mathrm{dB}}$. This can be explained as follows.

Fig. 8 shows the IIVGA-based VM and the Gilbert cell VM (in the 0° and 45° phase states) under the same dc current condition. As mentioned earlier, if the IIVGA consists of transistor arrays of N unit transistors, there are always N ON- and OFF-state transistors at the output for all gain states. Thus, considering both the I-path and the Q-path, there are always $2N$ ON- and OFF-state transistors for all phase states in the VM. As the I-path and Q-path consist of transistor arrays that operate at the same current density while consuming constant dc current for all phase states, the IIVGA-based VM shows a constant $\mathrm{IP}_{1\,\mathrm{dB}}$ for all phase states.

In the case of the Gilbert cell VM, each transistor size would be of the order of $2N$ to consume the same dc current under the same bias condition, as shown in Fig. 8(b). In the

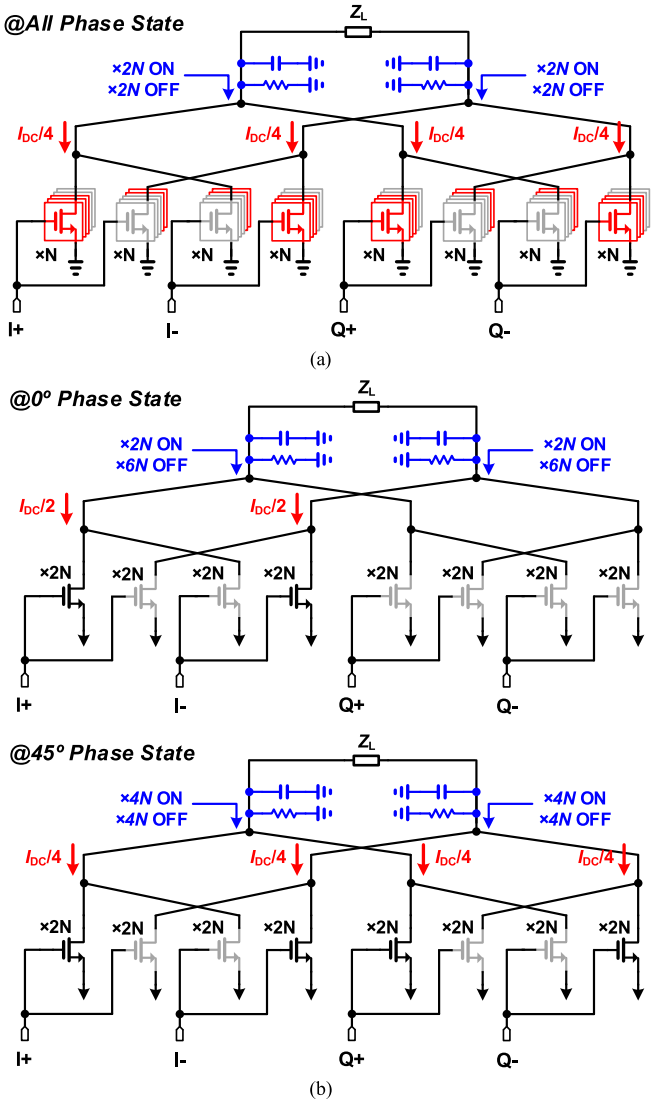
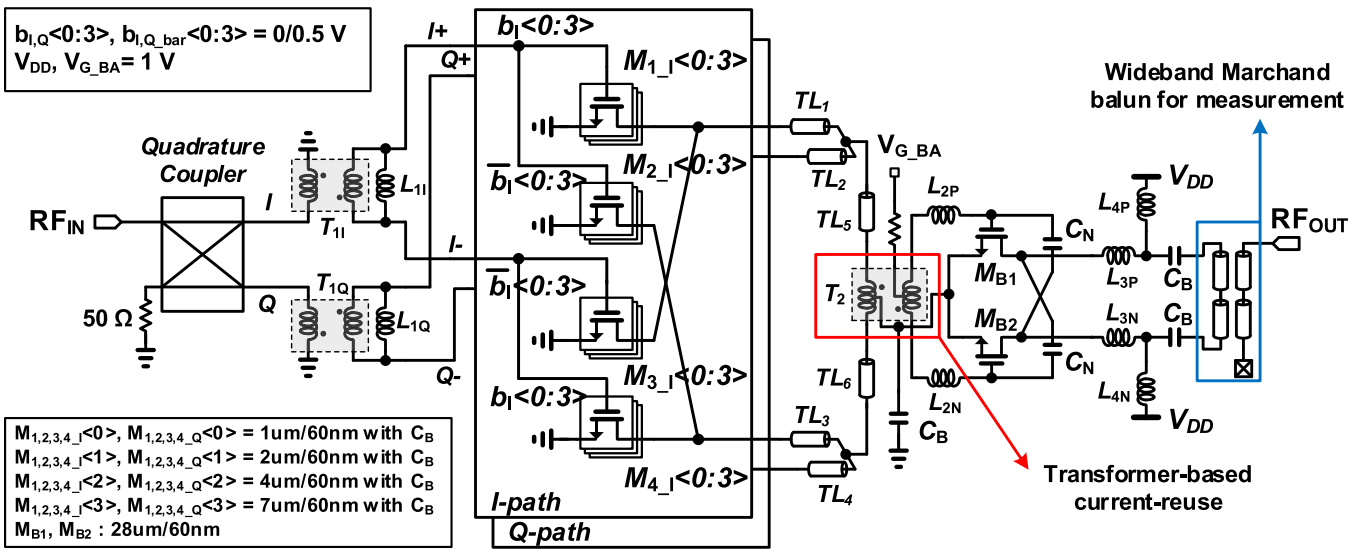


Fig. 8. Leakage power generated by the OFF-state transistor at the output node. (a) IIVGA and (b) Gilbert cell (at 0° and 45° phase state).

0° phase state, only one pair of transistors operates in the saturation region, and the remaining transistors are turned off. Thus, an equivalent size of $2N$ ON-state transistors and $6N$ OFF-state transistors exists for each differential signal. The ON-state transistors operate with the same current density as IIVGA-based VM, but the equivalent size of the OFF-state transistor is larger than that of the IIVGA-based VM. The OFF-state transistor generates parasitic capacitance and resistance at the output node, resulting in leakage of power delivered to the load impedance Z_L. As a result, at the 0° phase state, the effective size of the OFF-state transistor is larger in the Gilbert cell VM, resulting in a larger leakage of power due to parasitic elements, resulting in a lower $\mathrm{IP}_{1\,\mathrm{dB}}$ than IIVGA-based VM. This is also the case for the 90° phase state. In the 45° phase state, there are a pair of ON-state and OFF-state transistors in the I-path and Q-path, respectively. Thus, an equivalent size of $4N$ ON-state transistors and $4N$ OFF-state transistors exists for each differential signal. However, the ON-state transistor pair operates biased by half the current density compared with



[Passive Elements Parameters]

T_{1I} , T_{1Q}	102 pH / 36 pH, k = 0.5	L_{4P} , L_{4N}	100 pH
T_2	38 pH / 34 pH, k = 0.63	$TL_{1\text{-}4}$	Z_0 = 50 Ω, L = 70 µm
L_{1I} , L_{1Q}	159 pH	$TL_{5\text{-}6}$	Z_0 = 50 Ω, L = 70 µm
L_{2P} , L_{2N}	120 pH	C_N	10 fF
L_{3P} , L_{3N}	76 pH	C_B	366 fF

Fig. 9. Schematic of the proposed VSPS.

IIVGA-based VM or 0° phase-state Gilbert cell VM. As a result, Gilbert cell VM shows the lowest $IP_{1\,dB}$ at 45° phase state because both I-path and Q-path ON-state transistor pairs operate with low current density. The remaining phase states can be described similarly, and consequently, IIVGA-based VM shows better linearity compared with Gilbert cell VM for all phase states.

In summary, the IIVGA-based VM presents the following advantages: 1) it minimizes phase errors by eliminating impedance and phase variation during vector modulation; 2) it exhibits superior linearity compared with conventional structures that control gain through bias current; 3) it can operate under a low supply voltage, reducing dc power consumption, because it consists of a single transistor stack; and 4) as the IIVGA has a wide gain control range of approximately 50 dB, the VM can be configured as a single stage. Due to these advantages, the IIVGA-based VM achieves high linearity with low power while performing accurate vector modulation.

III. Circuit Implementation

Fig. 9 shows the VSPS schematic. The proposed VSPS is composed of a quadrature coupler and an improved VM based on the IIVGA. The proposed VSPS is fabricated in a commercial 65-nm CMOS process.

A. Quadrature Generator

The quadrature generator is the most crucial block affecting the gain/phase error. Therefore, it is necessary to analyze how the errors generated during I and Q signal generation affect the gain/phase error of the entire VSPS. Let us assume that the I and Q signals generated by the quadrature generator are $A\angle 0°$ and $A\Delta A\angle(90+\theta)°$, respectively. ΔA (in linear scale) and θ (in degree scale) represent the amplitude and phase errors in the Q signal with respect to the I signal, respectively. The generated quadrature signals are input to the VM with gain weights of G_I and G_Q. Fig. 10(a)–(d) shows how ΔA (in decibel scale) and θ affect the maximum phase error, maximum gain error, rms phase error, and rms gain error, respectively, in a 5-bit VSPS. To guarantee n-bit phase resolution, the maximum phase error should be lesser than $360°/2^{n+1}$ to avoid any phase overlap between the different phase bits [17]. In a 5-bit phase shifter, the maximum phase error should be less than 5.625°. Therefore, to guarantee a 5-bit phase resolution, ΔA and θ should be placed inside the 5.625° contour in Fig. 10(a). Moreover, to avoid the use of an additional VGA to compensate for the gain variations between phase states, we aimed for a maximum gain error of less than 0.5 dB. To achieve such an error, ΔA and θ should be placed inside the 0.5 dB contour in Fig. 10(b). To satisfy these conditions, we aimed for ΔA less than ± 1 dB and θ less than $\pm 4°$ in this study. From Fig. 10(c) and (d), the rms phase and gain errors are calculated as less than 3.5° and 0.41 dB, respectively, with the target quadrature error and ideal vector modulation conditions.

Fig. 11 shows the quadrature generator of the proposed VSPS. The transformer-based quadrature coupler [18], [20], [23] is chosen in this design to generate quadrature signals

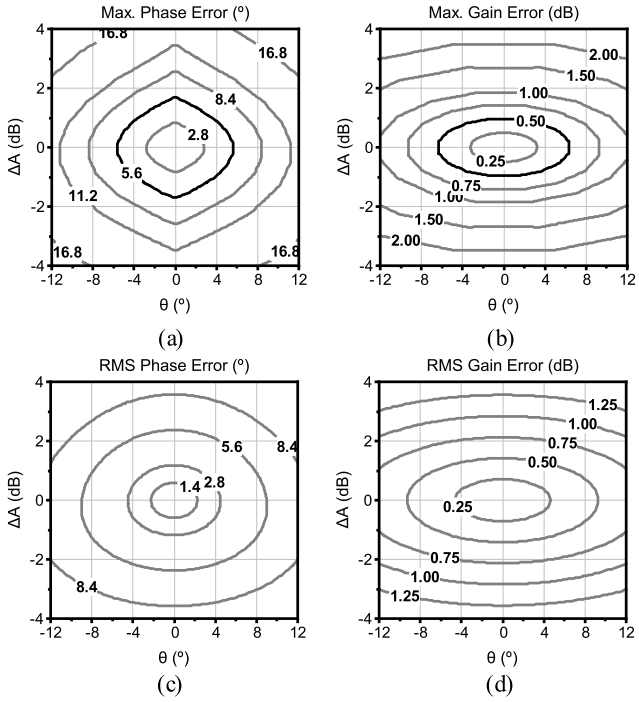


Fig. 10. Contours of phase/gain accuracy degradation of the overall 5-bit VSPS owing to ΔA and θ. (a) Calculated maximum phase error. (b) Calculated maximum gain error. (c) Calculated rms phase error. (d) Calculated rms gain error.

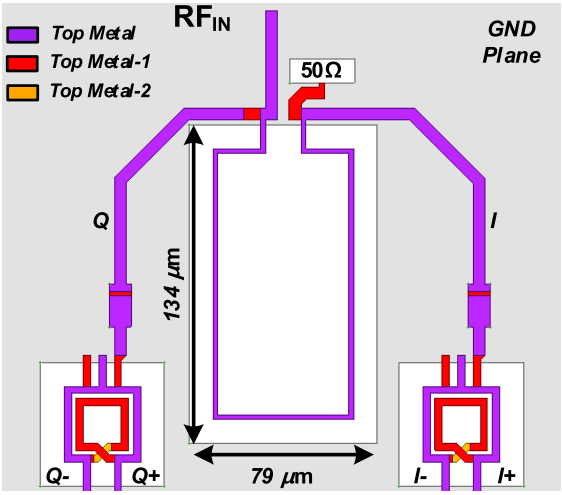


Fig. 11. Layout of quadrature generator of the proposed VSPS.

with low loss and compact circuit size. Fig. 12 shows the simulation results of the designed quadrature coupler. Both the I and Q paths have an insertion loss of −3.6 dB at 60 GHz with the amplitude and phase error of less than 0.61 dB and less than 0.3° in the 57–66-GHz band, respectively. Therefore, the designed coupler can sufficiently achieve a 5-bit phase resolution of less than 0.5 dB of the maximum gain error. After the quadrature coupler, as part of the input matching network of the VM, two transformers (for I and Q paths) with a 2:1 turns ratio is used to convert the single-ended signal into a differential signal.

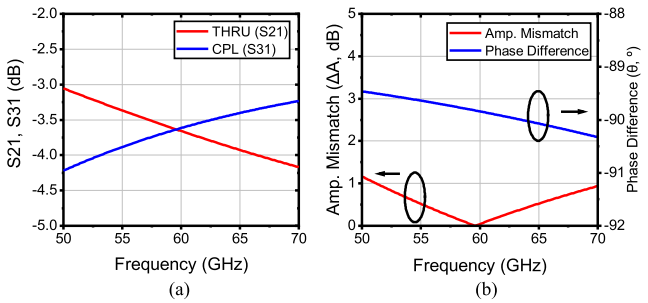


Fig. 12. Simulation results of the quadrature coupler. (a) Insertion loss. (b) Amplitude and phase mismatch.

	0	11.25	22.5	33.75	45	56.25	66.5	78.75	90
G_I	×14	×14	×14	×12	×10	×8	×6	×4	×0
G_Q	×0	×2	×6	×8	×10	×12	×14	×14	×14

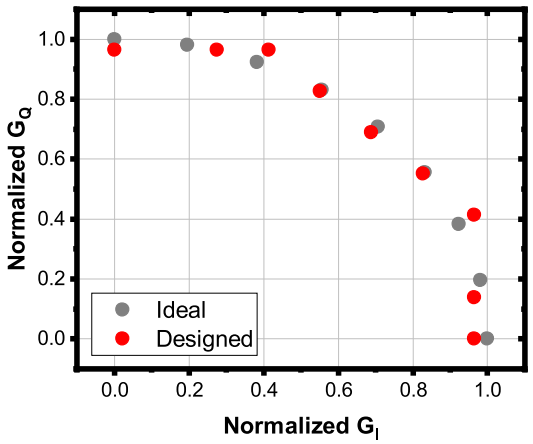


Fig. 13. I and Q gain weights of the designed VM.

B. Vector Modulator

The VM is designed with the structure proposed in Section II. Fig. 13 shows the I/Q gain weights G_I and G_Q of the designed VM from the 0° to 90° state. Compared with the ideal I/Q gain weight, the designed VM gain weight has some error. To investigate how the I/Q gain weight error in the VM affects the overall gain/phase error, the rms gain/phase error for the ideal gain weight and the designed gain weight was compared, as shown in Fig. 14(a) and (b), respectively. The contours with ideal gain weights are the same as the contours shown in Fig. 10(c) and 10(d). Fig. 14(a) and (b) shows that, compared with those of the ideal case, the rms gain and phase error increases for the designed gain weight case, and the phase error slightly shifts in the positive direction of the quadrature-phase error, θ. However, as the difference between the two cases is considerably small, the error due to the VM gain weight does not significantly affect the overall gain and phase error. Considering both the gain/phase error of the quadrature generator and the VM gain weight error, the rms phase and gain errors of the designed VSPS were calculated as 2°–2.6° and 0.27–0.34 dB from 57 to 66 GHz, respectively. As the simulation results of the rms phase and overall VSPS gain errors were 2.1°–2.4° and 0.27–0.34 dB from 57 to 66 GHz,

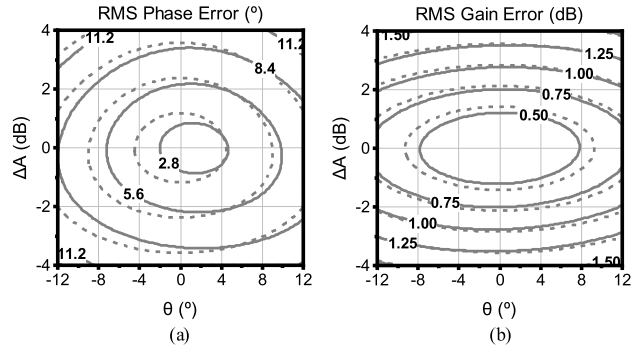


Fig. 14. Comparison of the calculated rms gain/phase error with an ideal gain weight and the designed gain weight (dashed line: ideal and solid line: designed).

respectively, this indicates that the gain/phase error of the proposed VSPS only occurred due to inaccurate gain weight and quadrature error. This is because the proposed IIVGA eliminates the effect of phase and impedance variation during vector modulation. The unit transistor size was set to 1 μm for low power consumption. Based on the I/Q gain weights in Fig. 11, each transistor array consists of four transistors of 1, 2, 4, and 7 μm with minimum channel lengths. Each transistor includes a capacitor and a resistor for the dc block and dc bias. Two 4-bit inverters were used in the I and Q paths to complementarily turn on and off the four transistors in each transistor array.

Vector modulated signals are amplified by the buffer amplifier (BA), which is designed with a CS structure. In the designed VM, an equivalent of 28 μm of transistor is turned on at the IIVGA, so the transistor BA size was set as 28 μm. To improve reverse isolation and gain, the capacitive neutralization technique [39] was adopted in the BA.

In multistage amplifier design, it is known that wideband characteristics can be achieved by designing the peak gain of each stage at different frequencies [1], [35]. In the proposed VSPS, we designed the I and Q VGAs to have peak gains at high frequencies and BA to have a peak gain at low frequencies so that the overall VSPS had wideband gain characteristics. In addition, to reduce the VSPS power consumption, a transformer-based current-reuse technique [36] was applied between the VM and the BA. Fig. 15 shows the layout of the transformer between the VM and the BA. As the sources of M_{B1} and M_{B2} and the center tap of the secondary coil are directly connected, the BA dc current can be reused. In this configuration, IIVGA and BA operate with a headroom voltage of half of the supply voltage. The capacitors are placed at the center tap of the secondary coil to create an ac ground for the RF signal. Due to the current-reuse technique, the proposed VSPS draws only 5 mA of dc current at a supply voltage of 1 V.

The proposed VSPS is matched to a differential 100 Ω at the output so that it can be integrated with a differential circuit block. However, due to the limitations of the measurement equipment, the Marchand balun is added to the output for single-ended measurement [40]. Fig. 16 shows the simulation results of the Marchand balun. The designed balun exhibits a 2–2.6-dB ohmic loss, <0.43-dB amplitude mismatch, and <0.54 ° phase mismatch.

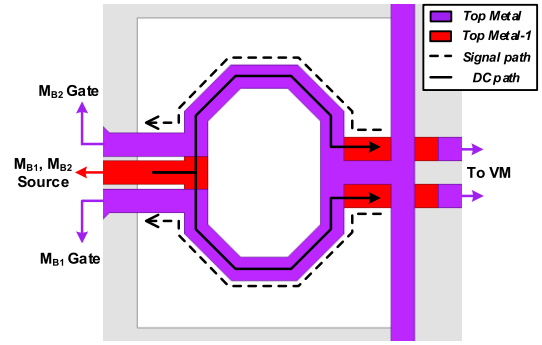


Fig. 15. Transformer-based current-reuse technique.

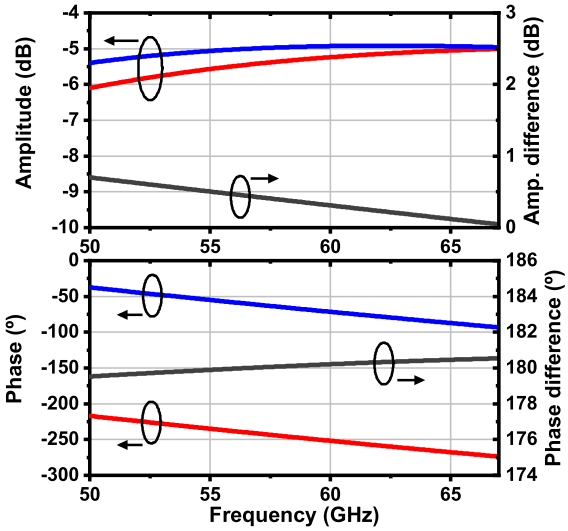


Fig. 16. Simulation results of the output Marchand balun.

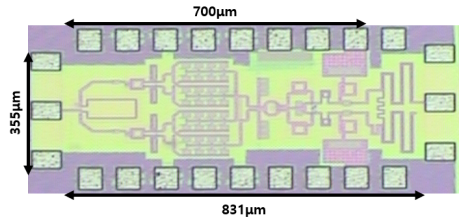


Fig. 17. Chip micrograph of the proposed VSPS.

IV. Measurement Results

The fabricated chip micrograph is shown in Fig. 17. The chip size of the proposed VSPS is 355 × 831 μm^2 excluding pads and 355 × 700 μm^2 excluding pads and output balun. The proposed VSPS consumes a dc power of 5 mW from a supply voltage of 1 V.

The small-signal performance was measured by using a network analyzer that operates up to 67 GHz, as shown in Fig. 18(a), and the large-signal performance was measured by using a signal generator, frequency extension module, variable attenuator, V-band coupler, V-band power sensor, and V-band power meter, as shown in Fig. 18(b).

Fig. 19(a) shows the chip micrograph of the test patterns for the quadrature coupler. Due to their large influence on the phase and gain errors, test patterns were fabricated and

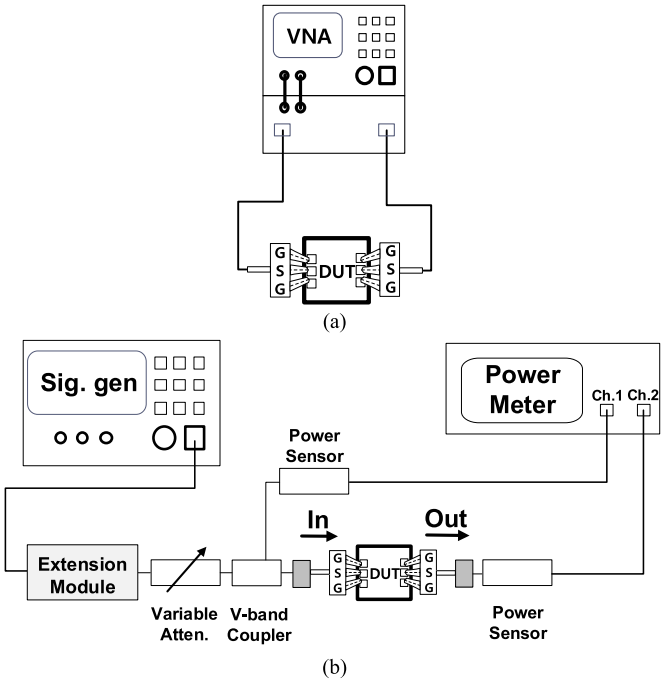


Fig. 18. (a) Block diagram of small-signal measurement setup. (b) Block diagram of large-signal measurement setup.

measured. For a two-port measurement, the test patterns were terminated with a 50-Ω on-chip resistor in the through and coupled ports. Fig. 19(b) shows the measurement results of the quadrature coupler. The designed quadrature coupler achieves an insertion loss of −3.7 dB. The amplitude and phase mismatch are less than 1.27 dB and 2.6°, respectively. Based on the measurement results, the quadrature coupler contributes an rms gain error of 0.30–0.53 dB and an rms phase error of 3°–4.3°, as shown in Fig. 14.

The measured and simulated S-parameters of the 0° state are plotted in Fig. 20. The measured results show a peak gain of −3.7 dB at 62 GHz and a 3-dB bandwidth of 15.6 GHz from 50.7 to 66.3 GHz, including the output balun. The input and output return losses are less than −10 dB from 50 to 67 GHz. Furthermore, compared with the simulation results, the measured gain was downshifted by approximately 3 GHz, which appears to be mainly due to imperfect modeling of the passive and active components in the 60-GHz band.

As shown in Fig. 21, for all 32 phase states, the input and output return losses are less than −10 dB from 50 to 67 GHz, indicating that the input and output matching is sufficient for all phase states and frequencies of interest. The measured return loss shows a fluctuation of approximately 3–4 dB, which appears to be due to the error in measurement.

The measured gain and rms gain error for all 32 phase states are plotted in Fig. 22. The peak average gain is −3.8 dB and the 3-dB bandwidth of the average gain is 15.3 GHz from 51 to 66.3 GHz. Only 1 dB of average gain variation from 52.6 to 64.7 GHz is observed. The measured rms gain error is 0.26–0.72 dB in the 3-dB bandwidth and 0.26–0.5 dB in the 57–66-GHz band.

The measured phase shift and rms phase error for all 32 states are plotted in Fig. 23. The phase shifter covers

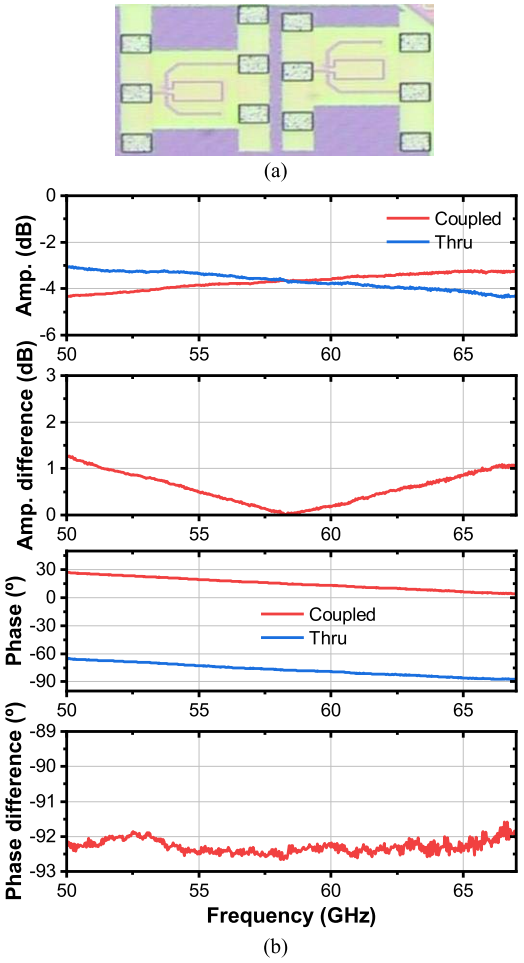


Fig. 19. (a) Chip micrograph of the test patterns for the quadrature coupler. (b) Measurement results.

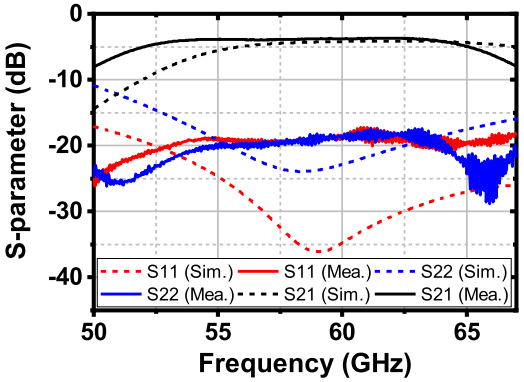


Fig. 20. Measured and simulated S-parameter of proposed VSPS at 0° state.

a 360° phase range with 5-bit resolution, and the measured rms phase error is 3°–7° in the 3-dB bandwidth and 3°–6° in the 57–66-GHz band. The measured rms gain and phase errors were higher than the simulation results for two reasons. First, the amplitude and phase mismatches of the quadrature coupler are higher than those of the simulation, as shown in Fig. 19. Second, the interstage 50-Ω matching between the quadrature coupler and the VM was varied compared with the simulation, especially at high frequencies, resulting in additional gain/phase error. This is because the load impedance

TABLE I
COMPARISON OF PRIOR ACTIVE VSPSS

	[17]	[19]	[21]	[22]	[25]	**This Work**
Technology	0.13 μm SiGe BiCMOS	65 nm CMOS	90 nm CMOS	28 nm FDSOI CMOS	40 nm CMOS	65 nm CMOS
Vector Modulation Topology	Gilbert cell	Common source	Tunable current splitter	Digital current steering	Analog current steering	Proposed IIVGA
Gain Control Method	Bias current	Gate voltage	Digital control with inverter	Digital control logic	Gate voltage	Complementary digital control with inverter
Frequency (GHz)	60–80	57–64	57–64	78.8–92.8	58–62	51–66.3
3-dB Bandwidth (GHz)	20	7	7	14	4	15.3
Phase Resolution (bits)	4	4	4	4	7	5
Average Gain (dB)	-3.2 (sim.)	4 (peak)	1.1 (peak)	2.3 (peak)	-5–0.4	-3.8 (peak) -1.8 (peak, w/o balun)
RMS Gain Error (dB)	<1.3	<1.2	0.75–1.6	<2	<0.5	0.25–0.72
RMS Phase Error (dB)	<9.1	<12	2.3–7.6	<11.9	<2.7	3–7
IP_{1dB} (dBm)	-27*	-38**	-9.8	-7***	-6.9	-0.23***
Noise Figure (dB)	9–11.6*	7.2****	9.7–13	10.8***	N/A	17*** (sim.)
Power Consumption (mW)	108* 34.8 (PS only)	16* 8 (PS only)	19.8	21.6	38	5
Size (mm^2)	1.06*	1.3*	0.61	0.12 (core only)	1.13	0.3 (core only)
FOM1 (GHz^2·bits/°)	367	193	792	440.7	1327	390 491 (w/o balun)
FOM2 (GHz^2·bits/°)	N/A	N/A	0.5	0.37	N/A	1.5 1.89 (w/o balun)

* Including LNA
**Including LNA and calculated from OP_{1dB} with gain
***Average values for all phase states
****LNA's noise figure

$$\text{FOM1}=\frac{f_0(\text{GHz})\times G(\text{lin.})\times B_{3\text{dB}}(\text{GHz})\times\text{Resolution(bits)}}{\theta_{\Delta,\text{RMS},3\text{dB}}(\text{deg})\times A_{\Delta,\text{RMS},3\text{dB}}(\text{lin.})},\quad \text{FOM2}=\frac{f_0(\text{GHz})\times G(\text{lin.})\times B_{3\text{dB}}(\text{GHz})\times IP_{1\text{dB}}(\text{mW})\times\text{Resolution(bits)}}{\theta_{\Delta,\text{RMS},3\text{dB}}(\text{deg})\times A_{\Delta,\text{RMS},3\text{dB}}(\text{lin.})\times P_{\text{dc}}(\text{mW})\times(NF(\text{lin.})-1)}\quad [22]$$

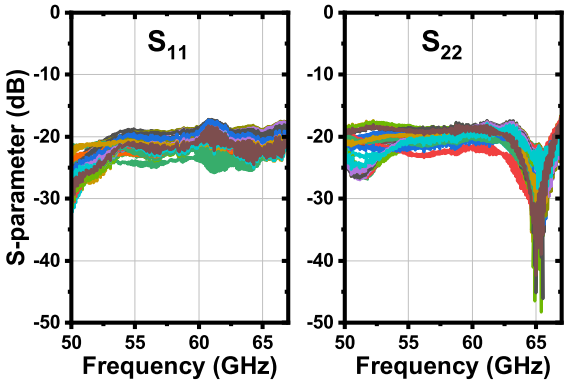


Fig. 21. Measured input return loss and output return loss for 32 phase states.

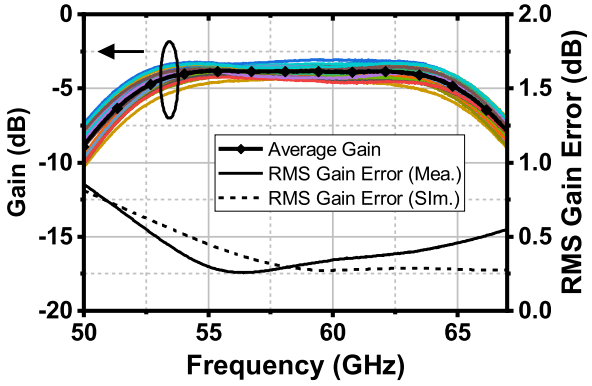


Fig. 22. Measured small-signal gain and rms gain error for 32 phase states.

variation of the quadrature generator can generate additional ΔA and θ.

The measured 1-dB compression point ($P_{1\,\text{dB}}$) at 60 GHz is shown in Fig. 24. The measured input $P_{1\,\text{dB}}$ varies from −1.1 to 0.86 dBm (average −0.23 dBm) and the measured output $P_{1\,\text{dB}}$ varies from −6.1 to −4.8 dBm (average −5.44 dBm).

Table I summarizes the proposed VSPS performance and compares it with other previously reported active vector-sum phase shifters in the 60-GHz and greater bands. The balun was deembedded by assuming a loss of 2 dB based on the simulation results, as shown in Fig. 16. For comparison with other works, two indicators, FOM1 and FOM2, are used, as proposed in [22].

In Table I, the proposed VSPS (excluding output balun) shows the highest FOM1 (apart from [21] and [25]) due to the low rms gain/phase error and wide 3-dB bandwidth.

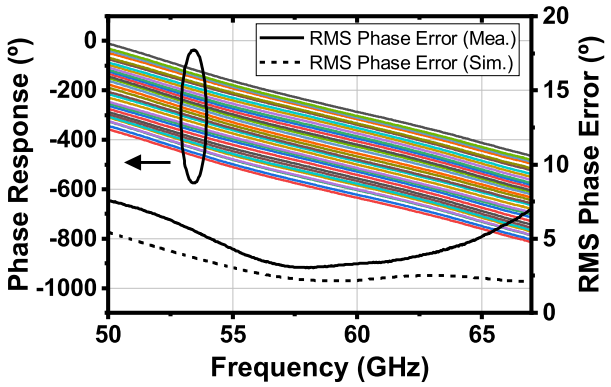


Fig. 23. Measured phase shift and rms phase error for 32 phase states.

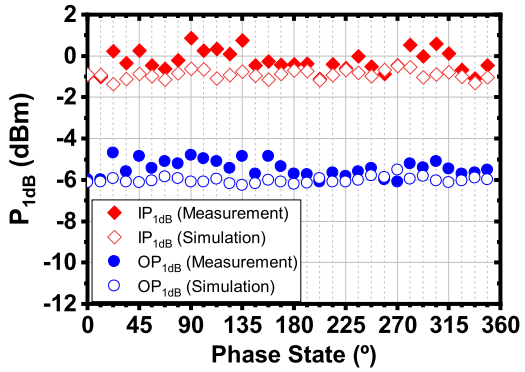


Fig. 24. Measured and simulated input $P_{1\,\mathrm{dB}}$ and output $P_{1\,\mathrm{dB}}$ at 60 GHz.

Yu *et al.* [21] and Wang *et al.* [25] showed higher FOM1 than this work due to higher gain and phase resolution, respectively. However, including linearity, dc power consumption, and noise figure, the proposed VSPS shows the highest FOM2 compared with the other works due to the low rms gain/phase error, the highest input $P_{1\,\mathrm{dB}}$, and the lowest dc power consumption regardless of the output balun and higher noise figure.

V. Conclusion

This study proposes a low-power VSPS fabricated in a 65-nm CMOS process. An IIVGA was proposed and applied to the VM to reduce the additional gain/phase error and improve the linearity of the VM. The proposed IIVGA eliminates the impedance and phase variation during gain control, thereby eliminating the additional gain/phase error during vector modulation. In addition, a transformer-based current-reuse technique was applied to reduce the VSPS power consumption. The prototype circuit occupies an area of 0.3 mm^2 (excluding the pads) and consumes only 5 mW of dc power. The measurement data revealed that the proposed VSPS achieved excellent performance with a gain of -3.8 dB (including a 2-dB loss of the measurement balun), an rms gain error of 0.25–0.72, an rms phase error of 3°–7°, a wide 3-dB bandwidth of 15.3 GHz, and higher than -1.1 dBm of input $P_{1\,\mathrm{dB}}$. These experimental results indicate that the proposed VSPS is highly suitable for low-power and large-scale phased array systems in the millimeter-waveband regime.

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