A 60 GHz 360° Phase Shifter with 2.7° Phase Resolution and 1.4° RMS Phase Error in a 40-nm CMOS Technology

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***Abstract*—This paper presents a vector modulator based active phase shifter for the 56-65 GHz frequency band in a 40-nm digital CMOS technology. The design comprises a magnetically-enhanced quadrature hybrid with better than 1-degree phase imbalance and 18 dB tuning range variable gain amplifiers with transformer broadband matching to generate 360° full-range phase tuning. It achieves 2.7° phase resolution for the first time. The rms phase error of the phase shifter is 1.4° and the rms gain error is 0.13 dB at 60 GHz. The insertion loss is 0.4 dB. The power consumption is 38 mW.**

***Index Terms*—Beam-forming, Beam-steering, Phase shifter, Phased Array, 60 GHz, phase resolution**

I. Introduction

Large scale phased arrays on silicon for 5G mobile devices, big data base station hardware and autonomous driving are drawing more attention than ever, targeting 100 Gbps data rate and high detection precision. The IEEE 802.11ad and IEEE 802.11ay standards target such applications at 60 GHz. In the 57-64 GHz band, [1, 2] present front-end designs for up to 42 Gb/s data rate. [2] utilizes only 2.16 GHz bandwidth per channel for IEEE 802.11ad and [1] implements only a single-path transceiver with 4-channel bonding for IEEE 802.11ay. To fully benefit from the 7-GHz wide bandwidth and large-scale beamforming techniques [2], a phase shifter with the full bandwidth, high phase resolution and low rms phase error is still one of the challenging blocks in a beamforming system.

State-of-art phase shifters [2, 4-7] achieve 4 to 5-bit-phase resolution either in a passive manner via reflective loading [4] or a switched-filter [5], or an active manner using a vector modulator based structure [6-8]. They have demonstrated the capabilities in a small or moderate-sized phased array but will introduce errors in precise beam steering in a large-scale array [3] and limit the continuous beam steering range to typically ±30°~±60°. This work presents a phase shifter with a 7-bit phase resolution for an RF phase shifting architecture (Fig. 1). It significantly improves the beam pointing accuracy to sub-1° and enables beam steering ranges of ±75° for the very first time as required for a 32×32(1024)-element array.

Passive phase shifters require more passive switchable stages for such fine phase resolution at the expense of large area cost and high signal loss. On the other hand, active phase shifters have advantages of low insertion loss, full phase shifting range, and are calibration-ready.

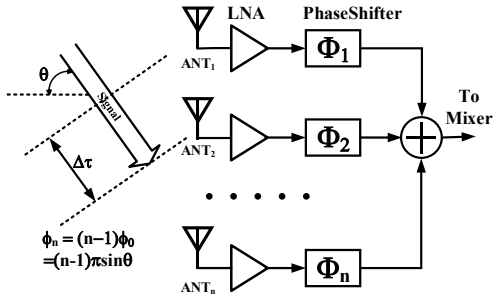

Fig .1. Phased array receiver FE with RF phase shifting.

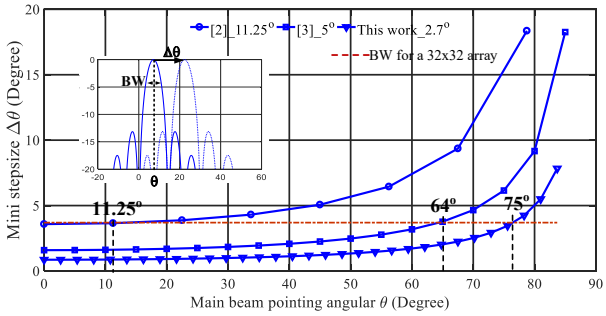

Fig. 2. Effect of phase shifter resolution (11.25°, 5° and 2.7°) on beam steering step-size.

This paper is organized as follows. In section II, the influence of the phase shifting resolution on the array performance is discussed. An active phase shifter with 7-bit resolution is presented in Section III, comprising a low phase invariant quadrature generator and large gain tuning range variable gain amplifiers (VGAs). Section IV provides the measurement results, with the measured variations over 5 samples. The conclusions are drawn in Section V.

II. Phase Resolution and Array Angular Accuracy

The phase shifting resolution has a significant impact on the beam pointing accuracy [3]. However, 5° phase resolution as demonstrated in [3] still limits the beam steering range for a 32×32(1024)-element array to ±64° (Fig. 2). In the past, the assumption of line-of-sight wireless communication is made for link calculation in the mm-Wave frequency range. In this ideal case, beam steering with small steps and narrow beam width is reached.

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For high angular coverage and high capacity, both the number of array elements and the range of continuous beam steering have to be improved. In general, for continuous beam steering, the main beam steering step size $\Delta\theta$ should be smaller than the half-power beamwidth (BW). Fig. 2 illustrates the beam steering range comparison between phase shifter configurations in [2, 3] and the 7-bit phase shifter of this work. It shows that for a 32×32-element array, the 7-bit phase shifter with 2.7° phase resolution can continuously steer for an angle of incidence θ between 0° and ±75° which translates into a significant increase of the angular coverage.

III. PHASE SHIFTER DESIGN

The single-ended phase shifter is based on a magnetically-enhanced 3 dB quadrature hybrid, a vector modulator and an output balun as shown in Fig. 3. To achieve the finest phase resolution and low phase error, there are two main design challenges: 1) Phase-invariant quadrature signal generation: better than 1° phase and ±1 dB amplitude imbalance is achieved in this work; 2) Large gain tuning range variable gain amplifiers (VGA): 18 dB tuning range is achieved.

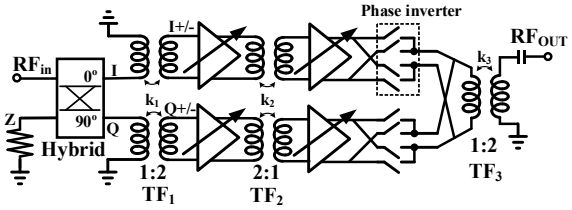

Fig. 3. Simplified diagram of vector-module based phase shifter.

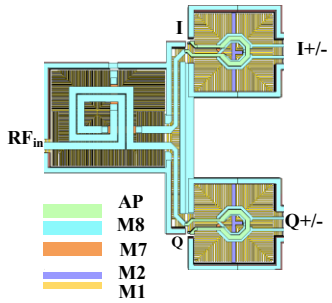

Fig. 4. EM model of the 3 dB quadrature hybrid and transformer-based baluns.

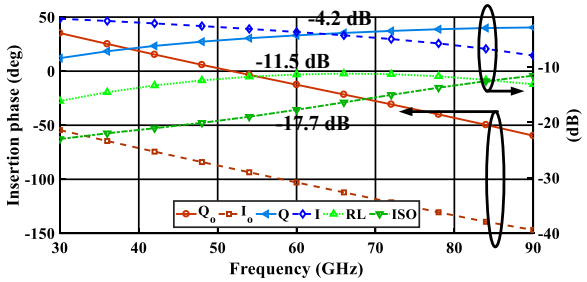

Fig. 5. EM simulation results of the quadrature hybrid.

A. Quadrature generation

A magnetic coupling enhanced quadrature hybrid with reduced dimension of 105×105 μm² is implemented in the top two metal layers as shown in Fig. 4, with a 0.606 coupling coefficient. The equivalent inductances of the primary/secondary windings are 308/335 pH. The transformer-based balun TF_1 (Fig.4) is utilized for single-ended to differential conversion and as matching network

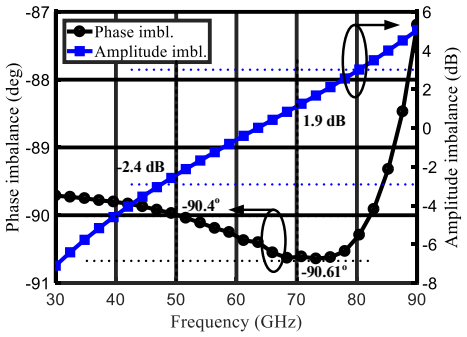

Fig. 6. Simulated Phase imbalance and amplitude imbalance of the quadrature generator.

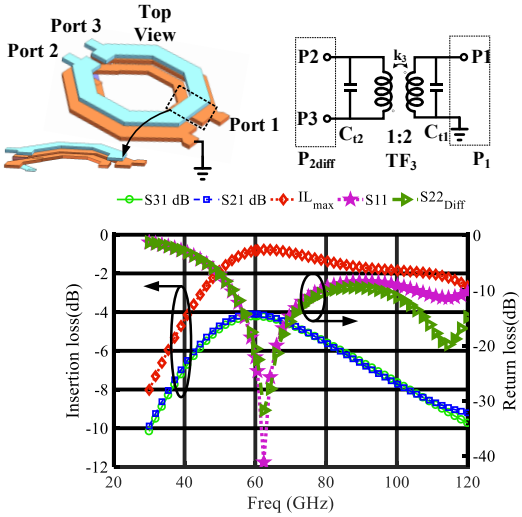

Fig. 7. EM model and simulation results of TF_3 transformer.

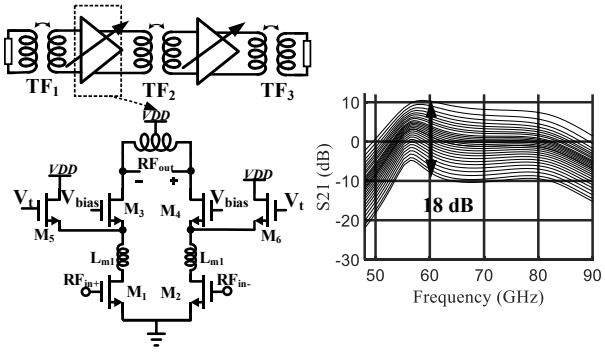

Fig. 8. Left: Simplified schematic of the differential VGA, Right: Simulation results of gain tuning S_{21}.

for the succeeding circuits from the lower impedance (50Ω) of the hybrid to the amplifier input. As shown in Fig. 4, transformer TF_1 has a 1:2 turn ratio and a self-resonance frequency of 103 GHz with a coupling coefficient of 0.726. Fig. 5 shows the electromagnetic (EM) simulation of the magnitude and phase responses of the hybrid. The coupling and through (Q, I) ports achieve -4.2 dB insertion loss, the return loss (RL) is 11.5 dB and the isolation (ISO) is 17.7 dB. Fig. 6 shows that the phase and amplitude imbalance is less than 1° and ±1 dB in the band of 56 GHz and 65 GHz. Moreover, the phase imbalance remains below 1.5° from 30 GHz to 90 GHz, and the 3-dB amplitude imbalance bandwidth is from 48 GHz to 80 GHz.

B. Variable gain amplifier

In the vector modulator, a pair of I/Q VGAs is deployed to implement the Cartesian amplitude weighting (Fig. 3). The VGA is a two-stage cascode differential structure, integrated with a phase inverter, to achieve a 360° phase tuning. Gain tuning is achieved by the current steering technique. The converted differential quadrature signals from baluns TF_1 are fed into VGAs, and the outputs sum up with a loading transformer TF_3 for differential to single-ended conversion. The EM model and simulation results of TF_3 are shown in Fig. 7, where the tuning capacitors C_{t1} and C_{t2} are deployed to compensate the leakage inductances. The insertion loss of the balun is optimized by substrate shielding and trace widths choice. The insertion loss of the transformer is 0.79 dB at 60 GHz and S_{11} is below 10 dB from 55 GHz to 79 GHz. The amplitude imbalance of port 2 and port 3 is less than 1 dB and the phase imbalance is 5°.

In Fig. 8, the details of the current steering amplifier and the differential VGA simulation results are presented. In the half circuit, the cascode transistor M_3 and the steering transistor M_5 splits the overall current I_d through the input transistor M_1. In general, the current steering ratio between M_3 and M_5 is proportional to the width ratio and gate biasing ratio of M_3 and M_5. The sizing of M_3 and M_5 is carefully chosen for gain tuning range requirements, trading off the maximum conversion gain and the linearity. The phase inverter uses Gilbert cell switches to select phases at 0°, 90°, 180°, 270° by the control signals I_0/I_{180}. Inter-stage inductors L_m are utilized to compensate the parasitic capacitances C_{gs} and C_{sb} of M_3 and M_5. Another transformer TF_2 with a 2:1 turn is deployed as loading and matching network. The simulated tuning range of S_{21} is 18 dB with a wide bandwidth from 55 to 80 GHz.

IV. Measurement Results

The circuit has been fabricated in a digital 40-nm CMOS technology. The die photo of the phase shifter is shown in Fig. 9 where the chip is DC wired bonded to a PCB. It occupies an area of 1545×735 μm^2, including all pads. Fig. 9 presents the measurement setup.

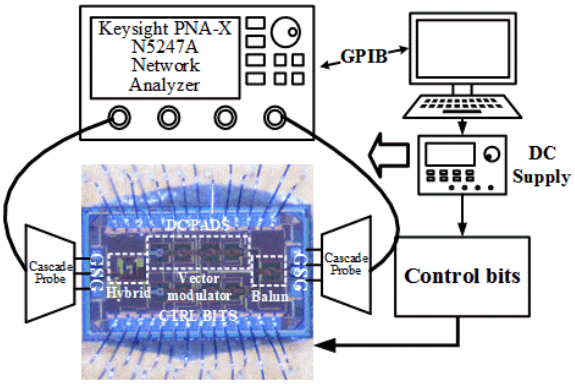

Fig. 9. Die microphotograph and measurement setup.

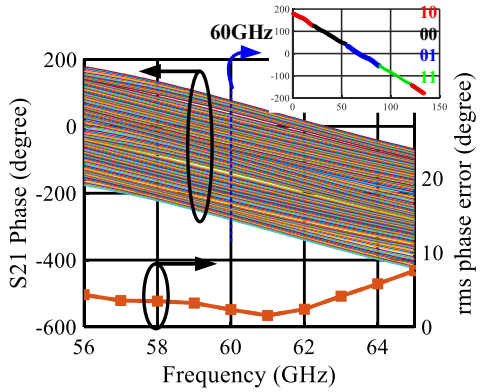

Fig. 10. Measured insertion phase and rms phase error of the phase shifter; zoom in: 360° tuning range at 60 GHz (phase inverter control I_0/I_{180} (10/00/01/11).

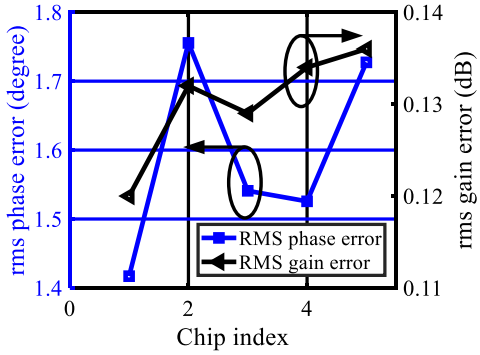

Fig. 11. Measured phase/gain error across 5 chip samples.

The phase tuning range is 360° as shown in Fig. 10, and the average phase resolution is 2.7°, 7-bit response. The lowest phase error of 1.4° is achieved between 60.48 GHz and 61.56 GHz for IEEE 802.11 ad. Standard. The rms phase error remains below 2.7° in the band of 58 GHz and 62 GHz, and less than 7° in the rest of the band. The measured rms phase error at 60 GHz of 5 chips is shown in Fig. 11 and demonstrates consistency in phase error.

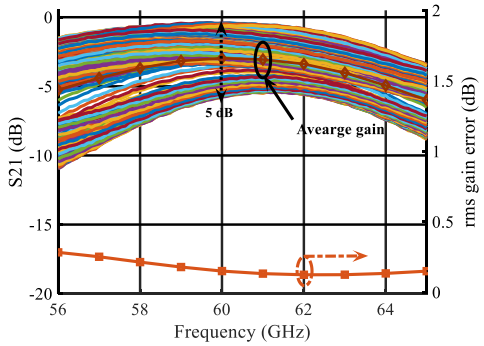

Fig. 12. Measured insertion loss of the phase shifter, rms gain error.

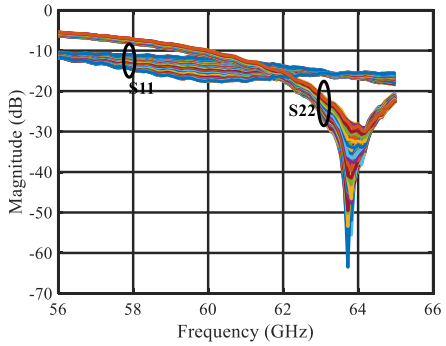

Fig.13. Measured return loss in the band.

The measured S-parameter S_{21} is shown in Fig. 12. It demonstrates maximum -0.4 dB conversion gain at 60 GHz. The conversion gain varies by 5 dB over the phase states. The total magnitude error is 0.13 dB rms at 60 GHz and better than 0.5 dB within the band. The gain error cross 5 chips is between 0.12 dB to 0.14 dB at 60 GHz. Fig. 13 shows that the return loss of S_{11}/S_{22} is below 10 dB in the band for all the phase states. The measured S_{22} is shifted to higher frequency (Fig. 13) because of the bias-dependent gate-source capacitances of the steering transistors. The measured phase shifter requires 38 mA current from a 1 V supply. Table I summaries the comparison with other prior state-of-art works of phase shifters in CMOS technology. This work achieves the best performance in combination of phase resolution, conversion gain, RMS gain/phase error and bandwidth at 60 GHz and above.

TABLE I
COMPARISON TABLE

	This work	**[6]**	**[7]**	**[8]**
Frequency (GHz)	56-65	78.8-92.8	57-64	55-65
Technology	40 nm CMOS	28 nm FDSOI	90 nm CMOS	55 nm CMOS
Architecture	VMPS	VMPS	VMPS	VMPS
Phase res. (°)	2.7	22.5	22.5	6.4
RMS phase error	1.4	9.4	2.3	2.5
max Gain (dB)	-5~ -0.4	2.3	1.1	-3
RMS gain error	0.13	1.68	0.75	<0.5
IP1dB (dBm)	-6.9	-8	9.7	-16
Area (μm^2)	1535×735	540×120(core only)	936×657	1300×1300
Power (mW)	38	21.6	19.8	16
FoM	1327*	440.7	792	686

$FOM = \frac{f_0(GHz)\times G(lin.)\times B_{3dB}(GHz)\times Resolution(bits)}{rmsPhaseError(°)\times rmsGainError(lin.)}$ [6]

*Bandwidth of 58~62 GHz for FoM calculation

V. CONCLUSION

This paper demonstrates a vector-modulator based 7-bit phase shifter which achieves a phase resolution of 2.7° and phase accuracy of 1.4°. A broadband quadrature hybrid with better than 1° phase imbalance as well as large tuning range VGAs have been implemented. This high-performance phase shifter improves the phase resolution of large scale arrays by 4 times as required for 5G mobile communication and autonomous driving applications.

ACKNOWLEDGMENT

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