

# A 2–24-GHz 360° Full-Span Differential Vector Modulator Phase Rotator With Transformer-Based Poly-Phase Quadrature Network

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**Abstract**—This article presents a differential vector modulator-based phase rotator (PR) performing 360° full-span phase interpolation over a first-ever decade-wide instantaneous bandwidth from 2 to 24 GHz. The proposed PR employs a three-stage transformer poly-phase network with high-precision and ultra-wide-bandwidth, two highly linear 5-bit variable gain amplifiers (VGAs), a differential series-shunt-series inductor peaking load network for bandwidth extension and an open-drain buffer. It is implemented in a standard 65-nm bulk CMOS process with a chip area of 1.2 mm × 1.8 mm. The measurement results demonstrate the maximum rms quantization phase error of 1.22° within a 1.5-dB output magnitude variation for full 360° interpolations from 2 to 24 GHz and the –3-dB magnitude bandwidth is up to 19 GHz, respectively. Moreover, due to the wideband high-quality in-phase/quadrature (*I/Q*) signal generation and high-precision *I/Q* interpolation of the VGAs, the PR can perform full-span phase synthesis with a constant set of phase shift code settings for all the operating frequencies. For interpolating 22.5°/15° phase step over the 360° full-span, the “one-code” setting operation achieves an rms phase error of 1.56°/1.42° from 3.5 to 22.5 GHz without any frequency-dependent code/look-up table (LUT), tunable element, or band-selection switch. Furthermore, with the “one-code” setting operation, the modulation tests demonstrate measured rms error-vector-magnitude (EVM) values below 5% for a 50-kSym/s QPSK signal from 3.3 to 22.3 GHz and for a 16-quadratic-amplitude modulation (QAM) signal from 2.7 to 22 GHz.

**Index Terms**—Phase shifter, phased-array, poly-phase network, quadrature (*Q*) generation, transformer, vector modulator.

## I. INTRODUCTION

PHASED-ARRAY systems play a critical role in modern wireless communication systems due to its unique advantages, e.g., spatial power combining, signal-to-noise-ratio (SNR) improvement, high equivalent-isotropic-radiated-power (EIRP), and beam-forming and beam-steering for

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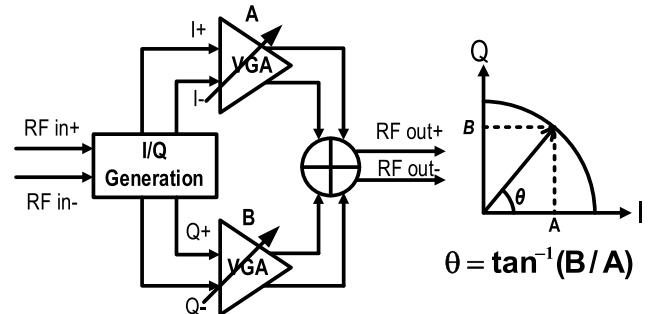


Fig. 1. Typical Cartesian *I/Q* vector modulator PR.

spatial filtering [1]–[3]. Recently, wideband phased-array systems are gaining an increasing interest in frequency-agile phased-array radars, hyperspectral imaging systems, and next-generation millimeter-wave (mm-Wave) communication systems. The phase rotator (PR) is one of the key elements in the phased-array systems, since the beam-forming/beam-steering performance of the array heavily relies on the phase interpolation accuracy of the PR.

A reflective-type phase shifter (RTPS) is a passive approach for phase interpolation. It consists of a 90° quadrature (*Q*) hybrid and two matched tunable reflective loads to achieve desired phase shifting. However, RTPS experiences a direct tradeoff between the insertion loss (IL) and the phase shifting range, and the 90° *Q* hybrid often requires an excessive chip area at GHz RF frequencies [4], [5]. Other passive phase shifters, such as tunable delay lines [6] and switched low-pass/high-pass-filter-based phase shifters [7], also often suffer from substantial passive loss. On the other hand, a Cartesian vector modulator-based PR is widely used as an active approach, and it can achieve dense phase interpolations over 360° full-span together with signal amplification [8]. It typically consists of an in-phase/*Q* (*I/Q*) generation network, *I/Q* variable gain amplifiers (VGAs), and a signal summing circuit network (Fig. 1). The input RF signal is first divided into *I* and *Q* signals with matched amplitude and phase. These *I/Q* signals are then independently amplified by the *I/Q* VGAs with proper weightings and subsequently combined at the output summing circuit to achieve the desired phase interpolation. The phase interpolation accuracy highly relies on

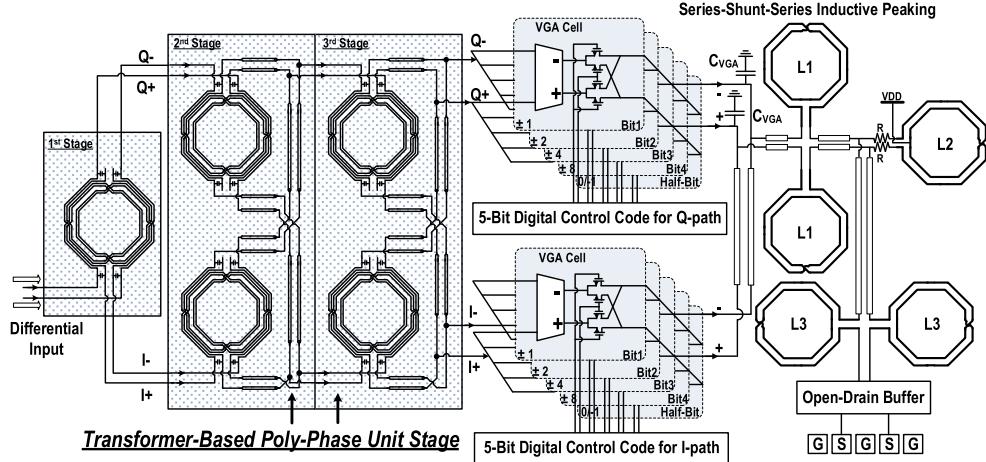


Fig. 2. Schematic of the proposed PR with a transformer poly-phase network, broadband  $I/Q$  VGAs, and a shunt-series-shunt inductive peaking load network. An open-drain buffer is included to facilitate the testing.

the  $I/Q$  magnitude/phase balance and the VGA linearity and matching performance. Therefore, it is essential to realize an  $I/Q$  generation network design with low loss, high-precision  $I/Q$  magnitude/phase balance, robustness to process variations, and input–output matching. In parallel, the  $I/Q$  VGAs need to provide good linearity to allow for high-performance  $I/Q$  interpolations. Moreover, an ultrabroadband vector modulator PR requires the  $I/Q$  generation network,  $I/Q$  VGAs, and the output summing circuit to operate over the entire bandwidth, posing further challenges on the PR design. As a result, reported vector modulator-based PRs typically cover less than a 3:1 frequency bandwidth, limiting their use in ultrabroadband and highly frequency-agile phased-array systems [8], [15], [16], [21], [22].

The  $RC$ – $CR$  pairs are widely used for  $I/Q$  signal generation [9]. However, it suffers from several issues, such as signal loss, narrow bandwidth, loading effects, and sensitivity to process variations. The  $RC$ – $CR$  poly-phase network configuration provides design robustness and bandwidth extension but at the direct expense of exacerbated signal loss [9], [10]. On the other hand,  $\lambda/4$  transmission line-based passive networks, e.g., branch-line couplers, can generate  $I/Q$  signals with low loss and design robustness [11]. However, they often require excessive chip area, limiting their use at the GHz RF frequency ranges.

To address these challenges, transformer or  $LC$ -resonance-based  $I/Q$  generation networks are demonstrated in CMOS to generate high-precision  $Q$  signals with low loss, robustness, compact chip areas, and input–output matching [12]–[15]. Folded transformer  $I/Q$  generation network is reported to generate fully differential  $I/Q$  signals within a one-transformer footprint for further area reduction [17]. However, the bandwidth of these approaches is limited to only 20%–30%, directly limiting their use in ultrabroadband PRs.

In this article, we propose and demonstrate a Cartesian vector modulator-based PR that is capable of performing high-precision phase interpolation over a first-ever one-decade instantaneous bandwidth [18]. We propose to employ a three-stage transformer poly-phase network for ultrabroadband

$I/Q$  generation with low loss, input matching, high robustness to the process variation, and a compact chip area [19]. In addition, broadband well-matched  $I/Q$  VGAs with a differential shunt-series-shunt inductor output peaking load are employed to ensure high-precision  $I/Q$  scaling and signal combining over this decade-wide operation bandwidth [20].

This article is organized as follows. Section II presents the architecture of the proposed vector modulator-based PR. The design details and the full 3-D electromagnetic (EM) simulation results of the three-stage transformer poly-phase network are introduced in Section III. Section IV presents the design and implementation of the  $I/Q$  VGAs. Section V presents the complete measurement results, including the VGA linearity performance, full-span 360° static phase interpolation, and dynamic modulation tests with 16-quadratic-amplitude modulation (QAM)/QPSK signals. The measurements demonstrate that our PR is capable of high-precision phase interpolation with a constant set of phase shifting code settings for an over-a-decade bandwidth without any frequency-dependent code/look-up table (LUT), tunable element, or band-selection switch.

## II. PROPOSED ULTRABROADBAND PR ARCHITECTURE

The schematic of the proposed Cartesian  $I/Q$ -modulator-based PR is shown in Fig. 2 [18]. It consists of a three-stage transformer poly-phase network, two 5-bit  $I/Q$  VGAs, a differential series–shunt–series inductive peaking load network, and an open-drain buffer for testing. The differential input signals are first divided into differential  $I/Q$  signals with well-matched amplitude/phase by the transformer poly-phase network over a one-decade bandwidth [19]. The resulting  $I/Q$  signals are then independently scaled by the  $I/Q$  VGAs. The scaled  $I/Q$  outputs are combined in the current domain to achieve desired phase interpolations. Each  $I/Q$  VGA comprises 4-bit binary-weighted VGA cells and an additional half-bit VGA cell. The VGA cell includes a differential common-gate (CG) buffer and current-commutating switches to provide broadband input matching and output polarity selection. The 4-bit binary VGA cells provide normalized

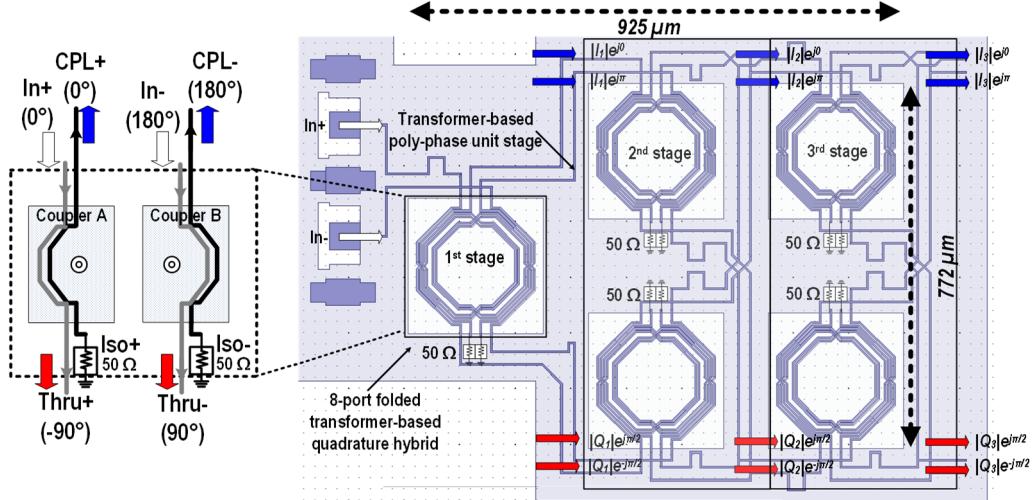


Fig. 3. Full 3-D EM model of the three-stage transformer poly-phase network.

current weightings of  $\pm 1$ ,  $\pm 2$ ,  $\pm 4$ , and  $\pm 8$  on the RF  $I/Q$  signals. The extra half-bit VGA cell provides a normalized weighting of  $-1/0$ , which together with the 4-bit binary VGA cells realize a normalized current weighting from  $-15$  to  $+15$ . The differential series–shunt–series inductive peaking load absorbs the VGA output parasitic capacitors  $C_{\text{VGA}}$  and the input parasitic capacitors  $C_{\text{buff}}$  of the open-drain buffer for bandwidth extension [20].

### III. THREE-STAGE TRANSFORMER POLY-PHASE NETWORK FOR I/Q GENERATION

In this section, the three-stage transformer poly-phase network will be introduced [19]. The interface design considerations of the poly-phase network and the  $I/Q$  VGAs are presented.

Fig. 3 shows the 3-D EM model (HFSS) of the three-stage transformer poly-phase network. It consists of a differential transformer  $Q$  hybrid as the first-stage and two transformer poly-phase unit stages as the second and third stages. First of all, the first stage takes the differential RF input signal to generate differential  $I/Q$  signals (Fig. 3). The magnitude and phase responses of an example design of the first-stage differential transformer  $Q$  hybrid at normalized frequency are shown in Fig. 4(a). The 1-dB  $I/Q$  magnitude mismatch bandwidth is from 0.75 to 1.18, and the  $5^\circ I/Q$  phase mismatch bandwidth is from dc to 1.28. Thus, the  $I/Q$  magnitude mismatch is the limiting factor and should be suppressed to allow for ultrabroadband  $I/Q$  signal generation. Note that the  $I/Q$  magnitude mismatch is mainly due to the inherent path mismatches between the couple (CPL) path and the through (THRU) path of the transformer  $Q$  hybrid in Fig. 4(b). Next, cascading the transformer poly-phase unit stages is used to suppress this  $I/Q$  magnitude mismatch. Fig. 5 shows the schematic of the transformer poly-phase unit stage in its unfolded configuration. It consists of four single-ended transformer  $Q$  hybrids and has four inputs ( $|I_N|e^{j0}$ ,  $|I_N|e^{j\pi}$ ,  $|Q_N|e^{j\pi/2}$ ,  $|Q_N|e^{-j\pi/2}$ ) and four outputs ( $|I_{N+1}|e^{j0}$ ,  $|I_{N+1}|e^{j\pi}$ ,  $|Q_{N+1}|e^{j\pi/2}$ ,  $|Q_{N+1}|e^{-j\pi/2}$ ). The suppression of

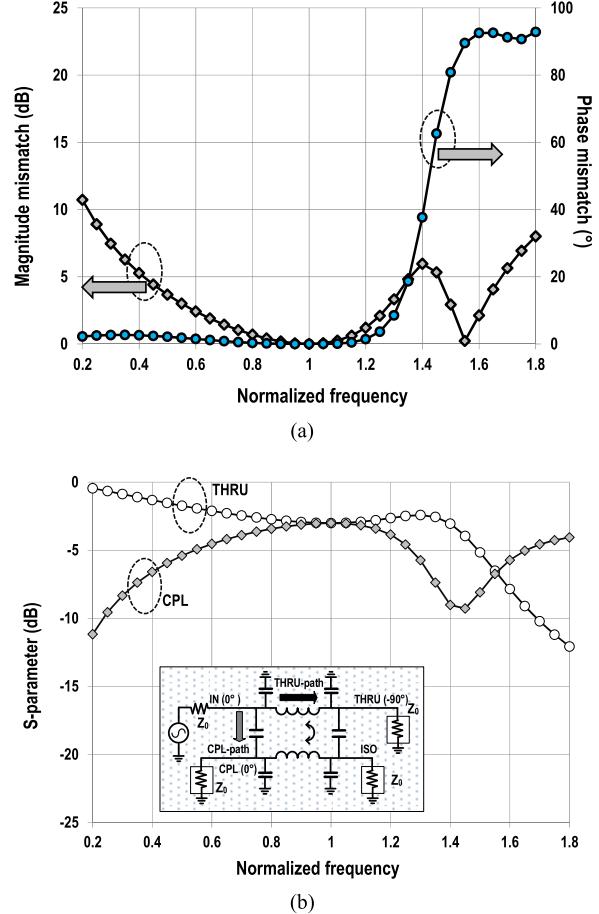


Fig. 4. Simulated (a)  $I/Q$  magnitude/phase mismatches and (b) magnitude responses of THRU and CPL of a differential transformer  $Q$  hybrid that is used as the first stage in the three-stage transformer poly-phase network.

$I/Q$  magnitude mismatches can be intuitively explained as follows. Taking the output  $0^\circ$  ( $|I_{N+1}|e^{j0}$ ) as an example, it is generated by combining two output signals; one is from the input  $0^\circ$  ( $|I_N|e^{j0}$ ) passing through the CPL-path (gray coil) of

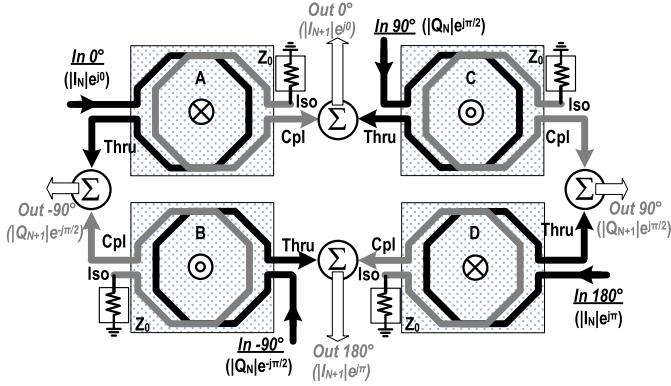


Fig. 5. Schematic of the transformer poly-phase unit stage in its unfolded configuration.

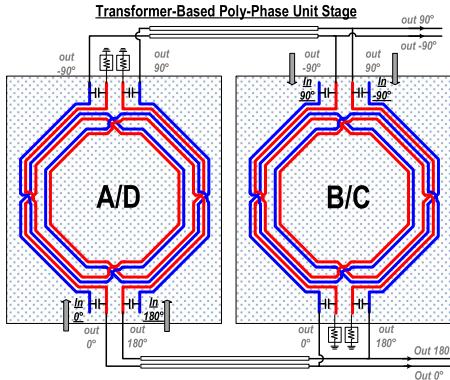


Fig. 6. Implementation of the transformer poly-phase unit stage using two eight-port differential folded transformer  $Q$  hybrids.

the coupler A with a phase shift of  $0^\circ$ , and the other is from the input  $90^\circ (|Q_N|e^{j\pi/2})$  passing through the THRU-path (black coil) of the coupler C with a phase shift of  $-90^\circ$ . The other three outputs are generated similarly. Thus, each output is generated by combining an output from the CPL-path and an output from the THRU-path, and this balances the amplitude response of the four output signals and achieves matched  $I/Q$  amplitudes over an ultrabroadband frequency range. The analytical modeling of this  $I/Q$  magnitude mismatch suppression is provided in [19]. In addition, due to the differential signaling relation between the couplers A and D (or couplers B and C), the couplers A and D (or B and C) can be folded together within a one-transformer footprint by exploiting the proper magnetic enhancement. Thus, the network with four single-ended transformers (Fig. 5) can be merged within only two differential transformers (Fig. 6) for area reduction.

To maximize the bandwidth and minimize the passive loss, the interface design between the poly-phase network and the  $I/Q$  VGAs is very critical. Fig. 7 shows the simulated performance of the transformer poly-phase network at different output loads; the transformer network is modeled with the 3-D EM simulation. Note that the input parasitic capacitance of VGA is absorbed into the proposed poly-phase network. Fig. 7(a) and (b) shows that the  $I/Q$  magnitude/phase mismatches are below 1 dB and  $5^\circ$  from 3 to 24 GHz, demonstrating very robust and high-precision  $I/Q$  generation versus

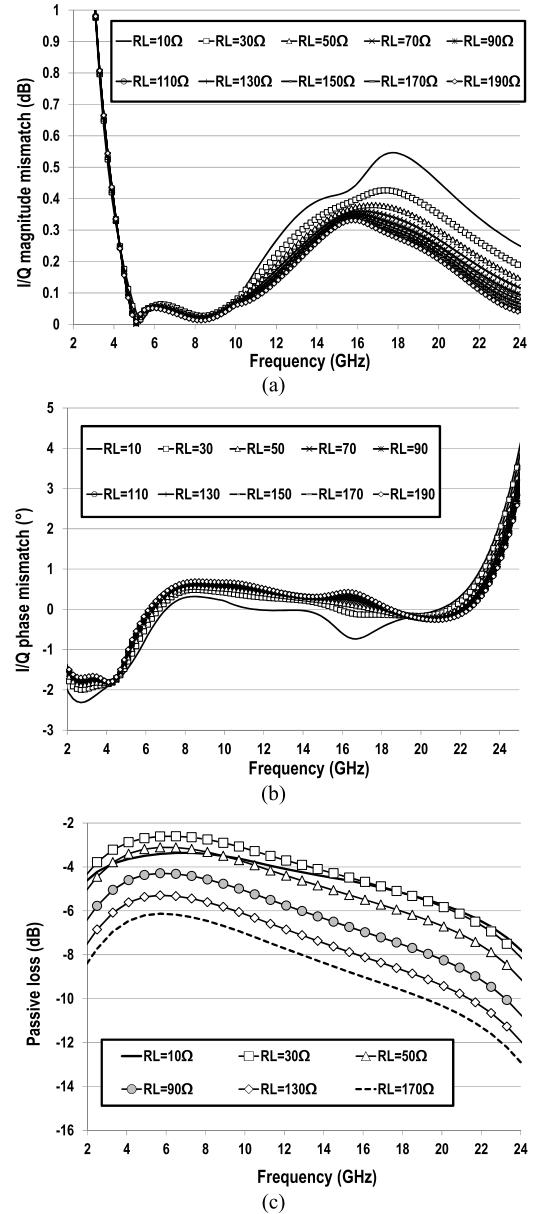


Fig. 7. Simulated (a)  $I/Q$  magnitude mismatch, (b)  $I/Q$  phase mismatch, and (c) passive loss for different output loads ( $R_L$ ) versus frequency. The transformer network is modeled using full 3-D EM simulation. Note that the input parasitic capacitance of VGA is absorbed into the proposed poly-phase network.

the load variations. Fig. 7(c) shows the passive loss of the three-stage transformer poly-phase network at different output loads. As the load  $R_L$  increases, the voltage gain increases monotonically. On the other hand, the network passive loss increases as the load  $R_L$  deviates from the matched load (single-ended  $25 \Omega$ ). Note that all the transformer  $Q$  couplers here are designed with  $50\Omega$  characteristic impedance, and the output impedance of the poly-phase unit stage is thus single-ended  $25 \Omega$  due to the output signal combining (Figs. 5 and 6) [19]. Considering these simulation results, we design the VGAs with a CG amplifier configuration that provides  $34\Omega$  single-ended load resistance to achieve a balanced voltage gain and passive loss. In addition, the extracted CG

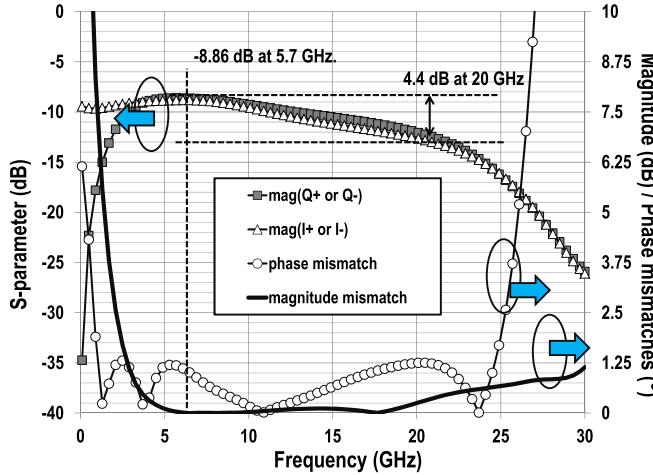


Fig. 8. Simulated  $I/Q$  magnitude responses and  $I/Q$  magnitude/phase mismatch with the output load impedance of  $34 \Omega/96 \text{ fF}$  (single-ended) by the CG  $I/Q$  VGAs. The transformer network is modeled using full 3-D EM simulation.

VGA input parasitic capacitance is  $96 \text{ fF}$  (single-ended), when implemented in a standard 65-nm CMOS process (Section IV). The effective parasitic pole by  $34 \Omega$  and  $96 \text{ fF}$  is well beyond 25 GHz and will not affect the response of the poly-phase network. With the four output loads each as  $34 \Omega/96 \text{ fF}$ , the simulated  $I/Q$  magnitude mismatch is within 1 dB from 2.9 to 29 GHz, while the  $I/Q$  phase mismatch is within  $5^\circ$  from 2 to 26 GHz. The simulated passive loss is only 2.86 dB (Fig. 8). Note that the input RF signal is equally divided into four  $|I_3|e^{j0}$ ,  $|I_3|e^{j\pi}$ ,  $|Q_3|e^{j\pi/2}$ , and  $|Q_3|e^{j-\pi/2}$  by the transformer poly-phase network (Fig. 2), and thus the ideal IL is 6 dB due to the signal dividing. Therefore, the interface design allows the on-chip three-stage transformer poly-phase network to achieve high-quality low-loss  $I/Q$  signal generation over a one-decade bandwidth with the realistic complex input impedance of the  $I/Q$  VGAs.

#### IV. BROADBAND I/Q VGA IN CMOS

In this section, we will present the design details of the ultrabroadband linear digital  $I/Q$  VGAs, their bias generation circuit, and the output inductive peaking network.

##### A. Linear Digital VGA

The schematic of the linear digital VGA is shown in Fig. 9. It consists of 4-bit binary weighted VGA cells and one additional half-bit VGA cell. Each VGA cell includes a differential transconductance stage as a differential CG input ( $M_5$  and  $M_6$ ) and four current-commutating switches ( $M_1$ ,  $M_2$ ,  $M_3$ , and  $M_4$ ) to configure the output current polarity. The source nodes of the input CG transistors of all the 5-bit VGA cells are connected in parallel to form the differential VGA inputs, i.e., input+ and input-, while the drain nodes of the switch quad transistors are connected in parallel to from the differential outputs, i.e., output+ and output- (Fig. 9). The differential  $I/Q$  outputs of the three-stage transformer poly-phase network

are directly connected to the differential inputs of the  $I/Q$  VGAs. The CG transistors of the  $I/Q$  VGAs are properly sized, so that the single-ended input impedance is  $34 \Omega/96 \text{ fF}$  to ensure the broadband response of the poly-phase network (Section III). The transistor size for the half-bit cell is the same as that for the Bit1 cell. The sizing information for the half-bit cell is shown in Fig. 9.

Each VGA cell behaves as a polarity selector to provide a normalized output RF current amplitude of  $\pm 1$  (Bit1),  $\pm 2$  (Bit2),  $\pm 4$  (Bit3),  $\pm 8$  (Bit4), or  $-1/0$  (Half-Bit). Combining the outputs of these five cells thus allows the 5-bit VGA to accurately interpolate an output RF current with its normalized amplitude from  $-15$  to  $+15$ . Taking the Bit1 VGA cell of the  $I$ -path VGA as an example, when its differential control Bit1 is “high” ( $S^+ = \text{high}$  and  $S^- = \text{low}$ ), the transistors  $M_1$  and  $M_4$  are turned on, and the transistors  $M_2$  and  $M_3$  are turned off. Thus, the output current of the transistors  $M_5$  and  $M_6$  are sent to the output+ and output-, respectively, achieving a normalized output current weighting of  $+1$ . Conversely, when the control Bit1 is “low” ( $S^+ = \text{low}$  and  $S^- = \text{high}$ ), the output current phase is reversed, providing a normalized output current weighting of  $-1$ . For the half-bit VGA cell, the drains of the transistors  $M_1$  and  $M_4$  are directly tied to the power supply VDD. Thus, when its control Bit\_Half is “high” ( $S^+ = \text{high}$  and  $S^- = \text{low}$ ), its output RF current is terminated at the VDD, producing a zero-normalized output current. When its control Bit\_Half is “low” ( $S^+ = \text{low}$  and  $S^- = \text{high}$ ), the output RF current are reversely connected to the output+/output-, providing a normalized current weighting of  $-1$ . Besides accurate output RF current interpolation, this  $I/Q$  VGA architecture also ensures that the VGA input and output present constant impedance values independent of the VGA settings, facilitating the wideband input and output matching.

The  $I/Q$  VGAs’ layout is shown in Fig. 9. The layout is arranged to maintain symmetry between the  $I$ -path and  $Q$ -path and provide a minimized chip area. The  $I/Q$  VGAs occupy  $57 \mu\text{m} \times 80 \mu\text{m}$ . The Bit4 cell is designed as two Bit3 cells to minimize the differential nonlinearity.

##### B. Bias Generation Circuit for $I/Q$ VGAs

Since a CG topology is employed for the  $I/Q$  VGAs, the source nodes of the differential input CG transistors should be properly biased (Fig. 9). A conventional approach is to use current sources to bias the CG transistors, and ac capacitive coupling can be employed to couple the poly-phase network outputs to the CG source inputs. However, this approach will introduce excessive parasitic capacitance and substantially limits the high-frequency PR operations. Moreover, the input ac coupling capacitors will limit the low-frequency cutoff. To maximize the PR operation bandwidth, we choose to employ dc connections between the poly-phase network and the  $I/Q$  VGA CG inputs. As a result, the dc currents of the CG transistors need to flow through the transformer network and are eventually terminated at the on-chip termination resistors of the isolation ports in the transformer

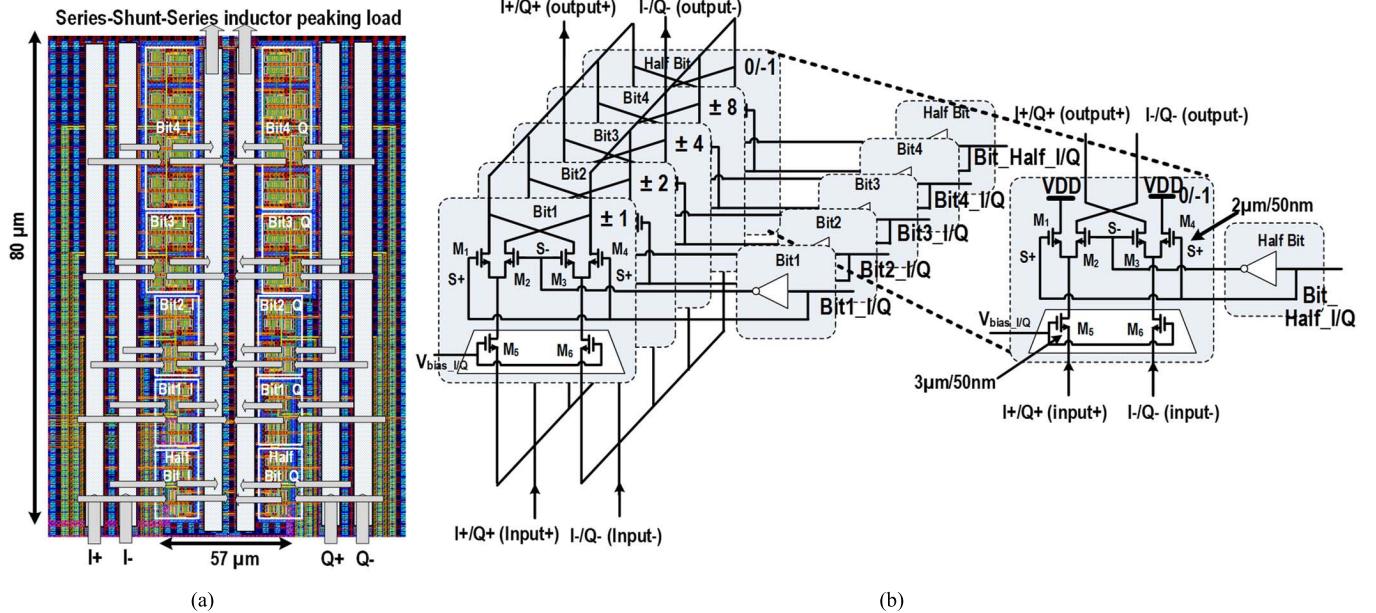


Fig. 9. (a) Layout and (b) schematic of the linear digital VGA.

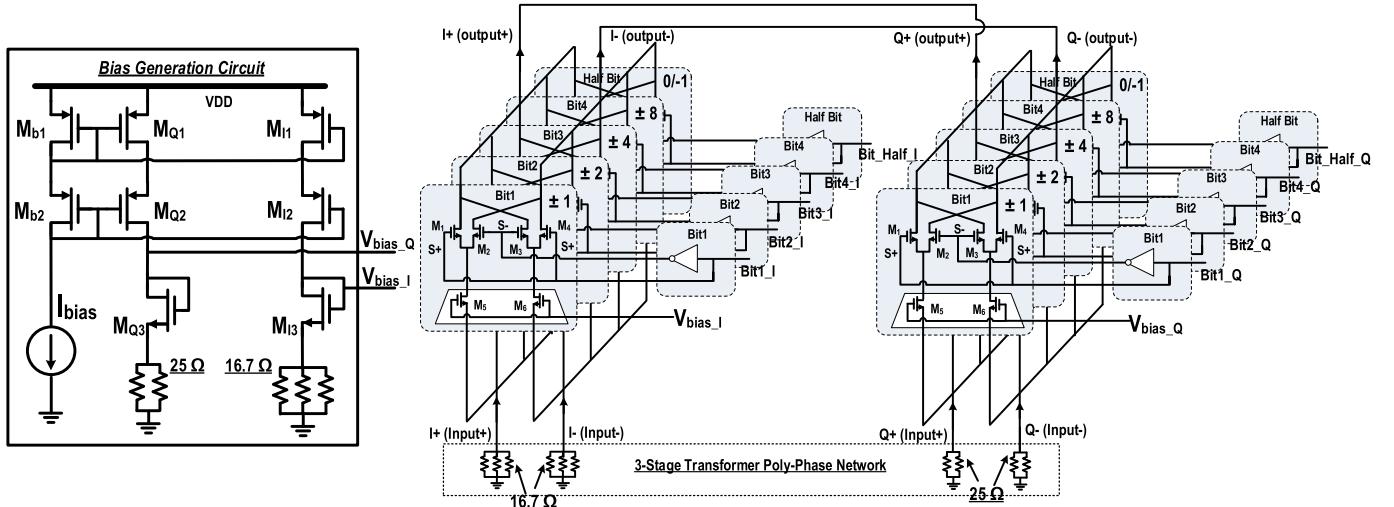


Fig. 10. Schematic of the bias generation circuit for I/Q VGAs.

$Q$  hybrids. Unlike conventional  $RC-CR$  poly-phase network, our transformer poly-phase network does not have resistors in the signal path, and the transformer coils behave as dc short with negligible ohmic resistance and dc voltage drop for the biasing.

The details on the biasing generation and connections are explained as follows. The source nodes of the  $I/Q$  VGA CG transistors are connected to differential  $I/Q$  outputs of the three-stage transformer poly-phase network (Fig. 2). Thus, the dc resistance at each poly-phase network output due to the on-chip termination resistors is critical for the dc biasing design. If we first examine the dc resistance looking into a transformer poly-phase unit stage (Fig. 5), each output has two parallel dc paths; one dc path is connected to the isolation termination 50-Ω resistor within this poly-phase stage, while

the other dc path is connected to the input of this poly-phase stage, i.e., the output of the previous poly-phase stage. For example, the output  $0^\circ$  ( $|I_N|e^{j0}$ ) is connected to the on-chip isolation termination 50-Ω resistor at the coupler A by its CPL-path and is also connected to the input  $90^\circ$  ( $|Q_{N-1}|e^{j\pi/2}$ ) by the THRU-path of the coupler B. Thus, if we cascade two transformer poly-phase unit stages, each four outputs has two isolation termination 50-Ω resistors connected in parallel. Moreover, for the first-stage transformer poly-phase network, i.e., an eight-port folded transformer  $Q$  hybrid (Fig. 3), the dc resistance looking into each  $I$ -path output ( $|I_1|e^{j0}$  or  $|I_1|e^{j\pi}$ ) is 50 Ω due to the termination resistors via the CPL-path. However, the impedance looking into each differential  $Q$ -path output ( $|Q_1|e^{j\pi/2}$  or  $|Q_1|e^{-j\pi/2}$ ) is dc connected to the differential inputs driven by two off-chip bias tees, which presents

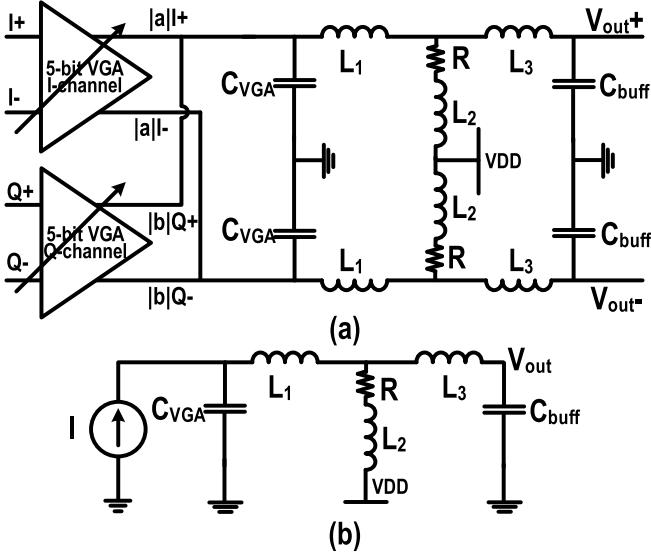


Fig. 11. Lumped element model of the (a) sixth-order series–shunt–series inductive peaking network for the  $I/Q$  VGAs' output current summing nodes and (b) equivalent half-circuits.

electrical open at dc. Thus, for the three-stage transformer poly-phase network, the total dc output resistance for the  $I+/I-$  output has three  $50\Omega$  resistors connected in parallel, i.e.,  $16.67\Omega$ , while the total dc output resistance for the  $Q+/Q-$  output has two  $50\Omega$  resistors connected in parallel, i.e.,  $25\Omega$ .

Since the  $I$ -path and  $Q$ -path CG VGAs exhibit different source dc resistance, their common-mode gate biasing voltages should be properly designed; this allows the  $I/Q$  VGA cells to have an equal biasing current density to ensure well matched  $I/Q$  weighting. Fig. 10 shows the bias generation circuit design. The reference bias current  $I_{bias}$  is mirrored to the cascode PMOS current source  $M_{II}/M_{I2}$  for the  $I$ -path biasing generation and cascode PMOS current source  $M_{Q1}/M_{Q2}$  for the  $Q$ -path biasing generation. Proper on-chip replica resistors are employed in the  $I/Q$ -current mirrors, i.e., three parallel connected  $50\Omega$  resistors for the  $I$ -path current mirror and two parallel connected  $50\Omega$  resistors for the  $Q$ -path current mirror. The diode-connected transistors  $M_{Q3}$  and  $M_{I3}$  are properly sized for the desired current density, and their gate voltages  $V_{bias\_I}$  and  $V_{bias\_Q}$  are then utilized to bias the common-mode input transistors in the  $I$ -path and  $Q$ -path VGAs, respectively. Thus, this biasing generation circuit ensures an equal biasing current density in the  $I/Q$  VGAs and thus well matched  $I/Q$  scaling.

### C. Series-Shunt-Series Inductive Peaking Load Network

The outputs of the two 5-bit VGAs are connected together for the output current summing (Fig. 9). Thus, the output summing nodes exhibit excessive capacitive loading, limiting the bandwidth of the PR. We employ a differential shunt-series-shunt inductive peaking network to substantially extend the bandwidth [20]. These schematics are shown in Fig. 11.  $C_{VGA}$  denotes the output parasitic capacitance of the  $I/Q$  VGAs (combined), while  $C_{buff}$  stands for the input parasitic

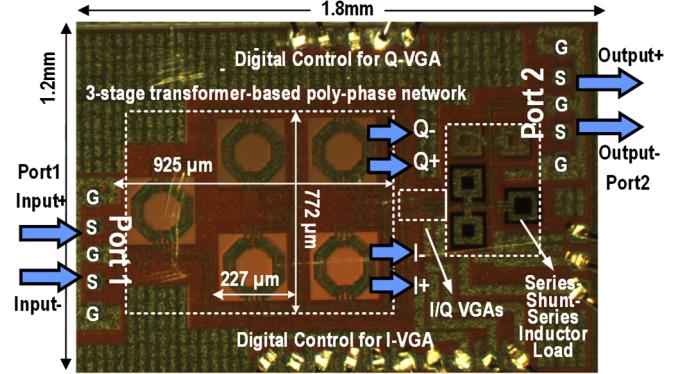


Fig. 12. Chip microphotograph of the vector modulator PR.

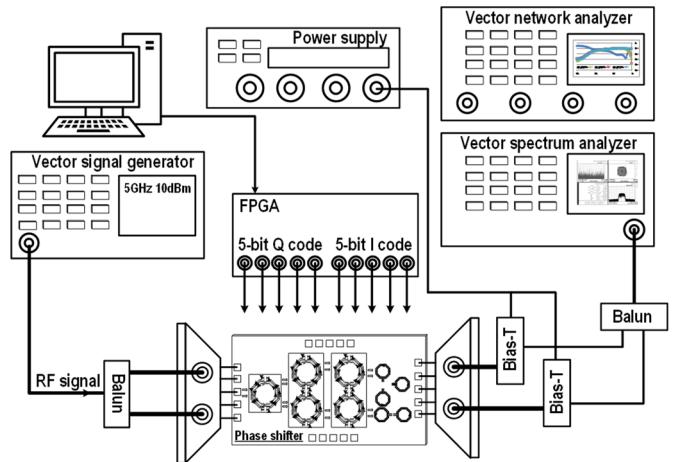


Fig. 13. Measurement setup for the four-port S-parameter and modulation.

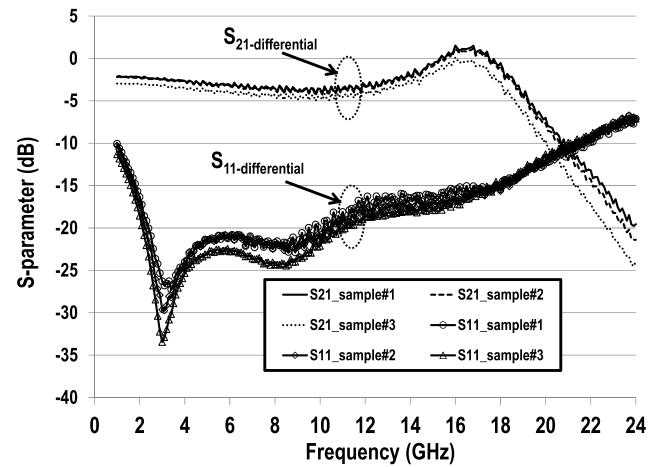


Fig. 14. Measured IL and input matching for three independent PR samples.

capacitance of the open-drain buffer. The half-circuit of this inductive peaking network consists of the  $C_{VGA}$ , a series inductor  $L_1$ , a parallel inductor  $L_2$  connected with a series load resistor  $R$ , a series inductor  $L_3$ , and  $C_{buff}$ , forming a sixth-order low-pass network. The transimpedance transfer function ( $V_{out}/I$ ) of this passive network is obtained by the

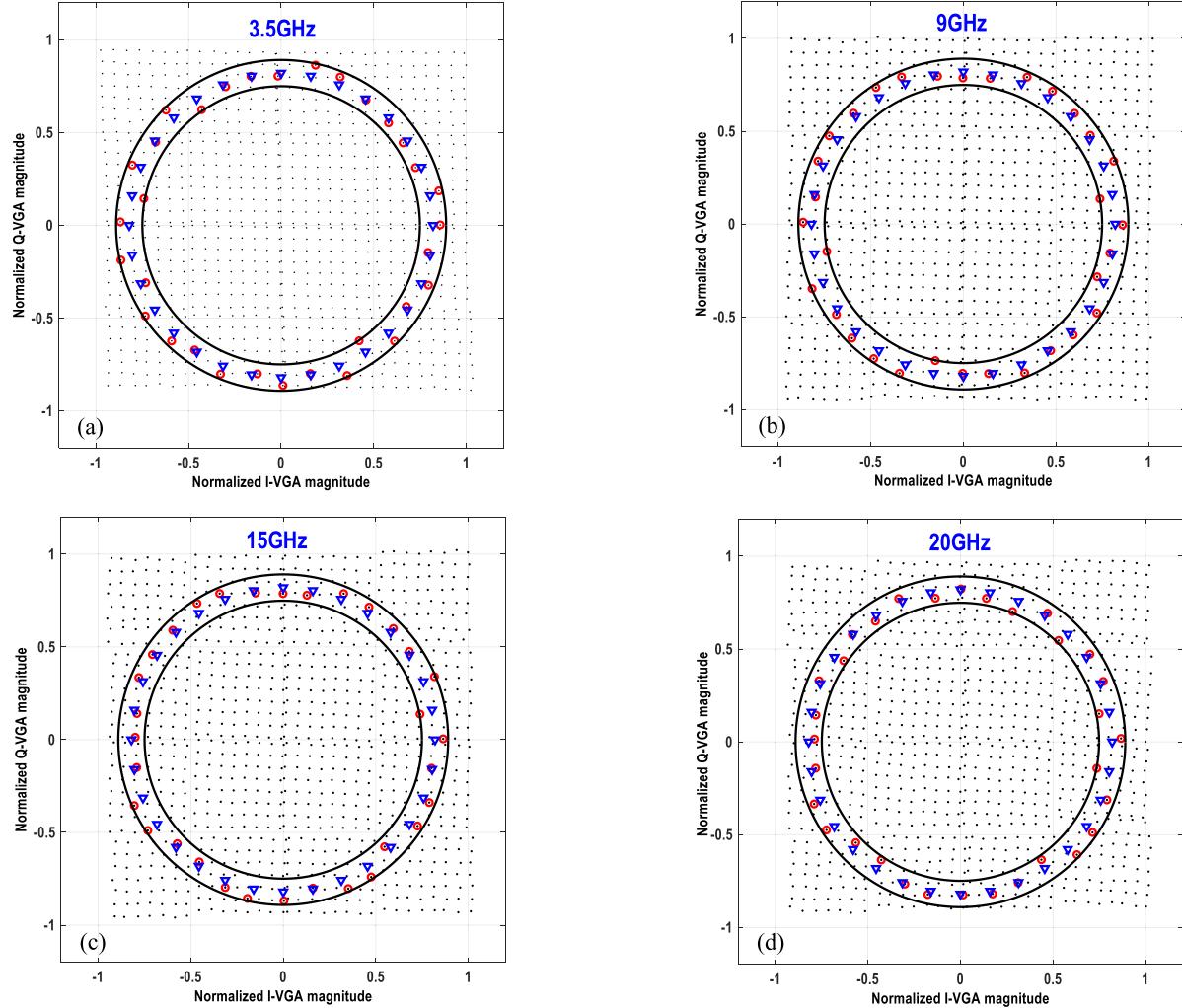


Fig. 15. Measured full 961 ( $31 \times 31$ ) phase interpolation points in normalized  $I/Q$  coordinate at (a) 3.5, (b) 9, (c) 15, and (d) 20 GHz. Red circles stand for the best matched interpolated phase points ( $11.25^\circ/\text{step}$ ) within a 1.5-dB magnitude variation, while the blue triangles highlight the ideal target phase interpolation point.

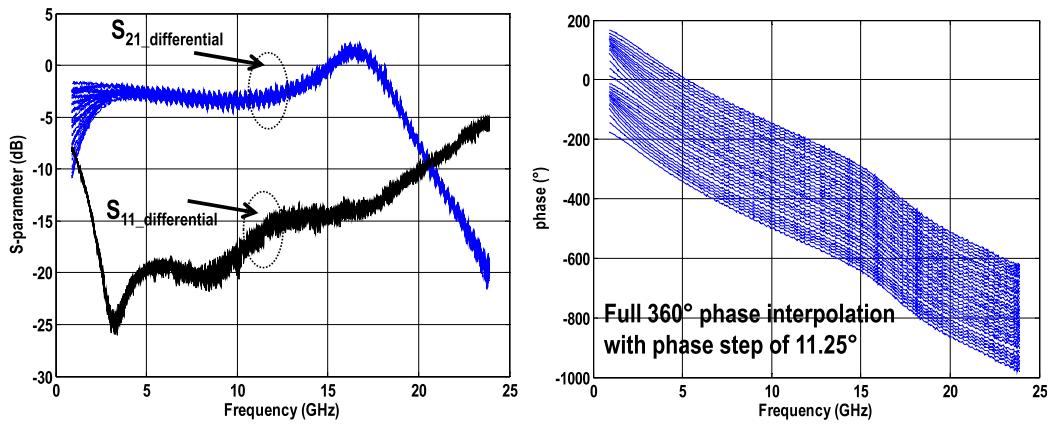


Fig. 16. Measured magnitude and phase responses for  $11.25^\circ/\text{step}$   $360^\circ$  full-span phase interpolations within a magnitude variation of 1.5 dB.

following equations:

$$\frac{V_{\text{out}}}{I} = \frac{a_3 S^3 + a_2 S^2 + a S + 1}{b_4 S^4 + b_3 S^3 + b_2 S^2 + b S + 1} \cdot \frac{1}{1 + c_2 S^2} \quad (1)$$

$$\frac{V_{\text{out}}}{I} = \frac{(S - z_1)(S - \bar{z}_1)(S - z_2)}{(S - p_1)(S - \bar{p}_1)(S - p_2)(S - \bar{p}_2)(S - p_3)(S - \bar{p}_3)} \quad (2)$$

$$a_3 = C_{\text{buff}} L_2 L_3 / R \quad (3)$$

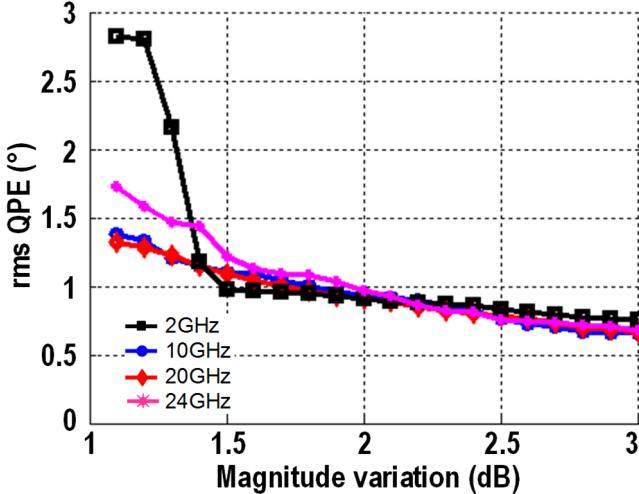


Fig. 17. Calculated QPEs versus magnitude variations at different frequencies based on the measured four-port S-parameters.

$$a_2 = C_{\text{buff}}L_3 \quad (4)$$

$$a_1 = L_2/R \quad (5)$$

$$b_4 = C_{\text{VGA}}C_{\text{buff}}(L_1L_2 + L_1L_3 + L_2L_3) \quad (6)$$

$$b_3 = C_{\text{VGA}}C_{\text{buff}}R(L_1 + L_3) \quad (7)$$

$$b_2 = C_{\text{VGA}}(L_1 + L_2) + C_{\text{buff}}(L_2 + L_3) \quad (8)$$

$$b_1 = R(C_{\text{VGA}} + C_{\text{buff}}) \quad (9)$$

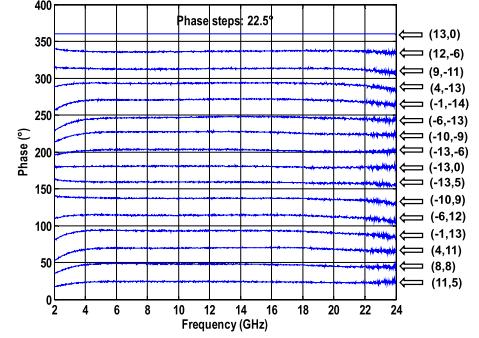
$$C_2 = L_3C_{\text{buff}}. \quad (10)$$

The sixth-order load network absorbs  $C_{\text{VGA}}$  and  $C_{\text{buff}}$  and allows for a substantial bandwidth extension by carefully placing the poles and zeroes of the inductive peaking load network. The simulated magnitude response of the three-stage transformer poly-phase network has its amplitude peak value at 5.7 GHz with a gradual magnitude roll-off at higher frequencies (Fig. 8). With the shunt-series-shunt inductive peaking load network compensation, the total 3-dB magnitude bandwidth of the PR is from 2.6 to 22.6 GHz, covering a decade-wide bandwidth. The selected passive component values are  $L_1 = 345$  pH,  $L_2 = 235$  pH,  $L_3 = 345$  pH, and  $R = 40 \Omega$  while the capacitance of  $C_{\text{VGA}} = 200$  fF and  $C_{\text{buff}} = 105$  fF.

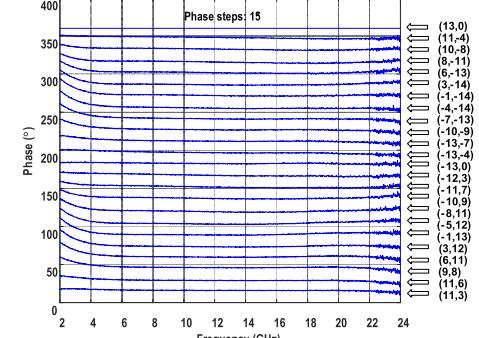
## V. MEASUREMENT RESULTS

The proposed PR is implemented in a standard 65-nm CMOS process with a very compact chip area of 1.2 mm × 1.8 mm (Fig. 12). The three-stage transformer poly-phase network occupies a chip area of 772 μm × 925 μm. Each transformer poly-phase unit stage takes 227 μm × 772 μm, and the eight-port folded transformer  $Q$  hybrid is 227 μm × 227 μm. The design consumes 46 mA from 2-V supply voltage excluding the open-drain buffer.

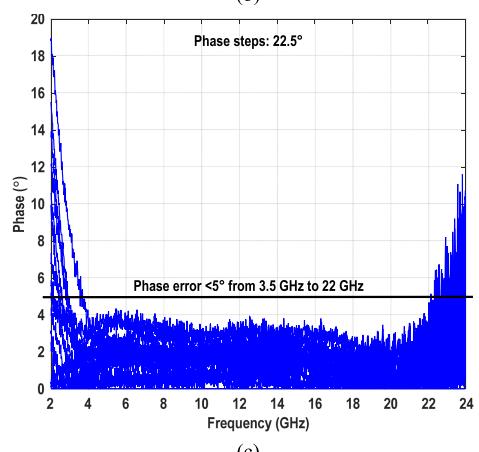
First, the amplitude response of the PR is characterized by a four-port vector network analyzer (Rohde & Schwarz ZVA 24) with full four-port S-parameters measurements (Fig. 13). The measured magnitude response of three independent samples is



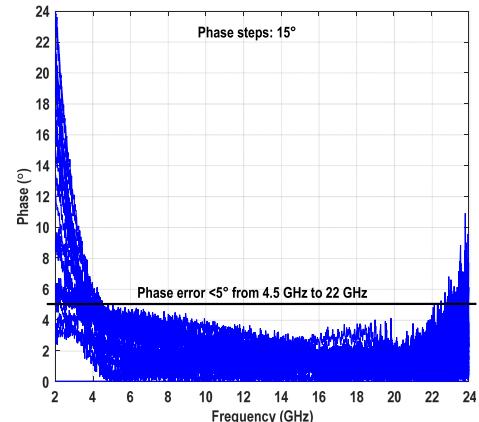
(a)



(b)



(c)



(d)

Fig. 18. Measured full-span 360° phase interpolation results for (a) 22.5°/step and (b) 15°/step versus the frequency and the calculated phase interpolation error for (c) 22.5°/step and (d) 15°/step phase interpolations.

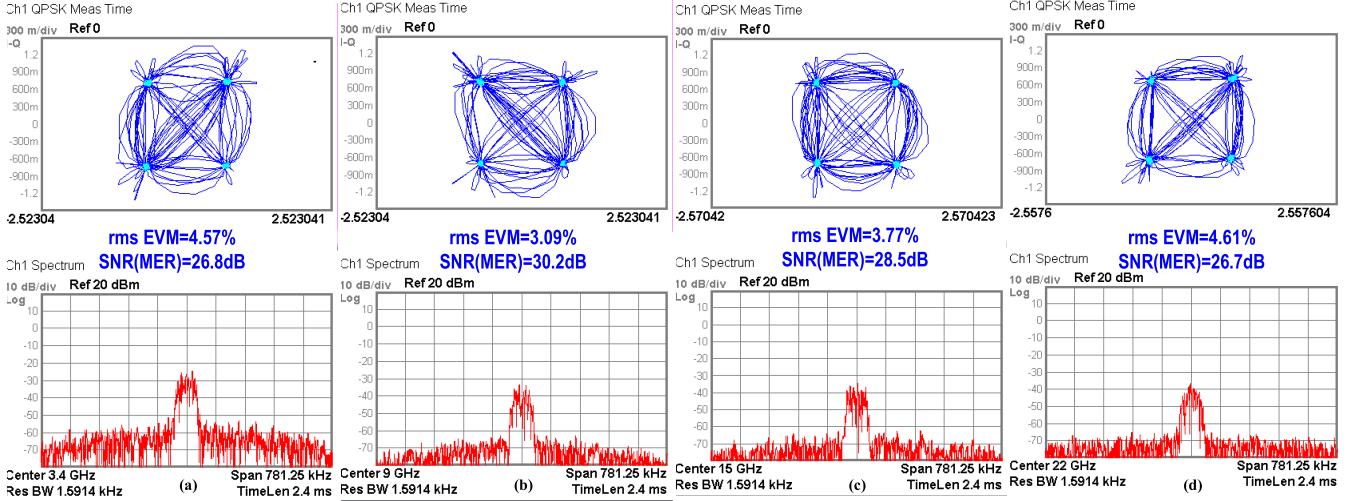


Fig. 19. Modulation for 50-KSym/s QPSK at (a) 3.4, (b) 9, (c) 15, and (d) 22 GHz by frequency-independent phase interpolation code settings.

shown in Fig. 14. The  $I/Q$  VGAs amplitude code setting of  $(I, Q) = (+15, 0)$  is used. The  $-3$ -dB magnitude bandwidth is up to 19 GHz, and the input matching is  $< -10$  dB from 1 to 21 GHz. The consistent and repeatable measurement results of three independent samples demonstrate an ultra-wide PR bandwidth and robustness against the sample-to-sample variations.

Next, the phase interpolation performance is evaluated using the four-port S-parameters measurements. The complete  $31 \times 31$  ( $-15$  to  $+15$  for  $I/Q$  VGAs) Cartesian phase interpolation points are measured, covering the full  $360^\circ$  phase span with 961 interpolation points. Fig. 15 shows the measured full 961 phase interpolation points in the normalized Cartesian plane at 3.5, 9, 15, and 20 GHz, demonstrating well-balanced  $I/Q$  signal generation and highly linear  $I/Q$  VGA operations over a very wide frequency range. For a full-span  $360^\circ$  phase interpolation at  $11.25^\circ/\text{step}$ , the best matched interpolation points within  $1.5$ -dB magnitude variation are highlighted in red circles, while the ideal target interpolation points are highlighted in blue triangles. Fig. 16 summarizes the measured output magnitude and phase response for  $11.25^\circ/\text{step}$   $360^\circ$  full-span phase interpolations within a magnitude variation of  $1.5$  dB, showing accurate phase interpolation over a very wide frequency span. The input matching is  $< -10$  dB from 1 to 21 GHz. Note that both the input matching and the PR gain exhibit consistent responses independent of the phase interpolation settings.

In practical phased-array applications, the target phase can be arbitrary over the  $360^\circ$  full span. When a digital PR tries to synthesize an arbitrary target phase using discrete phase interpolations, a quantization phase error (QPE) can be defined as the difference between the target and the interpolated phases. The measured rms QPEs versus the magnitude variations at different operating frequencies are shown in Fig. 17. As the allowed magnitude variation is relaxed, more phase interpolation points on the Cartesian plane can be employed for the target phase interpolation, lowering the measured rms QPEs accordingly (Fig. 17). Within a  $1.5$ -dB magnitude variation,

the PR achieves rms QPEs less than  $1.22^\circ$  from 2 to 24 GHz for interpolating an arbitrary phase in the  $360^\circ$  full phase span, achieving the first-ever high-quality phase interpolation over a one-decade bandwidth. In addition, for a PR, its bandwidth supporting high-quality phase interpolation is generally more critical than its  $-3$ -dB magnitude bandwidth. This is because the latter can be recovered by bandwidth extension techniques, such as staggered tuning, without affecting the phase interpolation results.

Moreover, because the transformer poly-phase network generates highly matched  $Q$  signals over a one-decade bandwidth (Fig. 8), and the  $I/Q$  VGAs perform accurate  $I/Q$  scaling also across a decade-wide bandwidth, one should expect that our PR design can achieve high-precision  $360^\circ$  full-span phase interpolations using frequency-independent code settings without any frequency-dependent code or LUT. This “one-code” for all frequencies performance is evaluated and demonstrated next. The measured  $360^\circ$  full-span phase interpolations with  $22.5^\circ$  or  $15^\circ$  phase steps over a frequency range from 2 to 24 GHz are shown in Fig. 18. Note that a constant  $I/Q$  VGAs’ code setting is used for each phase interpolation across the entire frequency range. Figs. 18(c) and 19(d) show that the measured maximum phase error is less than  $5^\circ$  over an ultra-wide-frequency range from 3.5 and 4.5 to 22 and 22 GHz. An ideal  $I/Q$  VGA gain setting per a target phase is  $\tan^{-1}(Q/I)$ . However, we implemented 5-bit  $I/Q$  VGAs and there is a quantization error. We utilize measured phase interpolation points within the amplitude variation of  $1.5$  dB among a full 961 constellation, as shown in Fig. 15. This is a first-ever reported Cartesian vector modulator PR that can perform high-precision phase interpolation with “one-code” for all the operating frequencies over a decade-wide bandwidth. Without using any frequency-dependent code sets/LUT, tunable elements, or band-selection switches, this unique PR performance will substantially simplify the system-level design in ultrabroadband and frequency-agile phased arrays.

Since this PR design can also serve as a Cartesian  $I/Q$  modulator, its modulation performance is thus evaluated next using

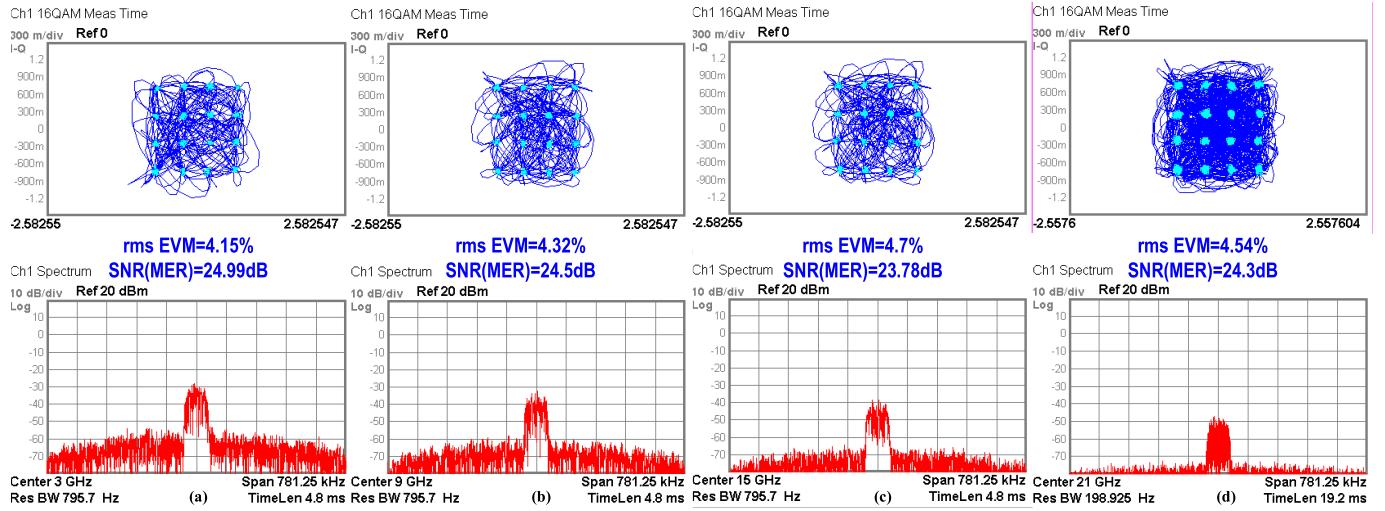


Fig. 20. Modulation for 50-KSym/s 16-QAM at (a) 3, (b) 9, (c) 15, and (d) 21 GHz by frequency-independent phase interpolation code settings.

TABLE I  
COMPARISON OF THE STATE-OF-THE-ART VECTOR MODULATOR PRS<sup>†</sup>

	Frequency (GHz)	Relative BW	Resolution (bit)	RMS Phase Error	Frequency-Dependent LUT	Quadrature Generation Type	Tech	DC Power Consumption (mW)
This work	2-20	1:10	10	<1.22°	No	Transformer-Based Poly-Phase Filter	65 nm CMOS	9.2
[8]	20-27	1:13	10	<1.22°	Yes	Folded Transformer-Based Quadrature	90 nm CMOS	10
[15]	5-18	1:3.6	8	<1.22°	Yes	Quadrature All-Pass Filter	130 nm CMOS	8.7
[16]	15-35	1:2.3	4	<1.22°	-	RC-CR Poly-Phase Filter + Inductor	180 nm CMOS	25.2
[21]	2.3-4.8	1:2.1	Analog	<1.22°	Yes	Modified Quadrature All-Pass Filter	180 nm CMOS	19.1
[22]	2-3	1:1.15	Analog	<1.22°	Yes	Active Balun + OTA	180 nm CMOS	24

<sup>†</sup>This comparison table only includes the vector-modulator phase-rotator designs with quadrature signal generation network.

QPSK and 16-QAM signals. The setup is shown in Fig. 13. The QPSK and 16-QAM signals are first synthesized in ADS and are digitized to the 10-bit *I/Q* amplitude codes. The 10-bit *I/Q* digitized codes are then sent to the PR as the *I/Q* VGAs' control codes by a field-programmable gate array (FPGA). A continuous-wave RF input differential signal is generated by a signal generator (Keysight E8267D) and an off-chip balun (Krytar 4010180 or 4060265). The PR then performs *I/Q* vector modulation on the input RF carrier by setting the *I/Q* VGA amplitude codes. A spectrum analyzer (Keysight N9010A) is used to demodulate the complex QPSK or 16-QAM signals from the PR output. In this set of experiments, a fixed VGA code setting is used for each phase interpolation point across the carrier frequencies, so no frequency-dependent VGA code optimization/LUT is used.

The measured rms error vector magnitude (EVM) values for the 50-KSym/s QPSK signal are 4.57% at 3.4 GHz, 3.09% at 9 GHz, 3.77% at 15 GHz, and 4.61% at 22 GHz, respectively (Fig. 19). The measured rms EVMs for the 50-KSym/s 16-QAM signal are 4.15% at 3.0 GHz, 4.32% at 9 GHz, 4.7% at 15 GHz, and 4.54% at 21 GHz, respectively (Fig. 20). Fig. 21 summarizes the measured rms EVM values for QPSK and 16 QAM at different carrier frequencies. The measured rms EVM values for QPSK are all below 5% from 3.3 to

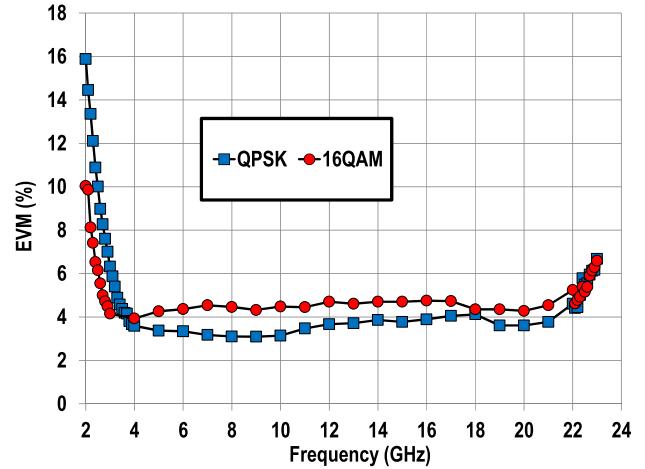


Fig. 21. Modulation summary for the 50-KSym/s QPSK and 16-QAM signals.

22.3 GHz, while the measured rms EVM values for 16 QAM are all below 5% from 2.7 to 22 GHz. The modulation speed is limited by the measurement setup, and the phase and amplitude errors of the off-chip baluns are within  $\pm 12^\circ$  and  $\pm 0.7$  dB, which degrade the measured rms EVMs. These

modulation measurements demonstrate that the proposed PR can perform high-performance *I/Q* vector modulation with frequency-independent VGA settings.

Performance comparison with reported fully integrated vector modulator PRs (with *I/Q* generation networks) is shown in Table I. Our design demonstrates its superior phase interpolation performance over a first-ever one-decade bandwidth (2–20 GHz) without frequency-dependent code optimization/LUT, tunable element, or band-selection switch.

## VI. CONCLUSION

This article presents a differential vector modulator PR performing 360° full-span interpolation. Implemented in a standard 65-nm CMOS process, the PR contains a three-stage transformer poly-phase network, digitally linear ultrabroadband *I/Q* VGAs, and a shunt-series-shunt inductive peaking load network. The 360° full-span phase interpolation measurements demonstrate measured rms QPEs less than 1.22° from 2 to 24 GHz within 1.5-dB magnitude variation. The modulation tests with QPSK/16-QAM signals demonstrate measured rms EVMs below 5% from 3.3 to 22 GHz. The proposed PR achieves superior phase interpolation over a first-ever one-decade bandwidth without any frequency-dependent code optimization/LUT, tunable element, or band-selection switch, providing a unique “one-code” for all frequencies solution.

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