A 6-bit CMOS Active Phase Shifter for *Ku*-Band Phased Arrays

Zongming Duan, Yan Wang, Wei Lv, Yuefei Dai, and Fujiang Lin, *Senior Member, IEEE*

***Abstract*— A 6-bit high-accuracy active phase shifter is developed in 0.13-μm CMOS technology for *Ku*-band phased arrays. Improved transformer balun with wriggly stub is applied to split the single input to differential and achieve high balance with reduced chip area. Two-stage polyphase filter (PPF) generates broadband I/Q signals with high accuracy. A main digital-to-analog convertor (DAC) controls the I/Q amplitude to achieve 6-bit phase resolution, while an auxiliary DAC compensates the amplitude/phase error introduced by balun and PPF. Consequently, high resolution along with low phase/gain error can be achieved. The phase shifter shows measured rms phase error of <4° at 12–18 GHz and <3° at 13–18 GHz. The measured mean gain is −2.5–1 dB, and the rms gain error is <0.9 dB at 12–18 GHz. The total power consumption is 37.5 mW, and chip size is 0.75 × 0.32 mm^2 excluding pads.**

***Index Terms*— Active phase shifters, CMOS integrated circuits, passive balun, phased arrays, polyphase filter (PPF).**

I. Introduction

PHASE shifters are an essential component for beaming-steering in phased array systems. For this application, high resolution and high accuracy are necessary for better beam performance, and implementation in CMOS technology is preferable for low-cost requirement [1], [2]. Different types of phase shifter topologies are suitable for the integrated circuit design including passive topology such as *LC*-based circuit [3], [4], [7], active topology such as quadrature all-pass filter (QAF)-based [5], [6], and the others [8]. Compared with the passive designs, active phase shifters can achieve a high integration level with decent gain and accuracy along with a small chip size.

Recently, higher resolution and accuracy are needed for the phase shifters due to high beam resolution in phased arrays, whereas previous works are mainly sub-6-bit (such as 4-bit in [2], [5], and [7] and 5-bit in [3] and [6]), and also with accuracy limited (3°–10° at *Ku*-band typically). QAF-based architecture is widely applied but it suffers from the capacitance loading effect [5], [6]; therefore, it is difficult to achieve high accuracy along with broadband operation. For high-resolution and high-accuracy design, phase/amplitude error introduced by input balun and quadrature networks (2°–4°/1 dB at *Ku*-band typically), along with the other circuits, should take into account carefully. Therefore, in this letter, an improved transformer balun is applied to split the single input to differential and two-stage polyphase filter (PPF) generates broadband I/Q signals, while the phase/gain error in the output of the PPF is compensated by an auxiliary digital-to-analog convertor (DAC), and consequently high resolution and low phase/gain error can be achieved.

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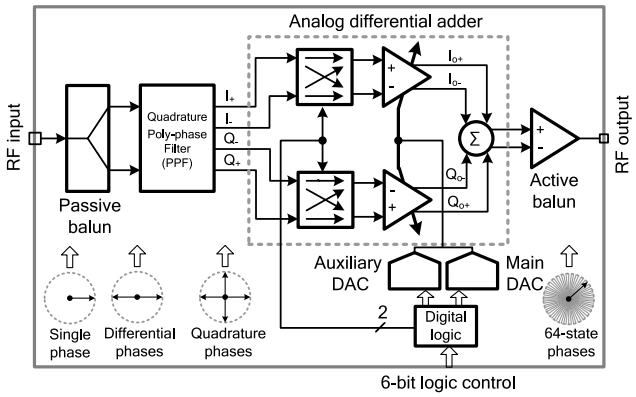

Fig. 1. Block diagram of the proposed active phase shifter.

II. Circuit Design

The block diagram of the proposed phase shifter is shown in Fig. 1. An on-chip passive balun is applied to split the single input to differential, then a second-order PPF is used to generate differential I/Q signals. An analog differential adder, composed of two Gilbert-cell signed variable gain amplifiers (VGAs), adds the I- and Q-outputs of the PPF with proper amplitude and polarities, achieving output signal with a synthetic phase of $\tan^{-1}(Q_{o\pm}/I_{o\pm})$ and amplitude of $\sqrt{(Q_{o\pm}^2 + I_{o\pm}^2)}$. Bit 5 and bit 4 of the 6-bit control logic are used to select the sign of the $I_\pm$ and $Q_\pm$. The 4-bit main DAC takes the role of controlling the bias current of the VGAs, as presented in [5] and [6]. To compensate the phase/gain error induced by the input balun and PPF, an auxiliary 2-bit DAC is applied to add additional current to the VGAs. Therefore, 64-bit phase shifting can be achieved.

The detail schematic of the proposed phase shifter is shown in Fig. 2. A transformer balun with center open stub, presented in [9] previously, is applied to transfer the single input to differential. The center open stub is used to optimize phase and amplitude imbalance, while in *Ku*-band the stub is excessively long leading to increased chip area. In this design, wriggly stub is used by two metals through vias (Fig. 3) to minimize the chip area. Electromagnetic simulations show that phase error of <2°, and amplitude error of <1 dB can be achieved. In addition, a well input match can also be achieved without additional matching component benefit from the configuration of balun followed with PPF.

In [5] and [6], QAFs are applied for quadrature signal generation. Although QAF can achieve decent performance of

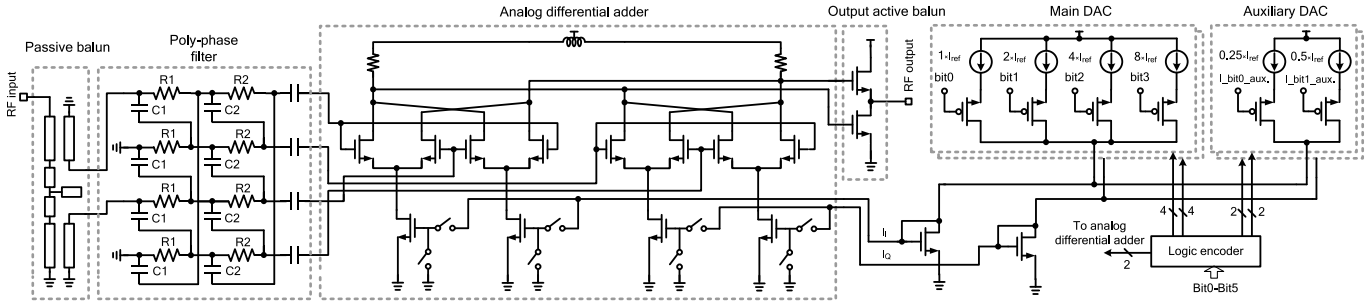

Fig. 2. Circuit schematic of the proposed active phase shifter.

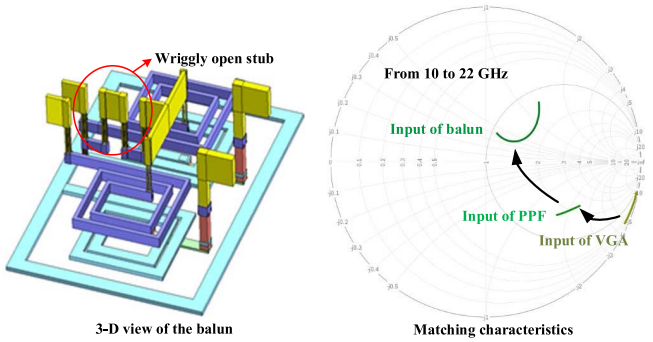

Fig. 3. Proposed transformer balun and input matching optimization scheme.

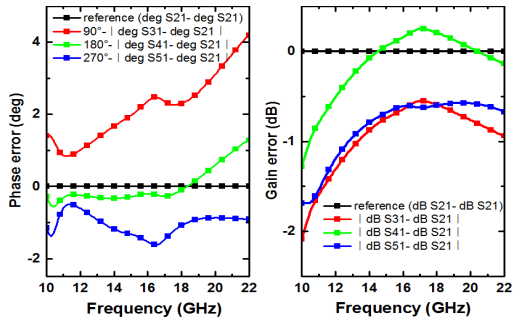

Fig. 4. Simulated phase/gain error of the I/Q signals.

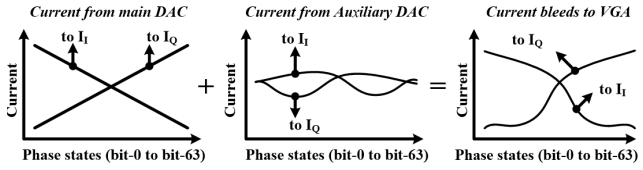

Fig. 5. DAC calibration for the 6-bit phase/gain responses.

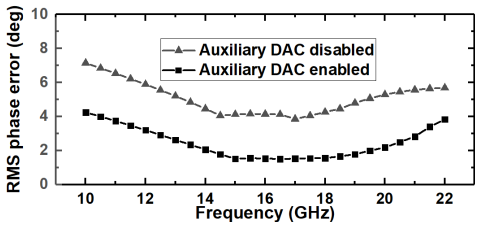

Fig. 6. Simulated phase error when auxiliary DAC enabled or not.

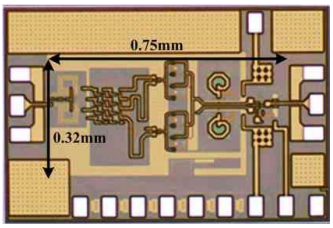

Fig. 7. Chip microphotograph of the 6-bit phase shifter.

voltage gain, bandwidth, and phase error, it suffers from the capacitance loading effect especially in high frequency [5]. Therefore, in this design, two-order RC PPF is used with optimized values of $R_1/C_1 = 78\Omega/83$ fF and $R_2/C_2 = 122\Omega/107$ fF. It can achieve identical relative bandwidth with QAF, while it is not sensitive to the capacitance loads.

The imbalance of the balun along with the quadrature mismatch of the PPF will introduce the I/Q error in the output of the PPF. Fig. 4 shows the simulated phase/gain error of the I/Q signals. $S_{21}/S_{31}/S_{41}/S_{51}$ presents the transfer characteristics of the PPF with input balun, respectively. The phase error will achieve 0.8°–2.8° at 90° vector and 0.5°–1.8° at 270° vector from 12 to 18 GHz. The gain error will achieve 0.7–1.6 dB at 90° vector and 0.7–1.5 dB at 270° vector from 12 to 18 GHz. Although the phase error may be optimized by choosing suitable values of $R_1/C_1/R_2/C_2$, the gain error may turn to worse.

An auxiliary DAC is applied to compensate the phase/gain error introduced by balun and PPF (Fig. 2). As shown in Fig. 5, the main DAC acts as a simple linear current supplier, and the auxiliary DAC provides compensation current which value is optimized due to the phase/gain error in the output of the PPF. In addition, phase/gain error caused by nonideal of the circuit such as layout asymmetry can also be compensated. Consequently, high resolution and low phase/gain error can be achieved. Simulations show that the rms phase error could be improved 2.5° typically (Fig. 6).

Analog differential adder which adds the I- and Q-outputs from the PPF synthesizes the required phase. An inductor load is used in it to achieve wideband frequency operation.

III. Measurement Results

The proposed 6-bit active phase shifter is fabricated in 0.13-μm CMOS technology. Fig. 7 shows the die photograph. The chip size is 0.95 mm × 0.6 mm with pads included and 0.75 mm × 0.32 mm excluding pads. The chip is tested with on-chip probing. With a supply voltage of 2.5 V, the power consumption is about 37.5 mW.

Fig. 8 shows the measured S-parameter of the phase shifter. The mean S_{21} of 64-state is −2.5–1 dB, and the peak-to-peak gain variations are $\leq \pm 1.1$ dB at 12–18 GHz. The input return loss (S_{11}) is <-8 dB at 12–18 GHz and <-10 dB at 14–18 GHz. The output return loss (S_{22}) is <-8 dB at

TABLE I
COMPARISON OF RECENT PHASE SHIFTERS

Ref.	Method	Reso.	Frequency (GHz)	RMS phase error (°)	RMS gain error (dB)	S21 (dB)	Die area (mm^2)	P_{DC} (mW)	Technology
[3]	Switch-LC	5-bit	57~66	4~8	0.18~0.25	-16~ -18.5	0.44	N/A	65-nm CMOS
[5]	QAF-based	4-bit	6~18	3~10	0.5~1.7	-2.1~ -0.2	0.45	8.7	0.13-μm CMOS
[6]	QAF-based	5-bit	6~18	2.8~5.6	0.75~1.1	16.5~19.5	0.9	61.67	0.18-μm SiGe
[8]	Vector sum	Cont.	20.5~26.5	2 typ.	N/A	-4~ -1	0.12	10	90-nm SiGe
This work	**PPF-based**	**6-bit**	**12~18**	**1.8~4**	**0.6~0.9**	**-2.5~1**	**0.57**	**37.5**	**0.13-μm CMOS**

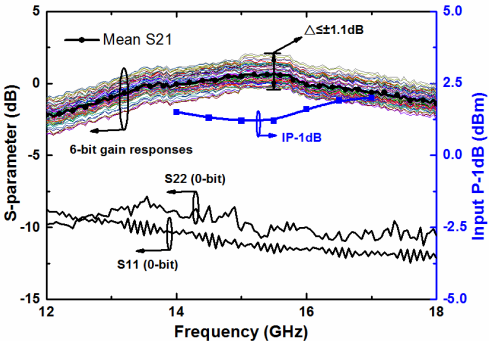

Fig. 8. Measured 6-bit gain responses and impedance.

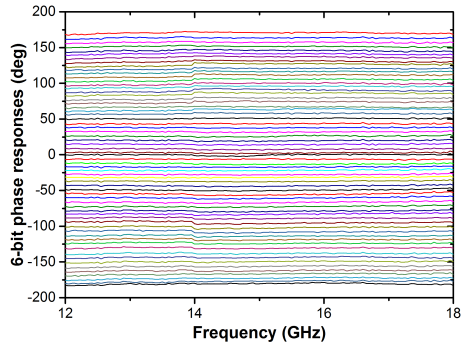

Fig. 9. Measured 6-bit phase responses of the phase shifter.

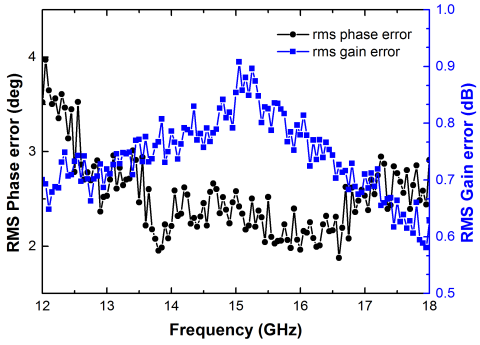

Fig. 10. Measured rms phase/gain error of the phase shifter.

12–18 GHz and <-10 dB at 15–18 GHz. The input P -1 dB is 2 dBm typically.

Fig. 9 shows the measured 6-bit phase responses of the phase shifter. The phase shifter demonstrates wideband phase shifting performance with small phase variations duo to the proposed design technique.

Fig. 10 shows the measured rms phase/gain error of the phase shifter. With reference to 0-bit, the rms phase error and gain error are defined as the same in [5]. The phase shifter $-4°$ rms phase error at 12–18 GHz, while 1.8°–3° at 13–18 GHz. The rms gain error is 0.6–0.9 dB at 12–18 GHz.

Table I summarizes and compares the performance of the proposed phase shifter with recently published *x*- and *Ku*-band silicon-based phase shifters in terms of various respects. To the authors' best knowledge, this 6-bit phase shifter achieves the lowest rms phase error and gain error with 40% relative bandwidth in silicon process, due to the proposed design techniques.

IV. CONCLUSION

This letter presents a 6-bit active phase shifter integrated with all digital control circuitry developed in 0.13-μm CMOS technology. On-chip transformer balun and PPF-based quadrature network are applied, and the phase/gain errors introduced by balun and PPF are compensated by additional adjust circuitry. The phase shifter achieves very low phase error and gain error at 12–18 GHz, with decent gain, input/output return loss, power consumption, and chip area. The results demonstrate its potential to be a low-cost and high-accuracy phase shifter for *Ku*-band phased array systems.

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