A 6-bit Active Phase Shifter for Ku-Band Phased Arrays

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***Abstract*—This paper presents a 6-bit active phase shifter in 0.13-µm SiGe BiCMOS technology for Ku-band phased arrays based on a phase interpolation technique. An input Marchand balun and a RC poly phase filter are used for high I/Q accuracy wideband quadrature generation with high linearity and an integrated current-mode DAC is used for controlling the amplitude of I/Q path signal to achieve 6-bit phase resolution. The phase shifter operates in the 12-18 GHz range. The simulation results show an rms phase error less than 2.61°. The average insertion gain ranges from -11.16 dB to -20.39 dB with an rms gain error less than 0.4 dB for 64 phase states. The phase shifter achieves an input P1dB of 9.98 dBm at 16 GHz for 0°-phase state. The core area of the phase shifter is 1.1×0.9 mm2, with a total current consumption of 13.4 mA from a 3.3 V supply voltage.**

Keywords—Active phase shifter, phased arrays, poly phase filter, Ku-band

I. INTRODUCTION

Phased array systems have been widely used in various tactical radars to achieve space beam forming and fast beam scanning [1]. Electronic phase shifter (PS) which varies the insertion phase of each received signal from antenna to compensate the path difference of free space is an essential part for phased-arrays. The insertion loss, phase shift accuracy and switching time of the phase shifter have a decisive influence on the performance of the phased array system.

Phase shifters can be implemented using passive or active components. Passive components such as true or synthetic transmission lines [2], lumped hybrid-couplers with reflection loads [3] or switches low-pass/high-pass passive networks [4] can achieve high linearity and low power consumption while with high loss, a large size and a narrow bandwidth. In [5], a passive 6-bit phase shifter employing switched LC topology is proposed with a simulated RMS phase error of < 2° and an RMS gain error of < 0.5 dB. However, the frequency bandwidth is only 8.5-10 GHz. On the other hand, active phase shifters [6]-[8] can achieve a decent phase shift accuracy with a certain gain and a high integration level under a constrained power budget. Most active phase shifters generate various phases using the phase interpolation method. In [6], an active 5-bit phase shifter using vector sum technology is presented with a measured power gain of 19.5 dB at 12 GHz. The RMS gain error is < 1.1dB and the RMS phase error is < 5.6° at 6-18 GHz. However, the linearity of the phase shifter is limited with the output P1dB of only -20~-17 dBm for 0°-bit phase state at 12 GHz. Thus, it is not suitable for relatively high power application, such as transmitters.

In this paper, a 6-bit (phase quantization level = 5.625°) active phase shifter to be integrated on-chip with multiple phased arrays for K*u*-band (12-18 GHz) applications is designed in IBM8HP 0.13-µm SiGe BiCMOS technology. Section II describes the architecture of the phase shifter in detail and section III presents more specific circuit level description of the building blocks. The results and comparison are discussed in section IV. Section V is the conclusion.

II. ACTIVE PHASE SHIFTER ARCHITECTURE

The architecture of the active phase shifter is shown in Fig. 1. The underlying principle of this architecture is a signal synthesis by combination of two amplitude-adjustable orthogonal vector signals to change the phase and the amplitude of the signal at the same time. The input signal is first divided into differential signals by an input balun and then split into quadrature phased I- and Q-vector signals using a poly phase filter (PPF). The differential adder where the quadrature signals are added with proper amplitude weight and polarities according to the required phase is composed of two Gilbert-cell type signed-VGAs, giving a polarity modulated output signal with a synthetic phase of $\angle\tan^{-1}\left(A_{Q_o\pm}/A_{I_o\pm}\right)$ and magnitude of $\sqrt{A_{Q_o\pm}{}^2+A_{I_o\pm}{}^2}$. Where $A_{Q_o\pm}$ and $A_{I_o\pm}$ refer to the amplitude of the signal $Q_o\pm$ and $I_o\pm$ respectively. For 6-bit phase resolution, a digital-to-analog converter (DAC) is used to control the bias current of each VGA to change the gain of the VGAs differently corresponding to different amplitude weighting requirements of each input of the adder. Also, the I/Q amplitude mismatch in the I/Q generator can be compensated by adjusting the I- and Q-path gains accordingly. This can result in a robust design against process, supply voltage and temperature. The sign change of each I/Q input of the adder is done by the control logic which also provide the control bits to DAC. The balun (differential-to-single) is also placed at the output port to provide a single-ended 50Ω interface to the measurement system.

III. CIRCUIT DESIGN

The detailed schematic of the active phase shifter is shown in Fig. 2.

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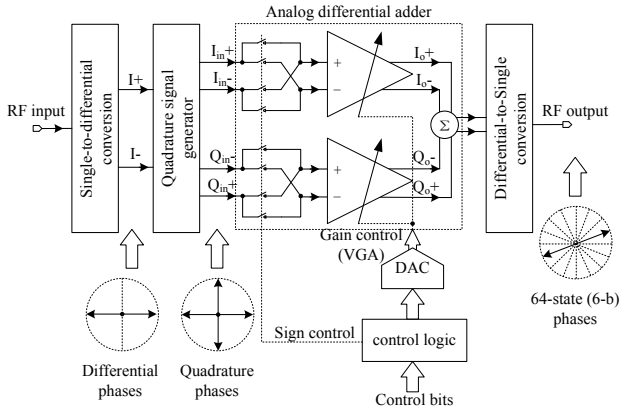

Fig. 1. Architecture of the active phase shifter.

A. Input Marchand balun

In order to bring high linearity to phase shifter, the input balun is realized with a passive Marchand balun, which is optimized with a center open stub to obtain low insertion loss and low phase imbalance in a broadband frequency range [9]. Fig. 3 shows the block diagram of the proposed Marchand balun, which consists of two identical coupled-line sections, an interconnected line and a center open stub with electrical length of λ=2400 μm , λ_θ=180 μm , λ_φ=115 μm respectively. SPECTRE simulations show that the Marchand balun provides peak values of 6.38 dB insertion loss, 0.56 dB amplitude imbalance and 2.21° phase imbalance at 12-18 GHz.

B. Poly phase filter (PPF)

Previously, an LC configuration was used to generate orthogonal signals with low phase error and low insertion loss. However, when loaded with capacitive or inductive loads, the generated vectors using this configuration cannot achieve low phase and amplitude imbalance. Thus, a poly phase RC filter is used in this design to generate the required quadrature signals (0°, 90°, 180°, 270°) for its small size and low phase and amplitude error with loads, despite of relatively high insertion loss. The poly phase RC filter is implemented in grid configuration with the resistors and capacitors located in grid and crossing paths implemented across the lattice [10], as shown in Fig. 2. A two stage poly phase RC filter is chosen to cover the desired bandwidth with acceptable amplitude imbalance. For the first stage, R_1=100 Ω and C_1=113 fF are chosen for mid-band operation at 14 GHz. For the second stage, R_2=100 Ω and C_2=99.5 fF are chosen for mid-band operation at 16 GHz. SPECTRE simulations show that the I/Q phase error is $\Delta\theta \leq$ 6.7° at 12-18 GHz with an I/Q amplitude error of $\Delta A \leq$1.1 dB.

C. Differential adder (I/Q VGAs)

The core of the phase shifter is the analog differential signed-adder, which is composed of two Gilbert cells for the addition of the V-I converted I/Q input signals from the PPF in the current domain at the output node to synthesize the required phase with consistent amplitude. The variable gain function is done by changing the tail currents I_{IB} and I_{QB} of I- and Q-path VGAs which are transferred from the control DC currents I_I and I_Q of DAC faithfully through the cascode mirror with a ratio of 4:1. The polarity of I/Q input can be chosen by switching the tail current from one side to the other with switches S_I/S_{IB} and S_Q/S_{QB} to realize four different output phase quadrants, of which the ranges of phase shifting are $0\sim\pi/2$, $\pi/2\sim\pi$, $\pi\sim3\pi/2$, $3\pi/2\sim2\pi$ respectively. As the DC model of a 0.13μm CMOS given from the foundry can be approximated to the conventional long channel quadratic I-V model under the low-level gate overdriving, the voltage gain (A_V) of VGAs can be approximated as (1) and the synthesized phase (θ) is given as (2) [6].

$$A_V=20\log\left(\sqrt{\mu_n C_{ox}(W/L)}Z_{eq}\sqrt{I_{IB}+I_{QB}}\right)\text{(dB)} \quad (1)$$

$$\theta=\tan^{-1}\left(\frac{A_{V,Q}}{A_{V,I}}\right)=\tan^{-1}\left(\frac{\sqrt{\mu_n C_{ox}(W/L)}Z_{eq}\sqrt{I_{QB}}}{\sqrt{\mu_n C_{ox}(W/L)}Z_{eq}\sqrt{I_{IB}}}\right)=\tan^{-1}\sqrt{\frac{I_{QB}}{I_{IB}}}\text{(deg)} \quad (2)$$

Where μ_n is the electron mobility, C_{ox} is oxide capacitance, W/L is the size of input NMOS, Z_{eq} is the load impedance determined mainly by the inductor L_{load} (494 pH) and resistor R_{load} (11 kΩ). Inductive loads are used with de-Q resistors for wideband operation. Thus for all the 64 different phase states, the value of $I_{IB}+I_{QB}$ remains unchanged to maintain the gain of VGA the same while the ratio of I- and Q-path bias current is changed to obtain desired phase. It contributes to the major benefit of active phase shifter. That is the ratio of I_{QB}/I_{IB} will track temperature variations so that the output phase would not change with the temperature. The size of the input transistors (M_1-M_8) is optimized as W/L =30/0.12 for good linearity while the gate length of the tail NMOS is chosen as L=1 μm for good current matching.

D. 6-bit phase control

The digital control part includes a current mode differential DAC and the control logic which generates the necessary control bits for the switches in the DAC and VGAs. The I- and Q-path current ratio of the adder is achieved by mirroring to the tail current of the DAC. Fig. 2 presents the 7- bit I/Q DAC which works together with the switches S_I/S_{IB} and S_Q/S_{QB} for the 6-bit phase generation. As the phase step 5.625° is relatively small, seven basic current branches are implemented in the DAC to provide the current of $1\times I_{ref}$, $2\times I_{ref}$, $4\times I_{ref}$, $8\times I_{ref}$, $16\times I_{ref}$, $32\times I_{ref}$, $64\times I_{ref}$ (I_{ref}=9.6 μA) respectively. By controlling the on/off switches $S_0/S_{0B}\sim S_6/S_{6B}$, current on each branch can be brought to I- or Q-path separately to get desired I_Q/I_I current ratio. For 0°-phase state, by setting $S_I=S_0=\cdots=S_6$=high, all the branch currents are directed toward the I-path of the diode connected loads in the DAC and then transferred to the I-path of the adder with a certain ratio. For 5.625°-bit, which is such small that is quite sensitive to all kinds of mismatch factors in the design, the phase imbalance in PPF, the layout asymmetry and the transistors mismatch should be taken into account. Hence, the control logic sets $S_I=S_Q=S_2=\cdots=S_6$=high and $S_0=S_1$=low to make $I_{QB}/I_{IB}=I_Q/I_I$=3/124 instead of the theoretical value 1/103 to get the phase step 5.625°. For 11.25°-bit, the switches are set as $S_I=S_Q=S_3=\cdots=S_6$=high and $S_0=S_1=S_2$=low which makes $I_{QB}/I_{IB}=I_Q/I_I$=7/120 .Setting $S_I=S_Q=S_2=S_3=S_5=S_6$=high and $S_0=S_1=S_4$=low makes $I_{QB}/I_{IB}=I_Q/I_I$=19/108 resulting in 22.5° phase shift at the adder output. For 45°-bit, the control logic sets $S_I=S_Q=S_6$=high

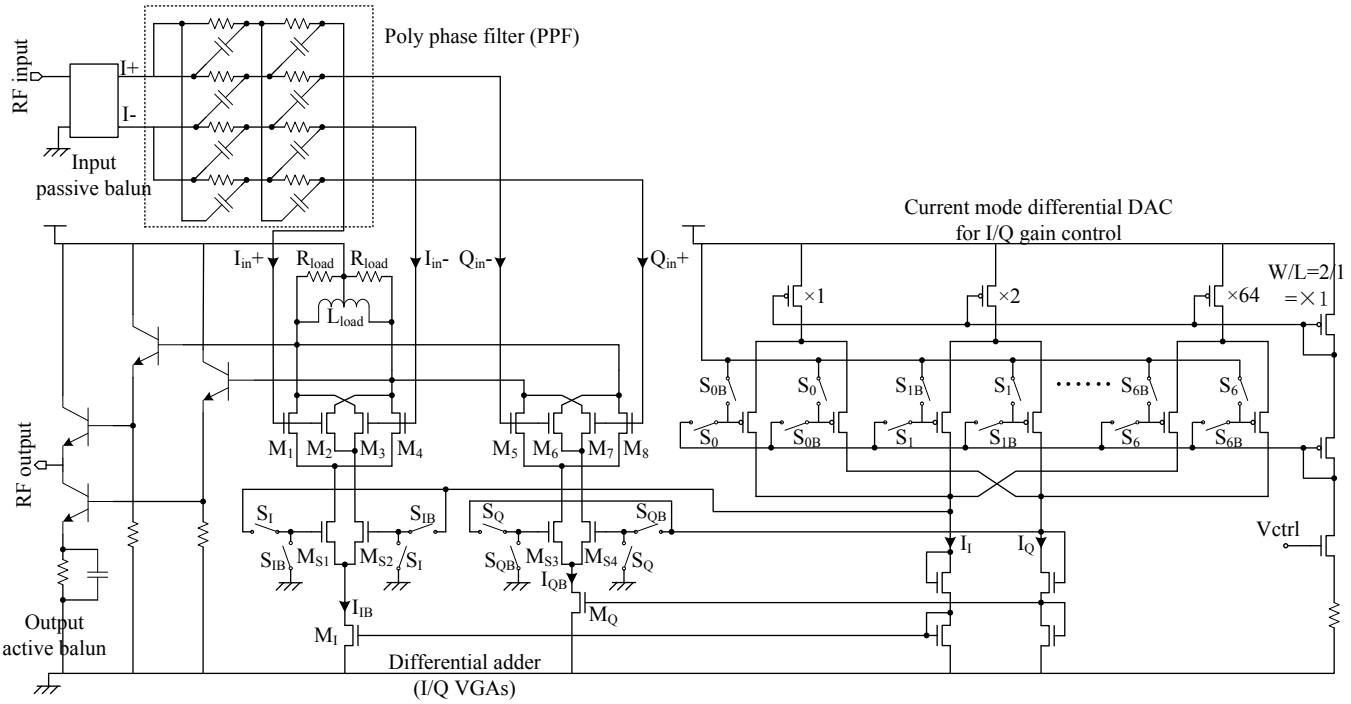

Fig. 2. The detailed schematic of the active phase shifter.

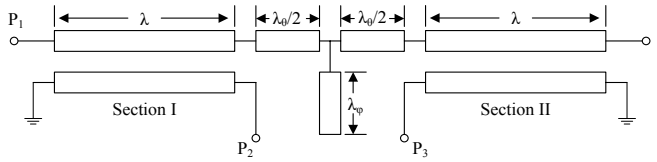

Fig. 3. The block diagram of proposed Marhand balun with a center open stub.

and S_0=⋯=S_5=low to make the current ratio between I- and Q-path equal in the DAC and adder. For other phase states, the state of the switches are changed with the similar rule. The DAC is implemented with long channel CMOS with L=1 μm to improve current matching.

IV. Results and Comparison

The layout of the phase shifter is shown in Fig. 4. The total size including all the pads is 1.77×1.18 mm^2 and the phase shifter core including input and output balun, PPF, VGAs and digital control parts occupies an area of 1.1×0.9 mm^2. Passives and RF interconnects have been simulated in ADS Momentum. The total current consumption is 13.4 mA under a 3.3 V supply voltage.

The relative insertion phases are shown in Fig. 5 over 12-18 GHz. Each state is separated by 5.625° at the center frequency of 15 GHz as required for 6-bit operation. The rms phase error calculated using the insertion phase curves is less than 2.61° in entire frequency range, as demonstrated in Fig. 6. Fig. 7 illustrates the insertion gain (S_{21}) of the phase shifter ranging from -11.16 dB to -20.39 dB for all 64 phase shift states in 12-18 GHz band. The gain slope seen at the output of the phase

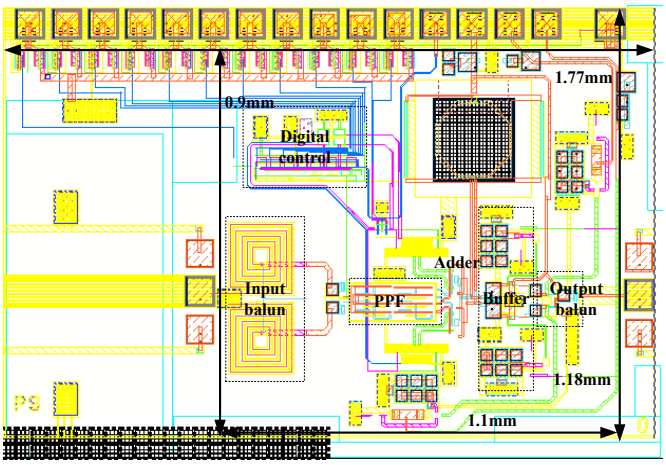

Fig. 4. Layout of the active phase shifter.

shifter is relatively large but can be easily compensated with other gain stages peaked at low/high frequency in a phased array. The rms gain error for the 64 phase shift states is less than 0.4 dB as shown in Fig. 8. The output return loss S_{22} is lower than -20.4 dB in the entire frequency range. The input P1dB for 0°-phase state is 9.98 dBm at 16 GHz. TABLE I presents the performance comparison of the proposed phase shifter with current state-of-the-art RF phase shifters. The simulation results show that the proposed 6-bit active phase shifter can function well in 12-18 GHz frequency band and is possessed of high linearity with low rms phase error and gain error.

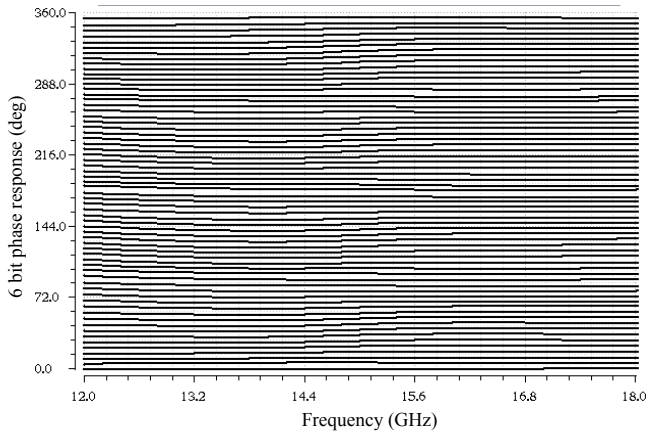

Fig. 5. Simulated 6-bit phase states (relative to 0°-phase state).

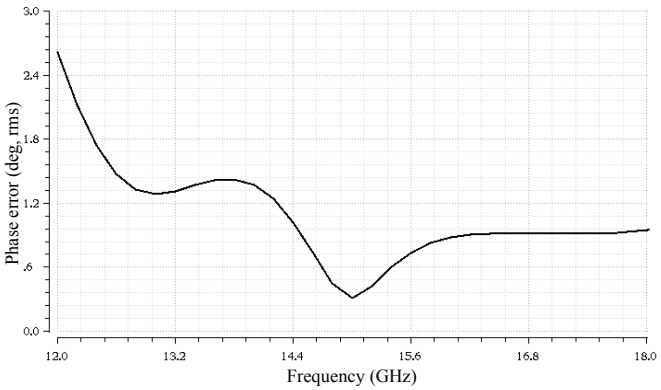

Fig. 6. The rms phase error versus frequency.

TABLE I. PERFORMANCE COMPARISON OF THE PHASE SHIFTER

Ref.	**[5][2]**	**[6][1]**	**[7][1]**	**[8][2]**	**This work[2]**
Tech.	0.18μm CMOS	0.18μm BiCMOS	0.18μm BiCMOS	0.13μm BiCMOS	0.13μm BiCMOS
Type	Switched LC	VS[3]	VS[3]	VS[3]	VS[3]
Freq. (GHz)	8.5-10	6-18	15-35	8-12	12-18
Phase Res.	5.625°	11.25°	22.5°	5.625°	5.625°
VDD (V)	3.3	3.3	1.8	2	3.3
Power (mW)	0	61.7	25.2	16.6	44.2
Insertion gain (dB)	N/A	16.5-19.5	5– -13.5	-10±1	-11.16– -20.39
Phase error (rms)	<2°	<5.6°	4.2-13°	<5.6	<2.61°
Gain error (dB, rms)	<0.5	<1.1	1-2.2	N/A	<0.4
Input P1dB (dBm)	N/A	-36.5[4]	-6.25	N/A	9.98
Chip area	N/A	0.9	0.19	0.45	0.99

1. Measured results, 2. Simulated results, 3. Vector sum (VS), 4. Estimated

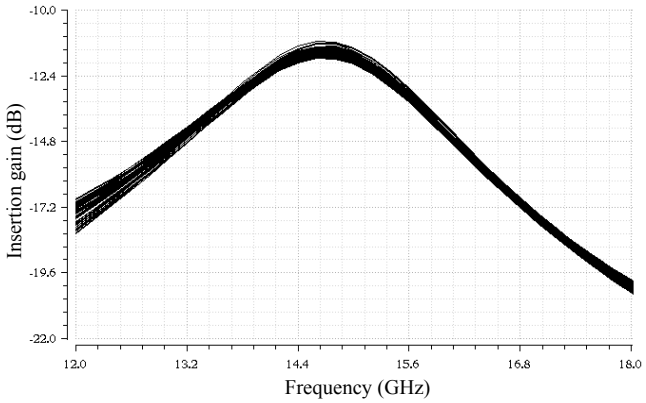

Fig. 7. Simulated insertion gain for 64 phase states.

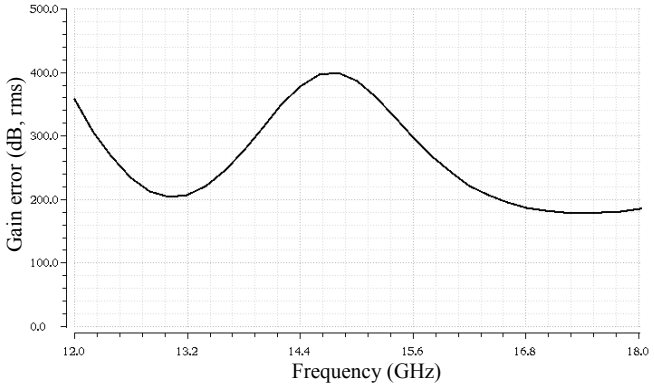

Fig. 8. The rms gain error versus frequency.

V. CONCLUSION

In this paper, a 6-bit active phase shifter integrated with all digital control circuitry in 0.13-μm SiGe BiCMOS technology is presented for K*u*-band application. An input Marchand balun with an open stub and a RC poly phase filter is developed to generate the quadrature signal with high I/Q accuracy and high linearity over a wide bandwidth. The DAC is designed ingeniously to generate the 64 phase states easily and can compensate the phase imbalance due to layout asymmetry, device mismatch and fabrication error. With all the performance figures, power consumption and size, the proposed architecture is suitable for Ku-band high resolution on chip phased arrays with multiple elements.

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