A CMOS 210-GHz Fundamental Transceiver With OOK Modulation

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***Abstract*—This paper presents a 210-GHz transceiver with OOK modulation in a 32-nm SOI CMOS process ($f_T/f_{\max}$ = 250/320 GHz). The transmitter (TX) employs a 2 × 2 spatial combining array consisting of a double-stacked cross-coupled voltage controlled oscillator (VCO) at 210 GHz with an on-off-keying (OOK) modulator, a power amplifier (PA) driver, a novel balun-based differential power distribution network, four PAs, and an on-chip 2 × 2 dipole antenna array. The noncoherent receiver (RX) utilizes a direct detection architecture consisting of an on-chip antenna, a low-noise amplifier (LNA), and a power detector. The VCO generates measured −13.5-dBm output power, and the PA shows a measured 15-dB gain and 4.6-dBm $P_{\rm sat}$. The LNA exhibits a measured in-band gain of 18 dB and minimum in-band noise figure (NF) of 11 dB. The TX achieves an EIRP of 5.13 dBm at 10 dB back-off from saturated power. It achieves an estimated EIRP of 15.2 dBm when the PAs are fully driven. This is the first demonstration of a fundamental frequency CMOS transceiver at the 200-GHz frequency range.**

***Index Terms*—CMOS, fundamental transceiver (TRX), *G*-band, low-noise amplifier (LNA), millimeter-wave, on-chip antenna, power amplifier (PA), terahertz, 200 GHz, voltage-controlled oscillator (VCO).**

I. Introduction

THE vastly under-utilized spectrum in the millimeter-wave/THz frequency range enables disruptive applications including 10-gigabit chip-to-chip wireless communications and imaging/spectroscopy. On the imaging applications front, THz imaging is considered to be one of the emerging technologies [1]. Electromagnetic wave at these frequencies can pass through nonconducting materials. Meanwhile, many materials have a fingerprint spectrum at millimeter-wave/THz frequency range, making it possible to be used in nonionized imaging and material spectroscopy [1]–[3]. On the sensing and communications front, the availability of broad unlicensed frequency spectrum across the millimeter-wave/THz frequency range unfolds new ideas on super-precise sensing at micrometer-level and multi-10-gigabit instant wireless access at the centimeter-level spacing between transmitter (TX) and receiver (RX) [4], [5].

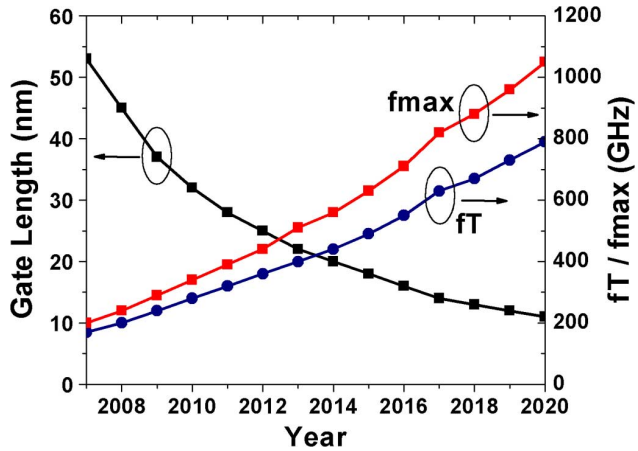

Fig. 1. ITRS 2008.

Today, THz front-ends are mainly implemented using Schottky diodes [6], nonlinear optical [7], [8], or III-V devices [9]. A complete transceiver (TRX) in a 50-nm mHEMT technology has been developed for wireless links with up to 25-Gbit/s data rate at 220 GHz [10]. Owing to aggressive scaling in feature size and device $f_T/f_{\max}$ (Fig. 1), nanoscale CMOS technology potentially enables integration of sophisticated systems at THz frequency range, once only able to be implemented in compound semiconductor technologies. Recently, CMOS THz signal sources and TRXs have been reported [11]–[14], employing techniques such as distributed active radiator (DAR) and super-harmonic signal generator.

This paper demonstrates a 210-GHz TRX with OOK modulation in a 32-nm SOI CMOS process ($f_T/f_{\max}$ = 250/320 GHz). This fundamental frequency TRX incorporates a 2 × 2 TX antenna array, a 2 × 2 spatial combining power amplifier (PA), a fundamental frequency voltage-controlled oscillator (VCO), and a low-noise amplifier (LNA). A short-range wireless test was carried out, showing the possibility of wireless data rate of 10 Gbps for chip-to-chip communications.

II. System Architecture

Harmonic-based TRXs reported to date in (Bi-)CMOS processes [13], [14] all suffer from high power consumption and noise figure (NF) due to the lack of front-end amplification. On the TX side, the frequency multiplier—placed usually as the last stage prior to antenna—exhibits negative power gain (e.g., −10 dB). Therefore, to generate adequate output power, a

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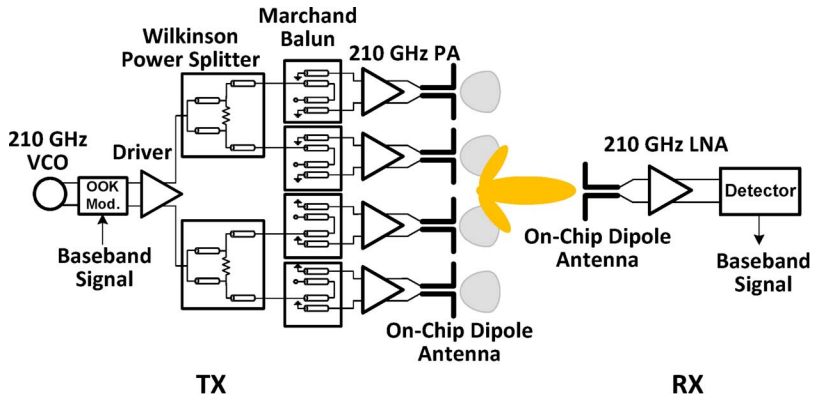


Fig. 2. Fully integrated 210-GHz differential TRX architecture.

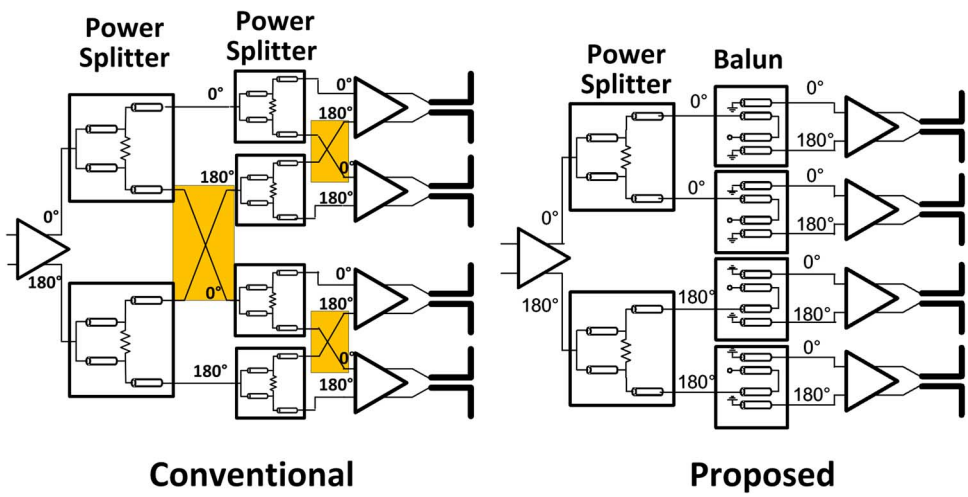


Fig. 3. Novel balun-based differential power distribution network.

stronger signal (e.g., 10 dB or higher) than the TX power needs to be generated by a lower frequency pre-PA, thus resulting in low efficiency and high power consumption. On the RX side, due to a lack of LNA in the chain, the noise contribution from the subsequent stages cannot be suppressed, thereby leading to poor NF and poor RX sensitivity.

This work addresses the above issues by implementing a TRX architecture that operates at TRX's fundamental frequency. The TRX system architecture is shown in Fig. 2 [15] and is integrated in a nanoscale CMOS process alongside on-chip antenna array. It employs fully differential topology, as it is inherently robust to common-mode substrate and power/ground induced noise and exhibits better linearity than single ended topology.

The TX incorporates a 2×2 spatial power-combining array architecture, consisting of a new double-stacked cross-coupled VCO at 210 GHz with an OOK modulator, a PA driver, a novel balun-based differential power distribution network, four PAs, and on-chip 2×2 dipole antenna array. The noncoherent RX employs a direct detection architecture comprising an on-chip antenna, an LNA, and a power detector.

Fig. 3 shows the balun-based differential power distribution network, which is amenable to high frequencies. In the conventional distribution network (Fig. 3), the undesired crossovers in the layout result in routing-related problems and signal integrity issues, such as delay/amplitude imbalance, crosstalk, and EM coupling. In the proposed structure, these unwanted crossovers are avoided by using a pattern of alternate power splitter and balun instead of using two-stage power splitters.

III. On-Chip Antenna Array and Balun Design

A. 2×2 Antenna Array

Fig. 4(a) shows an on-chip dipole antenna with surrounding ground shield, which is integrated in a 32-nm SOI CMOS process with a substrate resistivity of 13.5 Ω-cm. The high conductivity of the low-resistivity substrate of a CMOS process compared with off-chip substrate is one of the most crucial contributors to the poor radiation efficiency of on-chip antenna. The substrate thickness of 300 μm (i.e., the default post fabrication thickness) at 210 GHz is close to $3/4\lambda$ in the substrate, and the constructive reflection from the ground underneath the silicon substrate will help boost the radiation efficiency to as high as 24%, as shown in Fig. 4(b).

The dipole antenna, shown in Fig. 4(a), is implemented in the topmost metal layer. The length of the dipole is chosen to be 360 μm to maximize the radiation efficiency. The width of this antenna is chosen to be 40 μm to broaden the bandwidth, while achieving 50-Ω impedance matching. Moreover, a ground plane is placed underneath the silicon substrate to help improve the radiation efficiency, as mentioned above. Furthermore, in order to

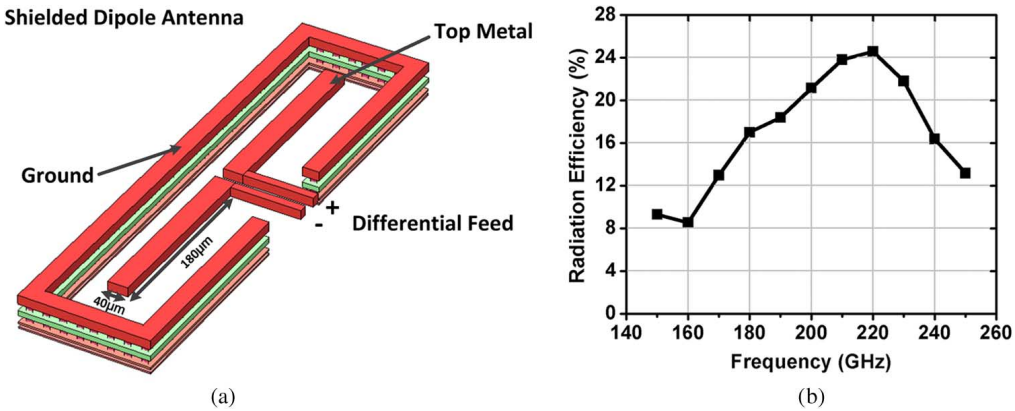


Fig. 4. On-chip shielded dipole antenna. (a) Structure. (b) Radiation efficiency with respect to frequency.

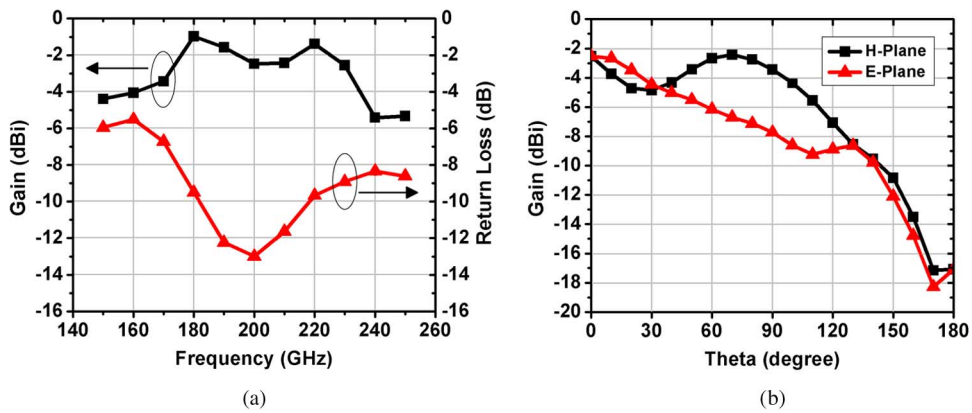


Fig. 5. Antenna parameters. (a) Gain and return loss. (b) Pattern at 210 GHz.

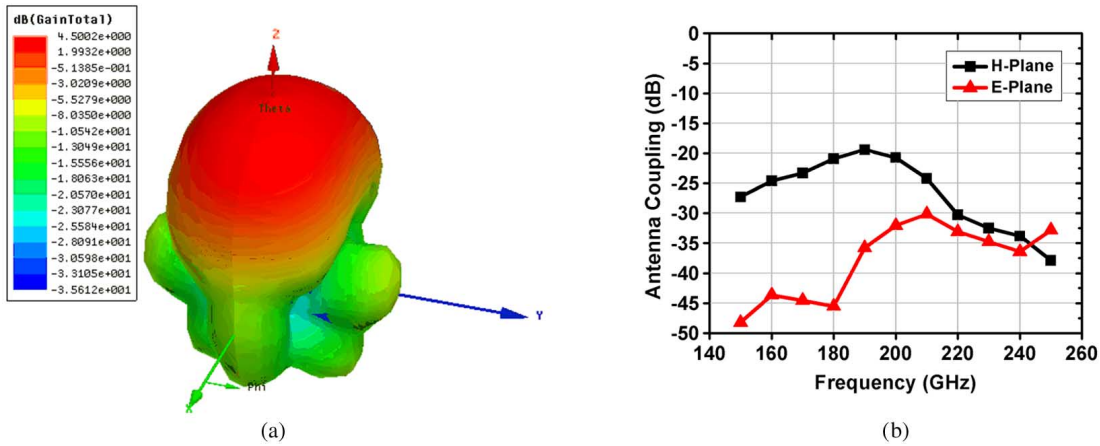
shield neighboring circuits from coupling from the antenna, an extra ground ring from the bottom to top metal surrounds each antenna. Since the on-chip antenna pattern is strongly subject to the excitation of strong substrate waves, four dipole antennas with surrounding ground shields are simultaneously simulated in HFSS on the diced prototype chip with an area of 1.4 mm $\times$ 2.5 mm to capture substrate waves as well as the mutual EM coupling between antennas elements. The simulated antenna gain and return loss versus frequency is shown in Fig. 5(a). The antenna gain at 210 GHz is -2.5 dBi, and the antenna bandwidth is 40 GHz centered at 200 GHz. Fig. 5(b) shows the simulated radiation pattern of the shielded dipole antenna. The constructive reflection from bottom ground contributes to another peak in the H-plane at $\theta = 70°$, where θ denotes the inclination angle in the spherical coordinate system.

A 2 $\times$ 2 antenna array with 0.57λ spacing between elements (i.e., 820 μm) at 210 GHz is designed to achieve a high directivity [16]. Fig. 6(a) demonstrates the radiation pattern of this 2 $\times$ 2 antenna array, where the overall antenna array gain is 4.5 dBi. The existing mutual coupling between antennas was simulated as a function of frequency [see Fig. 6(b)]. For frequencies from 200 to 220 GHz, the simulated antenna coupling in the E- and H-planes stays less than -20 and -30 dB, respectively. This low mutual coupling guarantees a negligible effect on the array's attributes, such as array factor and input impedance.

B. Marchand Balun

Owing to its wideband characteristics and ease of implementation, Marchand balun is chosen as an integral part of the proposed power distribution network [17]–[19]. Fig. 7 shows the balun structure, incorporating a cascade of two quarter-wavelength couplers. To achieve 50-Ω input matching ($S_{11} = 0$), the odd and even impedances Z_{oo} and Z_{oe} of the quarter-wavelength coupler in the balun should be 26 and 96 Ω, respectively [17]. Although both Z_{oo} and Z_{oe} are varied with the interlayer dielectric thickness, the width of the signal line, and the spacing between signal and ground lines, strict constraints exist on these geometrical parameters in a CMOS process. This makes it difficult to design the coupler to achieve the desired Z_{oo} and Z_{oe} values. A vertical coupler structure with overlapping offset is thus employed to realize the Marchand balun. This offset is introduced to provide additional degree of freedom in adjusting Z_{oo} and Z_{oe}.

Fig. 8 shows simulated S-parameters and phase difference versus frequency. The balun's bandwidth is greater than 100 GHz. Amplitude imbalance between Ports 2 and 3 is only



(a) (b)

Fig. 6. 2 × 2 antenna array parameters. (a) 3-D pattern. (b) Antenna coupling.

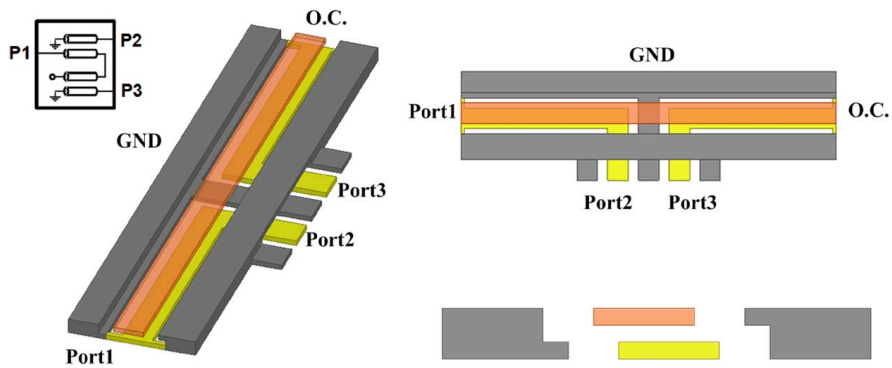


Fig. 7. Marchand balun.

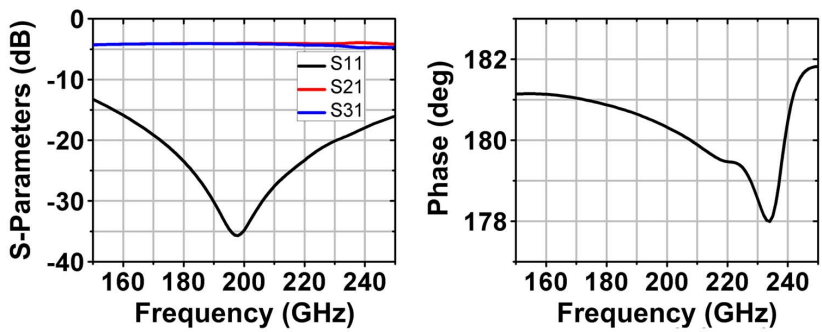


Fig. 8. Marchand balun performance. S-parameters and phase difference.

0.2 dB, while phase imbalance is less than ±2° around 180° over the 100-GHz bandwidth.

IV. Over-Neutralization Technique and PA Design

A. Neutralization Technique for Differential Pair

The neutralization technique, shown in Fig. 9(a), using a pair of cross-connected capacitors in a differential pair amplifier has been widely exercised to stabilize the amplifier. The neutralization capacitors C_n introduce an equivalent capacitance $-C_n$ that compensates for the effect of intrinsic C_{gd} of the transistor, thereby unilateralizing the device. In addition, neutralization technique is also utilized to achieve higher maximum available power gain (MAG, also called $G_{\max}$) [20]–[22]. The MAG for a fully unilaterized device is actually Mason's U, defined as [23]

$$U = \frac{|Y_{12} - Y_{21}|^2}{4\left(\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{21}]\mathrm{Re}[Y_{12}]\right)}. \tag{1}$$

C_{gd} is commonly considered to be the only contributor to Y_{12}, hence, $\mathrm{Re}[Y_{12}]$ is zero. In this case, (1) is often expressed as [20]

$$U = \frac{|\mathrm{Re}[Y_{21}]|^2}{4\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}]} = \frac{g_m^2}{4g_g g_{\mathrm{ds}}} \tag{2}$$

where g_g and g_{ds} are the gate and drain–source conductances of the device, respectively. Fig. 9(b) shows the MAG and the Mason's U of a MOS device versus frequency. The knee point

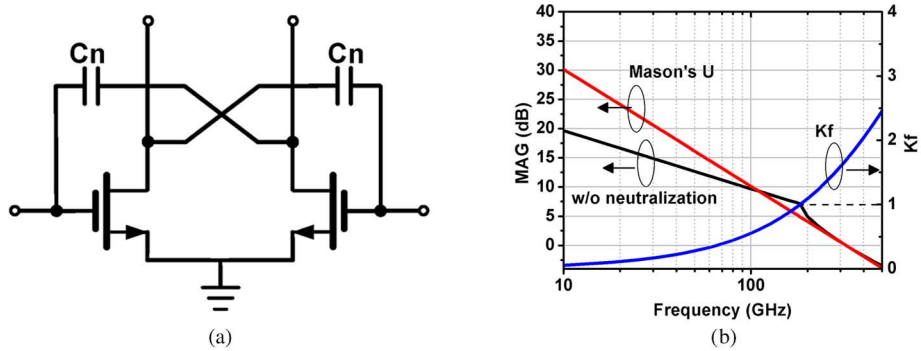


Fig. 9. Neutralization technique for differential pair. (a) Schematic. (b) MAG.

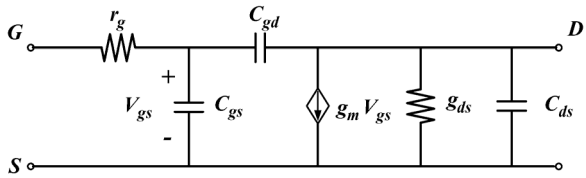


Fig. 10. RF small-signal model for SOI MOSFET.

existed in the MAG curve of the device without neutralization corresponds to stability factor K_f of one, and locates around 1/3 $\sim$ 2/3 of $f_{\max}$. For frequencies below the knee point, neutralization technique helps boost the gain while stabilizing the device. After the knee point, defined as "near-$f_{\max}$ region," only a slight difference exists between the MAG of device without neutralization and the Mason's invariant U.

B. Revisiting the Neutralization Technique

To boost the power gain in the near-$f_{\max}$ region, the neutralization technique is revisited. First, Y-parameters of the MOS common source configuration, shown in Fig. 10, are derived, i.e.,

$$\begin{aligned} Y_{11} &= \omega^2(C_{\rm gs}+C_{\rm gd})^2 r_g + j\omega(C_{\rm gs}+C_{\rm gd}) && (3)\\ Y_{12} &= -\omega^2(C_{\rm gs}+C_{\rm gd})C_{\rm gd}r_g - j\omega C_{\rm gd} && (4)\\ Y_{21} &= g_m\left[1-j\omega(C_{\rm gs}+C_{\rm gd})r_g\right] \\ &\quad -\omega^2(C_{\rm gs}+C_{\rm gd})C_{\rm gd}r_g - j\omega C_{gd} \\ &\approx g_m - j\omega\left[g_m r_g(C_{\rm gs}+C_{\rm gd})+C_{\rm gd}\right] && (5)\\ Y_{22} &= g_{\rm ds}+\omega^2 C_{\rm gd}r_g\left[g_m r_g(C_{\rm gs}+C_{\rm gd})+C_{\rm gd}\right] \\ &\quad + j\omega\left[C_{\rm ds}+C_{gd}(1+g_m r_g)\right] \\ &\approx g_{\rm ds}+j\omega\left[C_{\rm ds}+C_{\rm gd}(1+g_m r_g)\right]. && (6)\end{aligned}$$

The above approximations are obtained under the condition that $f < 2f_{\max}$ where $f_{\max}$ is the maximum oscillation frequency of the transistor, $f_{\max} = (1/4\pi)(g_m/[r_g C_{\rm gd}(C_{\rm gd}+C_{\rm gs})])^{0.5}$.

Substituting (3)–(6) into (1), the Mason's U for MOSFET is derived as

$$U \approx \frac{|g_m|^2}{4\left[\omega^2(C_{\rm gs}+C_{\rm gd})^2 r_g g_{\rm ds}+\omega^2(C_{\rm gs}+C_{\rm gd})C_{\rm gd}r_g g_m\right]}. \quad (7)$$

Noticing that $\mathrm{Re}[Y_{12}]$ is nonzero due to gate resistance r_g, the contribution of Y_{12} to Mason's U is nonzero, thereby invalidating (2). In a capacitance-based neutralization topology, an extra equivalent capacitance $-C_n$ is effectively placed in parallel with the input and output ports of the original two port network. The new Y-parameters thus become

$$\begin{aligned} Y'_{11} &= Y_{11} - j\omega C_n \\ &= \omega^2(C_{\rm gs}+C_{\rm gd})^2 r_g + j\omega C_{\rm gs} + j\omega(C_{\rm gd}-C_n) && (8)\\ Y'_{12} &= Y_{12} + j\omega C_n \\ &= -\omega^2(C_{\rm gs}+C_{\rm gd})C_{\rm gd}r_g - j\omega(C_{gd}-C_n) && (9)\\ Y'_{21} &= Y_{21} + j\omega C_n \\ &\approx g_m - j\omega\left[g_m r_g(C_{\rm gs}+C_{\rm gd})+C_{\rm gd}-C_n\right] && (10)\\ Y'_{22} &= Y_{22} - j\omega C_n \\ &\approx g_{\rm ds} + j\omega C_{\rm ds} + j\omega\left[C_{\rm gd}(1+g_m r_g)-C_n\right]. && (11)\end{aligned}$$

If $C_n = C_{\rm gd}$, the imaginary part of Y_{12}, $\mathrm{Im}[Y_{12}]$, will be neutralized, while $\mathrm{Re}[Y_{12}]$ will be intact. This means that the device is not fully unilateralized by an external equivalent capacitance $-C_n$. This rather different conclusion from what is conventionally known about capacitance-based neutralization technique stems from the nonzero contribution of gate resistance r_g at high frequencies.

K_f and $G_{\max}$ are derived using new Y-parameters in (8)–(11) [24] as follows:

$$K_f = \frac{2\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] - \mathrm{Re}\left[Y_{12}Y_{21}\right]}{|Y_{12}Y_{21}|}. \quad (12)$$

$$G_{\max} = \left|\frac{Y_{21}}{Y_{12}}\right|\left(K_f - \sqrt{K_f^2-1}\right). \quad (13)$$

Fig. 11(a) shows $G_{\max}$, Mason's U, and K_f with respect to C_n at 100 GHz, which is close to knee frequency in Fig. 9(b). Due to its invariance in the presence of any embedded linear lossless reciprocal network [23], the Mason's U remains constant with C_n. The bell-shaped K_f curve reaches its peak value at $C_n = C_{\rm gd}$. On the other hand, $G_{\max}$ reaches its peak value for two values of C_n when $K_f = 1$- and reaches a local minimum at $C_n = C_{\rm gd}$ [20]. Interestingly, at 100 GHz, $G_{\max}$ after neutralization ($C_n = C_{\rm gd}$) is higher than the unilateral power gain U, justifying this important notion that the differential pair with neutralization capacitance cannot be treated as a fully unilateralized device because $\mathrm{Re}[Y_{12}]$ is not compensated.

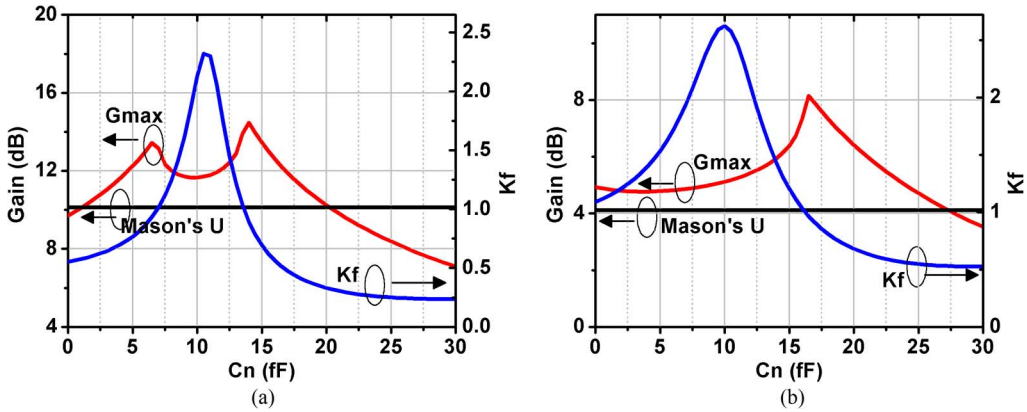


Fig. 11. Maximum power gain with respect to neutralization capacitance at (a) 100 GHz and (b) 200 GHz.

When the device is operating in its near-$f_{\max}$ region (e.g. 200 GHz), the K-factor of the original device itself is greater than unity, as shown in Fig. 9(b). The effects of the neutralization capacitance are shown in Fig. 11(b). Since now $K_f > 1$ even without any neutralization capacitance, the original device itself is unconditionally stable and the power gain is almost the same as that of the neutralized device. When C_n keeps increasing into the *over-neutralization* region, gain is boosted by pushing the device to the edge of the stability region. From Fig. 11(b), significant gain boosting is achieved by employing an over-neutralization technique, indicating that it is much more effective in gain boosting compared with a neutralization technique in the near-$f_{\max}$ region. The maximum boosted gain achieved using over-neutralization is close to the upper limit of $2U - 1 + 2\sqrt{U(U-1)}$ obtained in [25].

Based on our observation, the achievable power gain of the device is both upper and lower bounded when the device is located in the region $K_f > 1$, i.e.,

$$U \le G_{\max} \le (2U-1) + 2\sqrt{U(U-1)}. \tag{14}$$

Another interesting observation is that at $f_{\max}$, both lower and upper limits of $G_{\max}$ converge to one. Thus, f_{max} is fixed regardless of what kind of lossless reciprocal network is placed around the device. Fig. 12 shows $G_{\max}$ of devices with respect to frequency for different neutralization capacitances. All of these $G_{\max}$ curves intercept at $f_{\max}$.

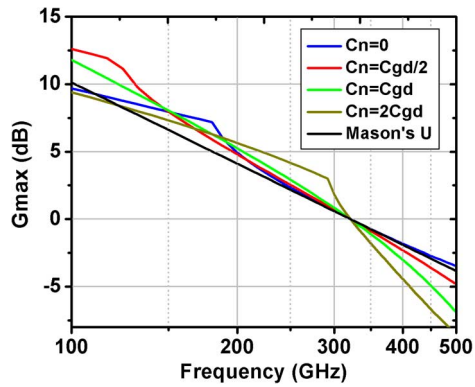


Fig. 12. $G_{\max}$ curves with different C_n cross over at the frequency point ($f_{\max}$).

C. 200-GHz Transistor Layout for PA

For millimeter-wave/THz circuit design, the effect of parasitics in the layout is considered to be one of the critical issues [26]–[28]. As the frequency approaches half-$f_{\max}$ of a 32-nm CMOS transistor, the parasitics associated with transistor layout (e.g., $C_{\mathrm{gs,e}}$, $C_{\mathrm{gd,e}}$, $r_{g,e}$) are directly absorbed to the transistor's RF model and thus degrade its performance, i.e., a poor layout may lead to a negative $G_{\max}$ at such high frequencies. Prior researchers have conducted investigations on ways of mitigating the parasitics [29], [30]. From (14), although Mason's U is smaller than $G_{\max}$, its invariance to any externally added lossless network makes it a good candidate to study the layout parasitics. Fig. 13(a) shows the effects of layout-induced parasitic capacitors $C_{\mathrm{gs,e}}$ and $C_{\mathrm{gd,e}}$ on the device's U. From this figure, the U degradation due to $C_{\mathrm{gd,e}}$ is around two times that due to extrinsic $C_{\mathrm{gs,e}}$. Therefore, the interconnect routings of source and drain terminals are done in such a way as to minimize $C_{\mathrm{gd,e}}$. For instance, external access to the drain terminal is made through the top metal layer so as to separate gate and drain metal lines.

Fig. 14 shows the transistor layout in IBM 32-nm SOI CMOS process, used in a 210-GHz PA. Multifinger configuration is used to reduce the finger width and, thus, parasitic gate resistance, which is crucial in the U degradation. However, the smaller finger width leads to more finger numbers. As the design of a PA requires extra wide transistor's width, two double-sided-gate configurations in parallel are employed to avoid having the layout get stretched in one dimension [Fig. 14(a)]. Two metal layers M1 and M2 are stacked for the gate interconnection, and the width of the gate line is intentionally widened to reduce its resistance. To minimize $C_{\mathrm{gd,e}}$, external access to the drain is made through top layers E1, MA to further separate the gate and drain lines [Fig. 14(b)]. Middle layers B1, B2 and B3 are used as source interconnection [Fig. 14(b)]. This layout configuration can also support large current density as drain and source connections use thick metal to account for electromigration. Three MOSFETs (width of 32 μm) with different finger widths are laid out and their $f_{\max}$ are shown in Fig. 13(b). The finger width of 640 nm is finally chosen to get the maximum $f_{\max}$.

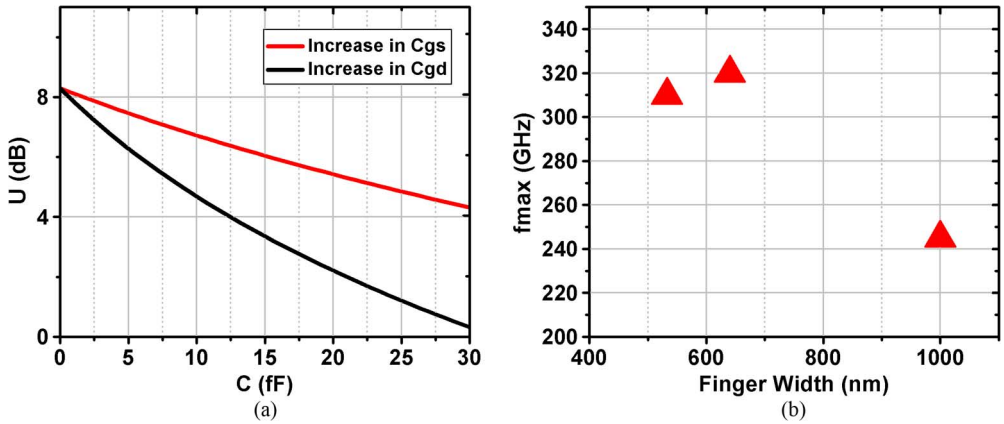


Fig. 13. Layout issues of 200-GHz transistor. (a) U's sensitivity to $C_{\rm gs}$ and $C_{\rm gd}$. (b) Post-layout $f_{\rm max}$ with different finger width.

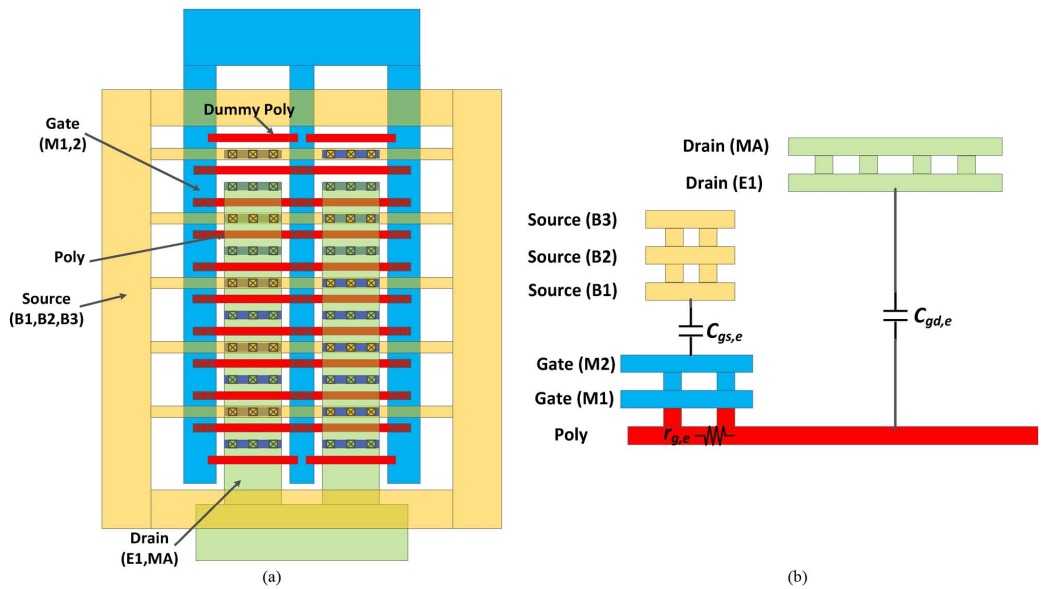


Fig. 14. Floorplan for transistor layout. (a) Top view. (b) Side view.

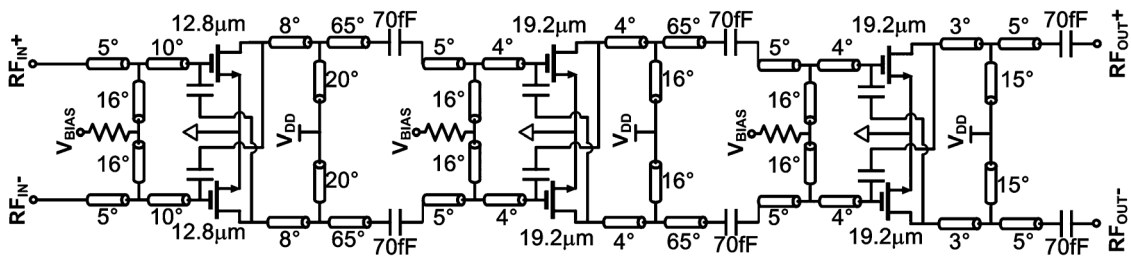


Fig. 15. 210-GHz CMOS PA schematic.

D. 210-GHz CMOS PA

Fig. 15 shows the schematic of the 210-GHz CMOS PA, which is comprised of a three-stage differential amplifier using an over-neutralization technique. Differential topology eliminates the parasitics' source-degenerative effects by providing shorter physical interconnection from its transistors' source terminals to ground compared with a single-ended counterpart and is also insensitive to the modeling inaccuracy of decoupling capacitors at 210 GHz. In addition, $C_{\rm gd}$-neutralization capacitor is simply realized by $C_{\rm gd}$ of a similar MOSFET to mitigate the mismatch between neutralization capacitor and main transistor's $C_{\rm gd}$, as shown in Fig. 16(a).

The transistor's intrinsic $G_{\rm max}$ after layout is only 4.5 dB, and, after deducting the loss of matching network (roughly 2.5 dB per stage), the achievable power gain per stage is only 2 dB. The 2-dB gain per stage raises two concerns: 1) it yields poor power-added efficiency (PAE), i.e., only around one third of drain efficiency, and 2) it leads to a large number of cascaded stages for high amplification (e.g., 10 dB), which will further

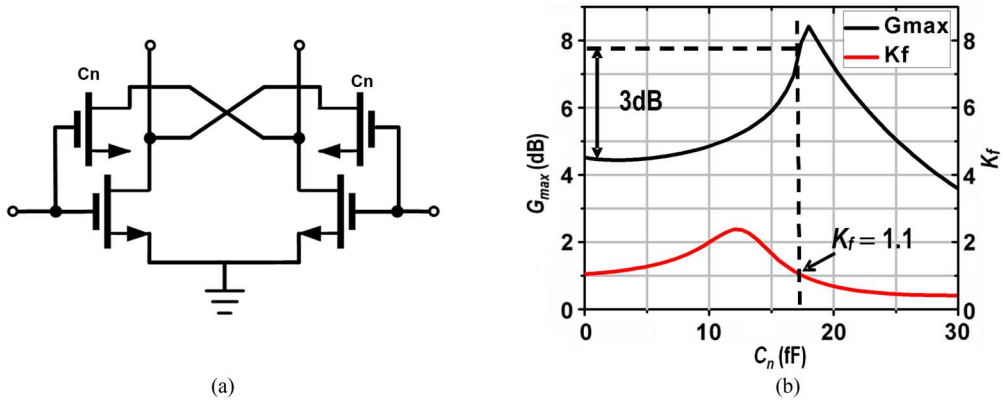


Fig. 16. Over-neutralization technique. (a) $C_{\rm gd}$ of similar MOSFET as C_n. (b) Gain boosting.

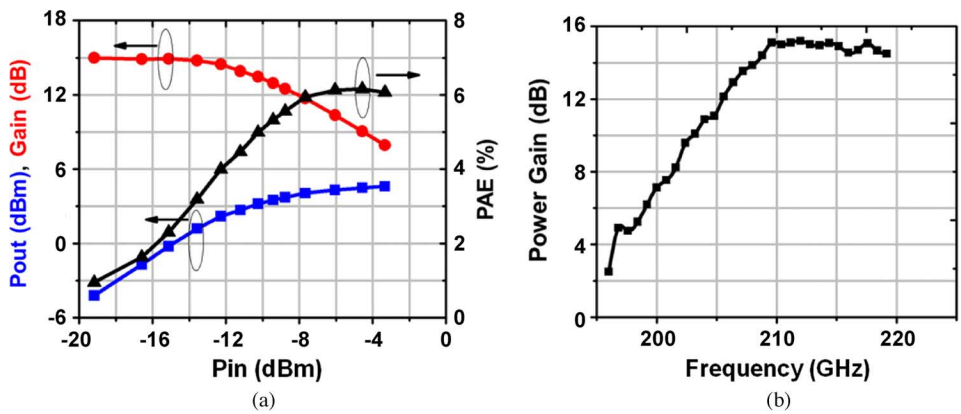


Fig. 17. Measurement result for PA. (a) $P_{\rm out}$, gain, and PAE with respect to $P_{\rm in}$. (b) Power gain with respect to frequency.

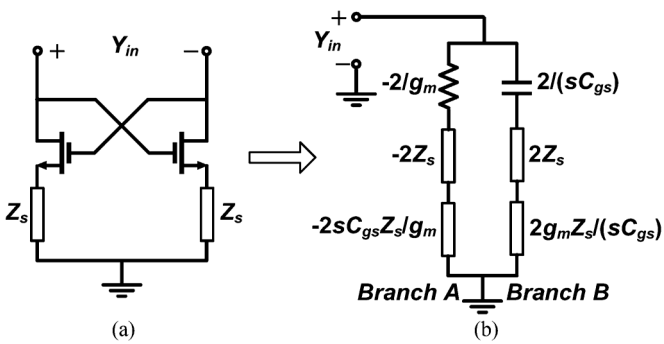


Fig. 18. Source degeneration for cross-coupled pair. (a) Schematic. (b) Equivalent circuit.

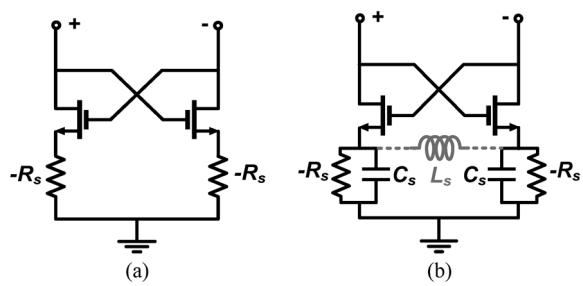


Fig. 19. Negative resistive source degeneration. (a) Resistance only. (b) With parasitic capacitance.

lead to higher power consumption and smaller bandwidth. In order to overcome this problem, an over-neutralization technique has been employed. The PA's main transistors are intentionally pushed to the edge of stability region, resulting in higher gain shown in Fig. 16(b). By choosing proper neutralization capacitance C_n, the $G_{\rm max}$ can be boosted by as much as 4 dB. To leave a margin for stability, a 3-dB gain boost, corresponding to K_f of 1.1, is chosen.

Considering that the quarter-wavelength is only around 180 μm at 210 GHz, the ground-shielded CPW line is utilized for impedance matching. All PA stages are interstage-matched to 50 Ω to make the design more robust to process-dependent uncertainties in passive components at this frequency, which, in turn, leads to more flexibility in layout. The PA's output matching network is designed for maximum $P_{\rm sat}$. The extra loss added by the matching network makes the amplifier more stable, and the stability factor of the overall PA is greater than unity at all frequencies, which means it is unconditionally stable.

The PA core occupies 150×400 μm^2 of die area (excluding pad). The PA breakout was tested by using a G-band (140–220 GHz) RF probe and power meters. To this end, on-chip baluns were used to convert the input and output differential signals to single-ended. The loss of the on-chip balun was calibrated using back-to-back configuration and was de-embedded from the PA output power. The PA circuit exhibits a measured peak gain of 15 dB, OP1 dB of 2.7 dBm, $P_{\rm sat}$ of 4.6 dBm, and a peak PAE of 6%, as shown in Fig. 17(a).

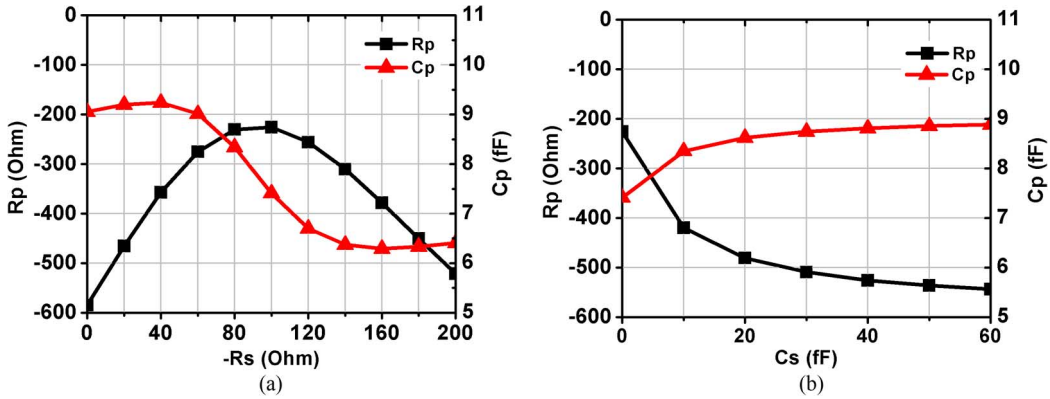


Fig. 20. Simulation effective parallel resistance R_p and effective parallel resistance C_p for cross-coupled pair with source degeneration. (a) Sweep R_s, when $C_s = 0$. (b) Sweep C_s, when $-R_s = -90\ \Omega$.

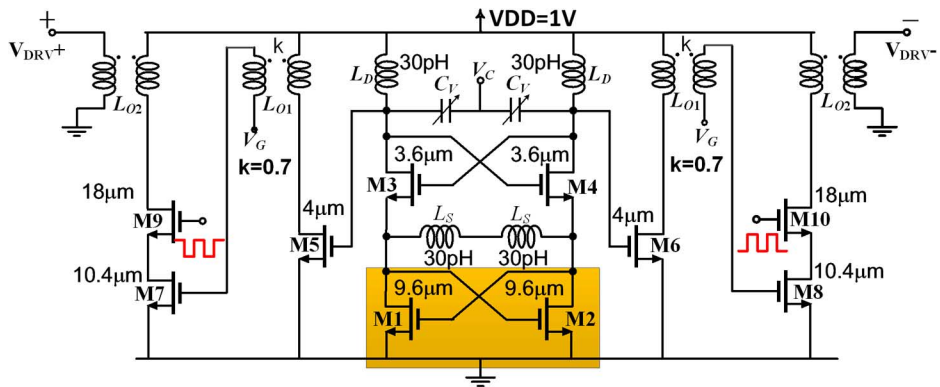


Fig. 21. Schematic of 210-GHz CMOS VCO.

Fig. 17(b) exhibits a 3-dB bandwidth of more than 14 GHz. The measured PA bandwidth is limited by the highest measurable frequency (220 GHz) of the test equipment. The system measurement in Section VI demonstrates a wireless link with 10-GHz baseband bandwidth, indirectly implying the PA bandwidth to be actually around 20 GHz. The PA draws 40 mA from a 1-V supply.

V. VCO, LNA, and Power Detector Design

A. VCO

As was discussed in the previous section, the transconductance g_m degrades significantly as the operation frequency increases towards half-$f_{\max}$ of the device. Moreover, varactor loss becomes the dominant contributor to the Q-factor degradation of the oscillator. As a consequence, new circuit techniques need to be examined in the design of a fundamental VCO at 200 GHz to overcome these limitations. Inductive tuning was demonstrated to be amenable to high frequencies compared with varactor tuning [31]. Capacitive source degeneration at the buffer stage was proposed to increase equivalent negative resistance for millimeter-wave design [32]–[34]. Also, capacitive source degeneration below the cross-coupled pair can decrease undesired parasitic capacitance [35], [36]. In this paper, the use of source degeneration in a cross-coupled pair has been extended to complex impedance Z_s. By injecting a test voltage source V_t to the cross-coupled pair with source degeneration impedance Z_s shown in Fig. 18(a), the equivalent admittance is obtained as

$$Y_{\text{in}} = \frac{-g_m + sC_{\text{gs}}}{2(1 + g_m Z_s + sC_{\text{gs}} Z_s)} = \frac{1}{-\frac{2}{g_m} - 2Z_s - \frac{2sC_{\text{gs}}Z_s}{g_m}} + \frac{1}{\frac{2}{sC_{\text{gs}}} + \frac{2g_m Z_s}{sC_{\text{gs}}} + 2Z_s}. \quad (15)$$

Therefore, the equivalent circuit of the cross-coupled pair with source degeneration is composed of a parallel combination of branch A and branch B in Fig. 18(b), corresponding to two terms in (15).

Assuming Z_s is purely negative resistance (i.e., $Z_s = -R_s$), the resistance $-2/g_m$ in Branch A is partially neutralized by $2R_s$. The Q-factors of branch A (defined as Q_A) and branch B (defined as Q_B) are obtained as

$$|Q_A| = \left|\frac{\text{Im}[Z_A]}{\text{Re}[Z_A]}\right| = \left|\frac{2\omega C_{\text{gs}} R_s/g_m}{-2/g_m + 2R_s}\right| = \left|\frac{\omega C_{\text{gs}} R_s}{1 - g_m R_s}\right|$$
$$|Q_B| = \left|\frac{\text{Im}[Z_B]}{\text{Re}[Z_B]}\right| = \left|\frac{-2/\omega C_{\text{gs}} + 2g_m R_s/\omega C_{\text{gs}}}{-2R_s}\right| = \left|\frac{1 - g_m R_s}{\omega C_{\text{gs}} R_s}\right|. \quad (16)$$

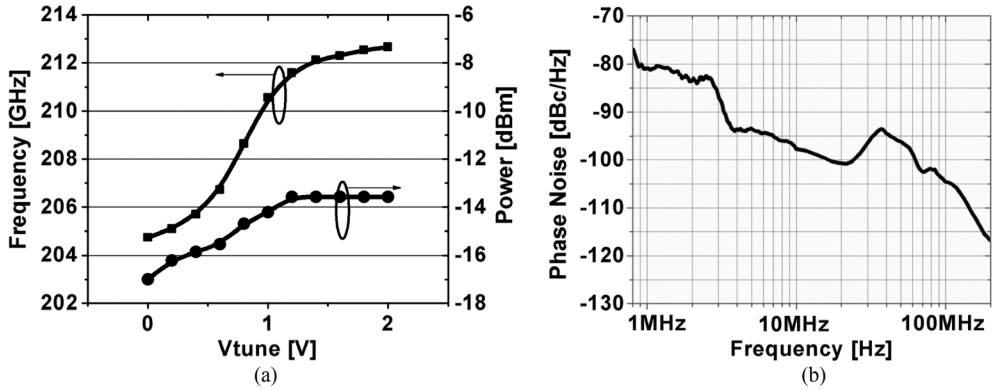


Fig. 22. Measurement results for VCO. (a) Tuning range and output power. (b) Phase noise.

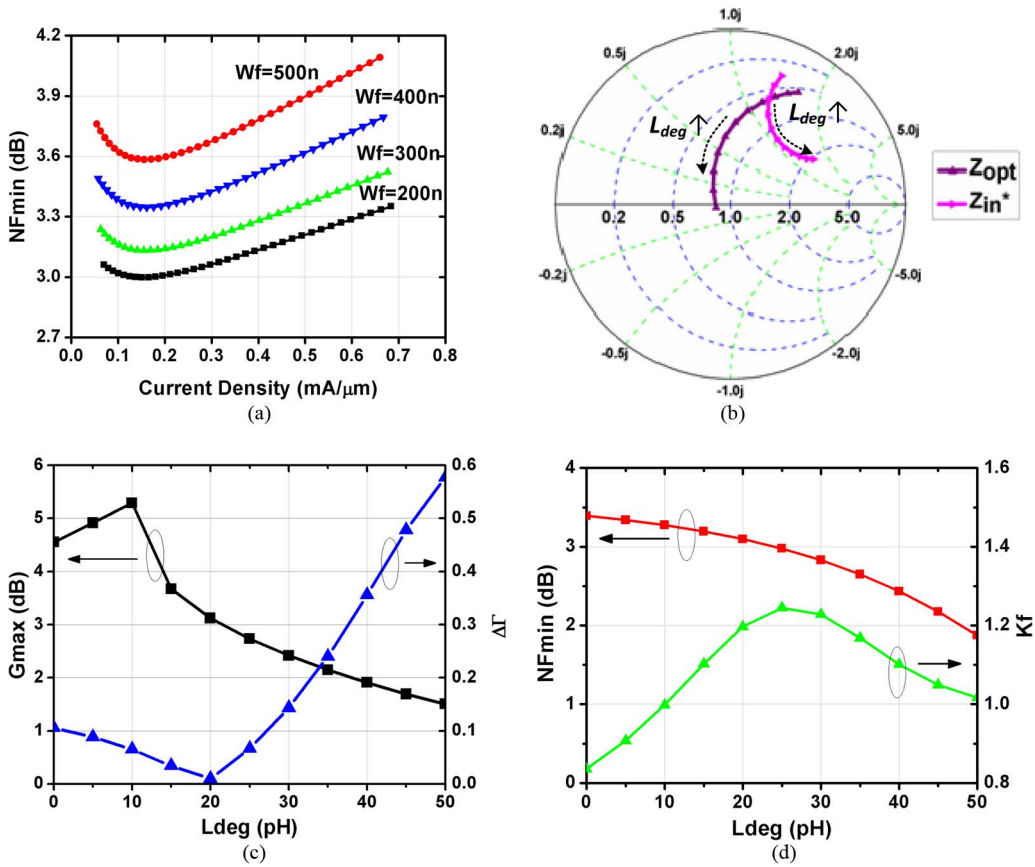


Fig. 23. LNA design. (a) $\mathrm{NF}_{\min}$ with respect to current density. (b) Simultaneous noise and power match. (c) Tradeoff between reflection and $G_{\max}$. (d) $\mathrm{NF}_{\min}$ and Kf with respect $L_{\deg}$.

Also, under the condition $R_s < (1/g_m).\ 1/(1+\omega/\omega_T)$, $|Q_B| > 1$ and $|Q_A| < 1$. $\mathrm{Re}[Y_{in}]$ is thus dominated by branch A, i.e.,

$$\begin{aligned}\mathrm{Re}[Y_{in}] &= \mathrm{Re}[Y_A] + \mathrm{Re}[Y_B] \\ &= \frac{1}{1+Q_A^2}.\frac{1}{\mathrm{Re}[Z_A]} + \frac{1}{1+Q_B^2}.\frac{1}{\mathrm{Re}[Z_B]} \\ &\approx \frac{1}{\mathrm{Re}[Z_A]} = -\frac{g_m}{2(1-g_m R_s)} < -\frac{g_m}{2}. \end{aligned} \quad (17)$$

Therefore, the real part of overall admittance of the equivalent circuit representing cross-coupled pair with negative resistance in the source terminal is enhanced compared to the conventional cross coupled pair. This negative resistance can readily be realized using an additional cross-coupled pair, as will be explained later in this section.

In order to verify the above first order analysis, two cross-coupled pairs with two different source degenerations, shown in Fig. 19, are simulated. Fig. 20(a) shows effective parallel resistance R_p defined as $R_p = 1/\mathrm{Re}[Y_{\mathrm{in}}]$ and effective parallel capacitance C_p defined as $C_p = \mathrm{Im}[Y_{\mathrm{in}}]/\omega$ at 200 GHz for circuit with source degeneration of only negative resistance R_s in Fig. 19(a). Simulation shows that there is an optimum value for R_p when R_s is around 90 Ω. A proper choice of negative resistance at the source of the cross-coupled pair will increase R_p by

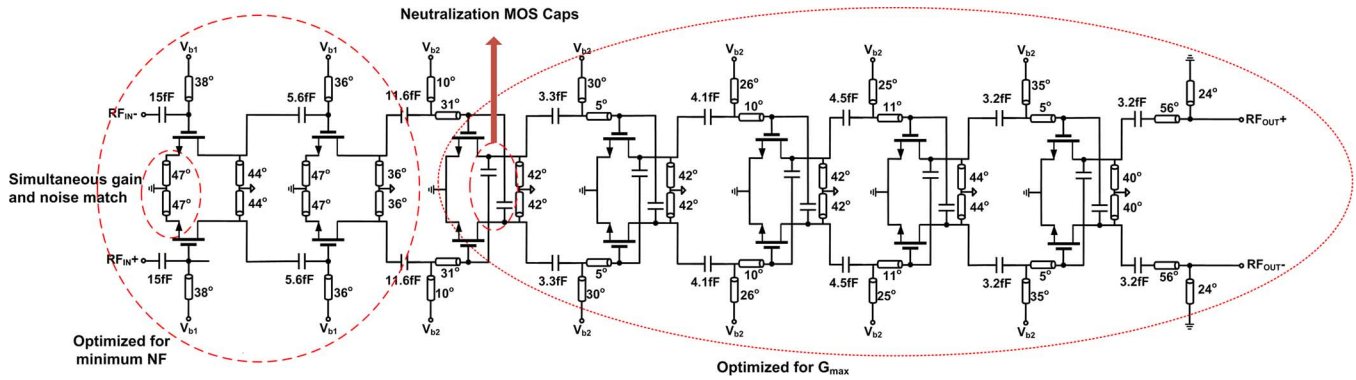


Fig. 24. Schematic of a 210-GHz CMOS LNA.

three times, leading to higher loop gain. Moreover, a decrease in effective capacitance C_p also helps improve tuning range and relax the choice of tank inductance value.

One effective way of realizing the negative resistance is by another cross-coupled pair. However, the corresponding parasitic capacitance cannot be neglected. Fig. 20(b) shows its effective parallel resistance R_p and parallel capacitance C_p at 200 GHz for circuit with source degeneration of both negative resistance R_s and parasitic capacitance C_s in Fig. 19(b). It indicates that both R_p and $X_p(=1/(j\omega C_p))$ are lowered as the source parasitic capacitance C_s increases. Therefore, an extra inductor L_s is added between the source terminals of the cross coupled pair to resonate out this undesired parasitic capacitance [Fig. 19(b)].

Fig. 21 shows the fundamental double-stacked cross-coupled VCO and the OOK modulator. The overall negative resistance of this oscillator is increased due to an additional negative source degeneration resistance provided by $\mathrm{M}_1 - \mathrm{M}_2$. This negative resistance compensates for the excessive varactor loss at very high frequencies, thereby improving overall loop gain. As mentioned above, the 30-pH inductor L_S in Fig. 21 mitigates the detrimental effect of parasitic capacitance of the bottom cross-coupled pair $\mathrm{M}_1 - \mathrm{M}_2$. The interstage matching network between the VCO buffer and the OOK modulator has been realized by transformers, thereby leading to compact layout. The OOK modulator utilizes a cascode topology $\mathrm{M}_7(\mathrm{M}_8) - \mathrm{M}_9(\mathrm{M}_{10})$, where the modulated signal is applied to the gate of transistor $\mathrm{M}_9(\mathrm{M}_{10})$. The output of the OOK modulator is matched 50 Ω using transformers.

The VCO core and modulator occupies 100 × 400 μm^2 of die area. The circuit was characterized using a G-band (140–220 GHz) RF probe, power meters, and subharmonic mixer. The VCO exhibits a measured output power of −13.5 dBm, a tuning range of 8 GHz (204.7–212.7 GHz), and a phase noise of −81 dBc/Hz at 1 MHz offset at 209 GHz (Fig. 22). The VCO plus the buffer and OOK modulator consumes a total of 42 mA from a 1-V supply.

B. 210-GHz LNA

Common source (CS) and cascode topologies are the most popular topologies for LNA design [37]. However, at frequencies close to $f_T/f_{\max}$, not only the gain of cascode amplifiers drops to almost that of a CS (due to the parasitic capacitance seen at the intermediate node of the cascode amplifier), but also the noise contribution of the common gate (CG) device to the cascode's NF becomes significant (∼0.5–1 dB higher NF compared to a CS amplifier). Nevertheless, a shunt or series inductance [38] can be placed between the CS and the CG devices, as an inter-stage matching network, to increase the impedance seen by CG device, thereby alleviating gain and NF degradation issues. However, CS topology was chosen for this design, since, for the given technology, after accounting for the loss of required inter-stage matching network, the CS topology outperforms the cascode topology in terms of gain and NF and therefore is chosen for the design.

Since the very first stage of an LNA mostly determines its NF, the design goal for the first stage of the LNA was to find the

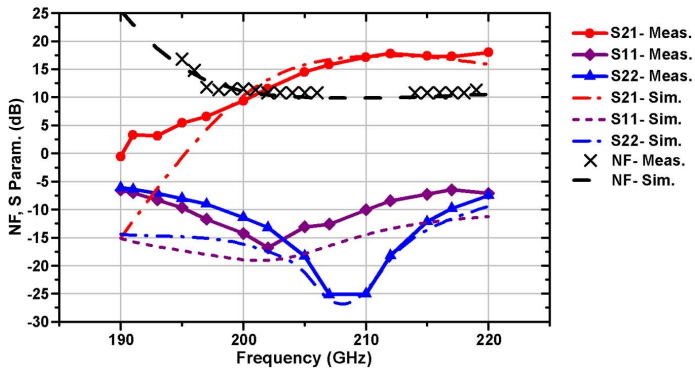


Fig. 25. Measurement results for LNA.

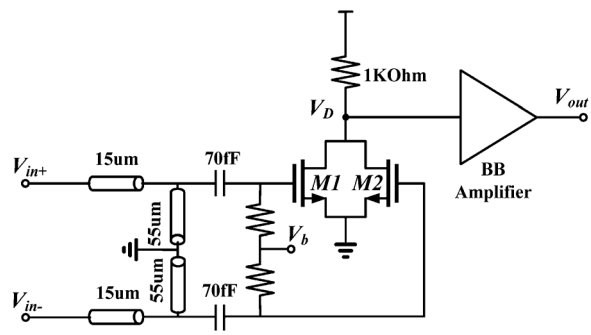


Fig. 26. Schematic of the 210-GHz CMPS OOK envelop detector ($M1$and $M2$) followed by a baseband amplifier.

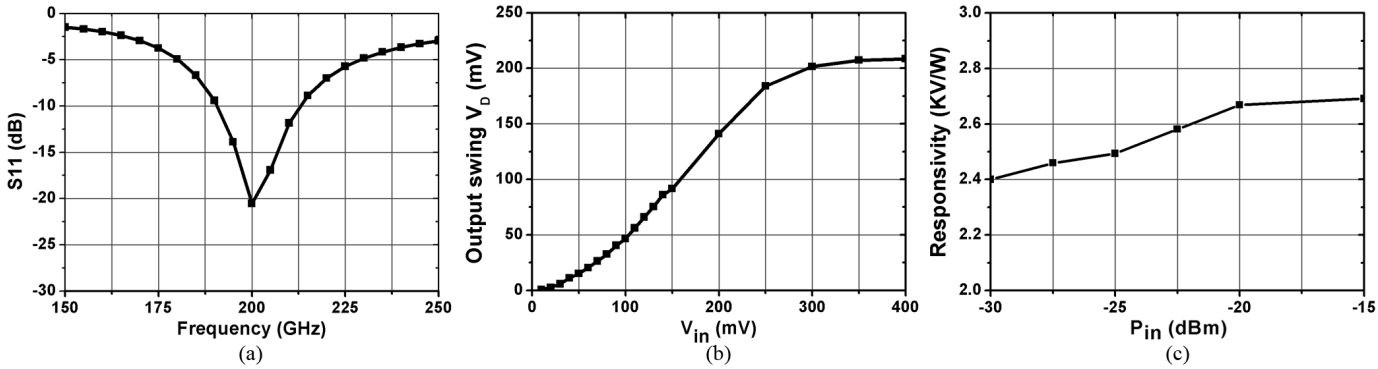


Fig. 27. Simulation results for detector. (a) Input return loss. (b) Output swing of V_D versus $V_{\rm in}$ for input signal of 200 GHz. (c) Responsivity versus $\rm P_{in}$ with input carrier frequency of 200 GHz and baseband signal with BW of 5 GHz.

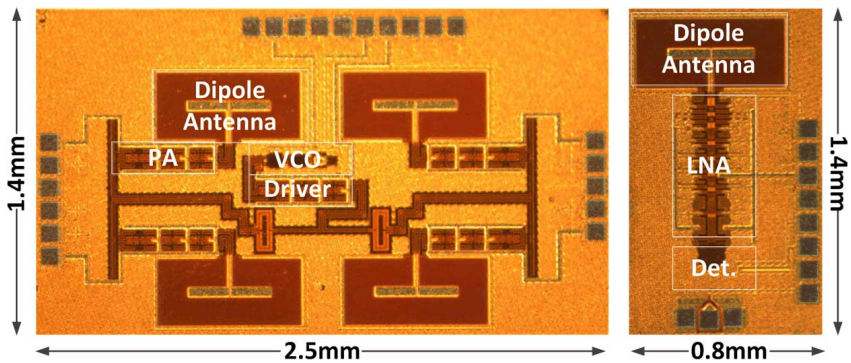


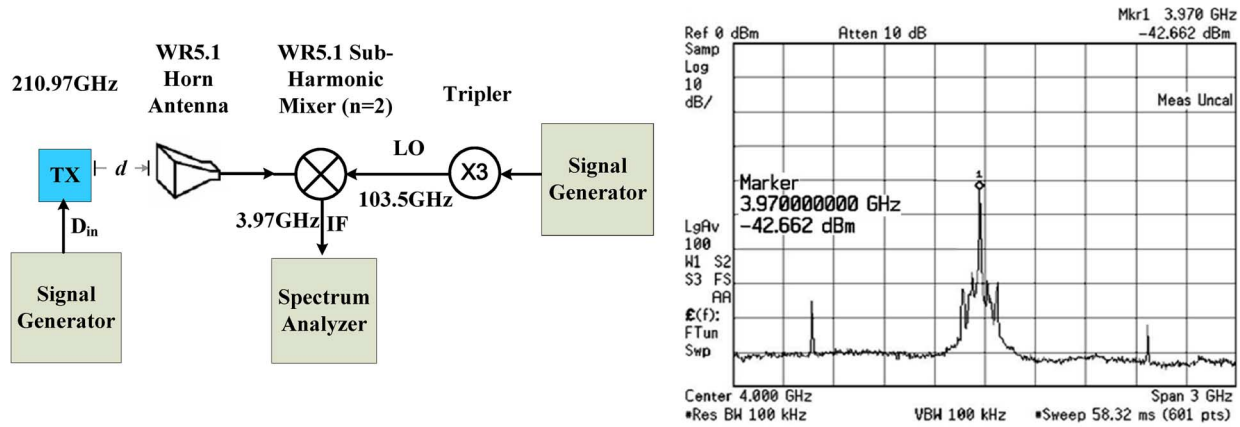
Fig. 28. Die photograph of the TRX.

optimum current density $(J_{\rm opt})$ and finger width for $\rm NF_{min}$. However, the maximum achievable gain of the device was too low when biased at $J_{\rm opt}$ (∼2–3 dB including the loss of input/output matching networks). Consequently, the first stage was unable to suppress the noise contribution of the subsequent stages; hence, the overall NF was drastically degraded. Therefore, a higher current density of 0.22 $\rm mA/\mu m$ as opposed to $J_{\rm opt} = 0.16\ \rm mA/\mu m$ was chosen to minimize the overall NF for a given finger width of 400 nm. $NF_{\rm min}$ of the first stage was only degraded by 0.05 dB for this current density shown in Fig. 23(a).

Inductive degeneration in the LNA design is commonly used to transfer the input impedance $Z_{\rm in}$ of the device to a value close to $Z^*_{\rm opt}$ to achieve simultaneous noise and power match [37]. In this approach, $R_{\rm opt} = \rm Re[Z_{opt}]$ is assumed to be independent of the degeneration inductance $L_{\rm deg}$. However, as the CMOS technology further scales down to nanoscale regime, $R_{\rm opt}$ becomes a stronger function of L_{deg}. Thus, the effect of $L_{\rm deg}$ on both $R_{\rm opt}$ and $B_{\rm opt} = \rm Im[Z_{opt}]$ should be taken into account. The goal is, therefore, to minimize the Euclidean distance between Z_{opt} and $Z^*_{\rm in}$, rather than only focusing on real part of the input impedance. Fig. 23(b) shows $Z_{\rm opt}$ and $Z^*_{\rm in}$ on the Smith chart as L_{deg} varies, clearly indicating variation in $R_{\rm opt}$. The distance between $Z_{\rm opt}$ and $Z^*_{\rm in}$ $(\Delta\Gamma)$ is calculated and plotted in Fig. 23(c). During the design, existing tradeoff between $\Delta\Gamma$ and $G_{\rm max}$ was accounted for so as to avoid too much gain degradation. At the same time, K_f is ensured to be greater than unity (i.e., unconditional stability) shown in Fig. 23(d). The $\rm NF_{min}$ variation vs. $L_{\rm deg}$ is also depicted on the same plot. As expected, the inductive degeneration slightly reduces $\rm NF_{min}$ [39].

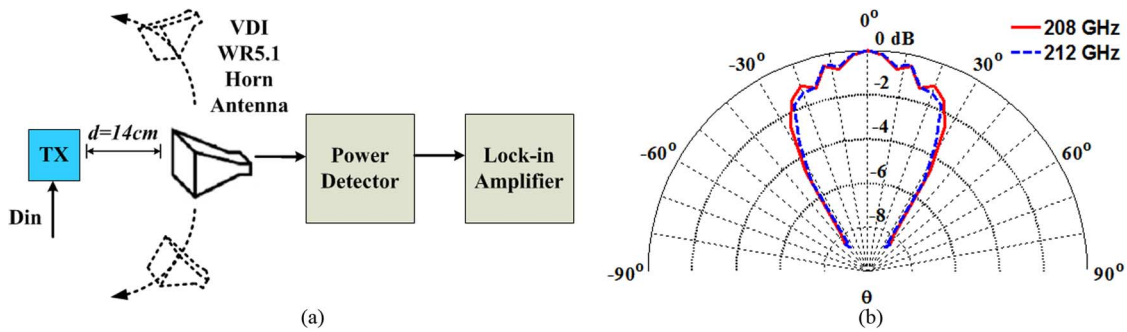
Fig. 24 shows the schematic of the seven-stage differential LNA. It turns out that the gain of the first stage is still insufficient to suppress the noise contribution of the second stage. Therefore, the current density of the second stage is also chosen to be identical to that of the first stage to minimize its noise contribution to the overall NF. The succeeding stage has been biased at current density of 0.56 $\rm mA/\mu m$ corresponding to maximum $f_{\rm max}$. Thus, highest gain per stage is achieved. For the first two stages, simple second-order matching networks is used to minimize the noise contribution of lossy on-chip passives. As for the succeeding five stages, fourth-order matching networks have been incorporated to achieve a wide 3-dB gain bandwidth (>15 GHz).

The LNA core occupies only 400×650 $\mu\rm m^2$. It has been tested by a set up composing of G-band (140–220 GHz) RF probe and vector network analyzer (VNA). The LNA exhibits a measured peak gain of 18 dB with a BW of at least 15 GHz, as shown in Fig. 25. The measured bandwidth in this design is limited by the highest measurable frequency (220 GHz) of the test equipment. Input/output return losses are better than 8 dB. The LNA's in-band NF has been estimated from the RX's output SNR measurement. Accounting for measured 18-dB gain for the LNA, the receiver's NF is mostly dominated by the LNA's NF. Therefore, the LNA's NF is upper-bounded by the receiver's NF, which approximately varies between 11 and



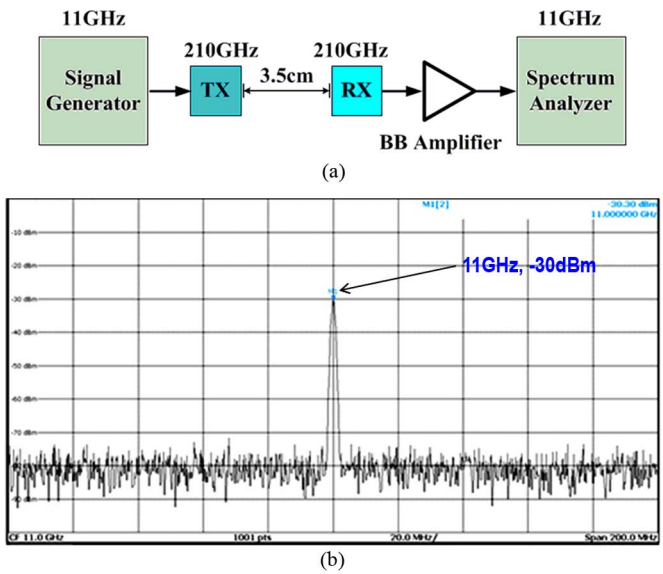
(a) (b)

Fig. 29. Transmitter spectrum measurement. (a) Test setup. (b) Measured IF spectrum after down-conversion.



(a) (b)

Fig. 30. Transmitter power measurement. (a) Test setup. (b) Measurement radiation pattern.



(a)

(b)

Fig. 31. CW wireless link over 3.5 cm. (a) Test setup. (b) Measured baseband spectrum after receiver.

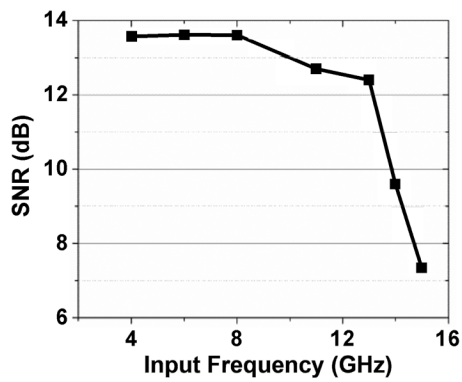


Fig. 32. Measured output SNR with respect to baseband signal frequency.

12 dB, as shown in Fig. 25. The LNA draws 44.5 mA from a 1-V supply.

C. Power Detector

Fig. 26 shows the schematic of OOK envelop detector followed by a baseband amplifier. The series-shunt CPW transmission lines are used for input matching. As shown in Fig. 27(a), the input return loss is less than -10 dB at the center frequency of 200 GHz over a bandwidth of 20 GHz. For the envelop detector, the transistors M1 and M2 are biased in class-AB operation region so as to provide square-law relationship between $V_{\rm in}$ and V_D. When differential voltage $V_{\rm in}(= V_{\rm in+} - V_{\rm in-})$ is larger than zero, M2 turns off and M1 turns on, drawing a current which is proportional to $V_{\rm in}^2$. This square-law characteristic has been verified by simulation of the detector, which is shown in Fig. 27(b). V_D is expressed as [32], [40]

$$V_D \cong \frac{1}{4}\mu_n C_{\rm ox}\left(\frac{W}{L}\right)_{1,2} R_L V_{\rm in}^2. \tag{18}$$

Operation in the square-law region increases the V_D's swing and improves the detector's responsivity. Shown in Fig. 27(c) is the simulation result of the detector responsivity vs. input power at the input carrier frequency of 200 GHz and baseband

TABLE I
PERFORMANCE SUMMARY OF THE 210-GHZ CMOS TRANSCEIVER

VCO		**LNA**	
Output Power	-13.5dBm	S21	18dB
Tuning Range	204.7-212.7 GHz	Bandwidth	>15GHz*
Phase noise	-81dBc/Hz @ 1MHz offset	Return Loss	>8dB
Power Consumption	42mW		
PA		**TRX**	
		EIRP	5.13dBm
Power Gain	15dB	RX's minimum NF	11 dB
OP1dB	2.7dBm	Bandwidth	>14GHz*
Psat	4.6dBm	Beamwidth	57deg
PAE	6%	TX Power Consumption	240mW
Power Consumption	40mW	RX Power Consumption	68mW

* Measurement limited to 220 GHz.

signal with bandwidth of 5 GHz. As can be seen, the responsivity varies within 10% around the nominal value of 2.5 KV/W as input power P_{in} varies from -30 to -15 dBm. This result is consistent with square-law operation. The responsivity can be further improved with additional baseband amplifier at the expense of lower dynamic range. Note that the load resistor R_L with the parasitic capacitance of the baseband amplifier forms a low-pass filter which filters out undesired harmonics generated by M1 and M2 and the 200-GHz ripples from input signal.

VI. MEASUREMENTS

A. Chip Fabrication

The 210-GHz TRX chip has been fabricated in a 32-nm SOI CMOS with $f_{\rm T}/f_{\rm max} =$ 250/320 GHz. Fig. 28 shows the die photograph of the TRX chip. The TX and RX occupy 1.4×2.5 mm^2 and 0.8×1.4 mm^2 of chip areas, respectively (including pads). The on-chip antennas are fabricated on the substrate with resistivity of 13.5 Ω-cm without any post process. The array elements are separated by 820 μm, which corresponds to approximately $0.57 \times \lambda$ at 210 GHz. A chip-on-board assembly is used to characterize the performance of the 210-GHz TRX chip. Owing to the on-chip antenna integration, a low-cost assembly was achieved without any millimeter-wave bonding.

B. System Measurements

The TX spectral measurement was carried out by utilizing the setup shown in Fig. 29(a). The transmitted signal from the TX chip is captured by a VDI WR5.1 horn antenna and then down-converted by a VDI WR5.1 subharmonic mixer. The W-band LO generation chain is composed of a signal generator and a W-band tripler. The down-converted IF signal is monitored by a spectrum analyzer. The IF spectrum exhibits modulated signal with the center tone located at 3.97 GHz shown in Fig. 30(b). The harmonic number for the WR5.1 subharmonic mixer is two, and the actual RF frequency from the TX is 210.97 GHz. Two sidebands in Fig. 29(b) represent the OOK modulated signals, which are 1 GHz apart from the carrier tone. Since conversion gain of the subharmonic mixer was not calibrated, accurate power measurement needs to be done by employing another method, as explained below.

Considering that the path loss from the TX antenna to the RX antenna for the 210-GHz signal is quite high (i.e., about 61.8 dB for a TX–RX distance of 14 cm), the power captured by power sensor is less than 1 μW. This makes it quite difficult to measure the TX power directly using power sensor. Placing the RX antenna closer to the TX can potentially yield higher power. However, the path loss estimated by Friis formula is not accurate when the RX antenna is not located in the far-field region. The measurement setup of Fig. 30(a) can measure the TX power for this OOK-modulation-based TX. A 1-kHz signal is used to modulate the 210-GHz carrier signal. After being captured by the WR5.1 horn antenna, the signal is detected by a G-band detector. A lock-in amplifier senses the voltage difference between on-state and off-state signals. The responsivity of the external G-band detector has been well calibrated using an external G-band source with different input power. Accounting for a responsivity of 440 V/W for the detector and 21 dBi of gain for VDI WR5.1 horn antenna in Fig. 30(a), the captured power translates to a broadside EIRP of 5.13 dBm. This 5.13-dBm EIRP exhibits 10-dB back-off from a saturated power of 15.2 dBm (4.6-dBm Psat of one PA + 6-dB combining gain + 4.5-dBi antenna gain), which is due to insufficient power from on-chip LO and routing loss. By rotating the horn antenna, the TX radiation pattern is also measured, as shown in Fig. 30(b). The measured beamwidth remains almost constant across the band, and it is 57° and 54° at 208 and 212 GHz, respectively.

A modulated continuous-wave (CW) wireless testing between TX and RX chip has been performed over a distance of 3.5 cm, as shown in Fig. 31(a). A baseband signal is sent to TX chip and then modulated to a 210-GHz carrier and radiated out. The RX chip captures the 210-GHz signal and detects the baseband signal and then monitors using a spectrum analyzer. The output-noise spectral density was also measured from spectrum analyzer. Accounting for RX bandwidth of 20 GHz, the output signal-to-noise ratio (SNR) was thus calculated. An external low-noise baseband amplifier is used to help increase the strength of the received signal. The amplifier's noise has negligible contribution to the output SNR, as it is attenuated by the LNA gain. By sweeping the frequency of baseband signal,

TABLE II
COMPARISON TABLE

	[11]	[12]	[13]	[14]	This work
Technology	45nm SOI CMOS	45nm SOI CMOS	0.13μm BiCMOS	65nm CMOS	32nm SOI CMOS
Frequency	291GHz	280GHz	380GHz	260GHz	210GHz
Architecture	2×2 DAR	4×4 DAR	Quadrupler-based TRX	2×2 Quadrupler-based TRX	2×2 Fundamental Frequency TRX
Modulation	None	None	FMCW	OOK	OOK
EIRP [dBm]	-1	9	-13	5	5.13 (15.2 @ P_{sat}) *
P_{DCTX} [mW]	74.8	430	182	688	240
EIRP/P_{DCTX}	1.1%	2%	0.028%	0.46%	1.4% (>6.9% @ P_{sat}) *
Area [mm^2]	0.64	7.29	4.18	6	3.5 (TX) + 1.12 (RX)

* The EIRP if the PAs are fully driven is 15.2 dBm (4.6 dBm Psat of one PA + 6-dB combining gain + 4.5-dBi antenna gain). With a stronger PA driver, the power consumption is assumed to double (a conservative estimation) to be 480 mW, and the expected $\mathrm{EIRP}/\mathrm{P}_{\mathrm{DCTX}}$ is 6.9%.

the output SNR for different CW frequencies has been obtained, as shown in Fig. 32. Considering that the TRX system operates in the linear region (TX is 8 dB back-off from OP1 dB), the thermal noise limits the performance of the wireless links rather than nonlinearity. In this case, with the requirement of SNR of 13 dB (corresponding to BER of 10^{-5} for noncoherent OOK modulation), the maximum baseband frequency is 10 GHz, which corresponds to a potential data rate of between 10 Gbps for no root-raised-cosine (RRC) filtering and 20 Gbps for ideal filtering. The RX sensitivity of -47 dBm corresponds to an RX NF of around 12 dB. The measured performance of the 210-GHz TRX is summarized in Table I. Table II compares this work with other state-of-the-art silicon-based signal sources or TRXs.

VII. CONCLUSION

A fully integrated 210-GHz fundamental TRX with on-chip antenna is demonstrated in 32-nm SOI CMOS technology. To the best of the authors' knowledge, this was the first known demonstration on a 210-GHz fundamental CMOS TRX. The neutralization technique was revisited and an over-neutralization technique is proposed to boost the power gain effectively for transistors in the near-$f_{\max}$ region. A first CMOS PA is demonstrated at 210 GHz with measured 15-dB gain (5 dB gain per stage) and 4.6-dBm output saturation power. A CMOS LNA with 18-dB gain was achieved at 210 GHz with more than 15-GHz bandwidth. The 2×2 spatial combining TX achieves an EIRP of 5.13 dBm at 10-dB back-off from saturated power. It achieves an estimated EIRP of 15.2 dBm when the PAs are fully driven. This work demonstrates the feasibility of using CMOS technology for chip-to-chip wireless communication with potential data rate of between 10 Gbps for no RRC filtering and 20 Gbps for ideal filtering.

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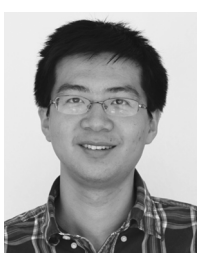

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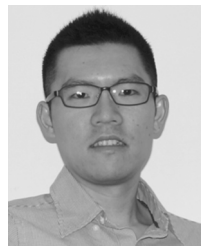

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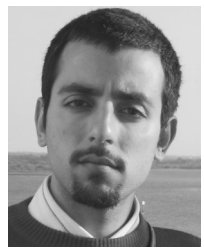

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