ON-CHIP TRANSFORMER MODELING, CHARACTERIZATION, AND APPLICATIONS IN POWER AND LOW NOISE AMPLIFIERS

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Abstract

A fully integrated radio-frequency (RF) front-end transceiver having no board-level components is highly desirable in order to lower costs. Typical RF front-end circuits are differential to minimize the effect of ground noise on a low noise amplifier (LNA) and to double the output power of a power amplifier (PA) under the same supply voltage. Baluns are thus needed to interface the differential RF circuits with the single-ended antenna. Low insertion loss is desired for on-chip transformer baluns because it directly affects the noise figure of LNA and the output power of PA.

In this work, a compact model for various on-chip spiral transformers was first developed and verified by simulation and experiment. A new layout technique was introduced to achieve high magnetic coupling coefficient and low insertion loss by segmenting and interleaving wide primary and secondary traces. Using the model and layout technique, a fully integrated front-end with on-chip transformers individually optimized for the LNA and PA, and targeted for medium power applications (e.g., WLAN) was designed and fabricated in a 0.18μm 1P5M 1.8V/3.3V standard digital CMOS technology. The receive path achieves S_{21} of 17dB, NF of 4.1dB and IIP3 of 0dBm at 2.45GHz. The PA achieves P_{sat} of 21dBm, P_{1dB} of 17dBm, and max PAE of 21%.

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Chapter 1

Introduction

The phenomenal growth of the wireless communication markets, such as cellular phones, wireless local area networks (WLAN) and other hand-held devices, has generated tremendous interest in low-cost, silicon-based, radio-frequency integrated circuits (RFICs) using complementary metal-oxide-semiconductor (CMOS) technology. The constantly shrinking feature size of CMOS technologies has resulted in deep submicron CMOS transistors, which permit the integration of the analog and digital components for "system-on-chip" solutions. Fully integrated single chip solutions are desired to eliminate off-chip components and to reduce cost. This chapter first provides an overview of some wireless communication systems and then presents the motivation behind a high level of integration. Finally, it shows the organization of the dissertation.

1.1 Background

After more than a decade of fast growth, portable wireless devices have become part of our daily lives. Figure 1.1 shows some popular applications for wireless communications. A wireless communication standard provides the framework within which the system is designed and operated, such as the operation frequency, channel allocation, modulation scheme, sensitivity, and output power level. The standard is essential to the proper

operation of the system as well as to the coexistence of other systems under different standards.

Table 1.1 summarizes some typical wireless communication systems. The Global System for Mobile communication (GSM) and IS-95 direct-sequence code-division multiple access (CDMA) systems are second-generation (2G) cellular phone systems [1]. They are very successful in Europe and the United States, respectively. The data rates are about 9.6kbps. To increase the data rate, some 2.5G communication systems have been developed, such as the General Packet Radio Service (GPRS), the Enhanced Data GSM Environment (EDGE), which have data rates of over 100kbps. These 2.5G standards are stepping stones between the 2G and 3G cellular wireless technologies. They support not only voice communications but also data services.

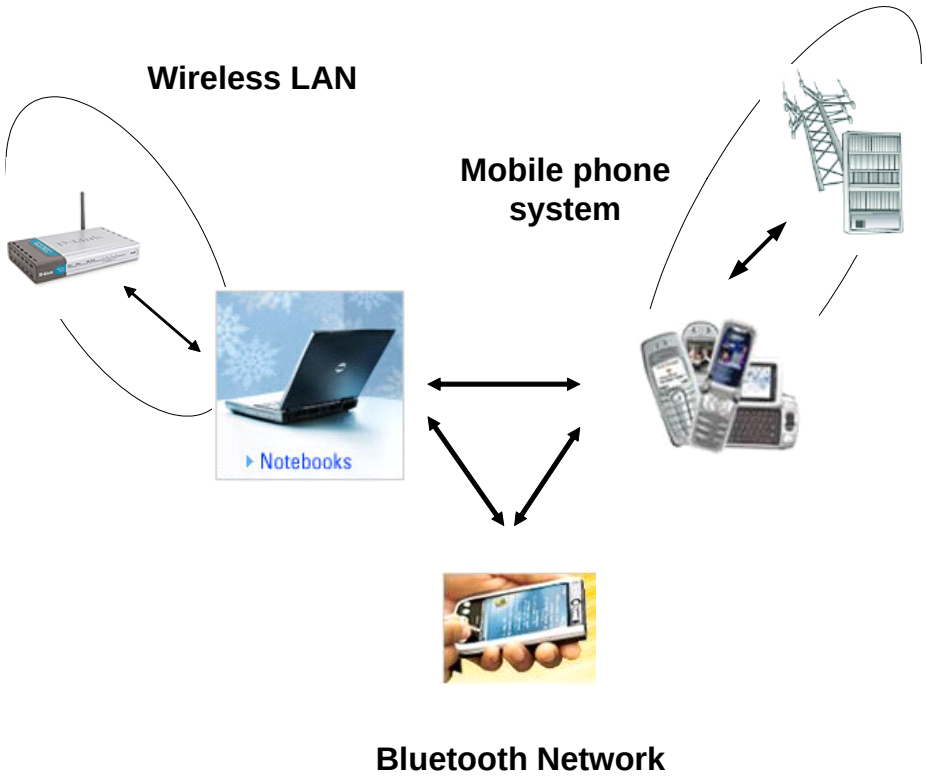


Figure 1.1: Some wireless communication systems.

Wideband CDMA/Universal Mobile Telecommunications System (UMTS) [2] is one

of the 3G cellular wireless communication standards. The maximum data rate is up to 2Mbps. Due to cost and complexity, the rollout of the 3G system has been slower than anticipated.

For cellular communications, the output power level is relatively high (∼30dBm) to allow large cell size. Many of the cellular systems utilize frequency-division duplexing (FDD) with a combination of frequency division multiple access (FDMA), time division multiple access (TDMA) and code division multiple access (CDMA) for multiple access.

The Personal Handy-phone System (PHS) provides a cheap solution for mobile communications in urban areas at walking speeds [1]. It employs a micro-cell architecture and is designed to be used in an Integrated Services Digital Network (ISDN) that accommodates ordinary wired telephones. As an extension of cordless phones, its output power level is much smaller than that of most cellular communication systems.

Applications	Standard	Frequency (MHz)	Modulation Scheme	Transmit Power (dBm)
Mobile phones	GSM	890-915(up) 935-960(down)	GMSK	36
	CDMA(IS-95)	824-849(up) 869-894(down)	O-QPSK	28
	PHS	1895-1918	$\pi/4$ DQPSK	10
	WCDMA (UMTS)	1920-1980(up) 2110-2170(down)	QPSK	33
Bluetooth	Bluetooth	2400-2484	FSK	4
Wireless LAN	802.11b	2400-2484	PSK-CCK	16-20
	802.11a	5150-5350	OFDM	14-19
	802.11g	2400-2484	OFDM	16-20

Table 1.1: Some typical wireless communication standards.

Bluetooth [3] applications operate at the unlicensed ISM band at 2.4GHz. They usually have a range of up to 10 meters and a data rate of up to 1Mbps. The standard aims to replace the wires between devices, such as PC peripherals, mobile phones and

headsets. It uses frequency-hopping spread spectrum (FHSS) transmission technology.

Wireless LAN [4] applications (802.11a/b/g) have a longer range (30-meter) and higher data rate than Bluetooth applications. For 802.11b/g, the direct-sequence spread spectrum (DSSS) is used so that WLAN applications won't interfere with Bluetooth applications in the same frequency range. The orthogonal frequency division multiplexing (OFDM) modulation scheme is used in 802.11a and g to achieve a high data rate, with a stringent requirement on transmitter linearity due to the large peak-to-average ratio of the OFDM modulation. The output power level is medium (around 20dBm) to cover the 30-meter range with a high data rate.

As the demand for wireless multimedia data transmission grows higher, some wideband technologies and new standards are under consideration. Among them are multiple-input multiple-output (MIMO), Ultra-Wide Band (UWB) and Worldwide Interoperability for Microwave Access (WiMAX/802.16).

1.2 Motivation for Integration

As the fierce price competition for handheld devices continues, the advantages of integrating RF circuits with analog and digital circuits are compelling. Although the aggressive scaling of CMOS devices does not always benefit the performance of RF circuits, the progressively smaller submicron CMOS device provides an increasingly higher f_T and f_{max}, which enable an RF front-end with sufficient performance in the GHz frequency range to be integrated with baseband circuits on a single chip. There is a similar desire to reduce the number of passive components on board, which will lead to smaller board size and usually lower power consumption. Furthermore, single chip solutions enhance the reliability and controllability of the end products because the variation of integrated devices is smaller than that of the discrete devices on board.

Fully integrated CMOS Low noise amplifiers (LNAs) [5] and power amplifiers (PAs) [6] have been realized. Figure 1.2 shows a conventional RF front-end architecture. The

Transmit/Receive (T/R) switch is used for time-division duplexing (TDD) communication systems, such as 802.11 Wireless LAN applications. Differential circuits are often chosen to reduce the effect of ground noise in LNA circuits and double the output power level for PAs under the same supply voltage. However, antennas are often single-ended. Therefore, baluns are needed to interface the single-ended antenna to differential circuits on-chip. Traditionally, baluns are realized on the board. Thus, proper impedance transformation and matching networks are often needed on the board too. Expanding the chip boundary to the single antenna pin is desirable to eliminate these off-chip components and lower the cost.

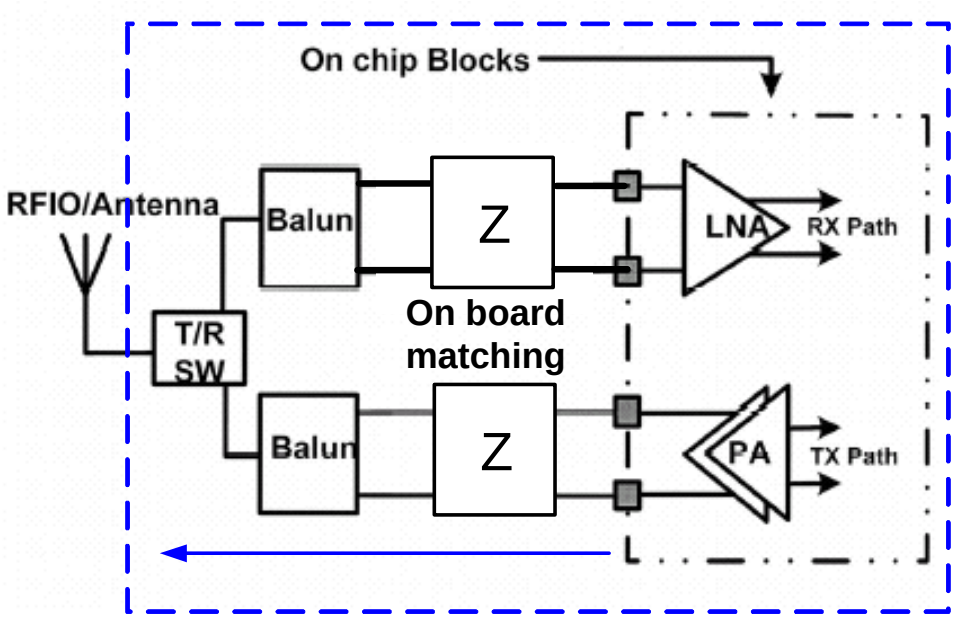


Figure 1.2: Conventional RF front-end architecture.

Bhatti [7] presented a multi-tap transformer-based balun solution (shown in Figure 1.3) for Bluetooth applications. This solution used cascode devices and/or bias transistors as T/R switches. The transformer combined the functionalities of baluns and matching networks for both LNA and PA. One problem with this solution is that it may compromise the isolation between the receive and transmit paths. It also needs careful tuning for each path. Optimizing the transformer for both LNA and PA is difficult.

There are several challenges for fully-integrated RF front-end of medium (∼20dBm) and high power (∼30dBm) applications. The important ones are:

1. The different functionalities of LNA and PA require different transformation networks for optimal performance. For LNA, input noise matching is desired to minimize noise figure; for PA, wide traces are often needed to handle high DC current.

2. Low quality factor passive components, e.g., on-chip inductors/transformers can compromise performance.

3. To save chip area and reduce insertion loss, function blocks must be combined.

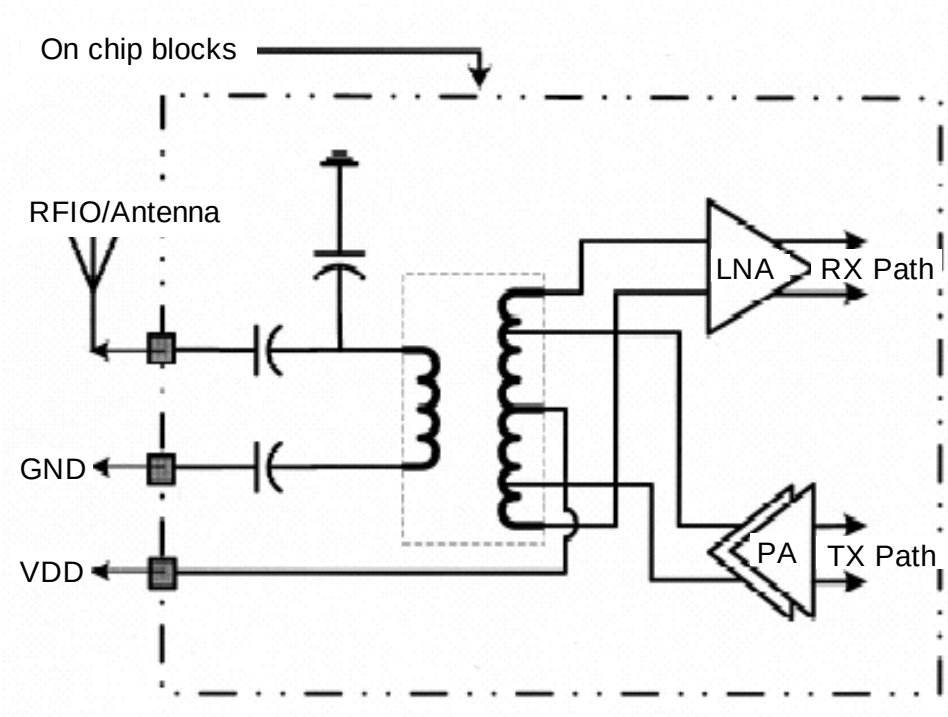


Figure 1.3: Transformer-based balun solution for Bluetooth applications.

1.3 Organization

This dissertation describes the design and performance of a fully integrated front-end with on-chip transformers individually optimized for LNA and PA and targeted for medium

power applications, e.g., WLAN. On-chip transformers combine the functions of baluns and matching networks. A variation of an integrated T/R switch solution with high power handling ability presented by Talwalkar [8] is used.

Chapter 2 begins with an overview of on-chip transformers, basic circuits and various layout structures. Transformers of 3-port and 4-port are also discussed in more detail. Then a broadband compact transformer model is derived, based on the analysis of high frequency phenomena that degrade transformer performance such as capacitive coupling, shield loss, and skin and proximity effects. The performance parameters of transformers, such as magnetic coefficient k and minimum insertion loss (ILm), are then introduced.

Chapter 3 first discusses the relationship between the transformer geometry and k. Then a new layout scheme is introduced to improve the k and ILm for wide Various transformer structures were fabricated in the Stanford Nanofabrication Facility (SNF). The measurement results are compared to the EM solver HFSS and to the compact circuit model results. They match well up to 4GHz. The model enables optimization of planar transformers.

Chapter 4 first summarizes the basic characteristics of different classes of power amplifiers. Different output baluns and matching networks for PAs are also presented. Then two layouts of transformer baluns using segmenting and interleaving scheme are discussed in detail, and their fabrication and measurement results are presented. A one-stage class AB push-pull power amplifier with an output transformer balun was fabricated in a 0.18μm 5 metal digital process. The measurement shows it to be suitable for 802.11b/g wireless LAN application.

Chapter 5 begins with reviews of different configurations of low-noise amplifiers. A fully integrated receive path with a receive switch, an input transformer balun and an inductive source-degenerated common source LNA is presented. The receive path is designed for 2.4GHz wireless LAN applications. The measurement results for the receive path are summarized. Finally a fully-integrated RF front-end architecture using the receive path and the PA discussed in Chapter 4 is presented.

The results of this research are summarized in Chapter 6, and future work is suggested.

Chapter 2

Transformer Model

This chapter discusses the modeling of on-chip transformers. Section 2.1 introduces the ideal transformer circuit and its variations. In Section 2.2, transformers with three and four ports are discussed in more detail. Section 2.3 briefly reviews different types of transformers and compares their advantage and disadvantage. Section 2.4 discusses detailed modeling issues of non-ideal transformers, such as capacitive coupling, skin and proximity effect, etc. A broadband transformer circuit model is also presented. Then the minimum insertion loss is introduced in section 2.5 as a figure of merit (FOM) to characterize the performance of transformers. A short summary is given in Section 2.6.

2.1 Transformer Fundamentals

2.1.1 Ideal transformer

The circuit model of an ideal transformer is shown in Figure 2.1. The magnetic flux produced by time-varying current I_1 flowing into the primary winding, induces a time-varying current of I_2 in the secondary winding.

The terminal voltages and currents of this ideal transformer are related as follows:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} j\omega L_p & j\omega M \\ j\omega M & j\omega L_s \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2.1}$$

where L_p and L_s are the self-inductance of the primary and secondary. M is the mutual inductance between the primary and secondary. The magnetic coupling coefficient k is given by

$$k = \frac{M}{\sqrt{L_p L_s}} \tag{2.2}$$

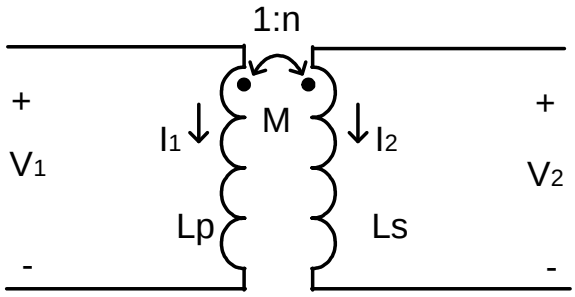


Figure 2.1: An ideal transformer.

For an ideal transformer, $k = 1$. For most on-chip transformers, k is between 0.3 to 0.9, due to the leakage of magnetic flux. Other non-idealities of practical on-chip transformers include parasitic capacitance, resistances due to ohmic loss, skin effect, proximity effect and substrate eddy current. These non-idealities will be discussed in more detail in Section 2.4. Another electrical parameter of interest is the transformer turn ratio n. It is related to the current and voltage transformation of the primary and secondary by

$$n = \sqrt{\frac{L_s}{L_p}} \approx \frac{V_2}{V_1} \approx \frac{I_1}{I_2} \tag{2.3}$$

2.1.2 Variations and circuit applications

Monolithic transformers have been used extensively in RF circuits. A transformer can be configured as a 2-port, 3-port or 4-port device as shown in Figure 2.2. The 2-port inverting transformer is often realized as a symmetric inductor with the center tap grounded. It is used in many differential circuits such as the load inductors or the source degenerated inductors in LNA circuits. The 2-port non-inverting transformer usually has smaller effective inductance, thus the self-resonant frequency is usually high. The 3-port transformer is often used as a single-ended to differential converter (balun) in LNA and PA circuits. The 4-port transformer has two pairs of differential ports and is often used in differential mixer circuits.

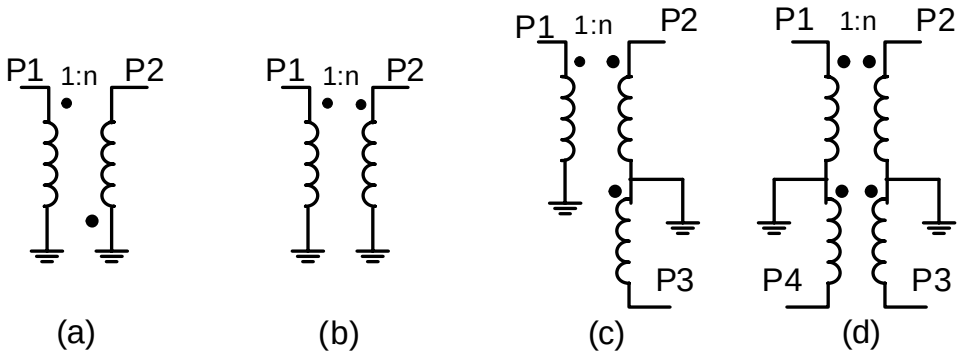


Figure 2.2: Transformer variations: (a) 2-port inverting, (b) 2-port non-inverting, (c) 3-port (balun), and (d) 4-port.

2.2 Balanced Device Characterization

Differential circuits are highly desirable in RF applications. They offer immunity from many noise sources, such as power supplies and digital circuits. Even-order harmonics are suppressed due to the symmetry. The bonding requirement for the virtual ground is largely relaxed. However, it is not easy to measure and characterize a device with more than two ports. For example, a 4-port transformer has four self-inductances and six k's.

To simplify the characterization process, we can exploit the symmetry of the differential circuits.

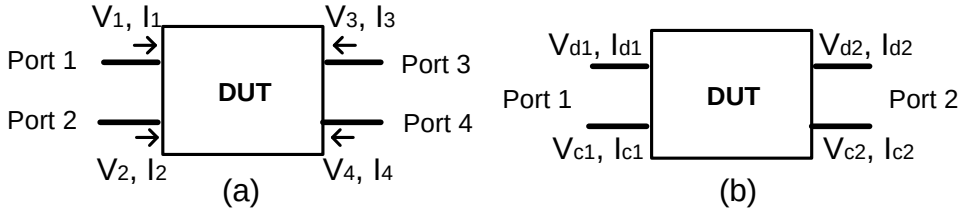


Figure 2.3: A 4-port device: (a) single-ended: ports referenced to ground; (b) mixed-mode: ports are in pairs, both with differential mode and common mode.

A 4-port device can be characterized in two ways, as shown in Figure 2.3:

- Single-ended: all four ports are referenced to ground.
- Mixed-mode: two pair of ports, both with differential mode and common mode.

The relationships between the two methods are shown in Table 2.1.

Differential Mode		Common Mode	
Port1	Port2	Port1	Port2
$V_{d1} = V_1 - V_2$	$V_{d2} = V_3 - V_4$	$V_{c1} = 0.5(V_1 + V_2)$	$V_{c2} = 0.5(V_3 + V_4)$
$I_{d1} = 0.5(I_1 - I_2)$	$I_{d2} = 0.5(I_3 - I_4)$	$I_{c1} = I_1 + I_2$	$I_{c2} = I_3 + I_4$

Table 2.1: Voltage and current relationships for the single-ended and the mixed-mode.

We can relate the single-ended S-parameter S_{se} to the mixed-mode S-parameter S_{mm} through the linear transformation

$$S_{se} = M^{-1} S_{mm} M \tag{2.4}$$

where

$$S_{se} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}; S_{mm} = \begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{bmatrix};$$

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}.$$

The mixed-mode S-parameter S_{mm} can be divided into four 2-by-2 matrices S_{dd}, S_{cc}, S_{dc}, S_{cd} with subscripts corresponding to differential mode to differential mode, common mode to common mode, differential mode to common mode, and common mode to differential mode, respectively. For a well-designed symmetrical device, there will be little conversion between differential mode and common mode. So S_{dc} and S_{cd} are a measure of device symmetry.

Similarly, a 3-port device with a single-ended port 1 and two differential ports 2 and 3 has the relationship

$$S_{se} = M^{-1} S_{mm} M \tag{2.5}$$

where

$$S_{se} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix}; S_{mm} = \begin{bmatrix} S_{ss11} & S_{sd12} & S_{sc12} \\ S_{ds21} & S_{dd22} & S_{dc22} \\ S_{cs21} & S_{cd22} & S_{cc12} \end{bmatrix}; M = \frac{1}{\sqrt{2}} \begin{bmatrix} \sqrt{2} & 0 & 0 \\ 0 & 1 & -1 \\ 0 & 1 & 1 \end{bmatrix}.$$

The imbalance between the two differential ports can be characterized through phase and amplitude:

- Phase imbalance

$$\theta = \left| \tan^{-1} \frac{\mathrm{Im}(S_{21}/S_{31})}{\mathrm{Re}(S_{21}/S_{31})} \right| \tag{2.6}$$

- Amplitude imbalance(dB) $= 20 \log(S_{21}/S_{31})$

Thus we can transform a multi-port device such as a 3-port or a 4-port transformer to a mixed-mode 2-port device and extend our knowledge regarding a single-ended 2-port system to a mixed-mode 2-port system, which is helpful for circuit design and device characterization.

2.3 Basic Transformer Structures

For different transformer structures, the coupling coefficient k, the turn ratio n, and other parameters may vary considerably. Depending on whether the lateral or vertical magnetic coupling is used, transformer structures have two categories: planar or stacked. Some circuits (e.g., differential circuits) prefer transformers with a symmetrical layout. Planar and stacked transformers are discussed below.

2.3.1 Planar transformer

As shown in Figure 2.4, there are many variations in planar transformer realization [9]. Planar transformers usually occupy a large area. In a multi-layer metal process, several top metal layers can be strapped together to reduce resistance. The tradeoffs are a larger terminal-to-substrate capacitance and a smaller self-resonant frequency.

Figure 2.4(a) shows a tapped 2-port transformer. It is actually an inductor with a middle tap. It allows a large range of turn ratios, although the coupling coefficient k is usually small ($0.3 \sim 0.5$). It is not a symmetric design.

Figure 2.4(b) shows a Shibata transformer: the primary and secondary are wound in parallel. It too, is asymmetric. Although the number of turns is the same for the primary and secondary, the self-inductances are not exactly the same. So $n \neq 1$.

Figure 2.4(c) shows a Frlan transformer, which is center symmetrical. It is useful for some applications that demand symmetry, but contacting the center tap of either primary or secondary is difficult.

Figure 2.4(d) shows a layout that is suitable for 3 or 4-port applications with center taps at about half of the physical length. The turn ratio is around 3:2.

For some applications, we want a high turn ratio to boost voltage gain or current gain. Figure 2.4(e) shows a symmetric realization for a 1:3 step-up transformer. To reduce the proximity effect and equalize the physical length of the three parallel branches, more cross-over is used in Figure 2.4(f). This geometry will improve the coupling coefficient k, but more metal layers are required, and via resistance also needs to be justified.

Figures 2.4(b) to (f) are all interleaved transformer variations. They have moderate coupling ($k \sim 0.7$) with reduced self-inductances and larger terminal-to-terminal capacitances.

2.3.2 Stacked transformer

A stacked transformer using three metal layers is shown in Figure 2.5. As both vertical and lateral magnetic coupling is utilized, self-inductance and coupling coefficient (k$\sim$0.9) are high. The lowest metal layer shields the substrate effect from the upper layers. Because of the wide metal traces and small inter-layer distance (ILD), the terminal-to-terminal capacitance is high. There are some variations to alleviate this problem, such as shifting the middle traces to reduce the overlaid area (shown in Figure 2.5(b)) or using alternate metal layers to increase the inter-layer dielectric thickness. To achieve the same inductance, the stacked layout needs a much smaller area than the planar ones. The method to calculate the effective capacitance can be found in [10]. The capacitance is inversely proportional to the square of the number of layers used.

Another concern is that in modern multi-level processes, different metal layers usually have different thicknesses, with the top metal layer usually thicker than the lower layers. The structure in Figure 2.5(a) is not a symmetric design. Figure 2.6 shows a symmetric

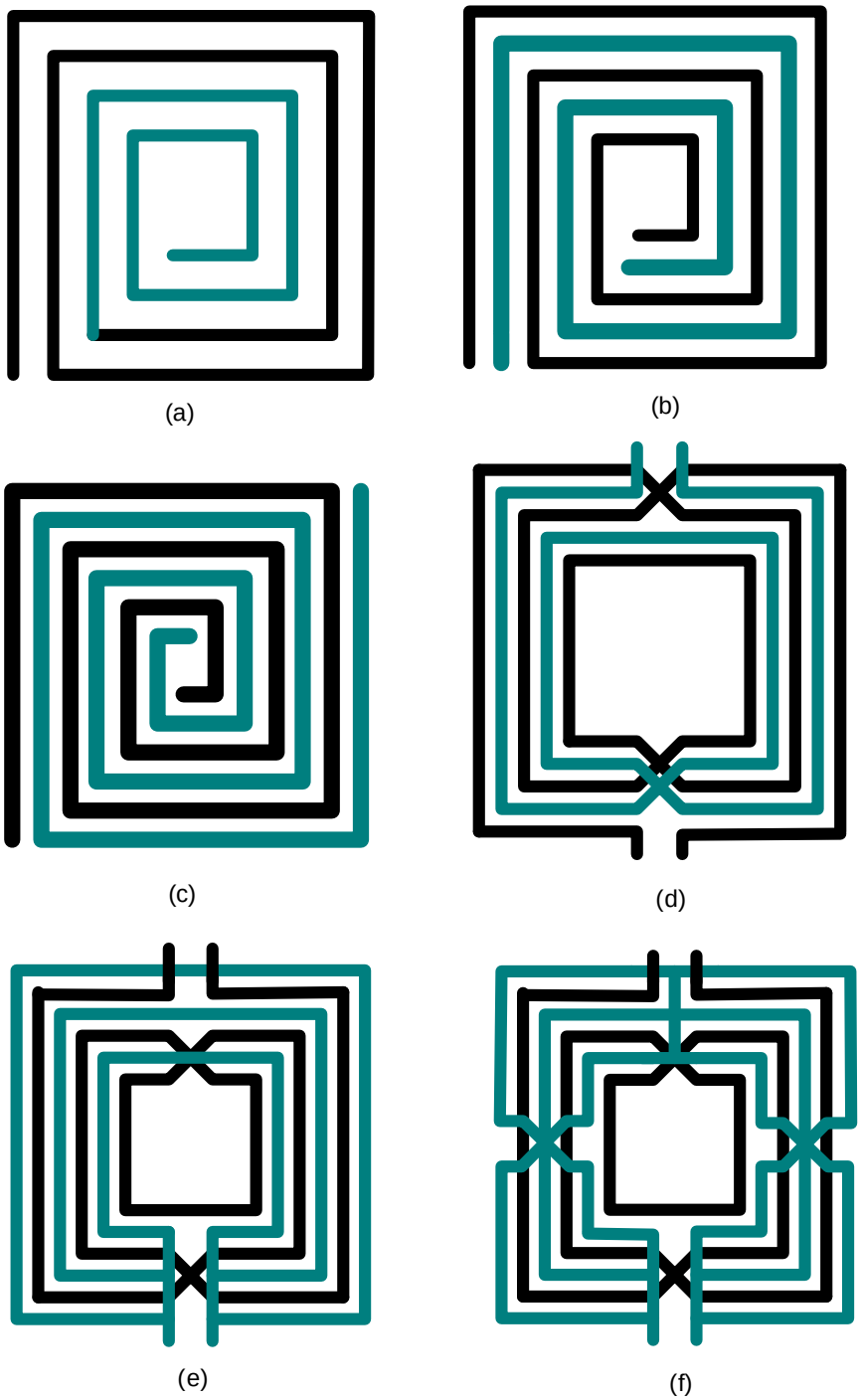


Figure 2.4: Planar transformer structures: (a) Tapped, (b) Parallel (Shibata), (c) Intertwined (Frlan), (d) Symmetric (3:2), (e) Step-up (1:3), and (f) Step-up variation.

layout for multi-layer stacked transformer. It is very similar to a symmetric inductor with a center tap. Other variations may combine interleaved and stacked features to achieve symmetry as in [11].

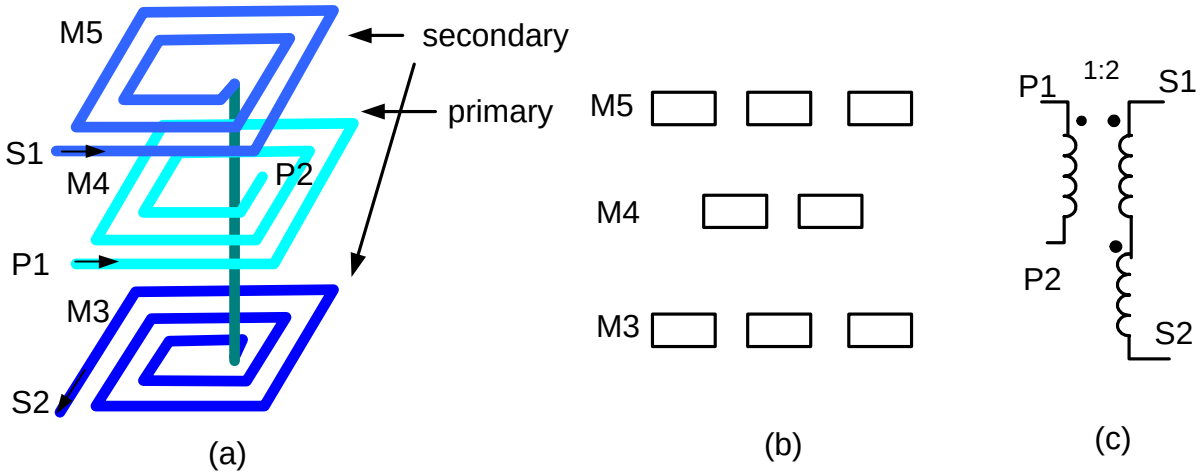


Figure 2.5: Stacked transformer (a) structure, (b) cross section, and (c) circuit model.

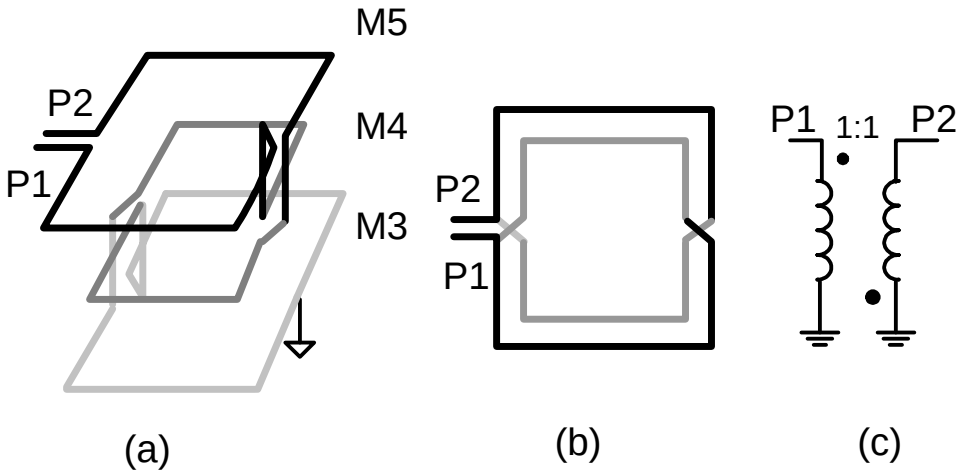


Figure 2.6: Symmetric stacked inverting transformer: (a) structure, (b) top view, and (c) circuit.

2.3.3 Comparison of transformer structures

For different transformer structures, different characteristics such as self-inductance, coupling coefficient k, series resistance, terminal-to-substrate, and terminal-to-terminal capacitance are achieved. Table 2.2 shows a comparison of some performance measures for various transformer structures. In general, a planar structure has a large area, better quality factor of the primary and secondary inductors, medium k, and high self-resonant frequency, while a stacked structure has a small area, high k, and low self-resonant frequency. For different applications, different characteristics, and thus different transformer structures, are desired.

	Tapped	Frlan	Step-up	Stacked
k	small	medium	medium	high
n	arbitrary	1	1∼4	arbitrary
Q	high	medium	medium	small

Table 2.2: Comparison of performance measures for different transformer structures.

2.4 Analytical Transformer Model

An accurate transformer model is desired for circuit design. Transformer analysis tools, usually as an extension of inductor analysis tools, use computationally intensive techniques such as the "Partial Element Equivalent Circuit" (PEEC) [12] or finite element solutions of Maxwell's equations [13]. These methods are time-consuming and have high computing requirements, yet provide limited insight and optimization possibilities. A physics-based compact model is needed for fast and accurate circuit simulation and optimization.

Most transformer compact models are built on the inductor models [11], as transformers suffer non-ideal effects very similar to those of inductors. To accommodate center taps of some transformer configurations and the distributed effect at high frequencies,

the 2-π model (shown in Figure 2.7) is better than the π model. It can be configured to a 2-port or 3-port transformer model by appropriately shorting the terminal and/or center tap to Gnd. The model includes non-idealities (as shown in Figure 2.8) such as terminal-to-substrate capacitance C_p and C_s, pattern ground shield (PGS) parasitic resistance R_b [14], terminal-to-terminal capacitance C_c, and series resistance due to the ohmic, skin and proximity effects. The electrical field induced substrate loss is shielded by PGS with star strapped metal [15]. The magnetic field induced substrate loss is not considered because highly resistive substrates ($\rho_{sub} > 10\Omega$-cm) are typically used for RF CMOS implementations. Processes using epi-substrate need to consider this loss, which is not discussed here.

As this study focuses on transformers with high quality factor and low insertion loss, only the planar interleaved transformer model based on geometric and technology parameters is discussed in detail, although stacked transformers can also be modeled using the circuit in Figure 2.7 with minor changes.

2.4.1 Self and mutual inductance and coupling coefficient k

The self and mutual inductance can be computed from the formulae given by Grover [16] or Greenhouse [17]. Mohan [11] proposed simplified expressions for calculating these inductances from geometric parameters, such as the outer dimension, the metal width, the spacing and the number of turns. He also provided a 2-port transformer model for interleaved and stacked transformers with a very rough series resistance approximation.

For tapped and interleaved transformers, the following relationship holds:

$$M = (L_T - L_p - L_s)/2 \tag{2.7}$$

where L_T is the total inductance of a single spiral with all the segments of both primary and secondary traces, L_p and L_s are the self-inductances of the primary and secondary, and M is the mutual inductance. The coupling coefficient k can be calculated using

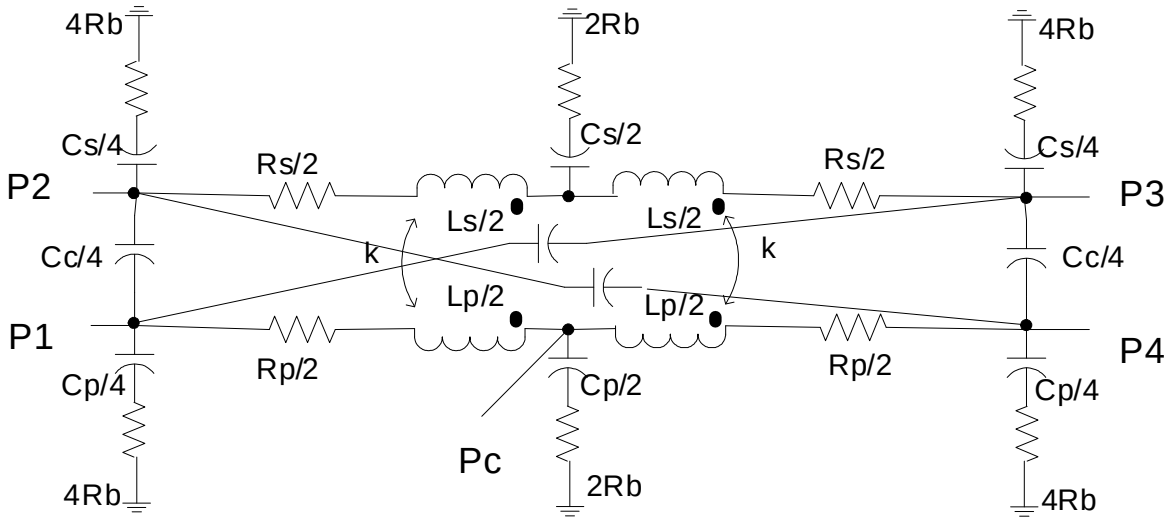


Figure 2.7: Transformer frequency dependent circuit model.

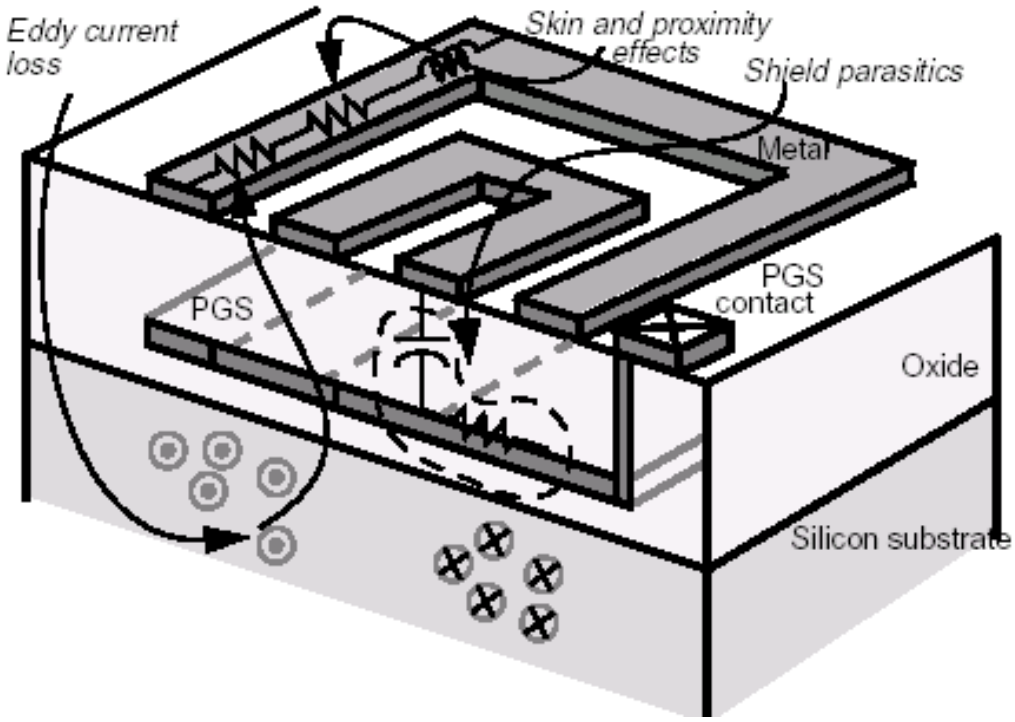


Figure 2.8: Non-idealities and loss mechanisms.

Eqn.(2.2). When the primary and secondary have different trace width W_p and W_s, the weighted average width W_{avg} can be used for L_T calculation,

$$W_{avg} = (W_p \times N_p + W_s \times N_s)/(N_p + N_s)$$

where N_p and N_s are the number of turns for primary and secondary.

2.4.2 Capacitances

The capacitances C_p and C_s to the substrate can be approximated as frequency independent parallel plate capacitances

$$C_i = \frac{\varepsilon_{ox}}{t_{ox}} \cdot l_i \cdot W_i;\ i = p \text{ or } s \tag{2.8}$$

where l_i and W_i are the length and width of the primary or secondary trace, and t_{ox} is the thickness of the oxide from the bottom of the metal layer to the top surface of the PGS.

The cross coupling capacitance C_c is the capacitance between the primary and secondary. It includes the fringing capacitance and the under-pass capacitance.

2.4.3 Shield resistance

In [14], the star-shaped metal 1 strapped PGS is discussed in detail. The shield parasitic resistance is given by

$$R_b = \left(\frac{D_{out}}{2W_{pgs}} + \frac{1}{12}(\frac{D_{out}}{2W_{pgs}})\right) Rsh_{M1} + \frac{1}{4} Rsh_{poly} \tag{2.9}$$

where D_{out} is the outer dimension of the transformer, W_{pgs} is the width of PGS strip. Rsh_{M1} and Rsh_{poly} are the sheet resistances of metal 1 and silicided poly, respectively.

2.4.4 Skin and proximity effects

This section presents a new modeling methodology for the skin and proximity effects, which results in a compact expression to compute the frequency dependent resistance. The skin effect is treated as a result of the "vertical" current redistribution along the metal thickness, while the proximity effect is treated as a result of the "lateral" magnetically induced eddy current losses. The product of the two causes the increased resistance at high frequency.

2.4.4.1 Previous work

Numerous experimental and numerical studies of skin and proximity effects can be found in literature [18, 19]. The resistance increase due to the skin and proximity effects becomes prominent when the operation frequency goes beyond 1 GHz. It is crucial to predict the quality factor of the windings and thus the performance of the transformer. In [14], a useful vertical skin effect model for inductor modeling is given and the proximity effect is solved by a 6-segment PEEC approach. It is not easy to adapt this model to a transformer model though. Sieiro [20] proposed a physics-based inductor model, which provides some insight for modeling proximity effect for transformers. However, the model predicts that the resistance saturates at high frequency, which does not agree with the simulation result, according to which the resistance is approximately proportional to the square root of the frequency.

2.4.4.2 Skin effect

Talwalkar [14] established that as the width-to-thickness ratio of the conductors of an inductor (and hence a transformer) is typically large, it is possible to solve the Maxwell equation

$$\nabla \times H = J \quad J_z \approx -\frac{\partial H_x}{\partial y} \tag{2.10}$$

with a function as the product of two functions in orthogonal coordinates

$$H_x = F(x)G(y). \tag{2.11}$$

Thus we can laterally divide the wide conductor into segments. Within each segment, H_x is just a function of y. The solution gives the normalized resistance:

$$R_{rfv}/R_{dc} = \max(real(\xi \cdot \coth(\xi)),\ \frac{t}{2\delta}) \quad \xi = (1+i)\frac{t}{2\delta} \tag{2.12}$$

where t is the thickness of the metal; R_{rfv} and R_{dc} are the rf (due to the vertical skin effect) and the dc resistance; δ is the skin depth given by

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{2.13}$$

where σ is the conductivity of the metal, μ is the permeability and ω is the frequency.

As shown in Figure 2.9, the skin effect is not significant at low GHz when the metal thickness is less than 2μm. At high frequency, the current is crowded to the edge of the metal. The center has little current density. The effective thickness of the metal is about twice the skin depth.

2.4.4.3 Proximity effect

The presence of changing magnetic fields induces eddy current in a conductor, thus changing its current density distribution. The current is usually crowded to the edges. The current density distribution $\mathbf{J}$ can be written as

$$\mathbf{J} = \sigma\mathbf{E} + \mathbf{J}_{src} \tag{2.14}$$

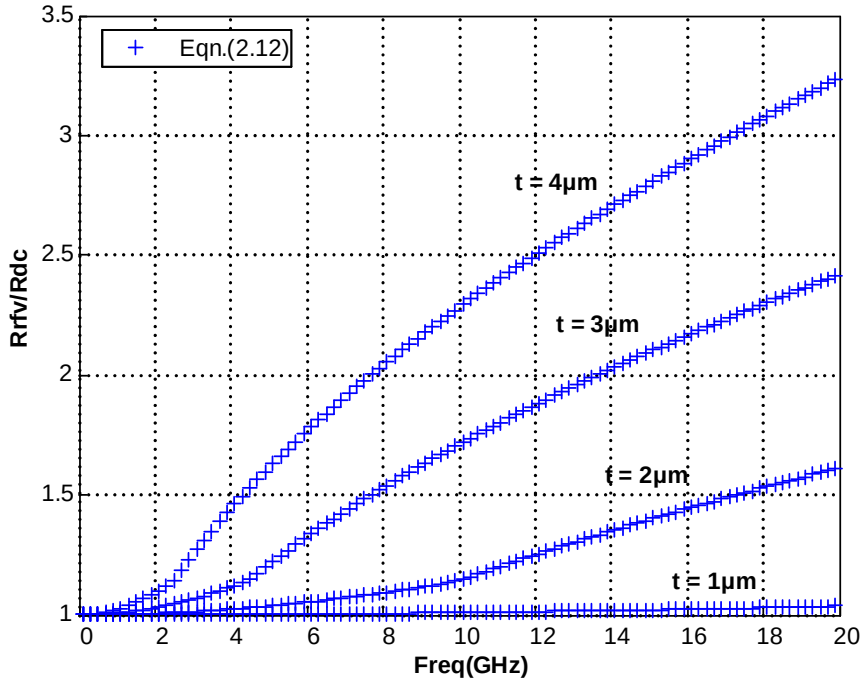


Figure 2.9: The normalized resistance model from Eqn. (2.12).

where $\mathbf{E}$ is the induced electric field inside the metal. $\mathbf{J}_{src}$ is the impressed current. Then the eddy current distribution is given by

$$\mathbf{J}_{eddy}(\mathbf{r}) = -j\omega\sigma[\mathbf{A}_{ext}(\mathbf{r}) + \int_V G^K(\mathbf{r},\mathbf{r}')(\mathbf{J}_{eddy}(\mathbf{r}') + \mathbf{J}_{src}(\mathbf{r}'))dv'] \tag{2.15}$$

where $G^K(\mathbf{r},\mathbf{r}')$ is the Green function of the vector potential and $\mathbf{A}_{ext}$ is an external vector potential. As the equation shows, there are two eddy current sources; one is from the impressed current $\mathbf{J}_{src}$, and the other is the external potential $\mathbf{A}_{ext}$, which is due to the magnetic coupling of all the remaining metal traces. To simplify the problem, we assume that $\mathbf{A}_{ext}$ is not affected by the current redistribution. We can then find the relationship between $\mathbf{A}_{ext}$ and the impressed current.

For transformer structures, when the primary is measured with the secondary open, i.e., the secondary terminals have no current, the external magnetic field produced by the primary still induces eddy current in the secondary winding. This eddy current also adds loss which needs to be included in the calculation. This is confirmed by a Fasthenry [21]

simulation (shown in Figure 2.10), comparing the normalized resistance of the primary of a transformer structure with the secondary open to that of the primary inductor itself.

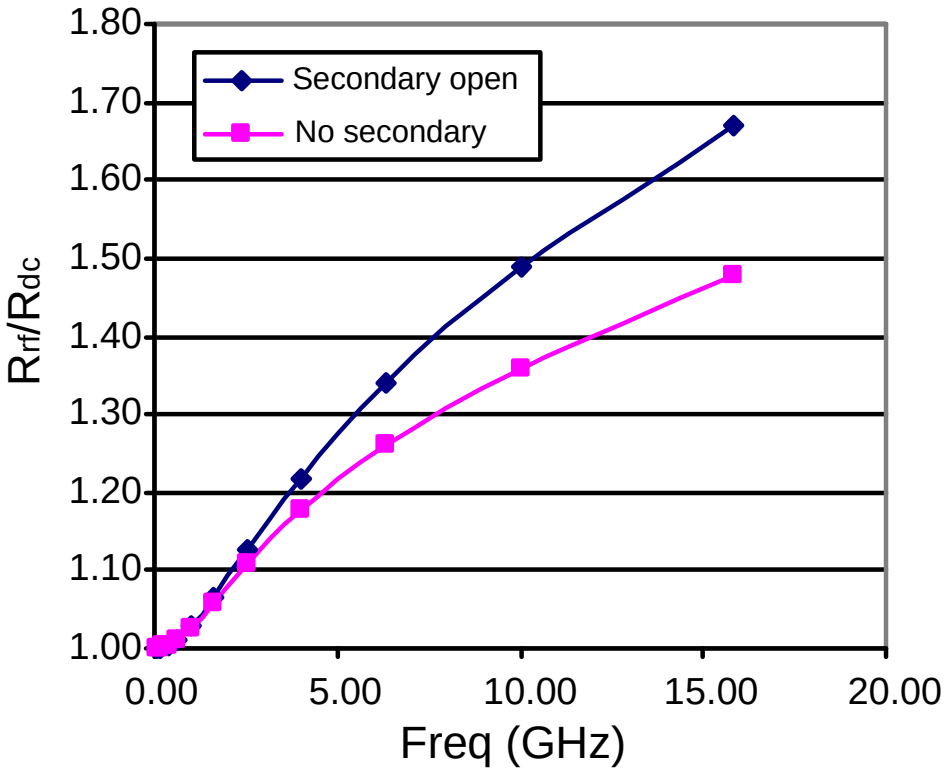


Figure 2.10: Fasthenry simulation of the normalized primary resistance with no secondary (red square) and secondary open (blue diamond) in 1:1 transformer, $D_{out} = 180\mu$m, $W_p = 30\mu$m, $W_s = 7\mu$m, $s = 2.5\mu$m.

We can further simplify the problem using just three segments of the wide metal trace as shown in Figure 2.11, where no end effect is considered. The total proximity effect needs to be considered from three perspectives as shown in Figure 2.12:

1. Eddy current loss due to external magnetic field from the remaining metal traces of the same inductor.

2. Eddy current loss due to impressed current in the metal trace.

3. Eddy current loss due to external magnetic field from the other inductor of the transformer.

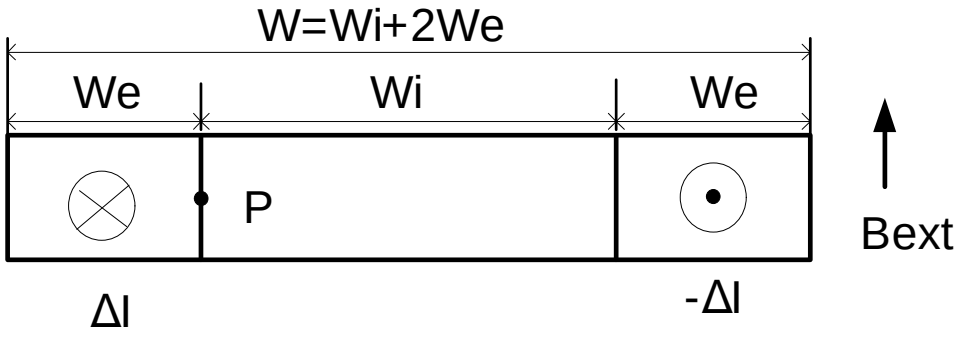


Figure 2.11: Segment geometry for the computation of the eddy current loss.

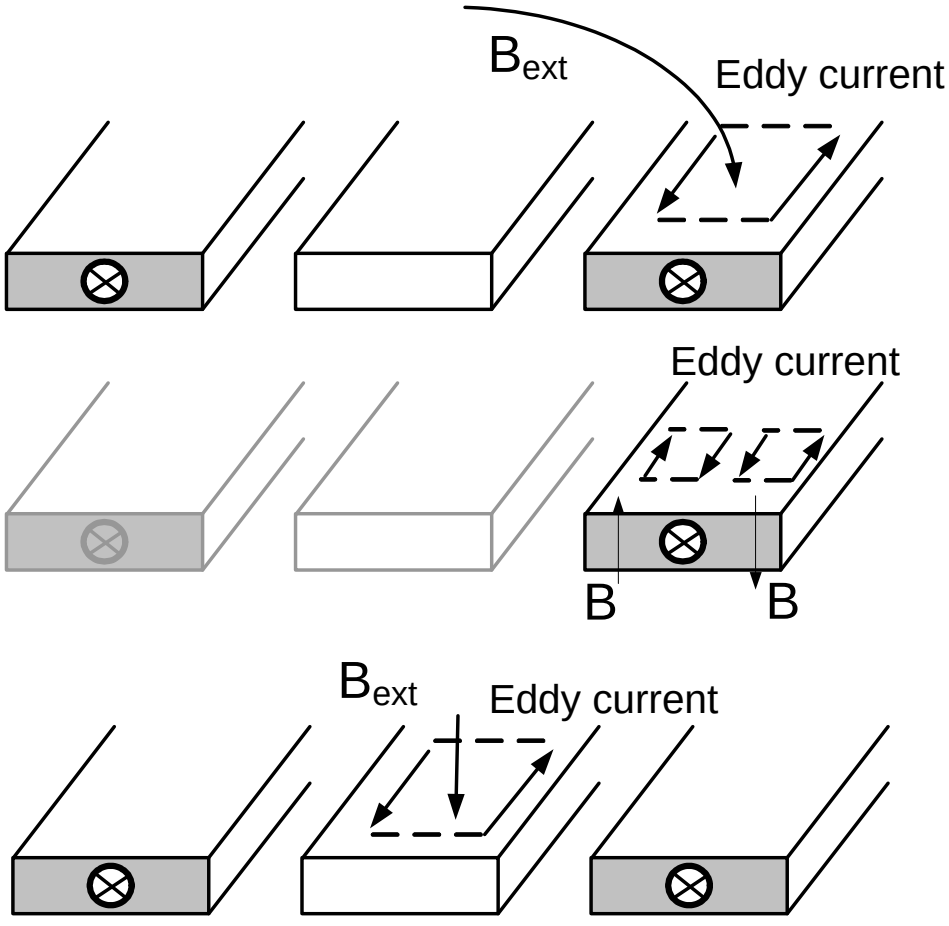


Figure 2.12: Eddy current losses due to (a) external magnetic field B_{ext}, (b) impressed current, and (c) external magnetic field B_{ext} from the other inductor.

Detailed analysis illustrated in Appendix A shows that the total resistance including all the losses can be expressed in the following form:

$$R_{total\_p} = R_{dc} + R_{rfp} = R_{dc}\left(1 + r_{rf}\frac{(f/f_0)^2}{1+(f/f_0)^2}\right) \tag{2.16}$$

where R_{rfp} is the increased resistance due to the proximity effect, r_{rf} is a transformer geometry and technology related coefficient, and f_0 is a frequency factor given by

$$f_0 = \frac{2R_{sh}(1+3q)}{\mu_0 W(1-q^2)} \tag{2.17}$$

where μ_0 is the permeability of free space, R_{sh} is the sheet resistance of the metal, W is the width of the metal trace, and q is the ratio of W_i/W. The frequency factor f_0 controls the transition from low frequency to high frequency behavior. We can see that at low frequency, $f/f_0 \ll 1$ and the increased resistance shows an f^2 dependency. At high frequency, f/f_0 levels off. We can increase f_0 by increasing R_{sh} or reducing W. The ratio r_{rf} is also geometry dependant. When R_{sh} is about 20m$\Omega/\square$ (metal thickness about 2μm) and W is about 10μm, f_0 is around 3GHz and r_{rf} is around 0.1$\sim$0.2.

2.4.4.4 Total series resistance

Now that we have analyzed both vertical and lateral current redistribution, we can combine them. The total series resistance becomes:

$$R_{total} = R_{dc} + R_{rf} \approx R_{dc} real(\xi \coth(\xi)) \cdot [1 + r_{rf}\frac{(f/f_0)^2}{1+(f/f_0)^2}]. \tag{2.18}$$

At low frequency, the added resistance R_{rf} increases with f^2, while at high frequency R_{total} mostly follows the $\sqrt{f}$ trend. This behavior is observed in both simulation and measurement data, which will be shown in detail in the next chapter. Although a small number of segments is used, Eqn. (2.16) gives us insight into how the series resistance changes with frequency and other geometry and process parameters.

2.4.4.5 Broadband resistance model

The frequency dependent series resistance model given in section 2.4.4.4 cannot be used directly in circuit simulators such as Cadence or Hspice. There are two ways to get around this problem. If narrow-band applications, such as WLAN, are of interest, Eqn. (2.18) can be used to calculate the resistance at the target frequency. This resistance can be treated as a constant in circuit simulations. However, to make the model useful for broadband applications, such as UWB, a ladder circuit can be used to model the frequency dependent series resistance as shown in Figure 2.13.

The overall impedance of the ladder circuit shown in Figure 2.13(a) is given by

$$Z(jf) = R(f) + jX(f) \tag{2.19}$$

where

$$R(f) = R_{dc} + R_f \frac{(f/f_0)^2}{1 + (f/f_0)^2}, \tag{2.20}$$

$$X(f) = R_f \frac{(f/f_0)^2}{1 + (f/f_0)^2}, \tag{2.21}$$

$$f_0 = R_f/(2\pi\, L_f). \tag{2.22}$$

At low frequency, the series resistance is just R_{dc}, while at high frequency, it approaches $(R_{dc} + R_f)$. Eqn. (2.20) is very similar to Eqn. (2.16). Hence this ladder circuit can capture the proximity effect quite well. For metal thickness $t < 2\mu$m, we can see in Figure 2.9 that the skin effect is not significant at low GHz. So the ladder circuit is sufficient. However, for thicker metal and/or higher frequency range, the ladder circuit has limitations. A more complicated T-model proposed by Horng [22] and proclaimed to be super-broadband, is not very intuitive and is hard to derive from the geometry and technology parameters.

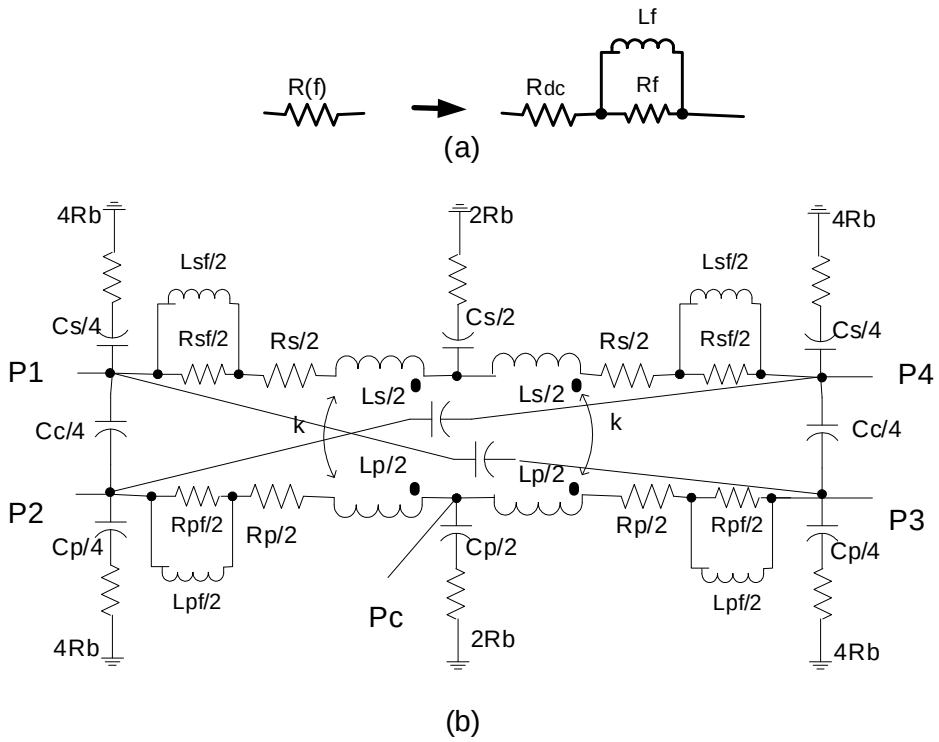


Figure 2.13: (a) Ladder circuit and (b) Broadband transformer model with ladder circuit to replace the frequency-dependent resistance.

2.5 Performance Measures of Transformer

Depending on the circuit application and frequency of operation, transformer design requirements can be quite different. For some LNA and VCO designs (as shown in Figure 2.14(a) [23], (b) [24] and (c) [25]), the transformer is optimized for voltage transfer and magnetic coupling. For a balun circuit (as shown in Figure 2.14(d)), single-ended to differential transformation and impedance transformation are emphasized.

Before we can optimize any transformer structure, we need to determine what performance measures are desired for the particular transformers.

2.5.1 Coupling coefficient k and turn ratio n

For voltage or current coupling, such as the transformer inter-stage coupling and feedback circuit, high coupling coefficient k, specific or high turn ration n, or both, are desired [23,

25] (see Figure 2.14(a), (c)). The step-up transformer works well for these narrowband applications. To increase k, the spacing between the primary and secondary should be as small as possible, constrained by the coupling capacitance and self-resonant frequency.

2.5.2 Quality factor Q

A simplified transformer model is shown in Figure 2.15. This simplified circuit model ignores all the capacitances, and only the loss of the inductors is included. The quality factor Q_p and Q_s of the primary and secondary windings are defined as

$$Q_p = \frac{\omega L_p}{R_p};\ Q_s = \frac{\omega L_s}{R_s} \tag{2.23}$$

where R_p and R_s are the series resistances of the primary and secondary.

As in the VCO application shown in Figure 2.14(b), the transformer is used to boost the effective Q seen from the primary port, which is given by [24]

$$Q = (1 + k)Q_0$$

where a 1:1 transformer is used in the analysis, with $Q_p = Q_s = Q_0$. The High-Q resonator reduces the phase noise of the VCO. High Q and k are desired in this application.

2.5.3 Insertion loss (IL)

For power transfer and impedance transformation applications, such as baluns, the insertion loss is used as a metric to measure the performance of a transformer. Based on the simplified transformer model shown in Figure 2.15, the port voltages and currents have a relationship similar to Eqn. (2.1), given as follows:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_p + j\omega L_p & j\omega M \\ j\omega M & R_s + j\omega L_s \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2.24}$$

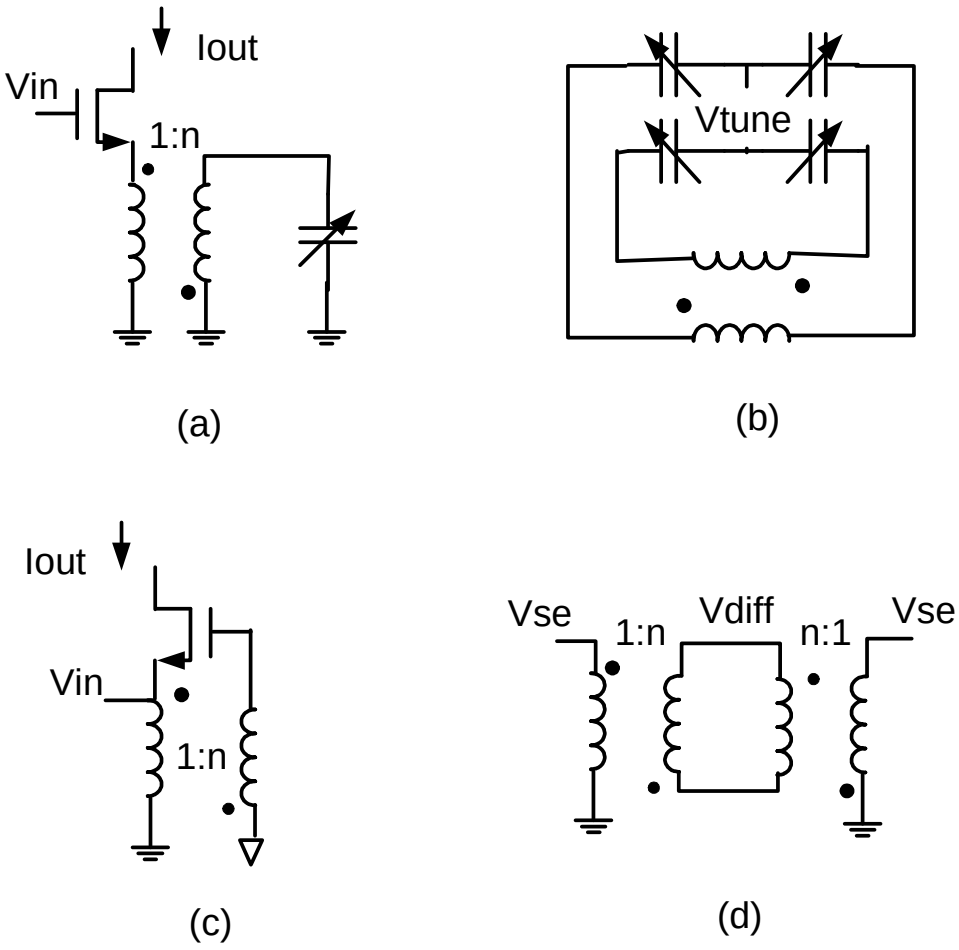


Figure 2.14: Transformer applications: (a) image-reflected filter in LNA, (b) high-Q resonator in VCO, (c) transformer feedback common gate LNA, (d) single-ended to differential transformation (balun).

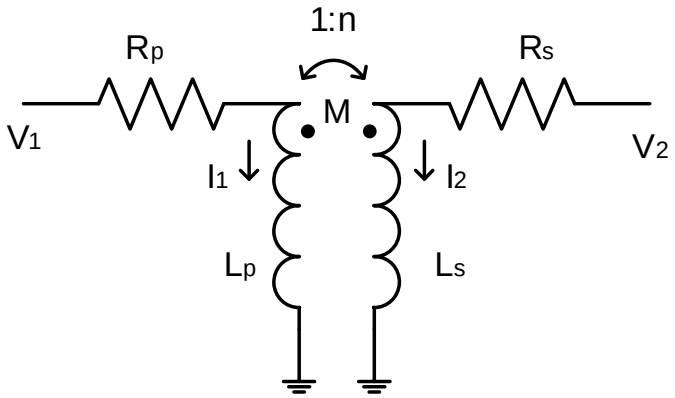


Figure 2.15: Simplified transformer model.

Its equivalent T-model is shown in Figure 2.16. The ratio of the power delivered to the load P_{load} to the total power delivered into port 1 P_{total} is given by [26]

$$\eta \equiv \frac{P_{load}}{P_{total}} = \frac{R_l/n^2}{(\frac{\omega L_P/Q_s+R_l/n^2}{\omega k L_p})^2 \cdot \frac{\omega L_p}{Q_p} + \frac{\omega L_p}{Q_s} + R_l/n^2}. \tag{2.25}$$

It has a maximum given as

$$\eta_{\max} = 1 + 2(x - \sqrt{x^2 + x}) \tag{2.26}$$

where $x = 1/(k^2 Q_p Q_s)$. It is a monotonically decreasing function of x.

The minimum insertion loss (ILm) is given by

$$ILm(dB) = -10 \log_{10}[1 + 2(x - \sqrt{x^2 + x})] \tag{2.27}$$

To get ILm, the product of $k^2 Q_p Q_s$ needs to be maximized. The ILm as a function of k and $Q = Q_p = Q_s$ is shown in Figure 2.17. It is not a function of the load. The insertion loss will increase several tenths of dB if the parameters are not optimum. But this increase is relatively small as shown in Figure 2.18.

Vendelin [27] discussed the maximum available gain $G_{\max}$ of a 2-port system, which

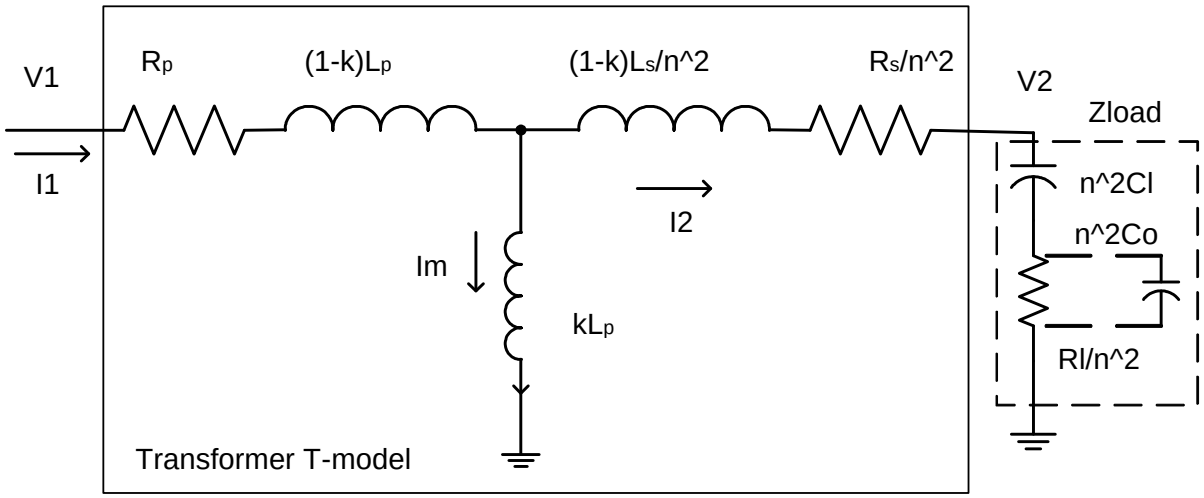


Figure 2.16: Transformer equivalent T-model with load impedance.

can be used for a more generalized transformer model. $G_{\max}$ can be expressed in S-parameters as follows:

$$G_{\max} = \left|\frac{S_{21}}{S_{12}}\right| (\xi - \sqrt{\xi^2 - 1}), \tag{2.28}$$

where

$$\xi = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|},\ \Delta = S_{11}S_{22} - S21S_{12}.$$

The expression is not very intuitive but it is very useful for transformer characterization. It can also be expressed in Z-parameters as shown in Eqn. (2.29) [28]. $G_{\max}$ is defined the same as $\eta_{\max}$ and has a very similar expression to Eqn. (2.26). In Eqn. (2.29), k_r is introduced to account for the real part of Z_{12} and Z_{21} caused by the capacitive coupling. The capacitive path to PGS also adds loss.

$$\begin{aligned} ILm &= -10\log_{10}(G_{\max}); \\ G_{\max} &= 1 + 2(x - \sqrt{x^2 + x}); \\ x &= \frac{\mathrm{Re}(Z_{11})\mathrm{Re}(Z_{22}) - [\mathrm{Re}(Z_{11})]^2}{[\mathrm{Im}(Z_{12})]^2 + [\mathrm{Re}(Z_{12})]^2} \ \rightarrow\ x = \frac{1 - k_r^2}{k_i^2 Q_p Q_s + k_r^2} \end{aligned} \tag{2.29}$$

where

$$Z_{11} = R_p + j\omega L_p;\ Z_{22} = R_s + j\omega L_s;\ Z_{12} = Z_{21} = R_m + j\omega L_m;$$

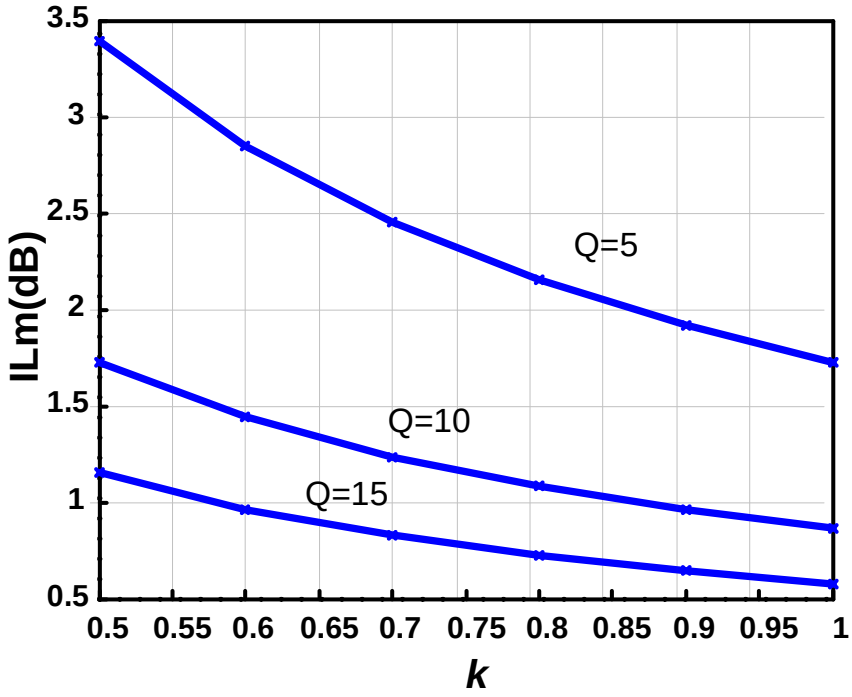


Figure 2.17: Coupling coefficient k versus minimum insertion loss ILm for different $Q = Q_p = Q_s$.

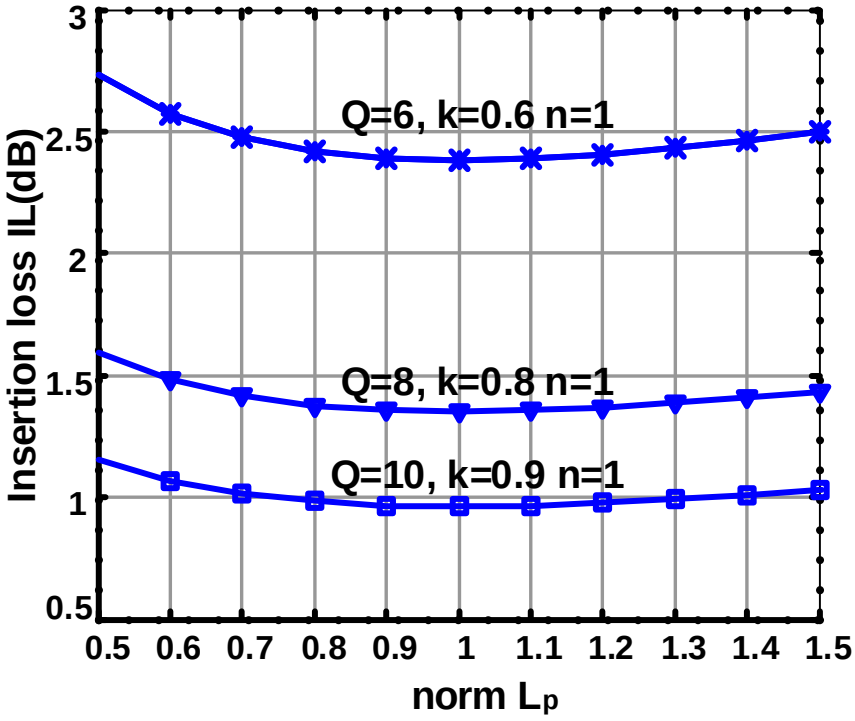


Figure 2.18: Insertion loss as function of normalized L_p with different Q, k and n.

$$Q_p = \omega L_p / R_p;\ Q_s = \omega L_s / R_s;$$

$$k_i = \sqrt{\frac{[\mathrm{Im}(Z_{12})]^2}{[\mathrm{Im}(Z_{11})][\mathrm{Im}(Z_{22})]}};\ k_r = \sqrt{\frac{[\mathrm{Re}(Z_{12})]^2}{[\mathrm{Re}(Z_{11})][\mathrm{Re}(Z_{22})]}}.$$

2.6 Summary

This chapter briefly reviewed the basics of transformers, summarized different physical layouts, and explored the compact circuit model for the on-chip interleaved transformer. The comparison of EM simulation, measurement, and model results will be presented in the next chapter.

Chapter 3

Methods to Improve Transformer Performance

This chapter further discusses the relationship between the performance measures and geometries of various on-chip transformer structures. Section 3.1 introduces the effects of the transformer geometry on k and Q. Section 3.2 discusses a novel way to improve k and, thus, the ILm. EM solver HFSS from Ansoft company [29] was used to simulate some structures. The key setup procedure is summarized in Section 3.3. Various transformer structures were fabricated in the Stanford Nanofabrication Facility (SNF). The measurement results are compared to HFSS simulation and model results in Section 3.4. Section 3.5 gives a short summery.

3.1 Introduction

Although on-chip transformers are more complicated than inductors, many of the techniques that have been applied to the optimization of inductors are also applicable to transformers, especially those methods used to improve the quality factor Q of the metal windings. There are several ways to improve Q. Some improvements can be made through the fabrication process, such as using thick copper top layers or strapping multiple levels

of metal layers to reduce the ohmic losses; or using a thick oxide layer and/or very high resistivity substrate (HRS) to reduce substrate loss; or even employing micromachining techniques [30]. Other improvements can be made through careful layout, such as using pattern ground shield (PGS) to reduce the substrate loss induced by electrical fields.

Transformers make use of the magnetic coupling between the primary and secondary windings. Figure 3.1 shows the coupling coefficient k versus the number of turns and width of the primary or secondary windings for a 1:1 Frlan transformer.

For the same width and spacing, there is a large improvement in k as N increases from 1 to 2, because of the coupling between adjacent lines. However, further increase of N does not improve k considerably. For the same N, k decreases when W and s increase. However, wider metal traces usually have a better Q. For some applications such as the output baluns for power amplifiers, the large DC current requires wide traces for reliability. As shown in the last chapter, to get ILm, the product of $k^2Q_pQ_s$ needs to be maximized. Hence, there must be an optimum metal width W_{opt} to balance k and Q for the maximum $k^2Q_pQ_s$.

3.2 Segment and Interleave

Without altering the fabrication process, the wide traces can be split into multiple parallel segments and interleaved, as shown in Figure 3.2(b) to improve k. Another advantage is that the proximity effect is also mediated. Because the effective width of the primary or secondary winding is enlarged, the self-inductances L_p and L_s are reduced while the resistance remains about the same. So the Q_p and Q_s will be reduced at low frequencies. The coupling capacitance between the primary and secondary windings increases. These contradictory effects need to be balanced in order to achieve an optimum ILm.

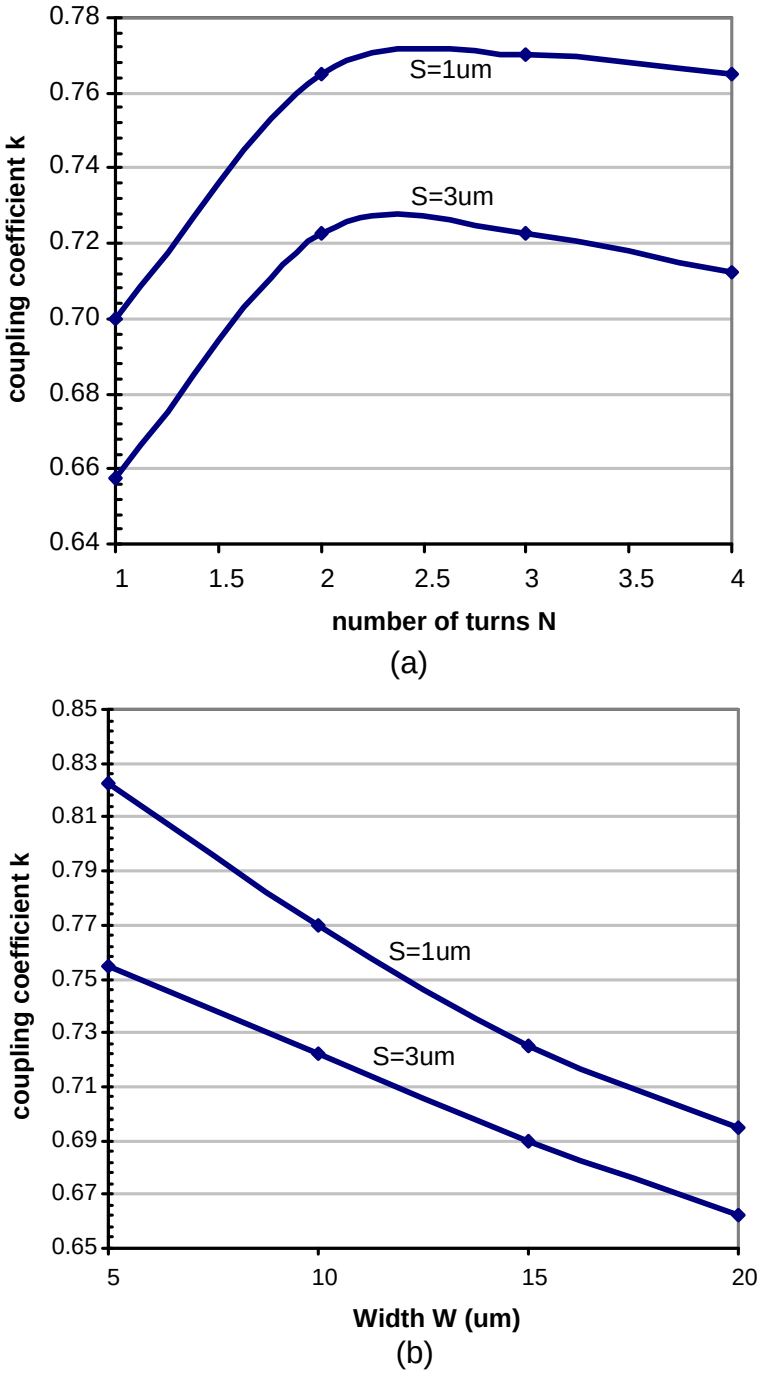


Figure 3.1: Coupling coefficient k versus (a) number of turns $N = N_p = N_s$ with W=10μm and (b) trace width $W = W_p = W_s$ with N=3 for a 1:1 Frlan transformer with $L_p = L_s = 2$ nH.

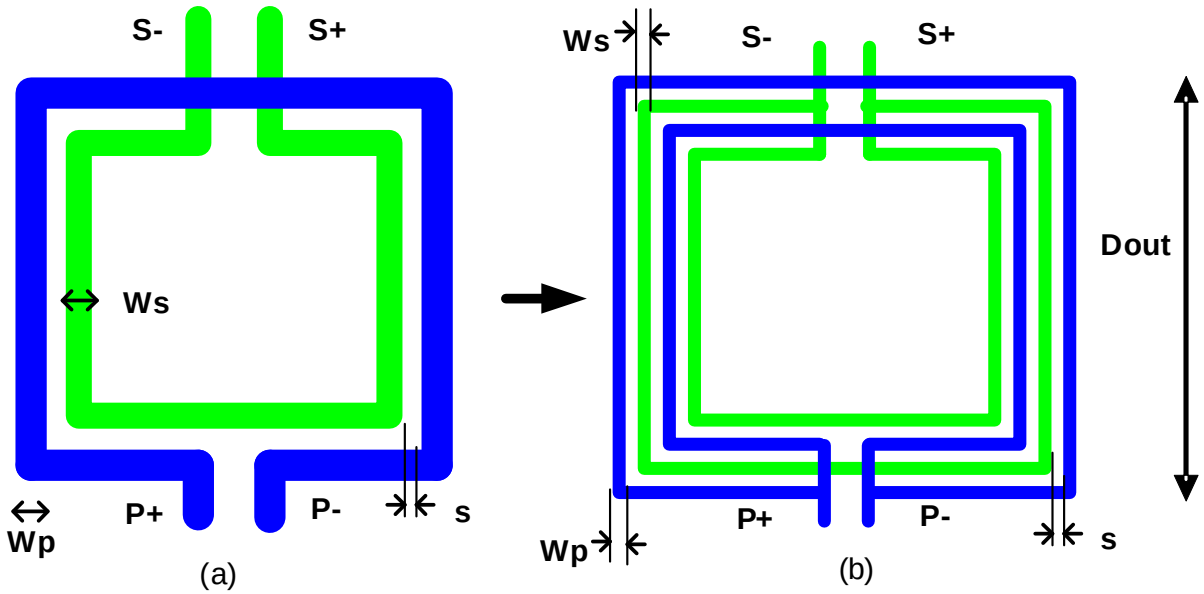


Figure 3.2: (a) A typical single-turn transformer and (b) a transformer with interleaving coils.

3.3 HFSS Simulation

HFSS is a 3-D EM solver from Ansoft [29]. HFSS usually takes a long time and a great deal of memory to simulate even simple structures. However, it can give relatively accurate results in a frequency range, as long as the simulation parameters are chosen correctly. So it is useful as a validation tool when the geometry of the desired transformer is fixed. Figure 3.3 shows an example of an HFSS setup for a 2:1 step-up transformer. To get correct results in a timely fashion, the following points are very important:

- Simplify the test structure (DUT) by combining the metal width, merging connected metals, merging vias and other details.
- GDS files from a layout tool can be imported to the HFSS simulation environment along with the correct technology files.
- The outer diameter of the airbox needs to be twice as large as the structure. If the airbox is large enough, the radiation boundary should produce the same result as a perfect E boundary.

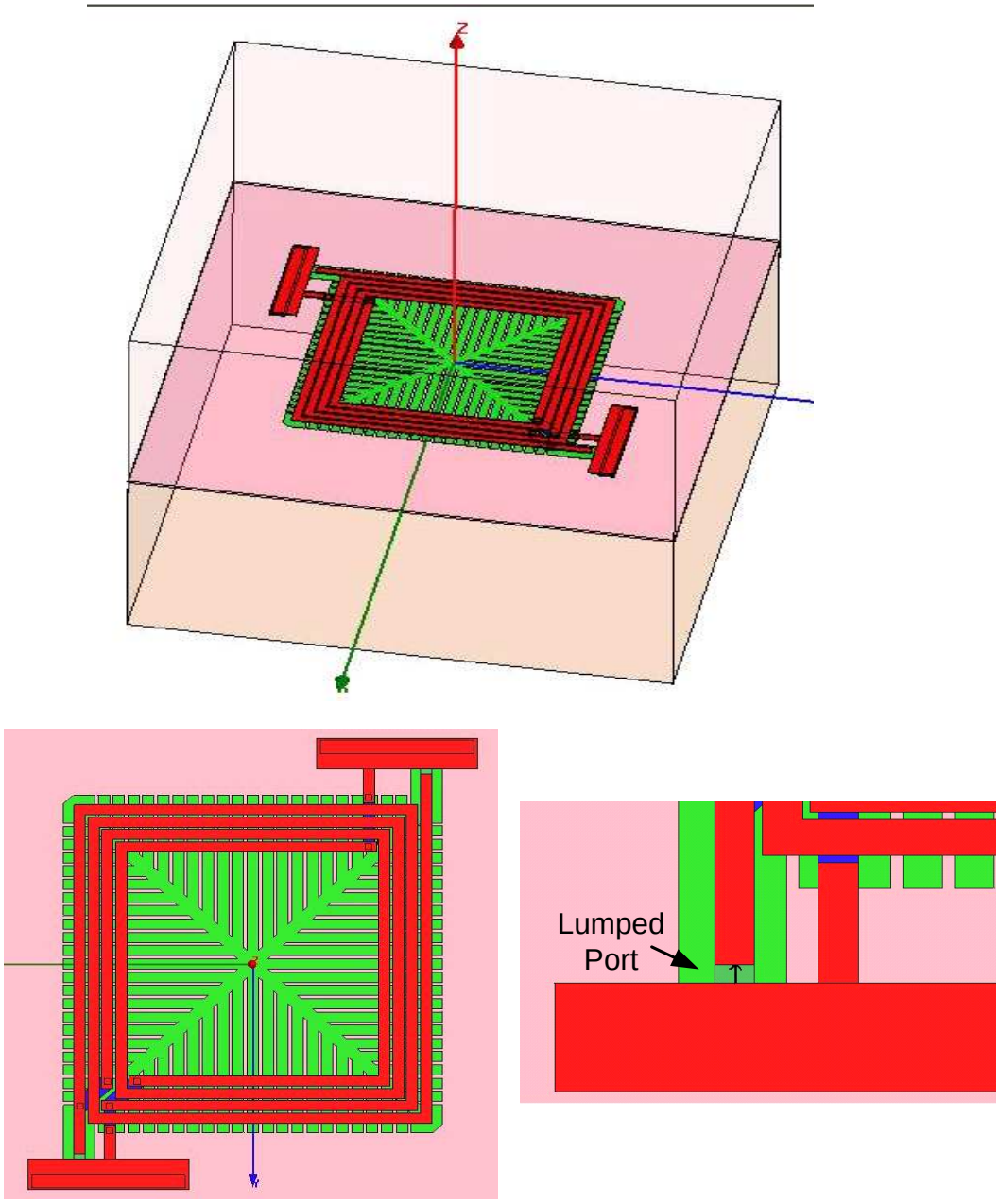


Figure 3.3: Example of HFSS setup for 2:1 step-up transformer.

- To emulate the GSG probe usually used in measurements, choose "driven terminal" as the solution type.
- Solve the inside conductors of interest.
- Seed mesh conductors with a length-based scheme. To save simulation time, the maximum number of elements can be restricted to 5000.
- Set ground ring or metal to be a perfect conductor.
- Define a lumped port on a rectangular between Ground and the structure end. Usually the resistance is 50Ω. The load line points from Ground to DUT.
- To get good results, in the Analysis setup, the maximum delta S needs to be less than 0.01. To reduce iterations and speed up the simulation, a lambda refinement of 0.05 is recommended. An interpolate sweep is usually used.

Given the high computation cost in HFSS simulation, it is not a good tool for optimization in the design process.

3.4 Experiment Results

3.4.1 Test structure fabrication

Experimental verification of the transformer model and the segmentation idea was carried out on transformers fabricated with different geometries in the Stanford Nanofabrication Facility (SNF).

A five mask process using deposited silicon-dioxide ($\varepsilon_r = 4$) as insulator and sputtered Aluminum ($\rho = 2.9 \times 10^7$S/m) as metal, was fabricated at the SNF. Figure 3.4 shows the cross-section of the various layers. The metal thickness and inter-layer distance (ILD) were chosen to emulate a typical five metal digital process. The PGS is made in M1 to ensure minimum loss in the shield and the substrate. A doped substrate with a resistivity

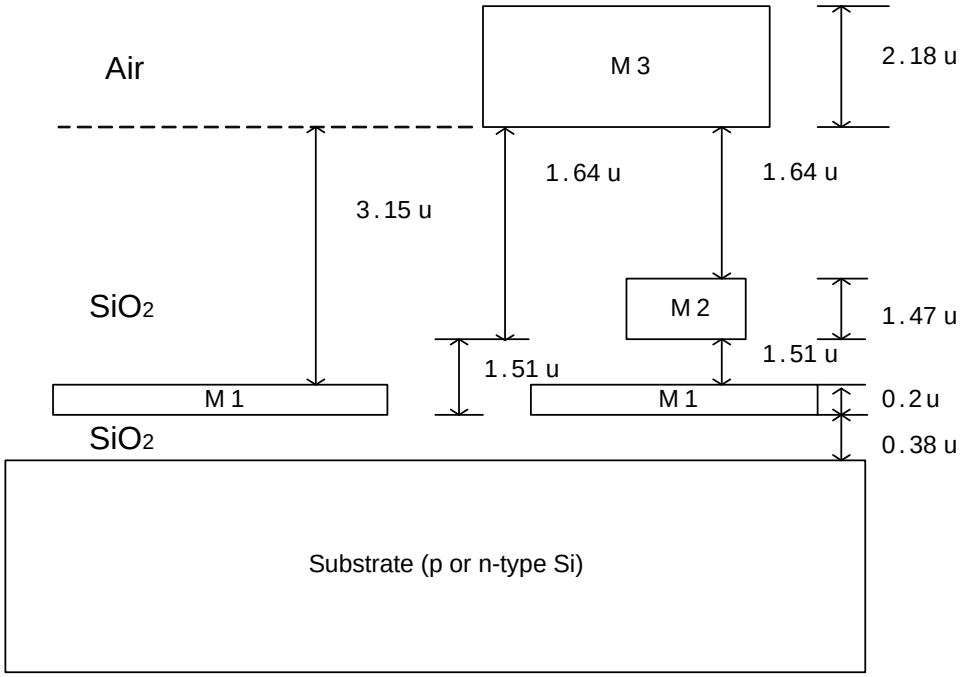


Figure 3.4: Transformer cross-section showing the various layers.

ρ_{sub} of around 10Ω-cm was chosen. This assured that the substrate loss due to magnetic fields is small and can be ignored. A set of geometries (Table 3.1) with different outer dimentions (D_{out}), widths (W), number of turns (N) and number of segmented traces (N_{seg}) were fabricated. All test structures are accompanied by de-embedding structures to subtract the effects of the pad capacitance and contact resistance. All transformers fabricated are in a 2-port configuration.

	$D_{out}(\mu\text{m})$	$W(\mu\text{m})$	N	N_{seg}	$s(\mu\text{m})$
Frlan	200-400	10-30	1-3	1	2 or 5
Step-up	300	10	1-4	1	2
Segmented	400-796	30-50	1-2	1-5	2 or 5

Table 3.1: Test structure geometries.

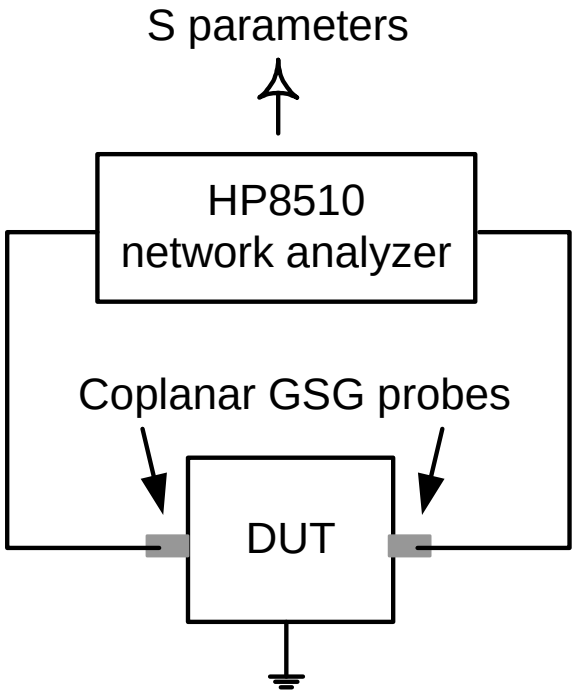


Figure 3.5: Experimental setup for measuring transformer.

3.4.2 Measurement results

Two-port S-parameter measurements of the device under test (DUT) were carried out using the HP8510 network analyzer, as shown in Figure 3.5 The standard de-embedding technique of Short-Open-Load calibration was used to ensure accurate measurements [31]. The de-embedding procedure is as follows:

1. DUT: S-to-Y (Y_{DUT})
2. Open calibration: S-to-Y (Y_O)
3. $Y_{cor} = Y_{DUT} - Y_O$, Y-to-Z (Z_{cor})
4. Short calibration: S-to-Y (Y_S)
5. $Y_{scor} = Y_S - Y_O$, Y-to-Z (Z_{scor})
6. $Z_{meas} = Z_{cor} - Z_{scor}$
7. Z_{meas} to S_{meas}

The impedance matrix Z_{meas} can be used to extract k, L's and Q's. We can also compare S_{meas} to S_{sim}, the latter generated from the model shown in the previous chapter.

In Mohan's thesis [11], only the open structure was used to de-embed the pad parasitics. Table 3.2 shows that for a variety of Frlan structures, the open-only de-embedding procedure generally overestimates the inductance of the windings and underestimates the coupling coefficient k. The absolute error of k is usually larger than 10%. On the other hand, the open-short de-embedding procedure results in a much better match between the simulated data and the measured data, especially for those structures with small inductances.

D_{out}	W	N	L_p(nH)					k				
(μm)	(μm)		simu	open	% **err**	open-short	% **err**	simu	open	% **err**	open-short	% **err**
300	20	3	2.12	2.30	**8.5**	2.10	**0.9**	0.68	0.63	**7.9**	0.69	**0.9**
300	20	2	1.64	1.78	**8.5**	1.60	**2.7**	0.67	0.58	**12.8**	0.65	**2.3**
300	20	1	0.76	0.92	**21.1**	0.72	**4.7**	0.55	0.40	**27.7**	0.51	**7.8**
300	15	2	1.96	2.12	**8.2**	1.92	**2.0**	0.71	0.63	**12.5**	0.69	**3.4**
300	10	2	2.38	2.56	**7.6**	2.35	**1.3**	0.77	0.68	**11.1**	0.73	**4.6**
300	10	1	0.92	1.12	**21.7**	0.93	**0.5**	0.63	0.46	**27.0**	0.56	**10.8**
250	20	2	1.18	1.34	**13.6**	1.14	**3.1**	0.61	0.53	**14.5**	0.62	**1.0**
250	15	2	1.45	1.62	**11.7**	1.42	**2.1**	0.68	0.58	**14.2**	0.66	**2.4**
250	10	2	1.81	1.96	**8.3**	1.77	**2.2**	0.74	0.64	**12.9**	0.71	**3.4**
200	10	2	1.26	1.45	**15.1**	1.26	**0.0**	0.71	0.58	**18.3**	0.67	**5.6**

Table 3.2: Comparison of the measured data from the open and open-short de-embedding procedure and the simulated results for various Frlan transformers.

3.4.2.1 Frlan structure

Figure 3.6 shows the comparison of measured, HFSS, and model data for a Frlan style transformer with $D_{out} = 200\mu$m, $W = 10\mu$m, $s = 2\mu$m, $N = 2$. They all match quite well.

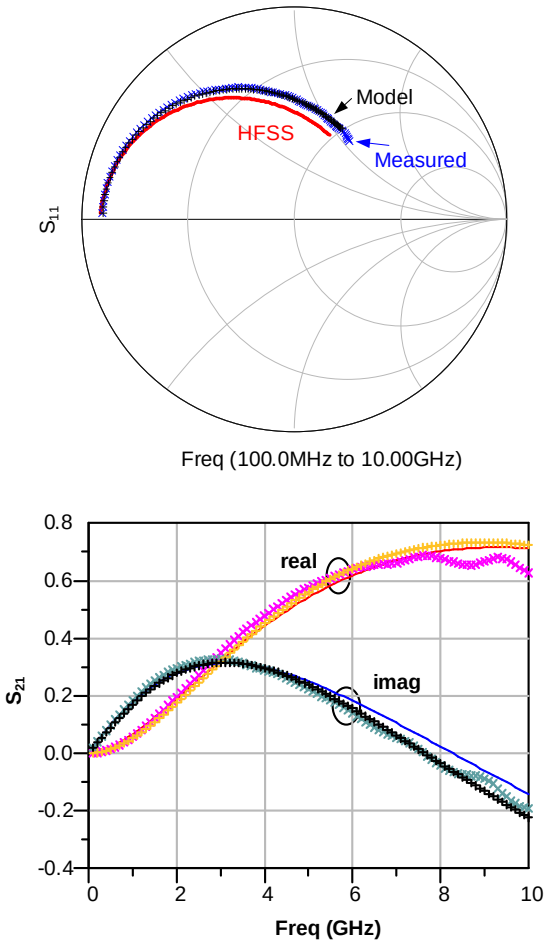


Figure 3.6: Comparison of measured, HFSS, and model data for a Frlan style transformer with $D_{out} = 200\mu$m, $W = 10\mu$m, $s = 2\mu$m, $N = 2$. Label x: measured; +: Model; line: HFSS.

3.4.2.2 Step-up structure

Figure 3.7 shows the comparison of measured, HFSS, and model data for a step-up style transformer with $D_{out} = 300\mu$m, $W = 10\mu$m, $s = 2\mu$m, $N_p = 2$, $N_s = 1$. They, too, match quite well.

3.4.2.3 Segmented and interleaved structures

Various transformer test structures (Table 3.3) using the segmentation scheme were fabricated. If the outer dimension (D_{out}) is to be kept constant, the inductances (L) will

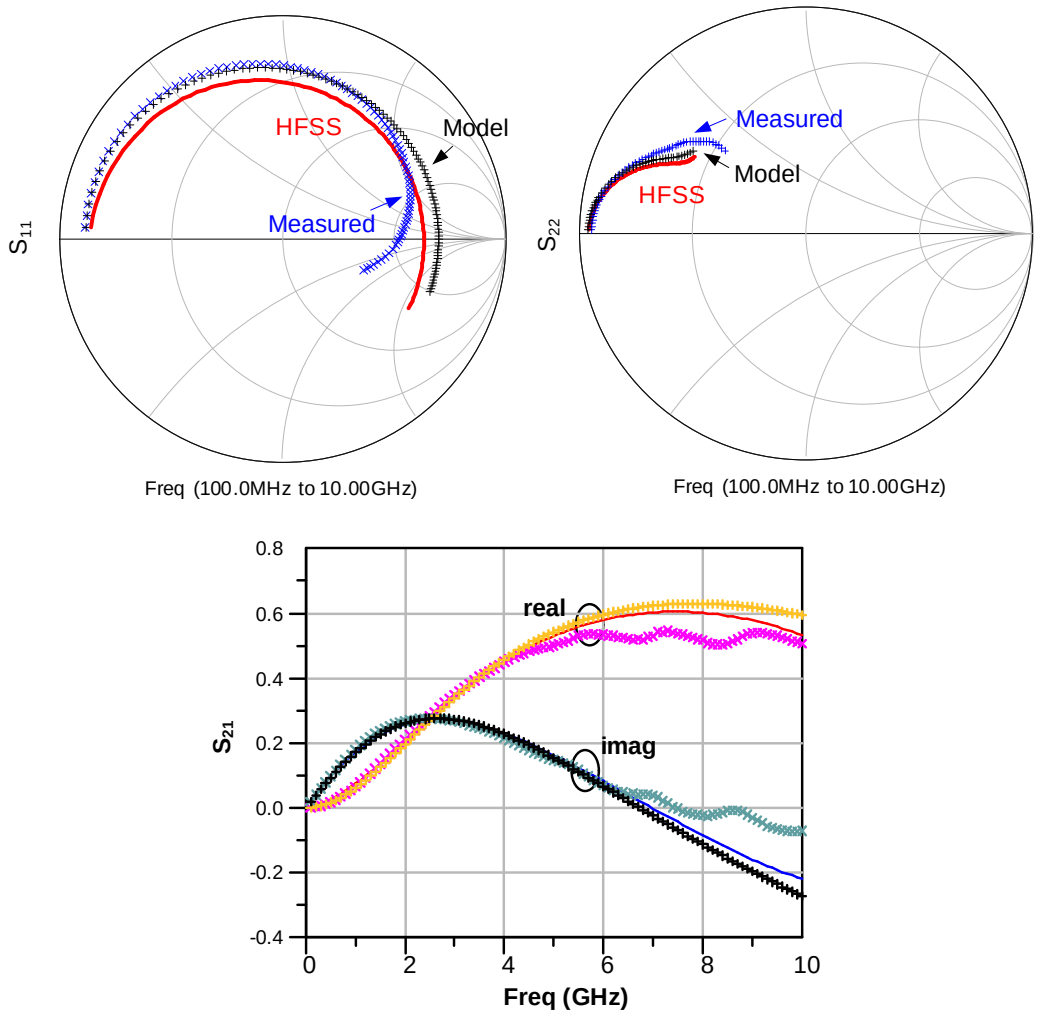


Figure 3.7: Comparison of measured, HFSS and model data for step-up style transformer with $D_{out} = 300\mu$m, $W = 10\mu$m, $s = 2\mu$m, $N_p = 2$, $N_s = 1$. Label x: measured; +: Model; line: HFSS.

decrease as the traces are split into more segments (#A, B, C). Alternatively, D_{out} will need to grow (#D, E, F) to achieve the same L.

Transformer	N_{seg}	W_p,W_s (μm)	D_{out} (μm)	s (μm)	L_p (nH)	L_s (nH)	Peak Q_p	Peak Q_s	k
A	1	32	400	2	0.85	0.68	8.8	13.0	0.55
B	2	16	400	2	0.68	0.59	9.0	12.0	0.76
C	4	8	400	2	0.56	0.52	8.5	11.5	0.85
D	1	35	654	2	1.65	1.44	7.0	9.0	0.61
E	2	17.5	720	2	1.58	1.48	6.7	8.3	0.81
F	5	7	796	2	1.56	1.51	6.3	7.0	0.91

Table 3.3: Transformer geometry parameters (as defined in Figure 3.2) and measured results.

Table 3.4 shows good agreement of the open-short de-embedded measured data, HFSS simulation, and model results of L_p, L_s and k for transformer structures A, B and C.

	L_p(nH)			L_s(nH)			k		
	Meas	HFSS	Model	Meas	HFSS	Model	Meas	HFSS	Model
A	0.85	0.84	0.94	0.68	0.70	0.72	0.55	0.59	0.55
B	0.68	0.72	0.75	0.59	0.65	0.65	0.76	0.73	0.74
C	0.56	0.64	0.62	0.52	0.61	0.57	0.85	0.79	0.86

Table 3.4: Comparison of measured, HFSS simulation, and Model results of L_p, L_s and k for transformer structure A, B and C.

Figure 3.8 shows the comparison of measured, HFSS and model data for transformer B. The results match quite well up to 4GHz. Similar matching for other transformers are observed.

Figure 3.9 shows that for transformers A, B and C, the quality factor reduces when the N_{seg} increases. However, the ILm of transformer C is about 0.4dB less than the ILm

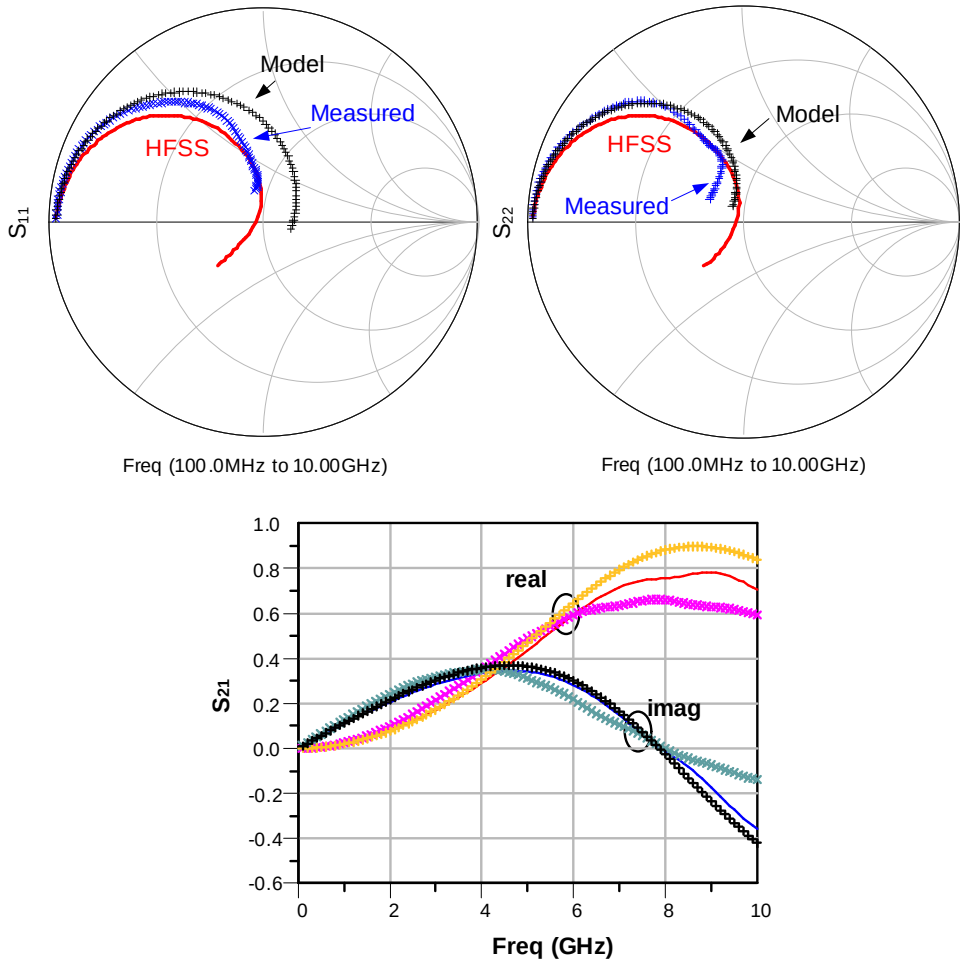


Figure 3.8: Comparison of measured, HFSS, and model data for segment-interleave style transformer B. Label x: measured; +: Model; line: HFSS.

of A due to the improvement of k. An ILm as low as 1dB can be achieved (Figure 3.9, #C).

HFSS results (in Figure 3.10) show similar improvement of the ILm with the segmentation and interleaving. The absolute values of the ILm from HFSS simulations differ from the measurement results due to the difference in the resistivity ($\rho = 2.78 \times 10^7$S/m) of the metal layers and other simplifications in the HFSS simulations.

Figure 3.11 shows a similar decrease of Q_p, Q_s and the ILm due to N_{seg} for transformers D, E and F.

Figure 3.12 shows that for the 2-turn Frlan style transformers, although the segmentation scheme still improves k, the decrease of Q offsets the benefit, and the resulting ILm is not improved. The geometry parameters are shown in Table 3.5.

3.5 Summary

This chapter discusses k, Q and ILm of various transformer structures. A novel layout scheme is proposed to improve k and ILm for transformers with wide traces. Test structures were fabricated and measured. The results are compared to HFSS simulation and model data. They all match quite well up to 4GHz.

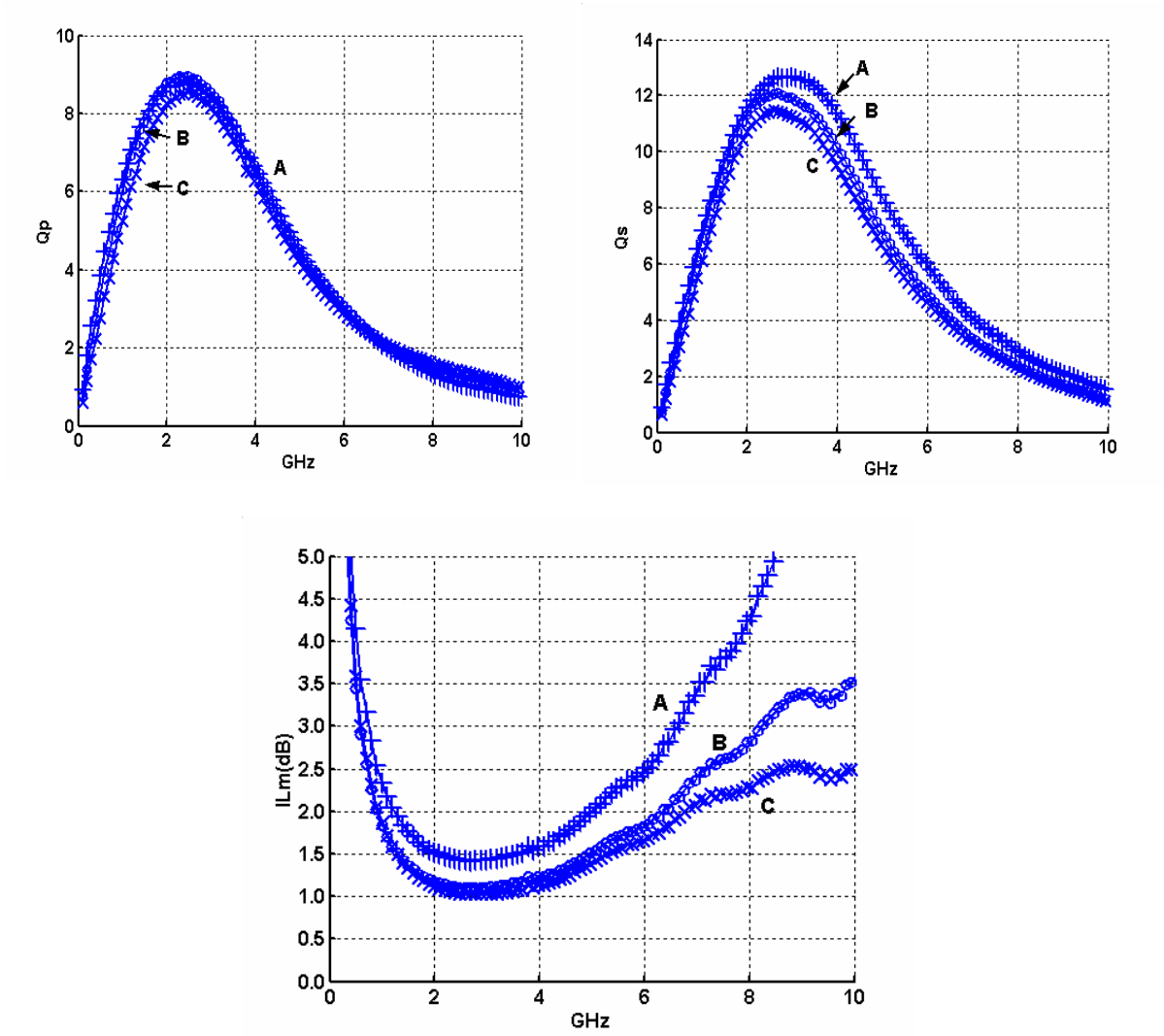


Figure 3.9: Q_p, Q_s and ILm comparison for transformers with same $D_{out} = 400\mu$m.

Transformer	N_{seg}	N	D_{out} (μm)	W_p,W_s (μm)	s (μm)	L_p (nH)	Peak Q	k
G	1	2	400	30	2	1.90	8.3	0.67
H	2	2	400	15	2	1.50	7.3	0.79
I	3	2	400	10	2	1.34	6.5	0.83

Table 3.5: Frlan style 2-turn transformer geometry parameters and measured results.

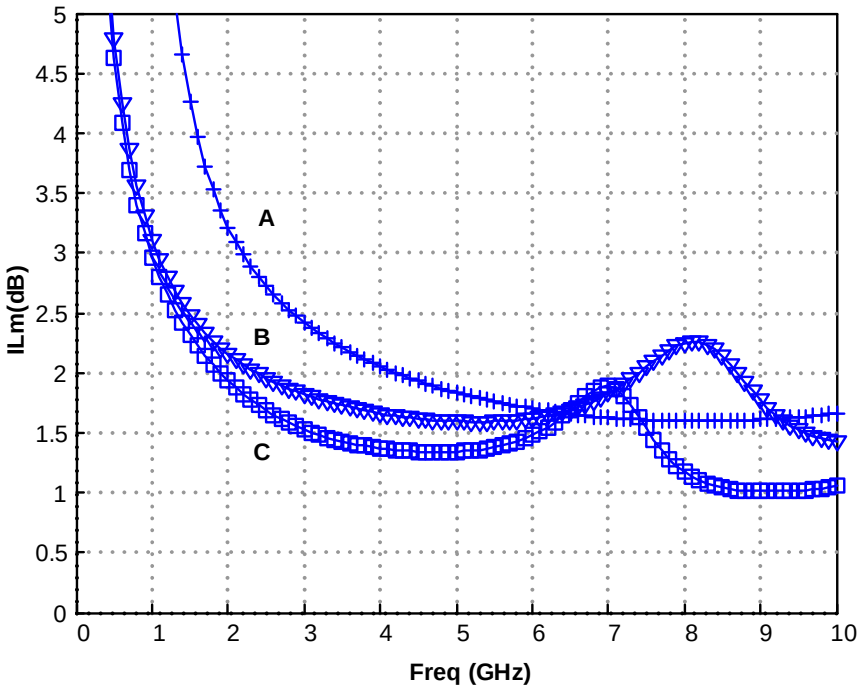


Figure 3.10: HFSS simulation results of structure A, B, and C.

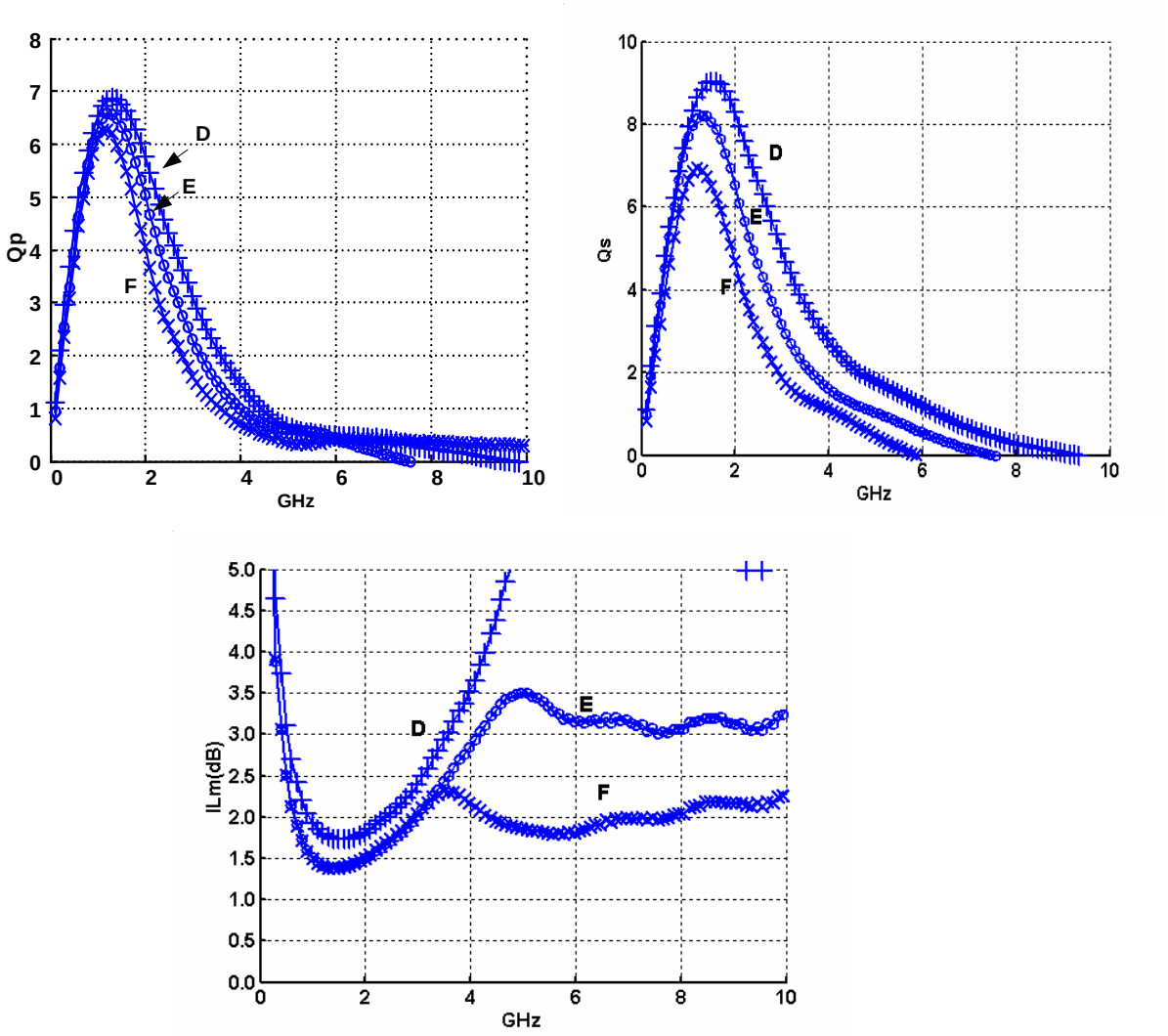


Figure 3.11: Q_p, Q_s and ILm comparison for transformers with the same $L \approx$1.6nH.

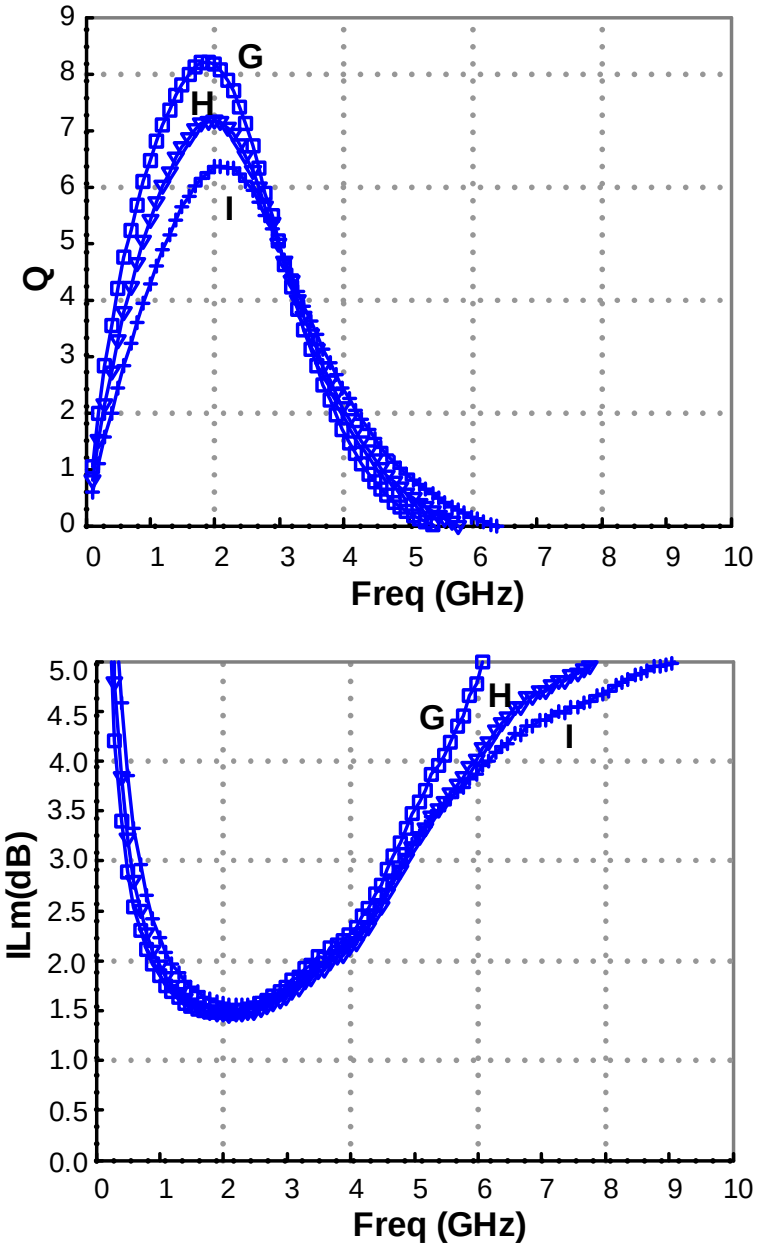


Figure 3.12: Minimum insertion loss comparison for transformers in Frlan style and $N = 2$.

Chapter 4

Power Amplifier with Transformer Balun

4.1 Introduction

This chapter first summarizes the basic types and performance measures of different power amplifiers. Different impedance matching networks and output baluns are also presented. The transformer as output balun is discussed in detail and two layouts are fabricated and compared. Then a one-stage class AB push-pull power amplifier with output transformer balun is examined in more detail. This PA is suitable for 2.4GHz wireless LAN application.

4.2 Basics of PA Class

Depending on the operating mode of the output transistors, PAs can be divided into two groups, linear and switching modes. In the linear mode PAs, the output transistor acts as a voltage-controlled current source. This type of PAs includes class A, B and C amplifiers. In the switching mode PAs, which comprise class D, E and F amplifiers, the output transistors act as an on-off switch. Due to its switching nature, this type of PA

is non-linear.

4.2.1 Output power

The performance of the RF power amplifiers can be evaluated by several metrics. The output power of an RF power amplifier is defined as the total power of the RF signal within the band of interest delivered to the load. In case of a sinusoidal signal, the output power is simply

$$P_{out} = \frac{V_{out}^2}{2R_L} \tag{4.1}$$

where V_{out} is the amplitude of an output RF signal and R_L is the load impedance, which is often 50Ω.

4.2.2 Efficiency

Amplifier efficiency is used to compare the performance of different PAs. Several definitions of efficiency have been used as performance metrics. The drain efficiency is defined as

$$\eta = \frac{P_{delivered}}{P_{DC}} \tag{4.2}$$

where $P_{delivered}$ is the RF power delivered to the output and P_{DC} is the total DC power consumption. The drain efficiency is often used as a performance measure for a specific stage and/or output transistors.

The power-added efficiency (PAE) is defined as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{4.3}$$

It is the ratio of the RF power generated by the amplifier to the total DC power drawn from the supply.

4.2.3 Linearity

Different linearity is required for different standards. Linear amplification is needed for some modulation schemes such as QPSK or QAM, which generate a modulated signal with variable voltage amplitude. For other modulation schemes such as GFSK and GMSK, which generate signals with constant envelope, a nonlinear power amplifier can be used at the expense of larger frequency bandwidths for a given data rate.

A measure commonly used to assess the power amplifier nonlinearity is the output 1-dB compression point P_{1dB}, which is defined as the point where the output power of the amplifier is 1dB below the level extrapolated from the linear small-signal region.

The spectrum emission is defined as the power spectral density of a transmitter's output. Nonlinear amplification of a signal may cause the signal to spread to adjacent frequency bands, a phenomenon called spectral regrowth. The spectral mask, often defined by communication standards, sets a limit on the spreading of the power density spectrum, harmonics of the carrier frequency, and other unwanted spurious signals generated by the amplifier.

Another measure of an RF power amplifier's nonlinearity is the adjacent channel power ratio (ACPR), which is defined as the ratio of the total power within a certain bandwidth, usually an adjacent channel, to the total power within the transmission bandwidth. The worse the nonlinearity, and thereby the spectral regrowth, the larger the power in the adjacent channel. Unlike P_{1dB}, the ACPR is heavily dependent on the modulation and signal.

4.2.4 Comparison of class A-F PAs

The performance summary for different classes of PAs is given in Table 4.1 [5]. The linearity required by a standard is a key factor in choosing the architecture and topology of the PAs. Generally, linearity can be increased at the cost of power efficiency by choosing a different class of PAs. Class A, AB and B amplifiers are often selected for

Class	Mode	Conduction angel	Max drain efficiency η (%)	Norm $V_{d,max}$ $\frac{V_{d,max}}{V_{dd}}$	Norm $P_{out,max}$ $\frac{P_{out,max}}{V_{dd}^2/(2R_L)}$	Power capability $\frac{P_{out,max}}{V_{d,max}I_{d,max}}$	Linearity
A	Current source	100%	50	2	1	0.125	Good
B		50%	78.5	2	1	0.125	Moderate
C		$< 50\%$	100	2	1	0.11	poor
D	Switch	50%	100	2	1.62	0.32	poor
E		50%	100	3.6	1.15	0.10	poor
F		50%	100	2	1.62	0.16	poor

Table 4.1: Summary of some basic PA measures for classes A-F.

applications such as 802.11 wireless LAN, where linearity is a major concern. On the contrary, switching amplifiers such as class E and F are used for applications where linearity can be exchanged for improved power efficiency.

4.3 Output Matching and Balun Structures

As the supply voltage of sub-micron CMOS technology scales down, output impedance transformation and matching networks are often needed to achieve output power levels higher than 100mW. Push-pull differential configuration can increase the output power for a fixed supply and impedance limitation. However, most RF instruments and typical antenna ports require single-ended connection. Therefore, a balun is needed to convert the differential signal to a single-ended signal.

Conventionally, baluns are often realized on board by transmission line structures, e.g., the Marchand balun [32] and the ring-hybrid [33] (shown in Figure 4.1 (a) and (b)), or by discrete components. To reduce the number of board-level components and increase the integration level, several on-chip baluns have been presented in literature. Transmission line structures are often area-consuming with quarter wavelength ($\lambda/4$) sections and are not easy to realize on chip for low GHz applications in standard processes [32]. An LCCL balun [34] was integrated on-chip with a 4.8-6 GHz power amplifier (shown

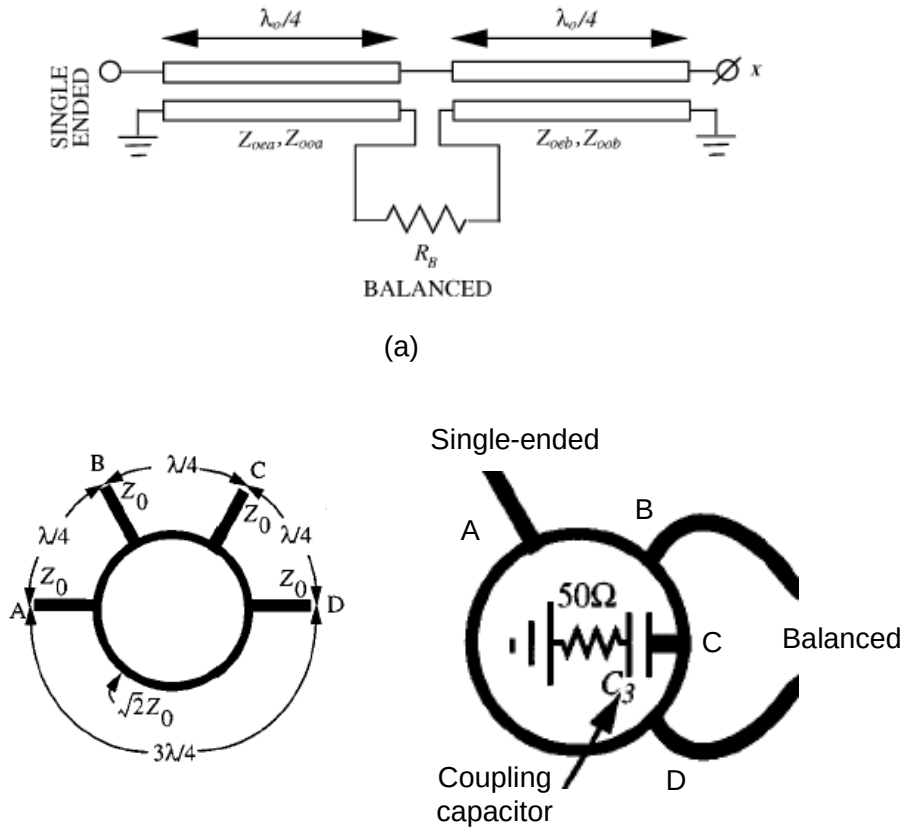


Figure 4.1: Conventional balun structures (a) Marchard balun and (b) ring-hybrid.

in Figure 4.2). It was a compact solution based on lumped components, but it required careful tuning. Distributed active transformer (DAT) structure was introduced in [26] (shown in Figure 4.3) for class E amplifier. It combined eight output transistors in parallel in a ring structure, and the secondary of the transformer acted as the power combiner. The transformer balun can easily be designed symmetrically, and thus desensitize the operation of the amplifier to the inductance of bonding wires. However, the wide traces required for the large DC current degrade the coupling coefficient k of the transformer to about 0.5∼0.6. Cheung [35] showed a 4-way transformer balun with improved k for a 21-27 GHz power amplifier.

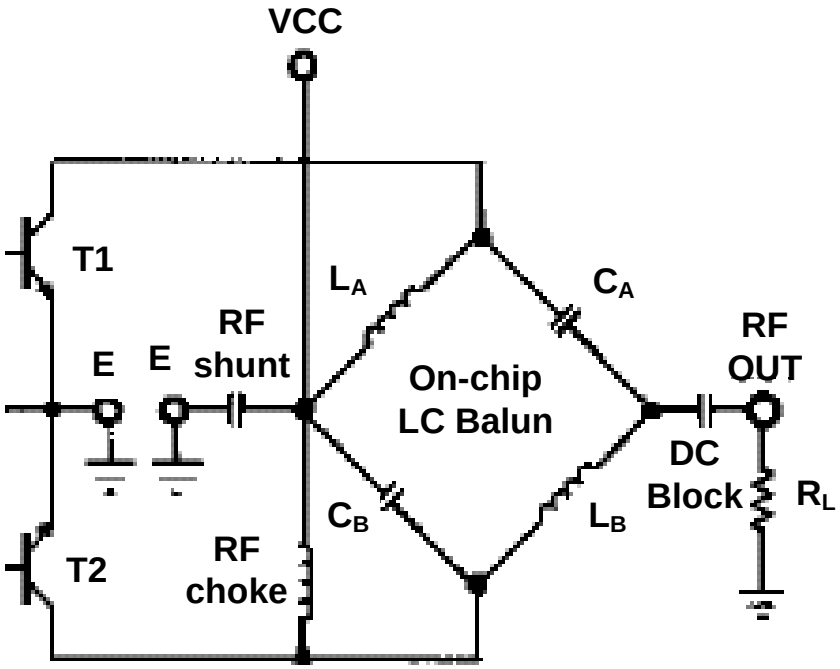


Figure 4.2: LCCL balun with RF chokes in a differential PA circuit.

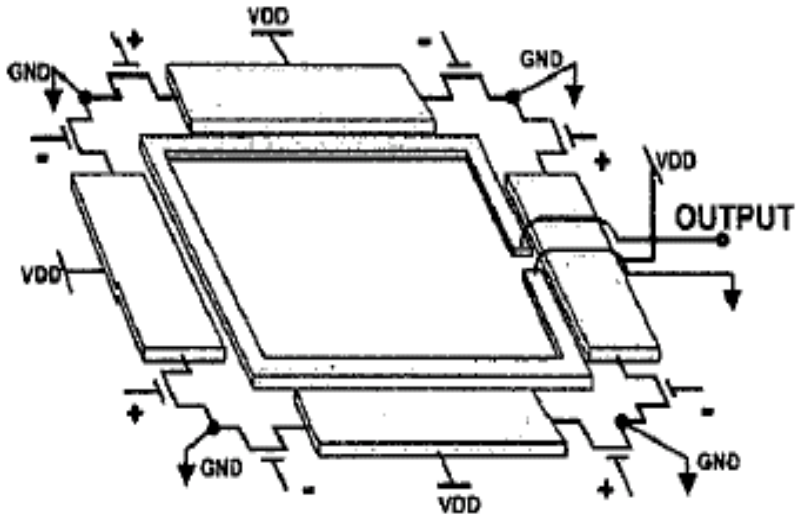


Figure 4.3: Distributed active transformer with 8 transistors.

4.4 Transformer Design

For transformer baluns, especially those used for power amplifiers, there are some practical issues. Usually a one-turn transformer is chosen for its better quality factor. Wide traces are used to meet the current density rules. Therefore, the magnetic coupling coefficient k is relatively small (around 0.5$\sim$0.6). Transformers with traces segmented and interleaved, which were discussed in the previous chapter, can be used to improve k.

4.4.1 Area concern

A transformer layout with large area may pose problems such as low metal coverage and increased PGS and/or substrate losses. It is possible to fold the square structure to reduce the area. Table 4.2 shows an outer dimension comparison of the square and folded structures (shown in Figure 4.4). For L =1.6nH, which is the optimum inductance for a 50Ω load at 2.4GHz, the area is reduced by 25% for the folded structure, with minimum impact on the Q. Further folding does not help in reducing the area.

Structure	$W(\mu$m)	30	40	50	60
(a)	$Do(\mu$m)	640	680	740	780
(b)	$Do(\mu$m)	385	420	450	480

Table 4.2: Outer dimension Do comparison for various widths W with the same inductance (L =1.6nH) for structures (a) and (b) shown in Figure 4.4.

4.4.2 Reduce imbalance

As shown in Figure 4.5, for a one-turn balun, the approximate voltage along the secondary trace is from 0 to V at the output. Thus, each primary half sees a different secondary voltage swing through the coupling capacitance, resulting in unequal load impedance seen at the primary ports, and difference in gain and phase difference [35]. Increasing the spacing between the primary and secondary, thereby decreasing the coupling capacitance, can alleviate this problem to some extent at the expense of reduced k. To solve this

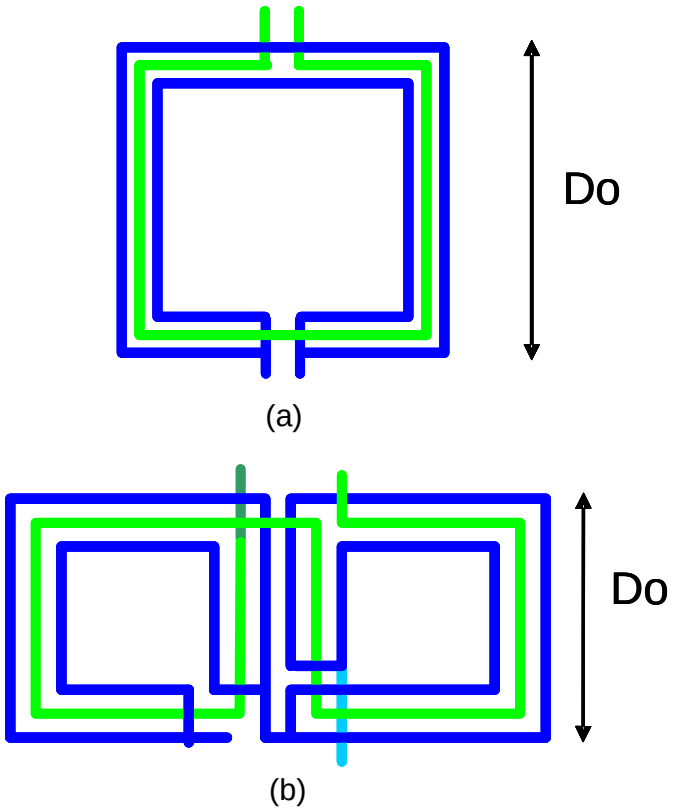


Figure 4.4: Sample structures for area comparison (a) square and (b) folded.

design dilemma, the traces can be segmented and interleaved in a way that restores the symmetry as shown in Figure 4.6(b).

4.4.3 Transformer results

4.4.3.1 Transformer structures

To test the idea of segmentation and the balance problem discussed in the last subsection, two transformer structures are designed and fabricated as shown in Figure 4.6. The spacing between the traces is 5μm to reduce the coupling capacitances between traces.

Structure	$Do(\mu\text{m})$	$W_p(\mu\text{m})$	N_p	$W_s(\mu\text{m})$	N_s	s(μm)
A	450	24	2	20	1	5
B	450	16	3	10	2	5

Table 4.3: Geometries for structure A and B shown in Figure 4.6.

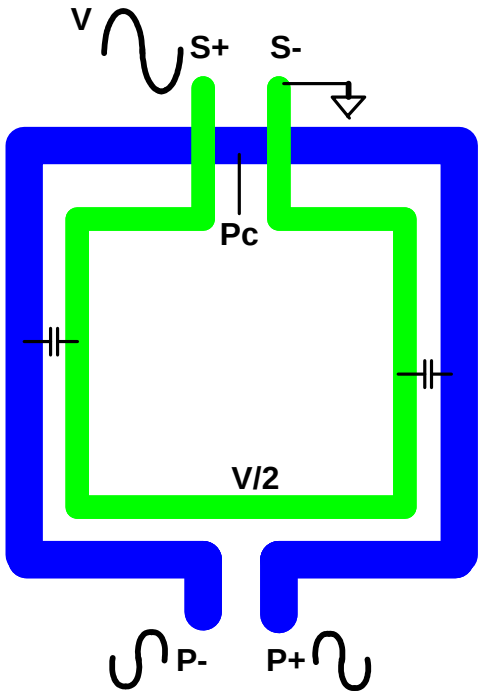


Figure 4.5: Each primary half sees a different secondary voltage swing through the coupling capacitance for a one-turn balun.

For structure A, the secondary trace is sandwiched in two parallel traces of the primary. Each primary trace is about the same physical length to improve the quality factor. Yet the primary traces still see a different secondary voltage swing.

For structure B, the primary and secondary have the same outer dimension and total metal width as structure A. The primary coil has three 16μm-wide segments, interlaced with two 10μm-wide segments of the secondary, resulting in a turn ratio of 1.1. The two secondary traces are routed so that each primary half sees about the same average voltage swing of the secondary.

4.4.3.2 Measurement method

To measure a 3-port device with a 2-port network analyzer, the test setup is shown in Figure 4.7. The method [32] is as follows:

- Terminate the 3rd port using auxiliary load, e.g., 50Ω.

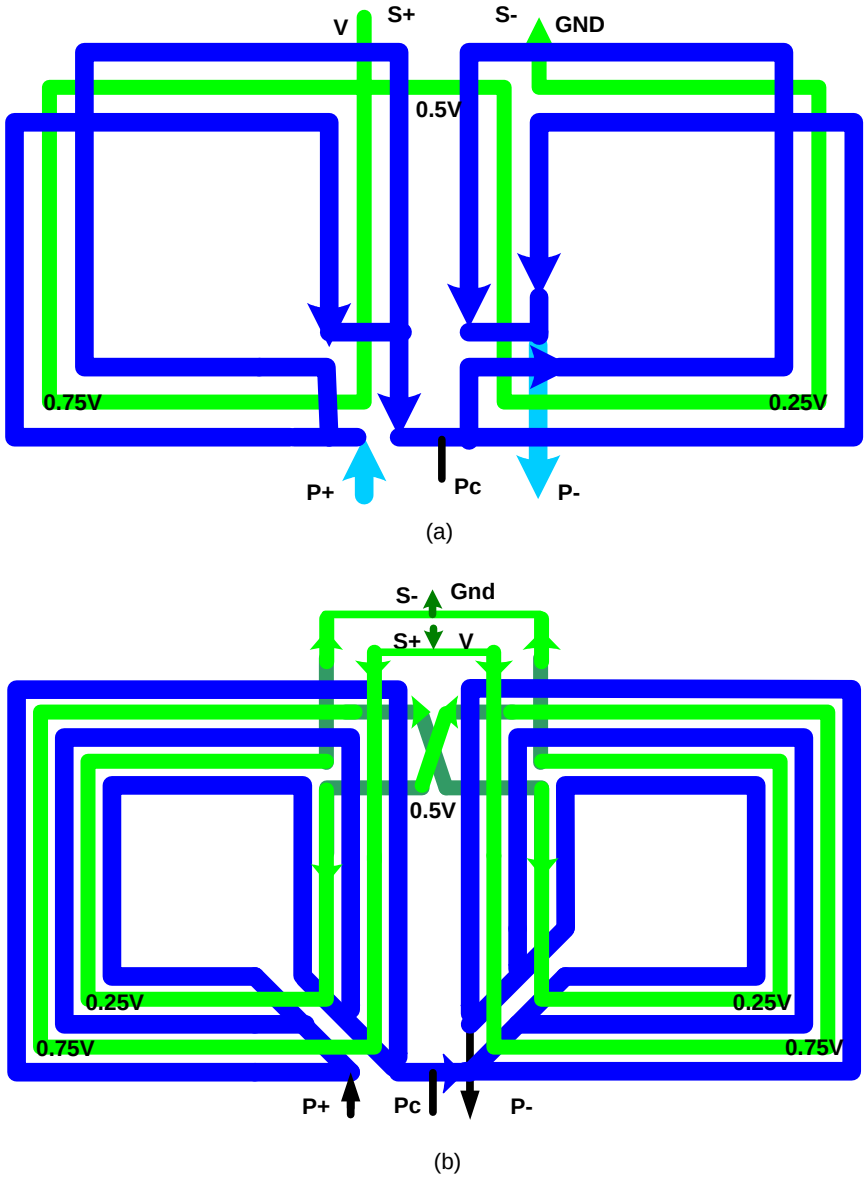


Figure 4.6: Output balun structures fabricated and tested: (a) structure A and (b) structure B.

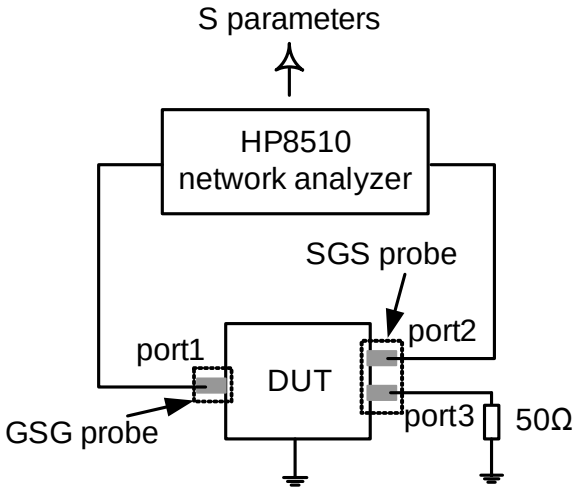


Figure 4.7: Test equipment setup for 3-port measurement using 2-port network analyzer.

- Make three 2-port measurements.
- 3 port S-parameter matrix construction:
  - De-embed each 2-port measurement result
  - Construct the reflection coefficient matrix Γ of the auxiliary load
  - Correct the S matrix using the following relationship

$$S' = S - (I + S)\Gamma(I - S\Gamma)^{-1}(I - S) \tag{4.4}$$

where S' and S are the corrected and measured S matrices.

4.4.3.3 Coupling coefficient k

The comparison of the magnetic coupling coefficient k of structures A and B is shown in Figure 4.8. The k of structure B is increased to 0.8 at 2.4GHz, and is 10% better than that of structure A.

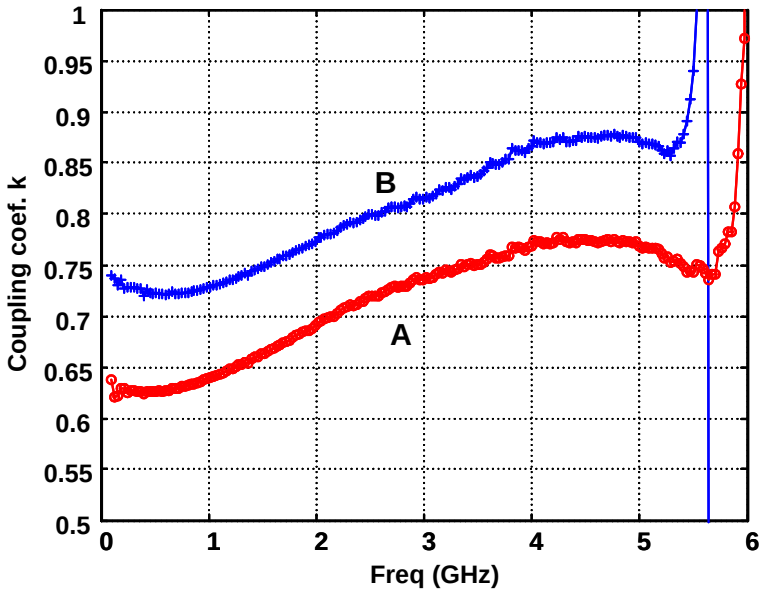


Figure 4.8: Comparison of the coupling coefficient k for structures A and B.

4.4.3.4 Amplitude and phase differences

The two structures shown in Figure 4.6 were simulated in HFSS and fabricated in a five metal 0.18μm standard CMOS digital process. The top three Al metals with an effective thickness of 2μm were strapped to reduce the ohmic loss. Table 4.4 shows the comparison of the amplitude and phase differences for structures A and B at 2.4GHz. Although the absolute values are different, both the HFSS and measured results indicate that structure B does have a smaller amplitude and phase differences because of the more symmetric layout.

Structure	Amplitude Diff (dB)		Phase Diff(°)	
	HFSS	Measured	HFSS	Measured
A	1.69	0.84	185.4	186.6
B	0.63	0.25	183.5	185.4

Table 4.4: Comparison of HFSS and measured results of amplitude and phase differences for structures A and B.

The measured amplitude and phase differences of structures A and B over a frequency range are shown in Figure 4.9. Structure B shows a better performance over the 2∼3

GHz range.

4.4.3.5 Minimum insertion loss

To measure minimum insertion loss for a 3-port device is not very straightforward. There are two ways to estimate the minimum insertion loss from measured data:

(I) Eqn. (2.5) is used to transform the S-parameter matrix S_{se} of three single-ended ports to the mixed-mode S-parameter matrix S_{mm} of one single-ended port and one pair of differential (balance) ports. Then the top 2x2 matrix of S_{mm} can be applied to Eqn. (2.28). If the balun is well-designed and symmetric, the result should be close to the minimum insertion loss.

(II) Back-to-back simulation as shown in Figure 4.10 can be used. The measured single-ended matrix S_{se} is used in the simulation. Tuning capacitors are added to resonate the inductance at the target frequency. Also the terminal source resistance is set to 50Ω. The minimum insertion loss is half of S_{21} in dB.

Figure 4.11 shows the comparison of the estimated minimum insertion loss from these two methods. Both show that structure B has a smaller insertion loss than structure A. The result from method (II) is larger than that from method (I) because of two reasons. One is the imbalance due to asymmetry. The other is because the 50Ω terminal resistance, which may not be the matching load for the transformer.

4.4.3.6 Comparison of measured and modeled results

Using the broadband model presented in previous chapters, the S matrix of structure B is calculated and compared to the measured data (shown in Figure 4.12). The model result and the measured data match well up to 4 GHz.

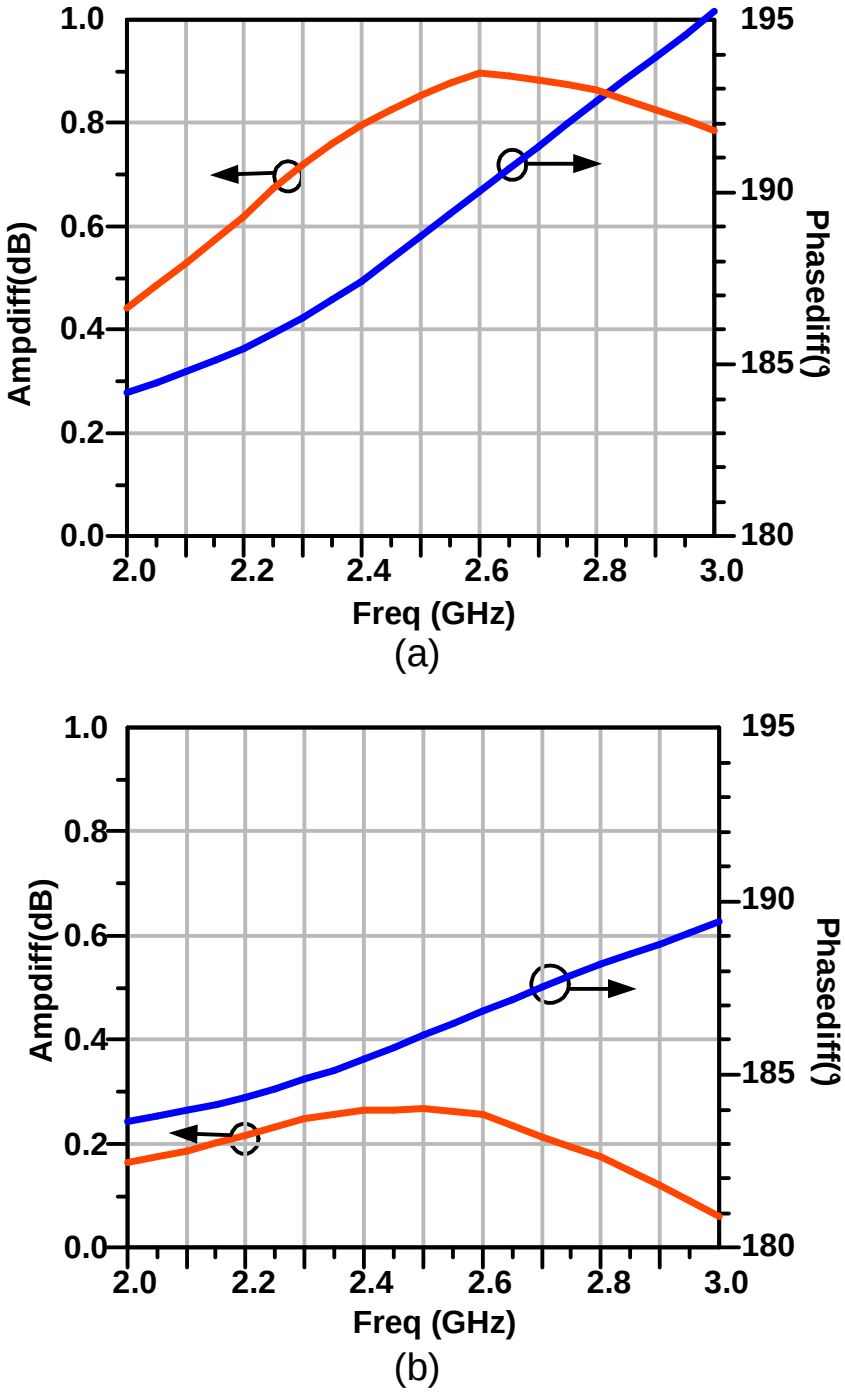


Figure 4.9: Measured amplitude and phase differences versus frequency for (a) structure A and (b) structure B.

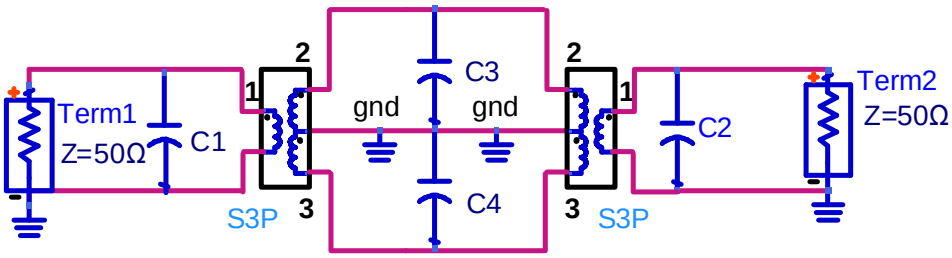


Figure 4.10: Back-to-back simulation setup to get minimum insertion loss.

4.5 Circuit Design

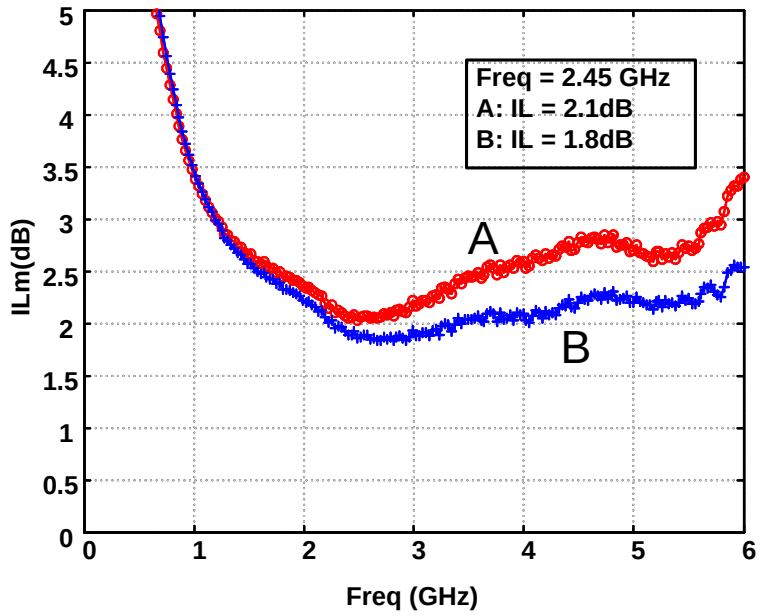
The transformer baluns characterized in the previous section were integrated on-chip as the output balun in a one-stage push-pull differential power amplifier for 2.4GHz wireless LAN applications. The transistors were biased in class AB for optimum tradeoff in linearity and power efficiency.

The circuit schematic is shown in Figure 4.13. The transformer primary also serves as the inductive loads for the differential PA and has a center tap connected to the 3.3V-supply. The cascode transistors M3 and M4 are I/O devices to withstand the high voltages. The 22Ω loads seen by each half of the differential output transistors are transformed to about 50Ω at the transformer secondary to match the load of the antenna.

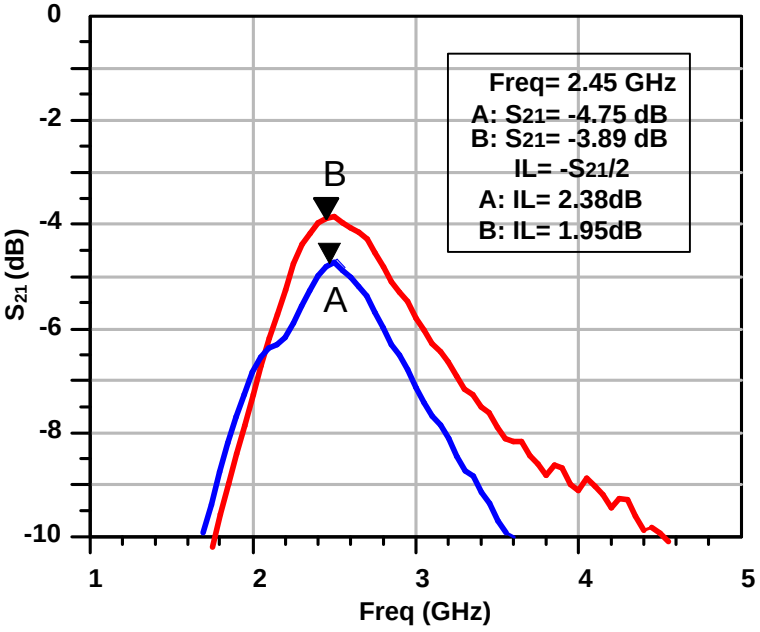
For testing purposes, a 1:2 on-chip balun with capacitors was used to match the 50Ω of the measuring equipment. The balun also resonates the large gate capacitance of the wide transistors.

The simulated result shows that:

- Freq = 2.45GHz
- I_{dc} = 120mA at 3.3V supply
- P_{1dB} = 18.3dBm
- $P_{out,max}$ = 23.7dBm at P_{in} = 10dBm



(a)



(b)

Figure 4.11: Comparison of insertion loss from two methods: (a) ILm from method (I) and (b) S_{21} from method (II).

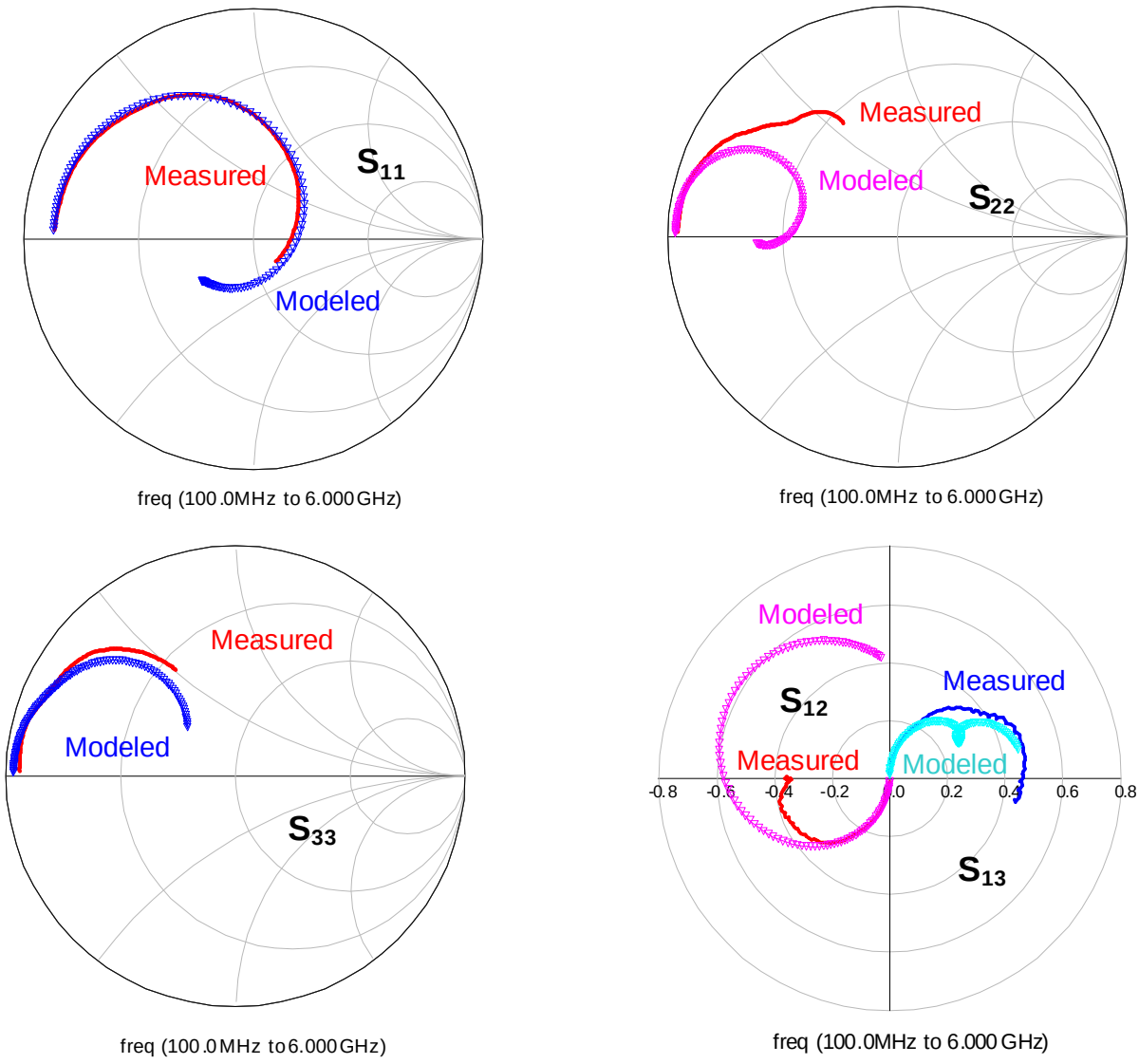


Figure 4.12: Comparison of model (triangle) result with measured (line) result.

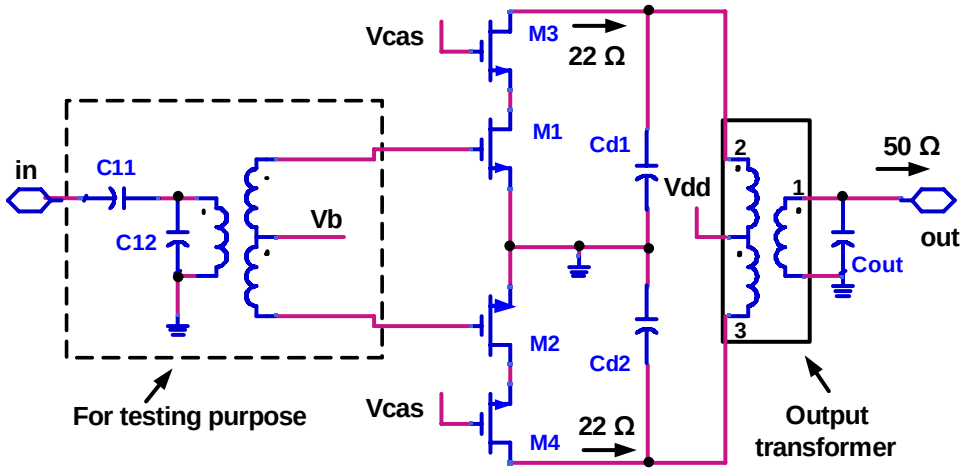


Figure 4.13: The circuit schematic for one-stage PA.

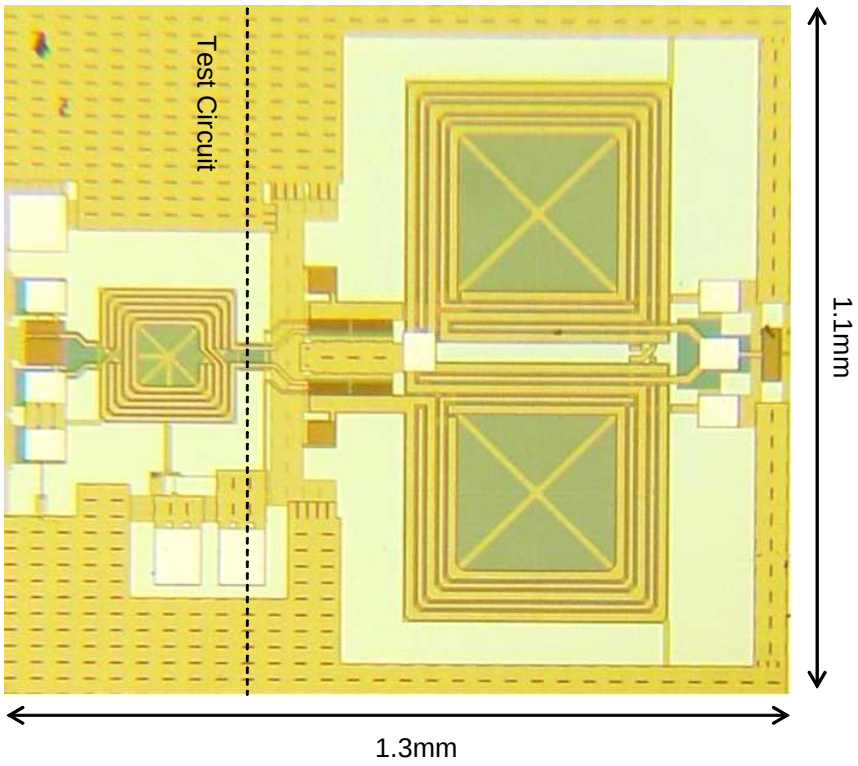


Figure 4.14: Die microphoto for the one-stage PA.

4.6 PA Performance

Figure 4.14 shows the die microphoto of the PA with structure B as the output balun. The core area is 0.91mm^2 (1.43mm^2 total). The chip is directly bonded to 0.062 inch FR4 board. No board level input or output matching element is used.

Figure 4.15 shows the S_{11} and S_{22} of the PA. At 2.45GHz, both $|S_{11}|$ and $|S_{22}|$ are less than -10dB, indicating good matching.

The output power and small signal gain of the PA versus the input power are shown in Figure 4.16. The maximum output power is 21dBm when the input power is 10dBm. The small signal gain is 17.5dB when the DC bias current is around 107mA. The 1dB compression point P_{1dB} is about 17dB. For different frequencies in the 2.4-2.5GHz range, the output power changes little for the same input power. The power-added efficiency versus input and output powers is shown in Figure 4.17. The maximum PAE is 21% while the PAE is about 10% at P_{1dB}.

Compared to the simulated result, the measured maximum output power and the P_{1dB} are smaller mainly because the generic transistor model used in the simulation does not account for the substrate resistance and some other effects.

For a fixed bias circuit, the power efficiency degrades considerably when the output power level is backed-off from the maximum output power. There are many ways to improve the linearity and efficiency of the power amplifier at the expense of more complexity. The linearization schemes can be put in several categories:

- At the input
  - Pre-distortion [36]
  - Cartesian feedback [37]
  - Polar feedback
- At the output
  - Feed-forward [38]

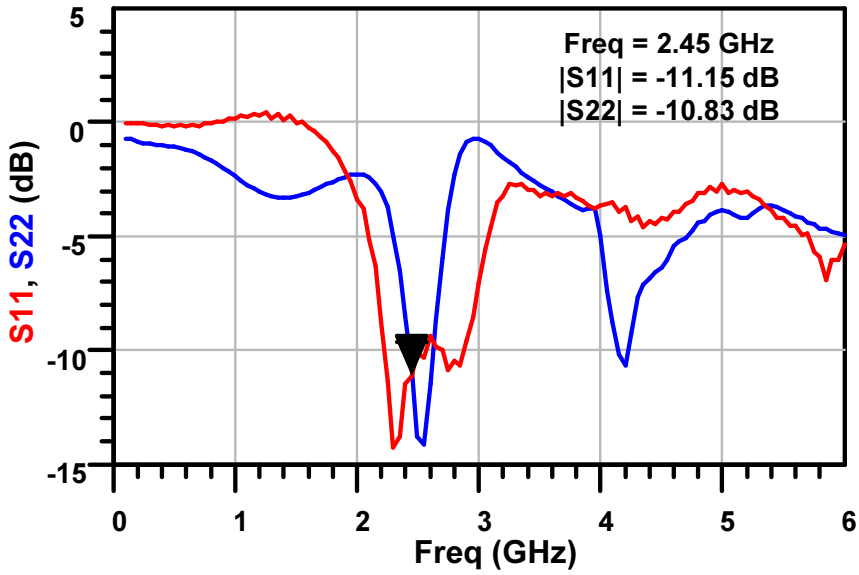


Figure 4.15: S_{11} and S_{22} of the PA.

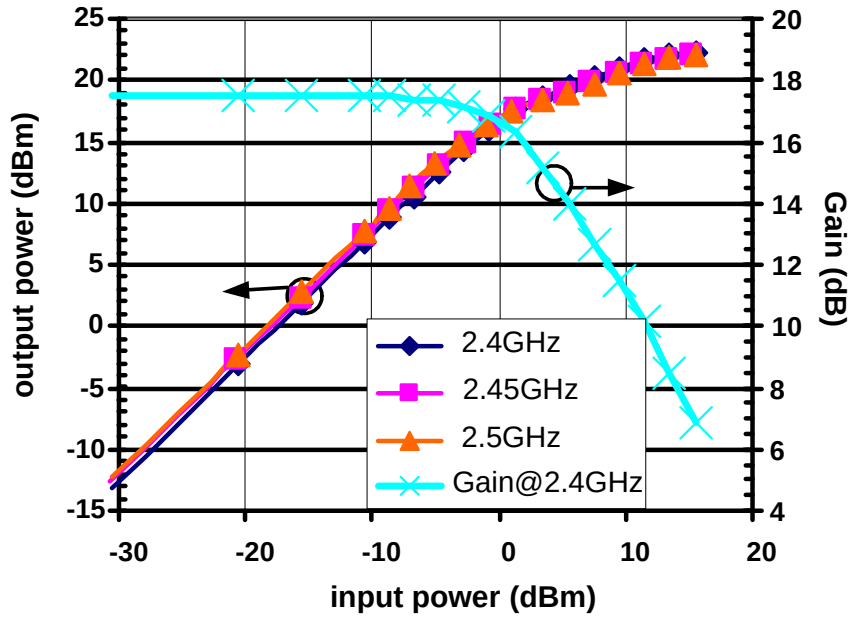
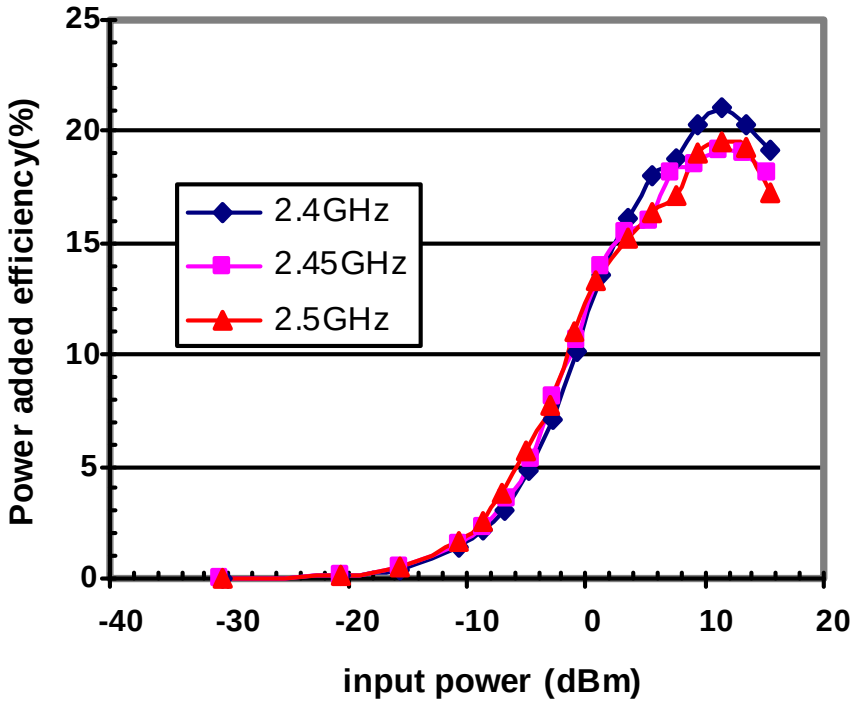
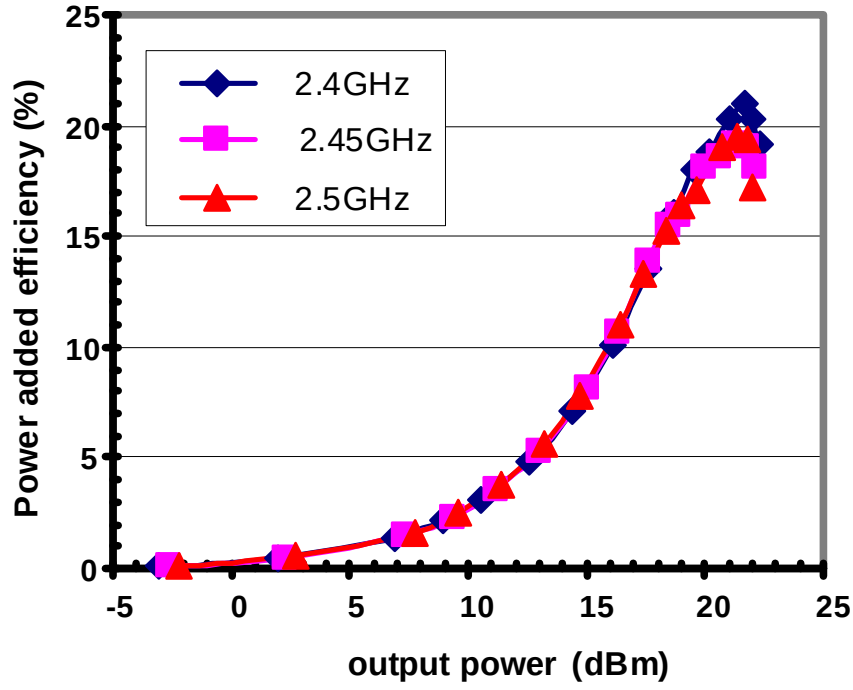


Figure 4.16: Output power and gain versus input power.



(a)



(b)

Figure 4.17: Power-added efficiency versus (a) input power and (b) output power for different frequencies.

  - Linear amplification with nonlinear components (LINC) [39]

- At the bias
  - Envelope elimination and restoration (EER) [40]
  - Sliding bias [41, 42]

4.7 Summary

This chapter provided a review of basic power amplifier topologies and performance measures. Different output matching and balun structures were discussed. Two transformer baluns, which were designed, fabricated and measured for 2.4GHz WLAN applications, were discussed. Baluns with good k, Q and symmetry were found to have small insertion loss. The chapter continued with the design details of a fully integrated medium output power one-stage differential PA with an output transformer balun. The measurement results were presented.

Chapter 5

Low Noise Amplifier with Transformer Balun

This chapter first reviews different configurations for low noise amplifiers (LNAs) and input matching schemes in section 5.1. Then a fully integrated receive path with a switch and an inductive source-degenerated differential common-source LNA with a transformer as the input balun is presented in section 5.2. It is designed for 2.4GHz wireless LAN applications. The receive path is fabricated in a five metal standard digital process. The measurement result for the input balun and the receive path is discussed in section 5.3. A fully integrated front end is enabled by this receive path and the power amplifier presented in the last chapter. The schematic is shown in section 5.4. Section 5.5 summarizes this chapter.

5.1 Circuit Design Considerations

5.1.1 LNA topologies

The low noise amplifier is a key component in a typical radio receiver and has been studied extensively. Generally, the main goal of the LNA design is to achieve simultaneous noise and input power matching. A number of design techniques have been demonstrated for

CMOS-based LNAs.

5.1.1.1 Common-source LNA (CSLNA)

A cascode CSLNA with inductive source degeneration and its small signal equivalent circuit are shown in Figure 5.1 [5]. It is a widely used topology in narrow-band RF applications. The cascode device decouples the input and output matching.

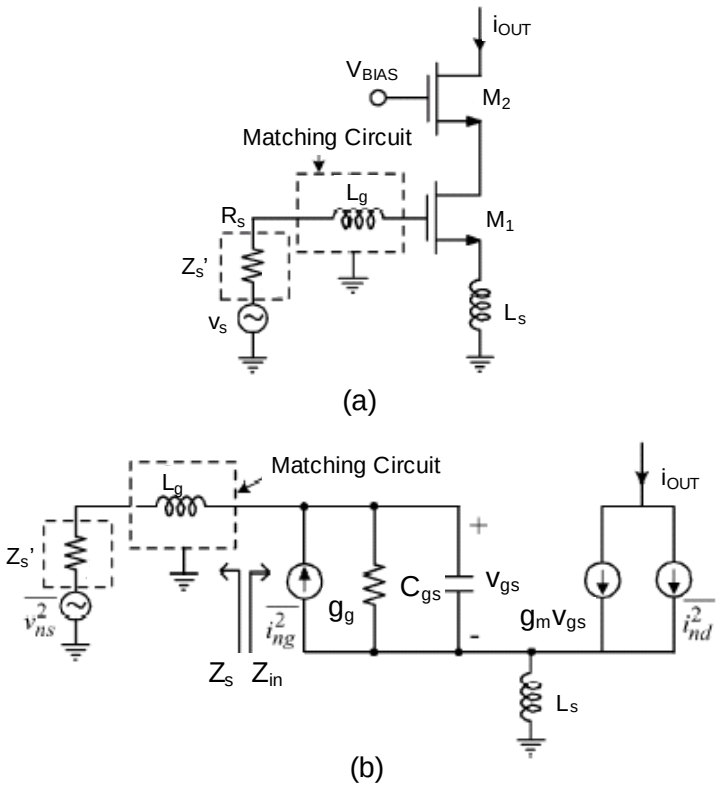


Figure 5.1: A cascode CSLNA with inductive source degeneration (a) schematic and (b) simplified small signal equivalent circuit.

Analysis [5, 43] shows that

$$Z_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \approx sL_s + \frac{1}{sC_{gs}} + \omega_T L_s \tag{5.1}$$

$$F_{min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1-|c|^2)} \approx 1 + 2.4 \frac{\gamma}{\alpha} \frac{\omega}{\omega_T} \tag{5.2}$$

where γ is a parameter related to $\overline{i_{nd}^2}$, the mean square of channel noise current. It is

a function of the transistor bias condition and channel length and is about 2 for short channel devices. Similarly, δ is a parameter related to $\overline{i_{ng}^2}$, the mean square of gate-induced noise current. With technology scaling, δ/γ stays nearly a constant 2. The parameter c is the correlation factor of the channel and gate-induced noise current. It is about 0.5 for 0.25μm technology. The parameter $\alpha = g_m/g_{d0}$ is about 0.85 for short channel device.

We can see from Eqn. (5.1) that the inductive source degeneration produces a real part $\omega_T L_s$ in the input impedance, which can be matched to the real part of the source impedance, and provides a simultaneous input and noise match. Eqn. (5.2) shows that F_{min} increases when the operating frequency approaches f_T.

With technology scaling, the ω_T of the transistor keeps increasing while the source resistance usually remains 50Ω. The resulting source inductance L_s can be very small and hard to control on-chip. At the same time, large inductance L_g is needed to resonate with the gate capacitance at the frequency of interest.

To make L_s and L_g more realizable on-chip without sacrificing the ω_T and thus F_{min} of the common source LNA, especially for low power applications, external capacitance can be added in parallel to C_{gs} as shown in Figure 5.2 [43].

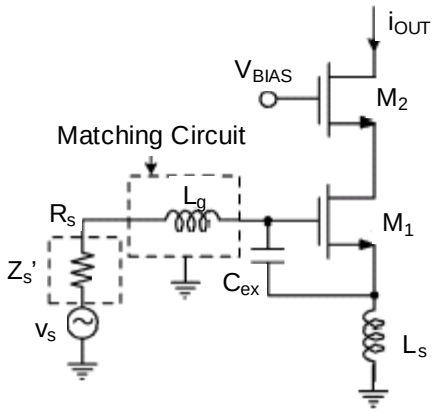


Figure 5.2: Inductive source-degenerated LNA with external capacitance for input matching.

The input impedance is given by

$$Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_m L_s}{C_t} \tag{5.3}$$

where C_{gs} is substituted by $C_t = C_{gs} + C_{ex}$. The relationship between F_{min} and ω_T in Eqn. (5.2) still holds. Thus the size and bias condition of the transistor can be chosen for F_{min} and good linearity, while C_{ex} is added to adjust the L_s and L_g value.

In [44], it is shown that inductive source-degenerated common-source LNA can also be used for broadband application with proper wide-band input matching.

5.1.1.2 Common-gate LNA (CGLNA)

A conventional CGLNA can also provide resistive input impedance as shown in Figure 5.3(a). The input admittance is given as

$$Y_{in} = g_m + s(C_{gs} + C_{pad}) + \frac{1}{sL_s} \tag{5.4}$$

Hence the resistance looking into the source terminal is about $1/g_m$ with proper matching. A proper transistor size and bias condition can provide the desired 50Ω resistance. However, the noise figure of the conventional CGLNA is

$$F_{min} = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{\omega}{\omega_T}\right)^2 \approx 1 + \frac{\gamma}{\alpha} \tag{5.5}$$

where the third term, accounting for the gate noise contribution, is usually negligible. Eqn. (5.5) shows that the noise figure is almost a constant regardless of the operating frequency. For a short channel device, it is around 5dB, which is not as good as that of a CSLNA in the low GHz frequency range.

Figure 5.3(b) shows a gm-boosted simplified topology [45]. The noise figure is changed to

$$F_{min} = 1 + \frac{\gamma}{\alpha}\frac{1}{1+A} \tag{5.6}$$

Thus, $(F-1)$ is reduced by a factor of $(1+A)$ on the condition that the boosting stage itself does not contribute significant noise, which makes a passive implementation such as a transformer [46] and a cross-coupled capacitor [47] a good choice. The transconductance of the device is reduced to $1/(1+A)R_s$, which means the power consumption is also reduced by a factor of $(1+A)$.

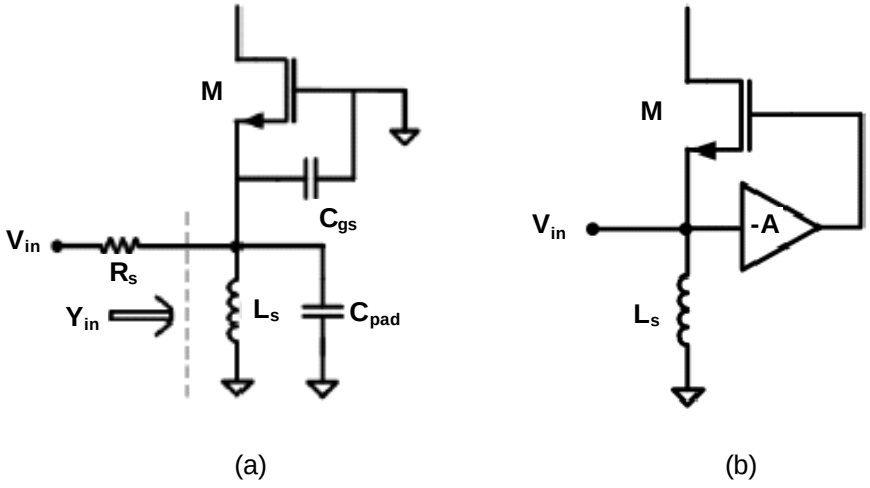


Figure 5.3: Common-gate LNA (a) conventional and (b) g_m-boosted feedback.

Figure 5.4 [45] shows the noise figure of various LNA topologies over the normalized frequency. For CGLNA, the noise figure is flat over all frequencies, while for CSLNA increases with frequency. Hence CGLNA can have a better noise figure at high frequencies. For gm-boosted CGLNA, the cross-over frequency is even lower. Also CGLNA has other advantages such as low power, and insensitivity to packaging parasitics, etc.

For a standard digital 0.18μm CMOS technology, the f_T is around 40GHz. At 2.4GHz, which is a frequency of interest for wireless LAN applications, $\omega/\omega_T < 0.1$. Thus theoretically, with $Z_{in} = 50\Omega$, CSLNA still works better than CGLNA or g_m-boosted CGLNA.

5.1.2 Input matching network

A differential circuit has the benefit of insensitivity to ground noise. Zhou [48] has used a Frlan-style transformer for the input matching of a 900MHz differential LNA. The transformer not only provides a better quality factor than two individual matching

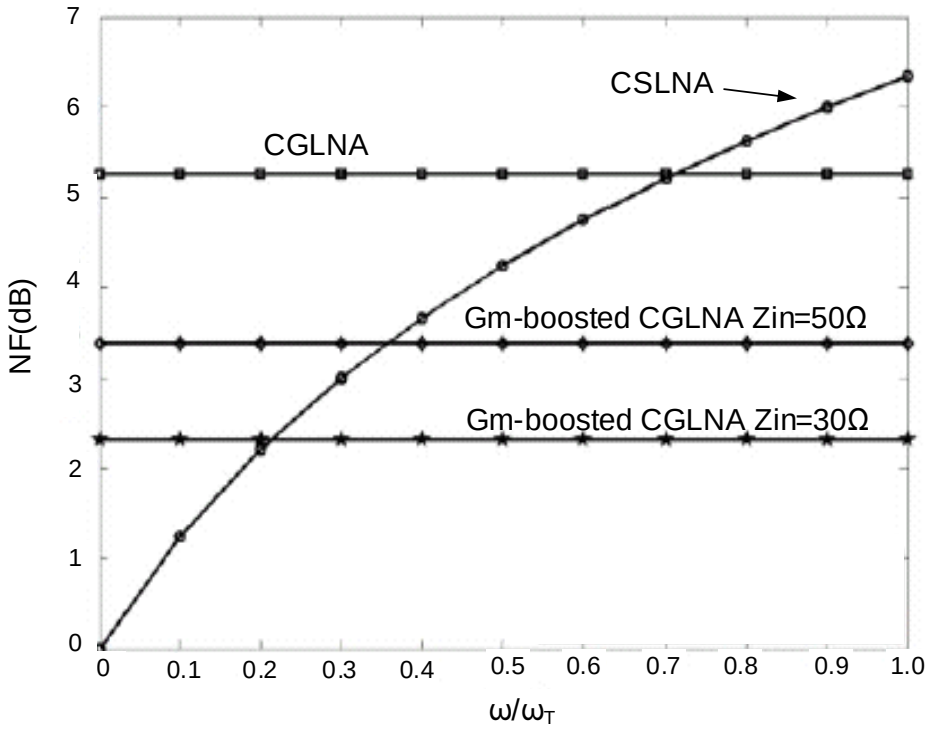


Figure 5.4: Noise figure vs. ω/ω_T for various LNA topologies.

inductors but also additional common-mode rejection in a fully differential application. However, it still requires an off-chip balun.

For communication systems utilizing the time-division duplexing (TDD) technique, a Transmit/Receive (T/R) switch is often used. In [8], an integrated T/R switch for wireless LAN applications is demonstrated. The receive switch utilizes a C-L-C π-network. To integrate the receive switch with an input balun, which provides good noise and power matching, needs careful design.

5.2 Circuit Schematic

A key challenge of integrating a receive switch and a transformer with an LNA is to match the input impedance without introducing excessive loss and noise. This is accomplished with the LC tuning network and a properly designed transformer as shown in Fig. 5.5. In receive (Rx) mode, Vctrl is set to GND and turns off transistor X_1. The π-network of

L_1 (3.8nH), C_1 (768fF) and the transformer primary (1.66nH) matches the antenna to the LNA input. The LNA is a fully differential, inductively degenerated common-source amplifier. The bias of the input transistors is fed from the center tap of the transformer secondary. A source follower stage is included only for test purposes. In transmit (Tx) mode, Vctrl is set to V_{dd} and turns on X_1. With the drain of X_1 pulled to GND, L_1 and C_1 form a parallel tank that resonates at 2.45GHz, and presents a high impedance to effectively minimize the leakage of the transmit signal to the receive path.

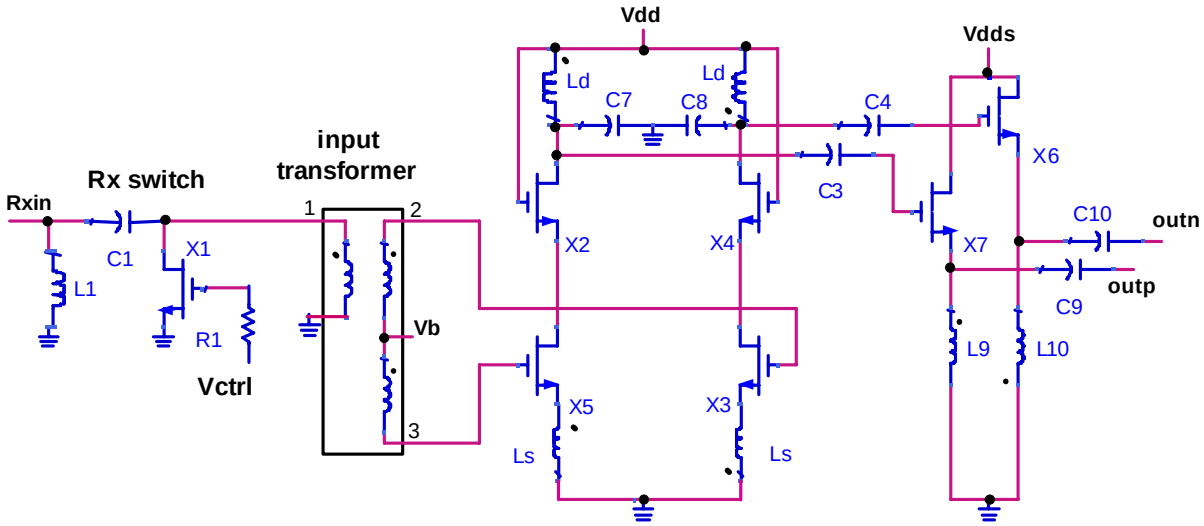


Figure 5.5: Schematic of the receiver path including a switch and an LNA with input transformer balun.

Figure 5.6 shows the die microphoto of the receive path with core areas of 0.84mm^2 (1.17mm^2 total).

5.3 Measurement Results

5.3.1 Input balun

The transformer has a turn ratio of 2:4, providing voltage gain, proper matching and single-end to differential transformation. The inductance of the transformer secondary (6.6nH) is chosen to resonate out the gate capacitance. Furthermore, the layout of the transformer, with trace width of 8μm and spacing of 1.5μm, is optimized for both quality

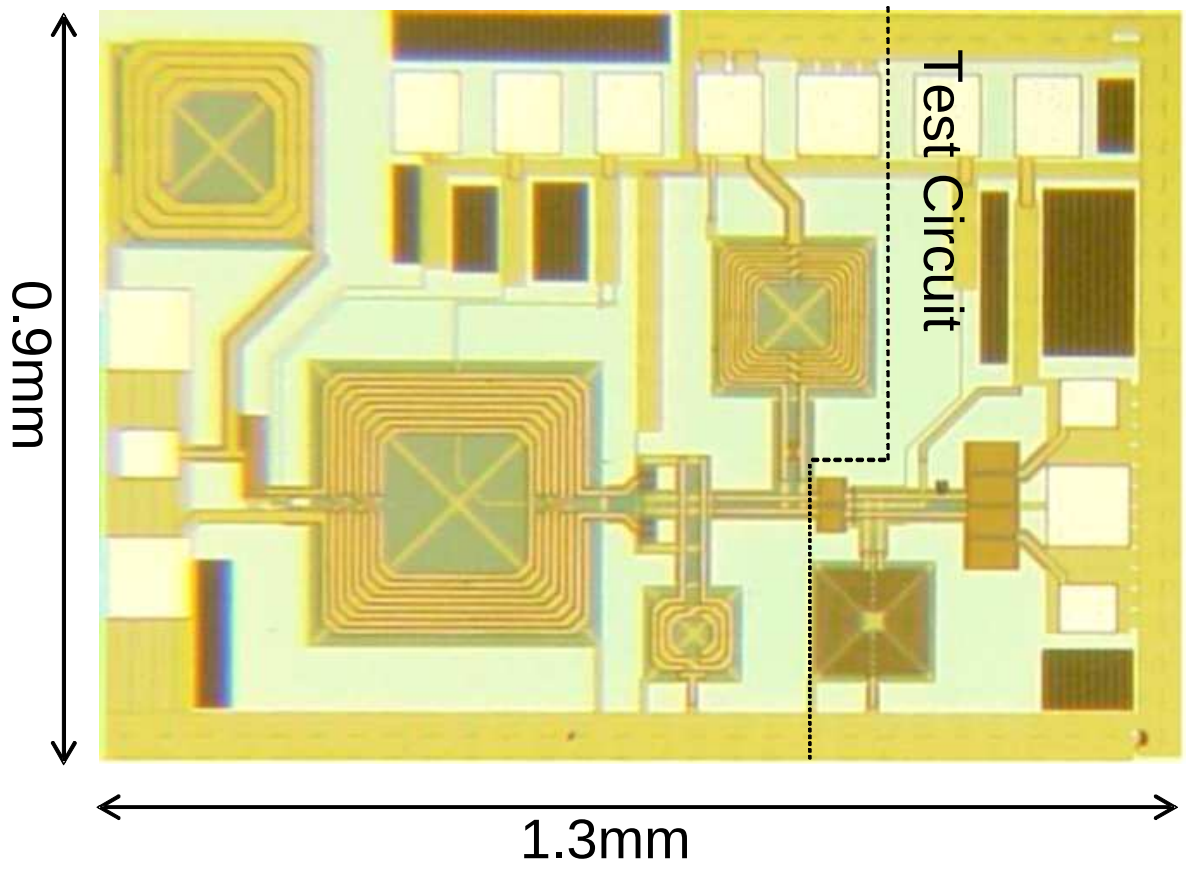


Figure 5.6: The die microphoto for the receive path.

factor Q_s and coupling coefficient k to minimize the IL, and thus the noise degradation. Figure 5.7 shows the transformer layout.

A 3-port measurement was carried out as mentioned in the previous chapter. The magnetic coupling coefficient k, is around 0.8 at low frequency and around 0.92 at 2.4GHz, the frequency of interest, as shown in Figure 5.8.

Figure 5.9(a) and (b) shows the insertion loss of the input transformer balun from the mixed mode S-parameter and from the back-to-back simulation with tuning capacitors using measured data, respectively. The results from the two methods are close, which indicates good symmetry. The insertion loss (IL) of the Rx switch and the transformer is about 2.06dB, with 0.5dB from the switch and 1.56dB from the transformer balun. This total IL is comparable to that incurred by off-chip components.

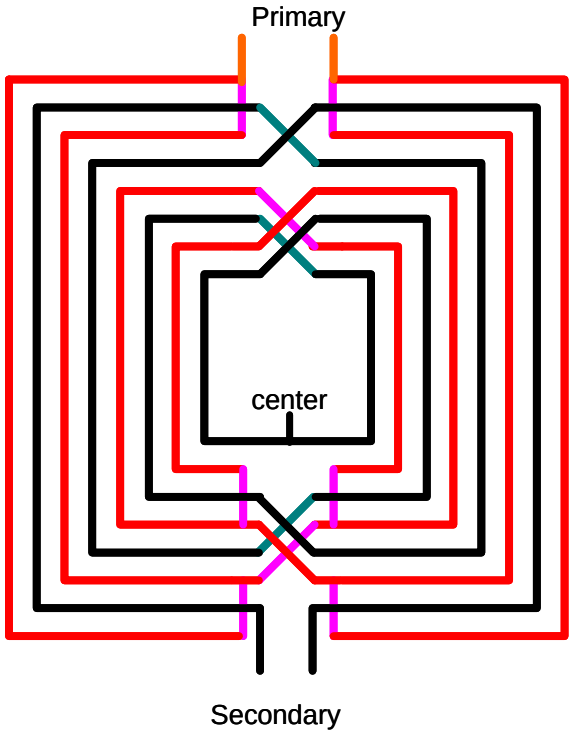


Figure 5.7: The input balun structure.

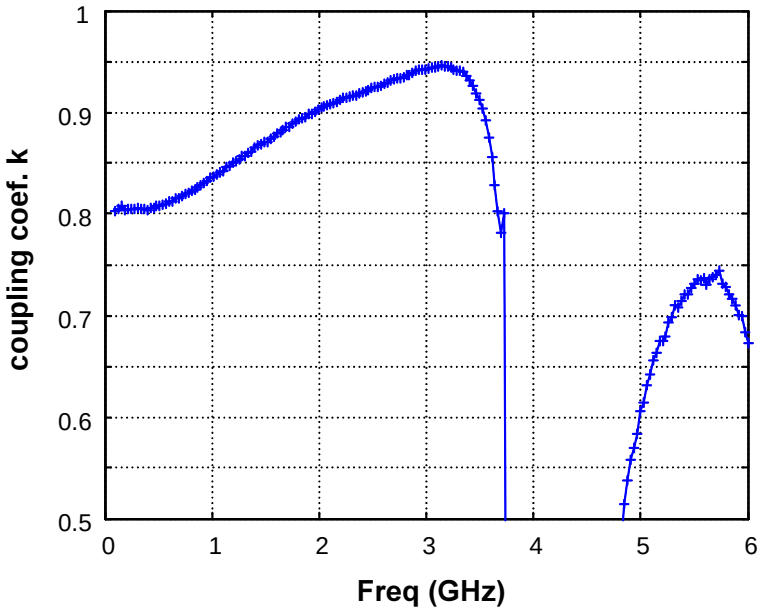


Figure 5.8: Input balun magnetic coupling coefficient k vs. frequency.

5.3.2 Receive path

The chip was bonded in a LCC40 package and then soldered on an FR4 board. The DC supply signals were provided on board. The LNA performance was measured using GSG and/or SGS probes from Cascade Microtech. As the LNA outputs are differential, an off-chip balun or a 50Ω termination was used in the measurement.

In receive mode, the measured S_{11} of the entire receive path, including the switch, the transformer and the LNA at 2.45GHz, is about -10dB, which indicates good matching (Figure 5.10). S_{21} is about 17dB at 2.45GHz. The LNA core draws 9mA from the 1.8V supply.

Figure 5.11 shows the measurement setup for the noise figure measurement. As the small signal gain of the LNA is sufficient, no preamplifier was used in the measurement. As shown in Figure 5.12(a), the measured NF for the entire receive path is 4.1dB at 2.45GHz.

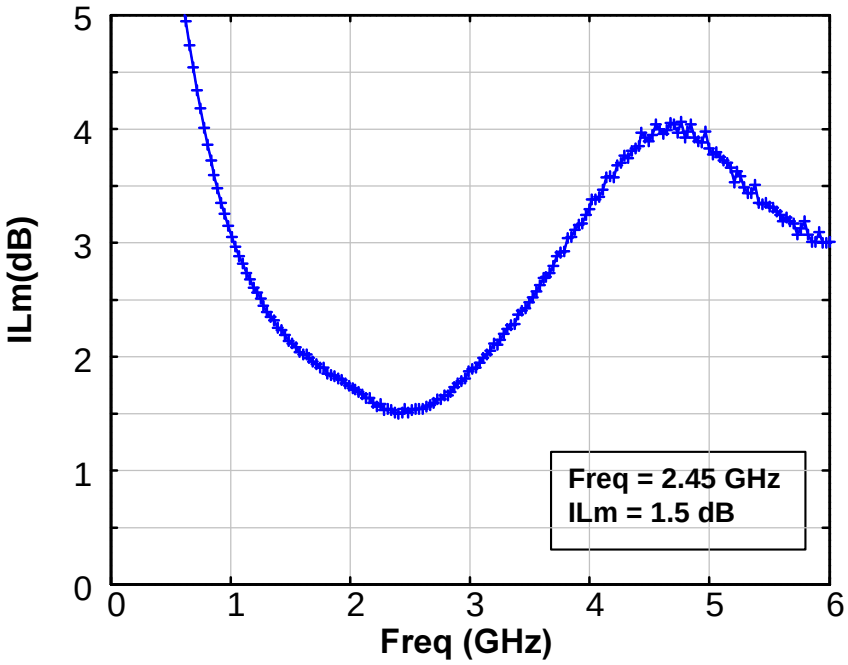
The setup for the input-referred third-order intercept point (IIP3) is similar to that mentioned in [49]. The IIP3 of the receive path is 0dBm as shown in Figure 5.12(b).

In transmit (Tx) mode, the parallel tank formed by L_1 and C_1 resonates at 2.45GHz and presents a high impedance (∼360Ω).

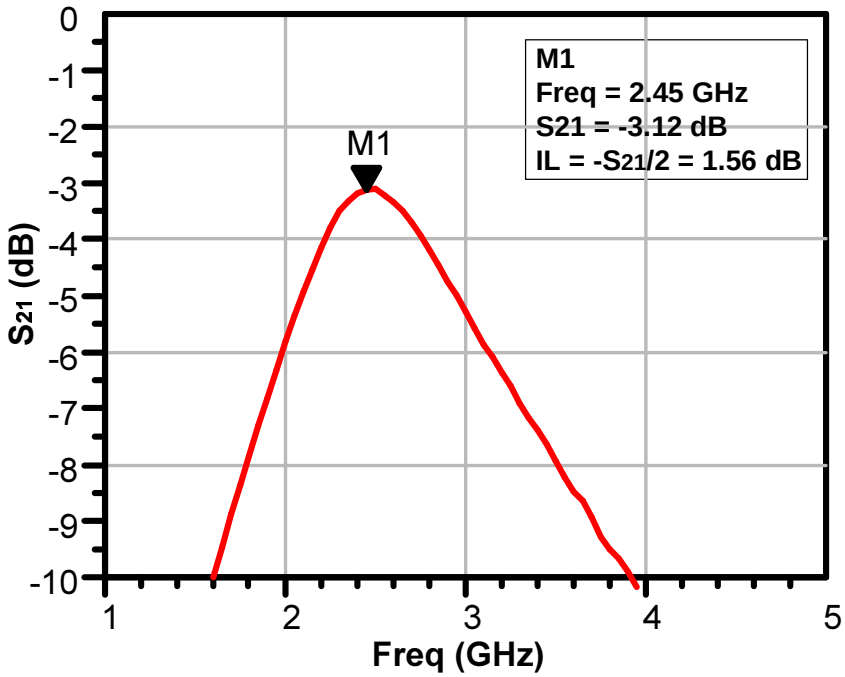
Table 5.1 shows a comparison of the simulated and measured results for the receive path. The difference in S_{21} comes mainly from the generic CMOS device model used in the simulation. A more sophisticated device model that takes substrate resistance and other effects into account would give a more accurate prediction.

LNA Spec	Rx Mode				Tx mode
	$\|S_{11}\|$ (dB)	$\|S_{21}\|$ (dB)	NF (dB)	IIP3 (dBm)	IL (dB)
Sim.	-11	20.6	3.91	–	0.54
Meas.	-9.4	16.9	4.07	0	0.60

Table 5.1: Comparison of simulated and measured results for the receive path.



(a)



(b)

Figure 5.9: Input balun insertion loss (a) from mixed mode S_{mm} and Eqn. (2.28) and (b) from back-to-back simulation with single-ended S_{se} and tuning capacitances.

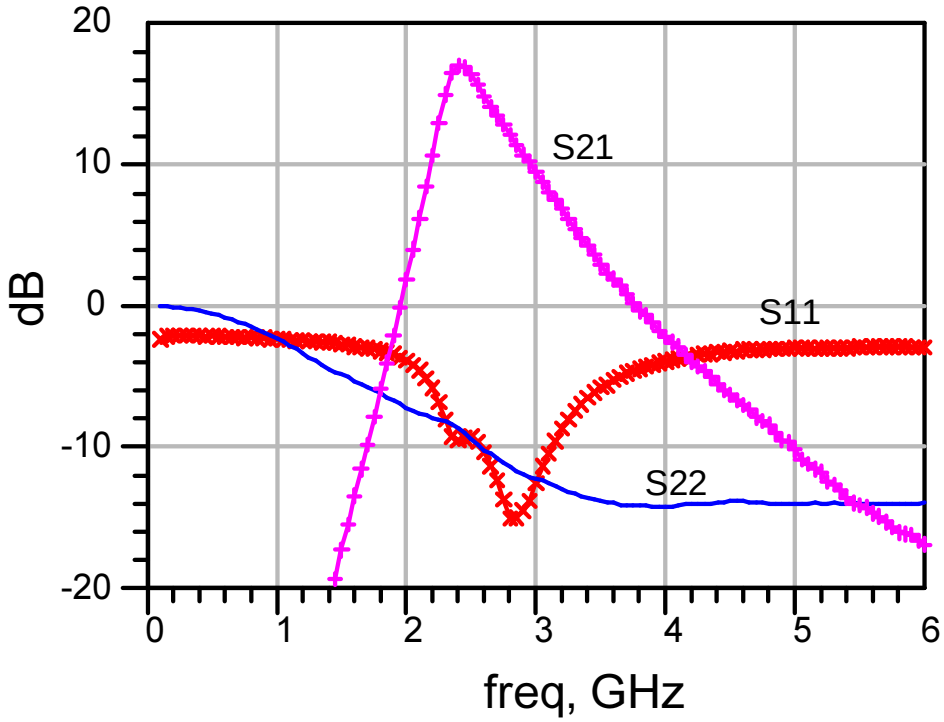


Figure 5.10: S-parameter of receive path in receive mode.

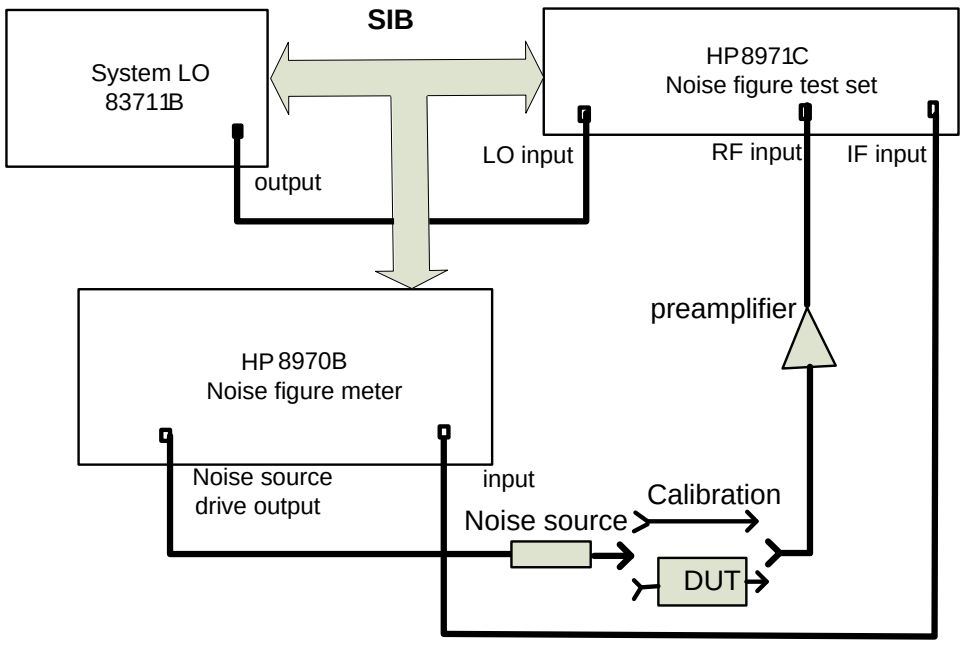
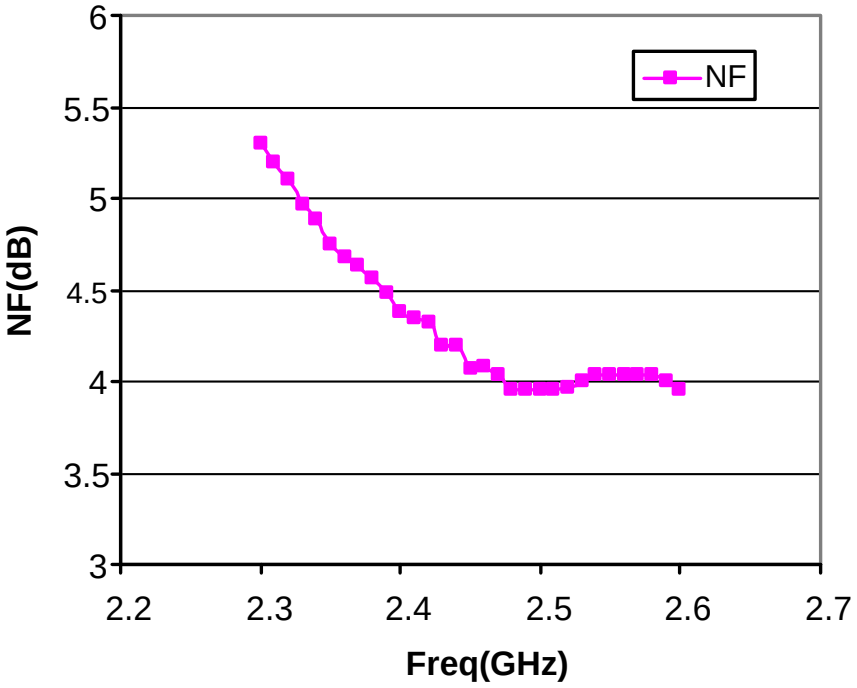
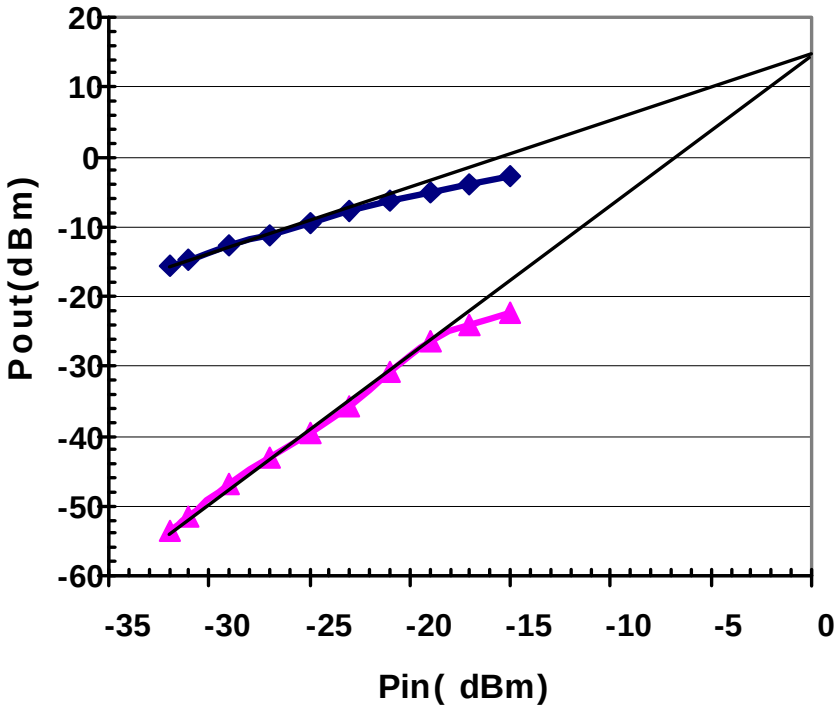


Figure 5.11: Noise figure measurement setup.



(a)



(b)

Figure 5.12: The receive path (a) Noise figure and (b) IIP3 at 2.45GHz.

5.4 Fully Integrated Front-end

The receive path discussed in this chapter and the PA discussed in the previous chapter enables a fully integrated front-end with on-chip transformers individually optimized for the LNA and the PA, and targeted for medium power applications, e.g., WLAN. Figure 5.13 shows the architecture. The transmit (Tx) switch has been described elsewhere [8] . With single antenna pin output and transformer matching, the electrostatic discharge (ESD) requirements are relaxed.

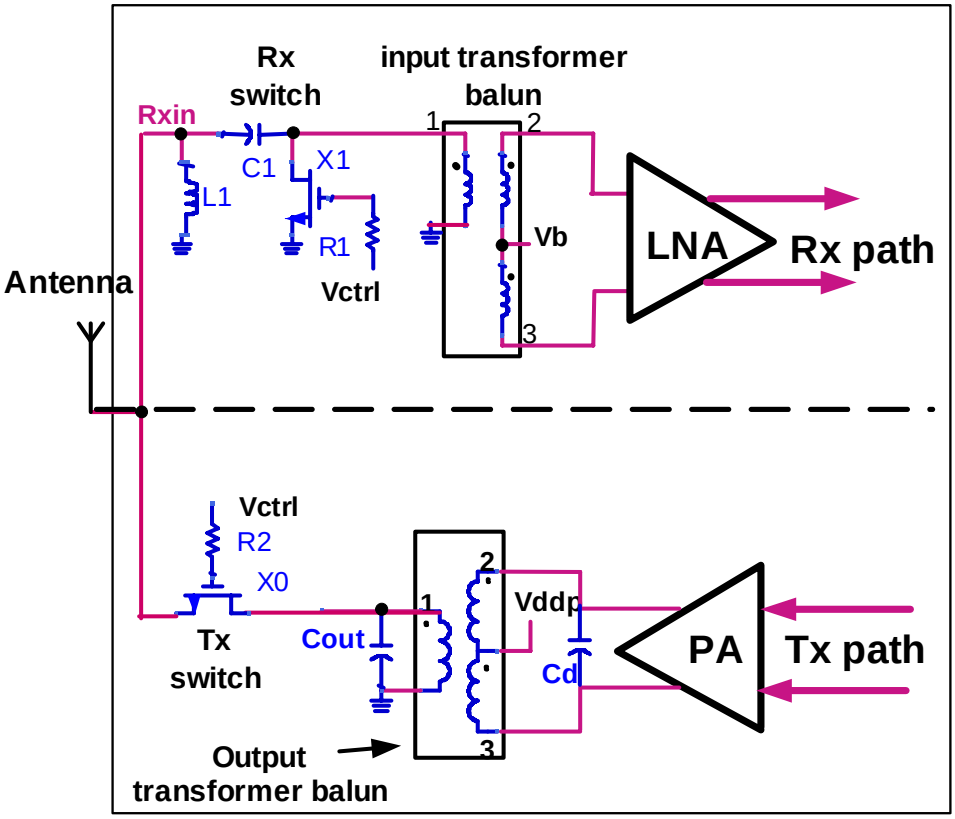


Figure 5.13: The fully-integrated front-end architecture.

5.5 Summary

LNA topologies and input matching schemes were reviewed. Implemented in a standard digital 0.18μm CMOS process, the receive path including a switch, an input transformer

and a differential LNA, achieves 17dB S_{21}, 4.1dB NF, and 0dBm IIP3 at 2.45GHz. With the fully integrated PA discussed in the previous chapter, it enables a fully integrated RF front-end architecture for medium power WLAN application. The IL of the Rx switch and the transformer is about 2.06dB, with 0.5dB from the switch and 1.56dB from the transformer balun. This total IL is comparable to that incurred by off-chip components. The higher integration eliminates off-chip component and potentially cut cost.

Chapter 6

Conclusions

This research has focused on the fully integrated RF front-end to eliminate off-chip components. To achieve this goal, the transmit/receive switch, output and input transformer baluns and other necessary matching networks are all implemented on-chip. This chapter first summarizes this work and then points out possible directions for future work.

6.1 Summary

Chapter 2 examines various transformer structures and various loss mechanisms. A broadband transformer analytical model is developed, which can be easily incorporated into a standard circuit design environment (such as Spectre or SPICE). The model also enables fast optimization of minimum insertion loss.

Various transformer structures have been fabricated at Stanford Nanofabrication Facility. In Chapter 3, the measured results of test structures are compared to the HFSS simulation results and the broadband model results. The model is accurate up to at least 4GHz. A novel layout scheme of segmenting and interleaving wide metal traces is also proposed in Chapter 3. Verified by measurement results, the layout scheme improves the magnetic coupling coefficient from 0.55 to over 0.8 and lowers the minimum insertion loss to 1.0dB.

Chapter 4 discusses the design of output transformer baluns. Using the segmenting and interleaving scheme described in the previous chapter, two output baluns are designed and compared. Other practical issues, such as area and amplitude and phase imbalances in a 3-port configuration, are also discussed. Fabricated in a five metal (Al) 0.18μm digital CMOS process, the output transformer balun has an insertion loss of 1.95dB with capacitive tuning. A one stage class AB push-pull power amplifier utilizing the output transformer balun achieves a P_{sat} of 21dBm, a P_{1dB} of 17dBm, and a maximum PAE of 21% fully on-chip.

In Chapter 5, a symmetric step-up transformer with a turn ratio of 2 is implemented as the input balun. The receive path is comprised of a receive switch, the transformer input balun, and an inductively source degenerated common source LNA. The insertion loss of the switch and the transformer is about 2.06dB, with 0.5dB from the switch and 1.56dB from the transformer. The receive path achieves an S_{21} of 17dB, an NF of 4.1dB and an IIP3 of 0dBm at 2.45GHz.

The receive path and the PA with a transmit switch enable a fully integrated front-end with a single pin to the antenna for 2.4GHz wireless LAN applications with 20dBm output power. The on-chip transformer balun and matching network provides similar or less loss than board components.

6.2 Future Work

6.2.1 Broadband transformer model

As discussed in Chapter 2, the broadband transformer model is only valid for a limited frequency range because of the vertical skin effect. The vertical skin effect is not significant for Al metal thicknesses up to 2μm in the GHz range. However, to reduce the ohmic resistance, thicker metal and/or low resistivity metal, such as copper, is becoming common in advanced technologies. To model transformer structures with these technology parameters will require more parallel branches in the ladder circuit [50] as shown in

Figure 6.1.

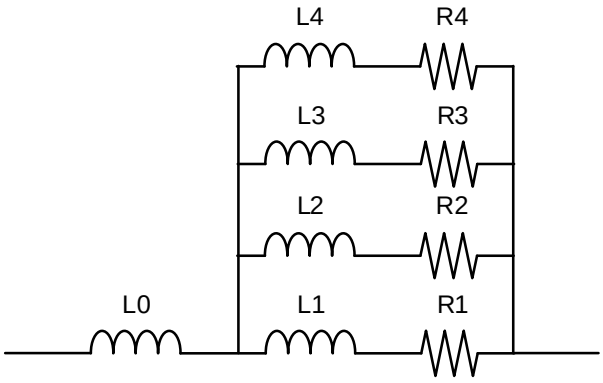


Figure 6.1: Ladder-circuit configuration for modeling skin and proximity effects.

6.2.2 MOSFET modeling at RF

Some measured results of the receive path and the PA are not in good agreement with simulation predictions. For the PA, large signal MOSFET modeling is needed. The measured gains of the LNA and PA circuits are smaller than predicted. This is mainly attributable to the substrate impedance network and other parasitic effects that are not included in the existing BSIM3v3 model. Accurate MOSFET model at RF will enable better prediction of the simulation of all blocks in the transceiver design.

6.2.3 Differential antenna

Although differential circuits have many design benefits compared to single-ended circuits, the antenna for mobile systems today is typically single-ended. Most of the measurement equipments, such as network analyzers and spectrum analyzers, are also single-ended. Thus a balun is needed to convert differential signals to a single-end signal. Even though work has shown that it is possible to integrate the balun on-chip, it costs area and performance loss (i.e. insertion loss). Therefore, it is desirable to remove the baluns altogether.

One way to eliminate the baluns is to use a differential antenna, as shown in Figure 6.2. An effective differential transmit/receive (T/R) switch needs to be developed.

To implement a differential antenna, a dipole structure can be used. Kuo [51] demonstrated that the performance of a differential antenna with a push-pull differential PA was better than that of a single-ended solution with a balun on board.

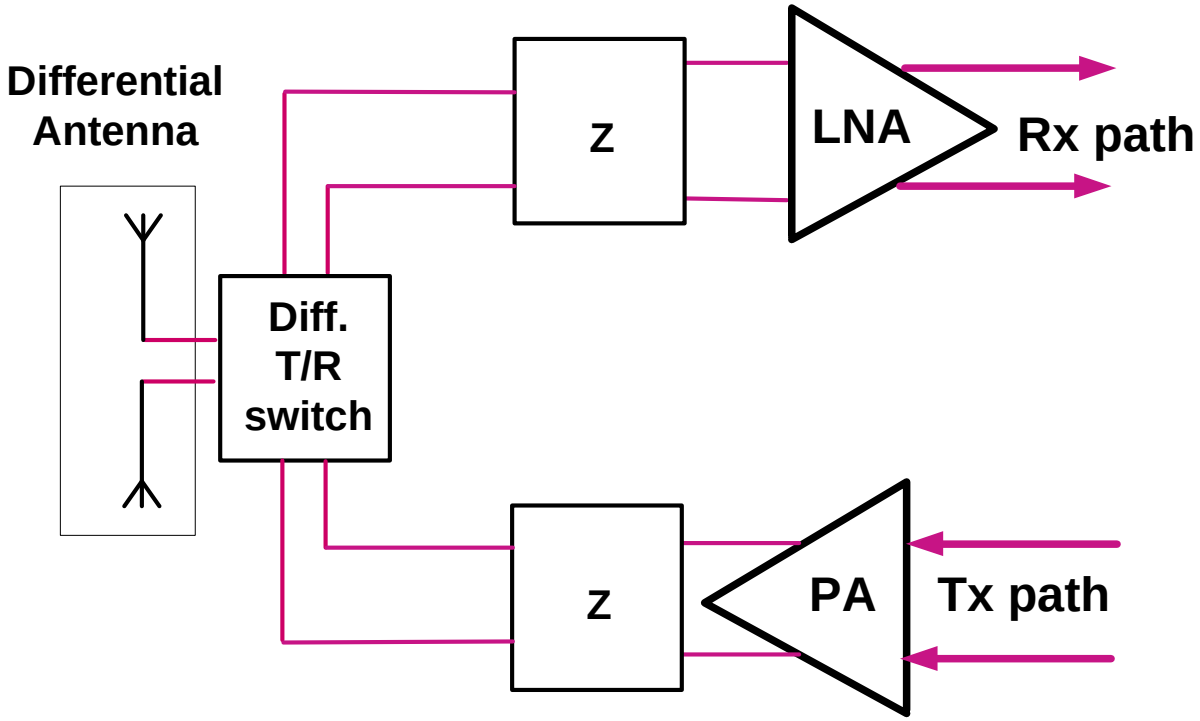


Figure 6.2: Front-end with differential antenna.

6.2.4 Matching load

With the scaling of the submicron CMOS technology, the supply voltage of core devices is approaching 1V or even lower. To keep the output power level around 100mW with the antenna/load impedance remaining at 50Ω, impedance transformation is needed under a low supply voltage. Fortunately, we can use the I/O device, which has a higher breakdown voltage, to extend the supply voltage and reduce the burden of impedance matching.

From a system design perspective, it is not necessary that the characteristic impedance for antenna be 50Ω. The impedance matching networks shown in Figure 6.2, and hence

the insertion loss associated with the matching networks, can be minimized by careful system/circuit co-design in which the antenna presents a proper impedance to the PA and the LNA.

Appendix A

Derivation of the Lateral Proximity Effect

As shown in Chapter 2, the total proximity effect has three components. The external magnetic field B_{ext} is first discussed in A.1. Then the eddy current due to the external magnetic field from the remaining metal traces of the same inductor is presented in A.2. The eddy current loss due to the impressed current in the metal trace is discussed in A.3. The eddy current loss due to the external magnetic field from the other inductor of the transformer is discussed in A.4. Finally, all three components are combined and the expression for total proximity effect is presented in A.5.

A.1 External Magnetic Field B_{ext}

Although the magnetic field distribution is complex and varies nonlinearly around the trace edges, it is possible to approximately expressed the magnetic field as

$$B_{ext}(\mathbf{r}) = G(\mathbf{r})I \tag{A.1}$$

where $G(\mathbf{r})$ is a function of the geometry parameters and I is the impressed current. Kuhn [52] provided an empirical expression of the magnetic field in turn n as

$$B(n) \approx 0.65\frac{\mu_0}{P}\frac{n-M}{N-M}\cdot I \tag{A.2}$$

where μ_0 is the permeability in free space, $P = W + s$ is the turn pitch, N is the total number of turns, $M \approx N/4$. A more involved expression can be found in [53], which average the B field in the middle of the nth turn and in one vertex.

A.2 Eddy Current Loss due to B_{ext}

Consider the simple mesh in Figure 2.11, the total magnetic field at point P can be expressed as

$$B(P) = G(P)I - \frac{4\mu_0\Delta I}{\pi W}\frac{1+q}{(1-q)(1+3q)} \tag{A.3}$$

where W is the trace width, $q = W_i/W$, and ΔI is the magnetically induced current. From Faraday's law, the induced electric field is

$$E \approx -j\omega Bx \quad \text{for} \quad -W_e/2 \le x \le W_e/2 \tag{A.4}$$

Using the Ohm's law,

$$\Delta I = \int_{-W_e/2}^{W_e/2} t\cdot\sigma\cdot E\cdot dx = \frac{j\pi f(1-q)^2W^2}{8R_{sh}}B \tag{A.5}$$

where R_{sh} is the sheet resistance of the metal. Substitute (A.3) to (A.5), and solve for ΔI as a function of I

$$\Delta I = \frac{K\Lambda + j\Lambda}{1+K^2}I \tag{A.6}$$

where

$$K = \frac{\mu_0 W}{2R_s}\frac{1-q^2}{1+3q}f \tag{A.7}$$

$$\Lambda = \frac{(1-q)^2 W^2 G\pi}{8R_{sh}} f \tag{A.8}$$

The power loss and corresponding resistance R_{ext} due to the eddy current can be calculated as

$$P_{loss} = 2\frac{R_{sh}}{W_e}|\Delta I|^2 = C_1 \cdot R_{dc}\frac{(f/f_0)^2}{1+(f/f_0)^2}|I|^2 \tag{A.9}$$

So,

$$R_{ext} = \frac{P_{loss}}{|I|^2} = C_1 \cdot R_{dc}\frac{(f/f_0)^2}{1+(f/f_0)^2} \tag{A.10}$$

where

$$f_0 = \frac{2R_{sh}}{\mu_0 W}\frac{1+3q}{1-q^2} \tag{A.11}$$

$$C_1 = 4(1-q)\left(\frac{(1+3q)GW\pi}{4\mu_0(1+q)}\right)^2 \tag{A.12}$$

We can see that C_1 is a geometry and technology dependant coefficient. The mesh factor q can set to 0.5 for GHz operating frequencies.

A.3 Eddy Current Loss due to Impressed Current

The similar procedure can be applied for the computation of the eddy current due to an impressed current. The total magnetic field at point P can be expressed as

$$B(P) = \frac{\mu_0}{\pi W q} I - \frac{2\mu_0 \Delta I}{\pi W}\frac{(1+q)^2}{q(1-q)(1+3q)} \tag{A.13}$$

The power loss can be calculated as

$$P_{loss} = \sum_{i=1}^{3} R_i |I_i|^2 = R_{dc}(1 + C_2\frac{(f/f_0)^2}{1+(f/f_0)^2})|I|^2 \tag{A.14}$$

$$R_{impcurr} = \frac{P_{loss}}{|I|^2} = R_{dc}(1 + C_2\frac{(f/f_0)^2}{1+(f/f_0)^2}) \tag{A.15}$$

where

$$C_2 \approx \frac{q}{4(1+q)^2} \tag{A.16}$$

A.4 Eddy Current Loss due to B_{ext} from the Other Inductor

Even when the terminals of the inductor have no current, the B_{ext} generated by the current flowing in the other inductors of the transformer induces the eddy current loops in the traces and adds extra loss. The procedure to compute the extra resistance in this situation is very similar to that described in A.2.

A.5 Total Loss due to Proximity Effect

Combining all three losses due to proximity effect together, we can get the total resistance as

$$R_{total\_p} = R_{dc}\left(1 + r_{rf}\frac{(f/f_0)^2}{1+(f/f_0)^2}\right) \tag{A.17}$$

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