Broadband Nonreciprocal Phase Shifter Design Technique

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***Abstract*— In this contribution, a novel method to design broadband nonreciprocal phase shifters (NRPS) is illustrated: this new topology is based on the combination of two directive-distributed amplifiers with a four-port phase-shifting network. The presented approach includes explicit design formulae allowing for arbitrary differential-phase implementation. Extensive design description of a 180° NRPS, acting as broadband differential-phase inverter, is also provided. The 3.5 × 3.4 mm^2 demonstrator, realized in 0.5 μm GaN HEMT technology, has an average zero insertion loss up to 25 dBm of input power, 180° ± 2° differential-phase shift, and good port matching over the 3–7-GHz operating bandwidth.**

***Index Terms*— Broadband, circulator, distributed amplifier, GaN, microwave monolithic integrated circuit (MMIC), phase shifter.**

I. Introduction

GALLIUM arsenide has been historically used for several-integrated circuit (IC) applications in the microwave and millimeter-wave domain. Examples include high-power and low-noise amplifiers, oscillators and mixers, and signal-routing and signal-conditioning circuits; recently, GaAs logic families for mixed-signal microwave monolithic IC (MMIC) have presented too. The maturity of this technology process permits to get reliable and precise models, which provide good agreement between simulations and measurements. Thanks to its versatility GaAs represents, in most cases, the best choice for a high-volume and cost-effective MMICs production; however, when extreme robustness or high linearity is requested, different technologies have to be selected.

GaN technology, first appeared in the 90s, soon exhibited its superiority in terms of high-power handling [1] to the high electronic bandgap, new system capabilities were achieved in a number of different fields such as RADAR, measurements instrumentation, space communications, and electronic warfare. Nevertheless, the growing system complexity for the above-mentioned applications [2], [3], a challenging roadmap for GaN technology evolution. In order to save cost and area occupation, IC downsizing is becoming more and more crucial: the introduction of multifunctional ICs, capable of implementing different functionalities, allows reducing chipset complexity and minimizing unwanted connections and hybrid circuitry. Another aspect, following the integration, is the best agreement obtained between simulations and measurements: the design of a single MMIC makes the modeling phase an easier task compared to the case in which different chips and technologies have to be interconnected.

For these reasons, the scientific world is striving to integrate different functionalities into a single chip. There are several examples of GaN MMICs implementing high-power amplifier, low-noise amplifier (LNA), and switch circuitry as standalone entities [4]–[14], and there are also some examples of their integration [15]–[17]. Unfortunately, the lack in signal routing and conditioning circuitry realized with this technology has prevented for a long time a higher grade of integration: GaAs, CMOS, and other cheaper technologies cannot be easily interfaced with GaN circuits as a consequence of the inherent mismatch in power levels. Such low-bandgap technologies cannot handle signals coming from GaN ICs because breakdown voltages, or maximum current limits are easily reached. Therefore, the realization of signal-conditioning circuits in GaN technology could represent the real breakthrough toward system integration and costs reduction.

Among all the signal-routing circuits, a particularly useful functionality consists in circulators, especially for those systems in which a full-duplex link is necessary. Circulators are used essentially in communication, RADAR, and measurement systems. The first—and probably still the most used—type of circulators was based on passive structures exploiting ferrite materials. This approach leads to cumbersome, scantly integrable, narrowband devices, and requiring an often-inconvenient magnetic bias [18]–[23]. A very interesting improvement could be represented by active circulators. In this case, there are a dc power consumption and a lower power handling as drawbacks, compared to the ferrite-based solution, but a better performance in terms of integration level and frequency bandwidth is expected thanks to intrinsic technology advantages (it is possible to use the same technology for different functionalities) and dedicated design techniques.

A former active, wideband approach was based on a distributed structure exhibiting a wideband behavior (6/18 GHz) but a very low isolation between ports, key performance for

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front-end circuits [24]. A wider bandwidth circuit was proposed in [25], but also in this case the insertion loss is critical, especially if the circulator is placed before an LNA. Another distributed approach making use of distributed amplifiers connected in a ring topology exhibits a 40% bandwidth [26] with an improved insertion loss. By the connection of an active splitter and an active combiner, it is possible to implement a two-branch active quasi-circulator [27]–[29] in which the circulation of signals is guaranteed by a phase-cancellation operation. Such an operation does not exceed the 12% operating bandwidth. Another phase-cancellation approach is reported in [30], leading to an even narrower bandwidth. A 20% operating bandwidth is possible by the combination of the Wilkinson power dividers and amplifiers [31]. A 3:1 bandwidth is achievable by using slow wave directional coupler and wideband amplifiers, as reported in [32].

Another interesting architecture makes use of the combination of particular two-port subcircuits able to vary differently the phase of signals flowing in different directions through them [33], [34]. Such special circuits are called nonreciprocal phase shifters (NRPSs). By means of NRPSs, it is possible to build a three-port architecture in which, by properly summing or subtracting signals at the ports, the circulation functionality can be obtained. The reported circulators do not exceed bandwidths of 10%/15%, but this is strictly correlated with the bandwidth of the NRPSs. From this point of view, an effort was spent to widen the operating bandwidth by proposing a new NRPS architecture based on Wilkinson power dividers, classical phase shifters and amplifiers (which introduce the nonreciprocal behavior thanks to the unilaterality of active devices), achieving a 28% bandwidth [35], [36]. Such NRPS topology provided the basis for a novel circulator architecture, achieving a measured 26% operating bandwidth in hybrid technology for L-band applications; even better results were obtained in the X-band with the design of a GaAs MMIC demonstrator [37], [38], which exhibited a simulated 36% band.

With the aim of extending the operating bandwidth of the NRPSs, a new active topology [39] has been proposed, based on a distributed amplification concept. In this contribution, a complete theoretical analysis is provided together with a step-by-step circuit design flow description. The present contribution is structured as follows. In Section II, the circuit architecture is introduced. In Sections III and IV, the detailed circuit analysis and test circuit design are, respectively, presented. In Section V, the experimental results are analyzed and compared with simulations. Finally, Section VI gives the main conclusion.

II. Circuit Architecture

Ideally, an NRPS is an active two-port network able to produce two different phase delays depending on the direction of the incoming signal. The difference between these delays, namely, the phase shift, should be kept as constant as possible on a wide frequency range to enable broadband circuit operation. Furthermore, the NRPS should not affect signal amplitude, providing negligible insertion loss in both signal directions. Such a complex analog operation can only

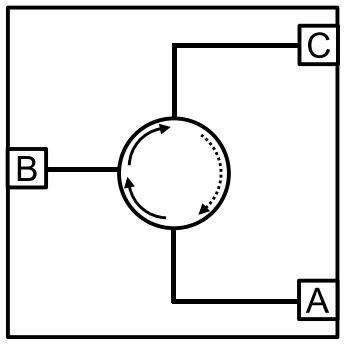

Fig. 1. Schematic representation of a quasi-circulator.

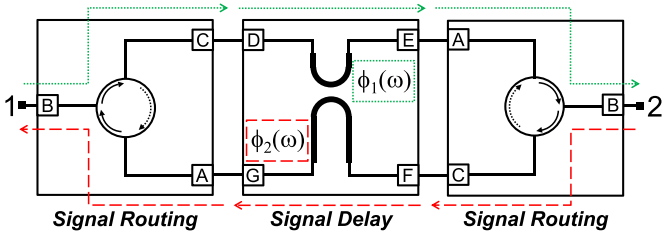

Fig. 2. NRPS block diagram.

be achieved by partitioning the process in different elementary operations which, in turn, can be addressed separately: in more detail, signal routing and signal delay functionalities are implemented by means of a quasi-circulating three-port network and a four-port filtering network, respectively.

A quasi-circulator is a three-port network that allows the signals to flow only from port A toward port B and from port C toward port A, as schematically depicted in Fig. 1.

On the other hand, the four-port filtering network consists of two separated paths, each featuring a different signal delay: obviously, by properly choosing such delays, different phase-shifting performances will be achieved.

NRPS operating principle can be easily understood by referring to the simplified block diagram proposed in Fig. 2: the signal at port 1 flows along the allowed path B-C, passing through the filtering (phase shifting) section ϕ_1 and the allowed path A–B, and finally emerges at port 2; on the other hand, a signal at port 2 flows along the allowed path B-C, passing through the filtering (phase shifting) section ϕ_2 and the allowed path A-B, and finally emerges at port 1. A signal flowing in the structure therefore undergoes different phase delays, depending on its direction: this phase difference, namely, differential-phase shift, is kept as constant as possible over the entire operating bandwidth.

In principle, every differential-phase shift can be implemented by the proper choice of the filtering section: depending on this value, different circulators or isolator architectures are possible (see Fig. 3). In more detail, connecting three NRPSs (featuring 60° each) in a delta topology, a broadband circulator is possible [33]; on the other hand, by connecting a single NRPS (featuring 180°) with a 0° delay line or two 90° delay lines, a broadband isolator or circulator are, respectively, achieved [40]; again, using a more complicated topology with two NRPSs (featuring 90° each), a 90° coupler and a 180° coupler, a broadband circulator featured by two isolated ports

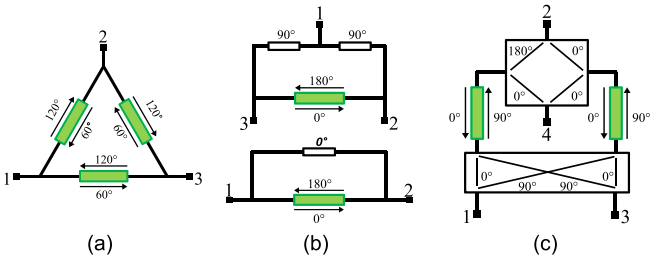

Fig. 3. Circulator and isolators achievable by means of (a) 60°, (b) 180°, and (c) 90° NRPSs.

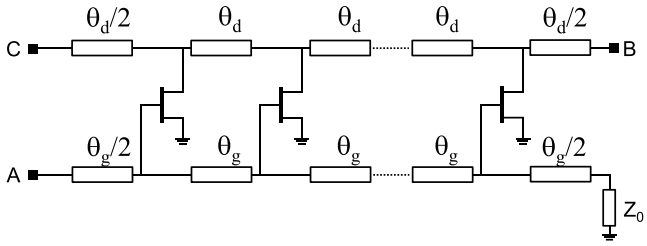

Fig. 4. Distributed amplifier as a quasi-circulator.

can be realized [41]. Furthermore, implementing a 180° NRPS, would theoretically enable the realization of a broadband microwave gyrator, providing that the insertion phase is at the same time minimized.

III. Design Method

As already stated, NRPS implementation can be successfully accomplished by addressing separately the signal routing and signal delay functionalities. In the following, two distinct sections are, respectively, dedicated to the directive-distributed amplifier and to the phase-shifting section designs.

A. Directive-Distributed Amplifier

Distributed amplifier represents a fairly old and well-known concept and is usually employed in a variety of applications where ultrabroadband performance represents a fundamental prerogative. Despite its inherent versatility, due to the presence of four ports, this topology is typically used as a single-input/-single-output network except for very rare applications like meta-distributed amplifiers [42] or quasi-circulating structures [43], [44]; in the latter case, the distributed amplifier actually behaves as an active three-port network, as shown in Fig. 4. Using the same port reference of Fig. 1, the related scattering parameter matrix should be the following:

$$S = \begin{pmatrix} S_{AA} & S_{AB} & S_{AC} \\ S_{BA} & S_{BB} & S_{BC} \\ S_{CA} & S_{CB} & S_{CC} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ G_{fwd} & 0 & 1 \\ G_{rev} & 1 & 0 \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{pmatrix}. \quad (1)$$

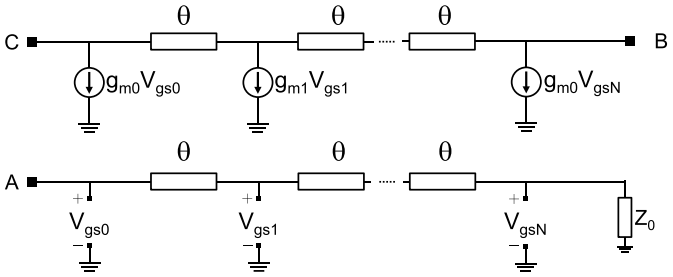

Fig. 5. Equivalent circuit of a symmetrically tapered distributed amplifier.

Looking at the matrix in (1), S_{ii} parameters (on the main diagonal) are 0 if the circuit shows perfect matching at the corresponding port; furthermore, S_{AB} and S_{AC} terms can be approximated to 0 as an effect of the intrinsic nonreciprocity of the active devices. Incidentally, it is worth pointing out that the term S_{BC} (ideally 0 in a quasi-circulator) maintains the same value of S_{CB}, because of the amplifier drain line's reciprocity; however, this is not a problem considering that C port is inaccessible in the presented topology.

On the other hand, S_{AB} and S_{AC} terms deserve a separate discussion since they must be carefully optimized by design: in particular, by tapering transconductances of the active devices, reverse gain G_{rev} can be minimized over the entire operating bandwidth while maintaining a forward gain G_{fwd} near to unity. Referring to the equivalent model of an N-cell symmetrically tapered distributed amplifier (see Fig. 5), the following expressions for the forward and reverse gains can be, respectively, obtained:

$$G_{fwd} = \left| Z_0 \sum_{i=0}^{M} g_{mi} \right|^2 \quad (2)$$

$$G_{rev} = \left| Z_0 \sum_{i=0}^{M} g_{mi} \cos[(N-2i)\theta(\omega)] \right|^2 = |Z_0 F(\omega)|^2 \quad (3)$$

where $M = N/2$ for N even and $M = (N-1)/2$ for N odd. Directivity $D(\omega)$ can be defined as the ratio between the above-mentioned gains: note that the expression in (2) is completely frequency independent, whereas array factor $F(\omega)$ in (3) depends on frequency by means of the electrical length $\theta(\omega)$. Controlling the array factor permits to obtain the desired directivity

$$D(\omega) = \frac{G_{fwd}}{G_{rev}} = \left| \frac{\sum_{i=0}^{M} g_{mi}}{F(\omega)} \right|^2 = \left| \frac{F(0)}{F(\omega)} \right|^2. \quad (4)$$

In particular, the maximum product between directivity and bandwidth can be achieved only if the array factor is designed to be a Chebyschev polynomial $T_n(x)$. Following the analysis in [18], an n-order polynomial has to be modified by a proper variable substitution which allows to restrict the ± 1 ripple within the range $[\theta_m, \pi - \theta_m]$:

$$x = \frac{\cos(\theta(\omega))}{\cos(\theta_m)} \quad (5)$$

$$T_n\left(\frac{\cos\theta}{\cos\theta_m}\right) = 2\frac{\cos\theta}{\cos\theta_m} T_{n-1}\left(\frac{\cos\theta}{\cos\theta_m}\right) - T_{n-2}\left(\frac{\cos\theta}{\cos\theta_m}\right). \quad (6)$$

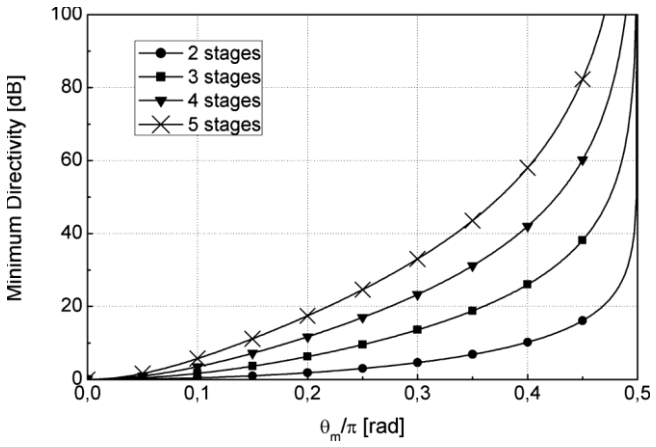

Fig. 6. Directive-distributed amplifier design chart.

The parameter θ_m is the electrical length at the beginning of the operating band and is related to the achievable fractional bandwidth by the following expression:

$$\theta_m = \frac{1}{2}\left(\pi - B\%\frac{\pi}{2}\right), \quad \text{where } B\% = 2\frac{\theta_2 - \theta_1}{\theta_2 + \theta_1}. \tag{7}$$

Now the array factor can be reformulated as

$$F(\omega) = K\left|T_n\left(\frac{\cos\theta}{\cos\theta_m}\right)\right|. \tag{8}$$

Considering last equality in (4), the K factor should be determined by imposing the desired value of forward gain

$$K = \frac{G_{\text{fwd}}}{Z_0}\left|T_n\left(\frac{1}{\cos\theta_m}\right)\right|^{-1}. \tag{9}$$

Finally, the directivity can be rewritten as follows:

$$D(\omega) = \frac{\left|T_n\left(\frac{1}{\cos\theta_m}\right)\right|}{\left|T_n\left(\frac{\cos\theta}{\cos\theta_m}\right)\right|} = \frac{D_m}{\left|T_n\left(\frac{\cos\theta}{\cos\theta_m}\right)\right|} \tag{10}$$

where D_m is the minimum directivity, i.e., the directivity at extreme electrical lengths (frequencies) θ_m and $\pi - \theta_m$ when the polynomial T_n approaches unity.

A useful design chart can be constructed by plotting, on the same graph, the minimum directivity (in log units) as a function of the parameter θ_m for different cell numbers (different polynomial orders). As can be noticed from Fig. 6, fixing a number of cells and decreasing parameter θ_m (i.e., increasing fractional bandwidth $B\%$), lower values of minimum directivity are possible; on the other hand, fixing the parameter θ_m (i.e., fixing fractional bandwidth $B\%$) and increasing the number of cells, higher values of minimum directivity can be achieved.

B. Phase-Shifting Section

The proper choice of this delay element allows for any value of differential-phase shift: in principle, any switched network topology can be exploited and rearranged to work as a four-port network featured by two isolated paths. Even limiting the attention to 180° differential-phase shift, as the most difficult to be implemented on a wide band, several

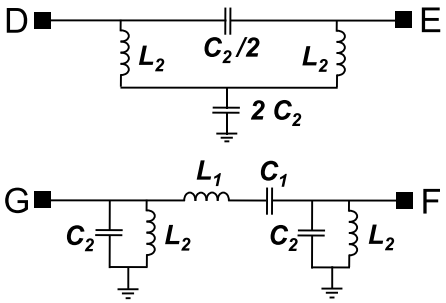

Fig. 7. Phase-shifting section schematic (APN/BPN).

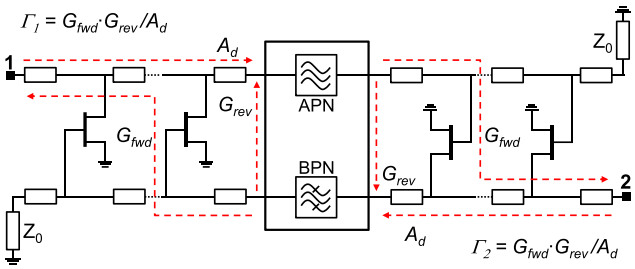

Fig. 8. Port reflection components.

distributed and lumped realization can be found: in [45], a distributed implementation is illustrated featuring pretty good phase shift and magnitude unbalance but implying an excessive amount of area occupation; in [46] and [47], two different lumped implementations are proposed, respectively, based on all-pass/all-pass network (APN/APN) and all-pass/bandpass network (APN/BPN).

The latter solution (APN/BPN), reported in Fig. 7, seems to guarantee a significantly better level of phase deviation in the bandwidth together with a circuit topology more suitable for active device biasing purposes. Circuit elements can be easily determined by means of the following formulas (where ω_0 is the center frequency and r is a dimensionless parameter setting the frequency slope of the passband response):

$$L_1 = r\frac{Z_0}{\omega_0} \quad C_1 = \frac{1}{\omega_0 r Z_0}$$
$$L_2 = \frac{Z_0}{\omega_0} \quad C_2 = \frac{1}{\omega_0 Z_0}. \tag{11}$$

IV. Test Circuit

A monolithic test circuit has been designed to verify the feasibility of the proposed topology and to evaluate its performance. Design starts fixing the number of distributed amplifier cells and associated directivity: in an ideal case of lossless and perfectly matched structure, G_{fwd} should be designed to be unity, while G_{rev} is numerically equal to the reflection coefficient Γ at both ports (see Fig. 8). Unfortunately, drain line loss A_d imposes a forward gain greater than unity which in turn worsen port reflections by the same factor, since the minimum directivity has already been chosen (see again Fig. 8).

Drain line loss A_d mainly depends on drain–source admittance G_{dsi} of the active devices, through the device size W_i, and the normalized drain–source admittance G_{dsw}. Simplifying the analysis [48] in the low-frequency approximation

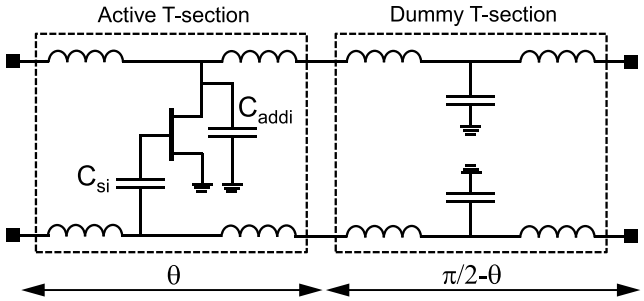

Fig. 9. Schematic of the elementary cell.

(far below line cutoff frequency), drain line loss expression becomes

$$A_d = \frac{Z_0}{2}\sum_{i=0}^{N} W_i G_{\mathrm{dsw}} = \frac{Z_0}{2} W_{\mathrm{TOT}} G_{\mathrm{dsw}}. \tag{12}$$

The choice of the actual periphery should be carried on the basis of the desired output power level (P_{TOT}), having device bias condition and relative output power density (P_W) already been determined

$$W_{\mathrm{TOT}} = \frac{P_{\mathrm{TOT}}}{P_W}. \tag{13}$$

Once the desired return losses and drain line insertion loss have been defined, a simple linear system allows setting the correct value for the forward and reverse gain (minimum directivity)

$$\begin{cases} \Gamma|_{\mathrm{dB}} = G_{\mathrm{fwd}}|_{\mathrm{dB}} + G_{\mathrm{rev}}|_{\mathrm{dB}} - A_d|_{\mathrm{dB}} \\ G_{\mathrm{fwd}}|_{\mathrm{dB}} - A_d|_{\mathrm{dB}} = 0. \end{cases} \tag{14}$$

Solving the linear set of equations (14), the required value of minimum directivity can be determined

$$D_m|_{\mathrm{dB}} = \Gamma|_{\mathrm{dB}} + A_d|_{\mathrm{dB}}. \tag{15}$$

The broadband NRPS has been designed using the 0.5-μm GaN/SiC HEMT process developed by SELEX ES (now Leonardo S.p.A.), featuring $I_{\mathrm{DSS}} = 600$ mA/mm at $V_{\mathrm{DD}} = 25$ V. The target design covers more than one octave, i.e., 3-7 GHz, with a saturated output power (P_{TOT}) of at least 30 dBm. Analyzing the device bias condition ($V_{\mathrm{DD}} = 25$ V and $I_D = 50\%\ I_{\mathrm{DSS}}$) lets the output power density and the normalized drain–source admittance to be assessed: considering 15% of drain efficiency (realistic for a distributed topology), a P_W of 1.12 W/mm is inferred; on the other hand, S-parameter measurements of FET devices suggest 13 mS/mm to be a consistent value for G_{dsw}. From (13), W_{TOT} results to be around 900 μm which, substituted into (12) gives an A_d approximately equal to -3 dB. Considering expression in (15) and imposing a return loss of 12 dB, a D_m of 15 dB is mandatory.

Looking at the design chart in Fig. 6 and applying (7), minimum directivity should be achieved for $\theta_m/\pi = 0.3$: desired value can be met by means of three cells. Total active periphery can be thus partitioned into three active devices featured by 4×75 μm periphery each. Applying a second-order polynomial, as reported in (6), the following expressions for the normalized transconductances can be derived:

$$\bar{g}_{m0} = \bar{g}_{m2} = \left(\frac{1}{\cos(\theta_m)}\right)^2 \quad \bar{g}_{m1} = \left(\frac{1}{\cos(\theta_m)}\right)^2 - 1. \tag{16}$$

Furthermore, substituting the second of (14) into (9) allows calculating K coefficient which, substituted in (8), returns the array factor (i.e., actual transconductance values)

$$F(\omega) = 16 + 24\cos(2\theta) \tag{17}$$

where $g_{m0} = g_{m2} = 24$ mS and $g_{m1} = 16$ mS. Now, these values have to be implemented by inserting a proper capacitance in series to the FET gate, whose expression, being g_{mw} the normalized transconductance and C_{gsi} the ith intrinsic gate capacitance, would be

$$C_{\mathrm{si}} = \frac{G_{\mathrm{dsw}}}{g_{\mathrm{mw}} - G_{\mathrm{dsw}}} C_{\mathrm{gsi}}. \tag{18}$$

Another capacitance should be placed in parallel to the drain node, in order to equalize gate and drain lines phase velocity, according to the following expression:

$$C_{\mathrm{addi}} = \frac{G_{\mathrm{gsi}} G_{\mathrm{si}}}{G_{\mathrm{gsi}} + G_{\mathrm{si}}} - C_{\mathrm{dsi}}. \tag{19}$$

Finally, for amplifier proper operation, it is mandatory to set 90° as the electrical length of the elementary cell (see Fig. 9) at center frequency, that is, the maximum phase shift achievable by a single T-section made up of lumped elements [49]. To improve amplifier frequency response, three elementary cells, made up by an active T-section (including the active device) and a dummy T-section (including capacitance), were employed.

Last step in MMIC design is the definition of the APN/BPN phase-shifting section: applying formulae in (11) for $f_0 = 5$ GHz and $r = 1.45$ (for best broadband performance [47]), the values of circuit elements are easily obtained (see Table I).

TABLE I
CIRCUIT ELEMENTS OF PHASE-SHIFTING SECTION

Element	VALUE
L_1	2.52 nH
C_1	0.48 pF
L_2	1.74 nH
C_2	0.69 pF

The photograph of the designed broadband NRPS is presented in Fig. 10. Chip size is 3.5×3.4 mm^2. As effect of g_{mi} modulation, achieved by series capacitors insertion, the use of bypass resistances becomes necessary for biasing FETs. According to (19), drain additive capacitances C_{addi} resulted to be so small that they were omitted, and phase velocities were equalized by simply tuning the inductor values.

Looking at Fig. 10, port 1 and port 2 are visible in the upper left and right borders, respectively. Bias pads are placed on the upper and lower sides of the MMIC. The four-port phase-shifting network can be seen between the two distributed

TABLE II
COMPARISON OF REPORTED NRPSs

Reference	PHASE-DIFFERENCE [DEG]	Frequency [GHz]	Typical Insertion Loss [dB]	Power handling [W]	Technology	Year
[34]	60	7.0-13	3	1	MMIC	1989
[35]	60	1.7-1.9	7	0.2	HMIC	2007
[38]	90	1.3-1.6	2		HMIC	2012
[19]	70	2.4-2.4		10^4	Ferrite	2006
[50]	300	30-50	1.3		Ferrite	2012
[51]	400	12-14	20	10^2	Ferrite	2013
This work	180	3.0-7.0	1	1	MMIC	2017

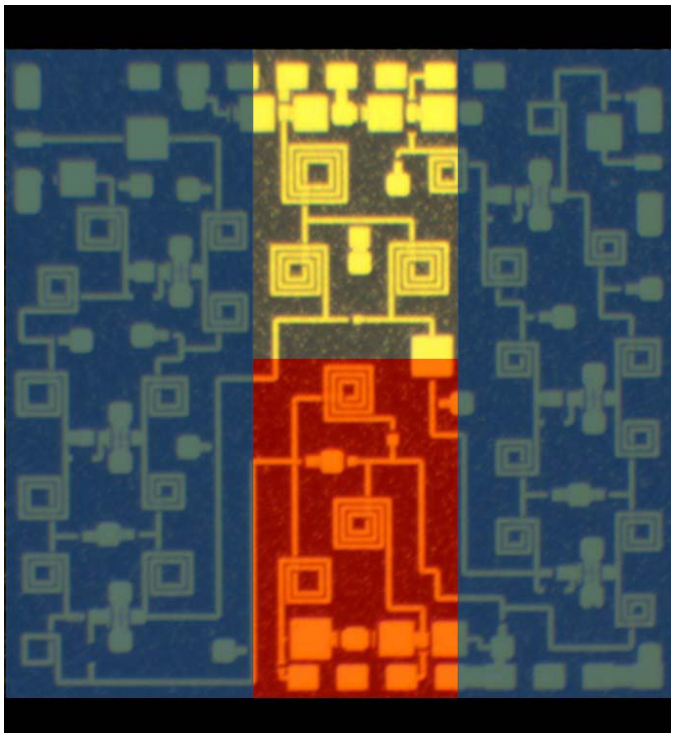

Fig. 10. Photograph of the fabricated MMIC.

amplifiers: the APN and the BPF are on the upper and lower sides, respectively. The classical APN structure was modified to bias the drain of the left distributed amplifier; the BPF circuit topology on the contrary was exploited in order to bias the gate of the left distributed amplifier and the drain of the other one. The remaining gate of the right distributed amplifier was biased by the termination resistor directly connected to the bias pad.

V. EXPERIMENTAL RESULTS

The presented MMIC was successfully tested by means of linear S-parameter and gain compression measurements, proving the effectiveness of the approach. As an effect of the design algorithm proposed in Section IV, both port matchings are below the desired level of 12 dB, except for a small portion of the band between 4 and 5 GHz (see Fig. 11); furthermore, a pretty good accordance between simulation and measurements can be noted.

The same accordance between simulated and experimental data can be appreciated about the insertion gain, roughly equal to 0 dB all over the operating band (see Fig. 12).

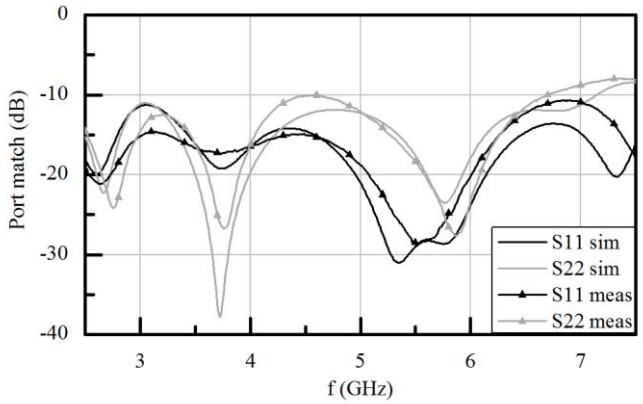

Fig. 11. Port matching.

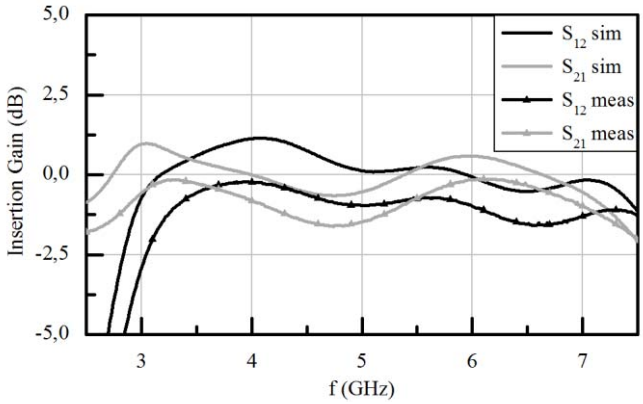

Fig. 12. Insertion gain.

The most important figure of merit, i.e., the differential-phase shift between the two ways, is reported in Fig. 13. The proposed topology provides an almost perfect phase inversion between signals traveling in opposite directions: 180° differential-phase shift with negligible errors as small as 2°, except for the really low portion of the band, again in good accordance with predictions.

Finally, large-signal measurements of insertion gain show a $P_{\text{out,1 dBc}}$ around 25 dBm, with a saturated output power in line with the required level of 30 dBm (see Fig. 14). Unfortunately, the absence of a nonlinear model for the concerned FET periphery does not allow for an accurate measurement versus simulation comparison.

A comparative table illustrates the differences among the present work and other NRPS implementation both as stand-alone topologies or as a part of isolator/circulator circuits

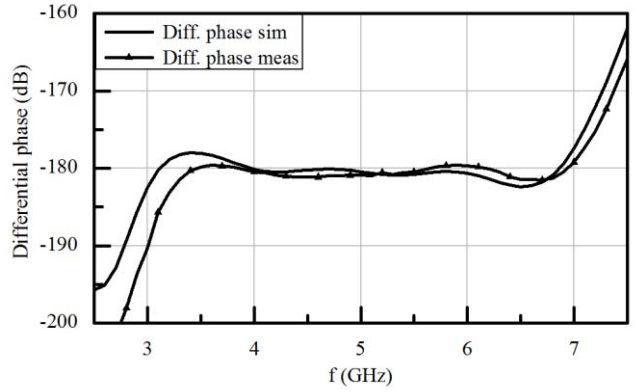

Fig. 13. Differential-phase shift.

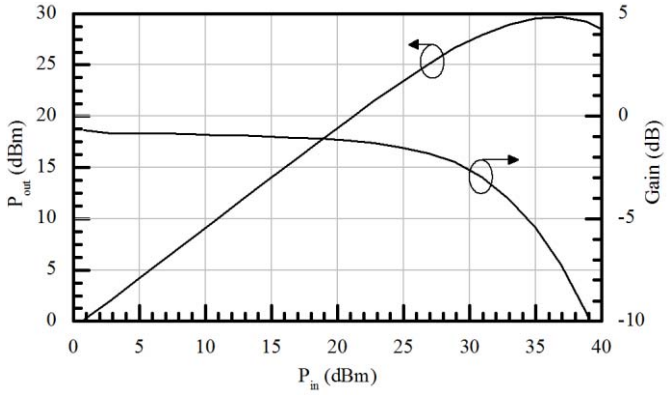

Fig. 14. Power and gain compression at center frequency (5 GHz).

(see Table II). Different implementations, herein considered, span across several technological domains from MMIC/HMIC to ferrite circuits. As can be noticed, this paper exhibits the best tradeoff between bandwidth and insertion loss; power-handling capability is definitely lower with respect to the ferromagnetic solutions which, in turn, are less suitable for integration and need to be provided with cumbersome magnetic bias circuitry.

VI. Conclusion

A novel technique for the realization of broadband NRPSs has been proposed: the design approach is based on the integration of directive-distributed amplifiers, employed as quasi-circulators, and a four-port filtering network as a signal delay element. A complete description of the circuit synthesis algorithm has been provided and accompanied with explicit design formulae and a design chart.

A monolithic test circuit in the 3–7-GHz band has been designed and measured to validate the effectiveness of the method: a 180° NRPS, acting as broadband differential-phase inverter, has been selected as the most challenging phase shift value to be implemented. The realized GaN MMIC features a quite compact layout (3.5×3.4 mm^2) and achieves the target 180° with a typical error of ±2°, showing an insertion loss of about 1 dB, a port matching better than 10 dB, and a saturated output power near to 1 W.

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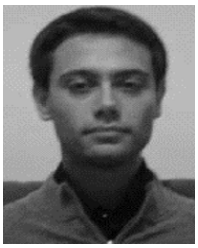

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