Architecture and Design of a New Non-Quadrature Vector-Sum Microwave Phase Shifter at 10 GHz With Maximum Residual Phase Error of 1.80°

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2023 International Conference on Electrical, Computer and Communication Engineering (ECCE) | 979-8-3503-4536-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/ECCE57851.2023.10101495

***Abstract*—This paper presents the architecture, design, and simulation of a new vector-sum phase shifter for prospected use in applications that require low amplitude loss. The architecture is based on non-quadrature phase generation and synthesis. The phase generation is done by splitting the input signal into two equal-phase output vectors and delaying one signal vector to the other; while the phase synthesis is implemented by subjecting the vectors through path selection and variable amplification & attenuation before subtracting the different paths. A two-bit phase path selection was employed for achieving 360° of coarse & fine tuning. EM simulations of the phase shifter architecture was carried out using RT-Duroid 5880 specifications (ε_r = 2.2, tanδ = 0.004) at center frequency of 10 GHz. A maximum phase error of 1.82° was obtained for the entire interval of 360 degrees of phase shift. With less than 2° of phase error, the proposed phase shifter architecture is feasible for millimeter-wave phase array beamforming applications; as it offers the possibility of lower power consumption with the use of lesser compartmental blocks (i.e. compared to a T-bridge phase shifter which uses a chain of multiple blocks that can lead to excessive losses of more than 30 dB).**

***Index Terms*—phase shifter, vector-sum phase shifter, digital phase shifter, analog phase shifter, vector synthesizer, phase path selector, vector subtractor, beamformers, phased-array, phased-array systems.**

I. Introduction

Broadband satellite communication systems require extensive use of phased-array beamformers (PABs). Beamformers are employed to adjust the gain and the beam angle of the transmitted and received signals. Phase shifters are essential elements of PABs as they control the phase information of the signal. Passive phase shifters such as the switch-type phase shifters (STPS) [1] - [5] and reflection-type phase shifters (RTPS) [6] - [12] consume either low or no power, they have high linearity, and high phase precision. However, they suffer from higher insertion loss and thus lower noise performance, and require significant area consumption, rendering them unappealing for applications above the Ku-band. On the other hand, active filters are more suitable for satellite communication band and above. The most commonly implemented active phase shifter type is the vector-sum phase shifter (VSPS) [13] - [17]. VSPSs are used in various applications including electronic testing equipment [18], amplifier linearization [19], and image rejection receivers [20]. VSPSs exhibit higher system gain and are more compact than passive phase shifters. Nevertheless, state-of-the-art VSPS use quadrature generation, which is impractical for millimeter-wave applications. Poly-phase filters (PPFs) based on RC configuration are commonly used for Quadrature signal generation [13] - [14]. Nevertheless, they suffer from higher insertion loss at higher frequencies. Design in [15] uses current-mode RC PPF to reduce the insertion loss. Despite the loss reduction, the overall area of the chip is relatively large, in addition to its higher power consumption. Moreover, the I/Q signals can be generated by the quadrature all-pass filter (QAF). The QAF suffers from the capacitive loading from the succeeding amplification stage, therefore creating an amplitude and phase mismatch in the quadrature signals. Inductive loading may be used to address the amplitude mismatch of the I and Q signals [16]. Nevertheless, it requires using an additional buffer in the I and Q signal paths to minimize the phase mismatch. This, in turn, increases the die area and power overhead of the phase shifter. Furthermore, conventional VSPSs require the generation of differential I and Q signals followed by sign selectors, often differential amplifiers. The sign selector module is necessary to increase the phase range. This results in higher power consumption and a larger chip area. Design in [17] employs two zero-pi variable-gain amplifiers (VGAs) in conjunction with a quadrature hybrid coupler to implement a two-branch VSPS to reduce the DC power consumption. However, the chip area of the overall design remains large.

Unlike traditional VSPS, this paper presents a vector-sum design based on non-quadrature phase generation and synthesis, where the phase difference between the vectors can be as low as 11°. The generation of a small phase difference between the signal paths results in a smaller chip area. A switching network is used to interchange the two-phase paths. Another phase path is added at the input or output to generate 360° phase shifting.

II. Design, Theory, and System Level Implementation of the New Non-Quadrature Vector-Sum Phase Shifter Architecture

This section will discuss the design theory and system level implementation of the new vector-sum phase shifter.

A. Design Theory Analysis & System Level Implementation

A general block diagram of traditional vector-sum phase shifters is seen in Fig. 1. The quadrature generator produces in-phase (I) and quadrature (Q) signals from an RF input signal, which are subjected to amplification before being added (or subtracted) by a vector combiner. The I/Q signals can be produced using quadrature hybrid couplers. However, since each signal must be differential, I/Q generation using QAF, and RC PPF are often preferred. The generation of differential I and Q signals is necessary to cover close to 360º phase range in the conventional VSPS.

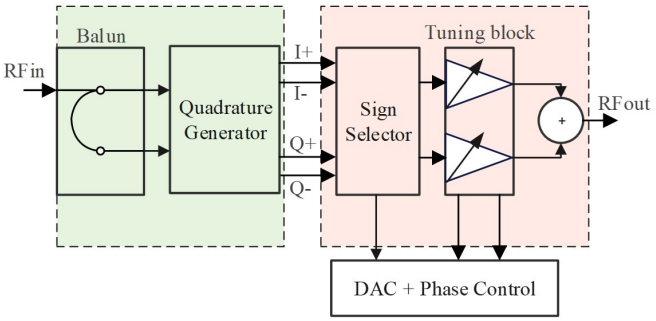

Fig. 1. System block diagram of conventional vector-sum phase shifter (VSPS). It consists of a balun for the two-pathways, a quadrature generator, a sign selector, a DAC phase controller, and a tuning block that is summed together.

Meanwhile, the I/Q generation often faces challenges, including amplitude and phase mismatches and large die areas. Next, a sign selector is used to switch between the phase quadrants. Amplitude variations between the signal paths are introduced using variable-gain amplifiers (VGAs), which produce phase change at the output. The vector combiner/adder combines the two signals. It can be implemented using a passive balun [17] - [21] or active circuit [22] - [23]. The sign selector, VGA and vector adder is referred to as vector synthesizer. Some works implement the sign selector and VGA as a single differential amplifier [17]. Other works use four independent VGAs at the four signal paths of the differential quadrature signals [24]. Either way, the power consumption of the vector synthesizer of the traditional VSPS appears to be often high.

The quadrature generation and synthesis in conventional phase shifter architectures prove to be area and power-consuming. Furthermore, A balun may be used before the I/Q generator [17] - [21], increasing the chip area. This work proposes a non-quadrature architecture, as seen in Fig. 2 (a). The input RF signal is split into two signals with the same phase and amplitudes. The signals are then subjected to a delay/bypass block, which is composed of two signal paths with a phase difference $\Delta\varphi < 90^o$. This block can be implemented using lumped elements high-pass/low-pass networks or transmission lines (Fig. 2 (b)). Next, a delay/phase path selector switches the phase lines between the upper and lower paths. This can be implemented using a double-pole double throw (DPDT) or two single-pole double-throw (SPDT) switches, as seen in Fig. 2 (c). The gain tuning stage can be implemented using a variable attenuator or a VGA, while the vector subtractor may be a passive or active balun. Alternatively, a single differential amplifier may be used as the subtractor, thus minimizing the chip area.

Assuming the input RF signal is represented as V_{in} and the gains/attenuations of the gain tuning stage are A_1 and A_2 for the lower and upper paths, respectively, the output RF signal can be written in phasor format as:

$$V_{out} = A_0(A_2 e^{j(\varphi_2+\varphi_0)} - A_1 e^{j(\varphi_1+\varphi_0)}) \cdot V_{in} \qquad (1)$$

where φ_1 and φ_2 are the phases introduced by the phase

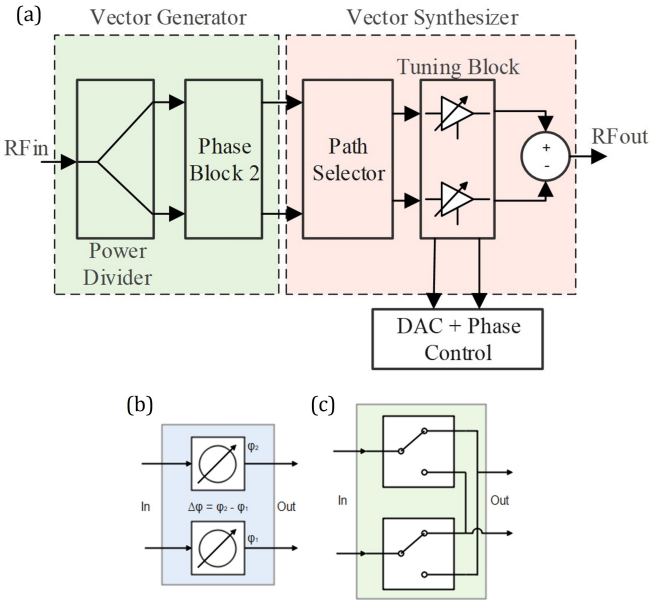

Fig. 2. Non-quadrature VSPS; (a) conceptual block diagram and implementation of (b) the delay/phase block and (c) phase path selector.

block to the lower and upper paths, respectively; φ_0 is the overall phase introduced by the remaining blocks including the splitter, the phase/delay path selector, the gain tuning stage and the vector subtractor. A_0 is the overall gain introduced by all the building blocks except the gain tuning stage. The phase and magnitude of V_{out} can be respectively expressed after using its complex format from (1) as:

$$\varphi_{out} = \begin{cases} \varphi_{in} + \tan^{-1}\left(\frac{Y}{X}\right), & \text{for } X \geq 0 \\ 180 + \varphi_{in} + \tan^{-1}\left(\frac{Y}{X}\right), & \text{for } X < 0 \end{cases} \qquad (2)$$

$$A_{out} = \mid V_{in} \mid \sqrt{X^2 + Y^2} \qquad (3)$$

where:

$$X = A_2\cos(\varphi_2 + \varphi_0) - A_1\cos(\varphi_1 + \varphi_0) \qquad (4)$$

$$Y = A_2\sin(\varphi_2 + \varphi_0) - A_1\sin(\varphi_1 + \varphi_0) \qquad (5)$$

As seen from (2), the output phase φ_{out} is a function of the gains A_1 and A_2 of the gain tuning block. Hence, the phase

tuning can be executed by tuning A_1 or A_2. Moreover, it is intended to inspect the behaviour of φ_{out} with respect to φ_1 or φ_2. For this purpose, assume $\varphi_2 = 0^o$, φ_0 = ° and A_1 = -10 dB. By plotting φ_{out} with respect to A_2, where A_2 is swept between -20 dB and 0 dB, and by stepping the value of φ_1 from -11.25° to -90°, the graph in Fig. 3 is obtained. It can be observed that the phase range increases for smaller values of φ_1. This is proven to be general for the phase difference $\Delta\varphi = \varphi_2 - \varphi_1$. In other words, larger phase tuning ranges are obtained for smaller $\Delta\varphi$ values. This is crucial for the proposed design as the phase difference is proportional to the size of the vector generator. In this regard, the phase range and area performance for $\Delta\varphi < 90^o$ is better than the traditional quadrature architecture. The value of φ_0, which is common for the two signal paths only changes the starting and the ending phases, keeping the phase range unchanged. Furthermore, by interchanging the path of φ_1 and φ_2, using the delay/phase path selector, the output voltage becomes inverted. As a result, the corresponding output phase becomes that in (2) added to 180°. Thus, similar phase ranges as seen in Fig. 3, expanding on the positive angle quadrant, are obtained.

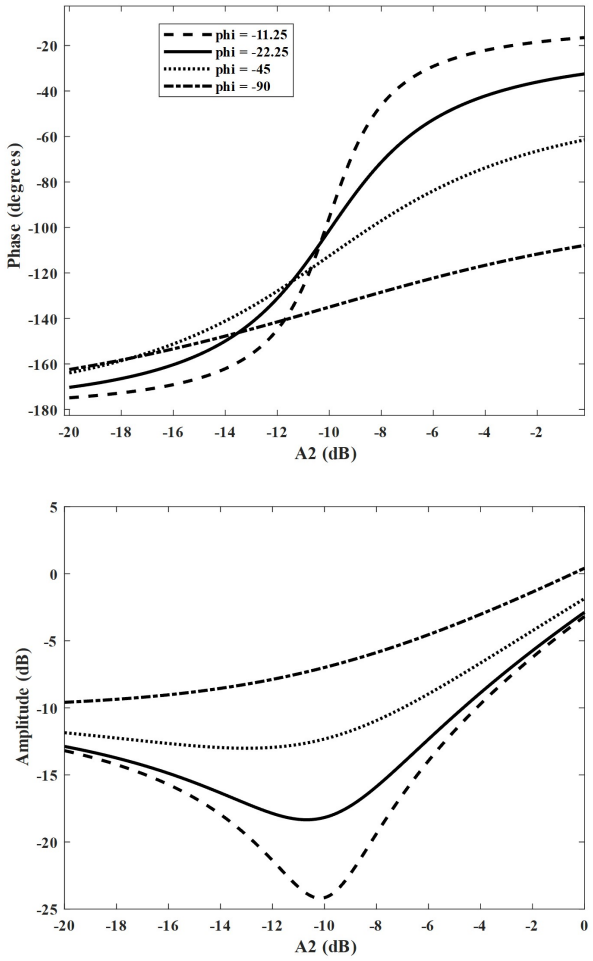

Fig. 3. Plot of the output phase (φ_{out}) for different values of φ_1.

B. Achieving the Full 360° Phase Tuning Range

In order to achieve a 360° phase tuning range using the design in Fig. 2, the gain tuning block must have an infinite attenuation (or gain) range. This is impractical as most attenuators (or VGAs) do not go beyond 30 dB of tuning range. As a result, each phase tuning quadrant will have a maximum phase shift of less than 10°. For instance, a 20 dB attenuation range produces a maximum phase shift of approximately 138° for $\varphi_1 = 22.5^o$ (as can be seen in Fig. 3 (a)). Therefore, a phase gap is created between the two phase quadrant, limiting the phase tuning range or the phase resolution. Furthermore, as the gain tuning range increases, more gain imbalance is created as seen from Fig. 3 (b); since strong gain imbalance is undesired in phase-array beamformer applications, a proper gain control must be adopted in order to bring the gain levels to the same level for different phase shifts. This adds more complexity to the design and increases the overall DC power consumption. For the aforementioned reasons, a different approach must be adopted in order to cover 360° phase shift with low gain imbalance.

The architecture in Fig. 4 shows the proposed full 360° non-quadrature VSPS. A second phase path block switched by two SPDT switches is added at the input of the structure in Fig. 2 (a). This alleviates the phase range requirement on the non-quadrature phase shifter. For instance, by selecting a phase difference of 90° for the second phase block, each quadrant is only required to produce 90° maximum phase shift. As a result, the attenuation (or gain) range of the gain tuning block is reduced. Similarly, the gain imbalanced is improved. For $\varphi_1 = 22.5^o$, the required gain range is only 8 dB and the maximum gain imbalance is about 6 dB. Hence, the power consumption of the gain tuning block is reduced and the effective gain of the phase shifter is boosted. The resulting phase is therefore able to accomplish 360° phase shift based on a coarse-fine tuning mechanism. The coarse tuning is effectuated by the two one-bit phase blocks, whereas the fine tuning is fulfilled by the gain tuning block, which can be controlled by a digital to analog converter (DAC), which determines the resolution of the phase shifter. By using a 6-bit DAC, a phase resolution of $90^o/2^6 \approx 1.4^o$ is feasible.

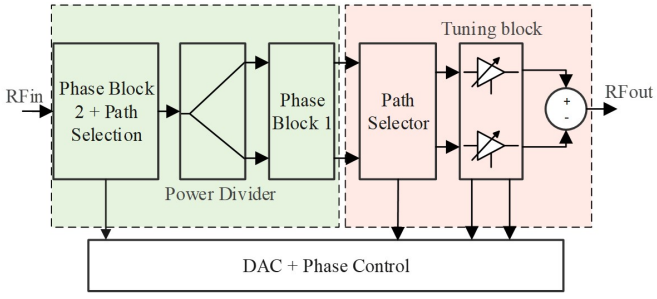

Fig. 4. Block digram of the proposed 360°non-quadrature VSPS.

III. Implementation of the New Proposed Phase Shifting Architecture in Advanced Design System (ADS) and Simulation Results

A proof-of-concept (POC) design of the proposed non-quadrature VSPS was set up and simulated using Keysight Advanced Design System (ADS) software as shown in Fig. 5. The input power splitter and the vector subtractor were implemented using microstrip line Wilkinson power divider and rat-race balun, respectively. The first phase block was designed and combined with the splitter to produce a phase difference of 22.5^o by elongating one output microstrip line of the splitter with respect to the other. The second phase block was also designed using microstrip transmission lines for providing a phase difference of 90^o. The splitter, phase paths, and rat-race balun were simulated using the electromagnetic (EM) Momentum simulator of ADS. The phase path selector was implemented using an ideal DPDT model with 0 dB insertion loss and 30 dB isolation. The gain tuning was performed by a variable attenuator with 8 dB attenuation range. The attenuation of the lower path attenuator, A_1 was fixed at -4 dB, while that of the upper path, A_2 was swept from -8 dB to 0 dB for the phase tuning. A 10 dB power amplifier was used at the output to bring the gain of the phase shifter closed to 0 dB. The substrate used for the simulation design was RT-Duroid 5880 with thickness height (h) of 0.254 mm and relative permittivity ε_r of 2.2. The targeted center frequency was 10 GHz. The input and output return losses are given in Fig. 6. Graph in Fig. 7 depicts the simulation results of the output phase and gain variations over frequency for different A_2 steps at all path selection bits. It can be observed that 360^o phase shift is obtainable for all frequencies from 8 GHz to 10 GHz.

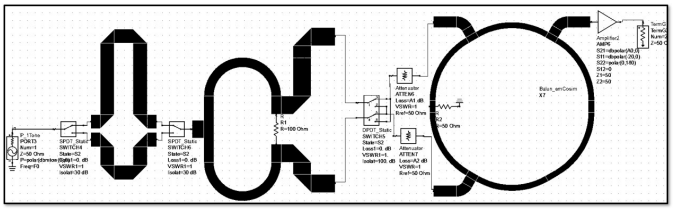

Fig. 5. Schematic diagram and implementation of the proposed VSPS architecture in Advanced Design System software. The phase delay, splitter, and the rat-race balun were all EM-Cosim-ed during simulation. A 50 Ohm input and output terminal ports were used for the simulations. Ideal switches, attenuators, and amplifiers were used for the simulations to show proof-of-concept of the new phase shifting architecture.

The phase tuning and gain variation with respect to A_2 at the center frequency can be visualized in Fig. 8(a) and Fig. 8(b), respectively. Each coarse bit provides a tuning range of 90^o with no phase gap, totalling 360^o phase shift. Additionally, the minimum and maximum gain of the phase shifter are -7.6 dB and -3.2 dB, respectively. Hence a total maximum gain imbalance of 4.4 dB is obtained, which is better than that of the traditional quadrature design. Moreover, the simulated phases added by the power splitter, balun, and path selectors at 10 GHz are -143.6^o, -168.5^o and -89.2^o,

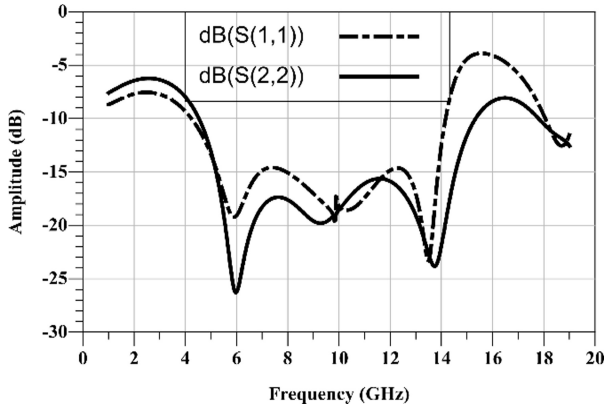

Fig. 6. Simulation results of the input and output reflection coefficients (S_{11} & S_{22}) of the new proposed phase shifting architecture.

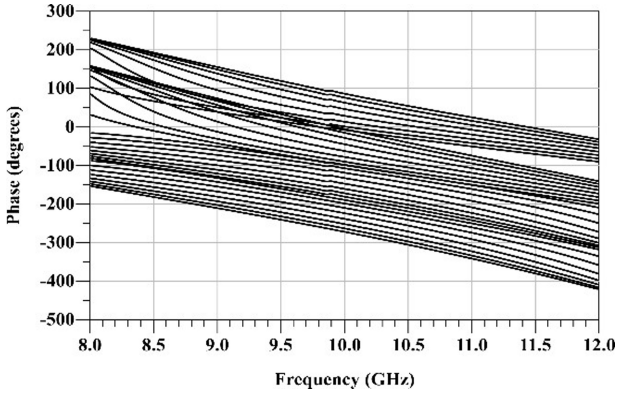

Fig. 7. Simulation of all phase states by stepping A_2 from -7 dB to 0 dB with 1 dB step sizes. A full 360 degree range is covered.

respectively. Assuming no further phases were added by the gain tuning and amplification stage , the total common phase shift of the two signal paths is about φ_0 = -401.3^o. Given that $\Delta\varphi = \varphi_2 - \varphi_1$ = -22.5^o, the theoretical or expected phase variation with respect to the attenuation A_2 can be calculated from (2). The residual phase error is therefore found by subtracting the simulated values from the calculated ones ($\varphi_{error} = \varphi_{simulated} - \varphi_{calculated}$). In percentage, this result may be normalized with respect to the calculated phase and scaled by 100. Fig. 9 presents the phase error of the simulated phase shifter with respect to the theoretically expected results for the four coarse tuning states. As can be observed from Fig. 9, the maximum error obtained is 1.82^o. The proposed phase shifter exhibits good performance in terms of phase error and reflection compared to state-of-the-art designs, achieving 360^o continuous phase change. See Table I for a comparison of the proposed phase shifter with other recent and relevant works.

IV. Conclusion

Active phase shifters are preferred in the implementation of phased-array beamformers at higher frequency bands due to their higher performance in terms of insertion loss and noise contribution. Conventional active phase shifters are based on

TABLE I
BENCHMARK AND COMPARISON OF PROPOSED PHASE SHIFTER WITH OTHER RECENT AND RELEVANT WORKS

Parameters	**This Work***	**[14]**	**[15]**	**[11]**	**[4]**
Architecture Type	VSPS	VSPS	VSPS	RTPS	STPS
Frequency (GHz)	10	28	24.55 to 27.4 & 26.55 to 29.4	29	6 to 18
Phase Range (^{o})	360	360	360	360	360
Phase Error (^{o})	$<$ 1.82	3.5	$<$ 2.3 @ 26.55 to 29.4 GHz	N.A.	10 @ 10 GHz
Phase Control	Continuous	Continuous	Continuous	Continuous	4-bits
Gain Imbalance (dB)	4.4	0.2	0.25 @ 26.55 to 29.4 GHz	4.6	N.A.
Minimum Return Loss (dB)	$>$ 18	N.A	$>$ 10	18	$>$ 4.5

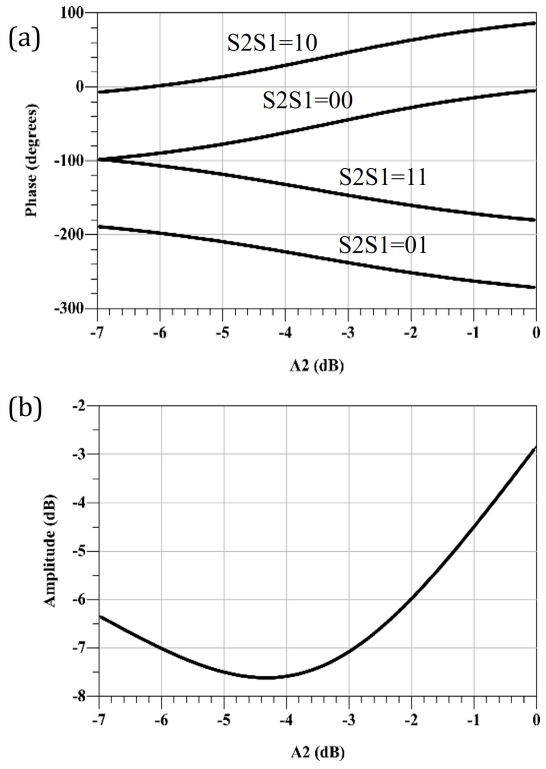

Fig. 8. Phase variation in (a) and gain variation in (b) or the proposed VSPS over various attenuation of A_2 at 10 GHz.

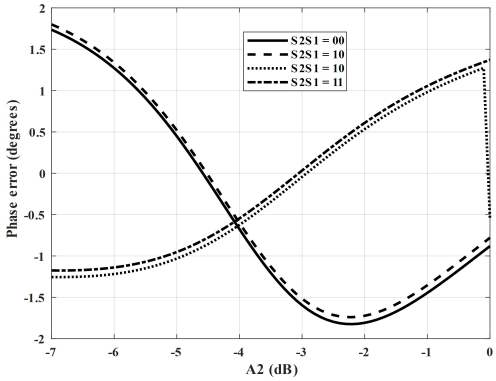

Fig. 9. Plot of residual phase error for different bits of phase blocks.

quadrature signal generation and synthesis that relatively consumes higher power and die area. This work proposes a power efficient active phase shifter based on a coarse-fine tuning of a non-quadrature vector summing to cover 360^o phase shift. The simulation results of a proof-of-concept PCB design, where the phase difference between the two signal paths is 22.5^o exhibit a maximum phase error and gain imbalance of 1.82^o and 4.4 dB at the center frequency of 10 GHz. Future works include the implementation of the design in CMOS process, where the signal splitting and subtraction will be done through active elements, which can prospectively further decrease the overall chip area requirement in subsequent implementations.

REFERENCES

[1] Y. -J. Liang, K. -C. Chiang, Y. -H. Lin, H. Alsuraisry, J. -H. Tsai, and T. -W. Huang, "A 19-GHz 5-bit switch-type phase shifter design using phase compensation techniques," IEEE Int. Symp. on Radio-Frequency Integration Technology, 2021, pp. 1-3.

[2] S. Abdullah, G. Gaozhi Xiao, and R. E. Amaya, "Design and implementation of an 8-bit, 256-step digitally-controlled phase shifter at 2.1 GHz with minimum 1.41° phase change for its LSB step size," IEEE Canadian Conf. on Electrical and Computer Engineering, 2021, pp. 1-4.

[3] S. Abdullah, W. Zhou and R. E. Amaya, "Design and Implementation of Fine Tuning Phase Shifting Trimmer in III-V Semiconductor Technologies," 2022 International Conference on Microelectronics (ICM), Casablanca, Morocco, 2022, pp. 209-212, doi: 10.1109/ICM56065.2022.10005379.

[4] S. Abdullah and R. E. Amaya, "A 4-Bit 360o 10 GHz Digitally-Controlled Passive Phase Shifter With Digital Logic Control On-Chip in 0.15 μm Indium Gallium Arsenide (InGaAs) pHEMT Process," 2022 International Conference on Microelectronics (ICM), Casablanca, Morocco, 2022, pp. 148-151, doi: 10.1109/ICM56065.2022.10005322.

[5] S. Abdullah, G. G. Xiao and R. E. Amaya, "Phase Shifting Trimmer with Small Precision Phase Change for Offsetting Process-Voltage-Temperature Tolerances," 2021 IEEE 19th International Symposium on Antenna Technology and Applied Electromagnetics (ANTEM), 2021, pp. 1-2.

[6] O. Occello, L. Tiague, M. Margalef-Rovira, L. Vincent, F. Ndagijimana, and P. Ferrari, "High-performance compact reflection-type phase shifter operating at 2 GHz using a transdirectional coupler," 50th European Microwave Conf., 2021, pp. 550-553.

[7] E. Kim and S. Jeon, "A Compact 275–320-GHz Reflection-Type Phase Shifter," in IEEE Microwave and Wireless Components Letters, vol. 32, no. 8, pp. 991-994, Aug. 2022, doi: 10.1109/LMWC.2022.3161971.

[8] Jen-Chieh Wu, Chia-Chan Chang, Sheng-Fuh Chang and Ting-Yueh Chin, "A 24-GHz full-360^o CMOS reflection-type phase shifter MMIC with low loss-variation," 2008 IEEE Radio Frequency Integrated Circuits Symposium, 2008, pp. 365-368, doi: 10.1109/RFIC.2008.4561455.

[9] S. Bulja, D. Mirshekar-Syahkal, M. Yazdanpanahi, R. James, S. E. Day and F. A. Fernández, "60 GHz Reflection Type Phase Shifter based on liquid crystal," 2010 IEEE Radio and Wireless Symposium (RWS), 2010, pp. 697-699, doi: 10.1109/RWS.2010.5434253.
[10] Y. Chang and B. A. Floyd, "A Broadband Reflection-Type Phase Shifter Achieving Uniform Phase and Amplitude Response across 27 to 31 GHz," 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2019, pp. 1-4, doi: 10.1109/BCICTS45179.2019.8972730.
[11] A. Basaligheh, P. Saffari, S. Rasti Boroujeni, I. Filanovsky and K. Moez, "A 28–30 GHz CMOS Reflection-Type Phase Shifter With Full 360° Phase Shift Range," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 11, pp. 2452-2456, Nov. 2020, doi: 10.1109/TCSII.2020.2965395.
[12] P. Gu and D. Zhao, "Ka-Band CMOS 360° Reflective-Type Phase Shifter with ± 0.2 dB Insertion Loss Variation Using Triple-Resonating Load and Dual-Voltage Control Techniques," 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2018, pp. 140-143, doi: 10.1109/RFIC.2018.8428987.
[13] M. Momeni and M. Moezzi, "A low loss and area efficient rc passive poly phase filter for monolithic GHz vector-sum circuits," IEEE Trans. Circuits and Systems II: Express Briefs, vol. 66, pp. 1134-1138, July 2019.
[14] P. Soni and G. Banerjee, "Continuously tunable 360^{o} quadrature phase shifter in 65-nm CMOS for 5G-NR," IEEE MTT-S Int. Microwave and RF Conf., 2021, pp. 1-4.
[15] F. Akbar and A. Mortazawi, "A frequency tunable 360^{o} analog CMOS phase shifter with an adjustable amplitude," IEEE Trans. Circuits and Systems II: Express Briefs, vol. 64, pp. 1427-1431, Dec. 2017.
[16] S. P. Sah and D. Heo, "An ultra-wideband 15–35 GHz phase-shifter for beamforming applications," European Microwave Integrated Circuit Conf., 2013, pp. 264-267.
[17] T. Wu et al., "A 60-GHz Variable Gain Phase Shifter With 14.8-dB Gain Tuning Range and 6-Bit Phase Resolution Across -25 ^{o}C-110 ^{o}C," in IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 4, pp. 2371-2385, April 2021.
[18] Dong Ho Lee, Chung-Hwan Kim and Songcheol Hong, "A quadrature signal generator using PLL technique," 33rd European Microwave Conference Proceedings (IEEE Cat. No.03EX723C), Munich, Germany, 2003, pp. 777-780 vol.2, doi: 10.1109/EUMC.2003.177591.
[19] G. Dalwadi, B. I. Shah, V. M. Verma, G. Kurkure, R. Sharma and P. Bhatnagar, "Efficient Doherty Feed-forward Linear Power Amplifier for CDMA 2000 Base-Station Applications," 2008 International Conference on Signal Processing, Communications and Networking, Chennai, India, 2008, pp. 35-40, doi: 10.1109/ICSCN.2008.4447157.
[20] J. Kim, Wooyeol Choi, Youngrak Park and Y. Kwon, "60 GHz broadband image rejection receiver using varactor tuning," 2010 IEEE Radio Frequency Integrated Circuits Symposium, Anaheim, CA, USA, 2010, pp. 381-384, doi: 10.1109/RFIC.2010.5477351.
[21] J. Zhou, H. J. Qian, and X. Luo, "A 9-Bit vector-sum digital phase shifter using high resolution VGAs and compensated quadrature signal generator," IEEE MTT-S Int. Microwave Conf. on Hardware and Systems for 5G and Beyond, 2019, pp. 1-3.
[22] E. V. Balashov and I. A. Rumyancev, "An unbalanced transformer-less vector-sum phase shifter architecture," IEEE NW Russia Young Researchers in Electrical and Electronic Engineering Conf., 2016, pp. 491-494.
[23] Y. -T. Chang, W. -Y. Wang, and H. -C. Lu, "A 19 GHz vector-sum phase shifter using active current-mode coupler and bi-phase modulator for satellite communication," IEEE Asia-Pacific Microwave Conf., 2020, pp. 988-990.
[24] Y. Ye, L. -Y. Li, R. Tong, and X. -W. Sun, "A full-360^{o} vector-sum phase shifter with low RMS phase and gain errors for 60 GHz 5-bit application," 9th European Microwave Integrated Circuit Conf., 2014, pp. 305-308.