High-Isolation Millimeter-Wave Subharmonic Monolithic Mixer With Modified Quasi-Circulator

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***Abstract*—This study presents a 21–40-GHz broadband subharmonic gate-pumped mixer using the standard 0.18-μm CMOS process. A modified quasi-circulator is monolithically integrated with an nMOS field-effect transistor to perform down-converter mixing while enhancing all port isolations through a broadband operation. The proposed configuration has a chip size of less than 0.9 mm ^{2}. The measured results demonstrate a low conversion loss from 8.3 to 14.2 dB, a local oscillation (LO)-to-RF isolation greater than 50 dB, and a high 2LO-to-RF isolation of 48 dB to 65 dB over the 21–40-GHz RF bandwidth at a 10.5-dBm LO power level.**

***Index Terms*—CMOS, isolation, quasi-circulator, subharmonic mixer (SHM).**

I. Introduction

RECENTLY, much attention has been given to millimeter-wave communication systems operating in the Ka-band with wide operational bandwidth, high-speed data transfer, low manufacturing cost, and low-power consumption. The mixer is an important component of the millimeter-wave transceiver because it converts signals from one frequency to another. The subharmonic mixer (SHM) enables the local oscillation (LO) to operate at a frequency half that of the fundamental mixer. Thus, SHMs are very suitable in millimeter-wave range applications, which make local-oscillator sources more reliable and less expensive than its counterparts [1]–[14].

Passive mixers have better linearity, broad bandwidth, and low dc power consumption. However, they suffer from high conversion loss and degraded noise performance of the communication system. Compared with passive mixers, active mixers provide higher conversion gain and better noise performance. Active mixers also have their drawbacks, namely, high dc power consumption, narrow operation bandwidth, and relatively low linearity. Previous studies have shown that SHMs using an antiparallel diode pair configuration have several advantages, such as suppressing any even harmonics of LO signals without dc power [1], [2]. The use of short and open stubs in SHMs limits the operation bandwidth [1], and undesirable LO-to-RF isolation results from the use of a directional coupler [2]. Many topologies have been proposed to achieve broad operation bandwidths [3]–[5], but these topologies do not provide high isolation levels between ports. The SHM using a rate-race coupler to achieve broad operation bandwidth has been proposed [4]. However, it does not provide high LO-to-RF isolation level because of the high amplitude/phase difference in the $\lambda_{\rm RF}/4$ and $\lambda_{\rm LO}/4$ transmission lines ($f_{\rm LO} = f_{\rm RF}/2$) of the rate-race coupler. The gate-pumped and source-pumped resistive mixers have gained increasing attention in recent years [5]–[11]. The subharmonic gate-pumped resistive mixers (SHPRMs) have the advantages of broad bandwidth and good linearity. However, SHPRM have poor port-to-port isolations. Although SHPRM using an LO frequency doubler circuit have been known to achieve good port-to-port isolation [6], it does not have a wide operating bandwidth. A low LO drive power SHPRM using the connection between drain and body structure with 0.13-μm CMOS has been proposed [7]. Compact baluns have been used in high-isolation SHPRMs [8], [9], but limiting the operation bandwidth resulted in an observed trade-off phenomenon. The W-band SHPRM uses the 0.15-μm GaAs pseudomorphic HEMT (pHEMT) process to achieve low conversion loss [11], but it has poor port-to-port isolation. Although the LO/2LO/RF-to-IF isolation can be improved by the structure of low-pass filter, the LO/2LO leakage to the RF port may be mixed to generate an output dc offset. The LO signal leaks through the RF port if the isolation level between the LO and RF ports is not high enough. The leak reduces the dynamic range of the preamplifier in the receiver. Thus, maintaining a good LO-to-RF isolation is important to suppress high-power leakage from the LO to the RF port.

Previous studies have shown that active circulators are more suitable for integrated system-on-chip applications using monolithic microwave integrated circuit (MMIC) integration [15]–[17]. Active circulators play an important role in MMIC integration because they allow signals to flow in only one direction and good impedance is observed at all ports. Thus, the transmitter and receiver of signals can simultaneously work at different frequencies without the use of diplexer filters. Moreover, active circulators have the most advantages in terms of bandwidth, chip dimension, and insertion loss. However, signal transfers from port 3 to port 1 in active circulators remain problematic. This transfer indicates that the receiver signals will leak to the transmitter port. The three-port quasi-circulators can

Manuscript received December 30, 2012; revised January 09, 2013; accepted January 10, 2013. Date of publication February 15, 2013; date of current version March 07, 2013. This work was supported in part by the National Chip Implementation Center, National Applied Research Laboratories, the National Science Council of Taiwan under Contract NSC95-2221-E-006-428-MY3, Contract 982C12, Contract 98IC05, and Contract 100C02, and by the Foundation of Chen, Jieh-Chen Scholarship of Tainan.

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Digital Object Identifier 10.1109/TMTT.2013.2244229

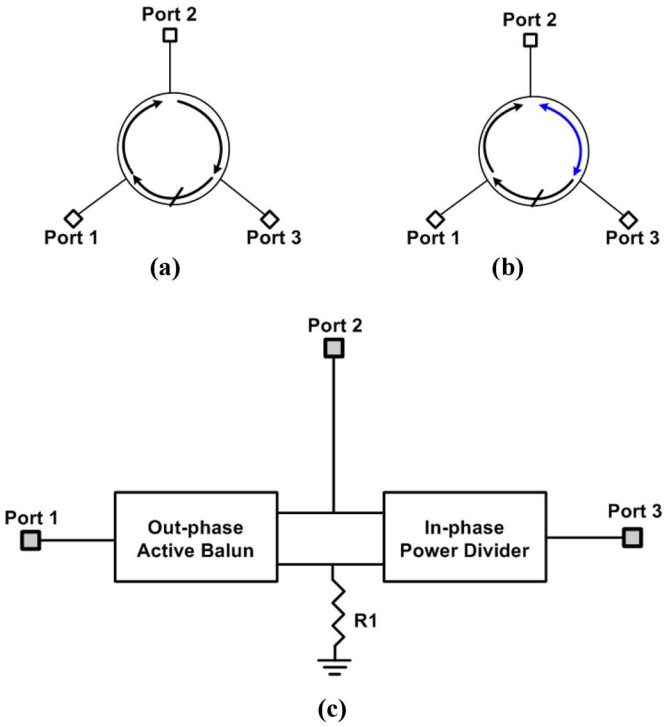

Fig. 1. Three-port quasi-circulators. (a) Conventional quasi-circulator. (b) Proposed modified quasi-circulator. (c) Block diagram of the proposed modified QCM.

resolve this issue because they only support two power flows in the same direction, as shown in Fig. 1(a) [18]–[24]. Thus, many active quasi-circulator module (QCM) configurations have been introduced in microwave system applications, such as separating the transmitted and received signals. Based on QCM property, the active QCM is used to improve the port-to-port isolations of SHM [25]. However, it causes a low 1-dB power compression and just passable LO-to-RF isolation.

In this work, a modified QCM is proposed to further enhance the LO-to-RF isolation and operation bandwidth of SHM. The major difference between the proposed modified QCM and the conventional QCM in practice is that the modified QCM enables bilateral power transfer between ports 2 and 3 without power transfer from port 3 to port 1, as shown in Fig. 1(b). Moreover, the conventional rat-race hybrid is different from the proposed modified QCM, because the proposed modified quasi-circulator is a three-port component that has unidirectional performance, only one operation mode, and excellent port-to-port isolation. Compare the property of the proposed modified quasi-circulator with that of conventional rat-race hybrid and conventional quasi-circulator, the major operation characteristic are both different. Actually, the design concept is from the conventional quasi-circulator and the operation characteristic of the proposed modified quasi-circulator is the same as the conventional quasi-circulator. The proposed modified quasi-circulator used the passive power divider to replace the unilateral in-phase combiner [26]. It can excite an RF and LO signal into gate mixer simultaneously and improve the isolation between the RF and LO ports during operation bandwidth. This feature can easily combine LO and RF signals into the gate-pumped transistor to achieve an excellent LO-to-RF isolation of SHM.

The proposed modified quasi-circulator uses an active balun, which has the features of phase cancellation, small chip size, and low insertion loss. Moreover, the passive power divider provides a high dynamic range with a wide operation bandwidth [see Fig. 1(c)]. The modified QCM has an insertion loss of 4.5 dB and a port 3-to-port 1 isolation of 53 dB at a bandwidth range between 21–40 GHz for SHM application. This paper presents a 21–40-GHz MMIC SHM using a TSMC 0.18-μm CMOS process. Using the modified QCM technique, the proposed SHM has good operating bandwidth, port-to-port isolation, chip dimensions, and high-level integration. This paper is organized as follows. Section II discusses the design of the proposed mixer configuration using a modified QCM. Section III presents the measured RF characteristics of the high-isolation SHM. Finally, Section IV provides a conclusion.

II. Proposed Mixer Configuration Design

A. Modified Quasi-Circulator

Compared with a conventional quasi-circulator [see Fig. 1(a)], the proposed modified QCM allows bilateral power transfers between ports 2 and 3 such that the power transfers of the proposed modified QCM occur from port 1 to port 2, from port 2 to port 3, and from port 3 to port 2 without power transfers from port 3 to port 1 [see Fig. 1(b)]. Fig. 1(c) shows the basic configuration of the proposed modified quasi-circulator, a unilateral out-phase active balun, and a passive in-phase power divider connected in cascade. Port 2 is branched from one of the connected lines, whereas the shunt impedance R1 is connected to the other line. The shunt impedance R1 is equal to the reference impedance of port 2 of the QCM and is connected to the other port of the in-phase power divider to obtain the same magnitude of signals with the out-phase active balun. The increased loss of shunt impedance R1 for the RF signal is about 3.5 dB (simulated). However, this design can enhance the LO/RF-to-RF/LO isolation of the proposed mixer and maintain the mixer performance at the expense of loss. Isolation in the proposed modified QCM occurs between port 1 and port 3, which is caused by the active balun with unilateral characteristic and phase cancellation. No power is transferred from port 3 to port 1 of the modified QCM because of the unidirectional property of the active balun. Moreover, the signals transferring from port 1 to port 3 are split into two out-phase signals with equal amplitudes by the active balun. The signals then flow through the in-phase power divider into port 3. Therefore, the two signals are canceled by the phase cancellation at port 3. The proposed modified quasi-circulator enables bilateral power transfers between ports 2 and 3 because of the nondirectional characteristic of the passive power divider. Thus, the proposed modified QCM can simply combine LO and RF signals into the gate-pumped transistor and enhance the LO-to-RF isolation of SHM.

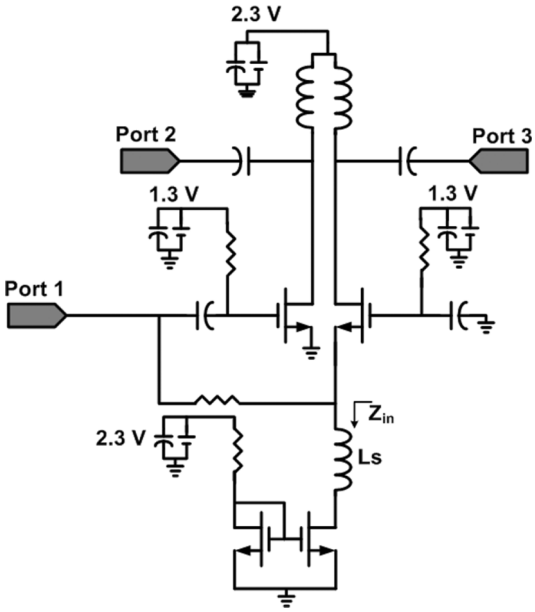

Fig. 2. Circuit diagram of the proposed active balun.

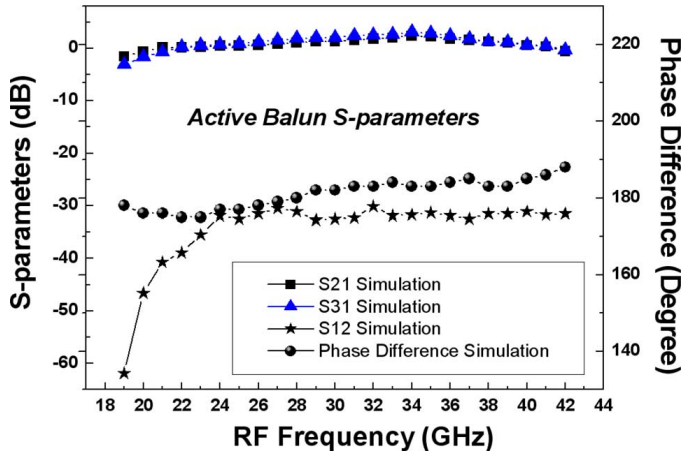

Fig. 3. Simulated S-parameters of the active balun at an RF range of 19–42 GHz.

B. Active Balun

The schematic diagram of the proposed active balun, which is composed of the common-source (CS), common-gate (CG), and current mirror configuration, is shown in Fig. 2. One input of the CS is single ended, whereas the other is grounded through the bypass capacitor.

The active balun circuit can be realized by CG and CS circuits. The $(S_{21})_{\rm CS}$ and the phase of $S_{21}((\angle S_{21})_{\rm CS})$ are [27]

$$(S_{21})_{\rm CS} = \frac{-2g_m Z_0}{1+j\omega C_{\rm gs} Z_0}$$
$$(\angle S_{21})_{\rm CS} = \tan^{-1}(-\omega C_{\rm gs} Z_0). \quad (1)$$

The $(S_{31})_{\rm CG}$ and the phase of $S_{31}((\angle S_{31})_{\rm CG})$ are

$$(S_{31})_{\rm CG} = \frac{2g_m Z_0}{1+(j\omega C_{\rm gs}+g_m)Z_0}$$
$$(\angle S_{31})_{\rm CG} = \tan^{-1}\left(\frac{-\omega C_{\rm gs} Z_0}{1+g_m Z_0}\right). \quad (2)$$

Therefore, from (1) and (2), the phase difference of the conventional balun is given by

$$(\angle S_{21})_{\rm CS} - (\angle S_{31})_{\rm CG} = \tan^{-1}\left(\frac{-g_m \omega C_{\rm gs} Z_0^2}{1+g_m Z_0+\omega^2 C_{\rm gs}^2 Z_0^2}\right). \quad (3)$$

At high frequency, the parasitic capacitance $C_{\rm gs}$ acts the role of low impedance resulting in certain power dissipation. Thus, the amplitude and phase imbalance between the two outputs of the active balun will increase at higher frequency.

To increase $Z_{\rm in}$, an inductor Ls is added to the source of the current mirror. Although Ls has a high insertion loss at high frequency, the main RF signals were blocked and maintained the performance of the active balun by the high-impedance $Z_{\rm in}$ [28]. Furthermore, the design of the current source is crucial to the amplitude and the phase imbalance. An active component is often used as the current source. However, the active component has parasitic effect at high frequency. A portion of the signal flows through this path and results in amplitude imbalance and phase error [29]. Therefore, the current mirror with inductor Ls is designed to improve the amplitude imbalance and the phase error at high frequency since a high common-mode rejection ratio (CMRR) can be obtained with a high-impedance $(Z_{\rm in})$ [30]

$$\text{CMRR} \approx \sqrt{\frac{(2+\Delta)^2+\theta^2(1+\Delta)^2}{\Delta^2+\theta^2(1+\Delta)^2}} \approx \frac{2+\Delta}{\sqrt{\Delta^2+\theta^2}} \quad (4)$$

where Δ is the amplitude imbalance and θ is the phase imbalance.

Thus, the inductor Ls is added to the source of the current mirror, as shown in Fig. 2, to improve the CMRR and amplitude/phase imbalance of the proposed balun with broad operation bandwidth at high frequency. The inductors and resistors are designed as an RF choke and matching network. In addition, the active balun of the proposed QCM is used to reduce the chip dimensions and obtain good insertion loss. Thus, the proposed SHM has good conversion loss.

Due to the use of the inductor Ls and the current mirror, the drain–source (D-S) bias voltage is then larger for the CS field-effect transistor (FET) compared to that of the CG FET. It can select the device size and component parameters of the active balun to tune the active balun performance. This will not affect the active balun performance, but enhance the phase/amplitude imbalance and bandwidth performance. Fig. 3 shows the simulated S-parameters of the proposed active balun with a dc power consumption of 46.6 mW. The simulated S_{21}/S_{31} of the active balun is from -1.8 to 3 dB, the phase difference of the out-phase is within 7°, and the amplitude error is within 0.5 dB from 20 to 40 GHz. Moreover, the S_{12} of the active balun is better than 30 dB. The simulated results show a 1-dB compression point of -3 dBm when the RF is fixed at 30 GHz. Based on simulated results, the active balun not only results in a small chip dimension and low insertion loss, but it also confers a unidirectional property. Therefore, the proposed modified QCM provides an excellent LO-to-RF isolation of SHM. Fig. 4 shows the simulated noise figure (NF) of the active balun as a function of RF

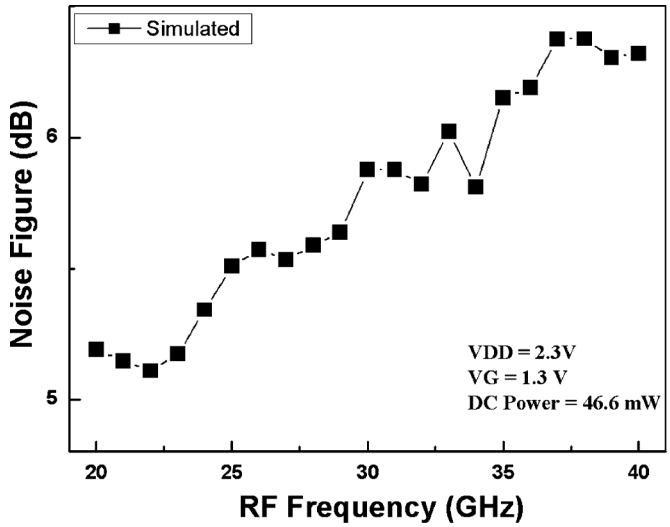

Fig. 4. Simulated NF of the proposed active balun at VDD of 2.3 V and VG of 1.3 GHz.

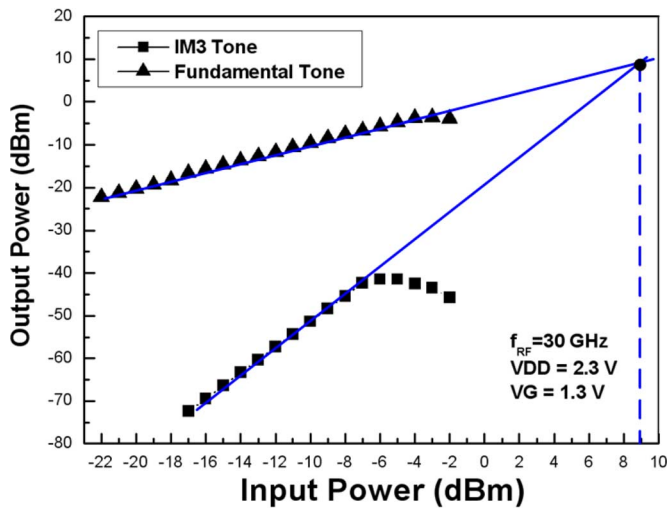

Fig. 5. Simulated IIP3 of the proposed active balun at VDD of 2.3 V and VG of 1.3 GHz.

frequency at drain biase voltage of 2.3 V and gate bias voltage of 1.3 GHz. The simulated NF of the proposed active balun ranges from 5.1 to 6.3 dB at an RF in the range from 20 to 40 GHz. Moreover, the simulated third-order intermodulation intercept point (IIP3) of the active balun is about 9 dBm, as shown in Fig. 5.

C. In-Phase Power Divider

The proposed configuration of the in-phase power divider is shown in Fig. 6. The high LO input drive power level causes the LO input to use the passive divider to achieve a high dynamic range. Moreover, the spiral layout is used to compress the size in the passive power divider. Agilent ADS Momentum is used to calculate the S-parameters of the passive structures and to optimize the geometry of the power divider to reduce insertion loss. Thus, the LO drive power level of the SHM is also reduced. The power divider is tightly spaced to extend the bandwidth and to ensure a sufficient coupling coefficient. Consequently, the optimal divider spacing between Metal 3 and Metal 6 can

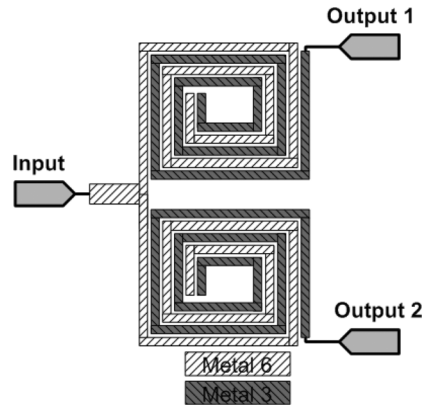

Fig. 6. Circuit diagram of the power divider.

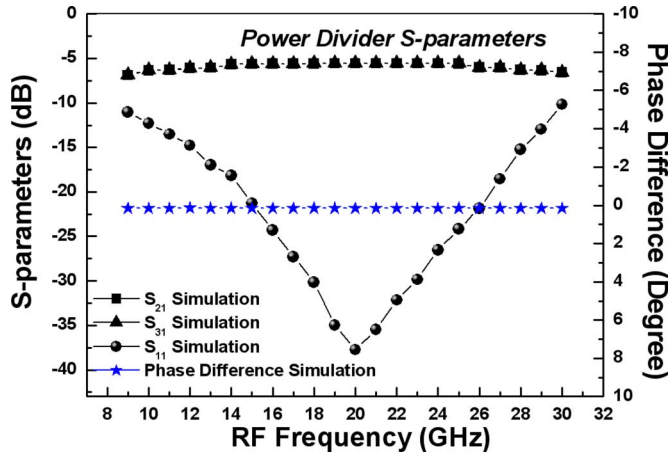

Fig. 7. Simulated S-parameters of the in-phase power divider at an RF range of 9–30 GHz.

be obtained at 0.5 μm, and the line width of Metal 3 and Metal 6 is 6 and 4 μm, respectively. The total length is 1260.5 μm at the 20-GHz RF center frequency.

Fig. 7 shows the simulated S-parameters of the proposed power divider at an RF range of 9–30 GHz. The simulated insertion loss of the power divider is from 5.4 to 6.3 dB, and the phase difference of the in-phase is within 0.1° from 9 to 30 GHz. The input return loss S_{11} of the power divider was from -11.2 to -38.8 dB from 14 to 40 GHz. Moreover, the 1-dB compression point of the power divider is higher than 12 dBm for high LO drive power level. The symmetrical spiral power divider not only supports a high LO power level, but also obtains an amplitude error of 0 dB, low insertion loss, and good phase difference.

Fig. 8 shows the simulated S-parameters of the proposed modified QCM at an RF range of 9–40 GHz. The simulated S_{13} of the proposed QCM range is from -32 to -53 dB at an RF frequency between 9–40 GHz. The simulated $|S_{23}|$ of the QCM is also equal to $|S_{32}|$, which is better than 6 dB at an RF range of 9–30 GHz. The simulated $|S_{21}|$ and $|S_{12}|$ of the QCM are from 4.5 to 6.5 dB and 20.3 to 24.8 dB, respectively, between 20–40 GHz. Based on the simulated results, the proposed QCM has good insertion loss for port 1 to port 2, port 2 to port 3, and port 3 to port 2. Moreover, the proposed QCM provides excellent isolation of port 2 to port 1 and port 3 to port 1 between 9–40 GHz. Therefore, the proposed modified QCM not only simultaneously

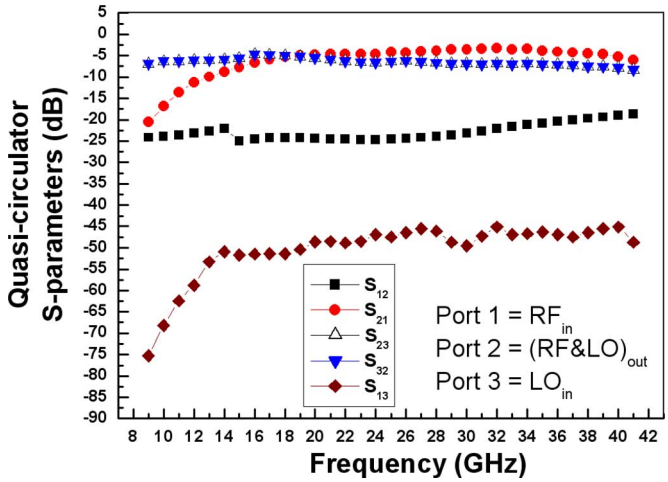

Fig. 8. Simulated S-parameters of the proposed modified QCM at an RF range of 9–40 GHz.

TABLE I
SIMULATED PERFORMANCES OF BUILDING BLOCKS FOR THE MODIFIED QUASI-CIRCULATOR IN STANDARD 0.18-μM CMOS TECHNOLOGY

Block	Item	Quantity
Active Balun (@ 20 GHz–40 GHz)	Return Loss	> 6 dB
	Gain	-1.8 dB–3 dB
	Amplitude Error	0.5 dB
	Phase Difference	7°
	DC Power	46.6 mW
Power Divider (@ 10 GHz–30 GHz)	Insertion Loss	5.4 dB–6.3 dB
	Amplitude Error	0 dB
	Phase Difference	0.1°
	Dimension	0.4 × 0.17 mm^2
Modified Quasi-circulator	S_{21} (@ 20 GHz–40 GHz)	-4.5 dB– -6.5 dB
	S_{23} & S_{32} (@ 10 GHz–30 GHz)	-5 dB– -7 dB
	S_{13} (@ 10 GHz–40 GHz)	-30 dB– -53 dB
	Return Loss (@ 10 GHz–40 GHz)	> 8 dB

excites RF and LO signals into the transistor for subharmonic mixing, but also provides excellent LO-to-RF isolation and wide operation bandwidth performance. In addition, the power divider does not affect the balun operation and performance by the capacitor. Equal insertion loss (S_{21} and S_{32}) of the proposed quasi-circulator is designed. Therefore, R1 (500 Ω) is added to obtain the same magnitude of signals with the out-phase active balun. Table I summarizes the performance of the proposed modified QCM and its building blocks. This modified QCM has high isolation, low insertion loss, and wide operation bandwidth performance.

D. SHM Configuration

When LO and RF signals are applied to the gate, the gate–drain transconductance g_m changes. The time-dependent conductance, which contains fundamental and harmonic frequency elements of the LO signal, generates a drain current that contains different frequency elements. Between these frequency elements, a component at the IF frequency, $f_{\rm IF} = |f_{\rm RF} - nf_{\rm LO}|$, is extracted using a low-pass filter at the drain, where $n = 1, 2, 3, \ldots$ is an integer [5]. In the fundamental mixer, an IF signal corresponding to $n = 1$ is selected. However, an IF signal corresponding to $n \geq 2$ is utilized in the SHM. Thus, the SHM requires only $1/n$ of the LO frequency in the fundamental mixer with the same RF and IF frequencies. Consequently, combining a high-frequency RF signal with a relatively low-frequency LO signal through the hybrid method is difficult.

In this study, a novel SHM configuration is proposed to overcome the problems mentioned previously and to achieve a superior isolation performance. The proposed novel configuration of the SHM, which consists of a modified QCM, low-pass filter, and a gate-pumped transistor M1 for subharmonic mixing, is shown in Fig. 9(a). The proposed modified QCM is composed of an active balun, an in-phase power divider, and a shunt resistance R1, as shown in Fig. 9(b). The LO signal is applied at the mixer nMOS gate and at the balun outputs as well. Thus, the proposed modified QCM is to simultaneously excite an RF and LO signal into the nMOS gate (M1) and to improve isolation between RF and LO ports during broadband operation. The mixer operates in a gate-pumped mode. The IF signal is extracted by the drain of the low-pass filter. The gate bias is applied through a resistor Rg, which also enhances the stability of the SHM. The LO and RF signals injected to the gate through a capacitor Cg are applied for dc decoupling, which reduces the IF signal leakage to this port. Moreover, the capacitor Cg and the inductor Lg are applied for inter-stage matching network between the modified quasi-circulator and the gate-pumped transistor M1. The matching network assures the smooth integration of the LO and RF signals into the M1. At the drain, an L-network composed of Lp and Cp, which acts as a low-pass filter for the RF/LO-to-IF isolations and extract the IF signal, is used. In addition, the modified quasi-circulator is used in the circuit to increase the LO-to-RF isolation and combining the LO and RF signals into the M1. After considering the tradeoff of the conversion loss, 2LO-to-IF/RF isolations, and operation bandwidth, the CMOS of an nMOS device with a gate width of 208 μm is used in the gate-pumped transistor.

In this work, the purpose of the modified quasi-circulator is to simultaneously excite an RF and LO signal into gate mixer and to improve isolation between RF and LO ports during operation bandwidth. Equations (5)–(7) are used to simplify the analysis using the schematics of the gate-pumped mixer shown in Fig. 10, when the LO voltage of amplitude is large enough to make $g_m(t)$ nonlinear. The elements of the IF current $I_{\rm IF}(t)$ is

$$I_{\rm IF}(t) = \frac{1}{4}\frac{g_1 V_{\rm RF}}{\omega_{\rm RF} C_{\rm GS} R_{\rm in}} \cos(\omega_{\rm RF} - 2\omega_{\rm LO})t \approx \frac{1}{8}\frac{g_{m,\max} V_{\rm RF}}{\omega_{\rm RF} C_{\rm GS} R_{\rm in}} \cos(\omega_{\rm RF} - 2\omega_{\rm LO})t. \quad (5)$$

If the conjugated IF port matches with the impedance of the $P_{\rm IF}$ while suppressing all other elements, the IF output power $P_{\rm IF}$ and conversion gain G_C can be expressed as follows:

$$P_{\rm IF} = \frac{1}{2}|I_{\rm IF}|^2 R_{\rm IF} = \frac{g_{m,\max}^2 V_S^2 R_{\rm IF}}{128\omega_{\rm RF}^2 C_{\rm GS}^2 R_{\rm in}^2} \quad (6)$$

$$G_C = \frac{P_{\rm IF}}{P_{\rm RF}} = \frac{g_{m,\max}^2 R_{\rm IF}}{16\omega_{\rm RF}^2 C_{\rm GS}^2 R_{\rm in}}. \quad (7)$$

From (7), we can deduce that the $g_{m,\max}^2$ increases with increasing G_C. Therefore, the properties of G_C are affected by

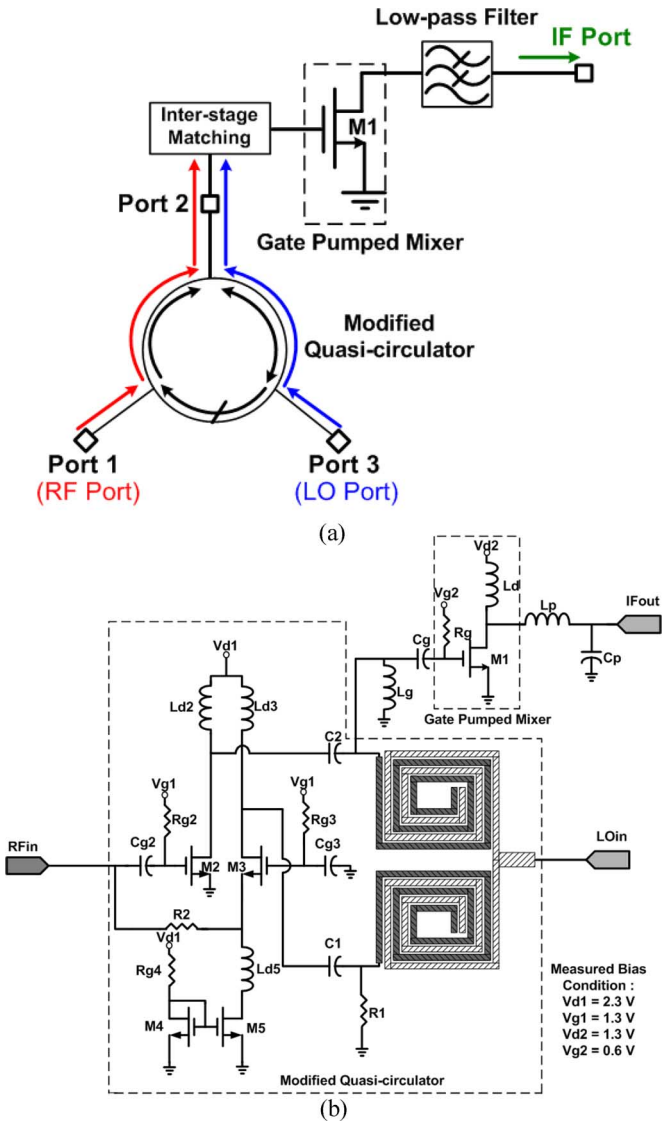

Fig. 9. (a) Schematic diagram and (b) detailed circuit configuration of the proposed CMOS SHM.

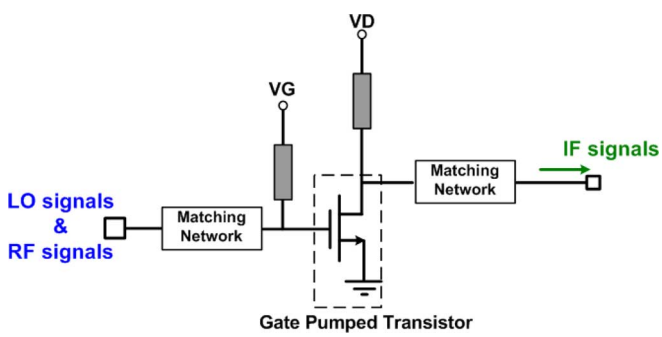

Fig. 10. Operation principle of the down-converted gate-pumped mixer.

the gate voltage $V_{\rm GS}$ and the LO amplitude $V_{\rm LO}$. Moreover, the simulated fundamental suppression of the proposed SHM for the down-converter mode is shown in Fig. 11. In the operation bandwidth range of 21–40 GHz, the fundamental suppression is higher than 16 dB.

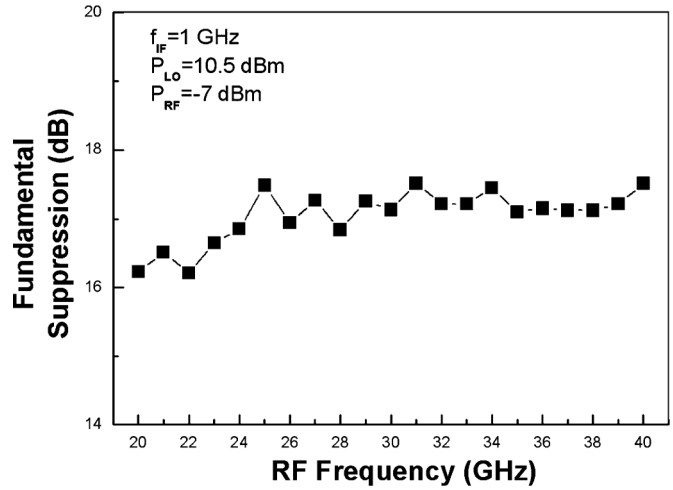

Fig. 11. Fundamental suppression as a function of RF frequency at an LO level of 10.5 dBm and IF of 1 GHz.

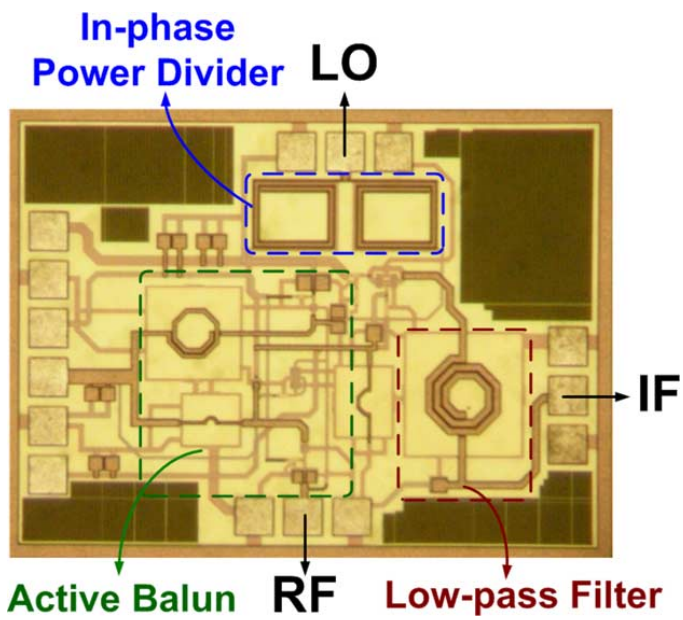

Fig. 12. Photograph of the fabricated subharmonic gate-pumped mixer. The chip dimensions, including the contact pads, are 0.92 × 1.05 mm^2.

III. Mixer Implementation and Results

An Agilent ADS corresponding to a TSMC design kit was employed for circuit simulation. These individual components were combined in a harmonic-balance simulator to optimize the mixer performance. Five nMOSFETs with f_T and $f_{\max}$ higher than 60 and 55 GHz, respectively, were used to construct the proposed SHM. In a practical circuit design, a tradeoff for the operation bandwidth and conversion loss of the proposed SHM is needed. The CMOS of the 26-finger nMOS M1 device with a gate width of 208 μm was used, as shown in Fig. 9(b). The gate bias of this gate pumped mixer was set to 0.6 V. The drain voltage Vd2 was set to 1.3 V through an inductor Ld (1.004 nH). To maintain the flatness insertion loss and same magnitude of signals with the out-phase active balun at operation bandwidth, the resistor R_1 (500 Ω) was selected. Four capacitors, C1, C2,

TABLE II
CIRCUIT PARAMETERS OF THE PROPOSED SHM

Components	Parameters	Components	Parameters
M1	208/0.18 μm/μm	Ld	1.004 nH
M2	64/0.18 μm/μm	Ld2	0.15 nH
M3	16/0.18 μm/μm	Ld3	0.5 nH
M4 and M5	72/0.18 μm/μm	Ld5	0.12 nH
C1	1.23 pF	Lg	0.2 nH
C2	0.14 pF	Lp	0.13 nH
Cg	1 pF	R1	500 Ω
Cg2	1 pF	R2	1.15 kΩ
Cg3	2 pF	Rg	464 Ω
Cp	0.83 pF	Rg2	173.5 Ω
Rg3	100 Ω		

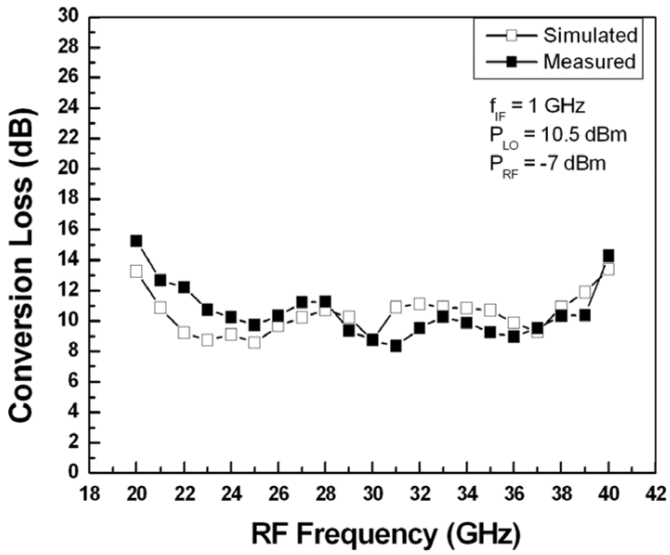

Fig. 13. Conversion loss as a function of RF frequency at a fixed LO power of 10.5 dBm and 1-GHz IF.

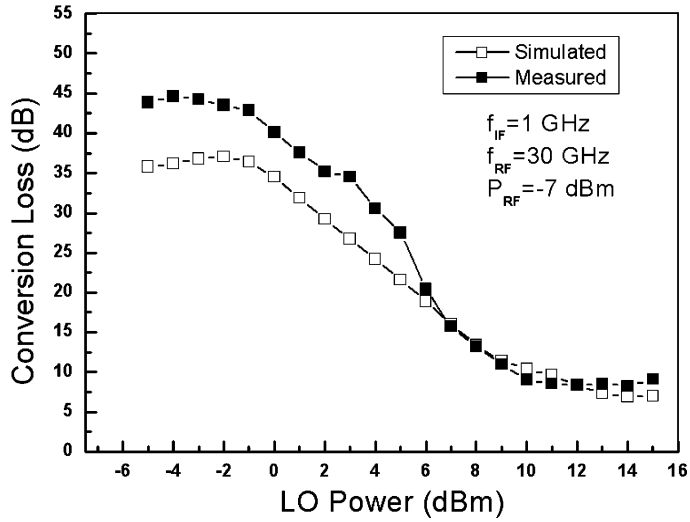

Fig. 14. Measured and simulated conversion losses as a function of LO power at an RF power level of −7 dBm.

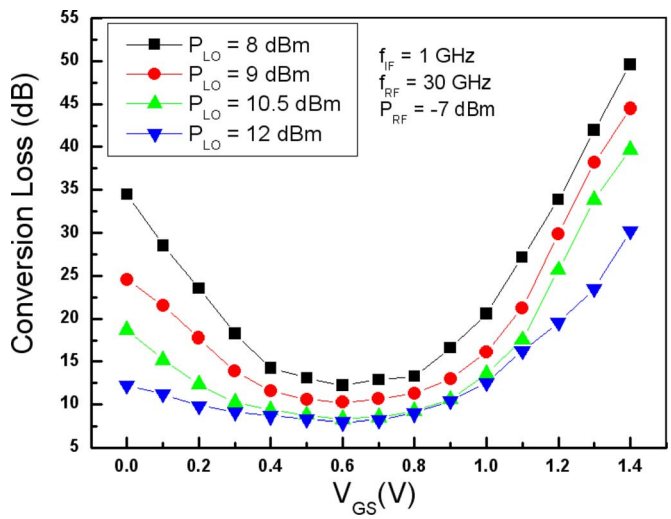

Fig. 15. Measured conversion loss versus $V_{\rm GS}$ with different LO powers at an RF power level of −7 dBm.

Cg2, and Cg3, were the dc-blocking capacitors of the power divider, RF port, and gate port of M3, respectively.

The passive components of the inductors, capacitors, and resistor were simulated by ADS RF Momentum. Finally, the used devices and components parameters of the proposed SHM are listed in Table II. The proposed MMIC mixer was fabricated using a TSMC standard 0.18-μm 1P6M CMOS process, as shown in Fig. 12. The chip size, including the testing pads, is 0.92 mm × 1.05 mm. The core chip dimension, excluding the contact ground–signal–ground (GSG) testing pads, is only 0.62×0.78 mm^2.

Measurement signals were obtained from the coplanar GSG on a wafer probe measurement system based on the Agilent E4446A spectrum analyzer calibrated with the E44198 power meter. The losses of the probes and cables were calibrated by a PNA E8364A network analyzer. In the mixer measurement, the LO drive power level was set to 10.5 dBm, and the RF power level was set to approximately −7 dBm to achieve optimum performance with a dc power consumption of 74.6 mW, 46.6 mW of which comes from the active balun. Fig. 13 illustrates the measured and simulated conversion losses of the SHM as a function of RF for the down-converter mode. The obtained conversion loss was from 8.3 to 14.2 dB within the RF bandwidth range of 21–40 GHz.

Fig. 14 shows the measured and simulated conversion losses as a function of LO power level at an RF frequency of 30 GHz and input power of −7 dBm. A significant mixing effect of an LO drive power level of 8 dBm is observed. The best conversion loss is 8.23 dB at an LO power level of 12 dBm.

Fig. 15 shows the conversion loss versus gate bias of M1 with different LO powers for the SHM. The proposed SHM has the lowest conversion loss at $V_{\rm GS} = 0.6$ V and an LO power level of 12 dBm. Moreover, the $V_{\rm GS}$ and LO power changes seriously affect conversion loss performance. Thus, the gate voltage $V_{\rm GS}$ and the LO amplitude $V_{\rm LO}$ are both affected by G_C performance, as discussed in Section II.

The measured and simulated LO-to-RF, LO-to-IF, and RF-to-IF isolations of the proposed SHM for the down-converter mode are shown in Fig. 16. In the operation bandwidth range of 21–40 GHz, the RF-to-IF isolation is higher than

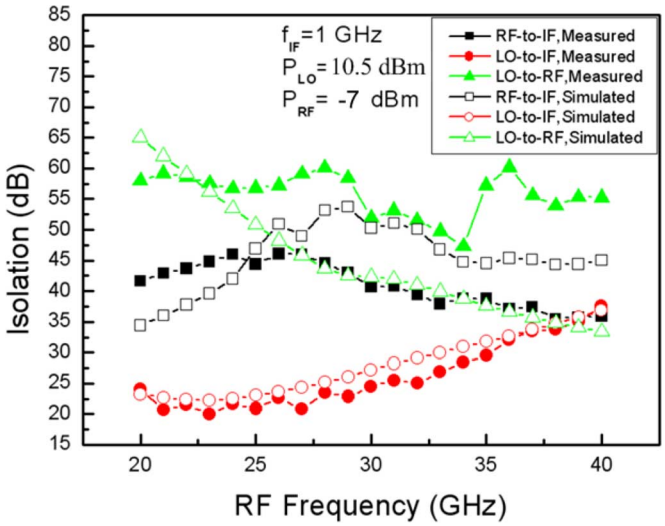

Fig. 16. Isolation as a function of RF frequency at an LO power level of 10.5 dBm and IF frequency of 1 GHz.

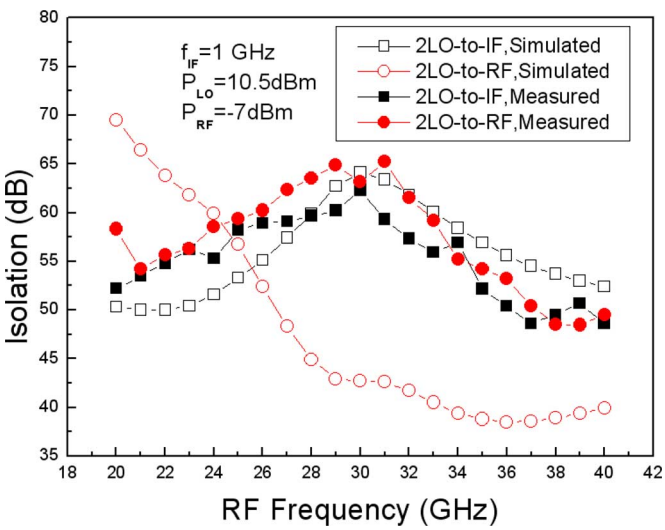

Fig. 17. Measured 2LO-to-RF and 2LO-to-IF isolations as functions of RF frequency at an LO power level of 10.5 dBm and IF frequency of 1 GHz.

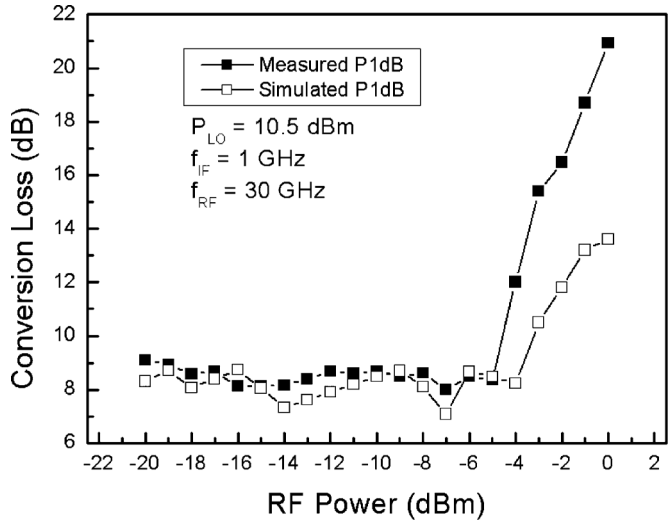

Fig. 18. Measured and simulated conversion losses versus the RF power level at a fixed RF frequency of 30 GHz and LO drive power level of 10.5 dBm.

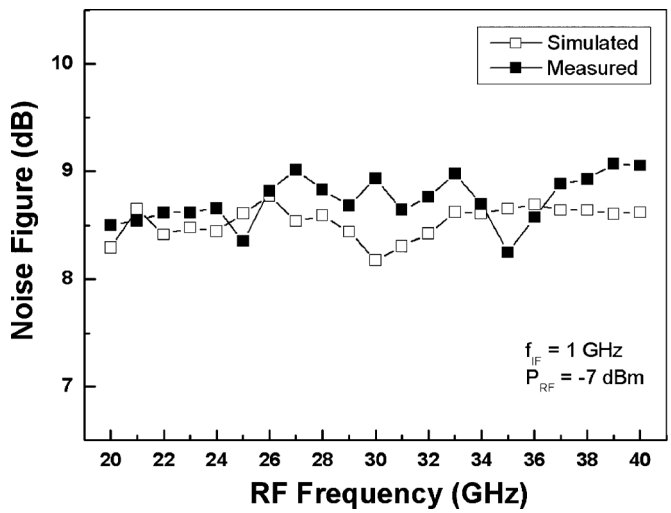

Fig. 19. Measured and simulated NF of the SHM as functions of RF frequency at an IF frequency of 1 GHz.

40 dB, and the LO-to-IF isolation is higher than 21 dB. The LO-to-RF isolation also greatly benefits from the modified QCM structure and exceeds 50 dB at a bandwidth range of 21–40 GHz. The limitation for this mixer may be partly because of the active balun. From the simulated results in Fig. 8, the active balun is a tradeoff between insertion loss (S_{21}) and isolation (S_{12}). The active balun also has relatively high insertion loss, which results in high conversion loss due to the design of the high LO-to-RF isolation level.

The 2LO-to-RF and 2LO-to-IF isolations as functions of RF frequency are illustrated in Fig. 17. The 2LO-to-IF isolation in the operating band range of 21–40 GHz is from 48.6 to 62.3 dB, and the 2LO-to-RF isolation is greater than 48 dB in the RF operational bandwidth. In addition, the measured results exhibit a 1-dB compression point of -4 dBm when the RF is fixed at 30 GHz, IF is fixed at 1 GHz, and at an LO power level of 10.5 dBm, as shown in Fig. 18. Fig. 19 shows the measured and simulated NF of the SHM as functions of RF frequency at an IF of 1 GHz. The NF of the proposed SHM ranges from 8.2 to 9.2 dB at an RF in the range of 20–40 GHz.

TABLE III
COMPARISON OF REPORTED SHMs

Ref.	Tech.	RF (GHz)	LO-to-RF iso. (dB)	Chip Size (mm^2)	LO Power (dBm)	Conversion Loss (dB)
[2]	0.15μm GaAs	23–37	22	0.72	12	9.4–12
[3]	0.18μm CMOS	10–40	12–20	0.837	8	15–17.6
[4]	0.13μm CMOS	32–70	23–33	0.36	13	11–13
[5]	90nm CMOS	9–31	>17	1	9.7	12–15
[6]	0.18μm CMOS	24–30	32–40	0.3	13	11–13
[9]	0.13μm CMOS	28–50	37	0.61	7	9.6–11
Present study	0.18μm CMOS	21–40	50–63	0.48[+]	10.5	8.2–14.3

[+] CORE CHIP SIZE

The deviation between the simulated and experimental results can be attributed to the process variation of CMOS, which causes the shift in the matching point in the circuit. The other reason for the deviation is attributed to the accuracy of the transistors with a nonlinear large signal model, which results in large deviations in the mixing. Table III compares the performance of the proposed SHM with those of other reported SHMs. The very high LO-to-RF isolation with broad bandwidth of the proposed SHM is excellent compared with that of the reported MMIC SHMs.

IV. Conclusion

A monolithic SHM with a broadband between 21–40 GHz constructed using 0.18-μm CMOS technology has been presented. Given the modified quasi-circulator, the proposed SHM not only has wide bandwidth performance, but also excellent port-to-port isolation. Based on the measured results, the proposed SHM exhibits good conversion loss, ranging from 8.2 to 14.3 dB, and excellent LO-to-RF isolation, ranging from 50 to 63 dB, for an RF bandwidth between 21–40 GHz with a miniature chip dimension of 0.48 mm^2. Therefore, the proposed SHM with a modified quasi-circulator is very suitable for RF front-end applications.

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