A Compact 275–320-GHz Reflection-Type Phase Shifter

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***Abstract*— This letter presents a WR-3.4-band reflection-type phase shifter (RTPS) in a 250-nm InP double heterojunction bipolar transistor (DHBT) technology. A reflective load with an L-section network is implemented using a diode-connected transistor, a transmission line, and a shunt capacitor. The reference impedance of the reflective load is set to a low impedance of 30 Ω, thus leading to a low-loss variation over a wide operating bandwidth. To minimize the chip area, a quadrature hybrid for combining reflected signals is implemented using a compact broadside coupled-line coupler. The measurement shows that the RTPS provides a continuous 180° phase shift with an average insertion loss of 9.9–10.9 dB over a frequency range from 275 to 320 GHz. The loss variation is only 1 dB. The root-mean-squared (RMS) amplitude and phase errors maintain below 2.9 dB and 7.3°, respectively. The chip size including all probing pads is as small as 0.37 × 0.46 mm^2, and the core size is only 0.02 mm^2. The dc power consumption is zero.**

***Index Terms*— InP double heterojunction bipolar transistor (DHBT), phased array, reflection-type phase shifter (RTPS), subterahertz, WR-3.4 band.**

I. Introduction

A WIDE bandwidth available in the subterahertz band is drawing attention for high-speed wireless links and post-5G communications. For example, IEEE 802.15.3d, which is the first standard released for consumer wireless communications in the subterahertz band, offers data rates of 100 Gbps and higher at distances up to a few hundred meters [1]. In addition, a subterahertz wireless link has been proposed for space, satellites, and unmanned vehicles [2], [3].

Nonetheless, subterahertz links suffer from high free-space path loss (FSPL) and high atmospheric absorption in contrast with the low-frequency spectrum. This results in an extremely tight link budget for wireless communications over medium and long distances. A phased array is widely adopted to overcome the tight link budget. By employing N antennas, the effective isotropic radiated power in the transmitter and the signal-to-noise ratio in the receiver are improved by a factor of $20\log N$ and $10\log N$, respectively. Given that the FSPL increases with the square of the frequency, a large N is required to support a reasonable link budget in the subterahertz band. To implement such a massive phased-array system in practice, each array channel including a phase shifter should be designed with low dc consumption and compact chip size.

Several topologies of phase shifters have been reported in the WR-3.4 band [4]–[10]. However, most phase shifters adopt an active topology that consumes significant dc power [4]–[7]. Nonetheless, most of the active phase shifters fail to provide gain due to the limited transistor speed or passive loss. In contrast, a reflection-type phase shifter (RTPS) has the advantages of zero dc power consumption and a continuous phase shift with only a few control voltages. However, in the WR-3.4 band, the RTPS usually suffers from a narrow bandwidth and a high insertion loss [8]. To compensate for the loss and improve the bandwidth, a variable gain amplifier can be added at the expense of dc power and large chip area consumption [9]. The RTPS reported in [10] suffers from a small phase shift range of 118°. For a full 360° coverage, this demands an additional phase shift component achieving a range significantly larger than 180°, which would consume additional dc power and chip area.

This letter presents a compact and wideband RTPS that provides a 180° phase shift in the WR-3.4 band. The chip size is reduced by adopting a broadside coupled-line hybrid coupler and an inverted microstrip structure. An L-section reflective load with 30-Ω reference impedance enables a 180° phase shift with low average loss variation over a wide bandwidth.

II. WR-3.4 RTPS Design

Fig. 1 shows a schematic of the proposed RTPS. It consists of a quadrature hybrid coupler and two identical reflective loads. The reflective load employs a diode-connected transistor (Q_1) as a varactor and an L-section network (TL_4 and C_2) to extend the phase shift range. The emitter length of Q_1 is chosen to be 6 μm, which is the maximum length provided by the foundry, for a large capacitance variation. In Fig. 2, the simulated impedance trajectories from Z_a to Z_d at 280 GHz are depicted as the control voltage of Q_1 (V_{ctrl}) varies from −0.5 to 0.5 V. The reference impedance of the Smith chart is 30 Ω. According to Z_a, the varactor Q_1 presents a capacitance ranging from 8.2 to 132 fF with a Q-factor of 1–14.4. This results in a phase shift range of only 94°. Therefore, a transmission line (TL_4) and a shunt capacitor (C_2) are connected to extend the range to 185°, as shown in Z_c in Fig. 2.

To minimize the insertion loss variation of the RTPS between the phase states, the reflective load is supposed to maintain a constant magnitude of the reflection coefficient

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TABLE I

PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART PHASE SHIFTERS IN THE WR-3.4 BAND

Reference	Technology	Topology	Frequency (GHz)	Resolution	Min. phase shift range (deg)	Average gain (dB)	Average gain variation (dB)	RMS amplitude error (dB)	RMS phase error (deg)	P_{dc} (mW)	Size (mm^2)
[4]	0.13-μm SiGe	VSPS	220–250	Cont.	360	-8 @ 235 GHz	–	–	–	105.6	–
[5]	250-nm InP	VSPS	220–320	Cont.	360	-15.6 – -11.8	3.8	<1.2	<10.2	21.8–42.0	0.23
[6]	50-nm GaAs	VSPS	240–270	Cont.	360	-4.5	–	<1.8	<12.5	<13.7	1.25
[7]	35-nm GaAs	STPS	235–279	2-bit	360	0.22 @ 267 GHz	3	<0.18	<2.8	50.4	0.21*
[8]	50-nm GaAs	RTPS	245–255	Cont.	145	-13.6 – -11.5	2.1	–	–	0	0.56
[9]	50-nm GaAs	RTPS	218–268	Cont.	205	-4.6 – -1.6	3	<1.5	<10.4	28.4	0.56
[10]	50-nm GaAs	RTPS	214–276	Cont.	118	-7.8 – -7**	0.8	<0.67	<5.6	0	0.25
This work	**250-nm InP**	**RTPS**	**275–320**	**Cont.**	**180**	**-10.9 – -9.9**	**1**	**<2.9**	**<7.3**	**0**	**0.17 0.02***

*Core size excluding the probing pads, **Read from a plot in the article

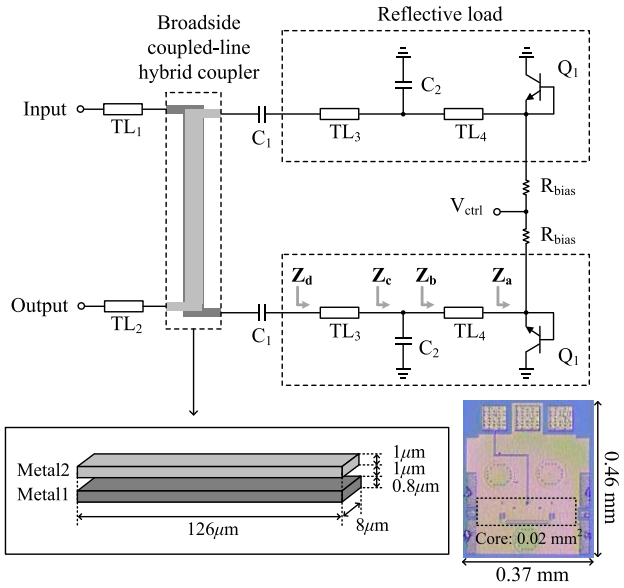

Fig. 1. Schematic and chip photograph of the proposed RTPS.

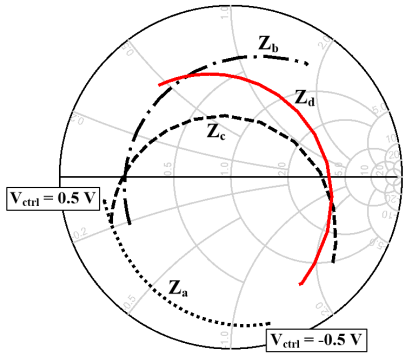

Fig. 2. Impedance trajectory at each node of the reflective load at 280 GHz as V_{ctrl} varies from −0.5 to 0.5 V. The Smith chart is normalized to 30 Ω.

over V_{ctrl}. However, Z_c in Fig. 2 presents a reflection coefficient with a significant variation in magnitude. To reduce the variation, a short transmission line (TL_3) is added, so that the trajectory of Z_d rotates around the center of the Smith chart.

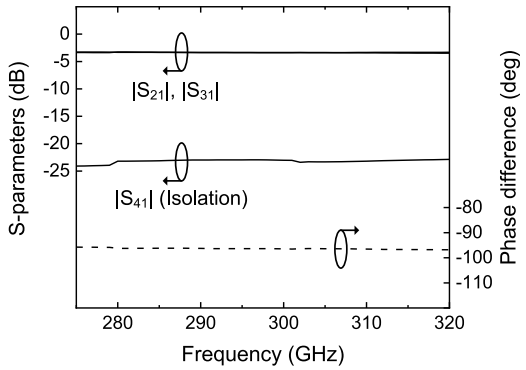

Fig. 3. Simulated performance of the quadrature hybrid coupler.

Therefore, the reflection coefficient of the load is maintained at a constant magnitude with respect to 30 Ω. Furthermore, it is found from the simulation that the load reflection coefficient keeps a low magnitude variation over the operating frequency range. Given that the reflective load operates with reference to 30 Ω, the quadrature hybrid coupler is also designed with an identical 30-Ω port impedance. This avoids an extra impedance matching network between the coupler and the reflective load, which would otherwise limit the operation bandwidth and increase the loss of the RTPS. Instead, quarter-wave lines (TL_1 and TL_2) as short as 125 μm at 300 GHz are added at the input and output of the RTPS for 50-Ω matching.

The 30-Ω quadrature hybrid coupler is implemented using a broadside coupled-line structure with two metal layers (M1 and M2), as shown in Fig. 1. Compared with a branch-line coupler or a Lange coupler, this structure occupies a smaller chip area. In addition, the coupler and transmission lines are realized using an inverted microstrip structure [11], which further reduces the chip size compared with other RTPSs implemented using a coplanar waveguide (CPW) structure [8]–[10]. In Fig. 3, the simulated $|S_{21}|$ and $|S_{31}|$ of the coupler range from −3.5 to −3.3 dB over the frequency from 275 to 320 GHz, while the isolation is higher than 23 dB. The phase difference ranges from 95° to 96°.

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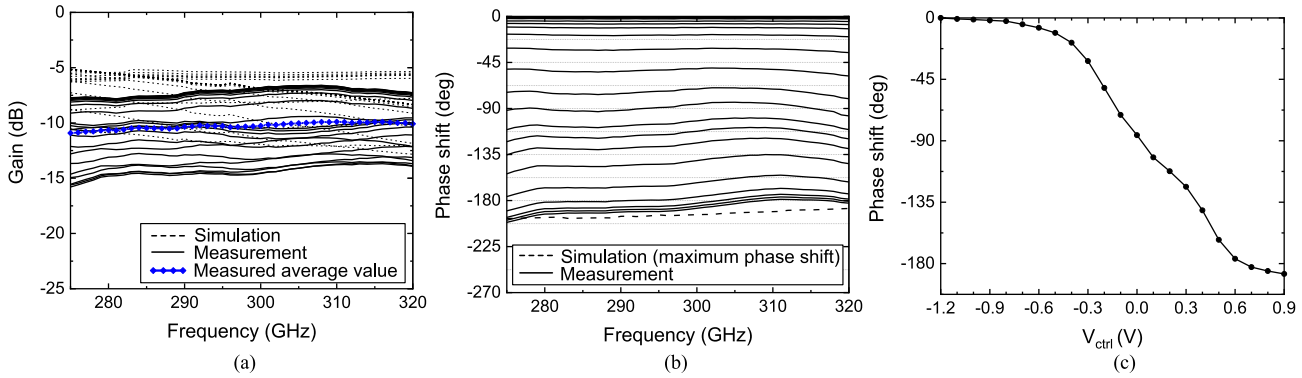

Fig. 4. Measured (a) gain, (b) phase shift versus frequency, (c) phase shift versus V_{ctrl} at 300 GHz as V_{ctrl} is varied from −1.2 to 0.9 V with a 0.1-V step.

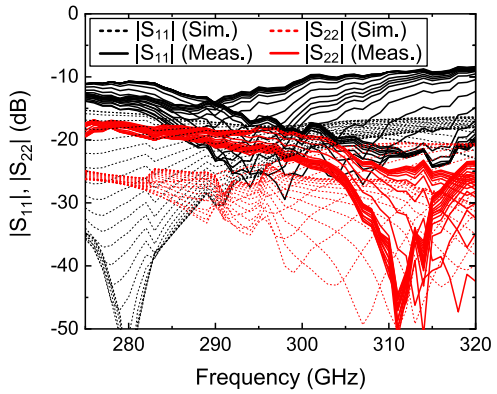

Fig. 5. Measured input and output matching performance.

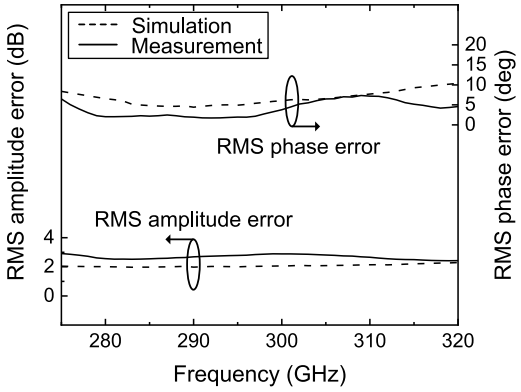

Fig. 6. Measured RMS amplitude and phase errors.

III. Measurement Results

The WR-3.4 RTPS was fabricated in a 250-nm InP DHBT technology. The chip micrograph is shown in the inset of Fig. 1. The chip area is 0.37 × 0.46 mm^2 including all probing pads and the core size is as compact as 0.02 mm^2. The *S*-parameters were measured on-wafer with a Keysight N5227A network analyzer and VDI WR-3.4 extension modules.

Fig. 4(a) presents the measured gain of the RTPS as V_{ctrl} is varied from −1.2 to 0.9 V. It should be noted that the range of V_{ctrl} is extended in the measurement compared with the simulation but is still within the safe operating region. The average gain ranges from −10.9 to −9.9 dB, resulting in only 1-dB variation over a frequency range from 275 to 320 GHz. The discrepancy between the measurement and simulation presumably originates from underestimated parasitic resistance and inductance in the transistor model. The measured phase shift versus the frequency and versus V_{ctrl} at 300 GHz are shown in Fig. 4(b) and (c), respectively. A continuous phase shift of at least 180° is achieved from 275 to 320 GHz. The simulation of the maximum phase shift is superimposed in dashed line, which agrees well with the measurement.

The matching performance at the input and output ports is shown in Fig. 5. The return loss is better than 8.4 and 16.8 dB at the input and output, respectively, from 275 to 320 GHz. Fig. 6 shows the root-mean-squared (RMS) amplitude and phase errors of the RTPS, which are 2.8 dB and 1.9°, respectively, at 290 GHz. The RMS errors maintain below 2.9 dB and 7.3° from 275 to 320 GHz.

In Table I, the proposed RTPS is compared with the state-of-the-art phase shifters in the WR-3.4 band. Unlike active phase shifters [4]–[7], this work consumes no dc power while presenting a decent insertion loss. Compared with other RTPSs [8]–[10], this work first provides a phase shift that exceeds 180° over a wide bandwidth in the upper WR-3.4 band utilized in the IEEE 802.15.3d standard. The average gain variation over the operation frequency range is as low as 1 dB. Finally, the proposed RTPS occupies the smallest chip area, which, along with zero dc power consumption, should be beneficial for the implementation of a massive phased-array system.

IV. Conclusion

A subterahertz RTPS was implemented in a 250-nm InP DHBT technology. By employing a reflective load based on an L-section network with a 30-Ω reference, the RTPS achieves a continuous phase shift of 180° and an average loss of 9.9–10.9 dB from 275 to 320 GHz. The compact design of a quadrature hybrid coupler and transmission lines accomplishes the smallest chip size among state-of-the-art phase shifters in the WR-3.4 band. The proposed RTPS would be suitable for massive phased-array systems in the subterahertz band owing to the zero dc power consumption and compact size.

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