A 240 GHz Fully Integrated Wideband QPSK Receiver in 65 nm CMOS

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***Abstract*—Operation at millimeter-wave/sub-terahertz frequencies allows one to realize very high data-rate transceivers for wireless chip-to-chip communication. In this paper, a 240 GHz 16 Gbps QPSK receiver is demonstrated in 65 nm CMOS technology. The receiver employs a direct-conversion mixer-first architecture with an integrated slotted loop antenna. A 240 GHz LO chain drives the passive mixers to down-convert the modulated data to baseband. The baseband signal is then amplified using high gain, wide bandwidth amplifiers. The receiver has a noise figure of 15 dB with a conversion gain of 25 dB calculated from measurement data. The receiver achieves a data rate of 10 Gbps (with BER $< 10^{-6}$) and a maximum data rate of 16 Gbps (with BER of 10^{-4}) with a receiver efficiency of 16 pJ/bit.**

***Index Terms*—Baseband amplifier, BPSK, communication system, delayed transmission line, direct conversion, frequency doubler, frequency tripler, high data rate, injection-locked oscillator, mixer-first architecture, on-chip slotted loop antenna, QPSK, receiver, sub-millimeter-wave, sub-terahertz, wideband, 240 GHz.**

I. Introduction

THERE are many wide and unallocated frequency bands in the millimeter-wave/sub-terahertz frequencies (above 100 GHz) that are attractive for wideband applications. Operation at these high frequencies allows one to achieve very high data rates for wireless chip-to-chip communication applications. Additionally, the wavelength at sub-terahertz frequencies is of the order of 1 mm, such that antennas can be integrated onto the same chip as other transceiver circuits, thereby reducing the overall form factor and obviating expensive off-chip packaging. However, the receiver design is faced with numerous challenges especially in finer CMOS technology nodes. CMOS technology has dominated digital and mixed-signal integrated circuits because of its good switching performance and low cost. Processors or memories can be integrated on the same chip with a receiver, and the received data can be quickly processed and stored. In addition, high-frequency circuits can be digitally controlled and calibrated. Despite these advantages, the CMOS receiver design is faced with many challenges. The cut-off frequencies (f_T, f_{max}) that are typically between 200 GHz and 300 GHz are relatively lower than for other technologies [1]. This directly affects the achievable sensitivity of the receiver. The reduced breakdown voltages also restrict the conversion gain of front end down-conversion circuits due to limited LO swing. The low quality factors of the passive devices also affect the receiver performance. The implementation of an efficient receiver thereby requires ideas both at the circuit and system level.

Several receiver architectures and building blocks [2]–[7] have been demonstrated in literature. In [2], a 260 GHz heterodyne on-off keying (OOK) receiver is proposed in 65 nm CMOS technology. The receiver has a simulated gain of 17 dB with a noise figure of 19 dB. In [3], receiver blocks operating at 220 GHz and 320 GHz are demonstrated. However, the achieved noise figure numbers are substantially high. An in-phase/quadrature-phase (I/Q) direct-conversion receiver operating at 240 GHz implemented in 0.13 μm BiCMOS is demonstrated in [4]. The receiver achieves 18 dB of conversion gain with double-sideband (DSB) noise figure of 18 dB. A heterodyne receiver with a RF frequency of 283 GHz is implemented in 65 nm CMOS [5]. It uses a 282 GHz carrier, thereby achieving limited operation bandwidth and a significantly high noise figure of 38 dB. In [6], a 200 GHz downconverter is demonstrated in 90 nm CMOS with data rates of 4 Gbps. However, the antenna is not integrated onto the die. Although the above receiver designs advance the state-of-the-art, none of them demonstrate a completely functional link with a transmitter (with measured eye diagram and bit error rates) at these operating frequencies. In this paper, we discuss the design of a 240 GHz sub-terahertz receiver in 65 nm CMOS technology [8]. The receiver performs coherent demodulation including binary phase shift keying (BPSK) and quadrature phase shift keying (QPSK) and operates up to a maximum measured data rate of 16 Gbps (with an efficiency of 16 pJ/bit). Together with [9], [10], this work demonstrates the first fully functional sub-terahertz link in CMOS technology.

The rest of the paper is organized as follows. Section II describes the challenges and considerations in the sub-terahertz receiver design. Section III discusses the receiver architecture in detail. Section IV covers the detailed aspects of the receiver blocks along with the tradeoffs in their design. Section V describes the measurement results and conclusions are given in Section VI.

II. Receiver Design Considerations

In typical receivers, a low-noise amplifier (LNA) is employed at the front-end to minimize the noise figure. However, the gain of the amplifier is severely limited while operating close to the cut-off frequencies (f_T/f_{max}) of the technology. Hence, the

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down-conversion must be performed upfront, thereby making the design a mixer-first architecture. The down-conversion process at the front-end also results in significant loss. The minimum detectable signal is limited by this conversion loss, the noise figure of the chain and the channel attenuation. These metrics must be optimized in the receiver design. Additionally, the bandwidth of the receiver must be sufficiently wide to process the high-data-rate modulated data. Additionally, since there are no standards at this frequency, no blockers or jammers are assumed. Hence, the intermodulation distortion/linearity of the receiver is not of concern. However, this would become important in the future or when complex modulation schemes such as Orthogonal Frequency division multiplexing (OFDM) are implemented. Several receiver architectures are discussed below.

A. Diode-Based Receiver

Diodes are widely used in optical receivers. In [11], [12], a Schottky barrier diode has been used to detect millimeter-wave signals. The cut-off frequency f_{cutoff} of the Schottky diode is given as $f_{cutoff} = 1/(2\pi R_s C_o)$ [11], where R_s is the series resistance, and C_o is the sum of the zero-bias junction capacitance and parasitic capacitance. The cut-off frequency of the diode is as high as 2 THz in 130 nm CMOS process, and the cut-off frequency can go beyond 3 THz in advanced CMOS processes. In [12], a 280 GHz detector using a Schottky diode is demonstrated. Amplitude modulation has been implemented with a modulation frequency of 1 MHz. For a received power of 0.33 μW (-35 dBm), the output rms voltage is 11.9 mV. The noise equivalent power (NEP) is estimated at 36 $\mathrm{pW}/\sqrt{Hz}$, which is dominated by the flicker noise. For multi-Gbps communications, this responsivity is insufficient and must be improved. Additionally, a wideband design is needed.

B. Self-Mixer

One could also self-mix the input signal as shown in Fig. 1(a) to demodulate the data. The self-mixer consists of one or two transistors. Additionally, an LO signal is not required; thus, the design is simple, the power dissipation is low, and the mixer occupies lesser area. However, this topology suffers from various issues. It requires high signal power to demodulate the data and the self-mixing process results in an output swing that is proportional to the square of the amplitude. Additionally, self-mixing can be used only for ASK (amplitude-shift keying) or OOK (on-off keying) modulation schemes.

C. Sub-Harmonic Mixer

Fig. 1(b) shows a sub-harmonic mixer architecture. In this topology, the mixer is driven using N phases of the LO signal to down-convert the N^{th} sideband to intermediate frequency (IF). This relaxes the LO generation scheme as a lower LO frequency is generated. However, the conversion gains of the N-push operation and the mixer itself should be taken into account. Analysis of the N-push operation shows that the conversion gain is low for N greater than two. The mixer is also lossy when the RF frequency exceeds f_T/f_{max}. Thus, the overall conversion gain of the sub-harmonic mixer is limited. The noise figure is accordingly higher. Additionally, the device size is small at these high frequencies. The resulting transistor mismatch degrades the N-push operation and the mixer performance.

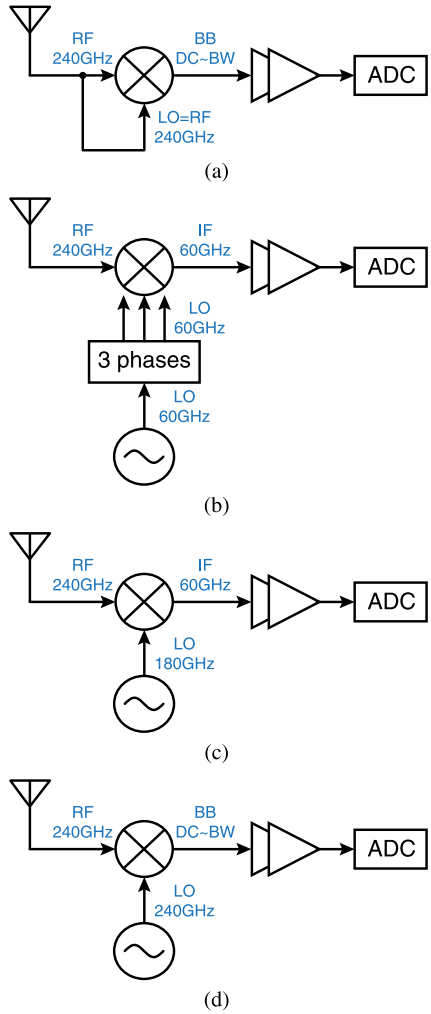


Fig. 1. Receiver architecture (a) with a self-mixer (b) with a sub-harmonic mixer (c) with a heterodyne conversion mixer (d) with a direct-conversion mixer.

D. Heterodyne Mixer

Fig. 1(c) shows a heterodyne mixer operating from an RF signal at 240 GHz. It is driven using 180 GHz LO signal resulting in an IF of 60 GHz [2]. Since the mixer down-converts the first sideband, it can potentially produce a high conversion gain and a low noise figure. However, a strong high-frequency LO is required in this case and its generation could be challenging in CMOS technology. A frequency doubler or tripler can be employed with a 90 GHz or 60 GHz power amplifier, respectively. Additionally, the IF must be chosen appropriately based on the required signal bandwidth. A high signal bandwidth results in a high IF and requires efficient wideband IF amplifiers that dominate the receiver power consumption.

E. Direct-Conversion Mixer

Fig. 1(d) shows a direct-conversion mixer, that is widely used for I/Q modulations such as BPSK, QPSK, and QAM. Only

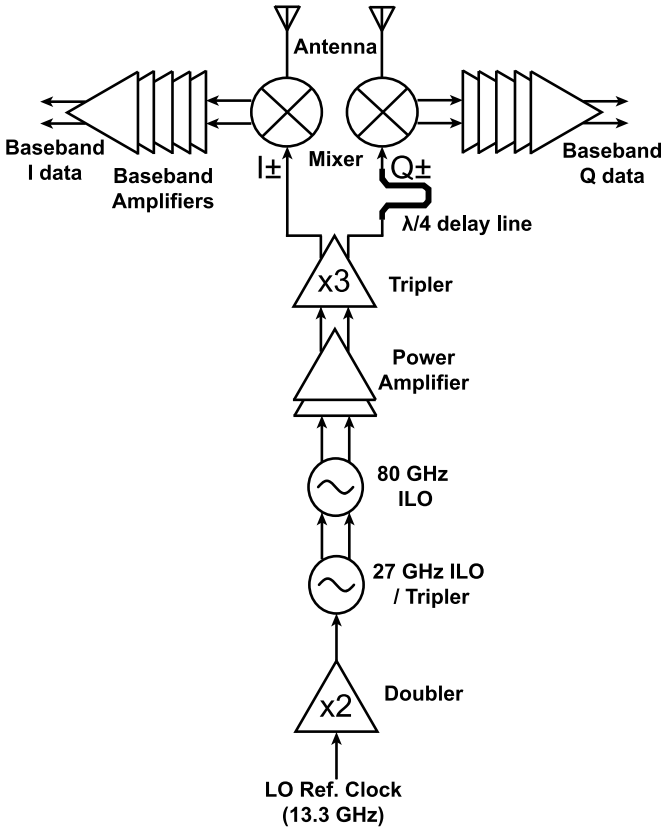


Fig. 2. Block diagram of the 240 GHz receiver.

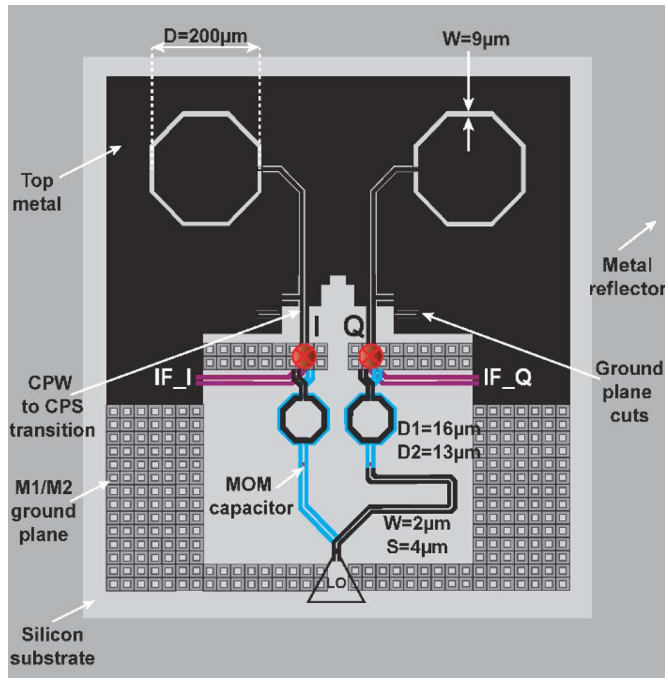


Fig. 3. Structure of the receiver slotted loop antenna (substrate thickness $=$ 300 μm).

one path (I or Q) is shown for simplicity. This direct-conversion architecture requires a higher LO frequency than the heterodyne mixer, but the IF design is relaxed. Because the IF is zero, baseband amplifiers can be employed at the mixer output to improve the power efficiency. The increased LO frequency can be addressed by increasing the multiplication ratio of the frequency multiplier or increasing the oscillator frequency with a fixed multiplication ratio. The mixer performance (the conversion gain and the noise figure) depends on the LO power, as in the case of heterodyne mixer.

III. Receiver Architecture

The receiver architecture is illustrated in Fig. 2 and is chosen based on the considerations discussed in the previous section. The transmitted 240 GHz signal is received using a slotted loop antenna. Each channel (I or Q) uses a separate slotted loop antenna to achieve better isolation. As the operation frequency is greater than the f_{max} of the technology, a front-end low noise amplifier (LNA) is not feasible in this design. Hence, the receiver employs a direct-conversion mixer-first architecture. A voltage-mode differential passive mixer operating from 240 GHz LO signal down-converts the received signal directly to baseband. Two oscillators are injection-locked to the 13.3 GHz input clock and the 80 GHz oscillator drives the amplifier chain, and then a frequency tripler. The I/Q quadrature phases are generated by a differential quarter-wave delayed line. Typically, a quadrature hybrid could be implemented in this case, but the insertion loss would be too high at 240 GHz. Moreover, the amplitude and phase mismatches of the delayed line are comparable to those of the hybrid because the delayed line design is much simpler and shorter at 240 GHz. The tripler has 80 and 160 GHz leakages, which are rejected by the delay lines and do not affect the mixer performance. The mixer output has a broadband response. The baseband amplifiers and a 50 Ω driver boost the voltage swing of the received signal to properly capture and measure the output. As the mixer is passive and has no gain, the noise of the baseband amplifiers contributes significantly to the overall noise figure of the receiver. Hence, a reasonable amount of power is spent in the first stage of the baseband amplifier to obtain an overall low noise figure for the receiver. The performance of the receiver is limited by the achievable noise figure and the overall bandwidth of the chain. In future designs, one could use equalization techniques to overcome the bandwidth limitation. Additionally, a single balanced mixer architecture could be implemented to reduce LO power thereby increasing efficiency. Finally, as technology scales a fundamental mode architecture would increase both the bit rate and the efficiency of the system.

IV. Building Blocks

In this section, we discuss the design of the major building blocks namely the 240 GHz antenna, the mixer, the 80 GHz LO chain, 240 GHz I/Q generation block and the baseband amplifiers. The details of the 80 GHz power amplifier and 240 GHz frequency tripler are given in [9], [10].

A. On-Chip Antenna

The structure of the receiver antenna consists of two slotted loop antennas as shown in Fig. 3. The substrate height is 300 μm and there was no die thinning. A metal reflector is used in order to generate a broadside radiation pattern. The I/Q channels each use a single antenna and are interfaced to

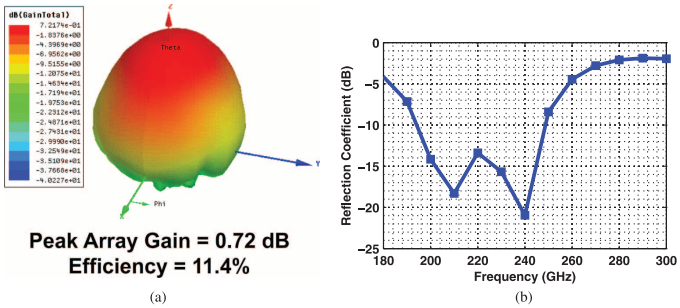


Fig. 4. Simulation results of the receiver antenna (a) gain pattern (b) input reflection coefficient (S_{11}).

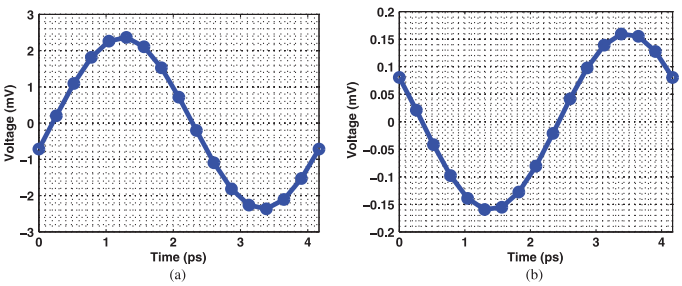


Fig. 5. Simulation results of the antenna-mixer interface (a) differential signal at the mixer RF ports (b) common mode signal at the mixer RF ports.

the mixer using co-planar waveguide (CPW) lines. To generate the required differential signals for the fully balanced mixer, a CPW to coplanar stripline (CPS) transition is made. In order to efficiently convert the CPW mode to the odd mode of the CPS (which is the desired mode), the common mode impedance of the CPS lines needs to be increased in comparison to the differential mode impedance. To achieve this, multiple cuts and serpentine layout is introduced along the periphery of the ground plane to increase the return path length, thereby increasing the common mode inductance. A 10° line is sufficient to generate the required differential signals. The mixer differential input also needs to be grounded for DC biasing. One of the signals of the CPS line is already connected to ground (CPW ground). To ground the other signal trace, a shorted stub is used to simultaneously achieve both DC biasing and impedance matching. The CPS lines are conjugate matched to the mixer impedance of 150 Ω||14 fF. Fig. 4(a) shows the simulated antenna pattern. The achieved gain per channel (I/Q) is −2.3 dBi with an efficiency of 11.4%. The input reflection coefficient S_{11} (shown in Fig. 4(b)) is less than −10 dB from 210 GHz to 250 GHz. Hence, the antenna has a bandwidth of 20 GHz centered around 240 GHz.

The complete link consisting of the transmitter [9], [10] and receiver is simulated for a link length of 1.5 cm. Here the receiver antennas were terminated using the mixer impedance at 240 GHz under switching conditions. Fig. 5 shows the simulated differential and common mode output of the RF ports of the fully balanced mixer. Due to the efficient mode conversion and careful layout of the ground plane, the common mode component is only 6.7% or −24 dB below the differential signal. Fig. 6 shows the simulated gain from the transmitter to both the channels of the receiver. For a 1.5 cm link, the path loss at this frequency is −43.5 dB. Including the antenna gain of 1.55 dB

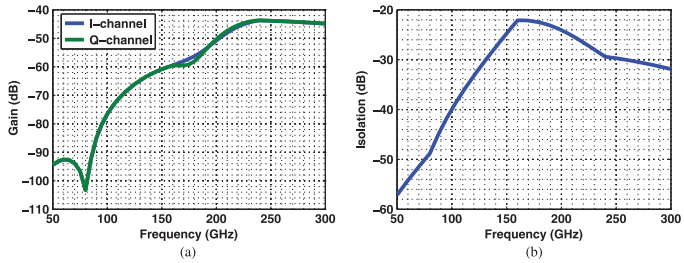


Fig. 6. Simulation results of the antenna-mixer interface (a) gain from Tx to Rx (b) isolation between the Rx antennas.

on the transmitter and −2.3 dB on the receiver, the gain is calculated to be around −44.3 dB at 240 GHz, which is close to the simulated value. The isolation between the receiver antennas (I and Q) is also plotted as a function of the frequency. The antennas have an isolation of −30 dB at 240 GHz which provides sufficient isolation between the I and Q channels.

B. 240 GHz Mixer

As discussed earlier, an LNA is not feasible in this receiver design. Hence, we employ a direct-conversion mixer-first architecture to demodulate the 240 GHz modulated signal. In an active mixer implementation, the input RF device does not provide any gain due to operation above f_{max} of the technology. This results in a much higher noise figure compared to a passive mixer implementation at the expense of higher power consumption. Hence, a passive mixer topology is used in this design. Fig. 7(a) shows the schematic of a fully balanced passive mixer. It consists of four transistors operating as switches. The transistors are driven by high swing LO signals that down-convert the RF signal v_{rf} fed from the antenna (with impedance R_a). The resulting IF signal is then filtered using the baseband impedance Z_{bb}. The transistor is modeled with a switch resistance R_{sw} and is driven by complimentary square wave signals $V_{LO}^{+} = A_{LO}s(t)$ and $V_{LO}^{-} = A_{LO}\overline{s(t)}$. Here A_{LO} is the amplitude of the switching waveform and $s(t)$ and $\overline{s(t)}$ are square wave signals. The baseband impedance Z_{BB} could either be purely capacitive or an RC filter. Typical analysis of current driven passive mixers is given in [13]. The output voltage here is given by the convolution of the IF differential current and the load impedance. When the transmitted RF signal is generated by modulating a real baseband waveform, the tones in the RF signal are symmetric about the carrier frequency i.e. every RF signal can be decomposed into a sum of two sinusoidal signal pairs around ω_{RF}. Hence, for analysis we assume $v_{rf} = A_{RF}\sin[(\omega_{RF}+\omega_m)t] + A_{RF}\sin[(\omega_{RF}-\omega_m)t]$. As the mixer is a linear time varying (LTV) system, we can find the resulting output waveforms by using superposition across different frequencies. The baseband output voltage is given as

$$v_{out}(\omega_m) = \frac{2}{\pi}\left[\frac{Z_{BB}(\omega_m)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega_m)}\right]A_{RF} \quad (1)$$

This is true as long as the baseband impedance filters the high frequency signals that include the up-converted mixer products. Hence, the baseband impedance can be purely capacitive in nature as long as the cut-off frequency is chosen to be lower than the operating LO frequency. The cut-off frequency of this

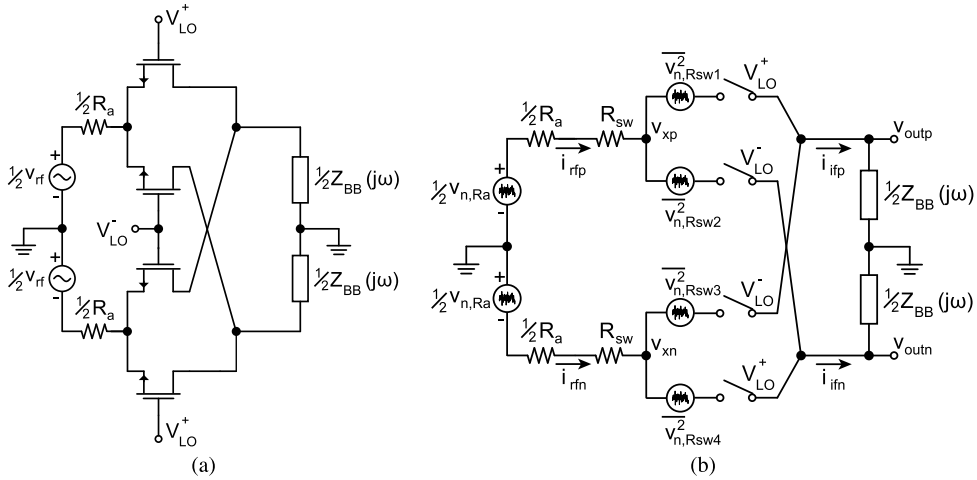


Fig. 7. (a) Schematic of fully balanced passive mixer (b) noise analysis of fully balanced passive mixer using the switch model.

filter is determined by the antenna and switch resistance and the value of chosen capacitance. The differential RF current $i_{rf} = (i_{rfp} - i_{rfn}/2)$ has two frequency components due to up-conversion from baseband. The RF differential impedance $R_{in,rf}$ at $\omega_{LO} + \omega_m$ and $\omega_{LO} - \omega_m$ is given as

$$R_{in,rf}(\omega_{LO}+\omega_m) = R_{in,rf}(\omega_{LO}-\omega_m) = \frac{R_a + 2R_{sw}}{1 - \frac{8}{\pi^2}\Re\left[\frac{Z_{BB}(\omega_m)}{0.5R_a+R_{sw}+0.5Z_{BB}(\omega_m)}\right]} \quad (2)$$

The analysis shown above assumes a square wave LO drive and ideal switching of the transistors. However, due to the high frequency of operation and sinusoidal LO drives, the conversion gain of the mixer is low. The term $8/\pi^2$ in (2) is related to the conversion gain of the mixer. Operating at these high frequencies leads to a lower conversion gain and this leads to an input resistance $R_{in,rf} \approx R_a + 2R_{sw}$.

We now estimate the noise figure of the passive mixer. As a simplification, we now consider the noise contribution only from the first sideband and compute the noise figure of the mixer. Consider the schematic of the passive mixer with the noise sources shown in Fig. 7(b). We will assume that the load impedance Z_{BB} is mostly capacitive in nature and thus its noise contribution can be ignored. Hence, there are mainly two noise sources, one from the antenna impedance (or the input noise source) modeled as v_{n,R_a} and the other from the transistor resistance R_{sw} modeled as $v_{n,R_{sw}}$. The output noise spectral density due to the switch resistances $S_{vout,R_{sw}}$ is calculated as

$$S_{vout,R_{sw}} \approx 4\left[(0.5)^2 + 2\left(\frac{1}{2}.\frac{2}{\pi}\right)^2\right] \times \left|\frac{0.5Z_{BB}(\omega)}{0.5R_a + R_{sw} + 0.5Z_{BB}(\omega)}\right|^2 (4kTR_{sw}) \quad (3)$$

The factor of $1/2$ is due to the sinusoidal multiplication and the factor of 2 is due to two sidebands (signal and image bands). The output noise spectral density due to the input $S_{vout,R_{sw}}$ is calculated using the baseband voltage gain and is given as

$$S_{vout,R_a} \approx \left(\frac{1}{2}.\frac{4}{\pi}\right)^2 \left|\frac{0.5Z_{BB}(\omega)}{0.5R_a+R_{sw}+0.5Z_{BB}(\omega)}\right|^2 (4kTR_a) \quad (4)$$

Hence, the noise factor F is calculated to be $F \approx 2 + (2 + 0.25\pi^2)(R_{sw}/R_a)$. From the above analysis, we conclude that it is feasible to achieve a reasonable noise figure with high voltage gain using a passive mixer topology. In actual practice, the LO waveforms are not exactly square wave in nature and this results in a higher switch resistance, lower conversion gain (the term $0.25\pi^2$ in the noise figure expression is inversely proportional to the conversion gain) and correspondingly a higher noise figure.

Fig. 8(a) shows the schematic of the mixer including the antenna interface and the baseband amplifier. It consists of a fully balanced structure with the baseband outputs capacitively coupled to a common source amplifier stage. Each transistor based switch is implemented as a triple well device for better isolation. A device size of 10 μm is used for all transistors. This size is chosen based on the available LO power and the minimum inductance realizable on the chip at these frequencies. The switches are biased at a DC voltage of 400 mV and are driven by LO signals with a power level of -3 dBm (LO swing of 400 mV). Using a higher DC bias allows one to obtain a lower on-resistance. However, as the LO swing is limited, the switch does not turn off easily. Hence, given a fixed LO swing (which is determined by the tripler output power), there exists an optimum bias point that maximizes the conversion gain of the mixer. The mixer is designed in tune with the antenna to obtain the best trade-off between conversion gain and noise figure. The conversion gain of the mixer is dependent on the device size and the LO power. Employing a direct conversion architecture greatly relaxes this constraint. For example, at DC or low frequencies, a baseband capacitive termination results in a large voltage gain with a modest switch resistance and low LO power. The variation of the mixer noise figure and voltage conversion gain as a function of the LO power is shown in Fig. 8(b). The mixer achieves a simulated peak gain of -3 dB and a SSB noise figure

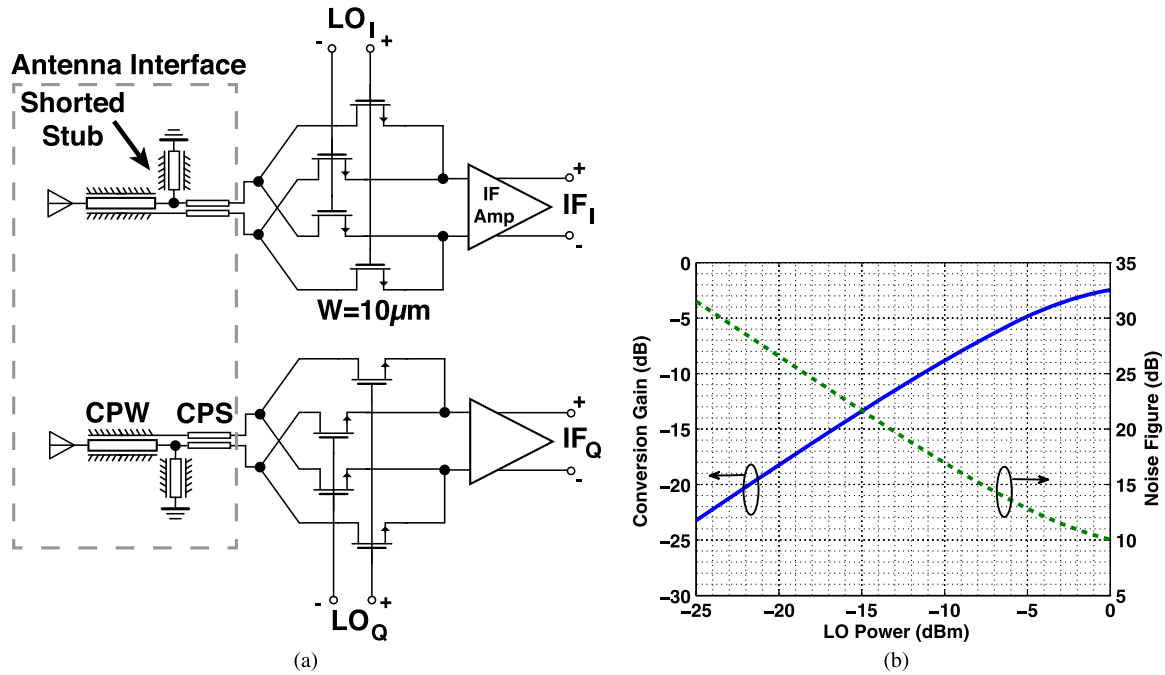


Fig. 8. (a) Schematic of the passive mixer with the antenna interface (b) simulated voltage conversion gain and noise figure as a function of the LO power.

of 12 dB with -3 dBm LO power at 240 GHz. The mixer has a baseband bandwidth of 20 GHz (DC to 20 GHz).

C. 80 GHz Local Oscillator Chain

The direct-conversion mixer used in this architecture is driven using a 240 GHz local oscillator chain. The chain consists of a 240 GHz tripler, an 80 GHz switching power amplifiers and an 80 GHz local oscillator chain. The details of the tripler and the power amplifier design are discussed in [9], [10]. In this section, we discuss the 80 GHz local oscillator chain. There are various techniques to generate the required 80 GHz LO signal. In this design, two injection locked oscillators operating at 27 GHz and 80 GHz (with an intermediate doubler and tripler) are used to generate the required LO. Injection-locked oscillator (ILO) based architecture keeps the design simple and avoids the use of phase locked loops. The phase generation is performed at the end of the chain using a passive delay line structure to minimize the I/Q phase error. The LO chain architecture is shown as part of Fig. 2. We now discuss the individual blocks of the LO chain.

1) Injection-Locked Voltage Controlled Oscillators (80 GHz and 26.6 GHz): The LO chain uses two injection locked oscillators operating at 80 GHz and 26.6 GHz. Fig. 9(a) shows the schematic of the 80 GHz ILO with the injection tripler devices. Transistors M1a and M1b form the core of the oscillator and are cross-coupled to generate the required negative impedance. The output from the VCO is coupled directly using buffer stages. Varactors are used to allow tuning of the VCO center frequency to compensate for process and temperature variations. In this design a MOS varactor operating in depletion/inversion region has been used. The injection into the VCO is performed using pseudo differential transistors M2a and M2b whose inputs are driven by the 26.6 GHz buffer. To maximize the lock range, devices M2a and M2b are biased in the Class-C regime which maximizes the generated third order non-linearity. The injection signal is then coupled into the oscillator using a transformer network which also provides the required inductance for the oscillation. Due to the highly non-linear action of the tripler devices, cascode stages M3a and M3b need to be added to improve the quality factor of the tank and to also keep the capacitance of the tank roughly constant during the switching action. In this design, a MOS varactor with a sizing of $14(1\ \mu\mathrm{m}/0.1\ \mu\mathrm{m})$ was used. The ILO operates from a supply voltage of 0.56 V and consumes 7.2 mA while the tripler operates from a supply voltage of 1 V and consumes 11.6 mA.

Fig. 9(b) shows the schematic of the 26.6 GHz ILO. The topology is similar to the 80 GHz VCO except for the fact that an explicit inductor is used for the tank and the injection is performed directly at the VCO output using transistors M2a and M2b. The VCO lock range covers the entire operation range of the 80 GHz ILO. In this design, a MOS varactor with a sizing of $28(1\ \mu\mathrm{m}/0.15\ \mu\mathrm{m})$ was used. The 26.6 GHz ILO operates from a supply voltage of 0.36 V and consumes 2.15 mA.

2) LO Chain Buffers: The output from the 80 GHz ILO is amplified to the desired level using a three-stage amplifier chain. Fig. 10(a) shows the schematic of the 80 GHz LO buffer chain. The first buffer stage is directly coupled to the output of the VCO and is biased at the supply voltage of the ILO. The first buffer consists of a pseudo cascode differential stage for good isolation between the output and the VCO. Each transistor is implemented using triple-well devices for good isolation and have a device size of $4(1\ \mu\mathrm{m}/0.06\ \mu\mathrm{m})$. The device size is selected based on the design of the ILO. The buffer is coupled to the second stage using a 2:1 transformer network. The second and third amplification stages consist of fully differential amplifiers coupled using transformer matching networks. The ILO along with the buffer (first amplification stage) is simulated to verify its performance and oscillation frequency. Fig. 10(b) shows the

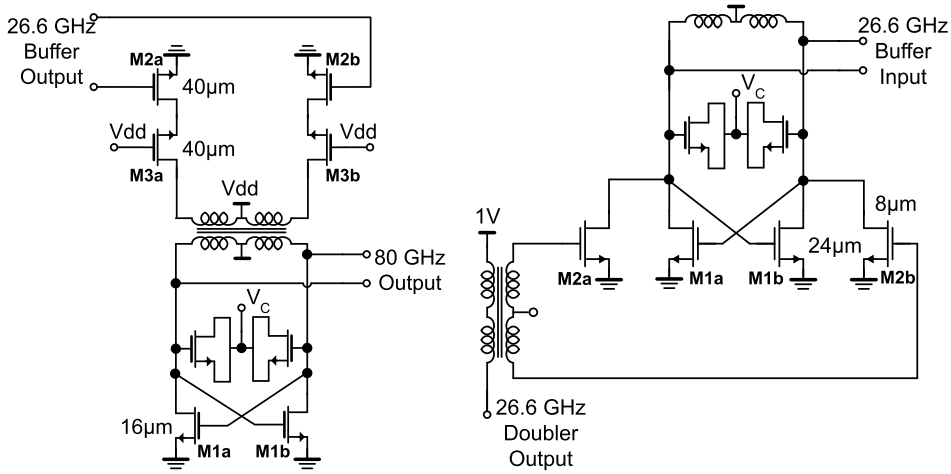


Fig. 9. (a) Schematic of the 80 GHz Injection-locked oscillator with the injection devices coupled using a transformer (b) schematic of the 26.6 GHz Injection-locked oscillator with the injection devices.

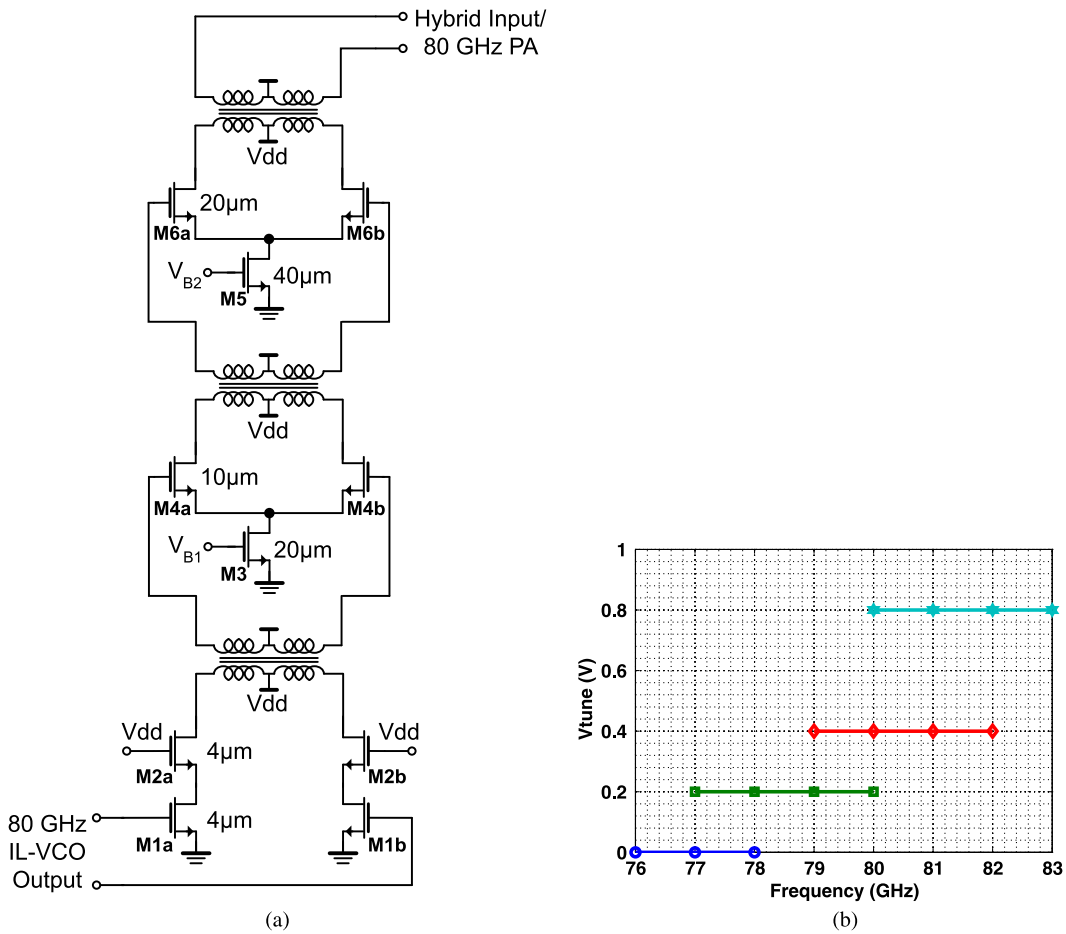


Fig. 10. (a) Schematic of 80 GHz LO buffer chain (b) Lock range of 80 GHz ILO as a function of the tuning voltage.

simulated lock range of the ILO as a function of the tuning voltage. As the tuning voltage is varied from 0 to 0.8 V, the ILO can lock to frequencies from 76 to 83 GHz. The generated output power by the buffer for these different settings is shown in Fig. 11(a). The ILO with the buffer generates a peak power of -3.6 dBm. The second amplification stage comprises of differential pairs M4a and M4b with sizing $10(1\ \mu\text{m}/0.06\ \mu\text{m})$. By adjusting the current flowing through the tail current source, the output power of the buffer stage is controlled. The LO chain consisting of the ILO and the three buffers generates an output power of 0 dBm and can be tuned from -5 dBm to 3 dBm.

The output from the 26.6 GHz ILO is capacitively coupled to a single buffer stage. A capacitive coupling is used to separately bias the buffers as the operating supply voltage of the ILO

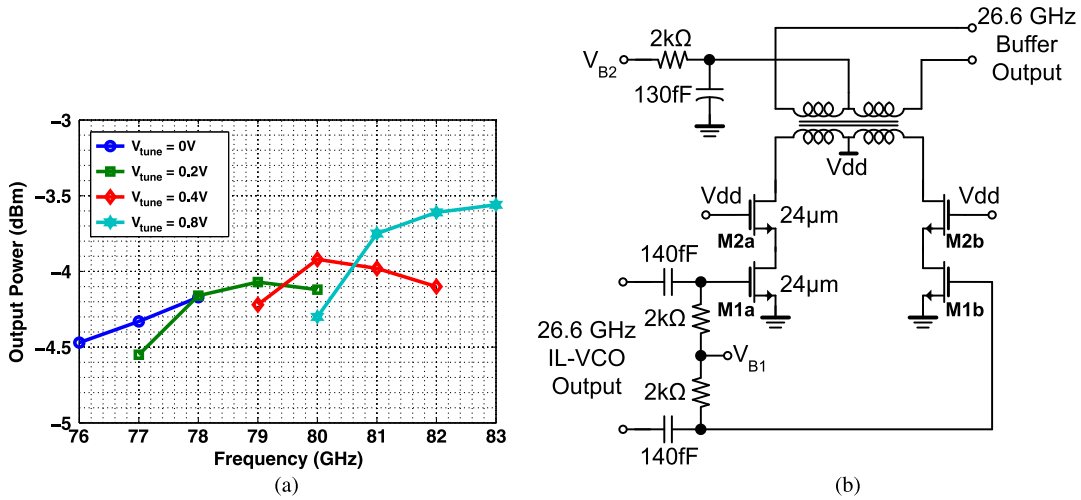


Fig. 11. (a) Output power of 80 GHz ILO with first buffer (b) schematic of 26.6 GHz LO buffer.

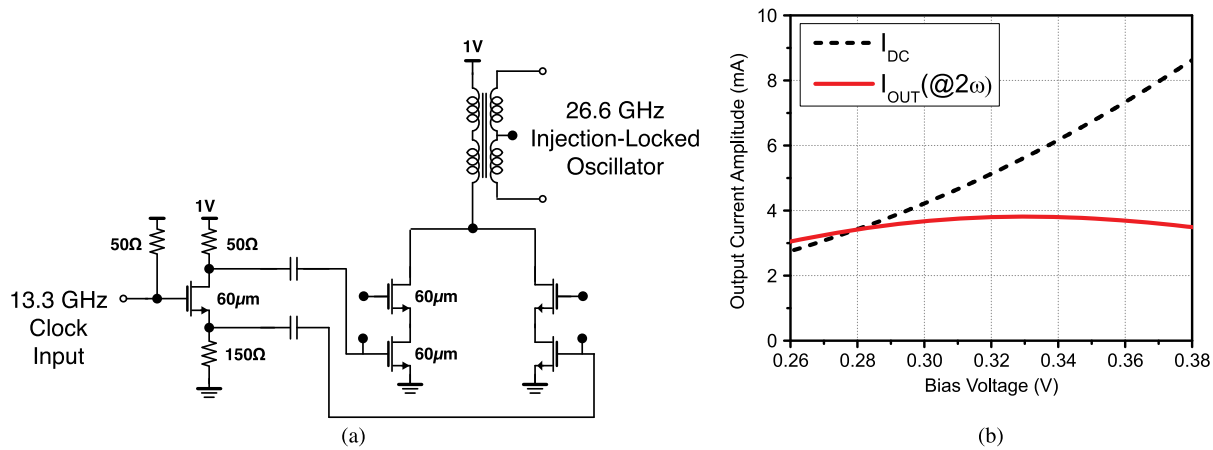


Fig. 12. (a) Schematic of the 26.6 GHz push-push doubler (b) simulated output current of the 26.6 GHz push-push doubler.

is 0.36 V. Fig. 11(b) shows the schematic of the 26.6 GHz buffer stage. It consists of a pseudo differential cascode stage and the output is load matched to the input impedance of the 26.6 to 80 GHz tripler. Each transistor has a sizing of $24(1\ \mu\text{m}/0.06\ \mu\text{m})$. Due to the highly non-linear action of the tripler and the finite C_{gd} of the transistors, there is significant second harmonic kick-back to the gate nodes. This leads to a distorted sinusoidal waveform at the input and degrades the conversion gain of the tripler. This in turn leads to a lower lock range for the 80 GHz ILO. Hence, the transformer matching network specifically uses a 2:1 turn structure. For a two turn inductor, the common mode inductance is one-fourth of its inductance at the fundamental [14]. By choosing the inductor diameter, trace width and spacing carefully, the second harmonic content at the gate nodes of M2a and M2b (Fig. 9(a)) are filtered out by adding a capacitor at the center tap. This shorts the second harmonic kick-back to ground and preserves the sinusoidal nature of the drive waveforms. The gate is biased using a high impedance resistor.

3) 26.6 GHz Doubler: Fig. 12(a) shows the schematic of the 26.6 GHz push-push doubler. A 13.3 GHz external clock drives the 50 Ω-matched active balun, which is self-biased and inductor-less. Two output voltages (source and drain) have the same amplitude and a 180° phase difference. At low frequencies, R_S (source degeneration resistor) and R_D (drain resistor) should have same resistance to obtain the same amplitude, but R_S is made larger than R_D because of lowered capacitance impedance at 13.3 GHz. The differential output are AC-coupled to the doubler. A cascode topology is chosen to increase the output impedance, boosting the gain and efficiency. The single-ended output from the doubler output is made differential using a passive balun. Simulation results are presented in Fig. 12(b). When V_b is 330 mV, the output current is maximized and the efficiency is 0.68. The bias voltage is set to a slightly lower voltage, 300 mV, considering both efficiency and output current. The input power of the front-end active balun is 0 dBm and the output power is −10 dBm including the output matching network. The active balun consumes 2.6 mW and the doubler consumes 4.2 mW from 1 V supply.

D. 240 GHz In-Phase/Quadrature Phase Generation

The required LO signal for the mixer is generated by the 240 GHz tripler in the LO chain. The tripler is interfaced to the 80 GHz LO generation blocks using the power amplifier and driver stages. For accurate demodulation of the received data, the phase mismatch between the I and Q LO signals must be

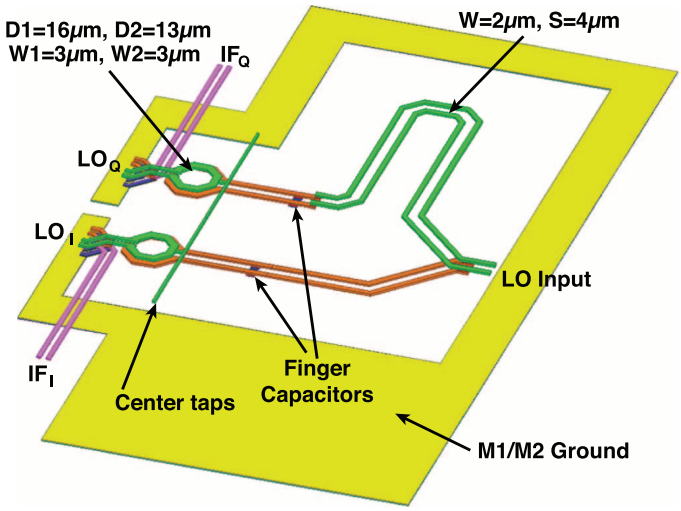


Fig. 13. 240 GHz I/Q generation and mixer LO matching interface.

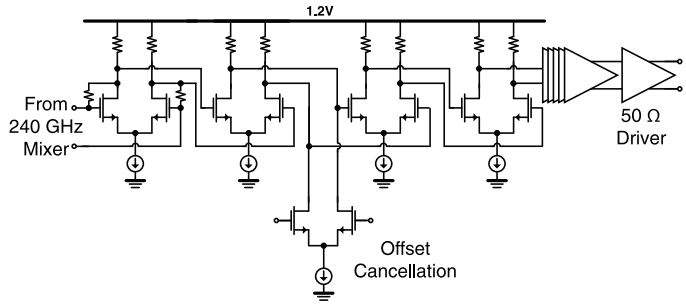


Fig. 14. Schematic of the baseband amplifier.

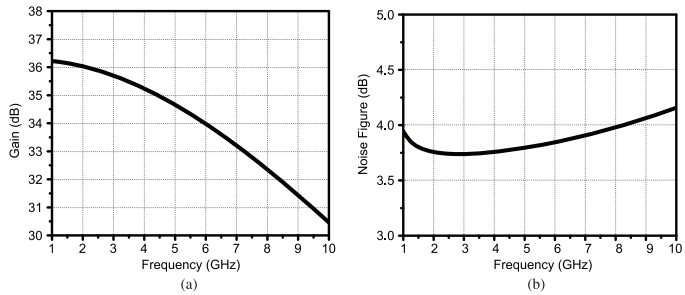


Fig. 15. Simulation results of the baseband amplifier (a) gain (b) noise figure.

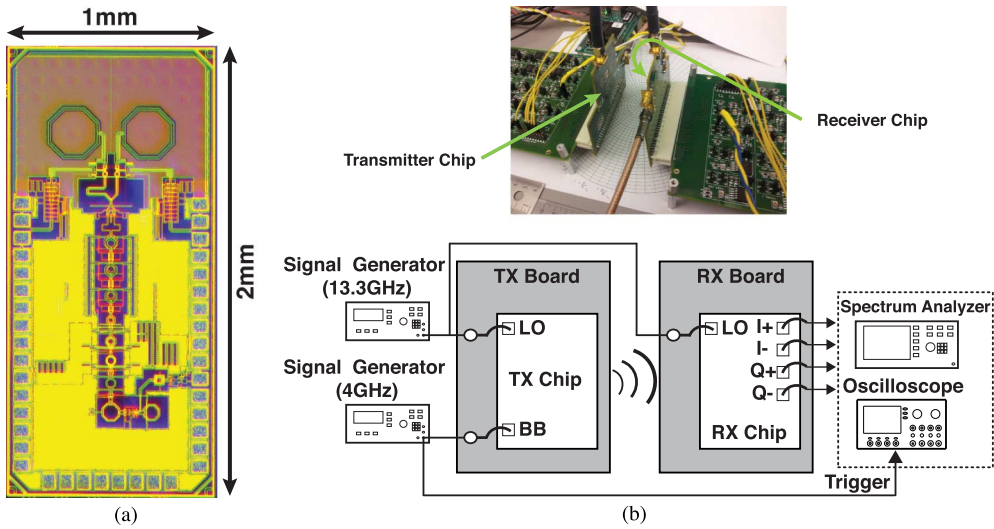
minimized. Hence, this design uses in-phase/quadrature generation using passive networks. Fig. 13 shows the passive network layout used for I/Q generation. The impedance seen at the gate of the mixer is transformed into a real impedance of 118 Ω using transformer networks. On the secondary side (mixer side), the top two thick metal layers are utilized to split the LO signals symmetrically. These are then used to drive the four LO ports of each mixer. Using a transformer network also allows one to conveniently bias the mixer gate node at the required potential. The transformer is then interfaced to coplanar striplines (CPS) with a characteristic impedance of 118 Ω and loss of 3.1 dB/mm. The lines are then connected in parallel and driven by the tripler. In order to achieve the quadrature signal, one leg has an additional length of $\lambda/4$, where λ is the wavelength. The CPS lines are implemented using the top two thick metal layers. The passive structure is surrounded by Metal1/Metal2 ground plane and characterized using full wave electromagnetic simulations. The structure has a simulated loss of 2.5 dB at 240 GHz in the LO path. The in-phase and quadrature LO outputs have a magnitude difference of 1 dB and a phase difference of 89.91° at 240 GHz. The IF outputs from the mixer are tapped in the lower strapped metal layers to minimize its coupling with the LO signals.

E. Baseband Amplifiers

A baseband amplifier is employed to amplify the received signal down-converted by the direct-conversion mixer in this work. The baseband amplifier is required to have a high gain, low noise figure, wide bandwidth, and low power dissipation. In order to achieve a lower noise figure for the receiver chain, the mixer is operated in voltage mode and is interfaced to a common source amplifier baseband stage (for lower noise figure). The input power for the baseband stage is determined by the transmit power, channel loss, and mixer conversion gain. Accordingly, the required gain is approximately 40 dB for output voltage swing of 100 mV. The noise figure should be minimized and the 3 dB bandwidth should be wider than 7 GHz to achieve a data rate of 20 Gbps in the QPSK modulation (or 10 Gbps in BPSK). The schematic is shown in Fig. 14. The baseband amplifier consists of nine differential pairs, and the last output amplifier is to drive two 50 Ω loads (differentially 100 Ω) for measurements. Device sizes and tail currents are taper-designed to optimize the performance. As the input stage dominates the chain noise figure, it consumes majority of the total power. In post-layout simulations, the baseband amplifier achieves a gain of 36 dB, as presented in Fig. 15(a). The noise figure is less than 4 dB over the bandwidth, as shown in Fig. 15(b). The power consumption is 40 mW with a supply voltage of 1.2 V. The offset cancellation is performed manually by a differential pair, as shown in Fig. 14. In simulation, the offset cancellation circuit is designed to correct the worst-case offset. If the size of the offset cancellation circuit is too large, the gain, bandwidth, and power consumption are degraded; thus, some design iterations are needed.

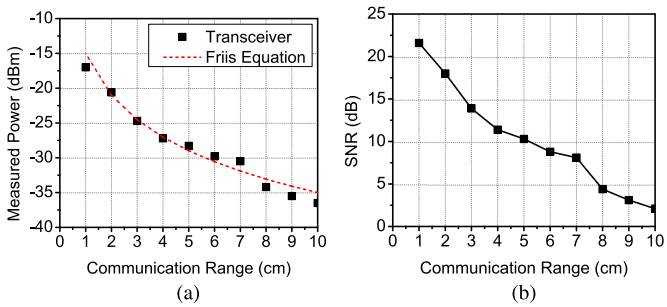
V. Measurement Results

The 240 GHz receiver chip is fabricated in 65 nm bulk CMOS process without any special options. The chip microphotograph is shown in Fig. 16(a) and occupies a die area of 2 mm × 1 mm. The chip is attached to FR-4 boards using conductive epoxy and the pads are wire bonded. The DC voltages and bias currents, the required LO chain input clock and the PRBS input clock are provided through a bonding wire. The required copper plate for the antennas is designed as part of the PCB board. The measurement setup is shown in Fig. 16(b). An external signal generator feeds the required LO clock at 13.3 GHz to both the transmitter and receiver chips using a splitter. The required data clock is fed by another signal generator as before. The chips are interfaced using PCI slots and placed vertically facing each other in a line of sight (LOS) communication. The radiated 240 GHz modulated signal from the transmitter [9], [10] is captured by the receiver chip and demodulated to baseband I and Q signals. This signal is then measured using a spectrum analyzer and the eye diagram is captured using a real time oscilloscope.



(a) (b)

Fig. 16. (a) Die photo (b) measurement setup.



(a) (b)

Fig. 17. (a) Variation of measured received output power with distance in CW mode (b) variation of measured SNR with distance in CW mode.

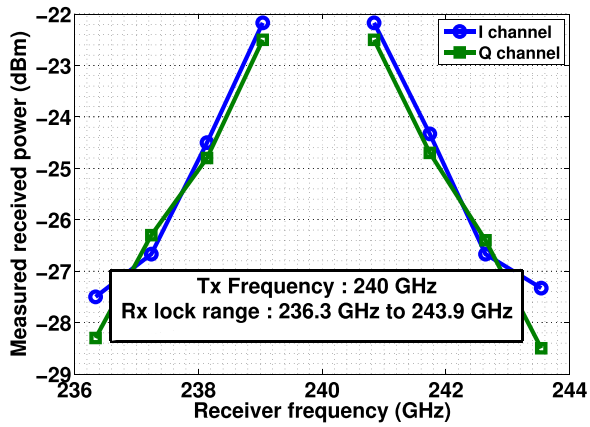
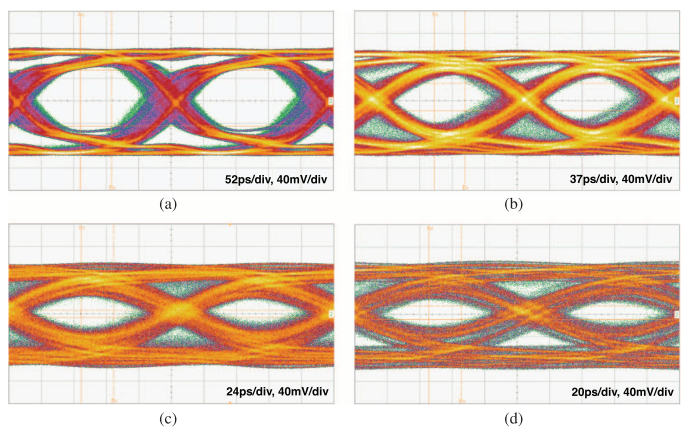


Fig. 18. Measured CW receiver power for I and Q channels with varying receiver LO frequency. Transmitter LO frequency is held at 240 GHz.



(a) (b) (c) (d)

Fig. 19. Measured receiver eye diagrams (a) 4 Gbps BPSK (b) 6 Gbps BPSK (c) 8 Gbps BPSK (d) 9 Gbps BPSK.

A continuous-wave (CW) measurement is performed using the transmitter chip. For the CW measurements, different LO frequencies are selected for the transmitter and receiver chips. The distance between the transmitter and receiver is adjusted and the resulting measured power level is plotted as a function of the distance. Fig. 17(a) shows the measured result and the data points follow the 20 dB per decade slope as predicted by Friis equation. The signal to noise ratio (SNR) of the received waveform is calculated by summing up the total noise power in the bandwidth of interest. Fig. 17(b) shows the measured SNR. The SNR at the receiver front end can be estimated using the transmitter power and the channel loss. From these two results, the gain and the SSB noise figure of the receiver chain is calculated to be 25 dB and 15 dB respectively. The link has a measured SNR of 17 dB at a distance of 2 cm. Next, the lock range of the receiver LO chains is measured for I and Q channels. Fig. 18 shows the measured received power in the I and Q channels as a function of the transmitter LO frequency. The transmitter LO frequency is held constant at 240 GHz. It is observed that the power levels in the I and Q channels have a mismatch of 0.2 dB. The receiver lock range is 7.6 GHz centered about 240 GHz. The phase noise measurement is shown in [10].

With the BPSK modulation mode, time-domain eye diagrams for data rates 4 Gbps, 6 Gbps, 8 Gbps and 9 Gbps are shown in Fig. 19. Using this data, the bathtub curves are plotted in Fig. 20 (with an instrument limit is 10^{-6}). With the 9 Gbps BPSK modulation, the BER is approximately 10^{-5}. With the QPSK modulation mode, the frequency spectrums of the receiver output are measured as shown in Fig. 21. The eye diagrams measured at the receiver output for 8 Gbps, 12 Gbps, and

TABLE I
COMPARISON OF SUB-TERAHERTZ RECEIVERS

	This work [8]		OOK receiver [2]	Ojefors [3]	Elkhouly [4]	Guerra [5]	Tytgat [6]	
Technology	65 nm CMOS		65 nm CMOS	130 nm SiGe	130 nm SiGe	65 nm CMOS	90 nm CMOS	
Modulation	QPSK/BPSK		OOK	-	I/Q	-	QPSK/BPSK	
Frequency (GHz)	240		260	220	245	283	200	
Gain (dB)	25		17	16	18	-6	6.6	
NF (dB)	15		19	18	18	38	29.9	
Power dissipation (mW)	260		485	216	512	97.6	63.3	
Area (mm^2)	2		3	0.66	2.1	0.64	0.375	
Antenna	on-chip		on-chip	-	-	-	-	
Integration	Full		Full	LNA/Mixer	LNA/Mixer/ IF Amp/Hybrid	Mixer/LO/ IF Amp	Mixer/IFAmp	
Data Rate (Gbit/s)	10	16	-	-	-	-	2	4
BER	$< 10^{-6}$	10^{-4}	-	-	-	-	10^{-10}	-
Receiver Efficiency (pJ/bit)	26	16	-	-	-	-	32	16

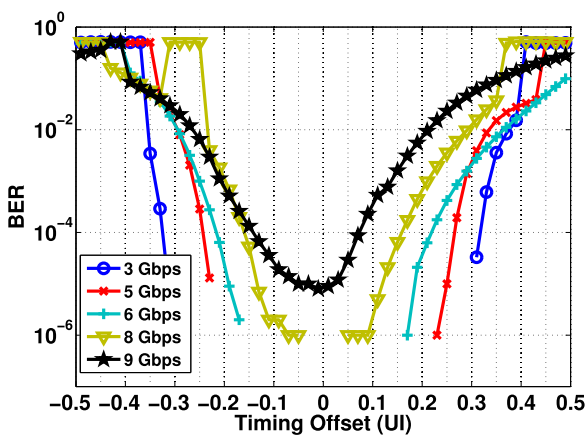


Fig. 20. BER bathtub curves of BPSK modulation.

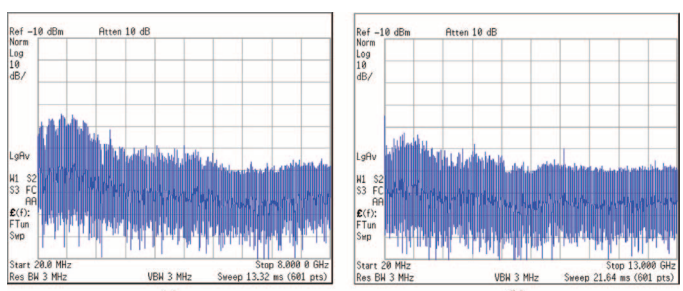


Fig. 21. Measured receiver output spectra (a) 8 Gbps QPSK (b) 16 Gbps QPSK.

16 Gbps QPSK mode are shown in Fig. 22. The eye opening degrades with increase in data rate. The maximum data rate is 16 Gbps with a communication range of 2 cm. The BER bathtub curves are shown in Fig. 23. In the 16 Gbps QPSK modulation, the BER is approximately 10^{-4}. The minimum BER detection is limited by the memory capacity of the real time oscilloscope. The receiver consumes 260 mW and the power breakdown is shown in Fig. 24. The summary and comparison of the receiver is presented in Table I.

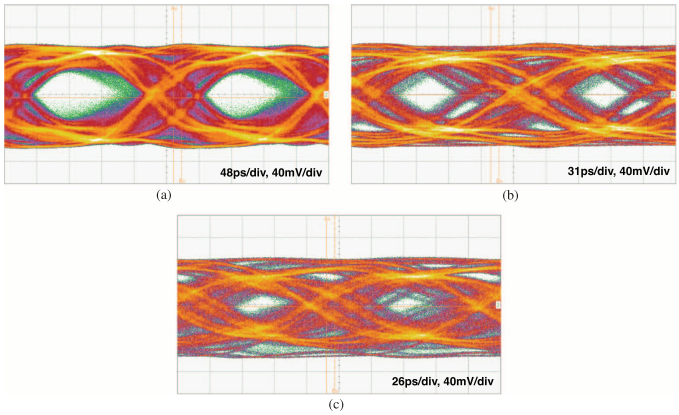


Fig. 22. Measured receiver eye diagrams (a) 8 Gbps QPSK (b) 12 Gbps QPSK (c) 16 Gbps QPSK.

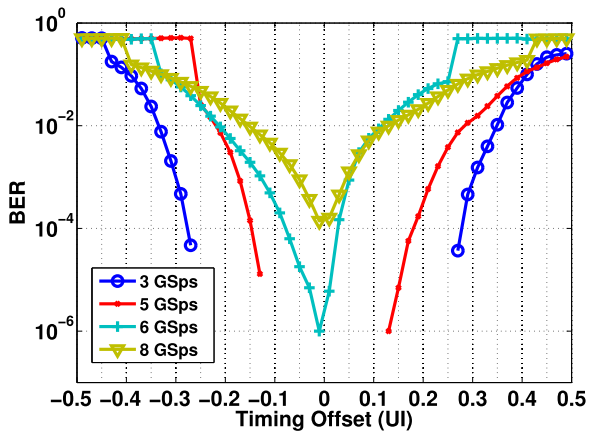


Fig. 23. BER bathtub curves of QPSK modulation.

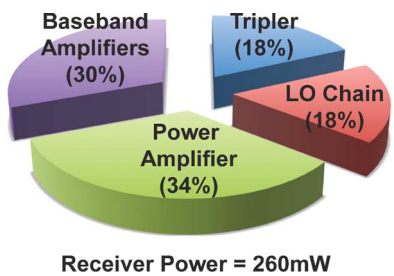


Fig. 24. Receiver chip power breakdown.

VI. CONCLUSION

This paper has demonstrated a 240 GHz QPSK/BPSK receiver design fabricated in 65 nm CMOS technology. The system challenges, design issues and receiver architectures are proposed for high-speed coherent phase modulations. Front-end layout designs, measured frequency spectrums, time-domain eye diagrams and BER bathtub curves are presented. The 240 GHz receiver achieves a data rate of 10 Gbps (with BER $< 10^{-6}$) and a data rate of 16 Gbps (with BER of 10^{-4}) in the QPSK mode with a range of 2 cm and a receiver efficiency of 16 pJ/bit. To date, the 240 GHz transceiver achieves the highest data rate and efficiency among CMOS transceivers above 200 GHz.

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