Chapter 9
Operational Amplifiers

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教材：模拟CMOS集成电路设计

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9.1 General considerations

- 运放：很高增益差动放大器。
- 开环增益：根据闭环电路精度要求选取。

9.1.1 Performance Parameters:

- Gain
- Small-signal bandwidth
- Large-signal bandwidth
- Output Swing
- Linearity
- Noise and offset(失调)
- 输入/输出阻抗(s)
- 输入/输出范围
- Supply Rejection
- 稳定性（相位裕量）
- 功耗

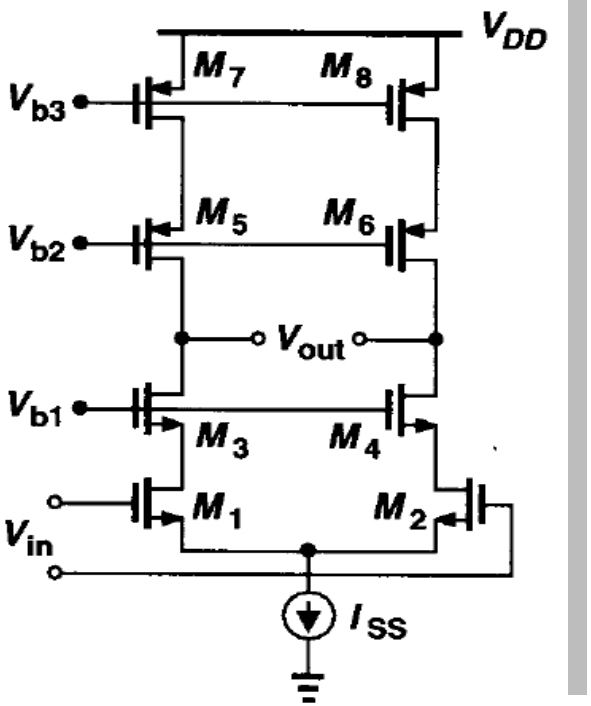


Figure 9.1 Cascode op amp.

a high open-loop gain may also be necessary to suppress nonlinearity.

The circuit of Fig. 9.2 is designed for a nominal gain of 10, i.e., $1 + R_1/R_2 = 10$. Determine the minimum value of A_1 for a gain error of 1%.

Solution

$$\frac{V_{out}}{V_{in}} = \frac{A_1}{1 + \frac{R_2}{R_1 + R_2} A_1}$$

$$= \frac{R_1 + R_2}{R_2} \frac{A_1}{\frac{R_1 + R_2}{R_2} + A_1}$$

$$\approx \left(1 + \frac{R_1}{R_2}\right)\left(1 - \frac{R_1 + R_2}{R_2}\frac{1}{A_1}\right)$$

$(1 + R_1/R_2)/A_1$ represents the relative gain error.

$\longrightarrow \quad A_1 > 1000.$

无负载，$A_1(s)$

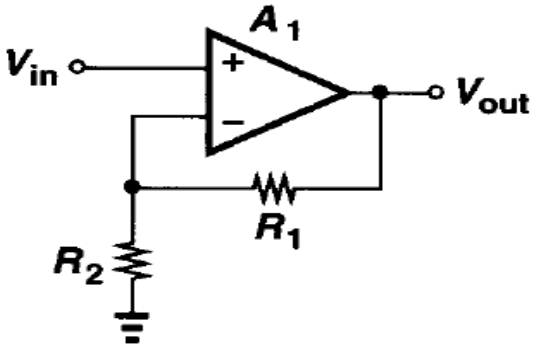
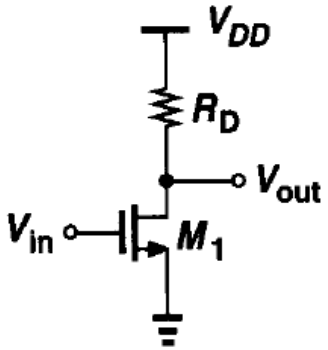


Figure 9.2

若$A_1(s)$高频时降为100，则无负载的$A_{vf}(s)$约为9



开环电路增益误差大：
电阻不准、温度系数大

Small-signal bandwidth

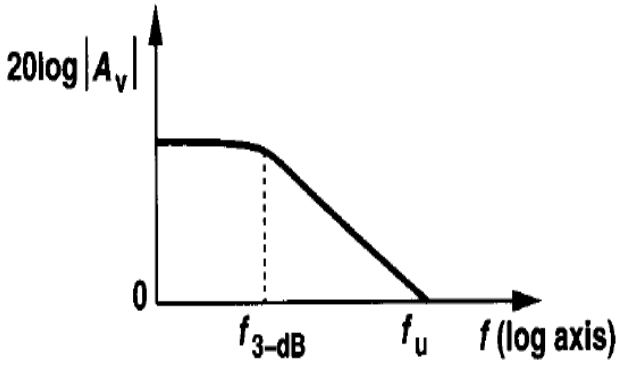
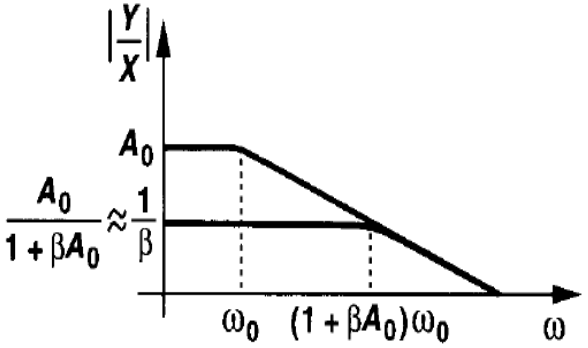


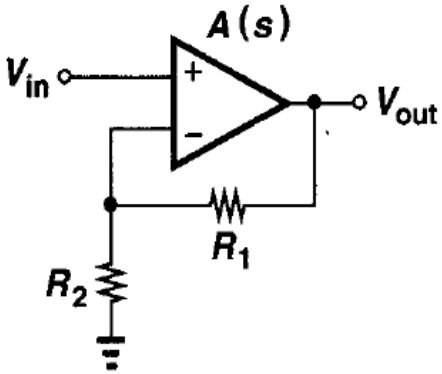
Figure 9.4
Gain roll-off with frequency

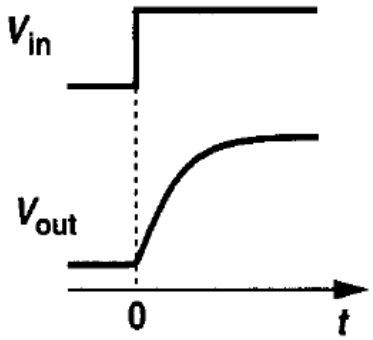
增益*带宽=常数（开环=闭环）=$A_o w_o$ =单位增益带宽
（例如电压跟随器）



Example 9.2

assume the op amp is a single-pole voltage amplifier.
calculate the time required for the output voltage to reach within 1% of its final value.





1+R1/R2=10，上升至终值1%时的稳定时间<5ns。运放的单位增益带宽?

Solution

Since $$\left(V_{in} - V_{out}\frac{R_2}{R_1+R_2}\right)A(s) = V_{out}$$

we have $$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1+\frac{R_2}{R_1+R_2}A(s)}$$

一阶传递函数运放

$$V_{out}(t) \approx a\left(1+\frac{R_1}{R_2}\right)\left(1-\exp\frac{-t}{\tau}\right)u(t)$$

Small-signal bandwidth (cont.)

$A(s) = A_0/(1 + s/\omega_0)$, where ω_0 is the 3-dB bandwidth

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_0}{1 + \frac{R_2}{R_1 + R_2}A_0 + \frac{s}{\omega_0}} = \frac{\frac{A_0}{1 + \frac{R_2}{R_1 + R_2}A_0}}{1 + \frac{s}{\left(1 + \frac{R_2}{R_1 + R_2}A_0\right)\omega_0}}$$

indicating that the closed-loop amplifier is also a one-pole system with a time constant equal to

闭环时间常数 $$\tau = \frac{1}{\left(1 + \frac{R_2}{R_1 + R_2}A_0\right)\omega_0} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{1}{A_0\omega_0}$$

The output step response for $V_{in} = au(t)$ can now be expressed as

$$V_{out}(t) \approx a\left(1 + \frac{R_1}{R_2}\right)\left(1 - \exp\frac{-t}{\tau}\right)u(t).$$

the final value $V_F \approx a(1 + R_1/R_2)$.

For 1% settling, $V_{out} = 0.99V_F$ → $1 - \exp\frac{-t_{1\%}}{\tau} = 0.99$. → $t_{1\%} = \tau \ln 100 \approx 4.6\tau$ =5ns

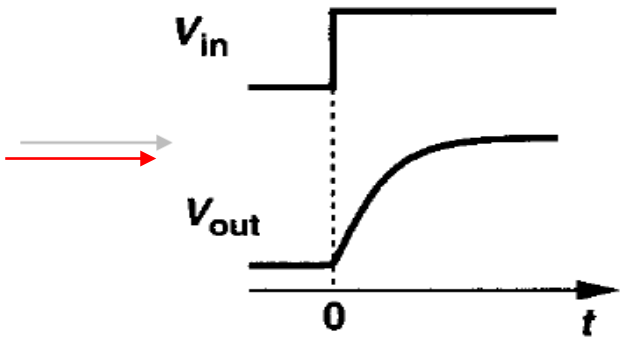
$\tau \approx 1.09$ ns.

放大运算（闭环）电路的增益带宽积= $(1 + R_1/R_2)/\tau = 9.21$ Grad/s (1.47 GHz).

=运放的单位增益带宽 $= A_0\omega_0$

Performance Parameters (cont.)

- Large-signal bandwidth
  - 幅度变化大，进入非线性，不适合AC仿真，
  - 转换速率slew rate



- Output Swing

tran仿真

- Linearity（假设幅度变化大）

Open-loop op amps suffer from substantial nonlinearity.

非线性问题通过两种方法解决:

1.采用全差动抑制偶次谐波;

2.足够高的开环增益以使反馈系统达到所要求的线性

Performance Parameters (cont.)

- 噪声和失调(offset)

  噪声限制了能处理的最小信号电平，分析关键器件噪声(例如输入管)。

  失调由失配引起。

- 稳定性（相位裕量）

  仅针对构建反馈系统。

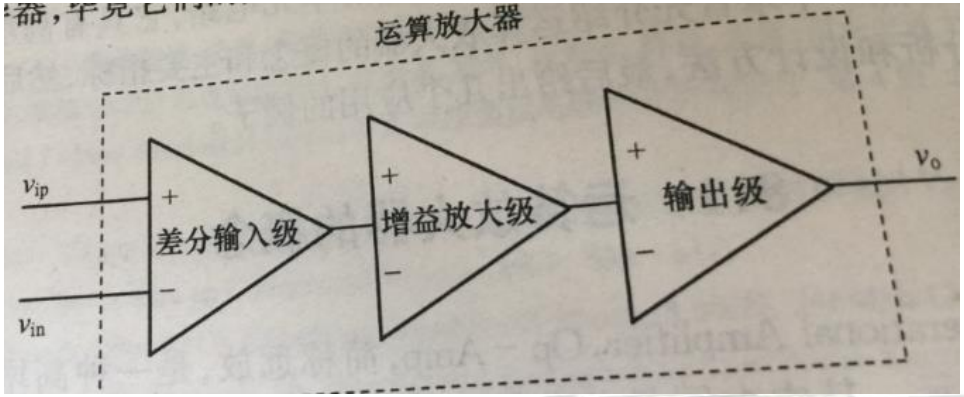
- 功耗

  若是微弱信号（几十uV以下)放大器输入级由信噪比确定；

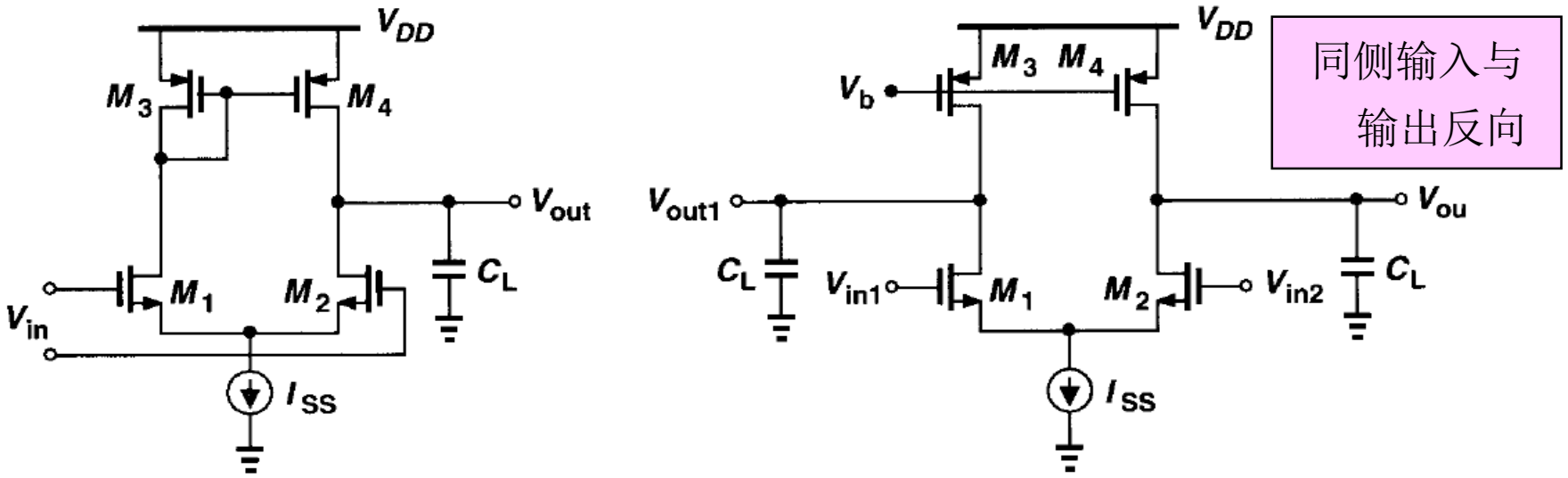
  输出是大信号或重负载时，输出级（尾电流源）需要大电流。

- 输入输出阻抗和电压范围

  级联接口。



9.2 One-Stage OP Amplifiers

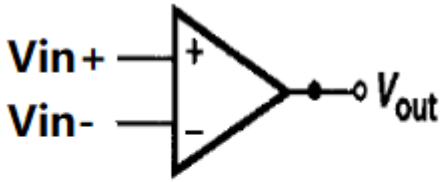


同侧输入与输出反向

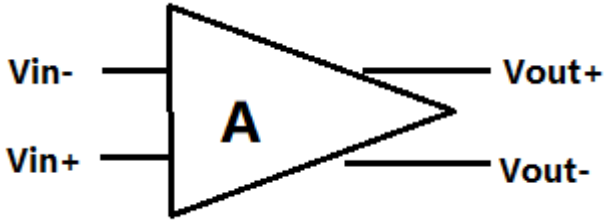
Figure 9.6 Simple op amp topologies.

- 低频小信号增益 $g_{mN}(r_{ON} \| r_{OP})$,
- 图9.6(a) 有一个镜像极点。

Fully differential OP need CMFB!

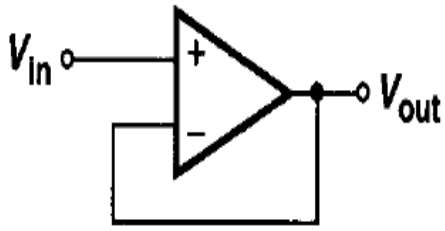


与输出方向相同的输入为Vin+



Example 9.3

Calculate the input common-mode voltage range and the closed-loop output impedance of the unity-gain buffer depicted in Fig. 9.7.



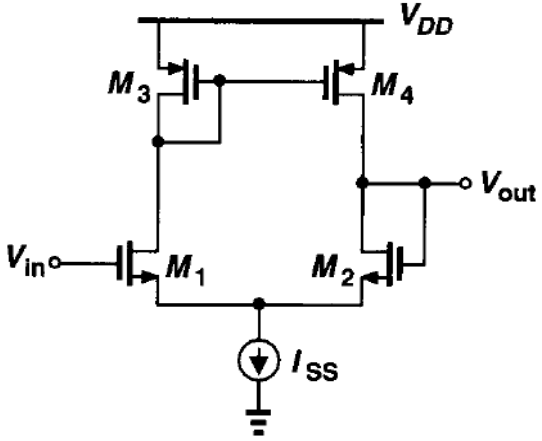


Figure 9.7

电压跟随器输入必须在输出允许范围内

开环增益小时虚短不成立！

设阈值电压V_{TH}=0.7V,

过驱动电压$V_{GS}-V_{TH}$=0.3V

The minimum allowable input voltage is equal to $V_{CSS} + V_{GS1}$, where V_{CSS} is the voltage required across the current source.

V_{OD}由漏极电流确定

$$V_{in,min} = 0.3 + 0.3 + 0.7 = 1.3\ \text{V}$$

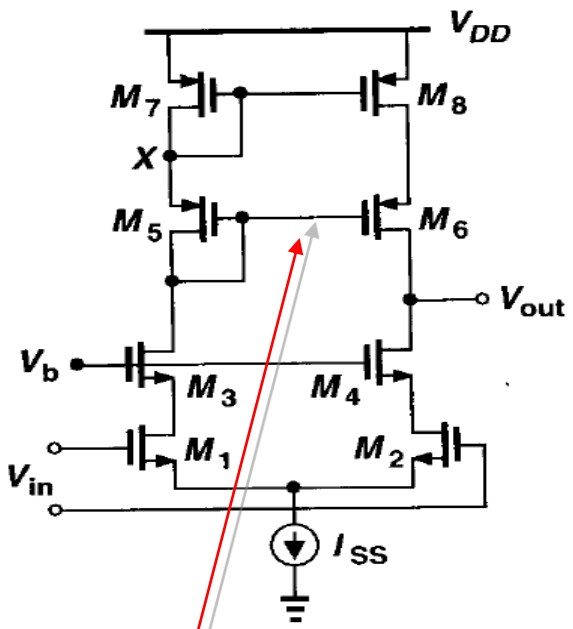
$$V_{in,max} = V_{DD} - |V_{GS3}| + V_{TH1} \qquad V_{in,max} = 3 - (0.3 + 0.7) + 0.7 = 2.7\ \text{V}.$$

Since the circuit employs voltage feedback at the output, the output impedance is

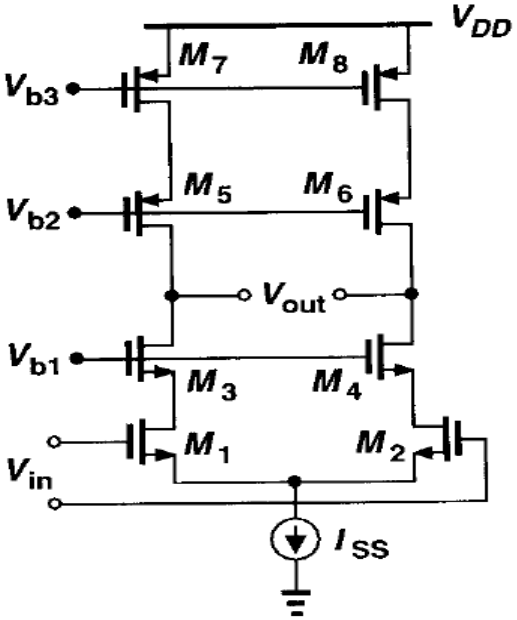
$$(r_{OP} \| r_{ON})/[1 + g_{mN}(r_{OP} \| r_{ON})] = 1/g_{mN}.$$

the closed-loop output impedance is relatively *independent* of the open-loop output impedance. *increasing* the open-loop output impedance while still achieving a relatively low closed-loop output impedance.

One-Stage OP Amplifiers (cont.)



(a)



(b)

Figure 9.8 Cascode op amps.

"telescopic" cascode op amps

套筒式

high gain,

on the order of

$$g_{mN}[(g_{mN}r_{ON}^2)\|(g_{mP}r_{OP}^2)]$$

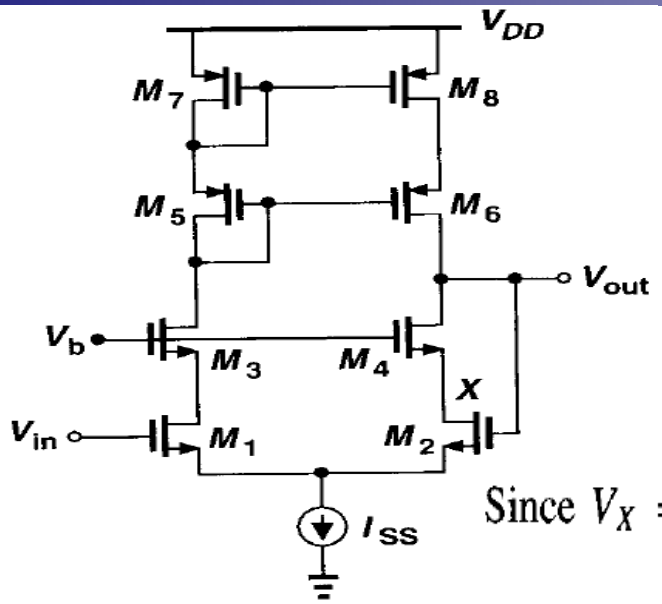
输出范围较小

Fig. 9.8(b) the output swing is

$$2[V_{DD} - (V_{OD1} + V_{OD3} + V_{CSS} + |V_{OD5}| + |V_{OD7}|)]$$

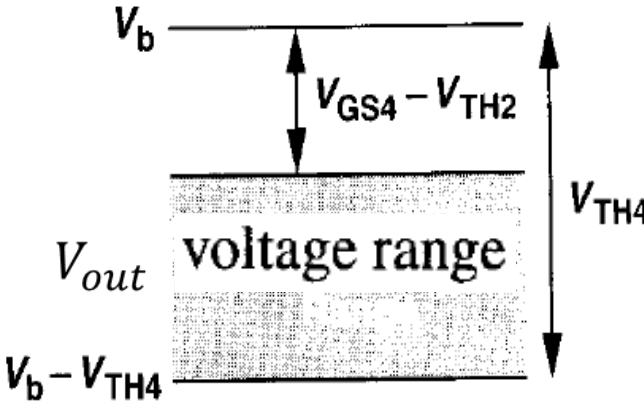
where V_{ODj} denotes the overdrive voltage of M_j.

套筒式电流镜负载放大器实现单位增益缓冲器的限制



$$V_{out} \le V_X + V_{TH2}$$

$$V_{out} \ge V_b - V_{TH4}$$



Since $V_X = V_b - V_{GS4}$, $V_b - V_{TH4} \le V_{out} \le V_b - V_{GS4} + V_{TH2}$.

$V_{omax}-V_{omin}=(V_b-V_{GS4}+V_{TH2})-(V_b-V_{TH4})=V_{TH4}-V_{GS4}+V_{TH2}$

$=V_{TH2}-V_{OD4}$

作为电压跟随器时，输出（虚短输入）范围太小！

$$V_{GS1} + V_{ODSS} \le V_{in} \le V_b - V_{GS3} + V_{TH1}$$

$$V_b \ge V_{GS3} + V_{OD1} + V_{ODSS}$$

$V_b \ge V_{in} + V_{OD}$　　若V_b取最低电平，则$V_{GS1} + V_{ODSS} \le V_{in} \le V_{GS1} + V_{ODSS}$

电压跟随器须工作在Vin和Vout共同有效的电压范围内

Example 9.5

Design a fully differential telescopic op amp with the following specifications: $V_{DD} = 3$ V, differential output swing = 3 V, power dissipation = 10 mW, voltage gain = 2000. Assume $\mu_n C_{ox} = 60\ \mu\text{A/V}^2$, $\mu_p C_{ox} = 30\ \mu\text{A/V}^2$, $\lambda_n = 0.1\ \text{V}^{-1}$, $\lambda_p = 0.2\ \text{V}^{-1}$ (for an effective channel length of 0.5 μm), $\gamma = 0$, $V_{THN} = |V_{THP}| = 0.7$ V.

Solution 思路：ID？→VOD→W/L→增益验证

We begin with the power budget,

allocating 3 mA to M_9

the remaining 330 μA to M_{b1} and M_{b2}.

Next, we consider the required output swings.

Each of nodes X and Y must be able to swing by 1.5 V without driving M_3-M_6 into the triode region.

$$|V_{OD7}| + |V_{OD5}| + V_{OD3} + V_{OD1} + V_{OD9} = 1.5\ \text{V}.$$

choose $V_{OD9} \approx 0.5$ V. overdrive voltages.

since M_5-M_8 suffer from low mobility

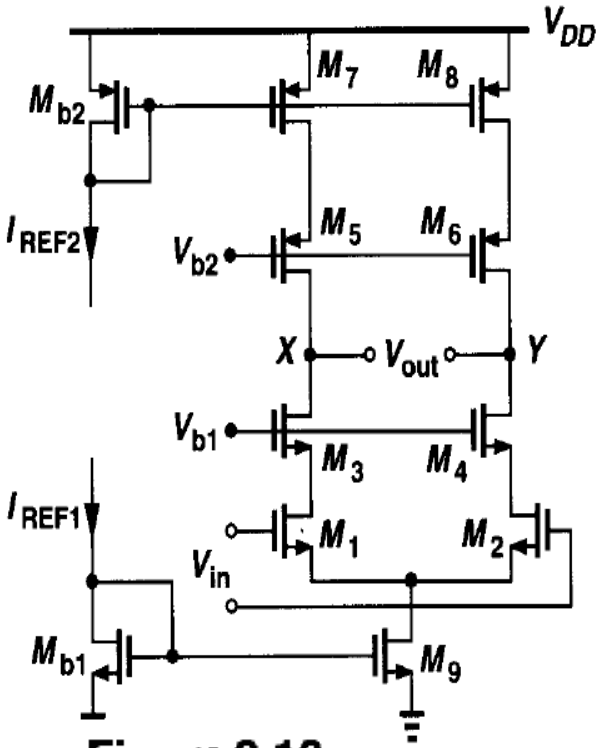


Figure 9.10

VOD5=VOD7=0.3V, VOD1=VOD3=0.2V

于是可确定各管宽长比aspect ratio from

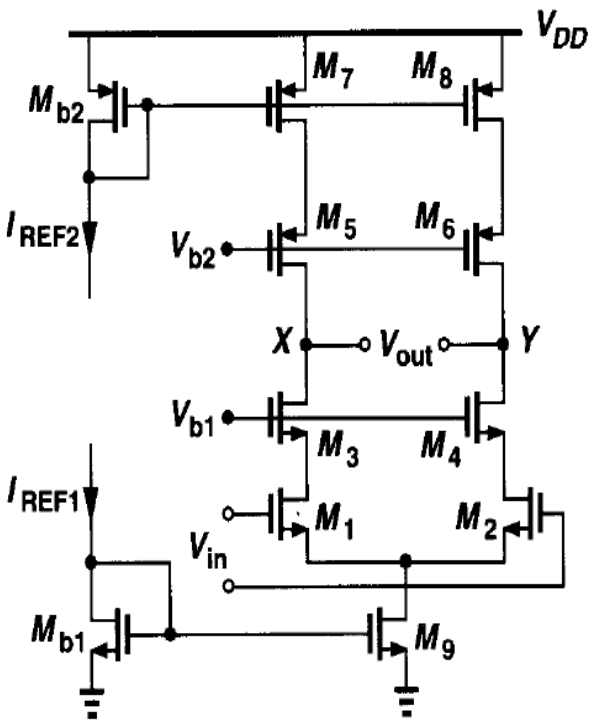
$$I_D = (1/2)\mu C_{ox}(W/L)(V_{GS} - V_{TH})^2$$

$$A_v \approx g_{m1}[(g_{m3}r_{O3}r_{O1})\|(g_{m5}r_{O5}r_{O7})]$$

Example 9.5 (cont.)

To minimize the device capacitances, we choose the minimum length for each transistor, obtaining a corresponding width.

$(W/L)_{1-4} = 1250, (W/L)_{5-8} = 1111, (W/L)_9 = 400.$



The design has thus far satisfied the swing, power dissipation specifications.

how about the gain?

$$A_v \approx g_{m1}[(g_{m3}r_{O3}r_{O1})\|(g_{m5}r_{O5}r_{O7})]$$

$\lambda I_D = 1/r_O,$

we have $A_v = 1416$, quite lower than the required value.

$$g_m r_O = \sqrt{2\mu C_{ox}(W/L)I_D}/(\lambda I_D) \qquad \lambda \propto 1/L,$$

hence $g_m r_O \propto \sqrt{WL/I_D}$.

We can therefore increase the width or length or *decrease* the bias current of the transistors.

Example 9.5 (cont.)

In practice, speed or noise requirements may dictate the bias current,

$$\text{支路电流} > \text{负载电流} C\frac{\Delta V}{\Delta t}$$

Which transistors in the circuit of Fig. 9.10 should be made longer?

Since M_1-M_4 appear in the signal path, it is desirable to keep their capacitances to a minimum.

The PMOS devices, M_5-M_8, affect the signal to a much lesser extent and can therefore have larger dimensions.

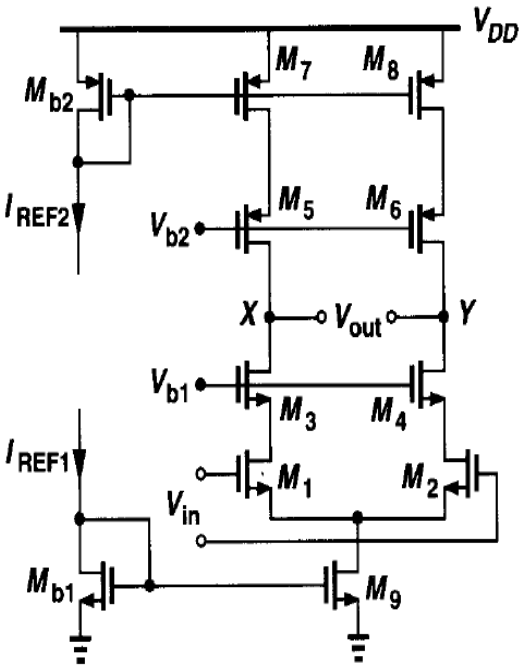


Fig. 9.10

Choosing $(W/L)_{5-8} = 1111\,\mu\text{m}/1.0\,\mu\text{m}$

hence $\lambda_p = 0.1\ \text{V}^{-1}$, ($\lambda_p = 0.2\ \text{V}^{-1}$ for an effective channel length of 0.5 μm)

we obtain $A_v \approx 4000$. $A_v \approx g_{m1}[(g_{m3}r_{O3}r_{O1})\|(g_{m5}r_{O5}r_{O7})]$

Note that with such large dimensions for PMOS transistors, we may reduce the overdrive voltages of M_9 by 100 to 200 mV and allocating more to the PMOS devices.

Example 9.5 (cont.)

the input CM level and the bias voltages V_{b1} and V_{b2} must be chosen so as to allow maximum output swings.

The minimum allowable input CM level equals

$$V_{GS1} + V_{OD9} = V_{TH1} + V_{OD1} + V_{OD9} = 1.4\,\text{V}.$$

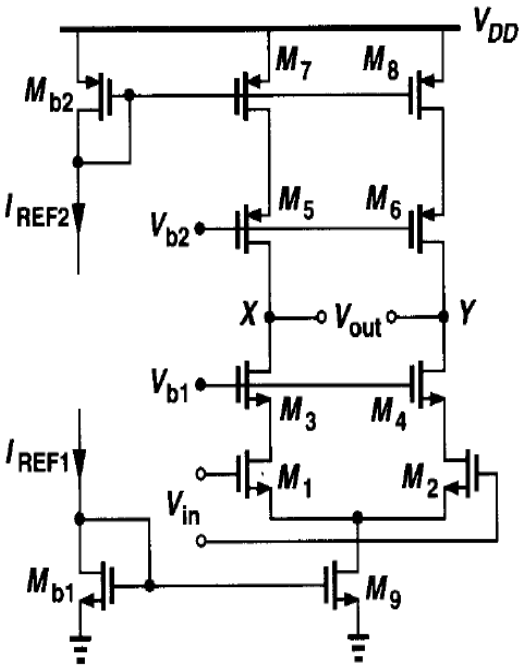
The minimum value of V_{b1} is given by

$$V_{b1,min}=V_{GS3}+V_{OD1}+V_{OD9}=1.6V$$

placing M_1-M_2 at the edge of the triode region.

$$V_{b2,max} = V_{DD} - (|V_{GS5}| + |V_{OD7}|)$$

$$=3-(0.7+0.3+0.3)=1.7V$$



V_{TH}=0.7,$V_{OD1,3}$=0.2

$V_{OD5,7}$=0.3,V_{OD9}=0.5

V_{outCM}受Vb1和Vb2限制（ Vb1-V_{THn} ~ Vb2+V_{THp} 即 0.9~2.4V，均值1.65V）

V_{inCM}下限（V_{TH1}+V_{OD1}+V_{OD9} =1.4V）受V_{OD9}限制，上限 （V_{b1}-V_{GS3}+V_{TH1}=1.4V）受V_{b1}限制，范围很小。解决：可降低V_{OD9}或提高V_{b1}

Folded折叠 cascode

In order to alleviate the drawbacks of telescopic cascode op amps, namely, limited output swings and difficulty in shorting the input and output, a "folded cascode" op amp can be used.

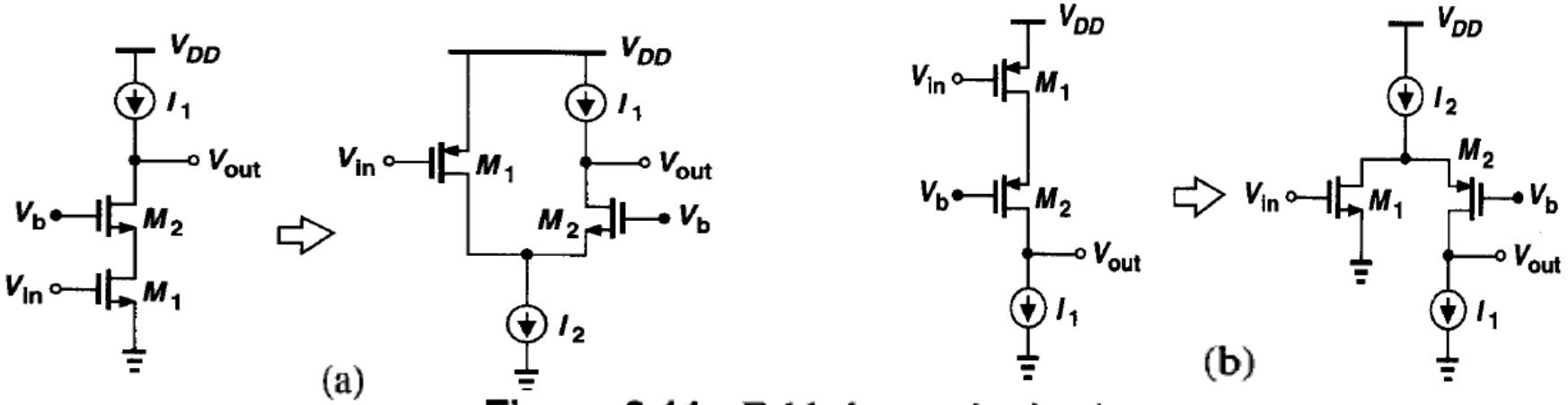


Figure 9.11 Folded cascode circuits.

the input device is replaced by the opposite type

output voltage

$$g_{m1} R_{out} V_{in}.$$

The primary advantage of the folded structure lies in the choice of the voltage levels because it does not "stack" the cascode transistor on top of the input device.

Differential folded-cascode

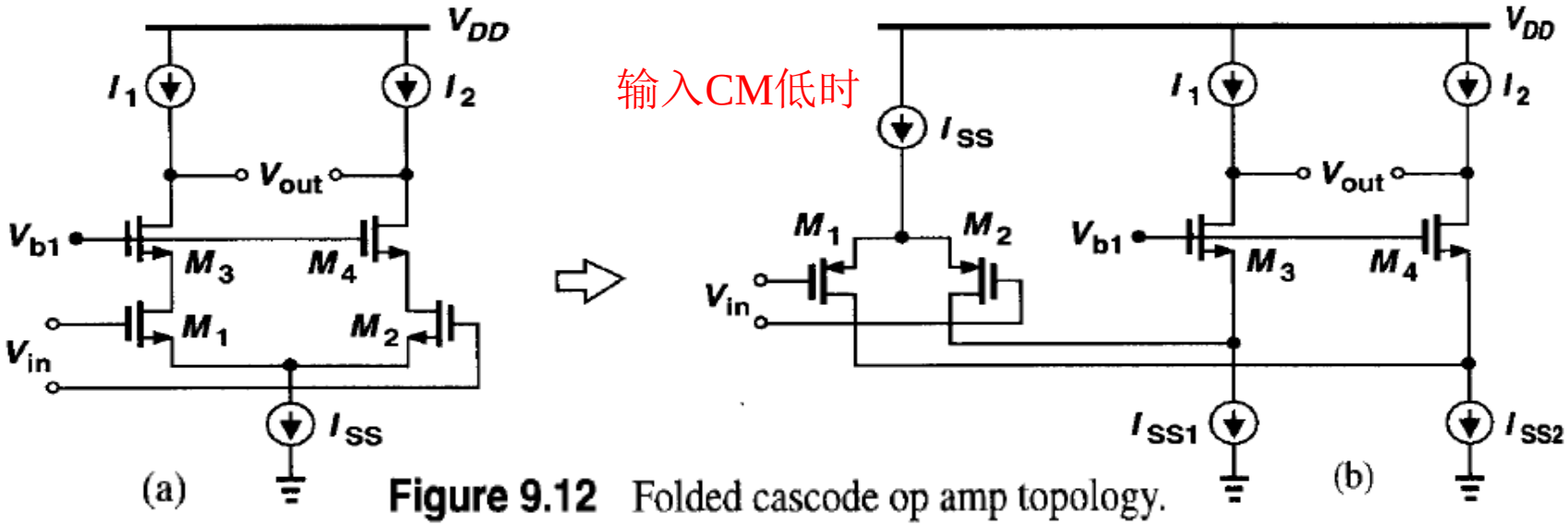


Figure 9.12 Folded cascode op amp topology.

$$I_{SS1} = I_{SS}/2 + I_{D3}$$

two important differences between the two circuits.

(1) the folded- cascode configuration generally consumes higher power.

(2) In Fig. 9.12(a), the input CM level cannot exceed $V_{b1} - V_{GS3} + V_{TH1}$, whereas in Fig. 9.12(b), it cannot be *less* than $V_{b1} - V_{GS3} - |V_{THP}|$

It is therefore possible to design the latter to allow shorting its input and output terminals with negligible swing limitation.

the maximum output voltage swing of the folded-cascode op amp

the lower end of the swing is given by $V_{OD3} + V_{OD5}$ and the upper end by $V_{DD} - (|V_{OD7}| + |V_{OD9}|)$.

Thus, the peak-to-peak swing on each side is equal to

$$V_{DD} - (V_{OD3} + V_{OD5} + |V_{OD7}| + |V_{OD9}|).$$

输入共模范围大，输出范围也有所增大

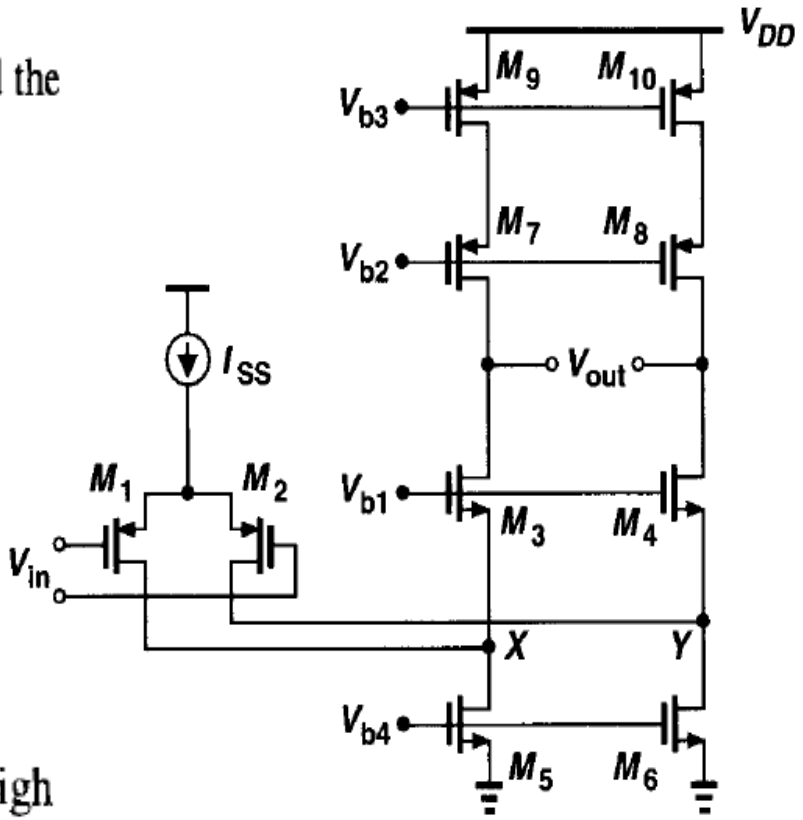


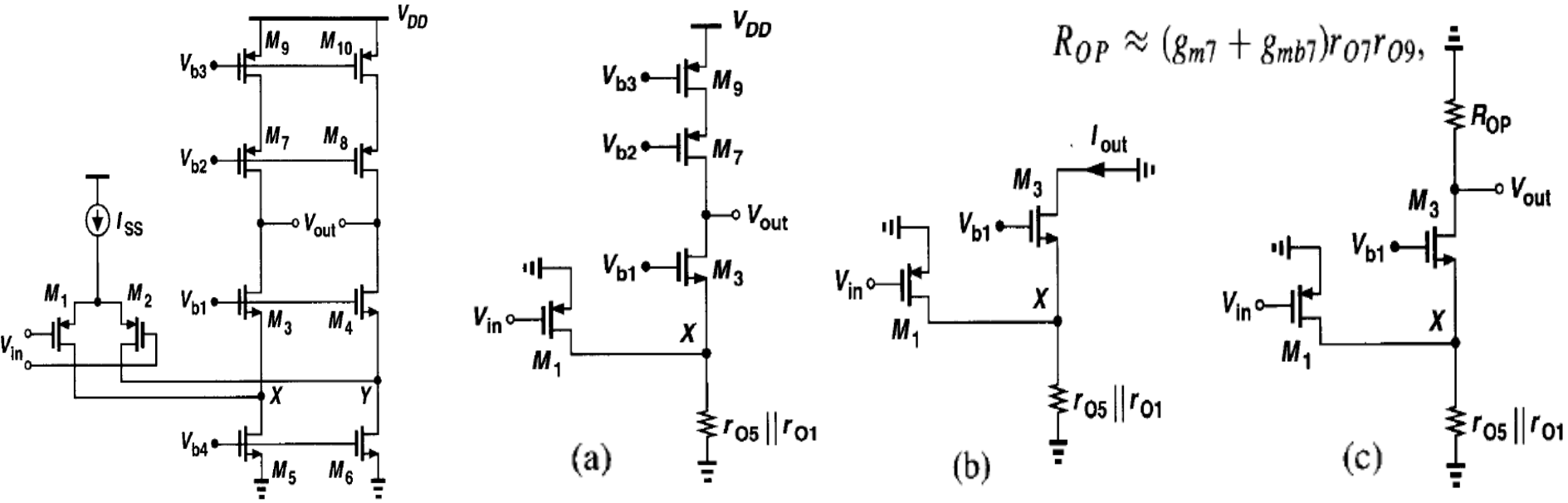
Figure 9.13 Folded cascode op amp with cascode PMOS loads.

carrying a large current, M_5 and M_6 may require a high overdrive voltage if their capacitance contribution to nodes X and Y is to be minimized.

if the device currents and widths scale together, $g_m r_O$ of each transistor and hence the open-loop gain of the op amp remain constant.

$$g_m r_O \propto \sqrt{WL/I_D}.$$

the small-signal voltage gain of the folded-cascode op amp



$$R_{OP} \approx (g_{m7} + g_{mb7}) r_{O7} r_{O9},$$

Figure 9.14 (a) Half circuit of folded cascode op amp, (b) equivalent circuit with output shorted to ground, (c) equivalent circuit with output open.

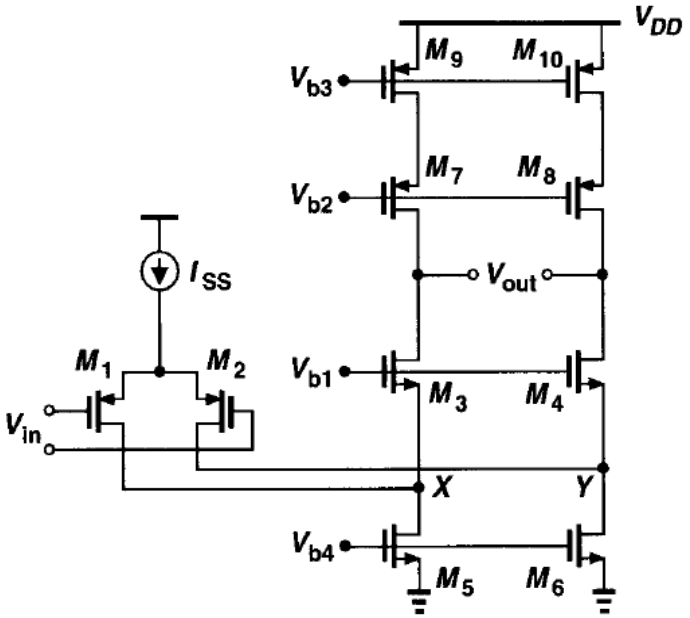
$$|A_v| = G_m R_{out}$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_{m1} V_{in}}{V_{in}} \times \frac{g_{m3} + g_{mb3}}{(r_{o5} \| r_{o1})^{-1} + (g_{m3} + g_{mb3})} \approx g_{m1}$$

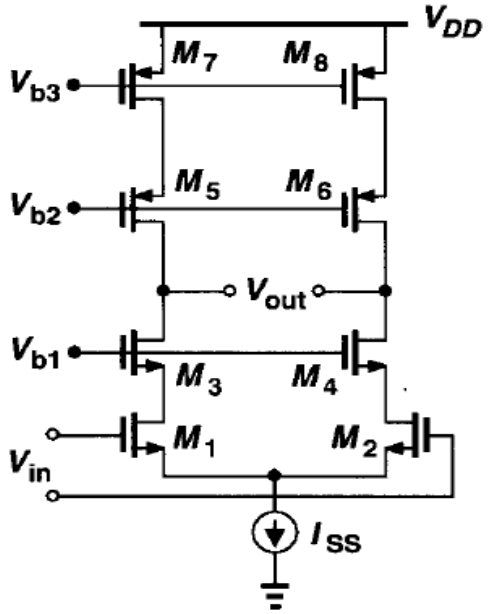
$$R_{out} \approx R_{OP} \| [(g_{m3} + g_{mb3}) r_{O3} (r_{O1} \| r_{O5})]$$

$$|A_v| \approx g_{m1} \{ [(g_{m3} + g_{mb3}) r_{O3} (r_{O1} \| r_{O5})] \| [(g_{m7} + g_{mb7}) r_{O7} r_{O9}] \}. \qquad (9.12)$$

Folded cascode compare with telescopic cascode



放大器核心指标：
1. 低频增益
2. 3dB带宽
   或单位增益带宽



$$|A_v| \approx g_{m1}\{[(g_{m3}+g_{mb3})r_{O3}(r_{O1}\|r_{O5})]\|[(g_{m7}+g_{mb7})r_{O7}r_{O9}]\} \quad (9.12)$$

$$|A_v| \approx g_{m1}[(g_{m3}r_{O3}r_{O1})\|(g_{m5}r_{O5}r_{O7})] \quad (4.53)$$

For comparable device dimensions and bias currents, the PMOS input differential pair exhibits a lower transconductance than does an NMOS pair. r_{O1} and r_{O5} appear in parallel, the gain in (9.12) is usually two to three times lower than that of a comparable telescopic cascode.

Folded compared with telescopic (cont.)

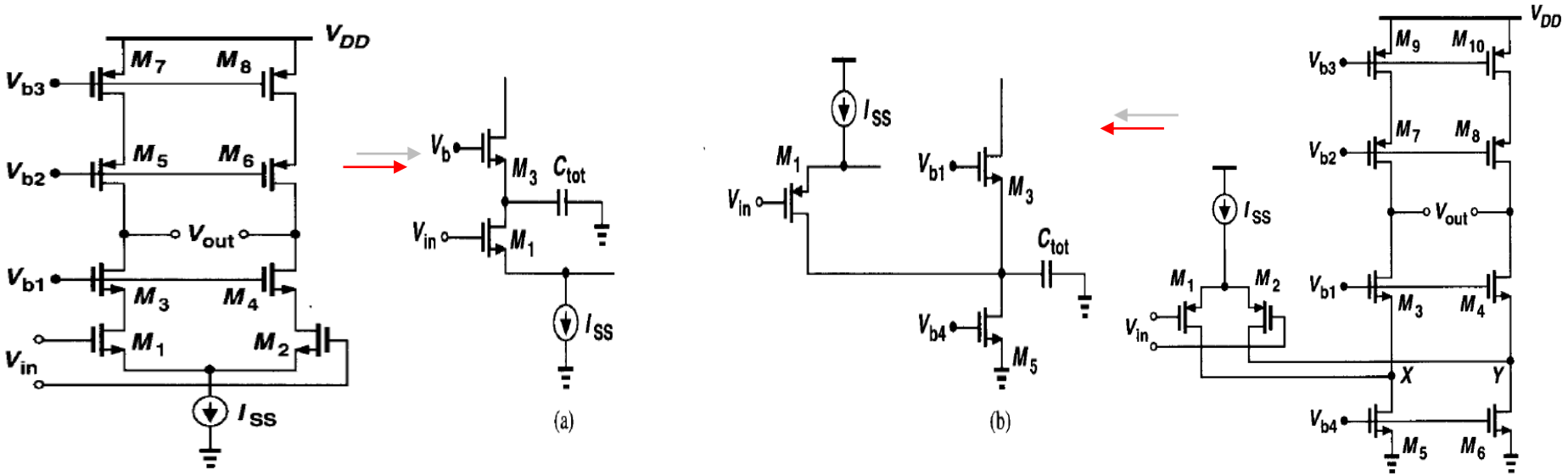
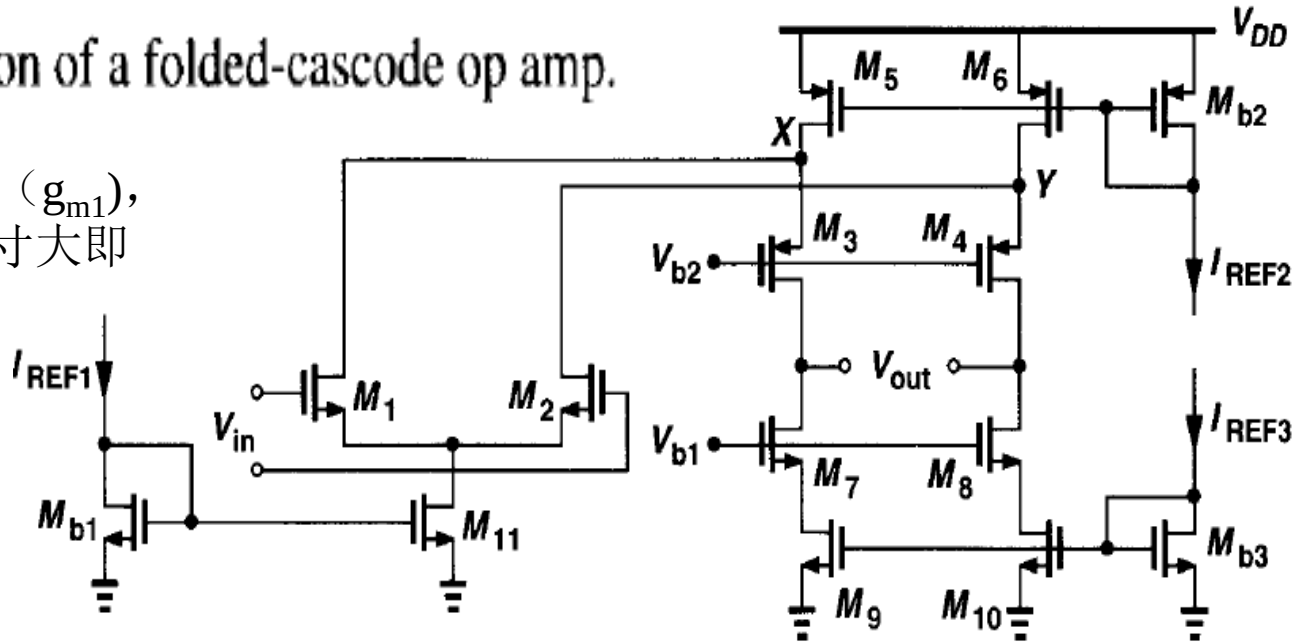


Figure 9.15 Effect of device capacitance on the nondominant pole in telescopic and folded-cascode op amps.

It is also worth noting that the pole at the "folding point," i.e., the sources of M_3 and M_4, is quite closer to the origin than that associated with the source of cascode devices in a telescopic topology. In Fig. 9.15(a), C_{tot} arises from C_{GS3}, C_{SB3}, C_{DB1}, and C_{GD1}. By contrast, in Fig. 9.15(b), C_{tot} contains additional contributions due to C_{GD5} and C_{DB5}, typically significant components because M_5 must be wide enough to carry a large current with a small overdrive.

输入共模电平高时的folded-cascode

Figure 9.16 Realization of a folded-cascode op amp.



与图9.13比较，增益大（g_{m1}），X点时间常数大(P管尺寸大即C_X大， 或g_{m3}小)

but at the cost of lowering the pole at the folding point.

note that the pole at node X is given by the product of $1/(g_{m3}+g_{mb3})$ and the total capacitance at this node.

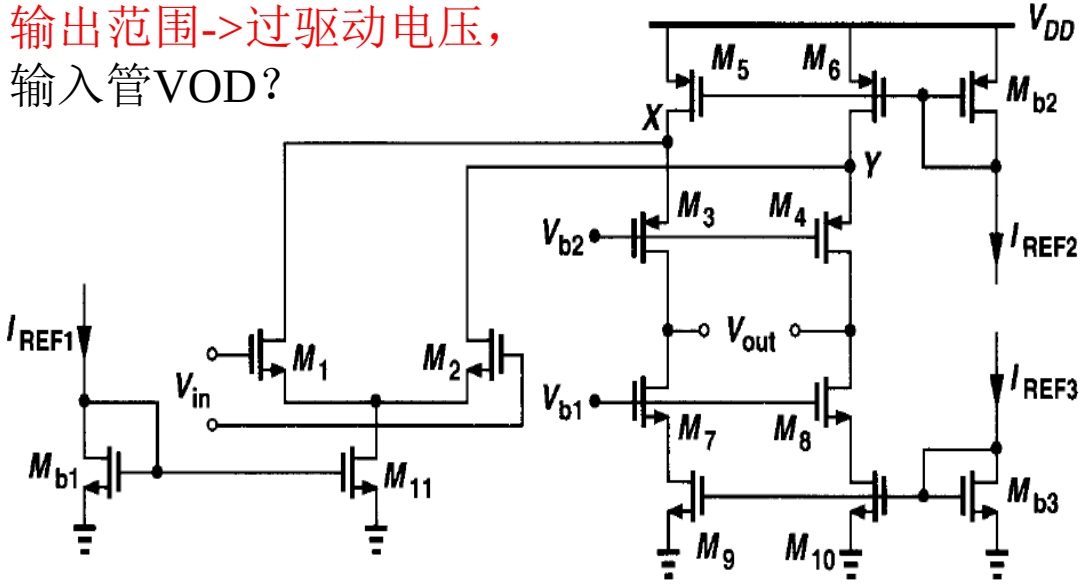
M_3 suffers from a low transconductance and M_5 contributes substantial capacitance because it must be wide enough to carry the drain currents of both M_1 and M_3.

for comparable bias currents, M_5-M_6 in Fig. 9.16 may be several times wider than M_5-M_6 in Fig. 9.13.

Example 9.6

Design a folded-cascode op amp with an NMOS input pair (Fig. 9.16) to satisfy the following specifications: $V_{DD} = 3$ V, differential output swing = 3 V, power dissipation = 10 mW, voltage gain = 2000. Use the same device parameters as in Example 9.5.

输出范围->过驱动电压，
输入管VOD?



Solution

we begin with the power and swing specifications.

Allocating 1.5 mA to the input pair, 1.5 mA to the two cascode branches, 330 μA to the three current mirrors,

V_{TH}=0.7V, 分配$V_{OD5,6}$=0.5V，$V_{OD3,4}$=0.4V, $V_{OD7\sim10}$=0.3V

$$(W/L)_{5,6} = 400, (W/L)_{3,4} = 313, (W/L)_{7-10} = 278.$$

Since the minimum and maximum output levels are equal to 0.6 V and 2.1 V, respectively, the optimum output common-mode level is 1.35 V.

Example 9.6 (cont.)

The minimum dimensions of M_1-M_2 are dictated by the minimum input common-mode level, $V_{GS1} + V_{OD11}$

if the input and the output are shorted, then $V_{GS2} + V_{OD11} = 1.35$ V.

With $V_{OD11} = 0.4$ V, we have $V_{GS1} = 0.95$ V, obtaining $V_{OD1,2} = 0.95 - 0.7 = 0.25$ V and hence $(W/L)_{1,2} = 400$.

The maximum dimensions of M_1 and M_2 are determined by the tolerable input capacitance and the capacitance at nodes X and Y in Fig. 9.16.

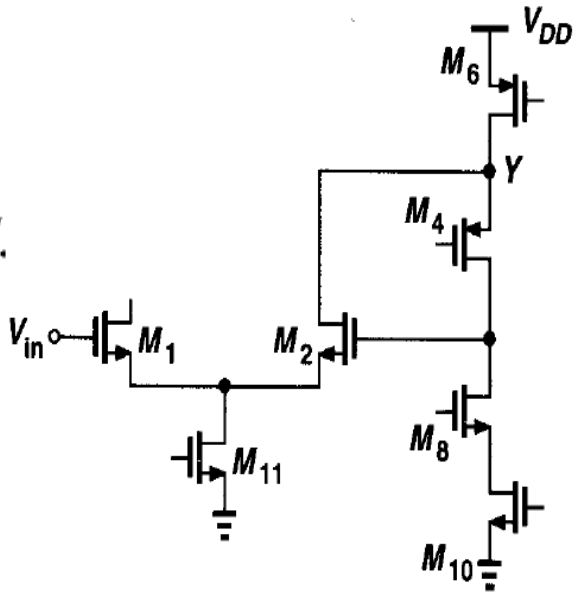
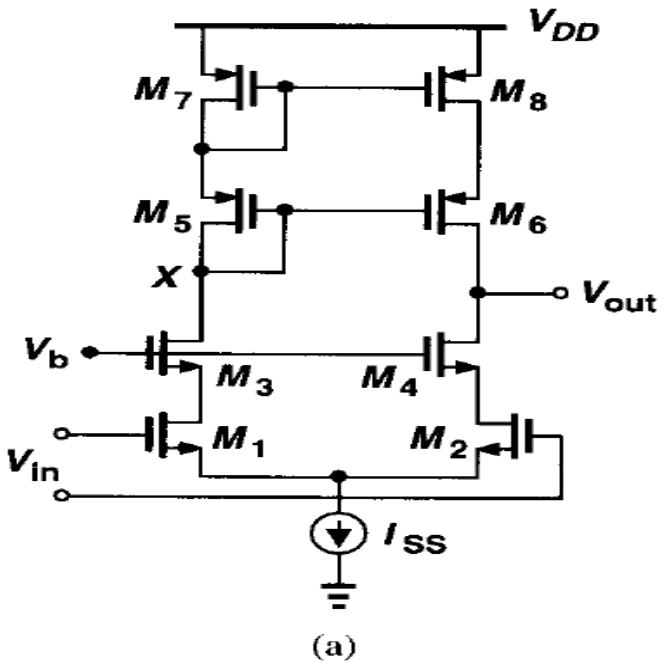


Figure 9.17 Folded-cascode op amp with input and output shorted.

An important property of folded-cascode op amps is the capability of handling input common-mode levels close to one of the supply rails. In Fig. 9.16, for example, the CM voltage at the gates of M_1 and M_2 can be equal to V_{DD} because $V_X = V_Y = V_{DD} - 500$ mV. By the same token, a similar topology using a PMOS input pair can accommodate input CM levels as low as zero.

单端输出的cascode 电流镜运放



$$V_X = V_{DD} - |V_{GS5}| - |V_{GS7}|,$$

limiting the maximum value of V_{out} to

$$V_{DD} - |V_{GS5}| - |V_{GS7}| + |V_{TH6}|$$

"wasting" one PMOS threshold voltage in the swing

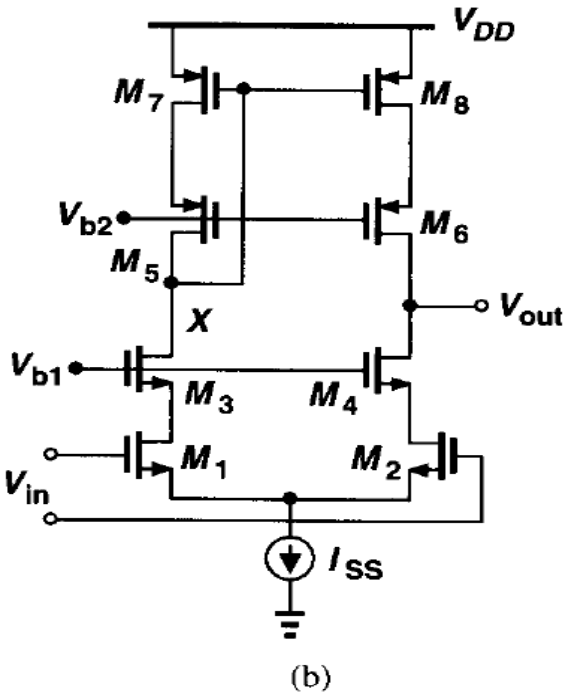
it contains a mirror pole at node X
thus limiting the speed of feedback systems

Figure 9.18 Cascode op amps with single-ended output.

---

one-stage op amps allow the small-signal current produced by the input pair to flow directly through the output impedance. The gain of these topologies is therefore limited to the product of the input pair transconductance and the output impedance. We have also observed that cascoding in such circuits increases the gain while limiting the output swings.

增大单端输出范围的cascode 电流镜运放

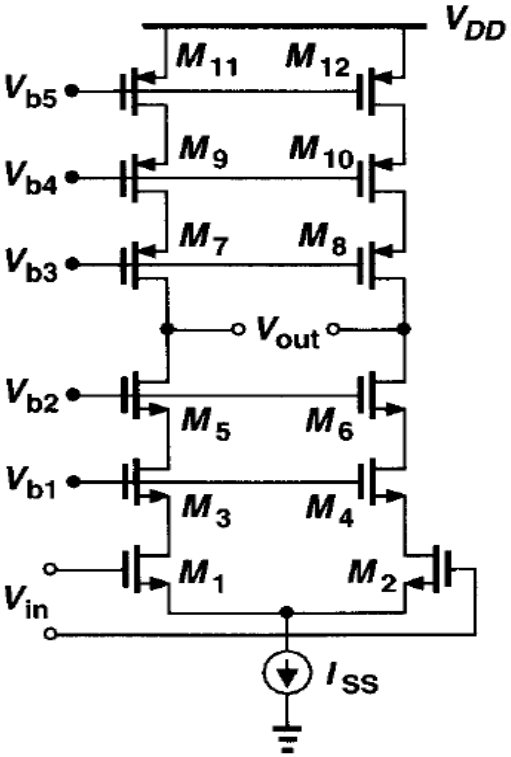


(b)

M_7 and M_8 are biased at the edge of the triode region.

Similar ideas apply to folded-cascode op amps as well.

不适合低电压电源，一般用两级cascode



It is preferable to use the differential topology, although it requires a feedback loop to define the output common-mode level

9.3 two-stage OP amps

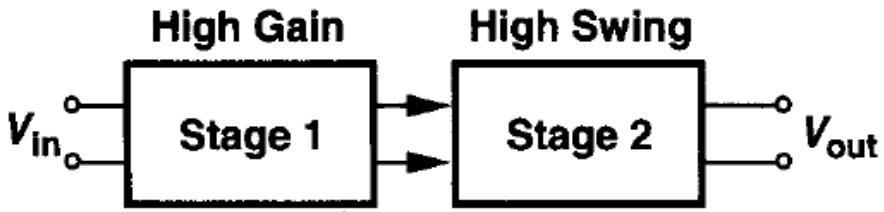
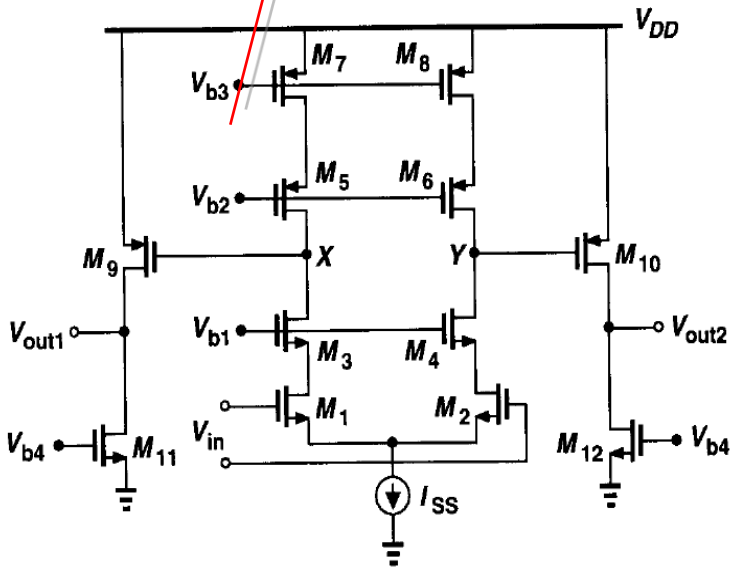


Figure 9.20 Two-stage op amp.

the second stage is typically configured as a simple common-source stage so as to allow maximum output swings.



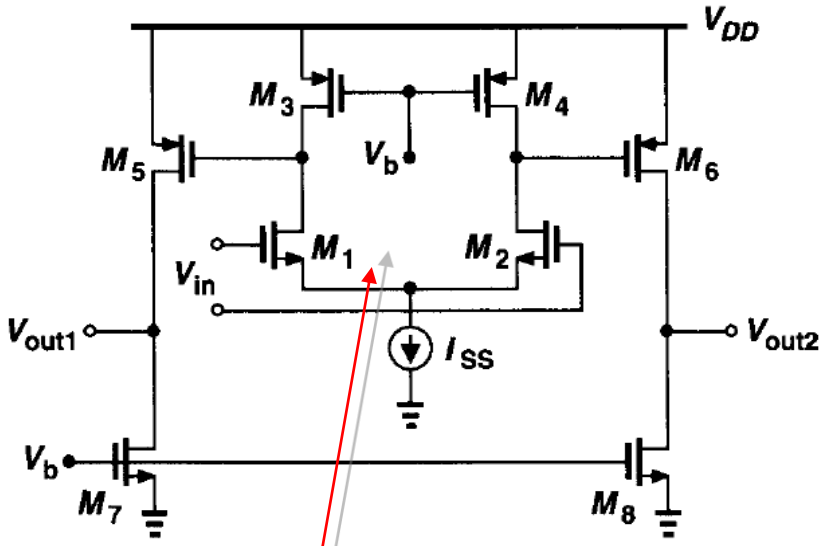
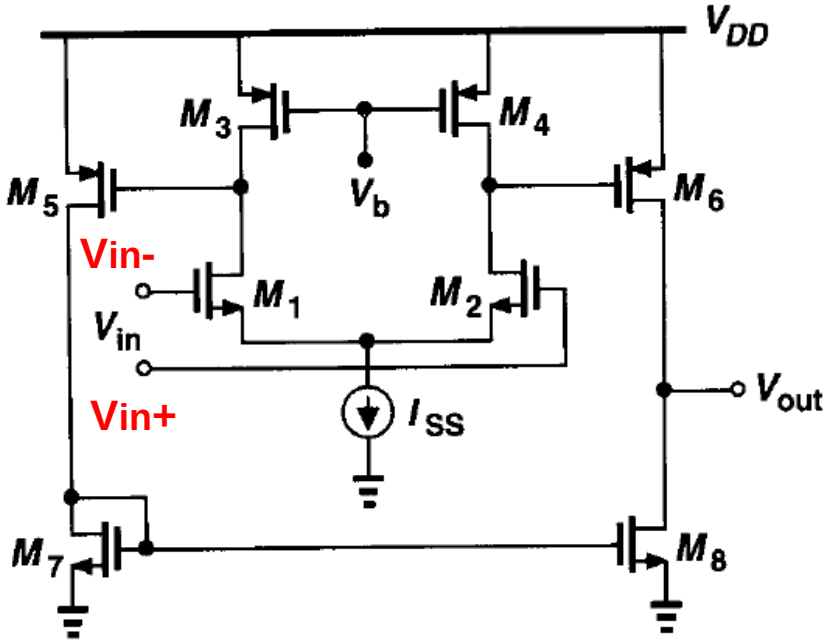


Figure 9.21 Simple implementation of a two-stage op amp.

gains equal to $g_{m1,2}(r_{O1,2} \| r_{O3,4})\, g_{m5,6}(r_{O5,6} \| r_{O7,8})$,

$$A_v \approx \{g_{m1,2}[(g_{m3,4} + g_{mb3,4})r_{O3,4}r_{O1,2}] \| [(g_{m5,6} + g_{mb5,6})r_{O5,6}r_{O7,8}]\} \times [g_{m9,10}(r_{O9,10} \| r_{O11,12})]. \quad (9.13)$$

A two-stage op amp may provide a single-ended output



Note that if the gate of M_1 is shorted to V_{out2} to form a unity-gain buffer, then the minimum allowable output level is equal to $V_{GS1} + V_{ISS}$, severely limiting the output swing.

Fully differential current source OP need CMFB!

Figure 9.23 Two-stage op amp with single-ended output. 差动输入单端输出

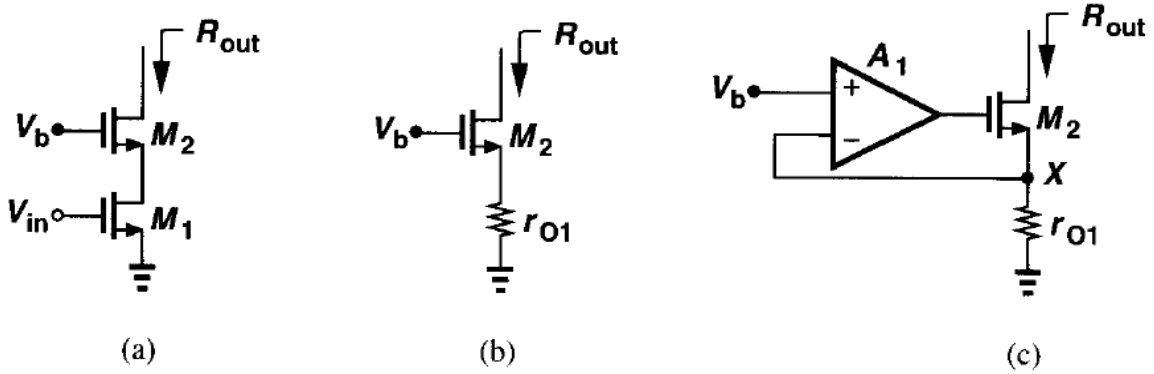
Can we cascade more than two stages to achieve a higher gain?

each gain stage introduces at least one pole in the open-loop transfer function, making it difficult to guarantee stability in a feedback system using such an op amp.

9.4 gain boosting(提高)

提高低频增益：如何提高输出阻抗？减小电流变化！

The idea behind gain boosting is to further increase the output impedance without adding more cascode devices.



the idea is to drive the gate of M_2 by an amplifier that forces V_X to be equal to V_b.

current-voltage feedback.

反馈放大器*Vb*为输入

Figure 9.24 Increasing the output impedance by feedback.

前馈(开环）放大器：$G_m = A_1 \dfrac{1}{\dfrac{1}{g_{m2}} + r_{o1}}$

开环输出电阻：$g_{m2} r_{o2} r_{o1}$

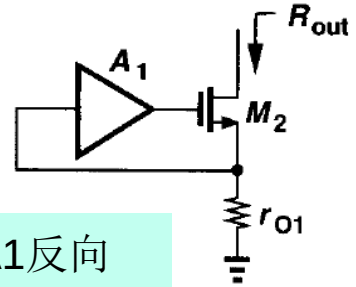
反馈系数：$\beta = R_f = r_{o1}$

闭环输出电阻：

$R_{out} = g_{m2} r_{o2} r_{o1}(1 + G_m R_f)$

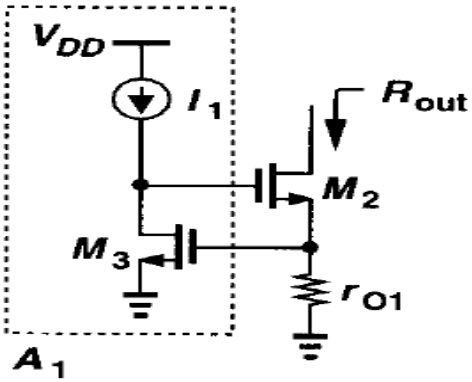
$= g_{m2} r_{o2} r_{o1}\left(1 + A_1 \dfrac{1}{\dfrac{1}{g_{m2}} + r_{o1}} r_{o1}\right) \approx A_1 g_{m2} r_{o2} r_{o1}$

gain boosting (cont.)

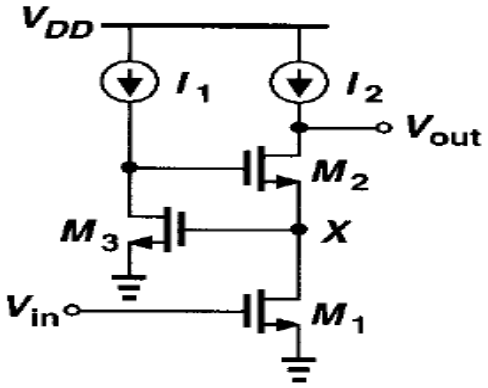


A1反向

(a)



(b)



(c)

半边电路的小信号通道

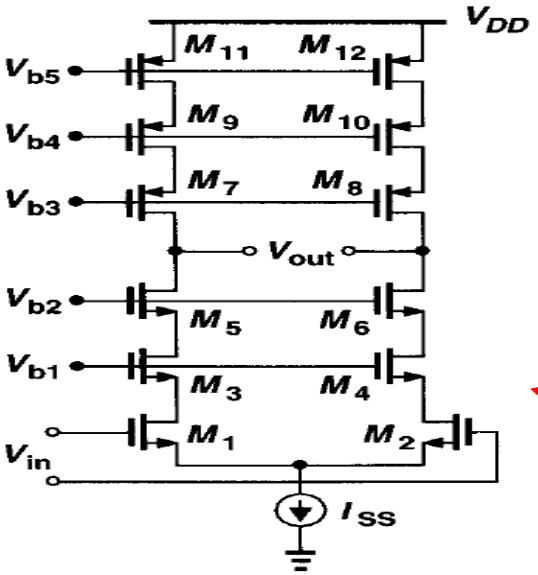


Figure 9.25 Gain boosting in cascode stage.

$$R_{out} \approx A_1 g_{m2} r_{O2} r_{O1}$$

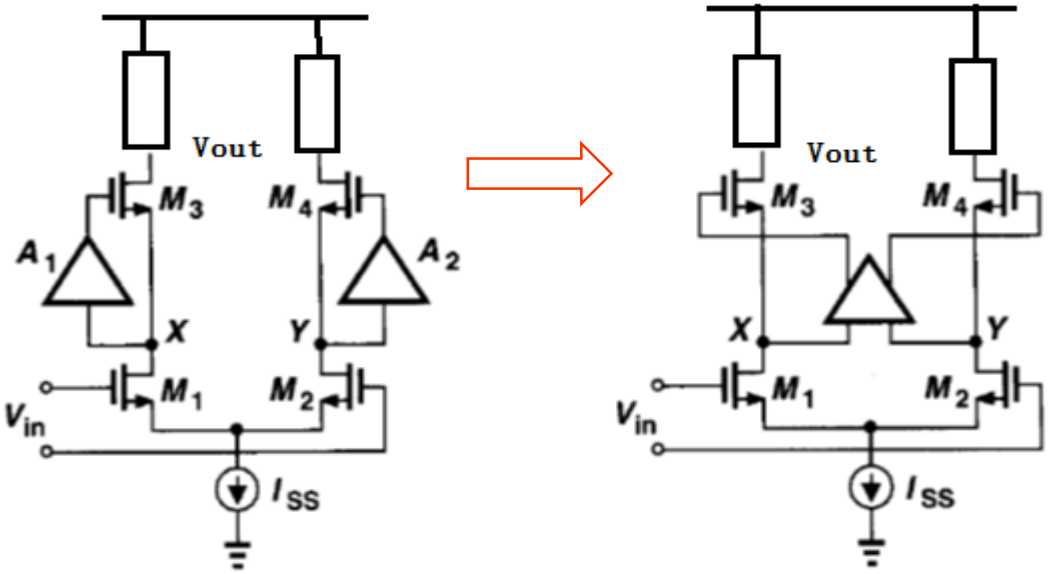
假设理想电流源I1和I2，则

$$|A_v| \approx g_{m1}(g_{m2} r_{O2} r_{O1})(g_{m3} r_{O3}),$$

similar to the gain of a *triple* cascode.

a "triple cascode," providing a gain on the order of $(g_m r_O)^3/2$

apply gain boosting to a differential cascode stage



A_1和A_2反向放大器Figure 9.26

单级差动放大器
同侧的输入与输出反向

apply gain boosting to a differential cascode stage

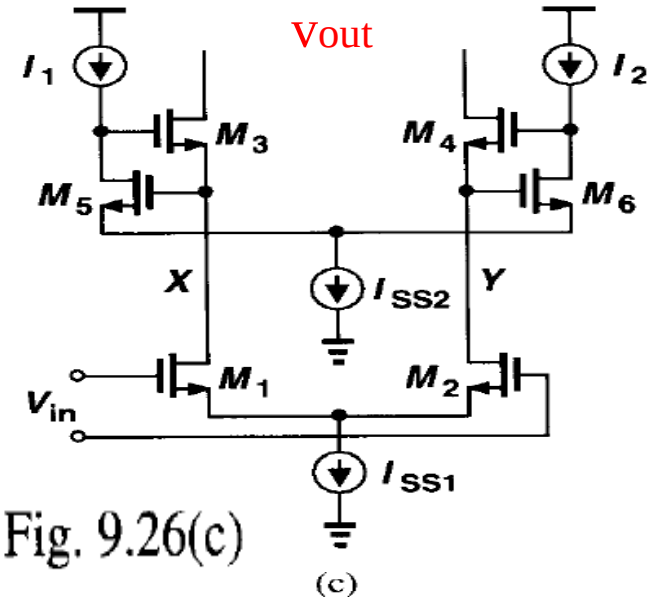


Fig. 9.26(c)

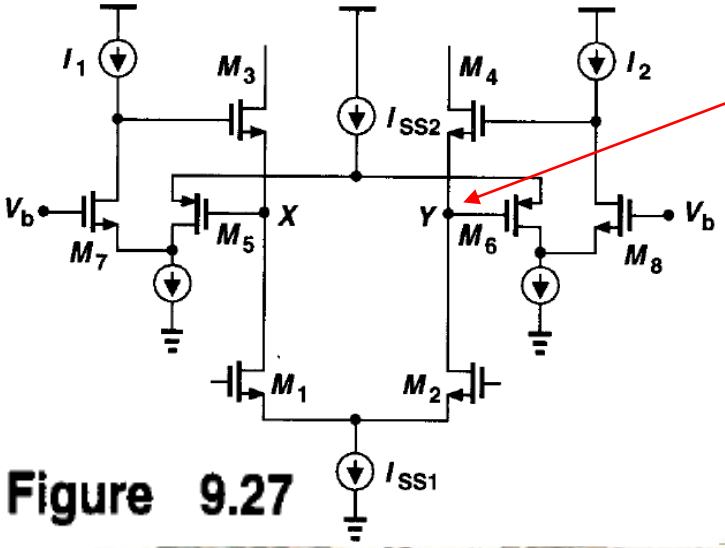


Figure 9.27

VX=VGS5+VISS，浪费了Vth

In a simple differential cascode, on the other hand, the minimum would be approximately one threshold voltage lower.

The voltage swing limitation in Fig. 9.26(c) results from the fact that the gain-boosting amplifier incorporates **(用…实现)** an NMOS differential pair.

X and Y are sensed by a PMOS pair, the minimum value of V_X and V_Y is not dictated by the gain-boosting amplifier.

the minimum allowable level of V_X and V_Y is given by $V_{OD1,2} + V_{ISS1}$.

Folded-cascode circuit used as auxiliary amplifier.

Example 9.7

Calculate the output impedance of the circuit shown in Fig. 9.27.

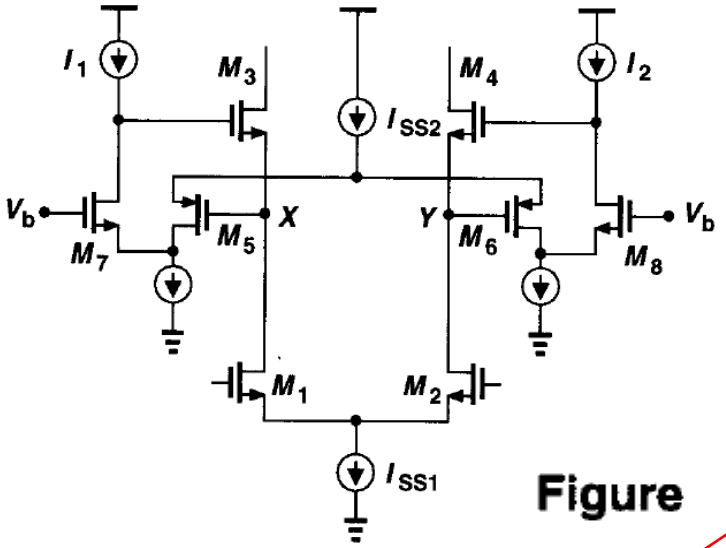
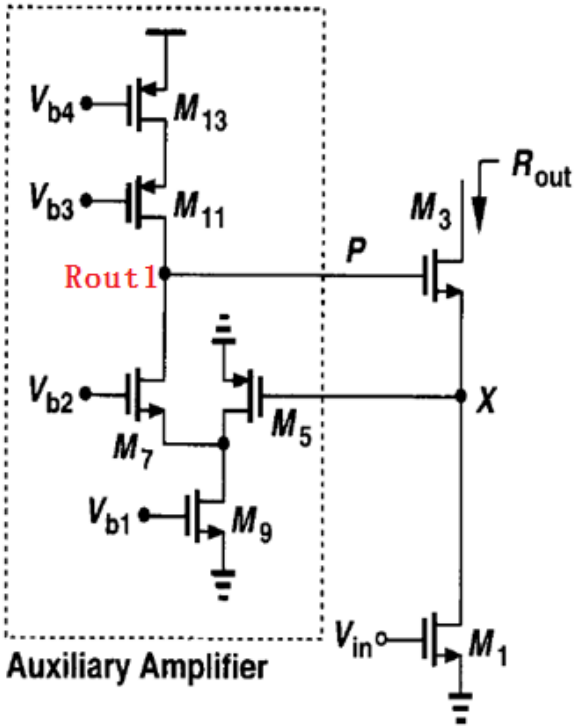


Figure 9.27



半边电路（小信号）

Figure 9.28

Solution

The voltage gain from X to P is approximately equal to $g_{m5}R_{out1}$,

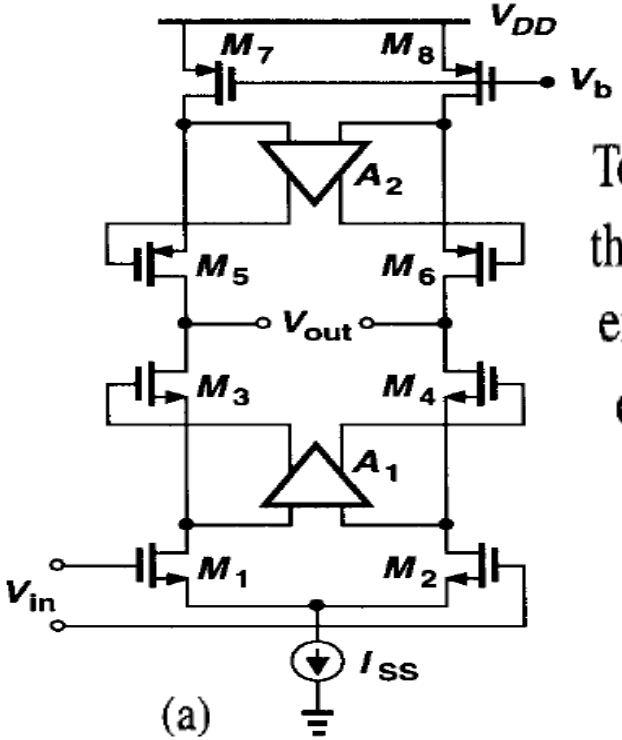
P点阻抗 where $R_{out1} \approx [g_{m7}r_{O7}(r_{O9}\|r_{O5})]\|(g_{m11}r_{O11}r_{O13})$.

由 (9.14) $R_{out} \approx g_{m3}r_{O3}r_{O1}g_{m5}R_{out1}$.

the overall output impedance is similar to that of a "quadruple" cascode.

Gain boosting is applied to load current source

Regulated cascodes can also be utilized in the load current sources of a cascode op amp.



To allow maximum swings at the output, amplifier A_2 must employ an NMOS input differential pair.

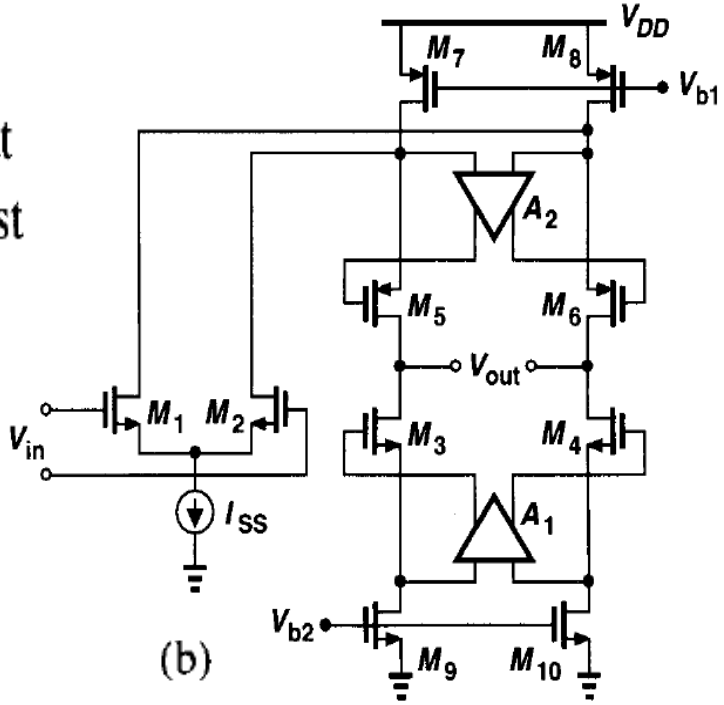


Figure 9.29 Gain boosting applied to both signal path and load devices.

In contrast to two-stage op amps, where the entire signal experiences the poles associated with each stage, in a gain-boosted op amp, most of the signal directly flows through the cascode devices to the output. Only a small "error" component is processed by the gain-boosting amplifier and "slowed down."

comparison

Table 9.1 Comparison of performance of various op amp topologies.

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

9.6 Common-Mode Feedback (CMFB)

fully differential

avoid mirror poles, thus achieving a higher closed-loop speed.

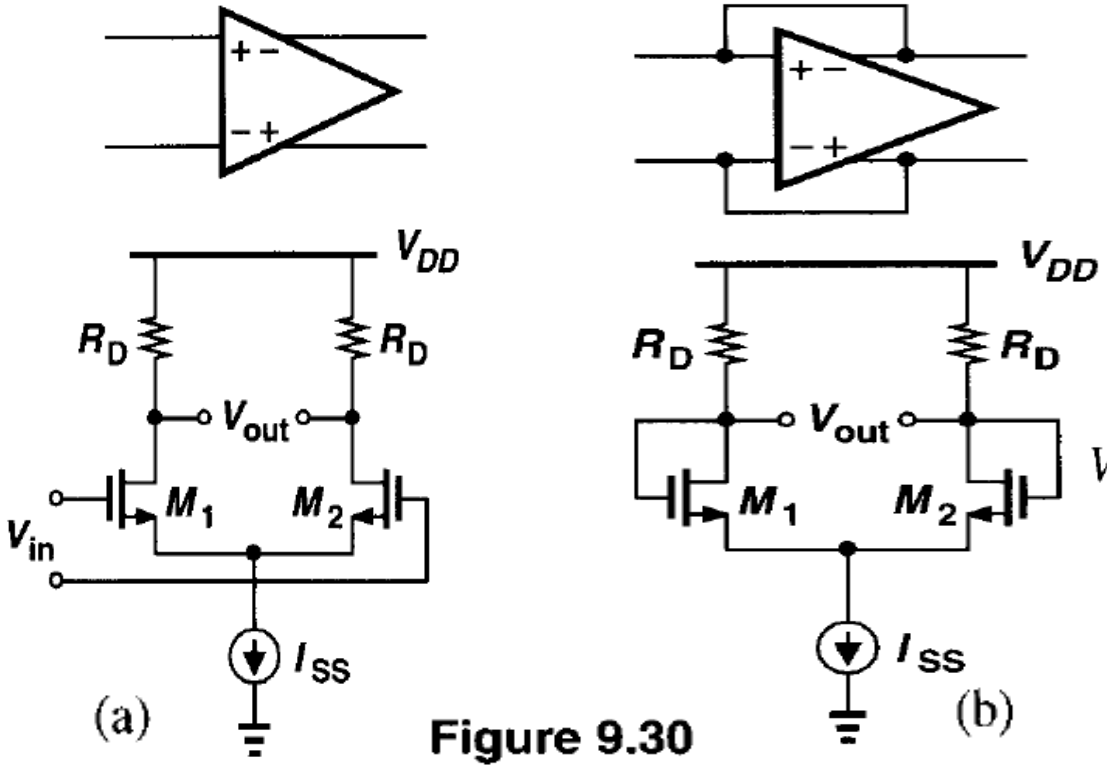


Figure 9.30

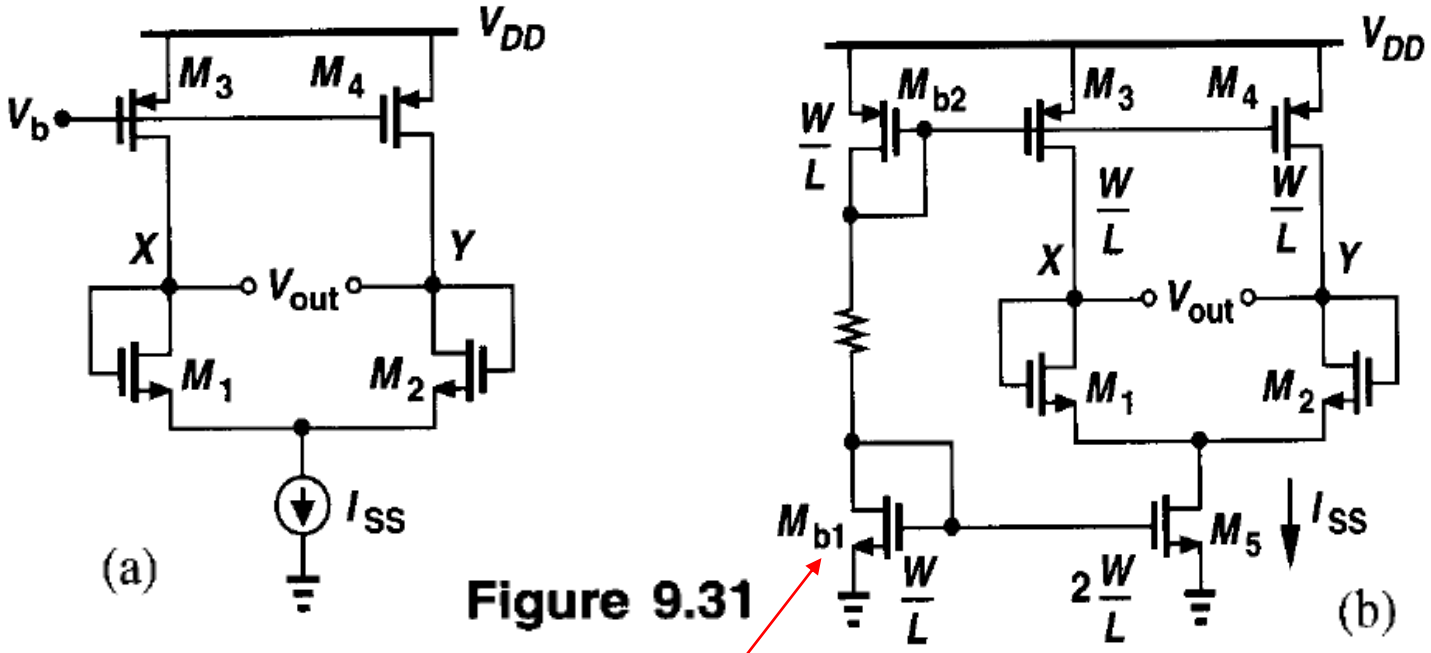
(a) Simple differential pair,

(b) circuit with inputs shorted to outputs.

$V_{DD} - I_{SS}R_D/2.$

共模电平确定

电流负载CM电平不确定



共模电平不确定

Figure 9.31

(a) High-gain differential pair with inputs shorted to outputs

(b) effect of current mismatches.

mismatches in the PMOS and NMOS current mirrors defining I_{SS} and $I_{D3,4}$ create a finite error between $I_{D3,4}$ and $I_{SS}/2$.

differential feedback cannot define the CM level.

Example 9.8

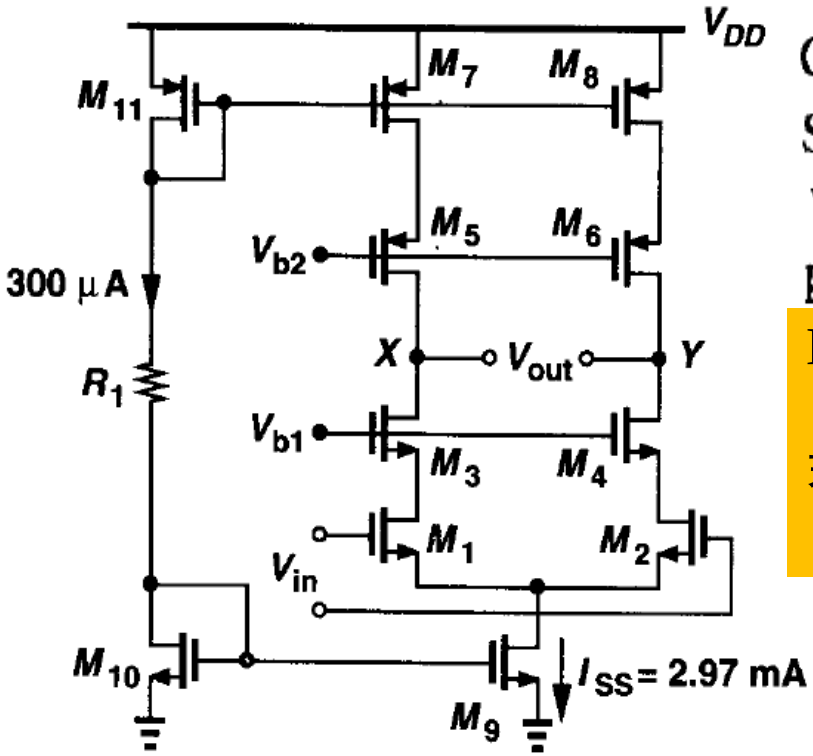


Figure 9.33

Consider the telescopic op amp designed in Example 9.5 Suppose M_9 suffers from a 1% current mismatch with respect to M_{10}, producing $I_{SS} = 2.97$ mA rather than 3 mA.

MOS非理想电流源，可被强制增加或减少电流，导致MOS管V_{DS}增大或减少；

若MOS近似为理想电流源，则被强制减少电流时，V_{DS}减小MOS管进入线性区。

the difference between the drain currents of M_3 and M_5 (and M_4 and M_6) is 30 μA/2 = 15 μA, V_X and V_Y must rise so much that M_5-M_6 and M_7-M_8 enter the triode region, yielding $I_{D7,8} = 1.485$ mA.

We should also mention that another important source of CM error in the simple biasing scheme of Fig. 9.33 is the *deterministic* error between $I_{D7,8}$ and I_{11} (and also between I_{D9} and I_{D10}) due to their different drain-source voltages. This error can nonetheless be reduced by means of the current mirror techniques of Chapter 5.

CMFB原理性电路

The foregoing study implies that in high-gain amplifiers, the output CM level is quite sensitive to device properties and mismatches and it cannot be stabilized by means of *differential* feedback. Thus, a common-mode feedback network must be added to sense the CM level of the two outputs and accordingly adjust one of the bias currents in the amplifier.

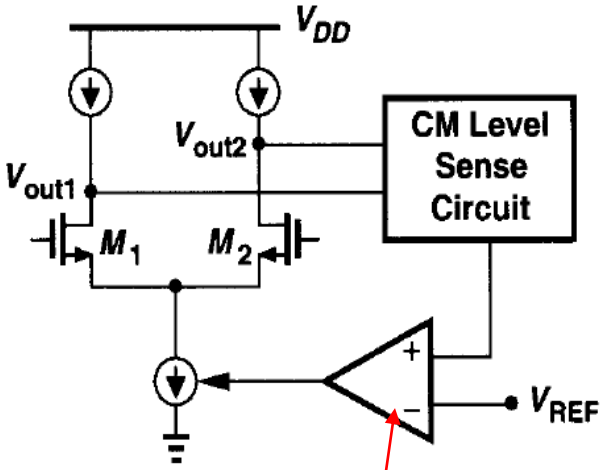


Figure 9.34 Conceptual topology for common-mode feedback.

比较器输出电平范围要合适

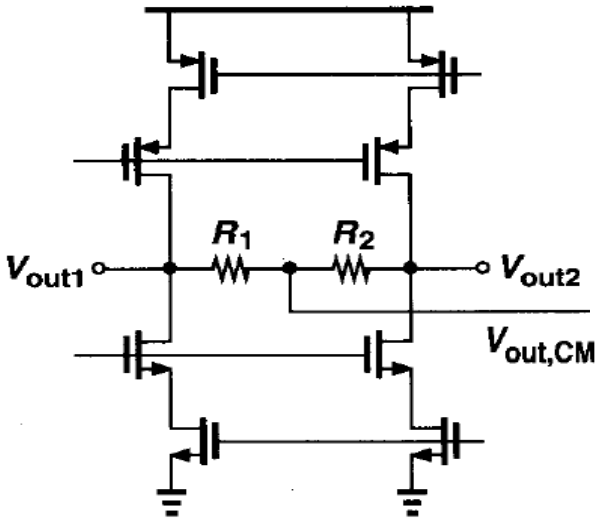


Figure 9.35 Common-mode feedback with resistive sensing.

The difficulty, however, is that R_1 and R_2 must be much greater than the output impedance of the op so as to avoid lowering the open loop gain. such large resistors occupy a very large area and suffer from substantial parasitic capacitance to the substrate.

一种CM检测电路

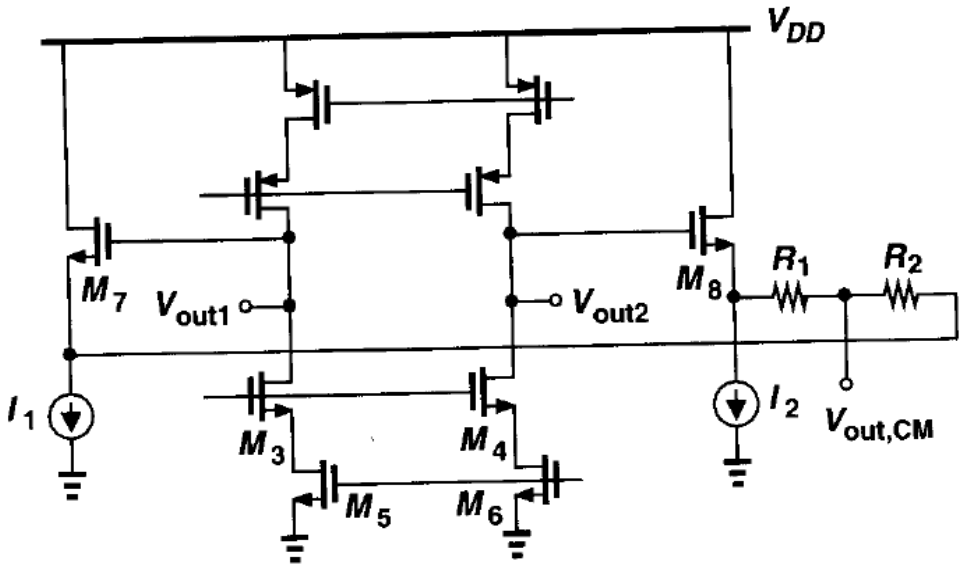


Figure 9.36 Common-mode feedback using source followers.

produces a CM level that is in fact lower than the output CM level by $V_{GS7,8}$, but this shift can be taken into account in the comparison operation.

Note that R_1 and R_2 or I_1 and I_2 must be large enough to ensure that M_7 or M_8 is not "starved" when a large differential swing appears at the output.

The sensing method suffers from an important drawback: it limits the differential output swings the minimum allowable level of V_{out1} (and V_{out2}) without CMFB it would be equal to $V_{OD3} + V_{OD5}$. With the source followers in place, $V_{out1,min} = V_{GS7} + V_{I1}$ Thus, the swing at each output is reduced by approximately V_{TH}

此处CM检测电路对信号通路的输出电压范围有影响

偏置电路的控制

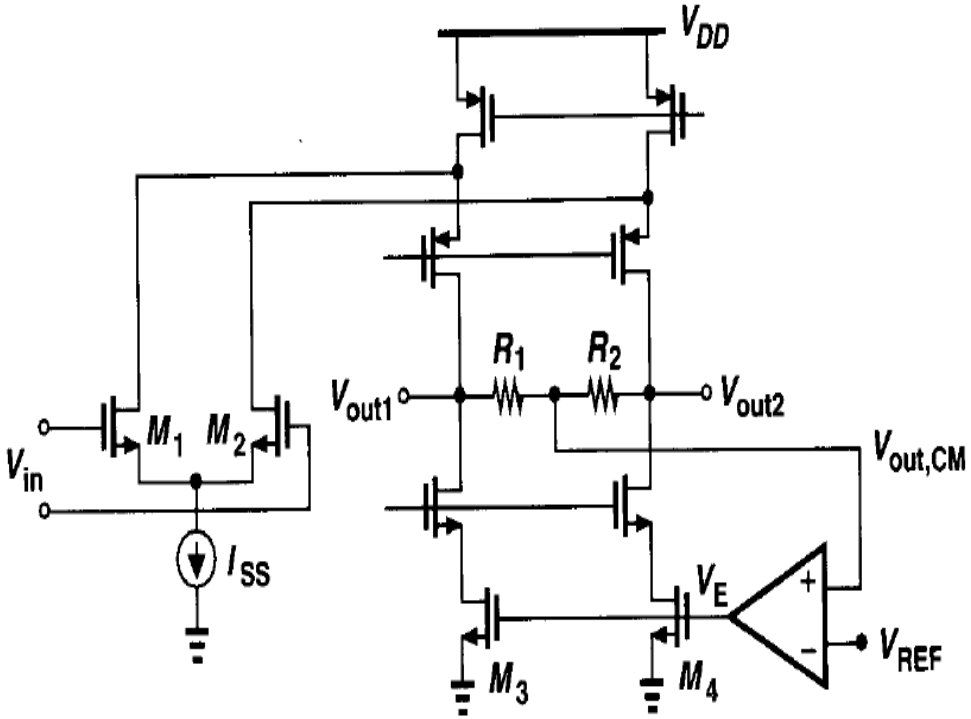


Figure 9.39 Sensing and controlling output CM level.

detect the difference between $V_{out,CM}$ and a reference voltage, V_{REF}, applying the result to the NMOS current sources with negative feedback.

the feedback network forces the CM level of V_{out1} and V_{out2} to approach V_{REF}.

Note that the feedback can be applied to the PMOS current sources as well.

each of M_3 and M_4 can be decomposed into two parallel devices, one biased at a constant current and the other driven by the error amplifier. allow optimization of the settling behavior.

CMFB in a folded-cascode op amp

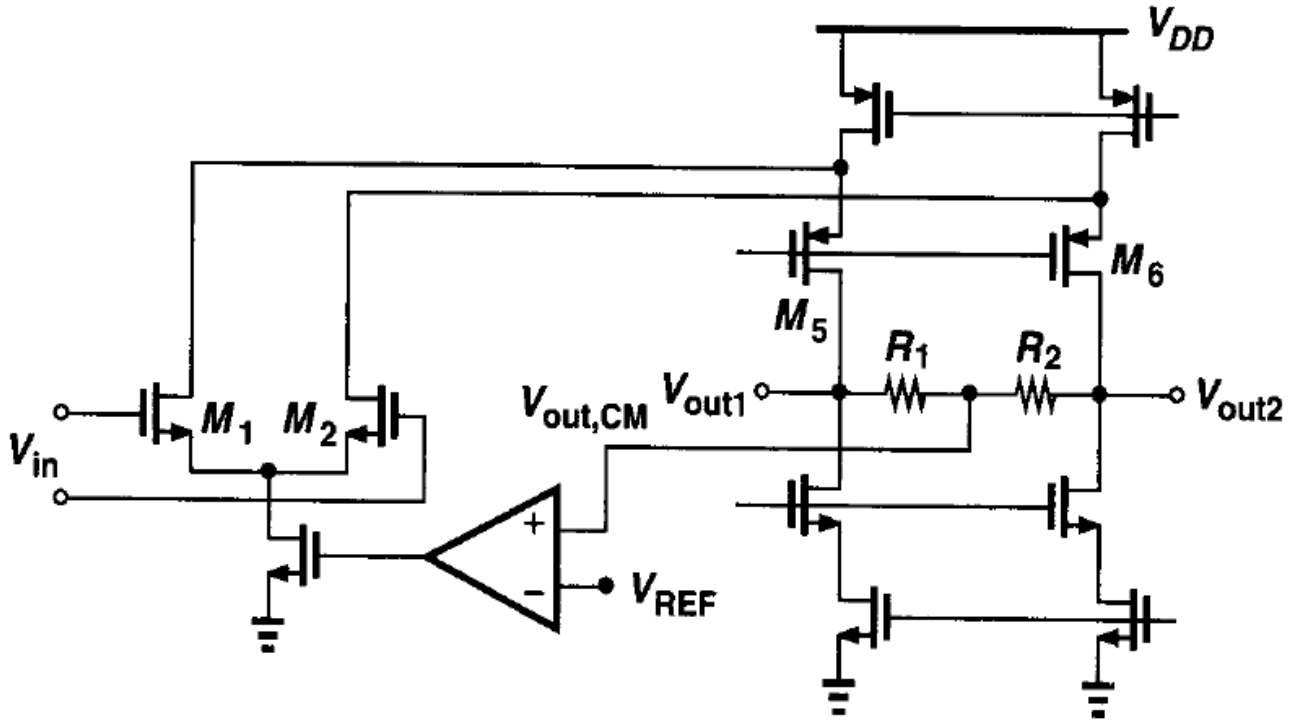
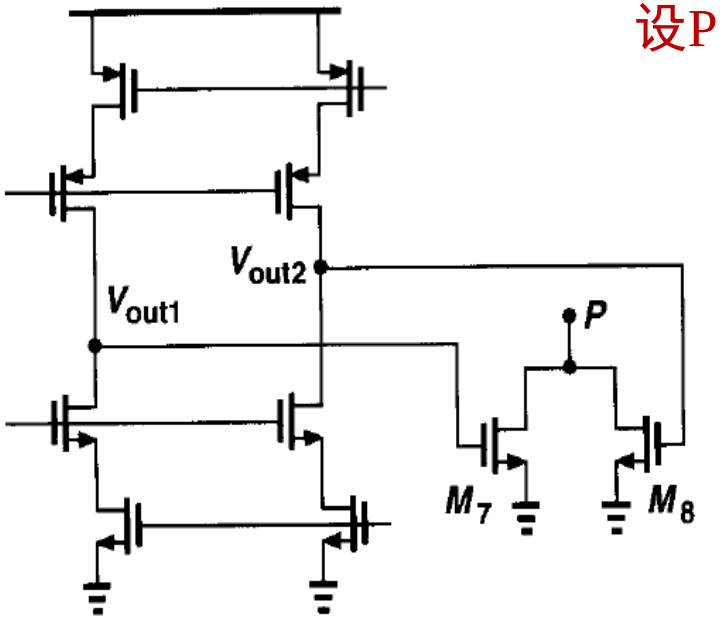


Figure 9.40 Alternative method of controlling output CM level.

另一种CM检测方法



设P点电位很低（M7、M8线性电阻区）

total resistance between P and ground

$$R_{tot} = R_{on7} \| R_{on8}$$

$$= \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out1} - V_{TH})} \Bigg\| \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out2} - V_{TH})}$$

$$= \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{out2} + V_{out1} - 2V_{TH})},$$

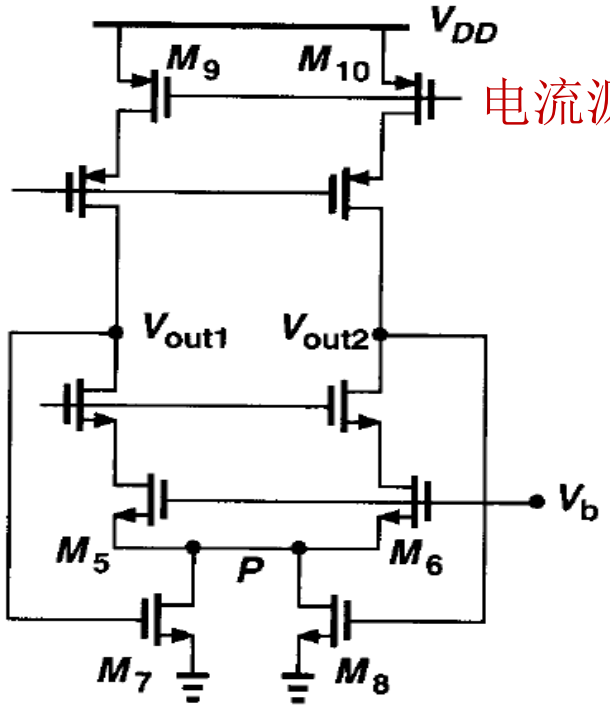
$V_{out1}+V_{out2}=2V_{OCM}$

Figure 9.38 Common-mode sensing using MOSFETs operating in deep triode region.

both M_7 and M_8 operate in deep triode region. limits the output voltage swings.

In fact, if, say, V_{out1} drops from the equilibrium CM level to one threshold voltage above ground and V_{out2} rises by the same amount, then M_7 enters the saturation region, thus exhibiting a variation in its on-resistance that is not counterbalanced by that of M_8.

CMFB using triode devices



电流源

Figure 9.41 CMFB using triode devices.

CM voltage is directly converted to a resistance or a current,

Assuming $I_{D9} = I_{D10} = I_D$,
we must have $V_b - V_{GS5} = 2I_D(R_{on7} \| R_{on8})$

hence

$$R_{tot} = R_{on7} \| R_{on8}$$

$$= \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{7,8}(V_{out2} + V_{out1} - 2V_{TH})} = \frac{V_b - V_{GS5}}{2I_D}$$

that is,

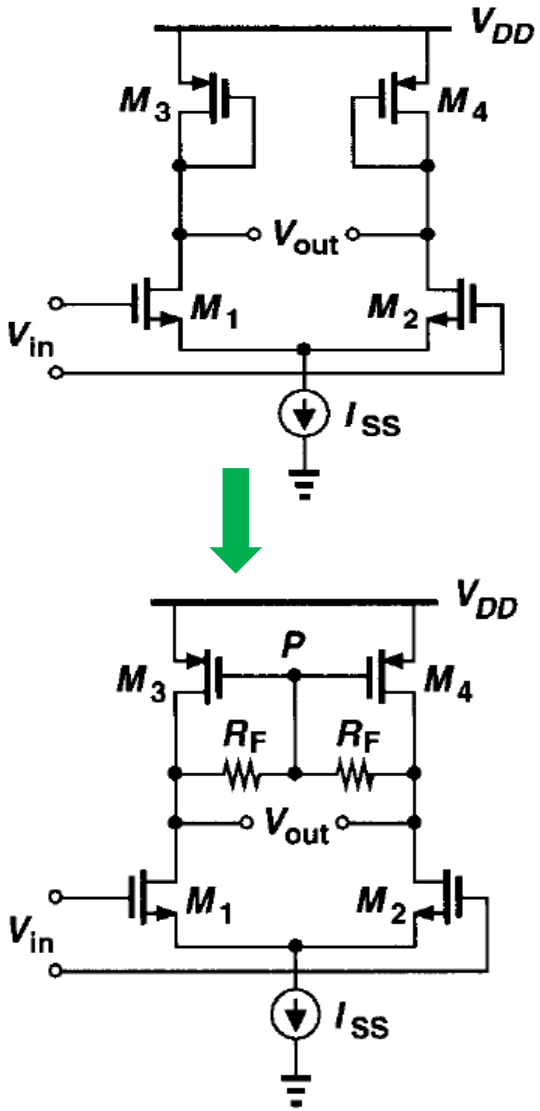
$$V_{out1} + V_{out2} = \frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{7,8}} \frac{1}{V_b - V_{GS5}} + 2V_{TH} \qquad (9.18)$$

$$V_{GS5} = \sqrt{2I_D/[\mu_n C_{ox}(W/L)_5]} + V_{TH5}. \qquad (9.19)$$

前提：V_{out1}和V_{out2}变化范围不大，保证M7和M8在深线性区

不很准，受温度和工艺偏差影响

二极管负载的简单差分对CMFB



the output CM level, $V_{DD} - V_{GS3,4}$, is relatively well-defined but the voltage gain is quite low.

对于共模信号，P点为电平确定的V_{OCM}

M_3 and M_4 operate as diode-connected devices.

对于差动信号，**P为虚地**。增益为：

$$g_{m1,2}(r_{O1,2} \| r_{O3,4} \| R_F)$$

9.7 input range limitations

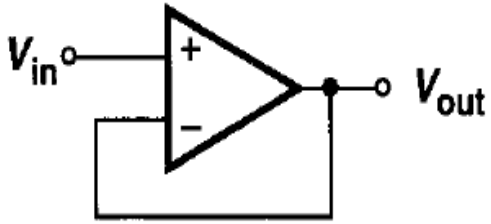
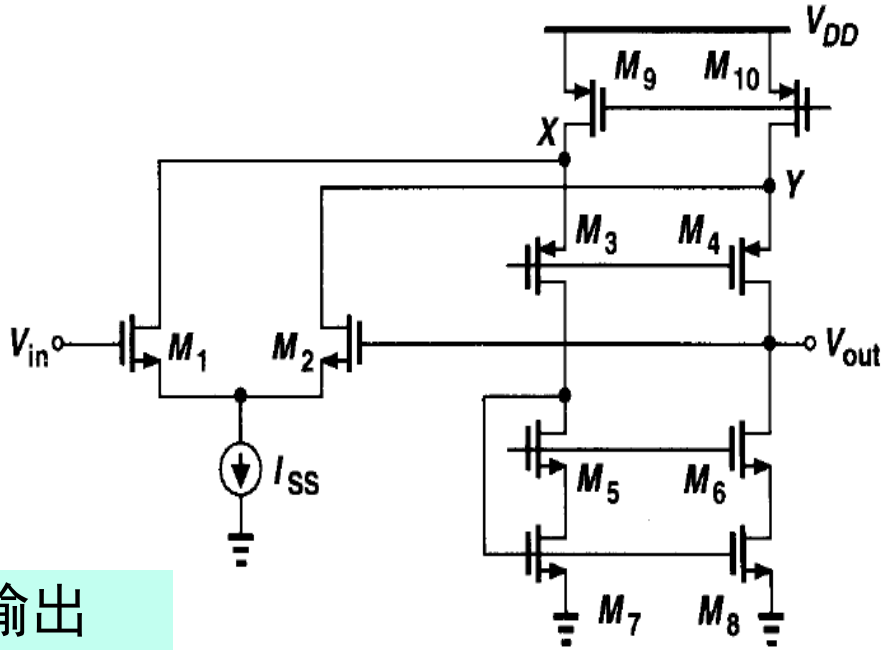


Figure 9.47 Unity-gain buffer.

电压跟随器有最大带宽、最强驱动（负载能力），最可能不稳定



电流镜单端输出

Specifically, $V_{in,min} \approx V_{out,min} = V_{GS1,2} + V_{ISS}$, approximately one threshold voltage higher than the allowable minimum provided by M_5-M_8.

What happens if V_{in} falls below the minimum given above? The MOS transistor operating as I_{SS} enters the triode region, decreasing the bias current of the differential pair and hence lowering the transconductance. We then postulate that the limitation is overcome if the transconductance can somehow be restored.

An approach to extend the input CM range

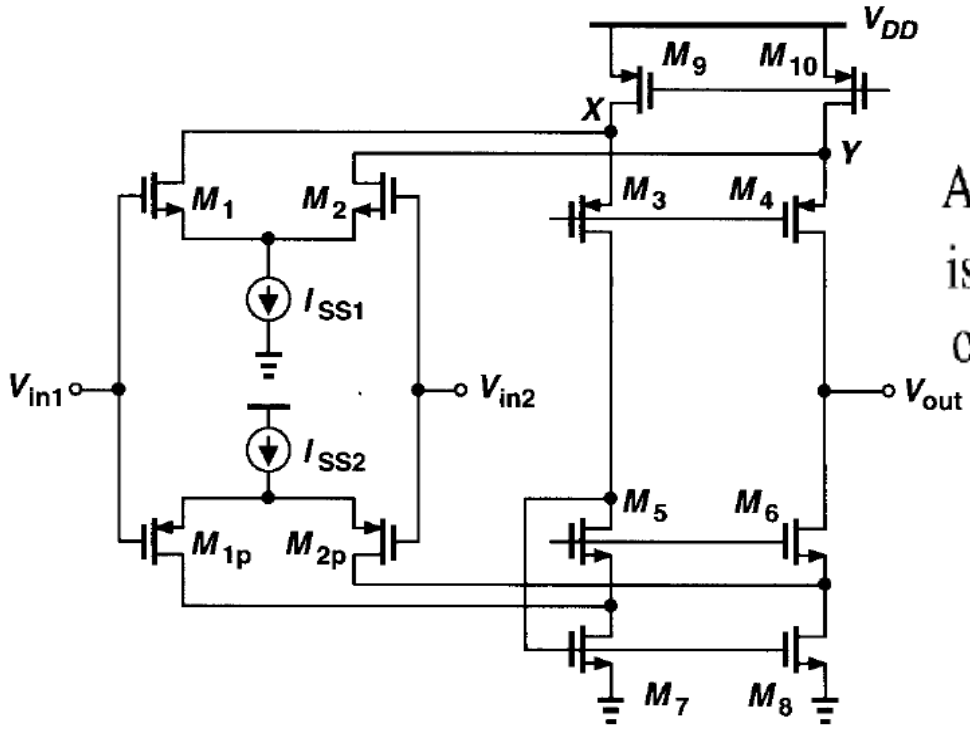


Figure 9.48 Extension of input CM range.

An important concern in the circuit of Fig. 9.48 is the *variation* of the overall transconductance of the two pairs as the input CM level changes.

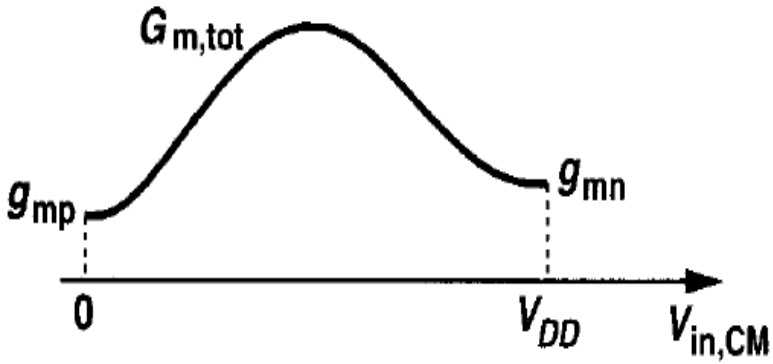


Figure 9.49 Variation of equivalent transconductance with the input CM level.

电流镜单端输出

负反馈运算电路仅需要大增益，与增益具体值无关。

9.8 slew rate（SR转换速率，大信号特性）

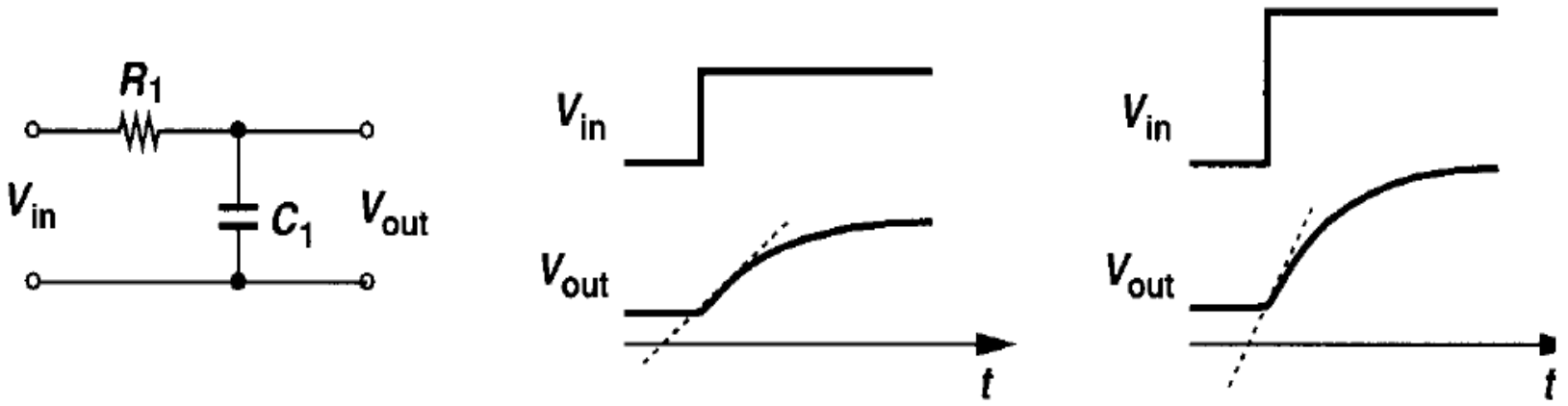


Figure 9.50 Response of a linear circuit to input step.

$$V_{out} = V_0[1 - \exp(-t/\tau)], \text{ where } \tau = RC,$$

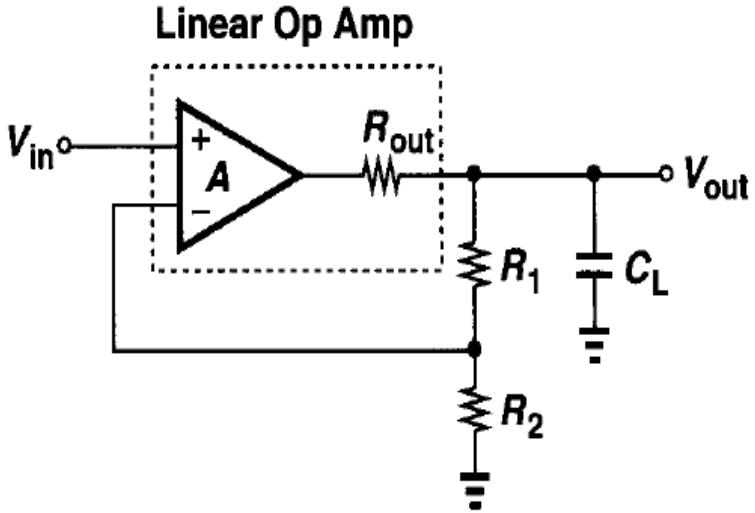
压摆率：

$$\frac{dV_{out}}{dt} = \frac{V_0}{\tau}\exp\frac{-t}{\tau}.$$

输出斜率应正比于输出（输入）幅度

the slope of the step response is proportional to the final value of the output; call the slope of the ramp the "slew rate."

Response of linear op amp to step input



$$\left[\left(V_{in} - V_{out}\frac{R_2}{R_1+R_2}\right)A - V_{out}\right]\frac{1}{R_{out}} = \frac{V_{out}}{R_1+R_2} + V_{out}C_L s.$$

Assuming $R_1 + R_2 \gg R_{out}$, we have

$$\frac{V_{out}}{V_{in}}(s) \approx \frac{A}{\left(1 + A\dfrac{R_2}{R_1+R_2}\right)\left[1 + \dfrac{R_{out}C_L}{1 + AR_2/(R_1+R_2)}s\right]}$$

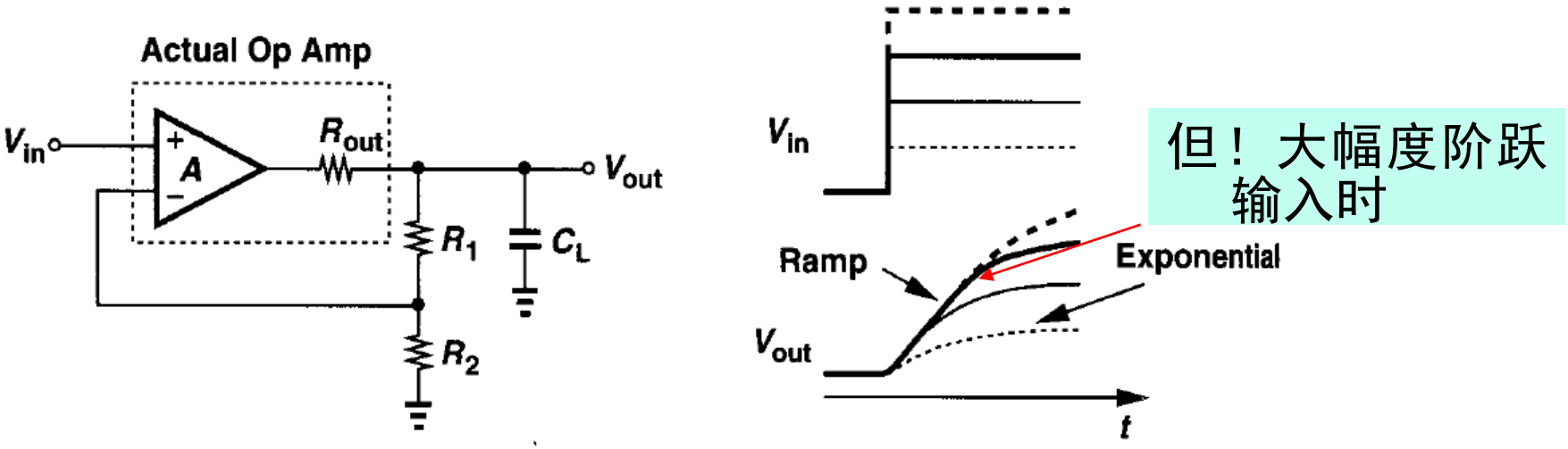
Figure 9.51 Response of linear op amp to step response.

如$R_1+R_2>>R_{out}$不满足，有反馈支路负载作用

The step response is therefore given by

$$V_{out} = V_0 \frac{A}{1 + A\dfrac{R_2}{R_1+R_2}}\left(1 - \exp\frac{-t}{\dfrac{C_L R_{out}}{1 + AR_2/(R_1+R_2)}}\right)u(t), \qquad (9.28)$$

Response of linear op amp to step input (cont.)



但！大幅度阶跃输入时

Figure 9.52 Slewing in an op amp circuit.

With a realistic op amp, on the other hand, the step response of the circuit begins to deviate from (9.28) as the input amplitude increases. Illustrated in Fig. 9.52, the response to sufficiently small inputs follows the exponential of Eq. (9.28), but with large input steps, the output displays a linear *ramp* having a *constant slope*. Under this condition, we say the op amp experiences slewing and call the slope of the ramp the "slew rate."

slewing is a nonlinear phenomenon.

Understanding the origin of slew

大阶跃输入

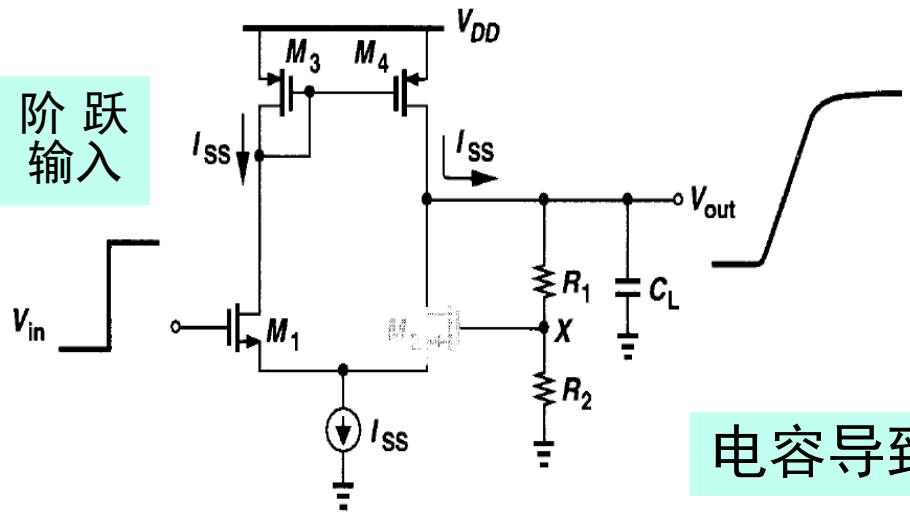


Figure 9.54 Slewing during low-to-high transition.

电容导致斜坡

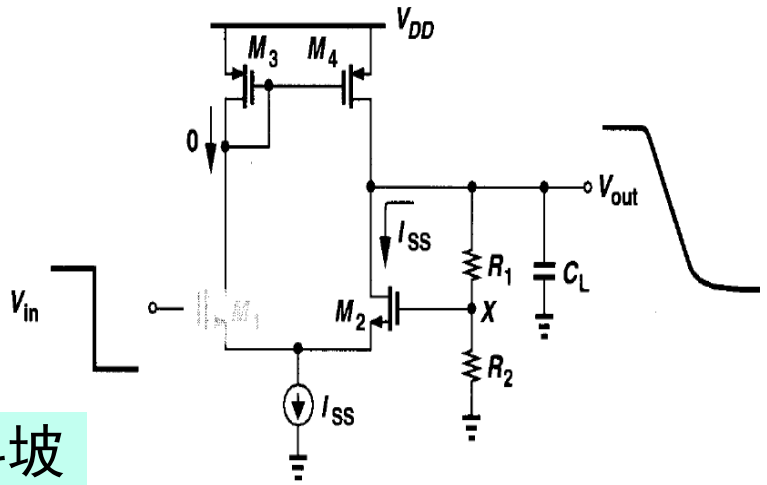


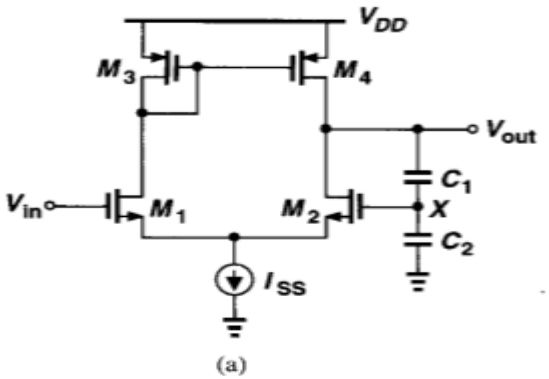
Figure 9.55 Slewing during high-to-low transition.

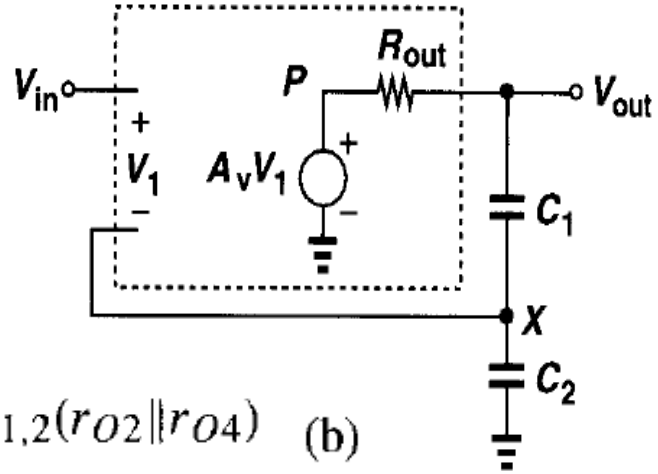
Slewing is an undesirable effect in high-speed circuits that process large signals. While the small-signal bandwidth of a circuit may suggest a fast time-domain response, the large-signal speed may be limited by the slew rate simply because the current available to charge and discharge the dominant capacitor in the circuit is small. Moreover, since the input-output relationship during slewing is nonlinear, the output of a slewing amplifier exhibits substantial distortion. For example, if a circuit is to amplify a sinusoid $V_0 \sin \omega_0 t$ (in the steady state), then its slew rate must exceed $V_0\omega_0$.

Example 9.10

(a) Determine the small-signal step response of the circuit.

(b) Calculate the positive and negative slew rates.





(a) (b)

Figure 9.56

$$A_v = g_{m1,2}(r_{O2} \| r_{O4})$$

Solution

要点：输出幅度和时间常数

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_v / \left(1 + A_v \dfrac{C_1}{C_1 + C_2}\right)}{1 + \dfrac{C_1 C_2}{C_1 + C_2} R_{out} s / \left(1 + A_v \dfrac{C_1}{C_1 + C_2}\right)}$$

Example 9.10 (cont.)

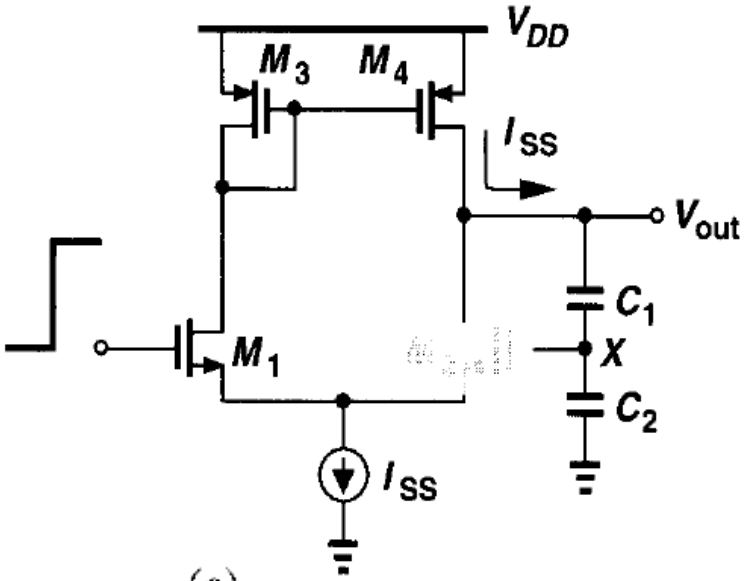
The response to a unity step is thus given by

$$V_{out}(t) = \frac{A_v}{1 + A_v \dfrac{C_1}{C_1 + C_2}} V_0 \left(1 - \exp \frac{-t}{\tau}\right) u(t), \tag{9.33}$$

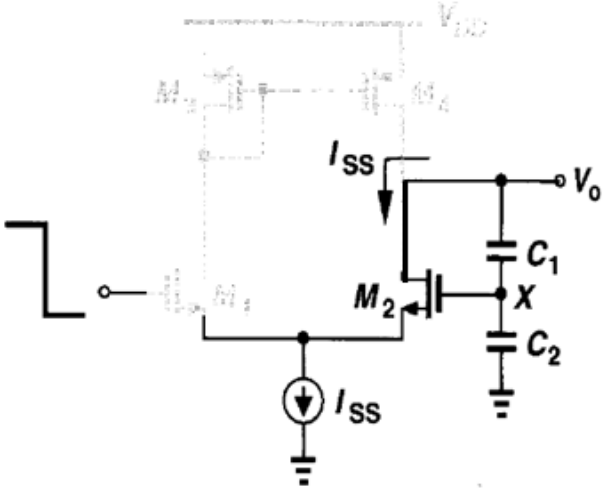
where

$$\tau = \frac{C_1 C_2}{C_1 + C_2} R_{out} / \left(1 + A_v \frac{C_1}{C_1 + C_2}\right).$$

Example 9.10 (cont.)



(c)



(d)

Figure 9.56

(b) Suppose a large positive step is applied to the gate of M_1 in Fig. 9.56(a) while the initial voltage across C_1 is zero. Then, M_2 turns off and, as shown in Fig. 9.56(c), V_{out} rises according to $V_{out}(t) = I_{SS}/[C_1C_2/(C_1+C_2)]t$. Similarly, for a large negative step at the input, Fig. 9.56(d) yields $V_{out} = -I_{SS}/[C_1C_2/(C_1+C_2)]t$.

Slew rate of telescopic(套筒) op

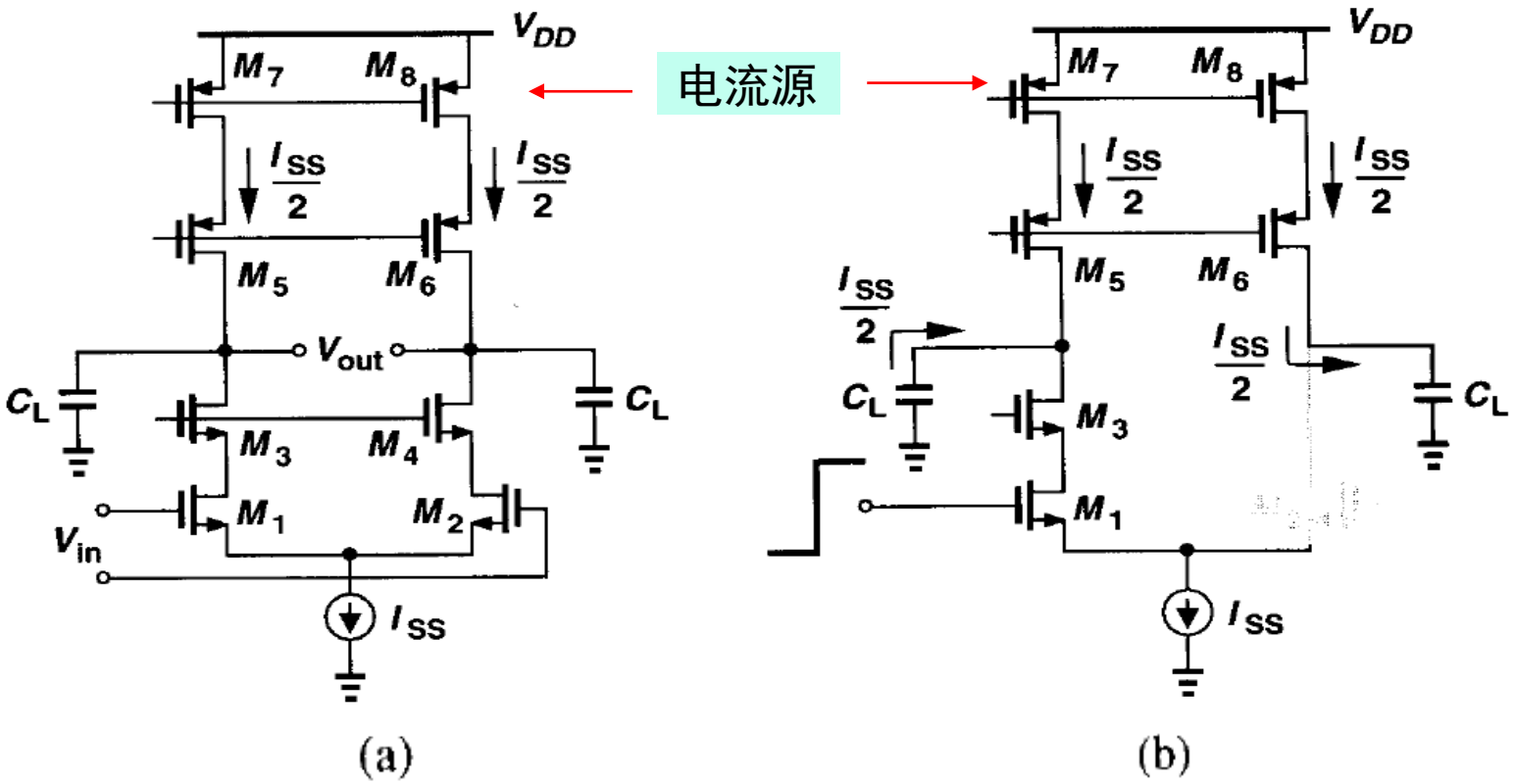
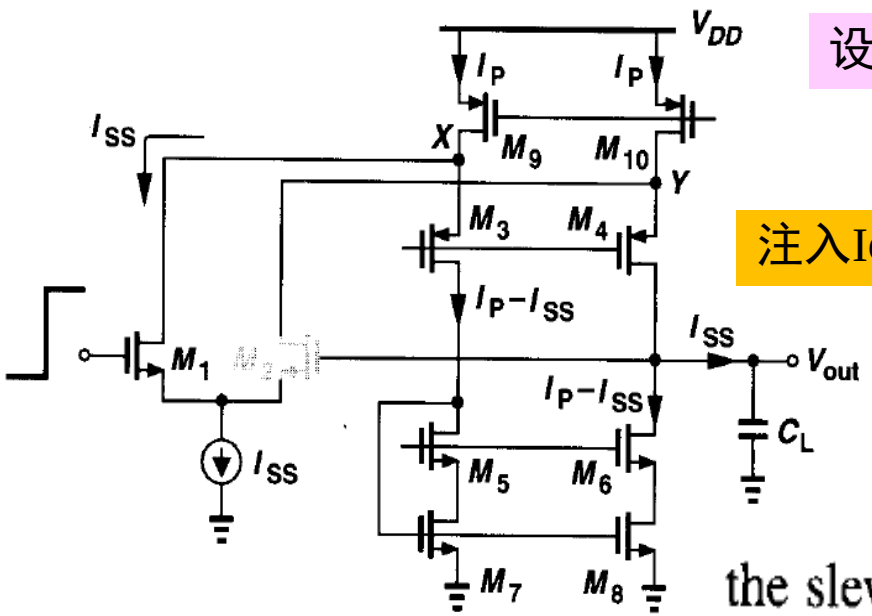


Figure 9.57 Slewing in telescopic op amp.

单边输出转换速率（压摆率）$dV_{out1}/dt=I_{SS}/(2C_L)$

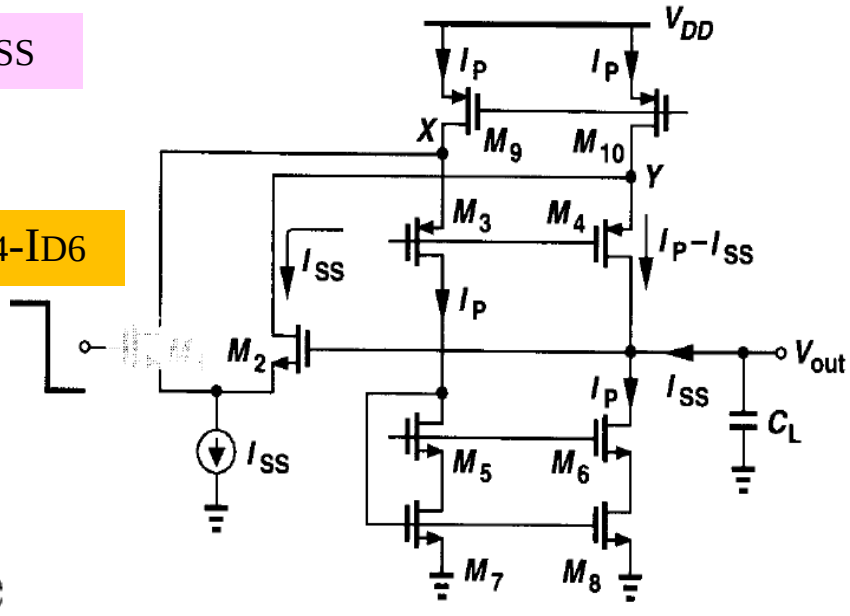
Slew rate of folded-cascode op



(a)

设IP>=ISS

注入ICL=ID4-ID6



(b)

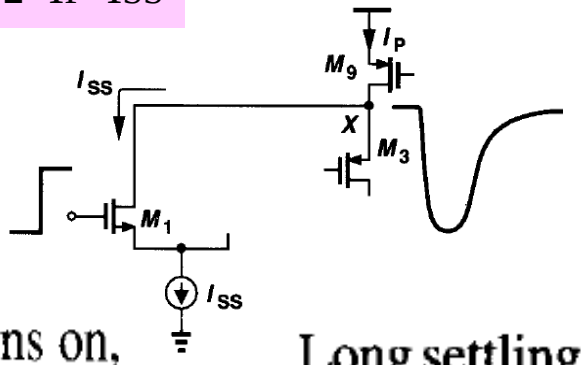
the slew rate I_{SS}/C_L.

若$I_{SS}/2<I_P<I_{SS}$

实际电路选取：IP=ISS。即4支路电流相同

if $I_{SS} > I_P$, then during slewing M_3 turns off and V_X falls to a low level such that M_1 and the tail current source enter the triode region.

Thus, for the circuit to return to equilibrium after M_2 turns on, V_X must experience a large swing, slowing down the settling.



Long settling

9.9 Power Supply Rejection

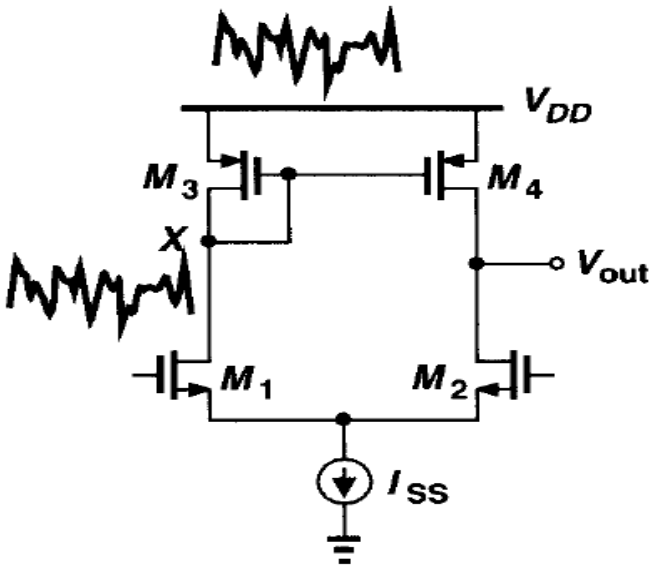


Figure 9.61 Supply rejection of differential pair with active current mirror.

the gain from V_{DD} to V_{out} is close to unity.

Power supply rejection ratio:

PSRR = 信号增益/电源到输出的增益

At low frequencies:

$$PSRR \approx g_{mN}(r_{OP} \| r_{ON}).$$

Example 9.12（负反馈）

Calculate the low-frequency PSRR of the feedback circuit shown in Fig. 9.62(a).

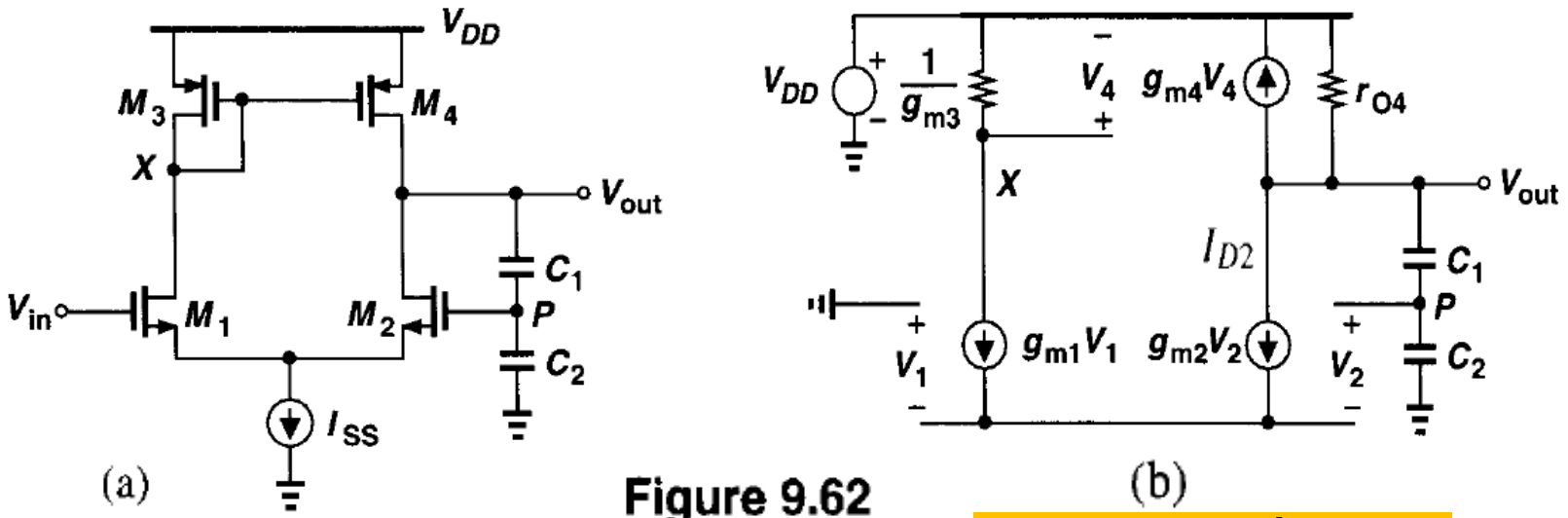


Figure 9.62

Solution

ΔV in V_{DD} appears unattenuated at the output.

CM: V_{DD}噪声

$V_1=V_{GS1}$, $V_2=V_{GS2}$

V_{out}通过r_{O4}引入V_{DD}(噪声)

V2-V1=VP ⟶ $V_{out}\dfrac{C_1}{C_1+C_2}-V_2=-V_1$

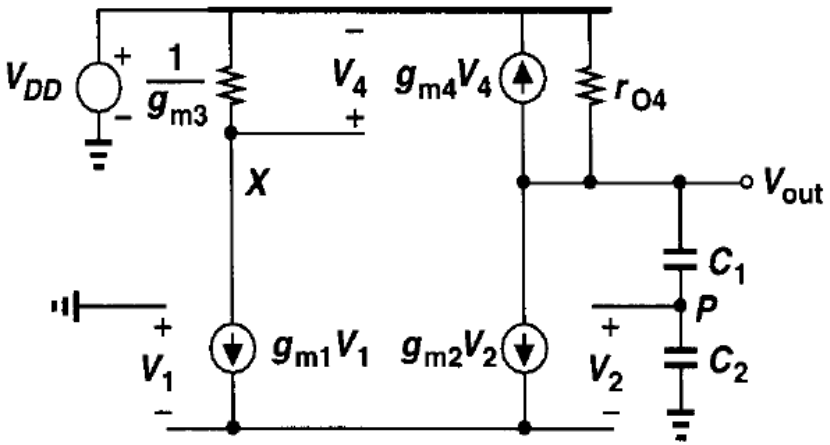
思路：求解V_{out}节点电流方程

Since $g_{m1}V_1+g_{m2}V_2=0$. ⟶ **V1=-V2** ⟶ $V_2=\dfrac{V_{out}}{2}\dfrac{C_1}{C_1+C_2}$.

Example 9.12 (cont.)

low-frequency

$$-\frac{g_{m1}V_1}{g_{m3}}g_{m4}-\frac{V_{DD}-V_{out}}{r_{O4}}+g_{m2}V_2=0.$$



(b)

It follows that

$$\frac{V_{out}}{V_{DD}}=\frac{1}{g_{m2}r_{O4}\dfrac{C_1}{C_1+C_2}+1}.$$

低频，忽略C

$$PSRR=\frac{\text{信号增益}}{\text{电源到输出增益}}=\left(1+\frac{C_2}{C_1}\right)\left(g_{m2}r_{o4}\frac{C_1}{C_1+C_2}+1\right)$$

$=g_{m2}r_{o4}$?