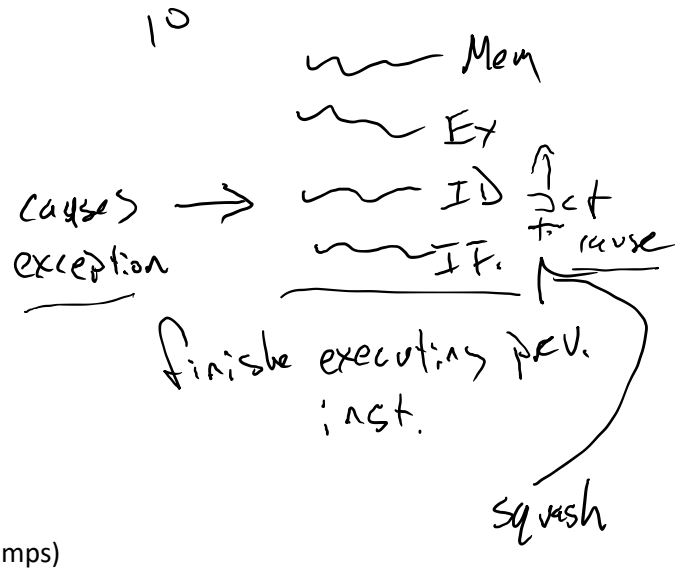
Material covered

Book: Chapters 1, 2, 4 (mostly 1 and 4).



- Technology and performance
  - Moore's law
  - Energy and power of CMOS devices
  - Latency, bandwidth, and their relation
  - Iron law
  - Amdahl's law and speedup
- Machine representation of programs
  - Definition of ISA
  - Instructions
  - Assembly and machine "language"
- Simple processor
  - Steps to process an instruction
  - Instruction behavior (r-type, lw/sw, branches, jumps)
  - Single cycle processor design
  - Performance of single-cycle and multi-cycle processors
- Pipelining
  - Reason for pipelined processors
  - Changes in control → beq/jmp
  - Hazards
  - Simple branch prediction
  - Exceptions
  - Instruction-level parallelism
  - Tradeoffs of deeper pipelines and instruction-level parallelism →

deeper pipeline will have higher CPI incr freq

_____ claims that the number of transistors per chip will double every 18-24 months.

Increasing the frequency of the processor leads to increased performance and increased power.

What are three ways to compare two systems to determine the “better” system?

A _____ predicts the performance of a real-world application but often has shorter runtime and is standardized to allow comparisons across systems.

There is a processor with three stages: fetch&decode, execute, and memory&writeback. The stages require 350ps, 250ps, and 400ps, respectively.

a) What is the cycle time if you implemented this as a *single cycle* processor (not pipelined)?
b) What is the CPI of this processor?
c) How long (in seconds) does it take to execute an application with 4 billion instructions?
d) If you were to design this processor to pipelined, what is the required CPI to perform as well as the single cycle processor?

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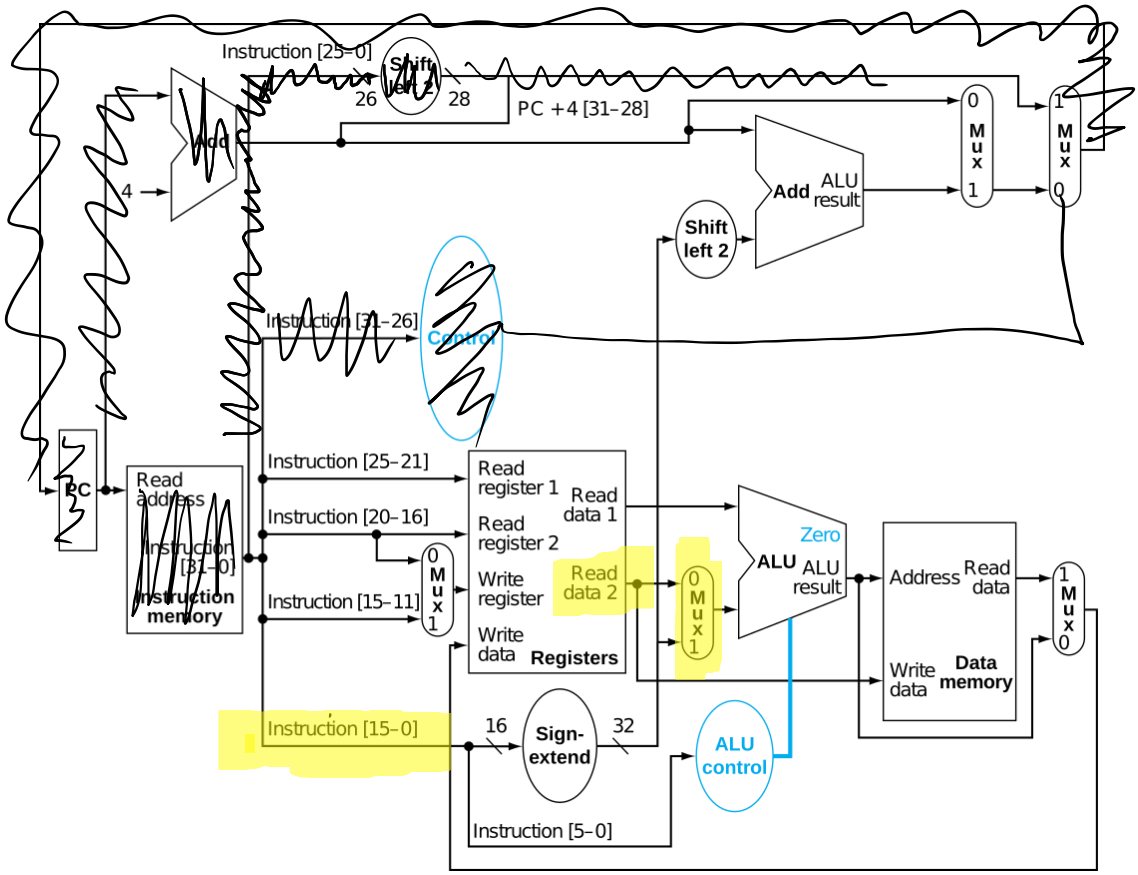
Processor A can run 1 billion instructions in 0.5 seconds at a frequency of 500 MHz. You are proposing a pipelined design for a new processor, design B. Your processor has a CPI of 4. The company you work for will not release a new design unless it has at least a 1.5x speedup compared to processor A. What is your target frequency?

Amdahl's law ($\text{Speedup} = \frac{1}{(1-F_E)+\frac{F_E}{S_E}}$) is a mathematical representation of what common computer architecture design principle?

fraction enhanced

common case fast

The ISA defines the interface between _____ and _____.



In the diagram above, shade the wires and structures used for a jump instruction.

In the diagram above, explain the “Instructions[5-0]” wire going into the ALU control.

What does the “Control” block in the diagram above do?

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What are the five canonical pipeline stages and what happens in each stage?

What instructions cause the PC to be written?

branches jumps

every instruction

What is a pipeline bubble?

_____ is one technique to eliminate many hazards due to read-after-write dependencies.

Generally, as you increase the number of pipeline stages the does the CPI increase or decrease? Why?

What are the three types of hazards? Describe each and describe a technique to reduce their performance impact.

Given the following systems, which will have a higher performance for a constant number of instructions? Why? Show your work.

	System A	System B
Pipeline depth	5	10
~~Cycle time~~	2 GHz	2.5 GHz
Average CPI	3	5

freq

Iron law: time = inst × CPI × cycle time

A: time = 3 · 600ps → 500ns = $\frac{1}{2 \cdot 10^9}$ s

= 1500 ps/inst

B: 5 · $\frac{1}{2.5}$ = 2000 ps/inst

Explain why predicting all branches as ***taken*** is better than predicting all branches as ***not taken***.

What are the two pieces of information that a branch predictor predicts?

On an exception, the processor must save the cause of the exception and the _____.

A processor that executes more than one instruction per cycle is leveraging _____ for increased performance.

Fill in the per-cycle pipeline diagram table for the following code. Show all cycles where forwarding occurs and the stages between which the data is forwarded. Assume there is ***no*** branch prediction and branches are resolved ***in the decode stage.*** The branch is resolved not taken in the decode stage.