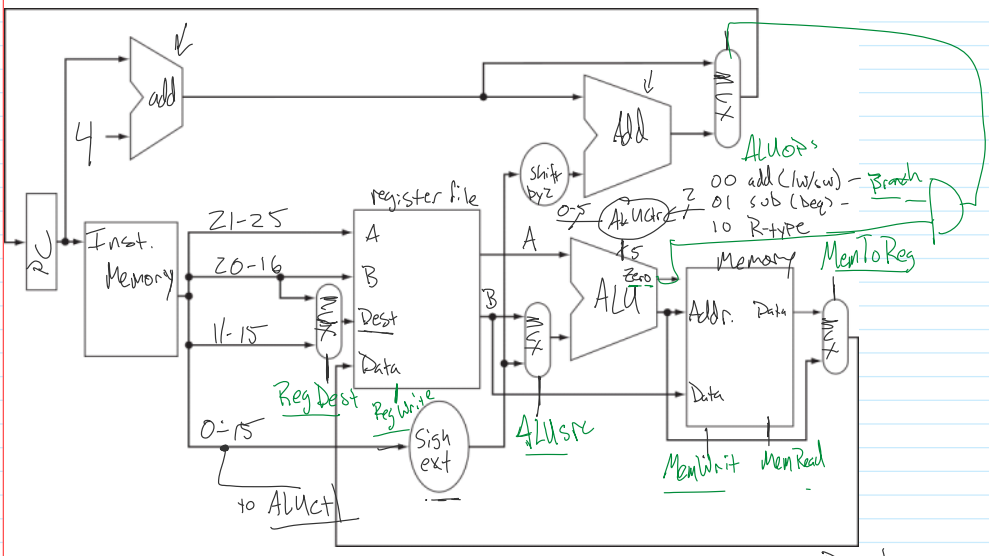
Lecture 6: Single/Multicycle MIPS

Wednesday, January 24, 2018 11:47 AM

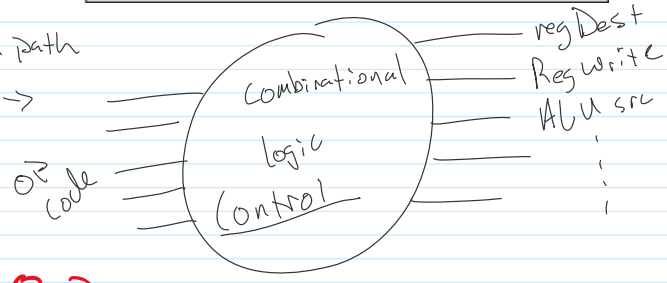
Outline

- Single-cycle control logic
- Multi-cycle design
- Multi-cycle state machine



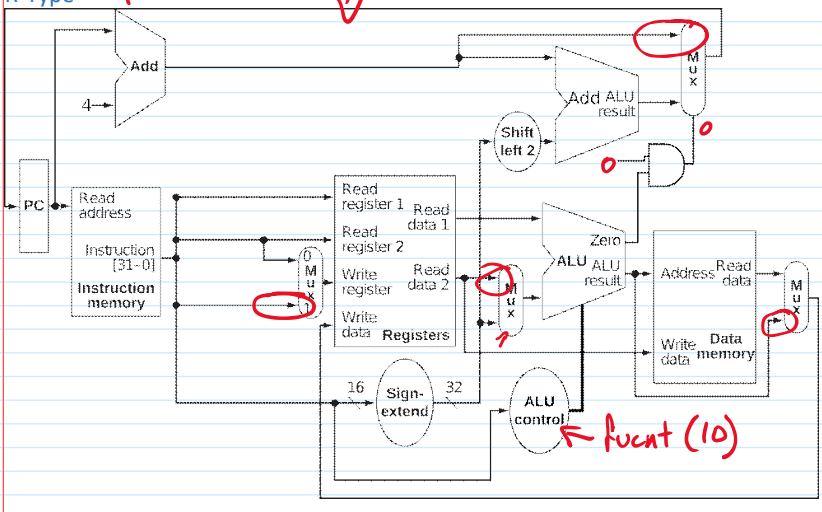
Last time => data path

Control logic =>



R-Type

opcode = 0



regDest

ALUsrc --

MemtoReg

RegWrite yes 1

MemRead 0

MemWrite 0

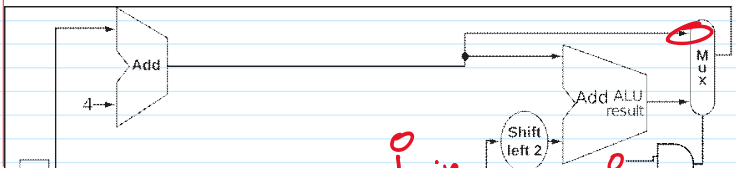
Branch 0

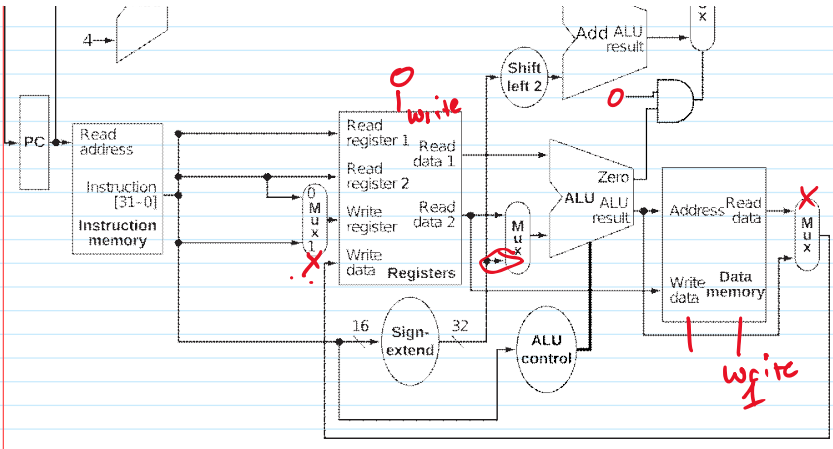
ALUop1

ALUop0

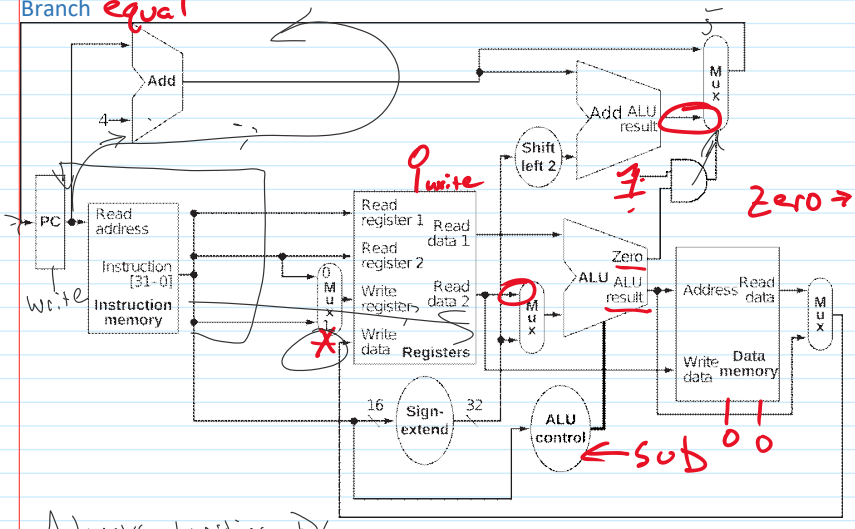
Store

opcode 43





Branch equal



Zero → 1 if A == B

MOV Y, eax, Y, ip

Always writing PC

Performance

Read inst memory	100 ps
Registers	50 ps
Muxes	5 ps each
ALU	75 ps
Mem	200 ps
Reg write	50 ps
Add	25 ps

R-type

100 inst
50 regs + 10 for mux
75 ALU
50 reg write + 5 mux
290 ps

lw

100 inst
50 + 10 regs + mux
75 ALU
200 mem
55 reg write + mux
490 ps

Br

100 inst
reg 50 + 5
ALU 75
5 for mux
235 ps

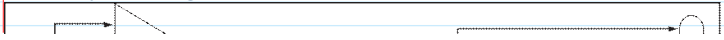
jump

100 + 10 + 5 = 115 ps

loads 490 ps
stores 440 ps
R-type 290 ps
br 235 ps
j 115 ps

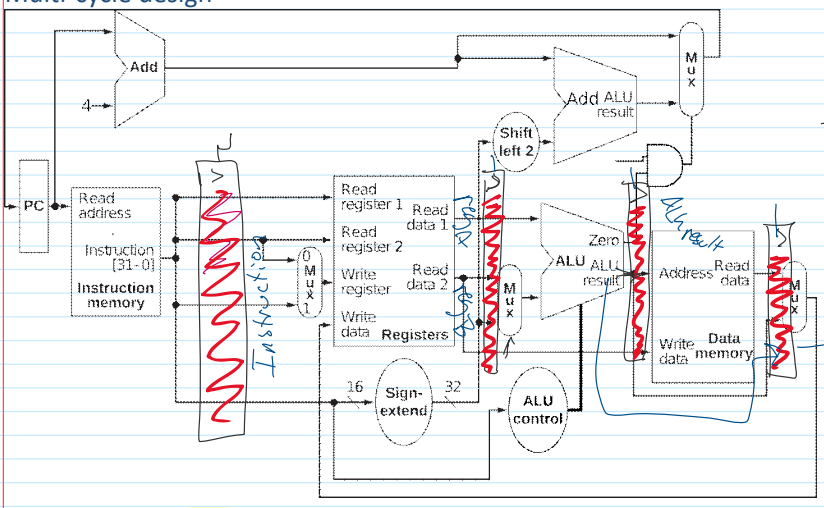
max → 490 ps cycle time
freq 1/490 ~ 2.1 GHz

Multi-cycle design



Stages

Multi-cycle design



Stages

1. Inst fetch
2. Decode/ register read
3. Execute ALU
4. Memory → 2 cycles
5. write back

ld → 6 cycles
St → 5
R → 4
Br → 3
jumps → 2

Multiple stages — each instruction takes 2-5 cycles

1. Fetch 100 ps
2. decode/read 75+5 ps 80ps
3. Execute 5+75 80ps
4. read/write mem 200ps → split 2 cycles @ 100ps each
5. WB 60 ps

What is cycle time
100 ps
freq: 10 GHz

Performance depends on application!

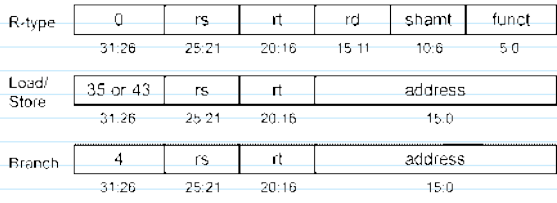
Iron Law

Time = # inst X CPI X cycle time

CPI of single cycle? → 1

CPI of multi cycle?

↳ depends on instruction mix


R-type
0
rs
rt
rd
shamt
funct
31:26
25:21
20:16
15 11
10:6
5 0
Load/
Store
35 or 43
rs
rt
address
31:26
25:21
20:16
15:0
Branch
4
rs
rt
address
31:26
25:21
20:16
15:0