Lecture 15: More caching

Tuesday, February 27, 2018 11:54 AM

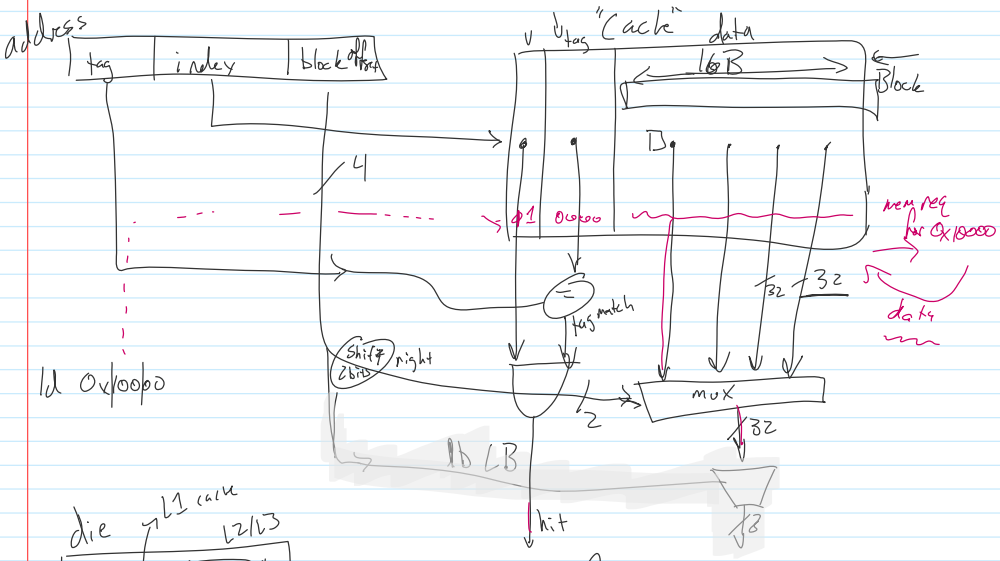
Outline

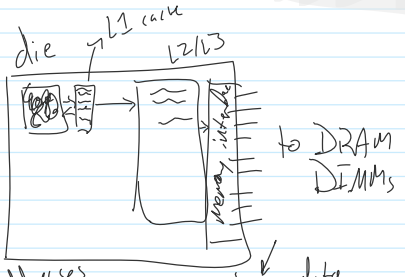
- Cache architecture
- Set associativity
- Cache state machines
- Non-blocking caches
- Multi-level caches & AMAT

ROM -> read-only memory

Flash -> not byte addressable

-> lw $1, 0x10000

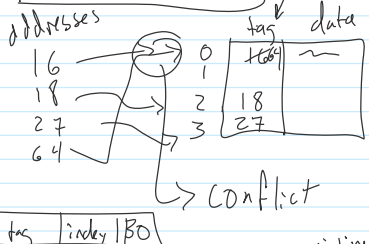




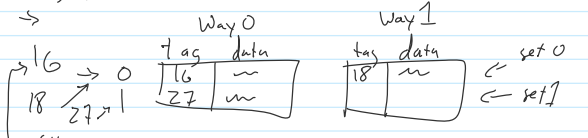
direct-mapped cache

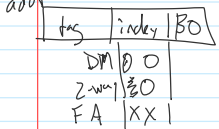
-> they have many conflicts

Conflict -> two memory addresses map to same cache location

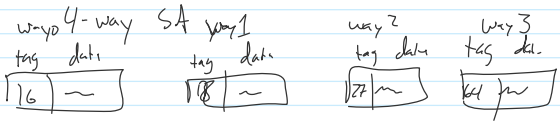


Solution: set-associative caches (2 way SA)





fully associative -> 4-way SA



-> set 0

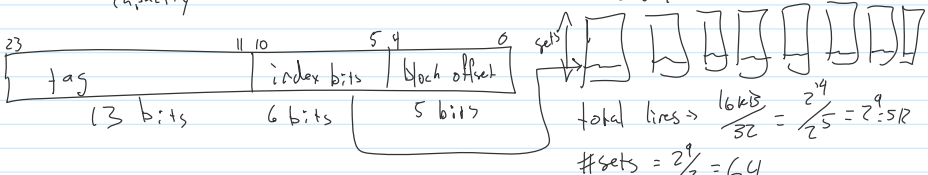
no index bits (one set)

tag field for DM cache vs SA

SA will have 2 more bits (4-way) in tag field than DM

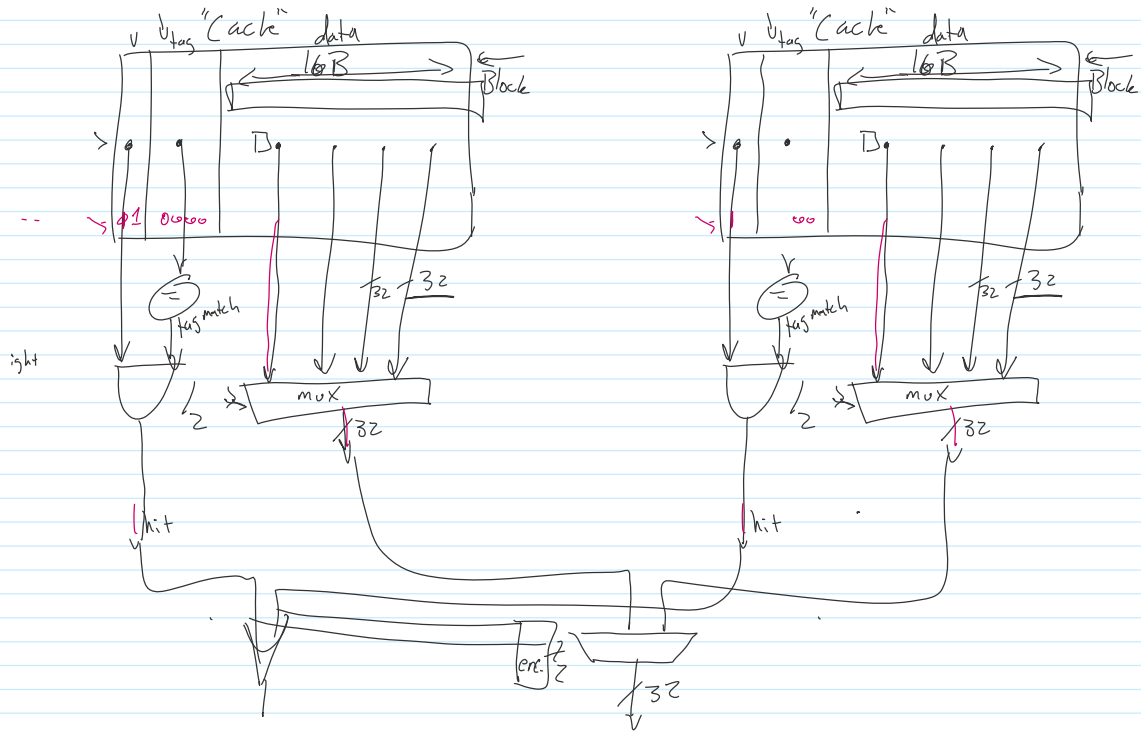
# of index bits -> $\log_2$(# of sets)

8-way SA 16 kB capacity 32 B blocks 24-bit address

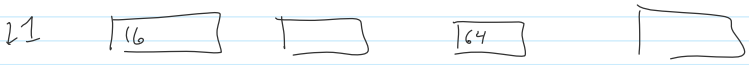


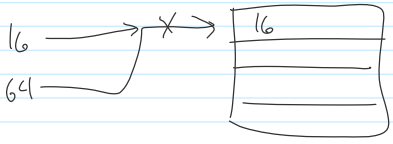
total lines -> $\frac{16\text{kB}}{32} = \frac{2^{14}}{2^5} = 2^9 = 512$

sets = $\frac{2^9}{2^3} = 64$



higher SA
more area
- more =
- more muxes
- more power
↳ selecting more data

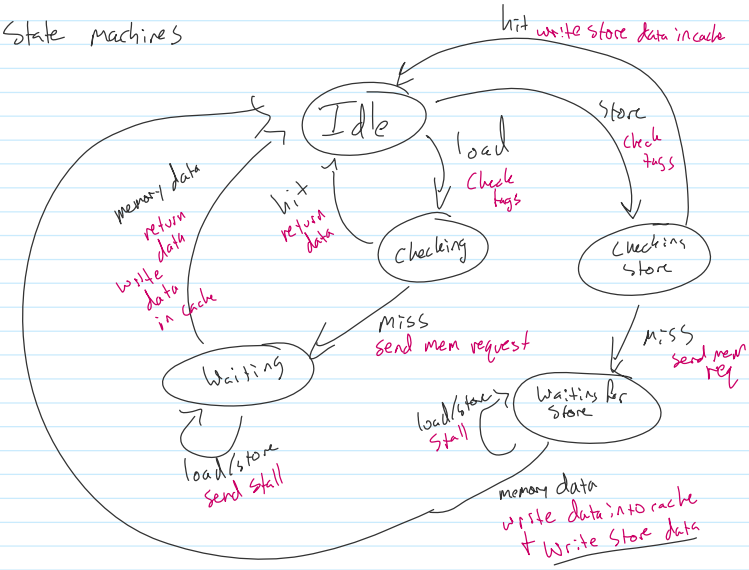




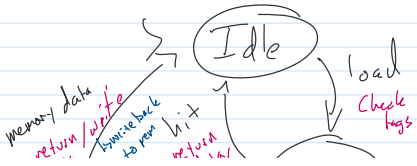
L2 Want higher associativity at lower level caches

Cache State machines

Blocking Cache

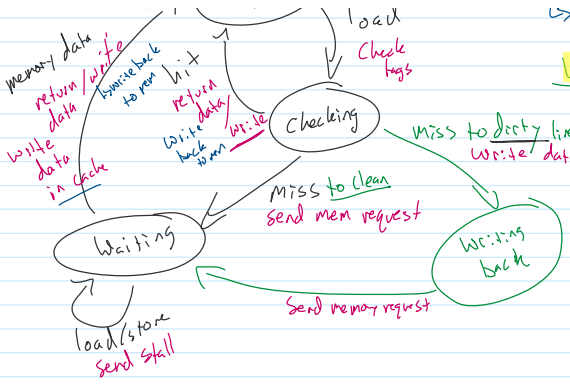


actions →
load from src
store
mem data



When writing to cache
must also update memory
↳ write-through caches

Write back cache → need dirty bit per line



↳ Write-through caches

Write back cache ⇒ need dirty bit per line