Lecture 5: Processor design 1

Monday, January 22, 2018 2:22 PM

Outline

- Steps to "process" an instruction
- Example instructions
- High-level processor design

3

Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3GHz clock rate and a CPI of 1.5. P2 has a 2.5GHz clock rate and a CPI of 1.0. P3 has a 1.5GHz clock rate and a CPI of 0.5.

a. Which processor has the highest performance expressed in instructions per second?

giga → 10^9
mega → 10^6
kilo → 10^3

gigabyte (gibibytes) → base 2 2^{30}
mega 2^{20}
kilo 2^{10}

P1 3 GHz or $3 \cdot 10^9$ clocks(cycles)/second
1.5 CPI
1.5 cycles/inst.
inst/sec → $3 \cdot 10^9$ cycles/second × 1 inst / 1.5 cycle
→ $2 \cdot 10^9$ inst/second

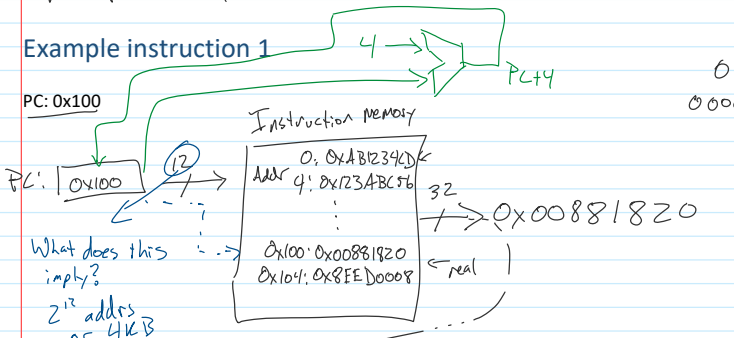
Steps to "process" instructions

identify which instruction to process → PC program counter (instruction pointer) = address in memory of current instruction
fetch the instruction from memory
identify parameters of inst. } decode → read registers
determine what to do

execute the instruction → write/read memory if lw/sw
save the result → write the registers (write back)
go to next instruction
check for interrupts

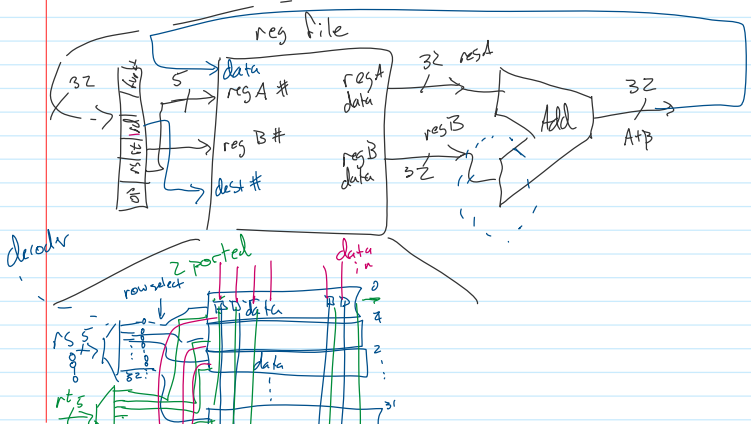
Example instruction 1

PC: 0x100



0 0 8 8 1 8 2 0
0000 0000 1000 1000 0001 1000 0010 0000
0 4 8 3 0 0x20

add $3, $4, $8 → reg[8] + reg[4] → reg[3]
rd rs rt

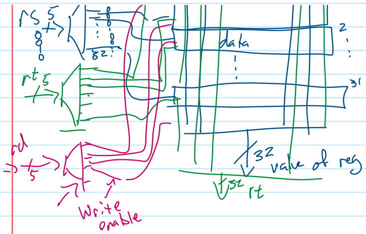


0 4 8 3 0 0x20

R	opcode	rs	rt	rd	shamt	funct
	31 26	25 21	20 16	15 11	10 6	5 0

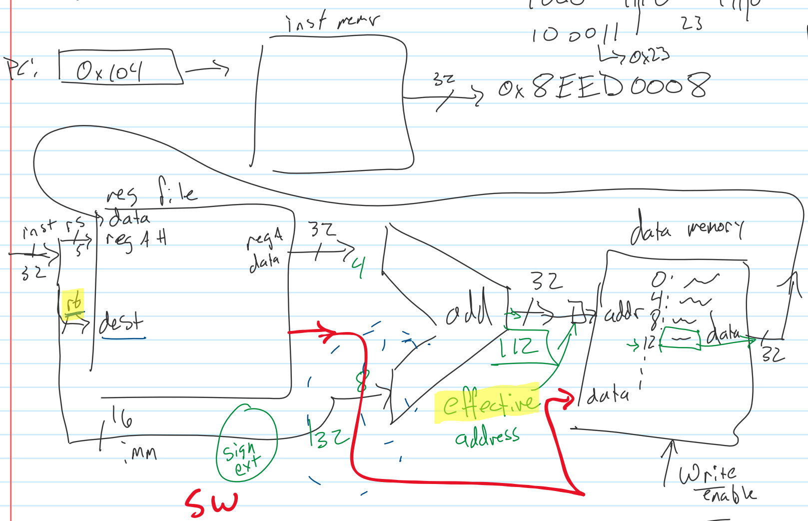
CORE INSTRUCTION SET

NAME, MNEMONIC	FOR-MAT	OPERATION (in Verilog)	OPCODE / FUNCT (Hex)
Add	add	R R[rd] = R[rs] + R[rt]	(1) (0) / 20_{hex}



Example 2

8 E E D 0 0 0 8
1000 1110 1110 1101 0000 0000 0000 1000
100011 | 23 | 13
→ 0x23



reg[13] = Mem[Reg[23] + 8]

lw $13, 8($23)

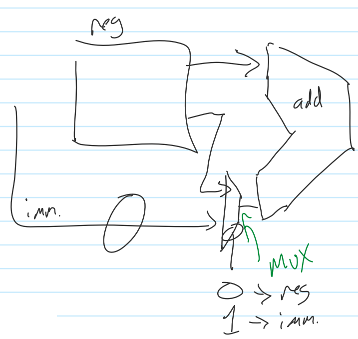
OP/funct

Load Word	lw	I	R[rt] = M[R[rs]+SignExtImm]	(2)	23_{hex}

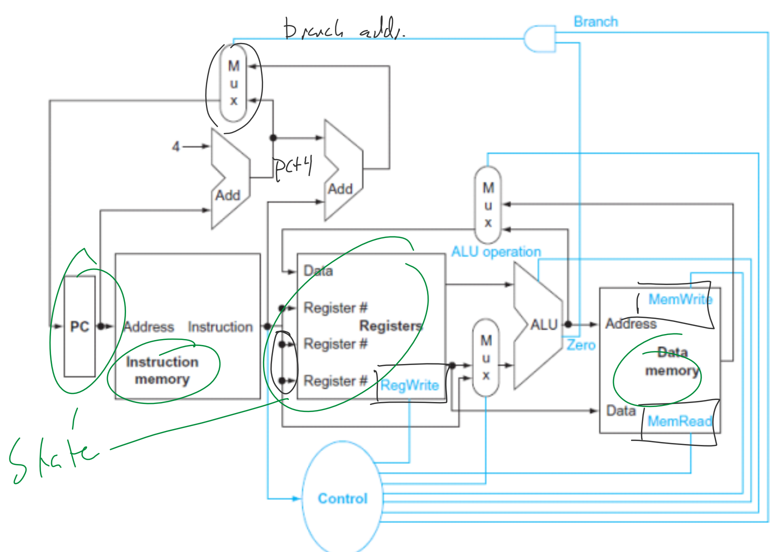
I	opcode	rs	rt	immediate
	31 26	25 21	20 16	15 0
	0x 23	23	13	8

Sometimes have immediate
+ sometimes a register for bottom Adder input
Choose which to use
→ mux (multiplexer) to choose imm or reg

Control signals

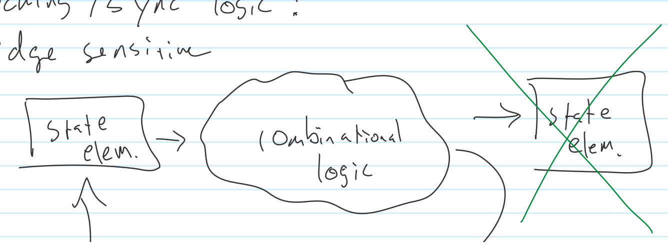


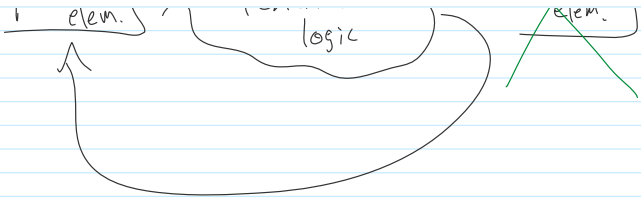
High-level system design



add
lw (sw)
j / bne

Clocking / sync logic?
edge sensitive





Single-cycle processor