Analysis and Optimization of 1Kb SRAM

ShanghaiTech University EE113 TAs

Checking Due: Jan 14, 2022
Report Due: 9 PM, Jan 15, 2022

1 Introduction and Rules

SRAM (static random access memory) is usually the yield bottleneck of the digital system and is hard to achieve high-speed, low-power, and low-cost. This project implements a 1Kb SRAM array in the SMIC180 process. You should fully understand the electronic properties using knowledge and experience from the EE113 class. You should submit the CDL and GDS file and pass TA's check before the checking due. You (2 students recommended) should submit one report of double-column IEEE template no more than 4/6 pages ex/including bonus before the report due. Contact TA. Wang if any questions about document expression.

Rules:

- Fully understand all details of your design.
- Encourage discussion and prohibit plagiarism.
- Treat experimental data with integrity.

2 Phase 1: Basic of SRAM Design (1 week)

2.1 Architecture and I/O

In this phase, you should learn architecture and the mechanism of read/write operations from your textbook [1] chapter 12. Fig .1 shows the architecture of this project with input signals in red and output signals in blue. The interconnected signals of each block do not have to be the same as Fig .1, but the input/output signals of the total SRAM are fixed.

For the row circuits, consisting of decoder and wordline (WL) buffers, the input of the decoder is the 5-b row address for 32 rows. The column circuits consist of pre-charge circuits (PC), write drivers, and sense amplifiers (SAs). For the core array, the bitcell is shown in Fig .1, which is the conventional bitcell of 6T SRAM. For the timing controller, you should generate all the waveforms by the posedge input of CLK with the different operation modes. Mode = 1 for read-mode and 0 for write-mode.

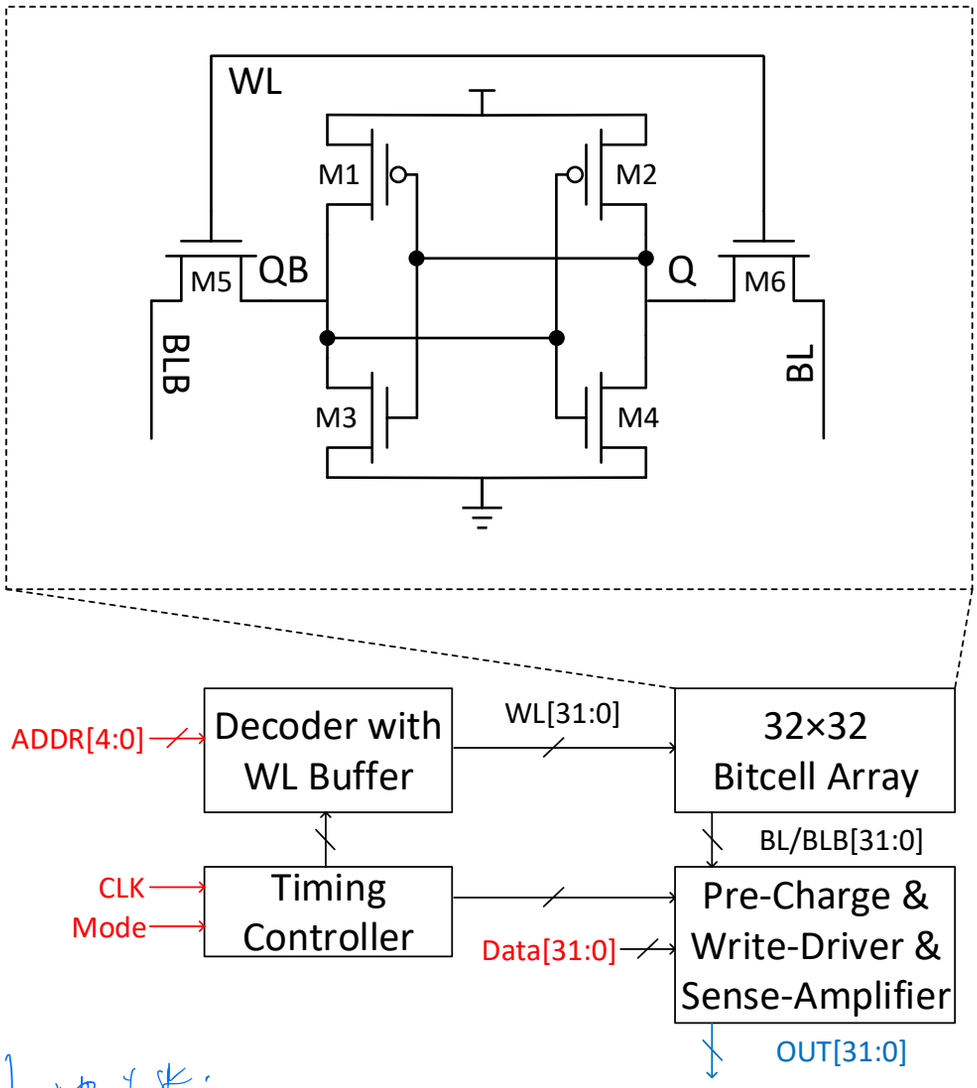

Figure 1: The block diagram of 1Kb SRAM array. The schematic of the bitcell is shown above. Note that all input in red and output in blue.

2.2 A Read After Write Example

Fig .2 shows the timing diagram of a read-after-write example with fixed ADDR[4:0] and DATA[31:0]. This example is used to guarantee the correct function and show the critical path.

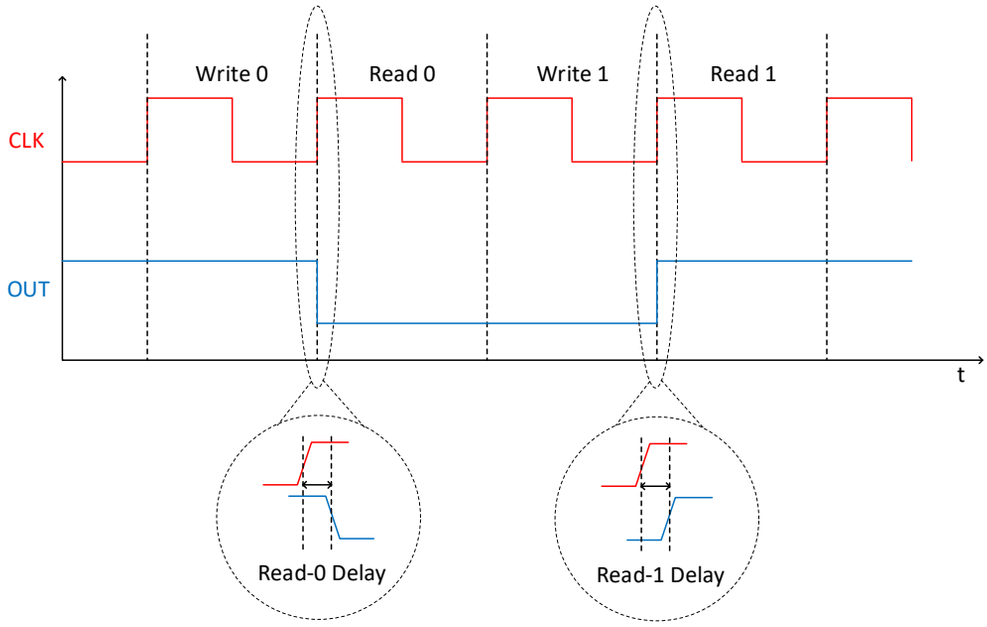

Figure 2: The timing diagram of the read-after-write example.

2.3 Sizing a Bitcell

To improve the yield at high speed, you should formulate the length and width of each transistor (M1 - M6) of a bitcell. Each width is no larger than 800nm.

2.4 Check List

- Fully understand the SRAM architecture and the data flow.
- The width and length of a bitcell with causality.

3 Phase2: Pre-simulation (2 weeks)

3.1 Build schematic of each component

For the row circuitry, you need to make sure the right function of the decoder. To drive each WL, the buffer is necessary. For the column circuitry, during the read-mode, the

voltage of the discharged BL/BLB is no lower than 70% VDD. The referenced SA is shown in Fig .3. For the bitcell array, you should add an estimated ideal capacitance model to each WLs/BLs to imitate the parasitic capacitance in the layout of the bitcell array after phase 3.

(Hint: Simulation of the sub-circuit is helpful; implementing an easy-adjusting timing module is recommended.)

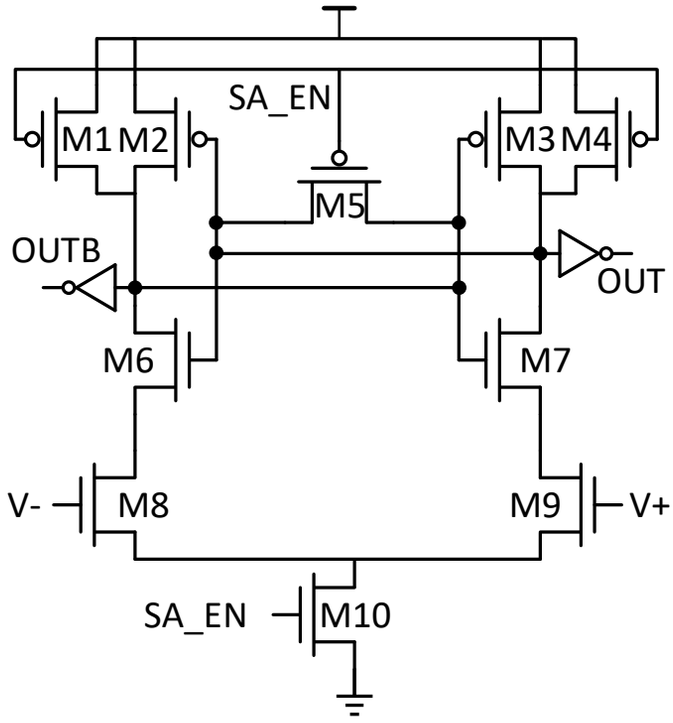

Figure 3: A latch-based sense amplifier.

3.2 Find the critical path

After building the whole circuit, please make the transient simulation and get the result like Fig. 2. Find your critical path of read-0 and read-1 operations and show them in your waveform. The critical path is from CLK to OUT[X], with your specific ADDR[4:0]. Note that you should plot all valid intermediate signals from CLK to OUT[X] in the specific waveform with the estimated ideal capacitance model from the layout.

(Hint: Analyze your architecture and the signal flow in RC model.)

3.3 Check List

- Analysis the critical path and the sensing mechanism.

- Important parts of the schematic of the design.
- Transient simulation waveform of read before write example.
- Two specific waveform of the critical path of read-0 and read-1 operation.

4 Phase3: Post-simulation (2 weeks)

4.1 Layout design

For the bitcell array, the layout should be symmetric in both horizontal and vertical directions. You must set a body tap every eight bitcells in the horizontal or vertical direction. For the row and column circuitry, setting the width of the unit circuit in layout matched with bitcell is recommended.

(Hint: Implementing the layout of reasonable sub-array is recommended; set the body tap to left/right side instead of top/bottom side for the row circuitry to fit the width of the bitcell layout.)

4.2 Parasitic capacitance estimation

After passing the LVS and PEX of the 32×32 bitcell array, you should extract the reasonable capacitance of WLs/BLs and add it to the schematic to finish pre-simulation in phase 2.

4.3 Energy and Delay result

When finishing post-simulation, present the result of the energy of 1bit read and 1bit write operations no more than 500fJ/bit, and the delay of critical path no more than 4ns. You should discuss the difference of energy for different input patterns.

(Hint: Repeat the same target operation, using the stable part (several cycles behind) to find the energy .)

4.4 Check List

- Important parts of the layout and the total design area.
- Pass DRC and LVS check of the top module.
- Transient post-simulation waveform of read-before-write example.
- Comparative waveform of the critical path (pre/post-simulation without estimated capacitance).

- Analyze and present the energy per read/write operation and the critical path delay.
- Finish the table of the comparison result.
- Compress and submit the CDL/GDS files of the schematic/layout of the top module.

	Pre-simulation	Pre-simulation with Estimated Capacitance	Post-simulation
Critical Path Delay (ns)			
Read Energy (fJ/bit)			
Write Energy (fJ/bit)			
Bitcell Array Area (μm^2)	NA	NA	
Total Area (μm^2)	NA	NA	

5 Bonus (3 weeks)

5.1 Bonus 1: Function Expansion

In this part, you are supposed to add extra functions to the circuit to use the SRAM in a small digital system with memory, computational logic, and register. The circuit will now be able to handle the following instructions. All instructions are processed in a single clock cycle. Please see the appendix for complete design requirements.

5.2 Bonus 2: Research Bonus

Please optimize your project design for high-speed, low-power, or low-cost based on at least three referenced papers with at least one from IEEE Journal of Solid-State Circuits (JSSC). First, you should motivate your improvement and list some application scenarios. Second, you should present your optimization method/methods and show its/their validity respectively. Third, you should extend the table of the comparison result. Note that please analyze the trade-offs of your design.

(Hint: Search SRAM + "keywords" in ieeexplore.ieee.org)

References

[1] N. H. E. Weste and D. Harris, "Cmos vlsi design: a circuits and systems perspective 4th edition," *Pearson Education*, India, 2015.