# Appendix – Bonus 1

This is a detailed discription for project bonus 1. Contact TA. Chen if you have any questions about this part.

## 1 Bonus 1 Requirement

The top view of your circuit is shown in Fig.1. Input signal is highlighted in red and output in blue. The instructions, which contains operations and address, are sent into your circuits one in a clock period. Register reset signal is named RST. When RST is 1, all registers would be cleared at clock edge.

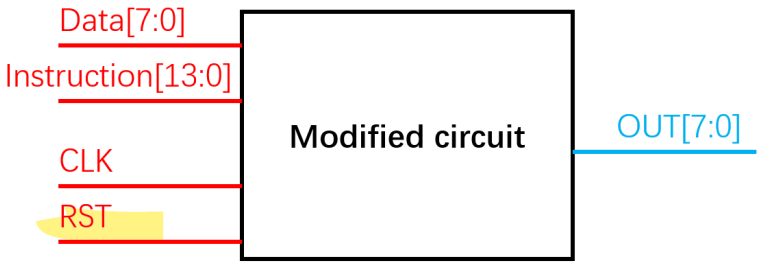


Figure 1: The topview of bonus 1 circuit

An unfinished example block diagram is shown as Figure 2. Your circuit should at least contain a modified 32x32 SRAM array, a 8x8 register and a 8-bit adder. Some control logics are needed to decode operation code and send proper command to registers and SRAM array.

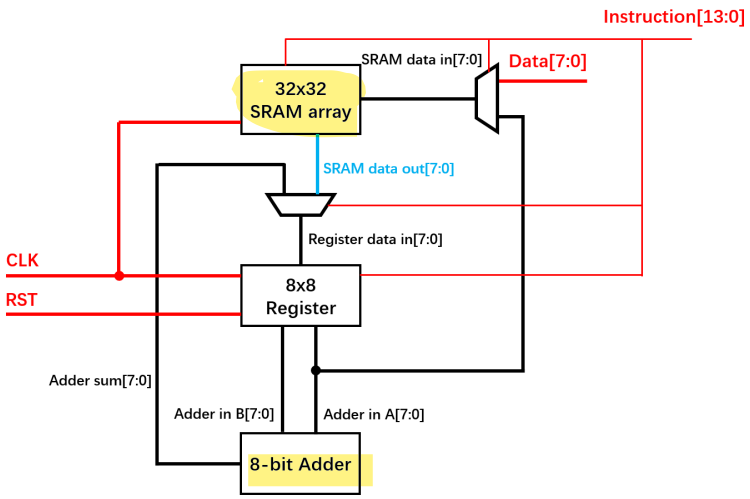


Figure 2: Example block diagram

In the basic part, SRAM array can only be accessed by row address. In this part, each row is divided into 4 bytes and can be accessed individually. Row and column address are now used to designate byte of interest. The data input and output of SRAM array is now 1 byte (8-bit).

| Byte3[31:24] | Byte2[23:16] | Byte1[15:8] | Byte0[7:0] |
|---|---|---|---|

The instructions to be handled are shown below. The first 3 bits are operation code, which defines the function. The used codes are marked with X, which can be either 0 or 1, while the unused code is 0.

- DATA to SRAM

  Write input data (8-bit) into SRAM array with given row and column address

| operation code | unused | SRAM column address[1:0] | SRAM row address[4:0] | unused |
|---|---|---|---|---|
| 000 | 0 | XX | XXXXX | 000 |

- REG to SRAM

  Write data in a register (8-bit) with given register address, into SRAM array with given row and column address

| operation code | unused | SRAM column address[1:0] | SRAM row address[4:0] | REG address[2:0] |
|---|---|---|---|---|
| 001 | 0 | XX | XXXXX | XXX |

- SRAM to REG

  Read data (8-bit) in SRAM array with given row and column address, and write it to a register according to given register address

| operation code | unused | SRAM column address[1:0] | SRAM row address[4:0] | REG address[2:0] |
|---|---|---|---|---|
| 010 | 0 | XX | XXXXX | XXX |

- SHIFT

  Shift the signals in a register with given register address. When the shift direction signal is 0, right shift the register and set 0 for MSB. When the shift direction signal is 1, left shift the register and set 0 for LSB.

| operation code | shift direction | unused | REG address[2:0] |
|---|---|---|---|
| 011 | X | 0000000 | XXX |

- ADD

  Add data in register A and B, save the sum to register C

| operation code | unused | REG C address[2:0] | REG B address[2:0] | REG A address[2:0] |
|---|---|---|---|---|
| 100 | 00 | XXX | XXX | XXX |

# 2 Hand In

## 2.1 Things to be checked

- You should implement both schematic and layout of the whole circuit, generate and submit CDL and GDS file.
- A testbench testing the functionality of the circuit is required. You should set up the testbench schematic by yourself. The instructions should be sent into the circuit as described in the document. TA will use your testbench to check your bonus 1 circuit.

## 2.2 Things should be included in report

- Your DETAILED block diagram of bonus 1 circuit. You should clarify how the instruction is decoded and sent to the storage/computational logic.
- Tables with the critical path delay of each instruction. Analyse each part of your circuit to find out which path limits your speed.

  Here is an example table of delay analysis of one instruction.

| | Path part1:Input to decoder output | Path part2: | Path part3: | total |
|---|---|---|---|---|
| Pre-simulation delay(ns) | | | | |
| Post-simulation delay(ns) | | | | |

- A table with the power consumption of each instruction. Analyse each part of your circuit to find out which component consumes the most of power.

  Here is an example table of delay analysis of one instruction.

| | SRAM array | Register | Adder | Your additional part | total |
|---|---|---|---|---|---|
| Pre-simulation energy(fJ) | | | | | |
| Post-simulation energy(fJ) | | | | | |