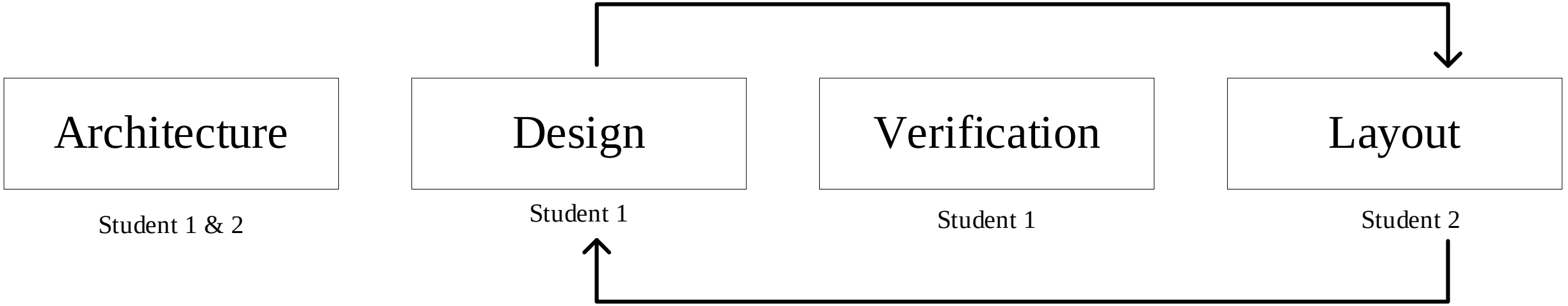
Project Guide 1

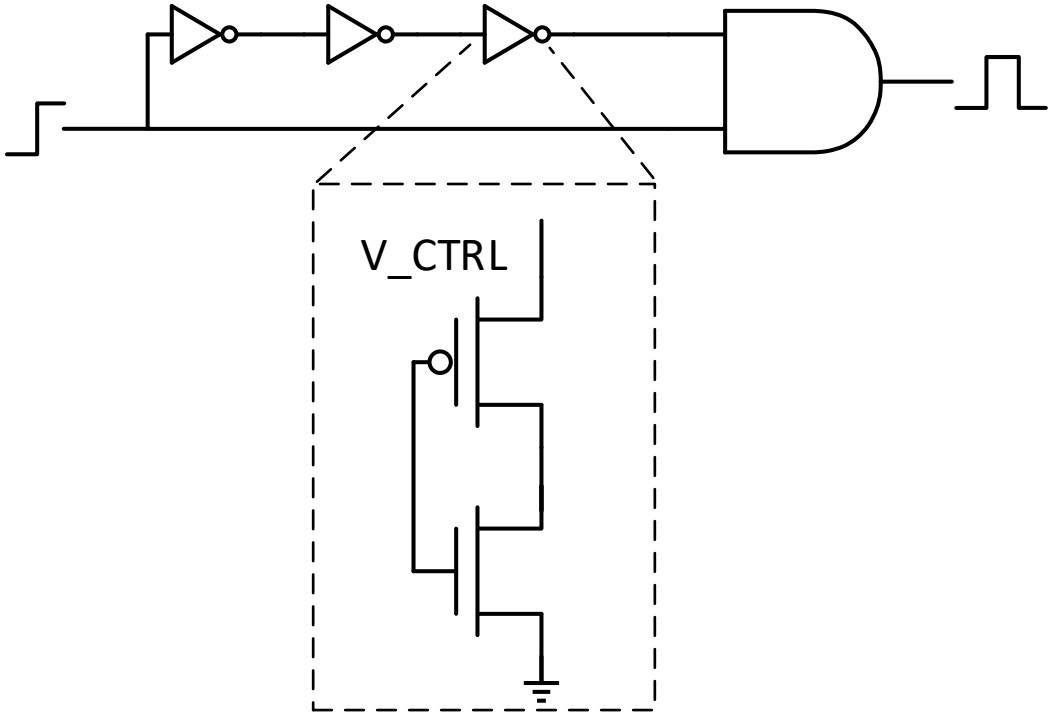
School of Information Science and Technology
ShanghaiTech University

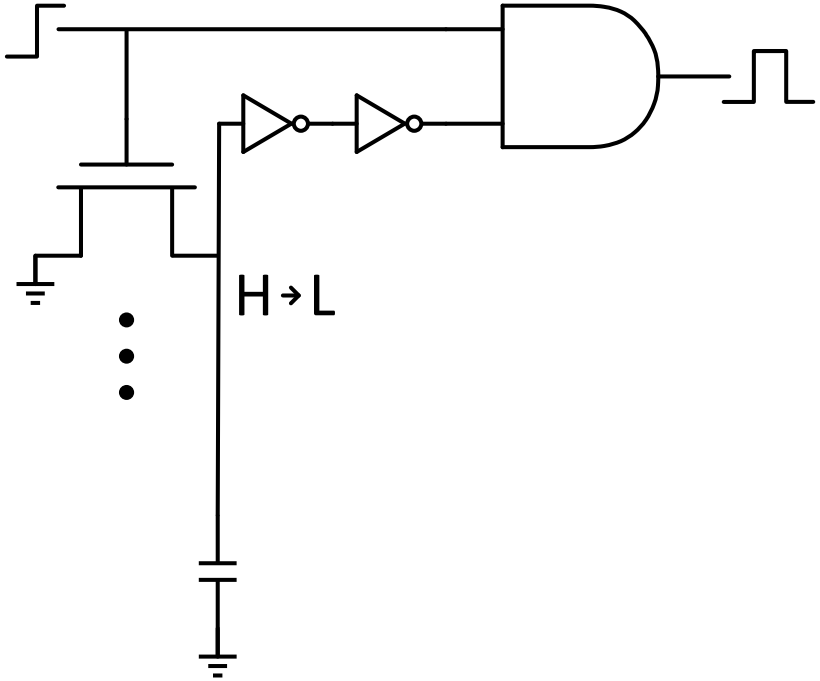
Recommended Division of Labor



Timing Design

- Pulse generation based on: delay line (left) & feedback (right).
- Signal with timing information is implemented by “waveform signal AND enable signal”.





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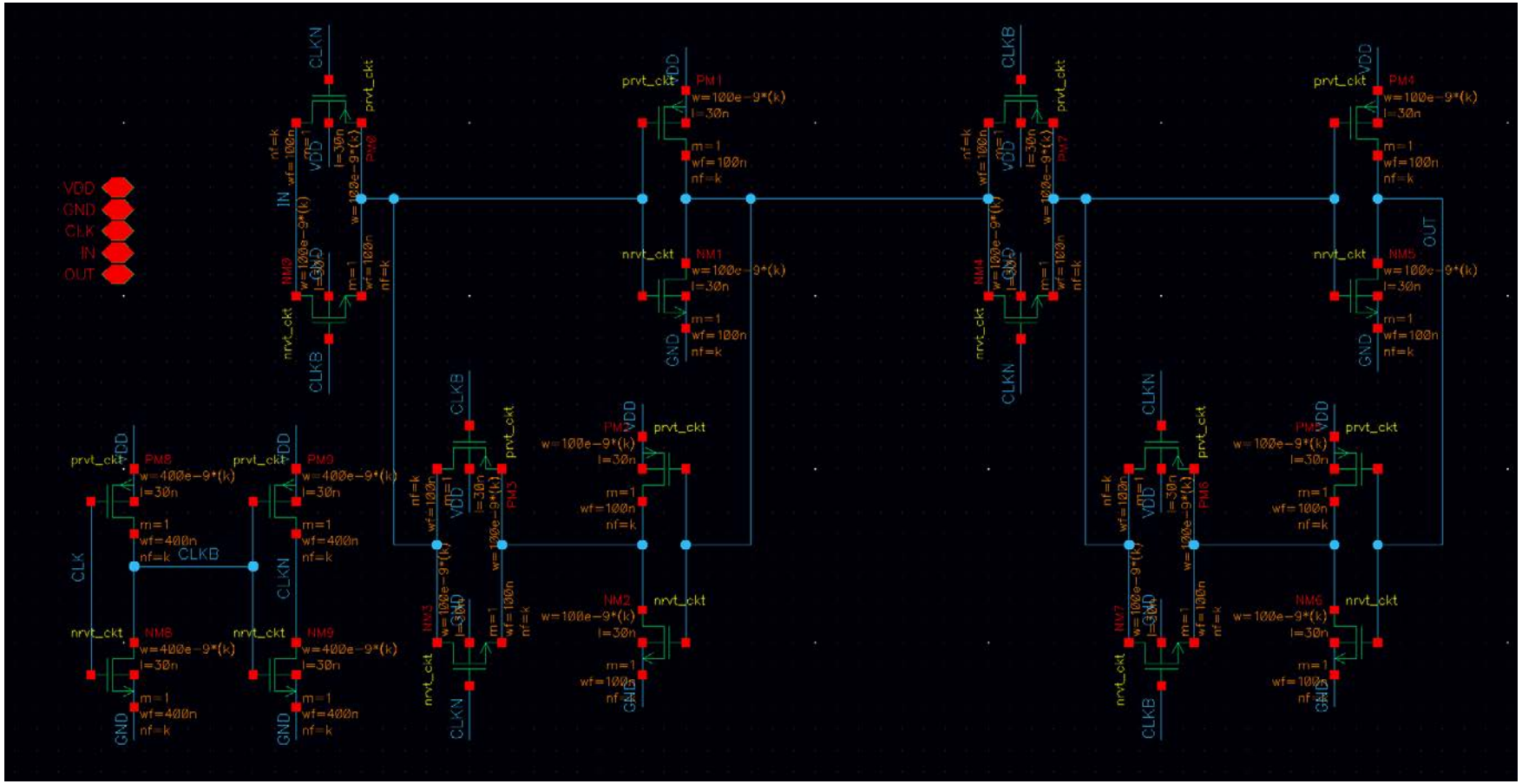
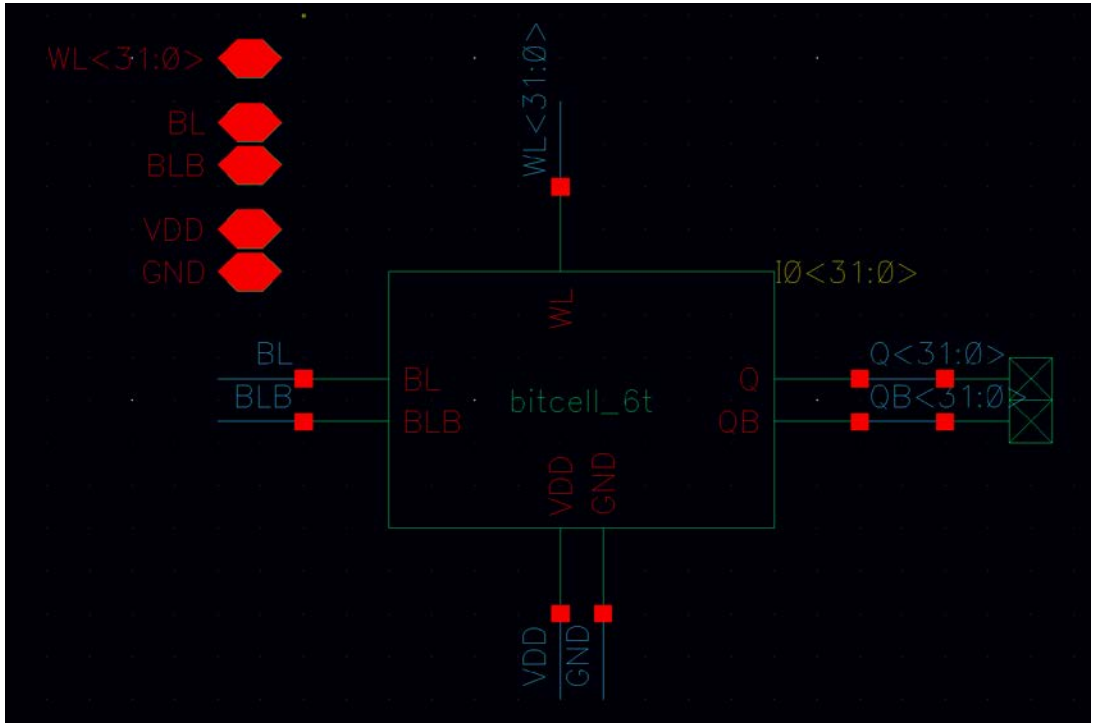
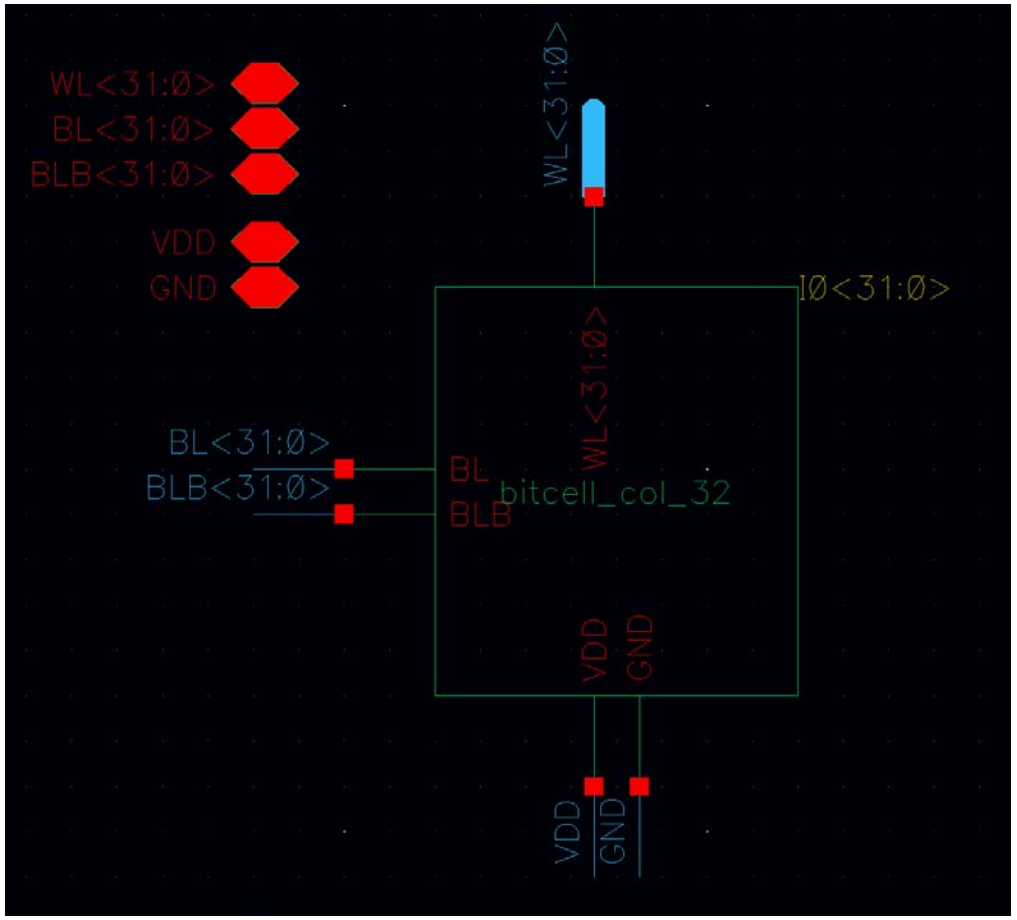

VDD
GND
CLK
IN
OUT
CLKN
CLKB
prvt_ckt
nrvt_ckt
PM0
PM1
PM2
PM3
PM4
PM5
PM6
PM7
PM8
PM9
NM0
NM1
NM2
NM3
NM4
NM5
NM6
NM7
NM8
NM9
w=100e-9*(k)
w=400e-9*(k)
l=30n
m=1
wf=100n
wf=400n
nf=k

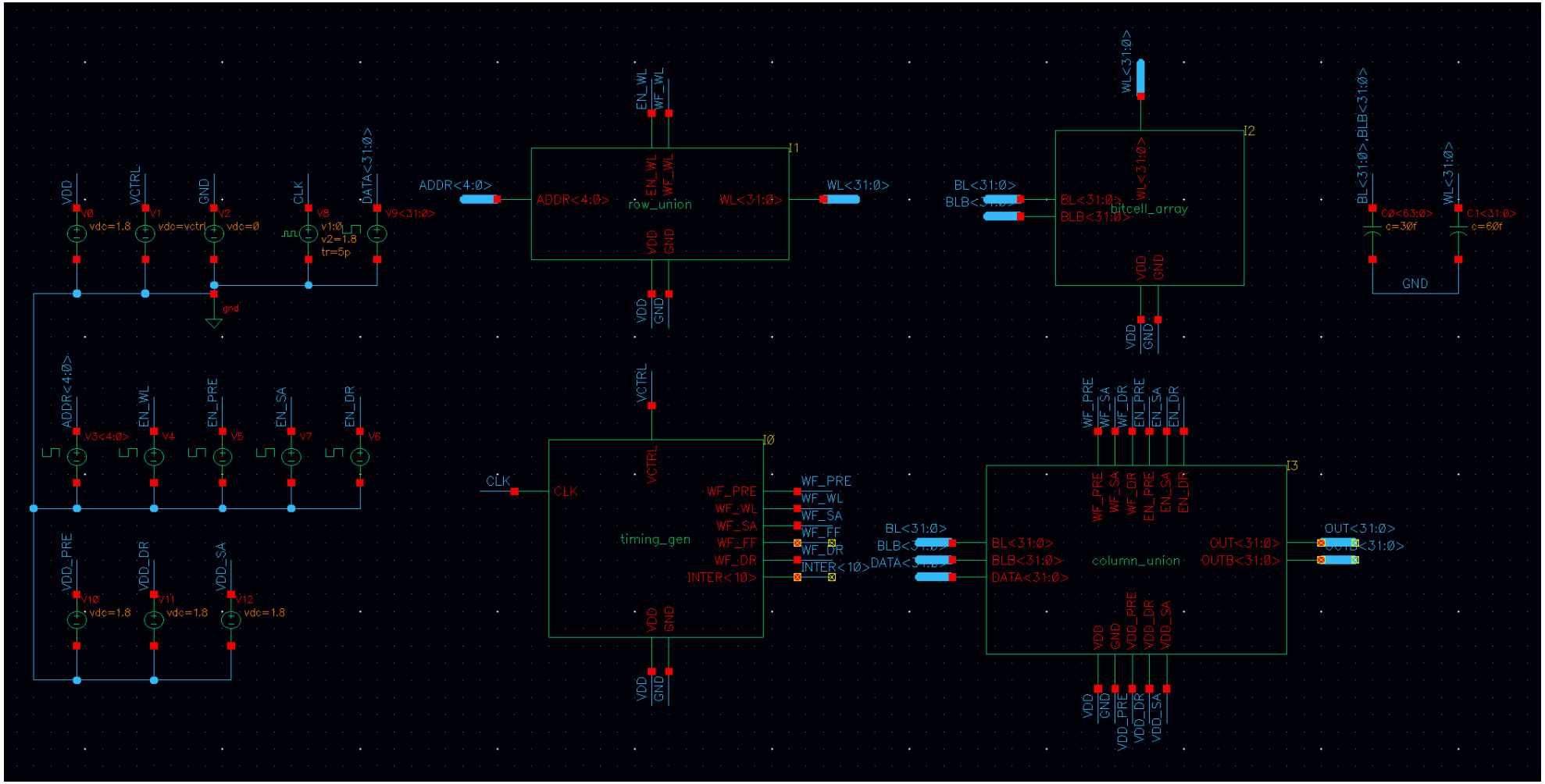
Bitcell Array with Bus

- Bitcell column (left); bitcell array (right).
- Use “shift+e” to select and plot the signal in the module.

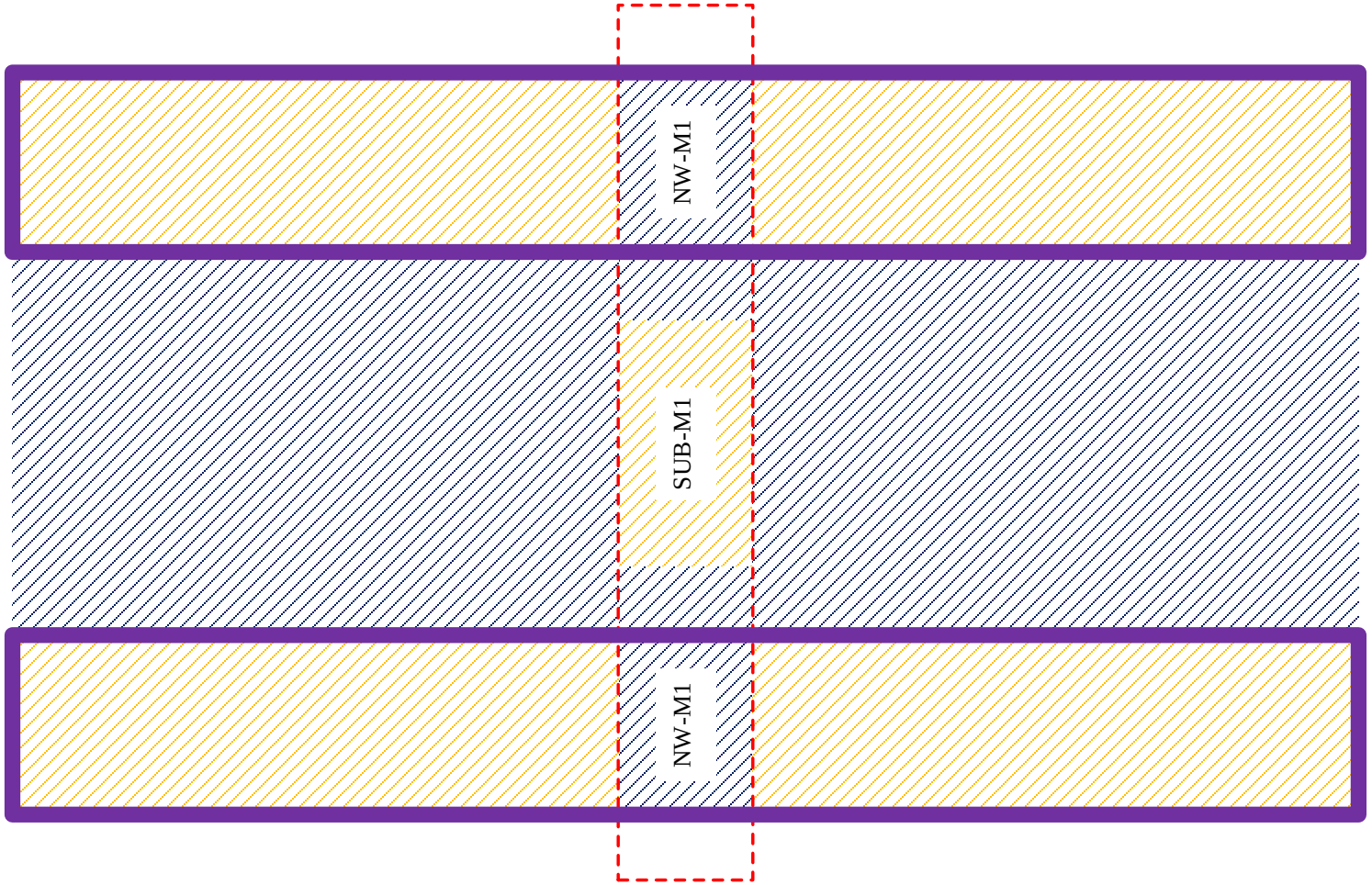


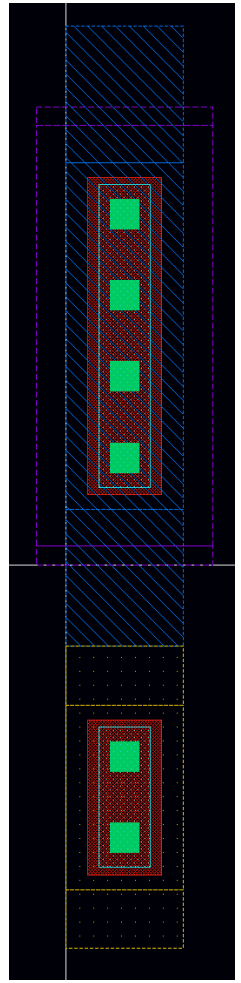


A Pre-Simulation Example



Layout with Body Tap





Layout with Multiple Views

- Cellview with multiple layout views (left) and with no schematic view (right).