

SLR 206 – Fondements des Algorithmes Répartis

Randomized Consensus and Other Agreement Protocols

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January 25th 2023



- Consensus is impossible to solve deterministically in a wait-free manner using read-write registers if at least one process may crash.

So far...

- Consensus is impossible to solve deterministically in a wait-free manner using read-write registers if at least one process may crash.
- Consensus is impossible to solve deterministically in an asynchronous message passing system if at least one process may crash.



Next

- Consensus is impossible to solve deterministically in a wait-free manner using **read-write registers** if at least one process may crash.
- Consensus is impossible to solve deterministically in an asynchronous **message passing system** if at least one process may crash.

These constructions have *Consensus number 1*

| Consensus Number | Object |
|------------------|--|
| 1 | read/write registers |
| 2 | test&set, swap, fetch&add, queue, stack |
| \vdots | \vdots |
| $2n - 2$ | n -register assignment |
| \vdots | \vdots |
| ∞ | memory-to-memory move and swap, augmented queue, compare&swap, fetch&cons, sticky byte |

Figure: Maurice Herlihy – Wait-free synchronization.



- Consensus is impossible to solve deterministically in an **asynchronous** message passing system if at least one process may crash.

Consensus can be deterministically solved in *partial-synchronous* and *synchronous* networks.

- **Asynchronous** – No bound on message delays.
- **Partial-synchronous** – There exists a delay, but it is unknown.
- **Synchronous** – There exists a known delay.



- **Consensus** is impossible to solve deterministically in a wait-free manner using read-write registers if at least one process may crash.
- **Consensus** is impossible to solve deterministically in an asynchronous message passing system if at least one process may crash.

In this lecture: There are other agreement protocols.

- Approximate Agreement
- Commit-adopt

- Consensus is impossible to solve deterministically in a **wait-free** manner using read-write registers if at least one process may crash.

In this lecture: Consensus can be deterministically solved in an *obstruction-free* run.

- **Lock-free** – If processes try infinitely many times to take steps, they eventually finish.
- **Obstruction-free** – If a process takes steps in isolation, then it finishes in finitely many steps.
- **Wait-free** – Every process finishes in finitely many steps.



- Consensus is impossible to solve **deterministically** in a wait-free manner using read-write registers if at least one process may crash.
- Consensus is impossible to solve **deterministically** in an asynchronous message passing system if at least one process may crash.

In this lecture: Consensus can be solved by randomized protocols with probabilistic guarantees.

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- 3 Commit Adopt
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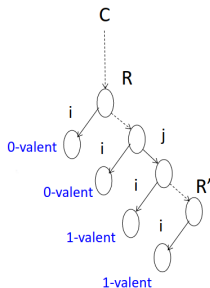
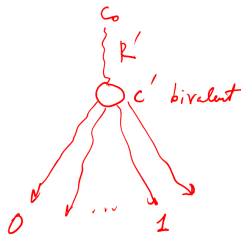
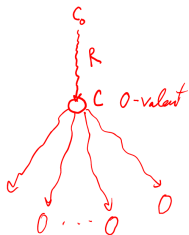


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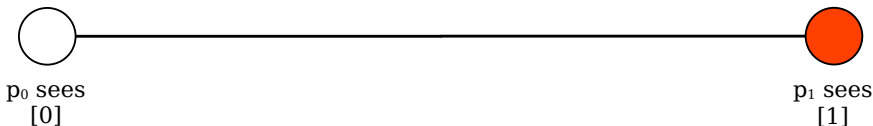
Review – FLP



The iterated memory model

Algorithm 1 Two processes iterated memory – Code for process i

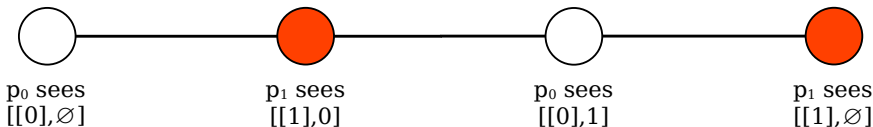
```
1: Infinite array of  $n$  atomic registers  $R_k[1 \dots]$ 
2:  $k \leftarrow 0$ 
3:  $v_i \leftarrow \text{input}$ 
4: while decision not reached do
5:    $k \leftarrow k + 1$ 
6:    $R_k[i].\text{write}(v_i)$ 
7:    $v_i \leftarrow [v_i, R_k[i - 1].\text{read}()]$ 
```



The iterated memory model

Algorithm 2 Two processes iterated memory – Code for process i

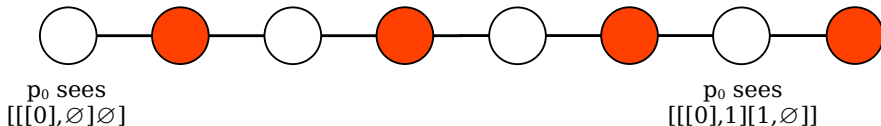
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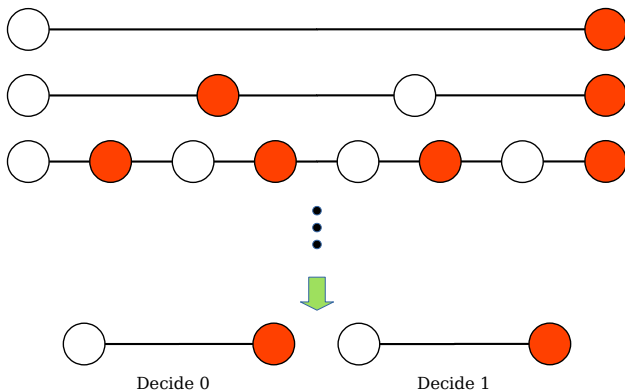
The iterated memory model

Algorithm 3 Two processes iterated memory – Code for process i

- 1: Infinite array of n atomic registers $R_k[1 \dots]$
 - 2: $k \leftarrow 0$
 - 3: $v_i \leftarrow \text{input}$
 - 4: **while** decision not reached **do**
 - 5: $k \leftarrow k + 1$ // $k = 2$
 - 6: $R_k[i].\text{write}(v_i)$
 - 7: $v_i \leftarrow [v_i, R_k[i - 1].\text{read}()]$
-



The topological argument for FLP



The topological argument for FLP

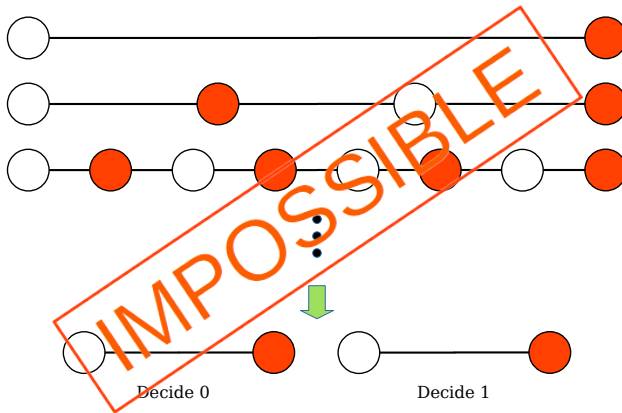


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Approximate Agreement

An approximate agreement protocol provides the following properties:

- **Validity** – Every output value is in the range of input values.



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| input: $v = [1 \ 1 \ 1 \ 1 \ 1 \ 1]$, $\epsilon = 0.01$ output: $[1 \ 1 \ 0.99 \ 1 \ 1]$ | input: $v = [1 \ 1 \ 1 \ 1 \ 1 \ 1]$, $\epsilon = 10000$ output: $[1 \ 1 \ 1 \ 1 \ 1]$ |



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| input: $v = [0 \ 2 \ 3 \ 9 \ 7 \ 3]$, $\epsilon = 0.5$ output: $[9.3 \ 9 \ 8.9 \ 8.95 \ 1]$ | |



Approximate Agreement

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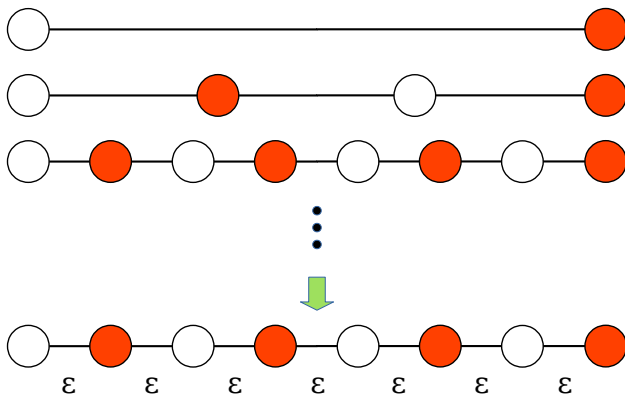
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The topology of AA



Algorithm 4 Two process wait-free ϵ -AA

- 1: Given two atomic registers $R[0], R[1]$
 - 2: $v_i \leftarrow \text{input}$
 - 3: **while** true **do**
 - 4: // $R[i]$ is originally \perp
 - 5: $R[i].\text{write}(v_i)$
 - 6: $v_j \leftarrow R[1 - i].\text{read}(v_i)$
 - 7: **if** $v_j = \perp \vee |v_j - v_i| \leq \epsilon$ **then** Decide v_i
 - 8: **else** $v_i \leftarrow \frac{v_i + v_j}{2}$
-

Algorithm 5 Two process wait-free ϵ -AA

- 1: Given two atomic registers $R[0], R[1]$
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Algorithm 6 Two process wait-free ϵ -AA

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Algorithm 8 Two process wait-free ϵ -AA

- 1: Given two atomic registers $R[0], R[1]$
 - 2: $v_i \leftarrow \text{input}$
 - 3: **while** true **do**
 - 4: // $R[i]$ is originally \perp
 - 5: $R[i].\text{write}(v_i)$
 - 6: $v_j \leftarrow R[1 - i].\text{read}(v_i)$
 - 7: **if** $v_j = \perp \vee |v_j - v_i| \leq \epsilon$ **then** Decide v_i
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- **Validity** – The decided values are either v_i or some iteration of $\frac{v_i + v_j}{2}$.

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- **Agreement** – If a process decides by reading \perp , because processes write before they read, process $1 - i$ will for certain begin looping. If both processes loop, they will converge to the same value.



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- **Liveness** – The algorithm is wait-free, a process does not need the other to take steps in order to make progress and always terminates.

The algorithm terminates in at most



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- **Liveness** – The algorithm is wait-free, a process does not need the other to take steps in order to make progress and always terminates.

The algorithm terminates in at most $O(\log(\frac{|v_1 - v_0|}{\epsilon}))$ steps.

AA with n processes

Simply extending the case for $n = 2$ by using snapshot objects results in a $O((n + \log n) \log(\frac{|v_1 - v_0|}{\epsilon}))$ complexity algorithm. In "Are wait-free algorithms fast?" by Attiya, Lynch and Shavit, the authors provide a wait-free solution with complexity $O(\log n)$.

In message passing:

- 1 Broadcast v
- 2 Wait for $n-f$ values
- 3 Compute mean of received values
- 4 Repeat

The problem is more interesting when there are Byzantine failures.



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Commit Adopt Definition

In commit adopt, processes propose an input value from V and output a couple $(c, v) \in \{false, true\} \times V$. If a process outputs either $(false, v)$ or $(true, v)$, we say that it adopts v . If a process outputs $(true, v)$, then we say that it commits to v .

- **Validity** – Every adopted value is an input value.
- **Termination** – Every correct process eventually adopts a value.
- **CA-Agreement**
 - If a process commits a value v , then every correct process adopts v .
 - If every process inputs the same value, then every correct process commits to a value.



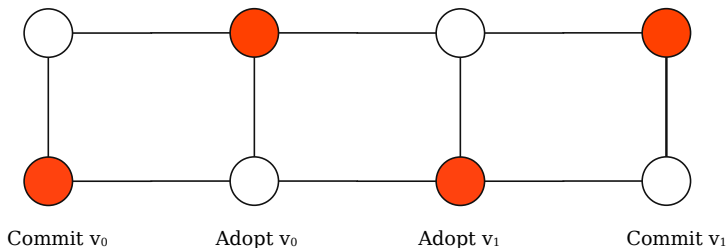
Graded Commit Adopt Definition

In **graded** commit adopt, processes propose an input value from V and output a couple $(c, v) \in \{0, 1, 2\} \times V$. If a process outputs either $(1, v)$ or $(2, v)$, we say that it adopts v . If a process outputs $(2, v)$, then we say that it commits to v , finally, if a process outputs $(0, v)$ we say that it sticks with its input.

- **Validity** – Every **output** value is an input value.
- **Termination** – Every correct process eventually **outputs** a value.
- **CA-Agreement**
 - If a process commits a value v , then every correct process adopts v .
 - If every process inputs the same value, then every correct process commits to a value.



Commit Adopt Topology



Graded Commit Adopt Algorithm

Algorithm 9 Graded Commit Adopt (GCA)

```
1:  $A[1..n]$   $n$  atomic registers  
2:  $B[1..n]$   $n$  atomic registers  
3:  $v_i \leftarrow v$  //  $v$  is the original input  
4:  $A[i].\text{write}(v_i)$   
5:  $U \leftarrow \text{read } A[1..n]$   
6: if All non- $\perp$  values in  $U$  are  $v_i$  then  $B[i].\text{write}((\text{true}, v_i))$   
7: else  $B[i].\text{write}((\text{false}, v_i))$   
8:  $U \leftarrow \text{read } B[1..n]$   
9: if All non- $\perp$  values in  $U$  are  $(\text{true}, v_i)$  then Decide  $(2, v_i)$   
10: else if  $\exists (\text{true}, v') \in U$  then Decide  $(1, v')$   
11: else Decide  $(0, v_i)$ 
```



Graded Commit Adopt Algorithm

Algorithm 10 Graded Commit Adopt (GCA)

```
1:  $A[1..n]$   $n$  atomic registers
2:  $B[1..n]$   $n$  atomic registers
3:  $v_i \leftarrow v$  //  $v$  is the original input
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10: else if  $\exists (\text{true}, v') \in U$  then Decide  $(1, v')$ 
11: else Decide  $(0, v_i)$ 
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Graded Commit Adopt Algorithm

Algorithm 11 Graded Commit Adopt (GCA)

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1:  $A[1..n]$   $n$  atomic registers
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10: else if  $\exists (\text{true}, v') \in U$  then Decide  $(1, v')$ 
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Graded Commit Adopt Algorithm

Algorithm 12 Graded Commit Adopt (GCA)

```
1:  $A[1..n]$   $n$  atomic registers  
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3:  $v_i \leftarrow v$  //  $v$  is the original input  
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Graded Commit Adopt Algorithm

Algorithm 13 Graded Commit Adopt (GCA)

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1:  $A[1..n]$   $n$  atomic registers
2:  $B[1..n]$   $n$  atomic registers
3:  $v_i \leftarrow v$  //  $v$  is the original input
4:  $A[i].\text{write}(v_i)$ 
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Graded Commit Adopt Algorithm

Algorithm 14 Graded Commit Adopt (GCA)

```
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3:  $v_i \leftarrow v$  //  $v$  is the original input  
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Graded Commit Adopt Algorithm

Algorithm 15 Graded Commit Adopt (GCA)

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10: else if  $\exists (\text{true}, v') \in U$  then Decide  $(1, v')$ 
11: else Decide  $(0, v_i)$ 
```



Graded Commit Adopt Algorithm

Algorithm 16 Graded Commit Adopt (GCA)

```
1:  $A[1..n]$   $n$  atomic registers
2:  $B[1..n]$   $n$  atomic registers
3:  $v_i \leftarrow v$  //  $v$  is the original input
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Graded Commit Adopt Algorithm

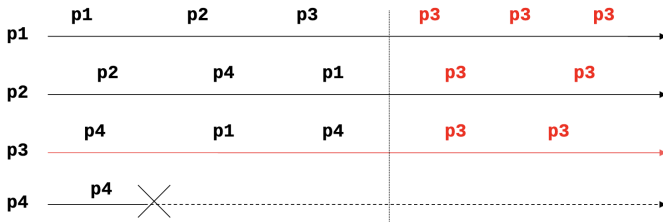
Algorithm 17 Graded Commit Adopt (GCA)

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1:  $A[1..n]$   $n$  atomic registers
2:  $B[1..n]$   $n$  atomic registers
3:  $v_i \leftarrow v$  //  $v$  is the original input
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11: else Decide $(0, v_i)$ 
```



Ω failure detector

- Eventual Leader Detector.
- Outputs at every process a process identifier.
- Eventually, the same correct process is output at every correct process.



It can be implemented in partial-synchronous systems.

Algorithm 18 $GCA + \Omega = \text{Consensus}$

```
1:  $D$  a regular register
2:  $R[1..n]$   $n$  regular registers
3:  $GCA_1, GCA_2, \dots$  a series of graded commit adopt instances
4:  $\Omega$  failure detector
5:  $v_i \leftarrow v$  //  $v$  is the original input
6:  $k \leftarrow 0$ 
7:  $R[i] \leftarrow v$ 
8: while decision not reached do
9:    $k \leftarrow k + 1$ 
10:  if  $v' \leftarrow D.read() \neq \perp$  then Decide  $v'$ 
11:     $(c, v_i) \leftarrow GCA_k.propose(v_i)$ 
12:    if  $c = 0 \wedge R[\Omega].read() \neq \perp$  then  $v_i \leftarrow R[\Omega].read()$ 
13:      //  $c = 1$  the process adopts the value from GCA
14:    else if  $c = 2$  then  $D.write(v_i)$ 
```

Algorithm 19 $GCA + \Omega = \text{Consensus}$

```
1:  $D$  a regular register
2:  $R[1..n]$   $n$  regular registers
3:  $GCA_1, GCA_2, \dots$  a series of graded commit adopt instances
4:  $\Omega$  failure detector
5:  $v_i \leftarrow v$  //  $v$  is the original input
6:  $k \leftarrow 0$ 
7:  $R[i] \leftarrow v$ 
8: while decision not reached do
9:    $k \leftarrow k + 1$ 
10:  if  $v' \leftarrow D.\text{read}() \neq \perp$  then Decide  $v'$ 
11:     $(c, v_i) \leftarrow GCA_k.\text{propose}(v_i)$ 
12:    if  $c = 0 \wedge R[\Omega].\text{read}() \neq \perp$  then  $v_i \leftarrow R[\Omega].\text{read}()$ 
13:      //  $c = 1$  the process adopts the value from GCA
14:    else if  $c = 2$  then  $D.\text{write}(v_i)$ 
```

Algorithm 20 $GCA + \Omega = \text{Consensus}$

```
1:  $D$  a regular register
2:  $R[1..n]$   $n$  regular registers
3:  $GCA_1, GCA_2, \dots$  a series of graded commit adopt instances
4:  $\Omega$  failure detector
5:  $v_i \leftarrow v$  //  $v$  is the original input
6:  $k \leftarrow 0$ 
7:  $R[i] \leftarrow v$ 
8: while decision not reached do
9:    $k \leftarrow k + 1$ 
10:  if  $v' \leftarrow D.read() \neq \perp$  then Decide  $v'$ 
11:   $(c, v_i) \leftarrow GCA_k.propose(v_i)$ 
12:  if  $c = 0 \wedge R[\Omega].read() \neq \perp$  then  $v_i \leftarrow R[\Omega].read()$ 
13:    //  $c = 1$  the process adopts the value from GCA
14:  else if  $c = 2$  then  $D.write(v_i)$ 
```

Algorithm 21 $GCA + \Omega = \text{Consensus}$

```
1:  $D$  a regular register
2:  $R[1..n]$   $n$  regular registers
3:  $GCA_1, GCA_2, \dots$  a series of graded commit adopt instances
4:  $\Omega$  failure detector
5:  $v_i \leftarrow v$  //  $v$  is the original input
6:  $k \leftarrow 0$ 
7:  $R[i] \leftarrow v$ 
8: while decision not reached do
9:    $k \leftarrow k + 1$ 
10:  if  $v' \leftarrow D.read() \neq \perp$  then Decide  $v'$ 
11:     $(c, v_i) \leftarrow GCA_k.propose(v_i)$ 
12:    if  $c = 0 \wedge R[\Omega].read() \neq \perp$  then  $v_i \leftarrow R[\Omega].read()$ 
13:      //  $c = 1$  the process adopts the value from GCA
14:    else if  $c = 2$  then  $D.write(v_i)$ 
```

Algorithm 22 $GCA + \Omega = \text{Consensus}$

```
1:  $D$  a regular register
2:  $R[1..n]$   $n$  regular registers
3:  $GCA_1, GCA_2, \dots$  a series of graded commit adopt instances
4:  $\Omega$  failure detector
5:  $v_i \leftarrow v$  //  $v$  is the original input
6:  $k \leftarrow 0$ 
7:  $R[i] \leftarrow v$ 
8: while decision not reached do
9:    $k \leftarrow k + 1$ 
10:  if  $v' \leftarrow D.read() \neq \perp$  then Decide  $v'$ 
11:   $(c, v_i) \leftarrow GCA_k.propose(v_i)$ 
12:  if  $c = 0 \wedge R[\Omega].read() \neq \perp$  then  $v_i \leftarrow R[\Omega].read()$ 
13:    //  $c = 1$  the process adopts the value from GCA
14:  else if  $c = 2$  then  $D.write(v_i)$ 
```

Algorithm 23 $GCA + \Omega = \text{Consensus}$

```
1:  $D$  a regular register
2:  $R[1..n]$   $n$  regular registers
3:  $GCA_1, GCA_2, \dots$  a series of graded commit adopt instances
4:  $\Omega$  failure detector
5:  $v_i \leftarrow v$  //  $v$  is the original input
6:  $k \leftarrow 0$ 
7:  $R[i] \leftarrow v$ 
8: while decision not reached do
9:    $k \leftarrow k + 1$ 
10:  if  $v' \leftarrow D.\text{read}() \neq \perp$  then Decide  $v'$ 
11:   $(c, v_i) \leftarrow GCA_k.\text{propose}(v_i)$ 
12:  if  $c = 0 \wedge R[\Omega].\text{read}() \neq \perp$  then  $v_i \leftarrow R[\Omega].\text{read}()$ 
13:    //  $c = 1$  the process adopts the value from GCA
14:  else if  $c = 2$  then  $D.\text{write}(v_i)$ 
```

Algorithm 24 $GCA + \Omega = \text{Consensus}$

```
1:  $D$  a regular register
2:  $R[1..n]$   $n$  regular registers
3:  $GCA_1, GCA_2, \dots$  a series of graded commit adopt instances
4:  $\Omega$  failure detector
5:  $v_i \leftarrow v$  //  $v$  is the original input
6:  $k \leftarrow 0$ 
7:  $R[i] \leftarrow v$ 
8: while decision not reached do
9:    $k \leftarrow k + 1$ 
10:  if  $v' \leftarrow D.\text{read}() \neq \perp$  then Decide  $v'$ 
11:   $(c, v_i) \leftarrow GCA_k.\text{propose}(v_i)$ 
12:  if  $c = 0 \wedge R[\Omega].\text{read}() \neq \perp$  then  $v_i \leftarrow R[\Omega].\text{read}()$ 
13:    //  $c = 1$  the process adopts the value from GCA
14:  else if  $c = 2$  then  $D.\text{write}(v_i)$ 
```

Algorithm 25 $GCA + \Omega = \text{Consensus}$

```
1:  $D$  a regular register
2:  $R[1..n]$   $n$  regular registers
3:  $GCA_1, GCA_2, \dots$  a series of graded commit adopt instances
4:  $\Omega$  failure detector
5:  $v_i \leftarrow v$  //  $v$  is the original input
6:  $k \leftarrow 0$ 
7:  $R[i] \leftarrow v$ 
8: while decision not reached do
9:    $k \leftarrow k + 1$ 
10:  if  $v' \leftarrow D.\text{read}() \neq \perp$  then Decide  $v'$ 
11:   $(c, v_i) \leftarrow GCA_k.\text{propose}(v_i)$ 
12:  if  $c = 0 \wedge R[\Omega].\text{read}() \neq \perp$  then  $v_i \leftarrow R[\Omega].\text{read}()$ 
13:    //  $c = 1$  the process adopts the value from GCA
14:  else if  $c = 2$  then  $D.\text{write}(v_i)$ 
```

Table of Contents

- 1 FLP Review
- 2 Approximate Agreement
- 3 Commit Adopt
- 4 Randomized Consensus



Modified Ben-Or Consensus Protocol in Shared Memory

Algorithm 26 Ben-Or in shared memory

- 1: D a regular register
 - 2: $R[1..n]$ n regular registers
 - 3: GCA_1, GCA_2, \dots a series of graded commit adopt instances
 - 4: $v_i \leftarrow v$ // v is the original input
 - 5: $k \leftarrow 0$
 - 6: $R[i] \leftarrow v$
 - 7: **while** decision not reached **do**
 - 8: $k \leftarrow k + 1$
 - 9: **if** $v' \leftarrow D.\text{read}() \neq \perp$ **then** Decide v'
 - 10: $(c, v_i) \leftarrow GCA_k.\text{propose}(v_i)$
 - 11: **if** $c = 0$ **then** $v_i \leftarrow$ random bit
 - 12: // $c = 1$ the process adopts the value from GCA
 - 13: **else if** $c = 2$ **then** $D.\text{write}(v_i)$
-

Algorithm 27 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle DECIDE, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

Algorithm 28 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle DECIDE, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

Algorithm 29 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle DECIDE, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

Algorithm 30 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle DECIDE, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

Algorithm 31 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle DECIDE, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

Algorithm 32 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle DECIDE, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

Algorithm 33 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle \text{DECIDE}, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

Algorithm 34 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle DECIDE, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

Algorithm 35 Ben-Or in message passing

```
1:  $v_i \leftarrow v$  //  $v$  is the original input
2:  $k \leftarrow 0$ 
3: while decision not reached do
4:    $k \leftarrow k + 1$ 
5:   Send  $\langle m_1, k, v_i \rangle$  to all
6:   Wait for  $n - f$  messages  $\langle m_1, k, * \rangle$ 
7:   if All msgs are  $\langle m_1, k, v \rangle$  then send  $\langle m_2, k, v \rangle$ 
8:   else send  $\langle m_2, k, \perp \rangle$ 
9:   Wait for  $n - f$  messages  $\langle m_2, k, * \rangle$ 
10:  //  $n - f = f + 1$ 
11:  if All msgs are  $\langle m_2, k, v \rangle$  where  $v \neq \perp$  then send  $\langle DECIDE, k, v \rangle$ 
12:  else if  $\exists \langle m_2, k, v \rangle$  where  $v \neq \perp$  then  $v_i \leftarrow v$ 
13:  else  $v_i \leftarrow$  Random bit
```

The expected number of rounds is $\mathbb{E}[R] = \sum_{r=1}^{\infty} (r \times P(\text{Decide at round } r))$.

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Let p be the probability that all processes get the same value.

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Let p be the probability that all processes get the same value.

$$P(\text{Decide at round } r) = (1 - p)^{r-1} p.$$

The expected number of rounds is $\mathbb{E}[R] = \sum_{r=1}^{\infty} (r \times P(\text{Decide at round } r))$.

Let p be the probability that all processes get the same value.

$$P(\text{Decide at round } r) = (1 - p)^{r-1} p.$$

$$\mathbb{E}[R] = \sum_{r=1}^{\infty} (r(1 - p)^{r-1} p) = \frac{1}{p}.$$

The expected number of rounds is $\mathbb{E}[R] = \sum_{r=1}^{\infty} (r \times P(\text{Decide at round } r))$.

Let p be the probability that all processes get the same value.

$$P(\text{Decide at round } r) = (1 - p)^{r-1} p.$$

$$\mathbb{E}[R] = \sum_{r=1}^{\infty} (r(1 - p)^{r-1} p) = \frac{1}{p}.$$

The probability of a decision being reached at every round as a result of all flips matching is: $p = 2^{-n}$. Hence, the number of expected rounds is $O(2^n)$.

Shared Memory Common Coin

Algorithm 36 Bracha-Rachman common coin

```
1: done – shared atomic register
2: R[1..n] – n atomic registers
3: count  $\leftarrow$  0
4: sum  $\leftarrow$  0
5: while not done do
6:   count  $\leftarrow$  count + 1
7:   sum  $\leftarrow$  sum + flip()    // The flip result is -1 or +1
8:   R[i].write((count, sum))
9:   if count mod n = 0 then
10:    U  $\leftarrow$  Read R[1..n]
11:    if  $\sum_{i=1}^n U[i].count \geq n^2$  then
12:      done  $\leftarrow$  true
13:      Decide  $\text{sgn}(\sum_{i=1}^n U[i].sum)$ 
```

Shared Memory Common Coin

Algorithm 37 Bracha-Rachman common coin

```
1: done – shared atomic register
2:  $R[1..n]$  –  $n$  atomic registers
3: count  $\leftarrow 0$ 
4: sum  $\leftarrow 0$ 
5: while not done do
6:   count  $\leftarrow$  count + 1
7:   sum  $\leftarrow$  sum + flip()    // The flip result is -1 or +1
8:    $R[i].\text{write}((\textit{count}, \textit{sum}))$ 
9:   if count mod  $n = 0$  then
10:     $U \leftarrow \text{Read } R[1..n]$ 
11:    if  $\sum_{i=1}^n U[i].\textit{count} \geq n^2$  then
12:      done  $\leftarrow$  true
13:      Decide  $\textit{sgn}(\sum_{i=1}^n U[i].\textit{sum})$ 
```

Shared Memory Common Coin

Algorithm 38 Bracha-Rachman common coin

```
1: done ← shared atomic register
2:  $R[1..n]$  ←  $n$  atomic registers
3: count ← 0
4: sum ← 0
5: while not done do
6:   count ← count + 1
7:   sum ← sum + flip()    // The flip result is -1 or +1
8:    $R[i].write((count, sum))$ 
9:   if count mod  $n = 0$  then
10:     $U \leftarrow \text{Read } R[1..n]$ 
11:    if  $\sum_{i=1}^n U[i].count \geq n^2$  then
12:      done ← true
13:      Decide  $sgn(\sum_{i=1}^n U[i].sum)$ 
```

Shared Memory Common Coin

Algorithm 39 Bracha-Rachman common coin

```
1: done ← shared atomic register
2:  $R[1..n]$  ←  $n$  atomic registers
3: count ← 0
4: sum ← 0
5: while not done do
6:   count ← count + 1
7:   sum ← sum + flip()    // The flip result is -1 or +1
8:    $R[i].write((count, sum))$ 
9:   if count mod  $n = 0$  then
10:     $U \leftarrow \text{Read } R[1..n]$ 
11:    if  $\sum_{i=1}^n U[i].count \geq n^2$  then
12:      done ← true
13:      Decide  $sgn(\sum_{i=1}^n U[i].sum)$ 
```

Shared Memory Common Coin

Algorithm 40 Bracha-Rachman common coin

```
1: done ← shared atomic register
2:  $R[1..n]$  ←  $n$  atomic registers
3: count ← 0
4: sum ← 0
5: while not done do
6:   count ← count + 1
7:   sum ← sum + flip()    // The flip result is -1 or +1
8:    $R[i].write((count, sum))$ 
9:   if count mod  $n = 0$  then
10:     $U \leftarrow \text{Read } R[1..n]$ 
11:    if  $\sum_{i=1}^n U[i].count \geq n^2$  then
12:      done ← true
13:      Decide  $sgn(\sum_{i=1}^n U[i].sum)$ 
```

Shared Memory Common Coin

Algorithm 41 Bracha-Rachman common coin

```
1: done ← shared atomic register
2:  $R[1..n]$  ←  $n$  atomic registers
3: count ← 0
4: sum ← 0
5: while not done do
6:   count ← count + 1
7:   sum ← sum + flip()    // The flip result is -1 or +1
8:    $R[i].\text{write}((\textit{count}, \textit{sum}))$ 
9:   if count mod  $n = 0$  then
10:     $U \leftarrow \text{Read } R[1..n]$ 
11:    if  $\sum_{i=1}^n U[i].\textit{count} \geq n^2$  then
12:      done ← true
13:      Decide  $\text{sgn}(\sum_{i=1}^n U[i].\textit{sum})$ 
```

Shared Memory Common Coin

Algorithm 42 Bracha-Rachman common coin

```
1: done ← shared atomic register
2:  $R[1..n]$  ←  $n$  atomic registers
3: count ← 0
4: sum ← 0
5: while not done do
6:   count ← count + 1
7:   sum ← sum + flip()    // The flip result is -1 or +1
8:    $R[i].write((count, sum))$ 
9:   if count mod  $n = 0$  then
10:     $U \leftarrow \text{Read } R[1..n]$ 
11:    if  $\sum_{i=1}^n U[i].count \geq n^2$  then
12:      done ← true
13:      Decide  $sgn(\sum_{i=1}^n U[i].sum)$ 
```

Shared Memory Common Coin – Analysis

The summation of n^2 can be approximated to a normal random function.



Shared Memory Common Coin – Analysis

The summation of n^2 can be approximated to a normal random function.
The probability that $sum \geq cn$ can be lowerbounded by a constant.



Shared Memory Common Coin – Analysis

The summation of n^2 can be approximated to a normal random function.

The probability that $sum \geq cn$ can be lowerbounded by a constant.

The probability that $count$ exceeds n^2 by more than $O(n)$ can be bounded by a constant.



Shared Memory Common Coin – Analysis

The summation of n^2 can be approximated to a normal random function.

The probability that $sum \geq cn$ can be lowerbounded by a constant.

The probability that *count* exceeds n^2 by more than $O(n)$ can be bounded by a constant.

The probability that processes agree is therefore constant.

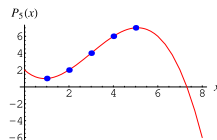
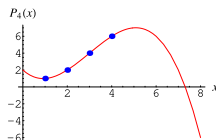
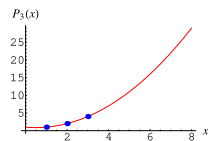
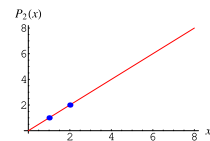


Message Passing Common Coin

Digital Signatures:

- **Unforgeability** – Processes with not enough keys cannot produce a signature.
- **Uniqueness** – Processes with enough keys always generate the same signature for the same message.

How to achieve it? – Polynomial interpolation.



These coins have constant success probability \rightarrow randomized consensus takes a constant amount of times in expectation.



Good Luck with the Exam!

