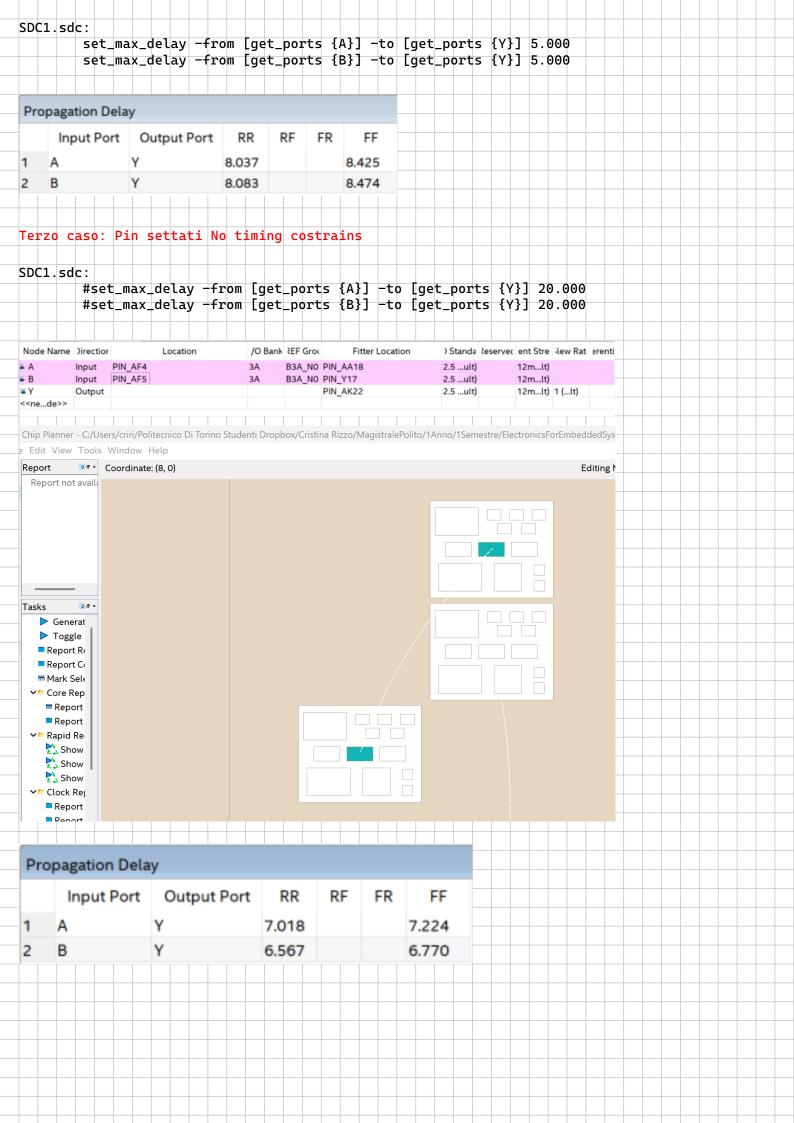
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Input Port Output Port RR RF FR FF 1	_,																			Ш	\vdash	$\overline{}$	_		$\overline{}$	_		-	<u> </u>	_	_	\perp	_	+	+	-	-	+
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2 B Y 6.165 6.325 DC1.sdc: set_max_delay -from [get_ports {A}] -to [get_ports {Y}] 10.000 set_max_delay -from [get_ports {B}] -to [get_ports {Y}] 10.000 Propagation Delay Input Port Output Port RR RF FR FF 1 A Y 5.660 5.751	-	1		F													6.	115	5	\vdash	\square	\dashv	\rightarrow	\dashv	\Box	-	\dashv		-	+	_	+	+	+	+	-	_	+
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Input Port Output Port RR RF FR FF		Pro	nag	atio	o Dr	ela	v				H		I					I																				I
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Quarto caso: Pin settati lontani No timing costrains
SDC1.sdc:
          #set_max_delay -from [get_ports {A}] -to [get_ports {Y}] 20.000
#set_max_delay -from [get_ports {B}] -to [get_ports {Y}] 20.000
                                  50 PIN
           /O Bank REF Grou er Locat D Standa Reserved ent Stre Flew Rat Perential Flalog Se VCCT_C I/O Pin ted I
Node Name Direction
                     Location
- A
                   PIN_AD9
                                        B3A_N0 PI...D9 2.5 V
           Input
                                зА
                                                                      12m...lt)
⊸ B
                   PIN_C13
                                        B8A_N0 PIN_C13 2.5 V
           Input
                                8A
                                                                      12m...lt)
¥ Y
           Output
                                               Pl...10
                                                       2.5 ...ult)
                                                                      12m...lt) 1 (...lt)
Propagation Delay
       Input Port Output Port
                                                              FF
                                       RR
                                     7.009
                                                           7.351
2
     В
                                     9.368
                                                           10.003
```

