

Programmable Logic Devices

First Laboratory Session

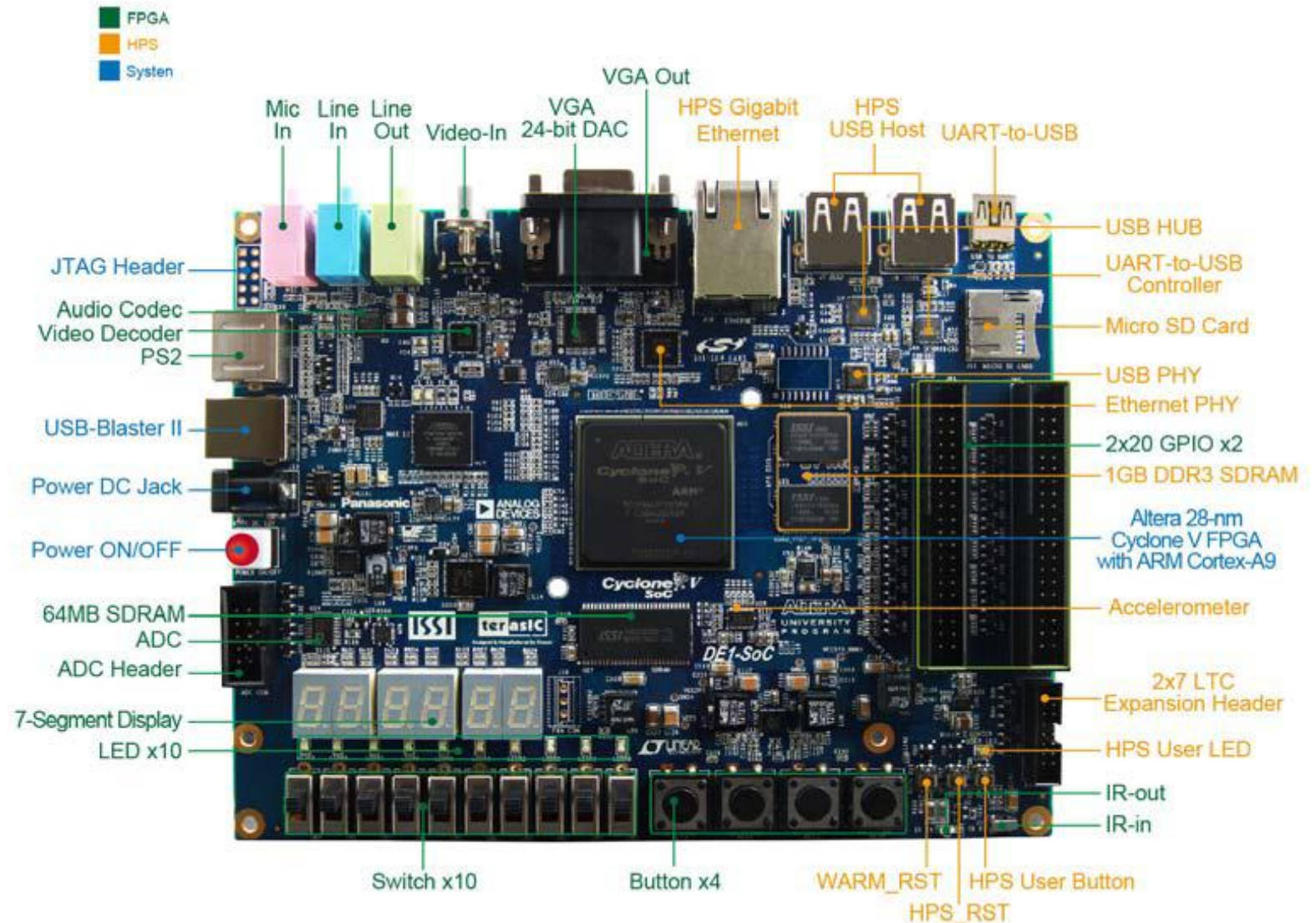
Prof. Claudio Passerone

(Electronics for Embedded Systems)

Altera DE1-SoC Board

- Altera DE1-SoC Board

- FPGA + HPS
- Memories
- ADCs
- Switches
- Buttons
- LEDs
- Displays
- Codecs
 - Audio
 - Video
- Connectors
- Expansion Headers



Altera DE1-SoC Board

- Pin assignments
 - Switches
 - SW0 → PIN_AB12
 - SW1 → PIN_AC12
 - ...
 - Buttons
 - KEY0 → PIN_AA14
 - ...
 - LEDs
 - LEDR0 → PIN_V16
 - ...
 - Clock
 - CLOCK_50 → PIN_AF14

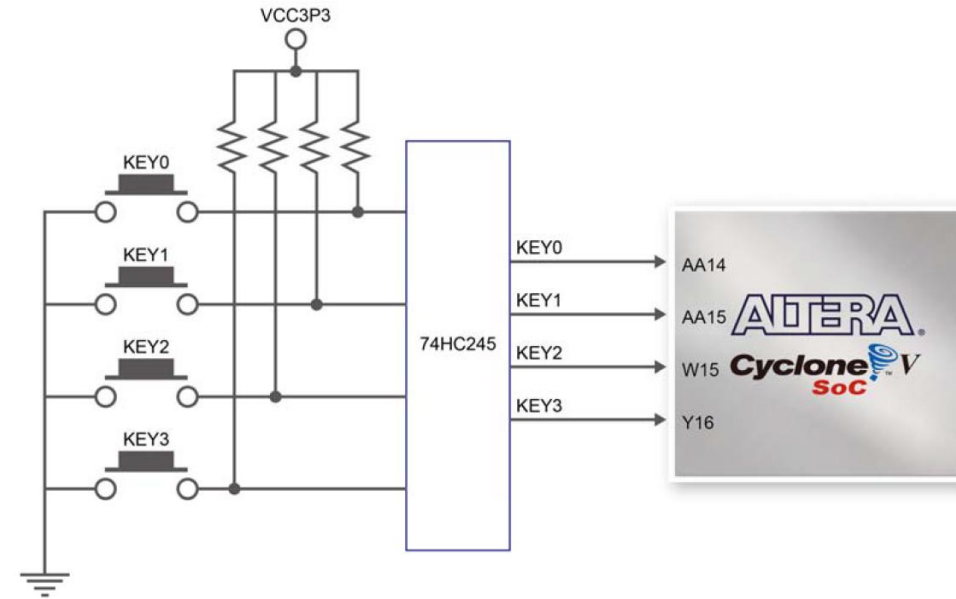
Signal Name	FPGA Pin No.	Description	I/O Standard
SW[0]	PIN_AB12	Slide Switch[0]	3.3V
SW[1]	PIN_AC12	Slide Switch[1]	3.3V
SW[2]	PIN_AF9	Slide Switch[2]	3.3V
SW[3]	PIN_AF10	Slide Switch[3]	3.3V
SW[4]	PIN_AD11	Slide Switch[4]	3.3V
SW[5]	PIN_AD12	Slide Switch[5]	3.3V
SW[6]	PIN_AE11	Slide Switch[6]	3.3V
SW[7]	PIN_AC9	Slide Switch[7]	3.3V
SW[8]	PIN_AD10	Slide Switch[8]	3.3V

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY[0]	PIN_AA14	Push-button[0]	3.3V
KEY[1]	PIN_AA15	Push-button[1]	3.3V
KEY[2]	PIN_W15	Push-button[2]	3.3V
KEY[3]	PIN_Y16	Push-button[3]	3.3V

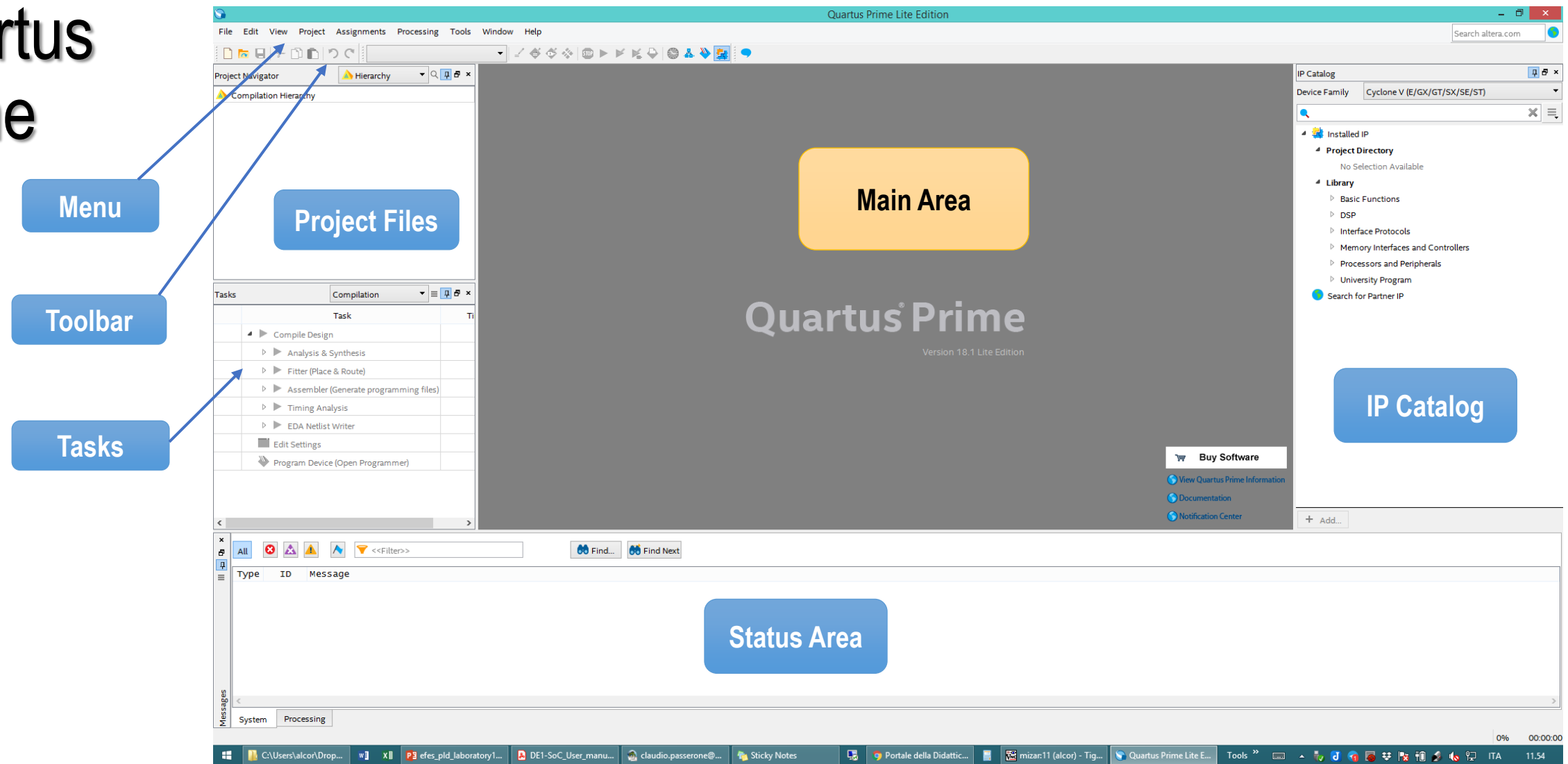
Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR[0]	PIN_V16	LED [0]	3.3V
LEDR[1]	PIN_W16	LED [1]	3.3V
LEDR[2]	PIN_V17	LED [2]	3.3V
LEDR[3]	PIN_V18	LED [3]	3.3V
LEDR[4]	PIN_W17	LED [4]	3.3V
LEDR[5]	PIN_W19	LED [5]	3.3V
LEDR[6]	PIN_Y19	LED [6]	3.3V
LEDR[7]	PIN_W20	LED [7]	3.3V
LEDR[8]	PIN_W21	LED [8]	3.3V
LEDR[9]	PIN_Y21	LED [9]	3.3V

Altera DE1-SoC Board

- Schematic diagrams
 - Useful to understand how things work
- See also
 - UART
 - Expansion Headers
 - VGA (Triple DAC)
 - 7-Seg Displays

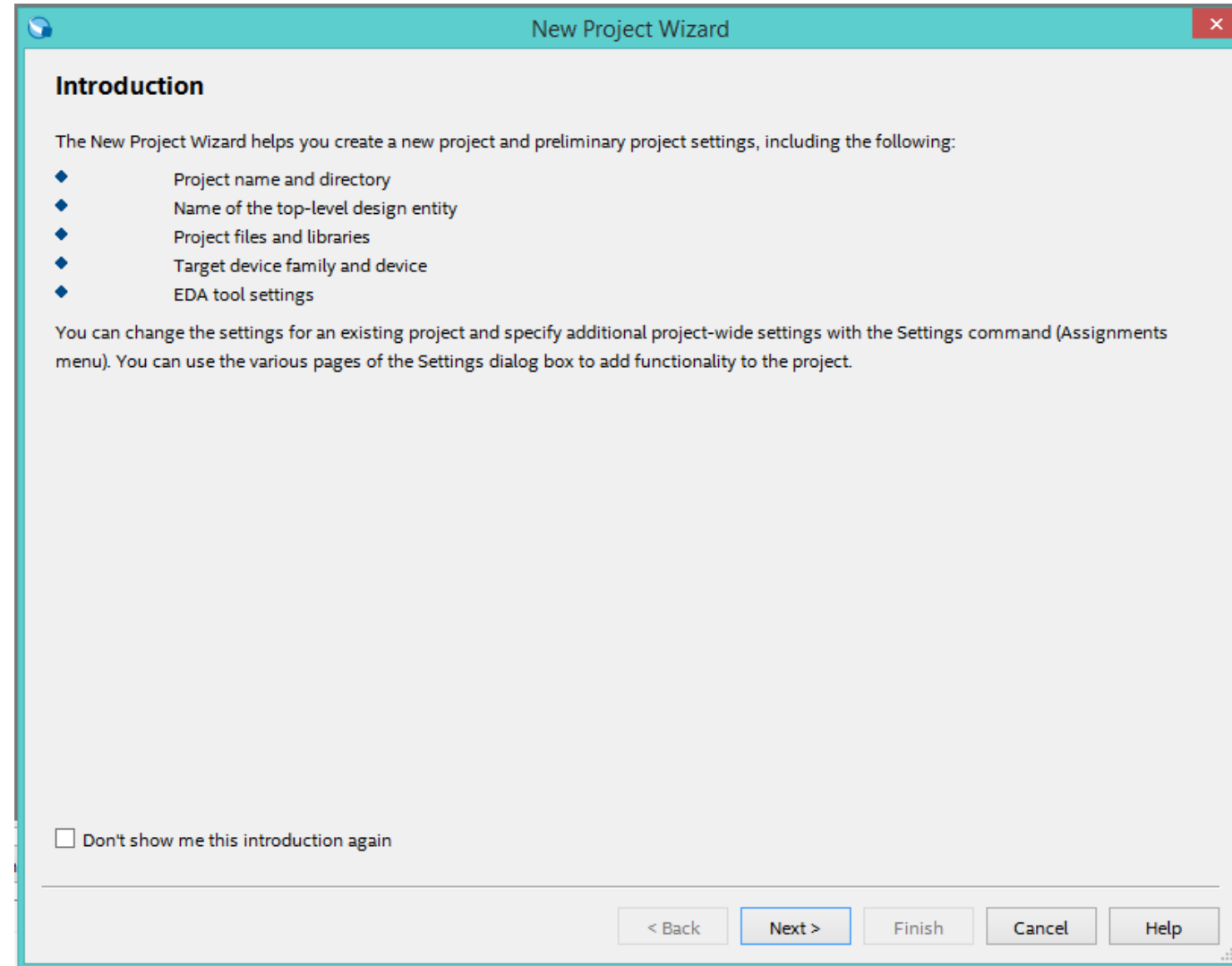


Quartus Prime



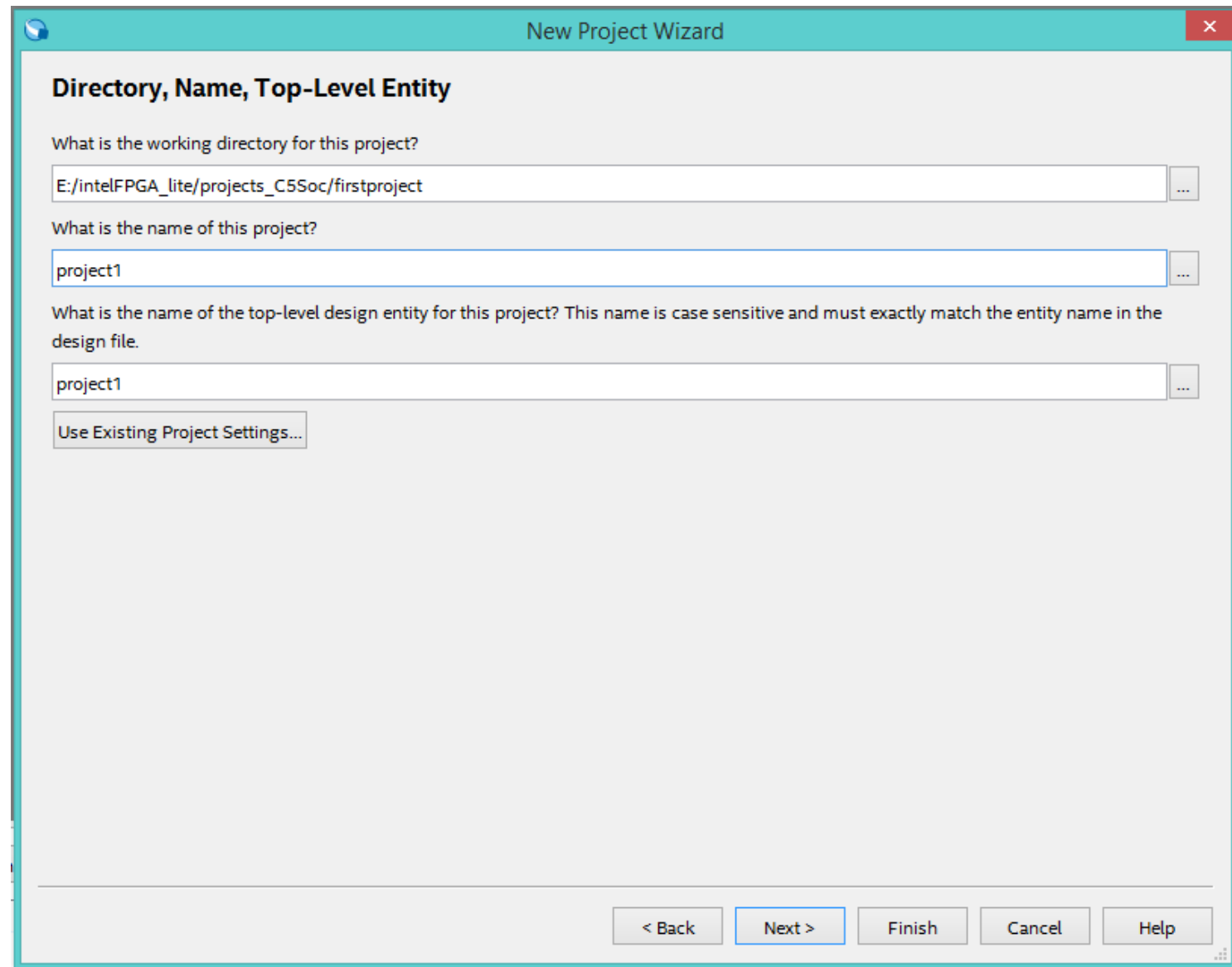
Quartus Prime

- Projects
 - Create a project
 - Under File menu
 - Choose New Project Wizard...
 - Click Next in the window that appears



Quartus Prime

- Projects
 - Create a project
 - Specify design directory
 - Directory names without spaces
 - You can use the character / (slash) instead of \ (backslash) to separate folder names
 - Make sure to have write access to the selected directory
 - Click Next



The screenshot shows the 'New Project Wizard' dialog box in Quartus Prime. The title bar is teal with a close button. The main area is light gray. The first section is titled 'Directory, Name, Top-Level Entity'. It contains three text input fields, each with a browse button (three dots) to its right. The first field is labeled 'What is the working directory for this project?' and contains the path 'E:/intelFPGA_lite/projects_C5Soc/firstproject'. The second field is labeled 'What is the name of this project?' and contains 'project1'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and contains 'project1'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom of the dialog are five buttons: '< Back', 'Next >' (highlighted with a blue border), 'Finish', 'Cancel', and 'Help'.

Directory, Name, Top-Level Entity

What is the working directory for this project?

E:/intelFPGA_lite/projects_C5Soc/firstproject

What is the name of this project?

project1

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

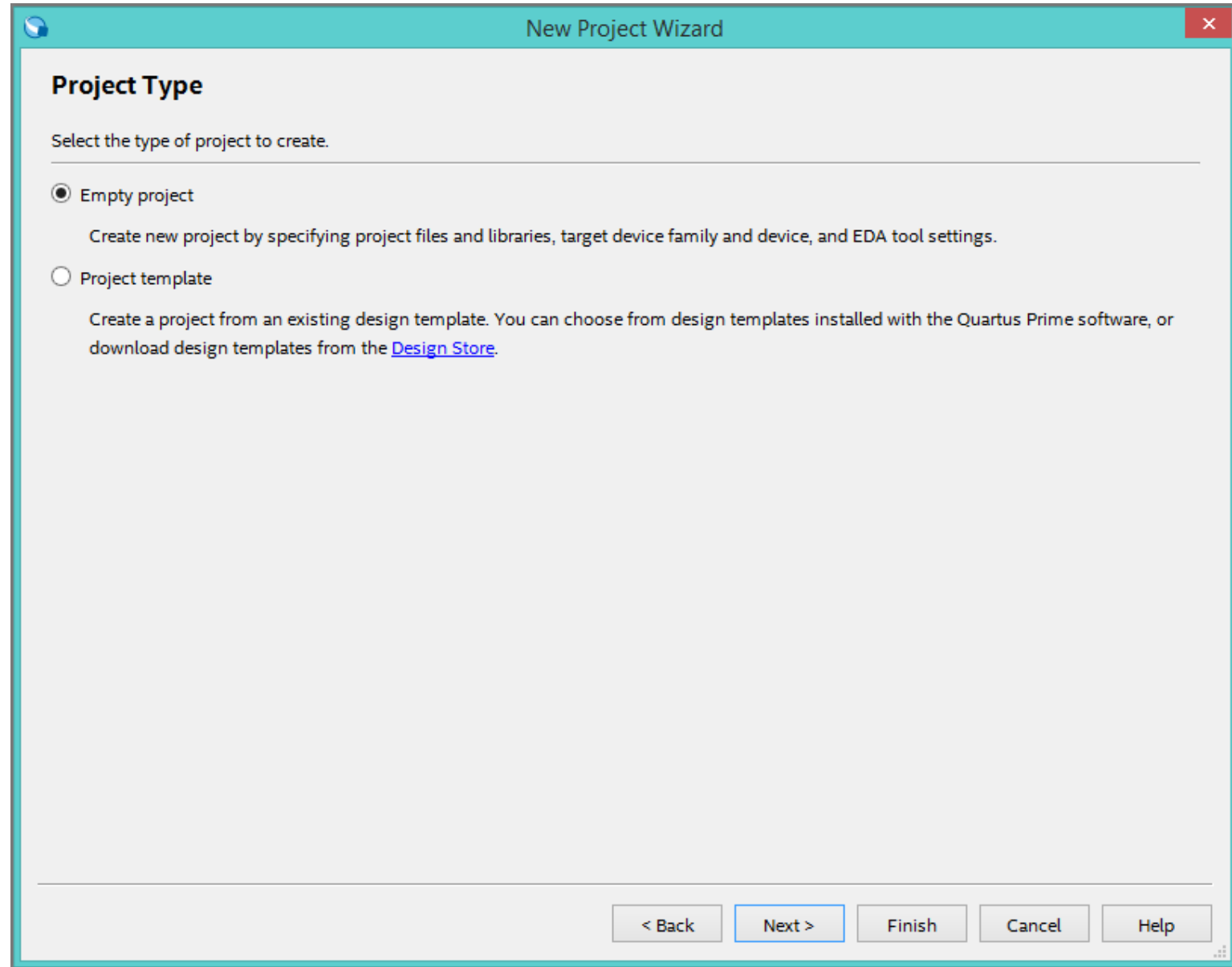
project1

Use Existing Project Settings...

< Back Next > Finish Cancel Help

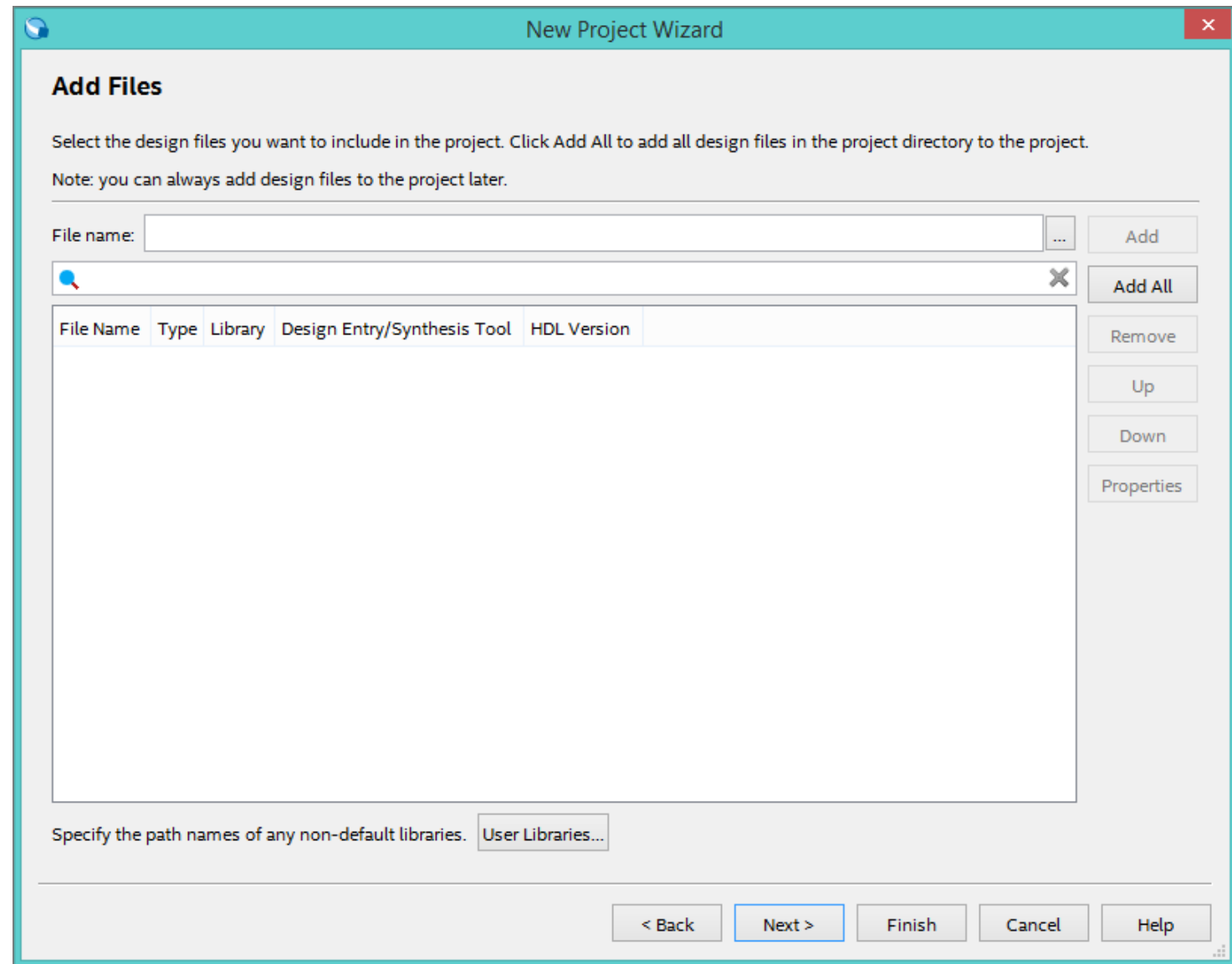
Quartus Prime

- Projects
 - Create a project
 - Specify template
 - Use Empty project if there is no template
 - Click Next



Quartus Prime

- Projects
 - Create a project
 - Specify design files
 - Add design files here if any
 - Otherwise simply click Next
 - You can always add design files later
 - You can write design files within the tool



Quartus Prime

- Projects

- Create a project

- Select the device

- 5CSEMA5F31C6
 - Cyclone V family
 - FBGA Package
 - 896 pins
 - Speed grade 6
 - Click Next

- Different board

- Cyclone 10 LP family
 - 10CL025YE144C8G
 - 10CL006YE144C8G

The screenshot shows the 'New Project Wizard' dialog box in Quartus Prime, specifically the 'Family, Device & Board Settings' tab. The 'Device' sub-tab is selected. The dialog provides instructions on selecting a device family and device, and offers a link to the 'Device Support List' webpage. It includes dropdown menus for 'Device family' (set to 'Cyclone V (E/GX/GT/SX/SE/ST)') and 'Device' (set to 'All'). There are radio buttons for 'Target device' selection: 'Auto device selected by the Fitter', 'Specific device selected in 'Available devices' list' (which is selected), and 'Other: n/a'. To the right, there are dropdowns for 'Package' (set to 'FBGA'), 'Pin count' (set to '896'), and 'Core speed grade' (set to '6'), along with a 'Name filter' text box and a checked 'Show advanced devices' checkbox. At the bottom, an 'Available devices' table lists the selected device. Navigation buttons at the bottom include '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'.

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: FBGA

Pin count: 896

Core speed grade: 6

Name filter:

☒ Show advanced devices

Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS
5CSEMA5F31C6	1.1V	32070	457	457	0	0

< Back Next > Finish Cancel Help

Quartus Prime

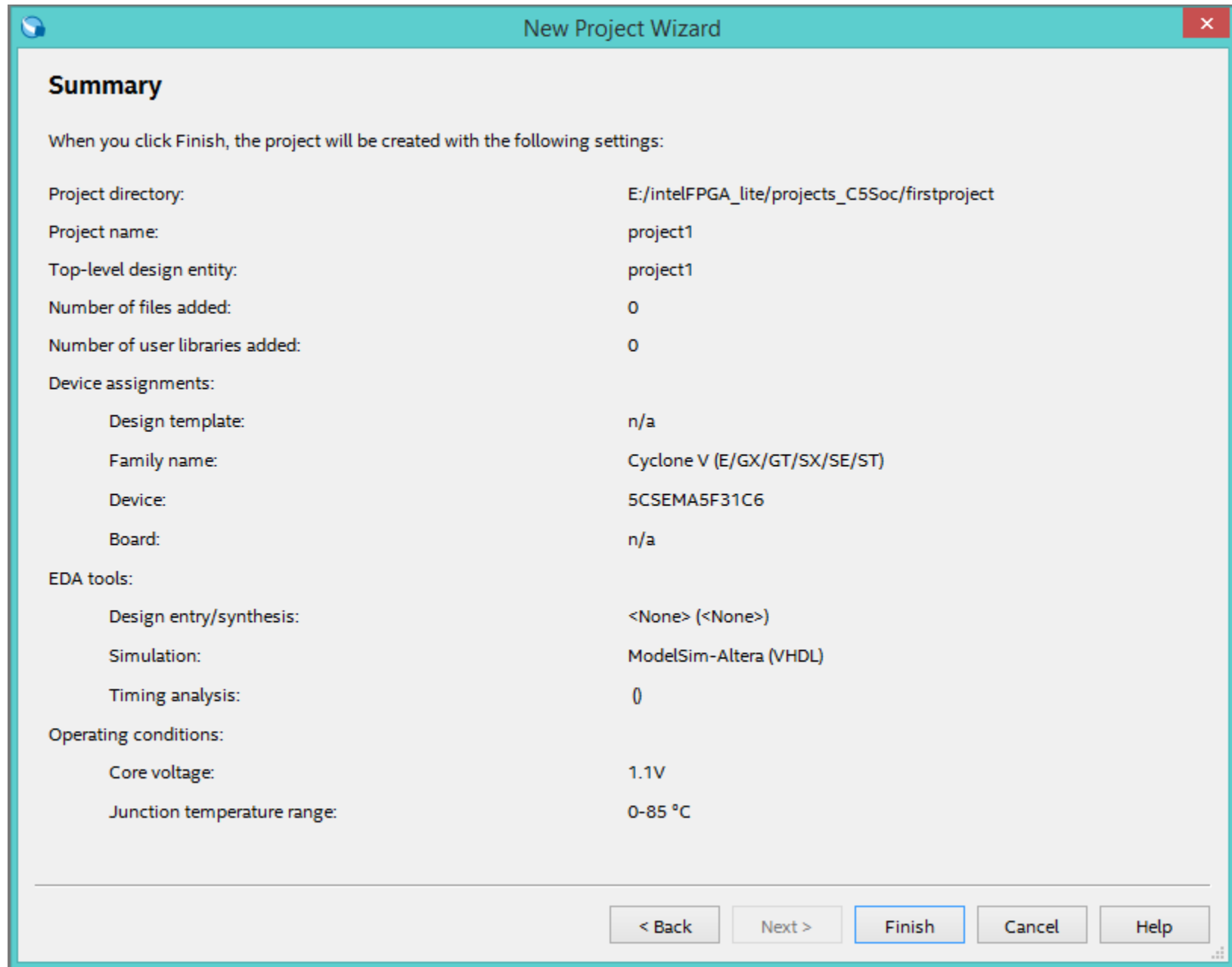
- Projects
 - Create a project
 - Select the simulator
 - ModelSim-Altera
 - Specify VHDL as the Format
 - All others tools are already included
 - Or not needed in this class
 - When designing a NiosII system or an HPS system you may want to leave this blank
 - Click Next

The screenshot shows the 'New Project Wizard' window in Quartus Prime, specifically the 'EDA Tool Settings' step. The window has a title bar with a close button. Below the title bar, the text 'Specify the other EDA tools used with the Quartus Prime software to develop your project.' is displayed. The main area is titled 'EDA tools:' and contains a table with four columns: 'Tool Type', 'Tool Name', 'Format(s)', and 'Run Tool Automatically'. The table has five rows. The first row is for 'Design Entry/Synth...' with 'Tool Name' set to '<None>' and 'Format(s)' set to '<None>'. The second row is for 'Simulation' with 'Tool Name' set to 'ModelSim-Altera' and 'Format(s)' set to 'VHDL'. The third row is for 'Board-Level' with 'Tool Name' set to 'Timing' and 'Format(s)' set to '<None>'. The fourth row is for 'Symbol' with 'Tool Name' set to 'Symbol' and 'Format(s)' set to '<None>'. The fifth row is for 'Signal Integrity' with 'Tool Name' set to 'Signal Integrity' and 'Format(s)' set to '<None>'. The 'Run Tool Automatically' column has checkboxes for each row. The first checkbox is checked, and the second is unchecked. Below the table, there is a large empty text area. At the bottom of the window, there are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a blue border.

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synth...	<None>	<None>	<input checked="" type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

Quartus Prime

- Projects
 - Create a project
 - Summary
 - Check all data
 - Click Finish



The screenshot shows the 'New Project Wizard' window in Quartus Prime, specifically the 'Summary' tab. The window has a teal title bar with the text 'New Project Wizard' and a close button. The main content area is light gray and contains a 'Summary' section. Below the title, it says 'When you click Finish, the project will be created with the following settings:'. The settings are listed in a two-column format. The first column lists the settings, and the second column shows the values. The settings include Project directory, Project name, Top-level design entity, Number of files added, Number of user libraries added, Device assignments (Design template, Family name, Device, Board), EDA tools (Design entry/synthesis, Simulation, Timing analysis), and Operating conditions (Core voltage, Junction temperature range). At the bottom right, there are five buttons: '< Back', 'Next >', 'Finish' (which is highlighted with a blue border), 'Cancel', and 'Help'.

Summary	
When you click Finish, the project will be created with the following settings:	
Project directory:	E:/intelFPGA_lite/projects_C5Soc/firstproject
Project name:	project1
Top-level design entity:	project1
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone V (E/GX/GT/SX/SE/ST)
Device:	5CSEMA5F31C6
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	ModelSim-Altera (VHDL)
Timing analysis:	0
Operating conditions:	
Core voltage:	1.1V
Junction temperature range:	0-85 °C

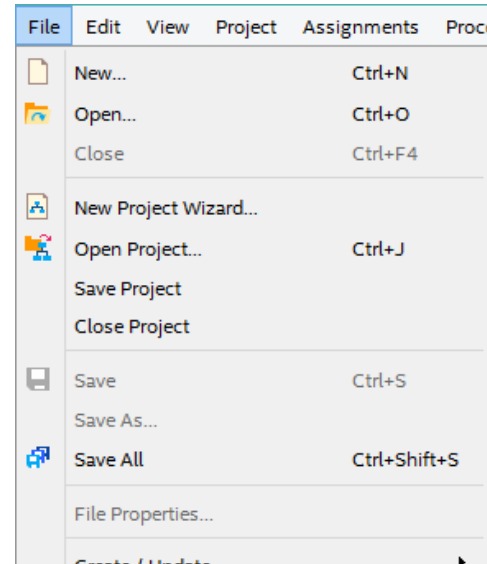
< Back Next > **Finish** Cancel Help

Quartus Prime

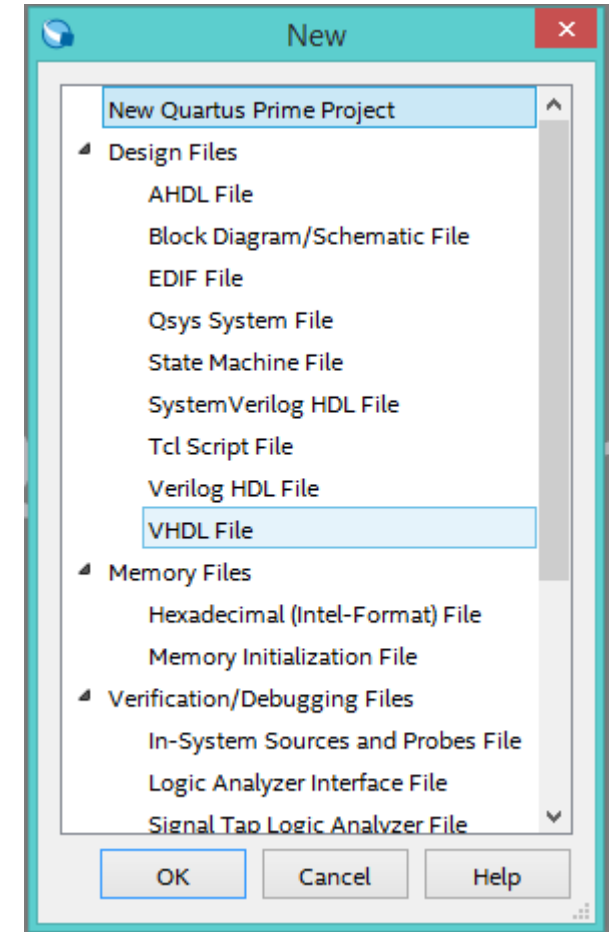
- Editor

- Create new VHDL file

- Under File menu
 - Click New
 - Choose your desired language
 - Editor provides syntax highlighting
 - You can use your own editor, if you prefer
 - One entity in each file
 - Save the file in the project directory
 - Give to the file the same name of the entity
 - Makes debugging easier



```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity project1 is
5      port (
6          a, b: in std_logic;
7          y: out std_logic
8      );
9  end entity project1;
10
11 architecture rtl of project1 is
12 begin
13
14     y <= a and b;
15
16 end architecture rtl;
```



File name: project1.vhd

Quartus Prime

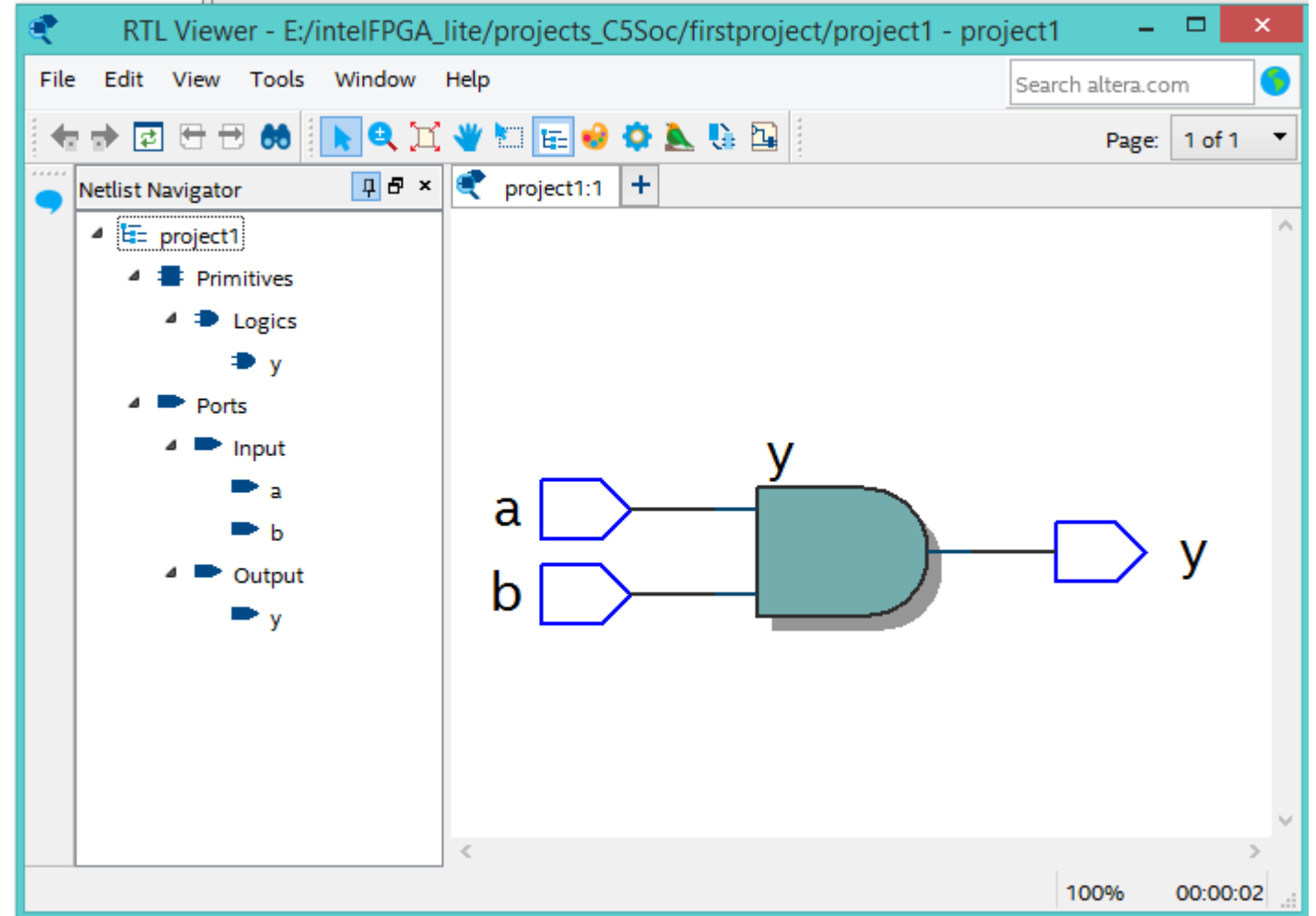
- Initial synthesis
 - Under Processing menu
 - Analyze Current File
 - Check syntax errors
 - Try inserting syntax errors to see what happens
 - Check also warnings
 - In particular Critical Warnings
 - Start → Start Analysis & Elaboration
 - Initial synthesis of the entire design
 - Generates an initial netlist
 - Generates an initial report

The image shows two screenshots from the Quartus Prime software interface. The top screenshot displays the 'Processing' menu, which includes options like 'Stop Processing', 'Start Compilation', 'Analyze Current File', 'Start', 'Update Memory Initialization File', 'Compilation Report', 'Dynamic Synthesis Report', 'Power Analyzer Tool', 'SSN Analyzer Tool', and 'Receive Compilation Status Notifications'. The 'Start' option is highlighted, showing a submenu with 'Start Hierarchy Elaboration', 'Start Analysis & Elaboration' (highlighted), 'Start Analysis & Synthesis', 'Start Partition Merge', 'Start Fitter', 'Start Assembler', 'Start Timing Analyzer', 'Start EDA Netlist Writer', 'Start Design Assistant', 'Start Power Analyzer', 'Start SSN Analyzer', and 'Start Rapid Recompile'. The bottom screenshot shows the 'Flow Summary' window, which provides a detailed overview of the compilation process, including flow status, version information, and resource utilization.

Flow Summary	
Flow Status	Successful - Mon Oct 19 12:27:56 2020
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	project1
Top-level Entity Name	project1
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	N/A until Partition Merge
Total registers	N/A until Partition Merge
Total pins	N/A until Partition Merge
Total virtual pins	N/A until Partition Merge
Total block memory bits	N/A until Partition Merge
Total PLLs	N/A until Partition Merge
Total DLLs	N/A until Partition Merge

Quartus Prime

- Initial synthesis
 - Under Tools menu
 - Netlist Viewers → RTL Viewer



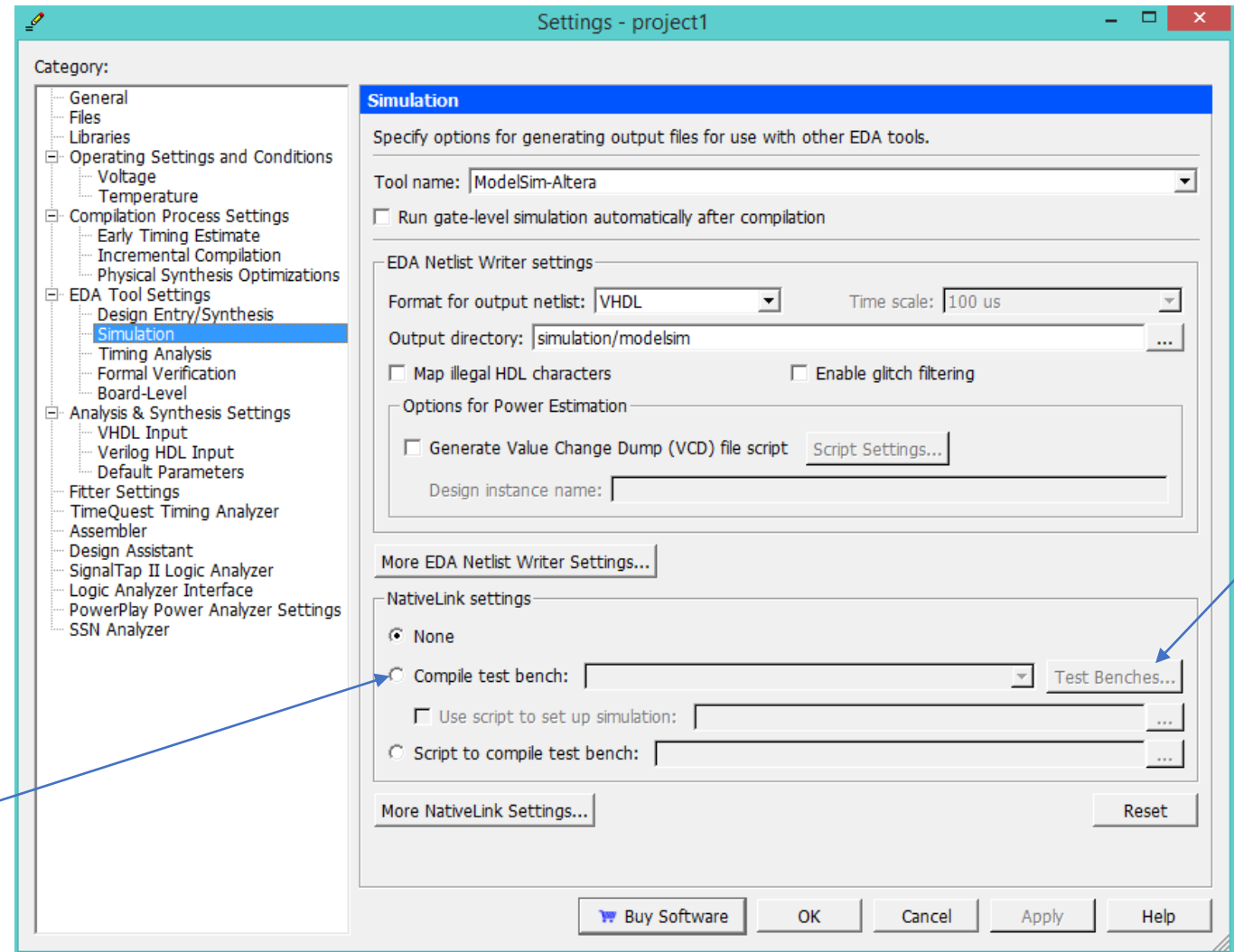
Quartus Prime

- Writing a testbench
 - Entity with no ports
 - Component is the Device Under Test (DUT)
 - Specify a label for the port map
 - Used later in simulation
 - Specify signals and initialize them
 - Specify a clock
 - Dedicated process
 - Specify stimuli
 - Another Process
 - Use wait to let time pass
 - It is not synthesizable
 - Save it in the project directory

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_unsigned.all;
4  use ieee.std_logic_arith.all;
5
6  entity testbench is
7  end entity;
8
9  architecture struct of testbench is
10
11     component project1 is
12     port (
13         a, b: in  std_logic;
14         y:   out std_logic
15     );
16     end component project1;
17
18     signal a: std_logic := '0';
19     signal b: std_logic := '0';
20     signal y: std_logic;
21
22     signal clk: std_logic := '0';
23     constant clk_period: time := 5 ns;
24
25     begin
26
27         dut: project1 port map (a, b, y);
28
29         myclock: process is
30         begin
31             clk <= '0';
32             wait for clk_period/2;
33             clk <= '1';
34             wait for clk_period/2;
35         end process myclock;
36
37         stim: process is
38         begin
39             a <= '0';
40             b <= '0';
41             wait for 20 ns;
42             a <= '1';
43             wait for 20 ns;
44             a <= '0';
45             b <= '1';
46             wait for 20 ns;
47             a <= '1';
48             wait;
49         end process stim;
50
51     end architecture struct;
```

Quartus Prime

- Configure Simulator
 - Under Assignments menu
 - Choose Settings...
 - Select Simulation on the left pane
 - Click on Compile test bench
 - Click on Test Benches...



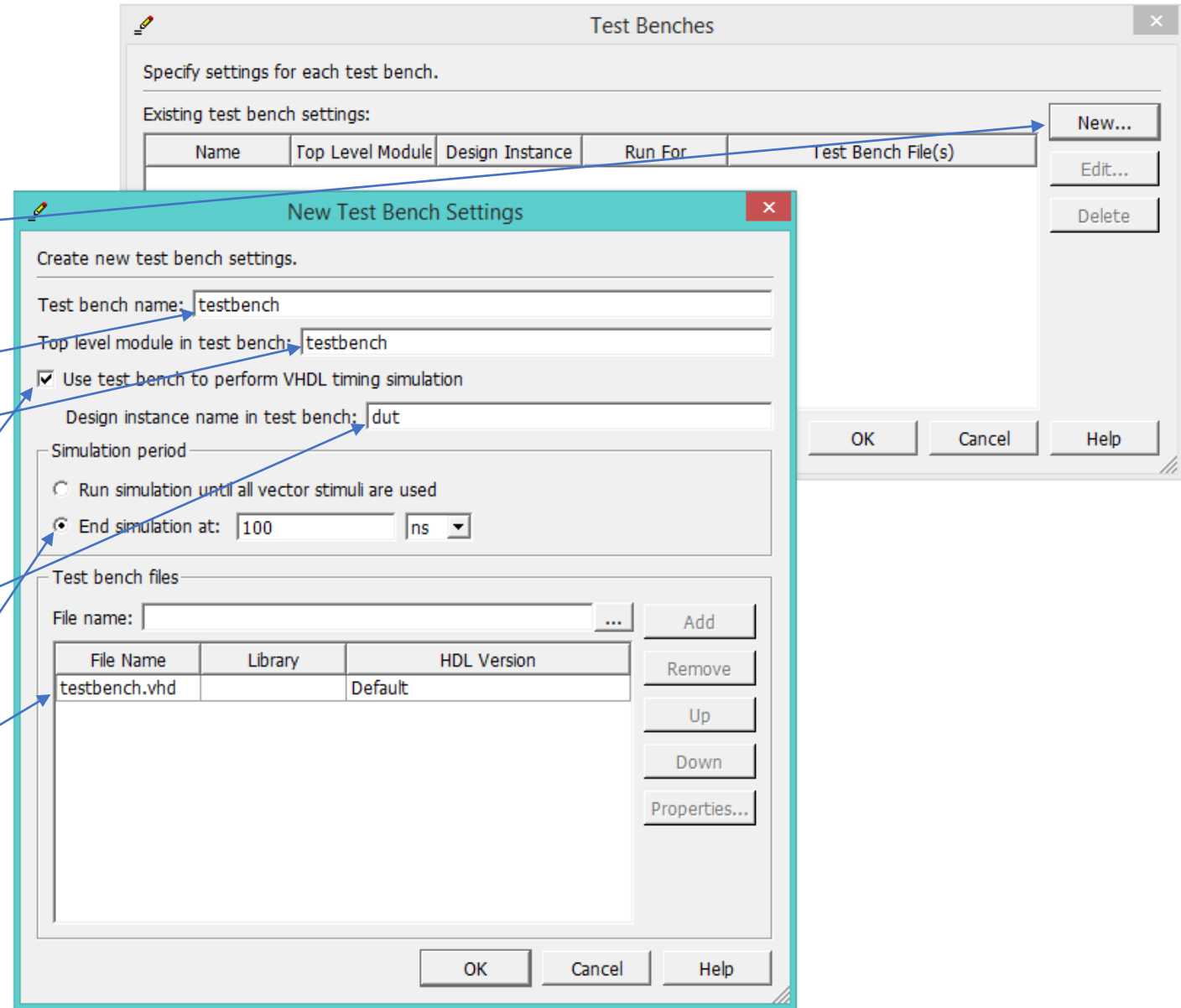
Quartus Prime

- Configure Simulator

- Click on New

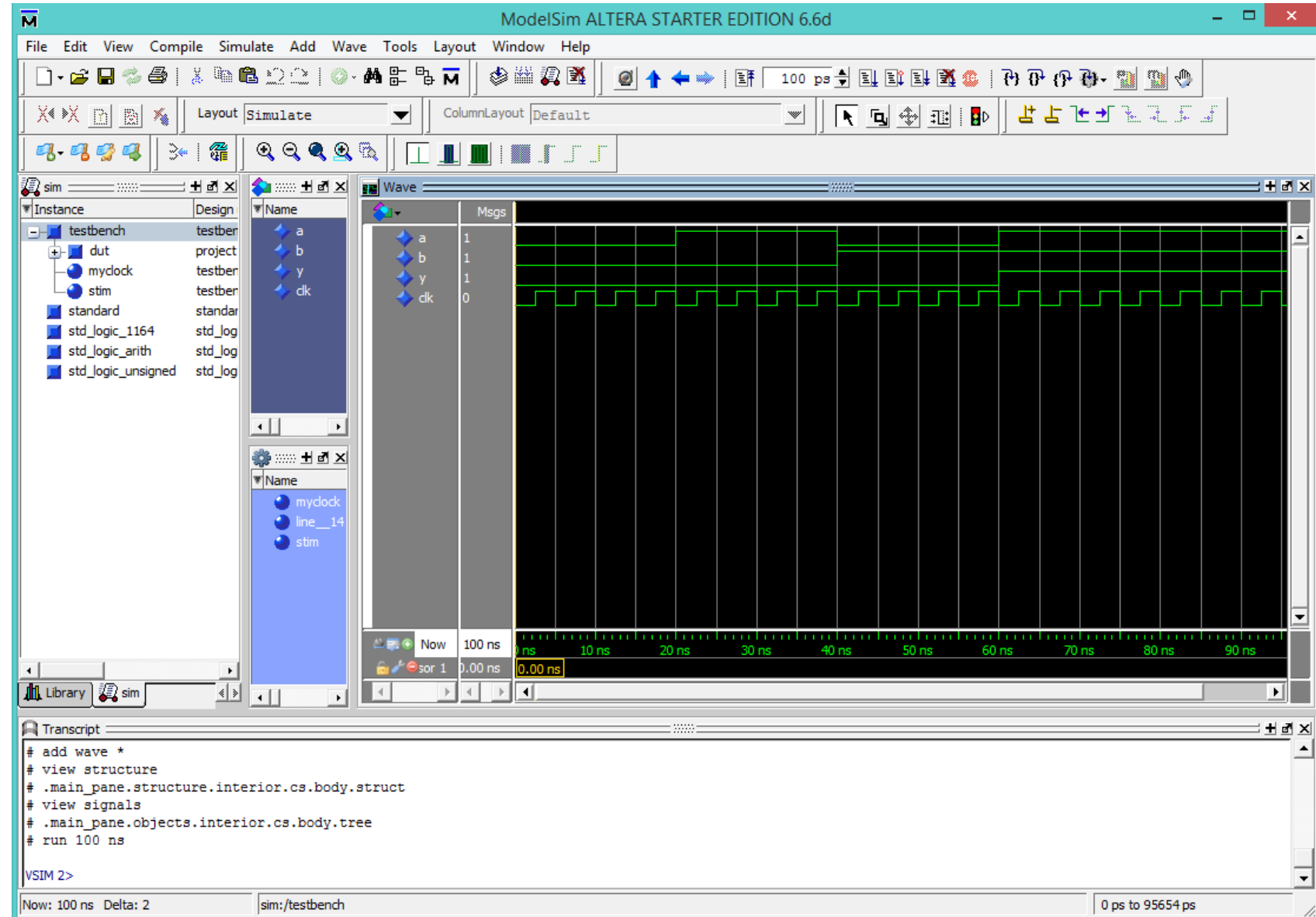
- Fill in the New Test Bench Settings

- Test bench name
 - Top level module in test bench
 - Activate Use test bench to perform VHDL timing simulation
 - Give the Design instance name in test bench
 - It is the label of the component
 - Choose the Simulation period
 - Add the testbench file
 - Click OK
 - Three times (three windows)



Quartus Prime

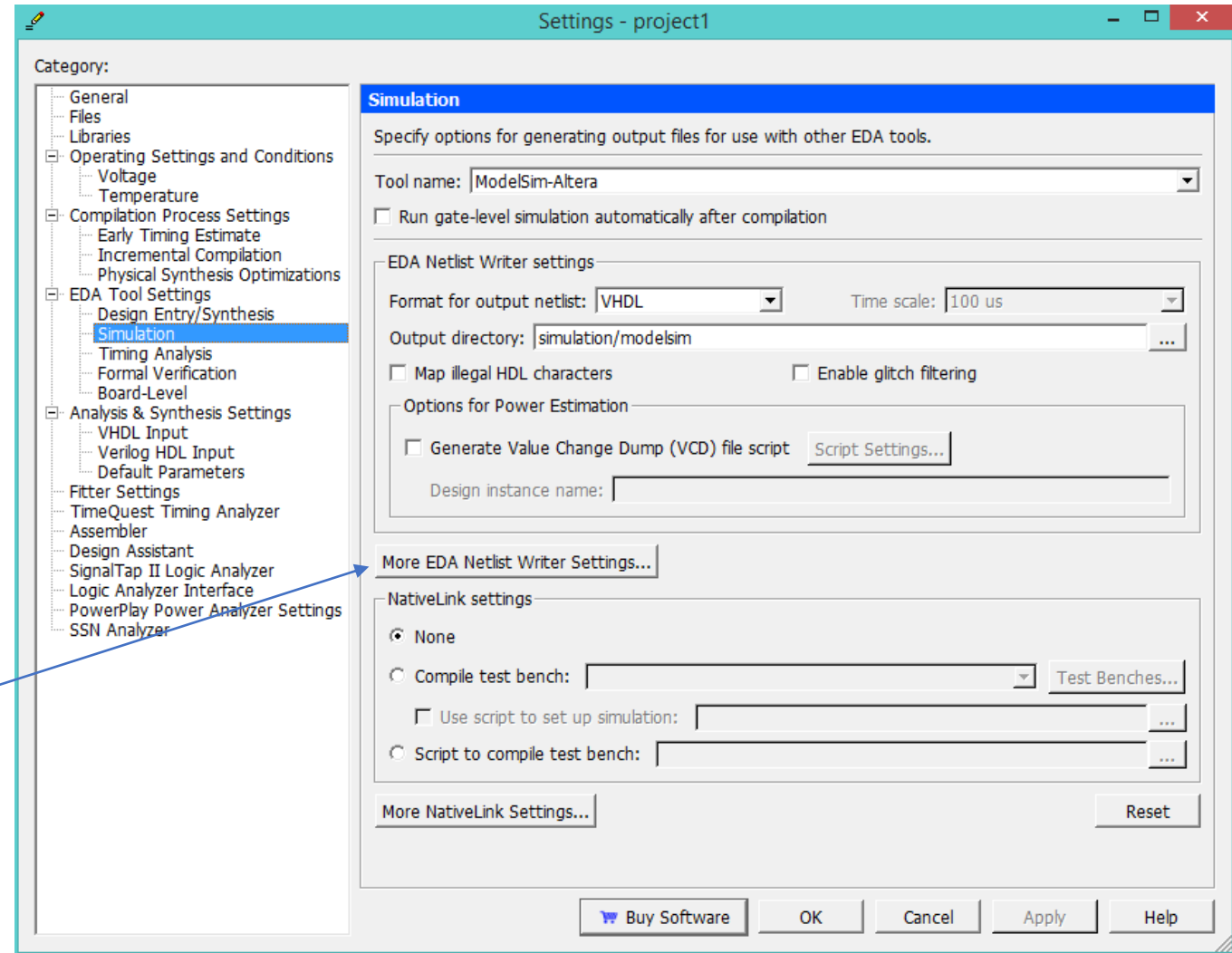
- Run Simulator
 - Under Tools menu
 - Choose Run Simulation Tool
 - Select RTL Simulation
 - If there are no errors, the simulation starts
 - You may need to reduce the zoom level in the wave window



Quartus Prime

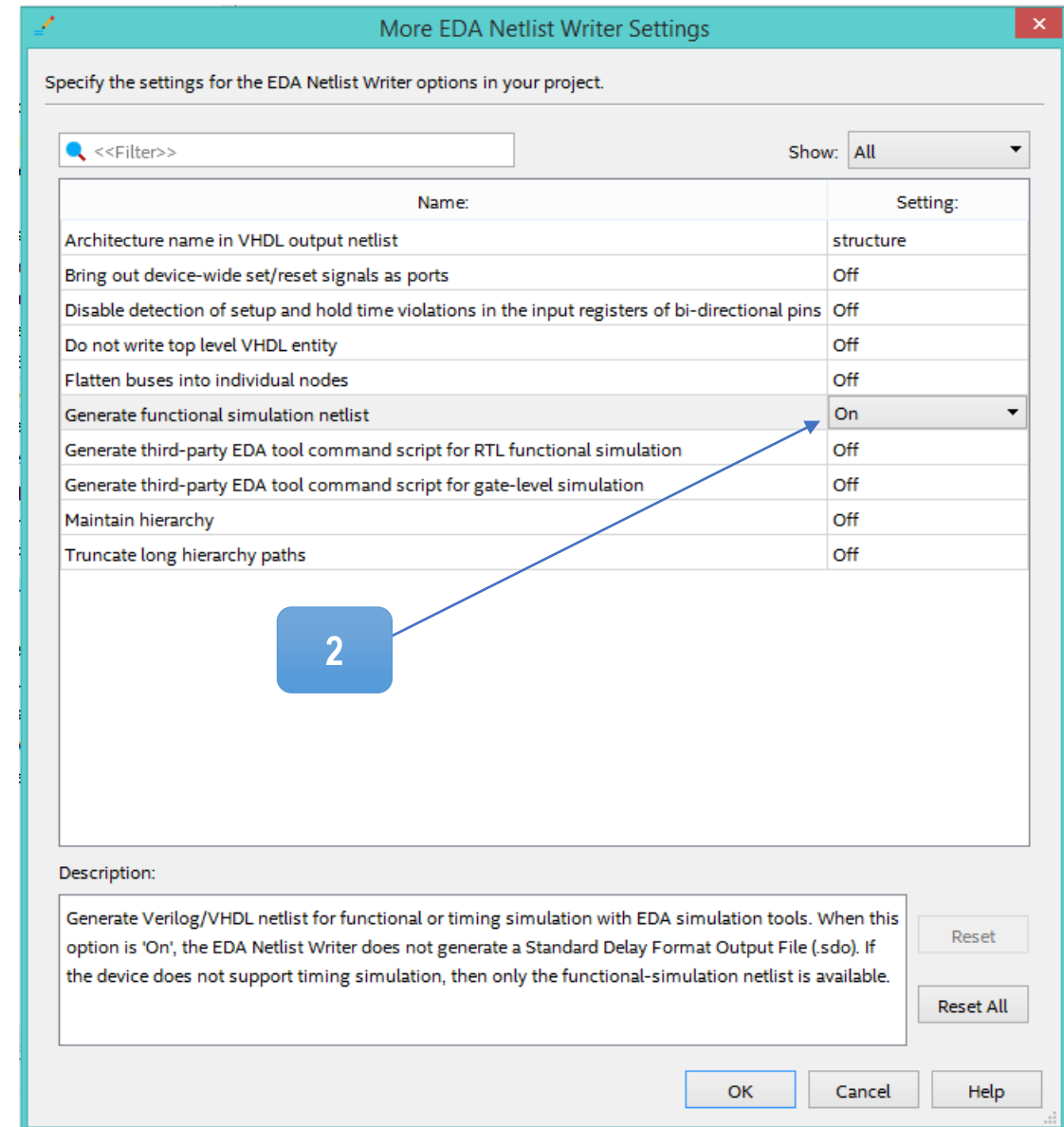
- Configure Simulator
 - Under Assignments menu
 - Choose Settings...
 - Select Simulation on the left pane
 - Click on More EDA Netlist Writer Settings

1



Quartus Prime

- Configure Simulator
 - Under Assignments menu
 - Choose Settings...
 - Select Simulation on the left pane
 - Click on More EDA Netlist Writer Settings
 - Enable Generate functional simulation netlist
 - Needed for gate level simulation
 - But Intel does not provide timing simulation anymore
 - Click OK twice (in two windows)



Quartus Prime

- Place & Route

- Under Processing menu

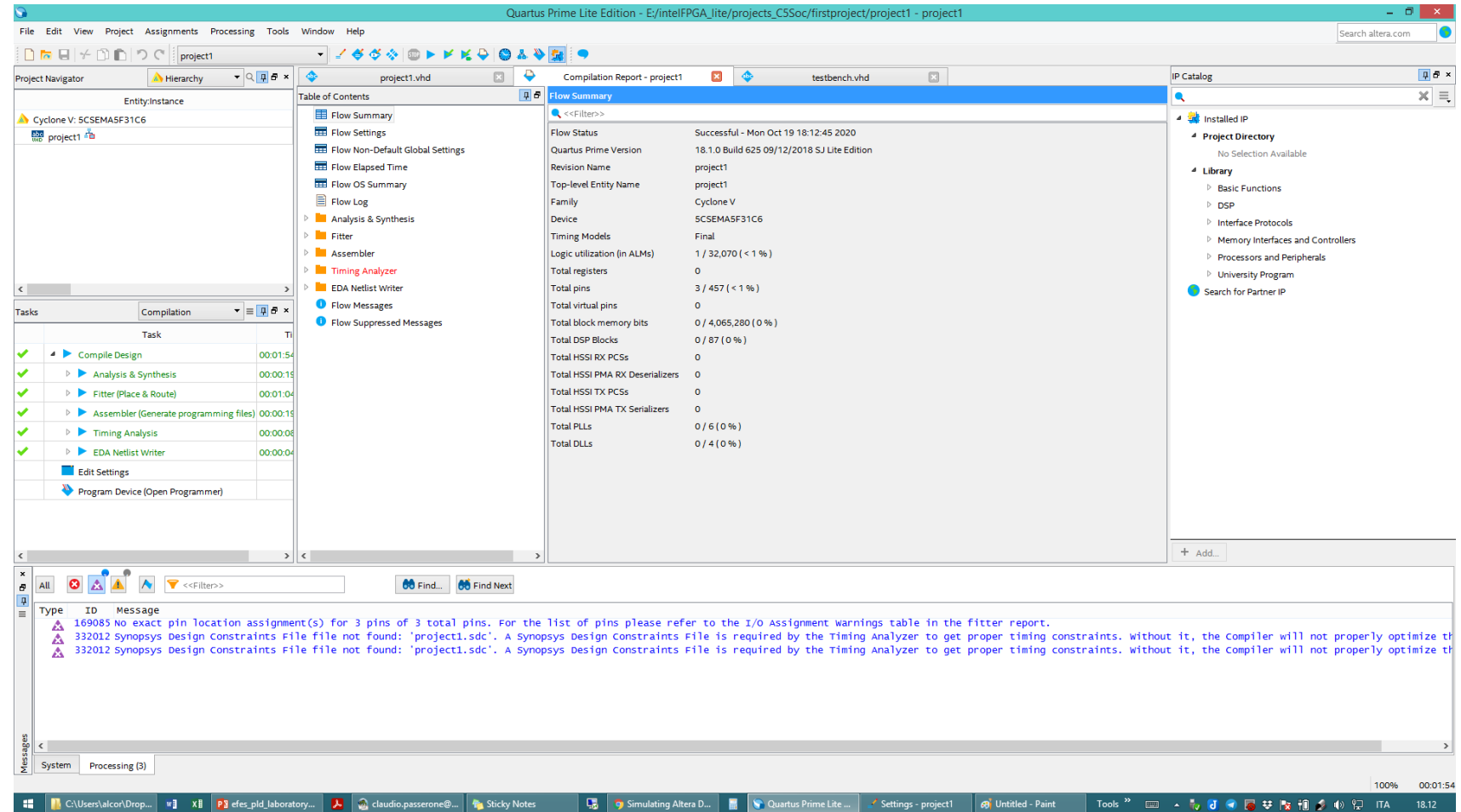
- Select Start Compilation

- Several steps are performed

- Analysis
 - Fitter
 - Assembler
 - Timing Analysis
 - EDA Netlist Writer

- There are some Critical Warnings

- Pins
 - Timing constraints



Quartus Prime

- Place & Route
 - Compilation report
 - It gives more information
 - Logic Elements
 - Registers
 - Pins
 - Memory
 - Expand the various tool reports

Table of Contents		Flow Summary	
Flow Summary		<<Filter>>	
Flow Settings		Flow Status	
Flow Non-Default Global Settings		Successful - Mon Oct 19 18:12:45 2020	
Flow Elapsed Time		Quartus Prime Version	
Flow OS Summary		18.1.0 Build 625 09/12/2018 SJ Lite Edition	
Flow Log		Revision Name	
▶ Analysis & Synthesis		project1	
▶ Fitter		Top-level Entity Name	
▶ Assembler		project1	
▶ Timing Analyzer		Family	
▶ EDA Netlist Writer		Cyclone V	
Flow Messages		Device	
Flow Suppressed Messages		5CSEMA5F31C6	
		Timing Models	
		Final	
		Logic utilization (in ALMs)	
		1 / 32,070 (< 1 %)	
		Total registers	
		0	
		Total pins	
		3 / 457 (< 1 %)	
		Total virtual pins	
		0	
		Total block memory bits	
		0 / 4,065,280 (0 %)	
		Total DSP Blocks	
		0 / 87 (0 %)	
		Total HSSI RX PCSs	
		0	
		Total HSSI PMA RX Deserializers	
		0	
		Total HSSI TX PCSs	
		0	
		Total HSSI PMA TX Serializers	
		0	
		Total PLLs	
		0 / 6 (0 %)	
		Total DLLs	
		0 / 4 (0 %)	

Quartus Prime

- Assign pins
 - Under Assignments menu
 - Choose Pin Planner
 - Assign pin locations
 - Check
 - I/O standard
 - Current Strength
 - If a pin does not show
 - Run compilation again
 - You don't need to save
 - But you need to recompile the entire design if any pin is changed

Pin Planner - E:\intelFPGA_lite\projects_C5Soc\firstproject\project1 - project1

File Edit View Processing Tools Window Help

Report not available

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment Analysis
 - Export Pin Assignments...
- Pin Finder...
- Highlight Pins

Top View - Wire Bond
Cyclone V - 5CSEMA5F31C6

Pin Legend

Symbol	Pin Type
○	User I/O
●	User assigned I...
●	Fitter assigned I...
○	Unbonded pad
●	Reserved pin
○	DIFF_n
○	DIFF_p
○	DIFF_n output
○	DIFF_p output
○	Hard processor ...
○	CLK_n
○	CLK_p
○	MSEL0
○	MSEL1
○	MSEL2
○	MSEL3
○	CONF_DONE
○	DCLK

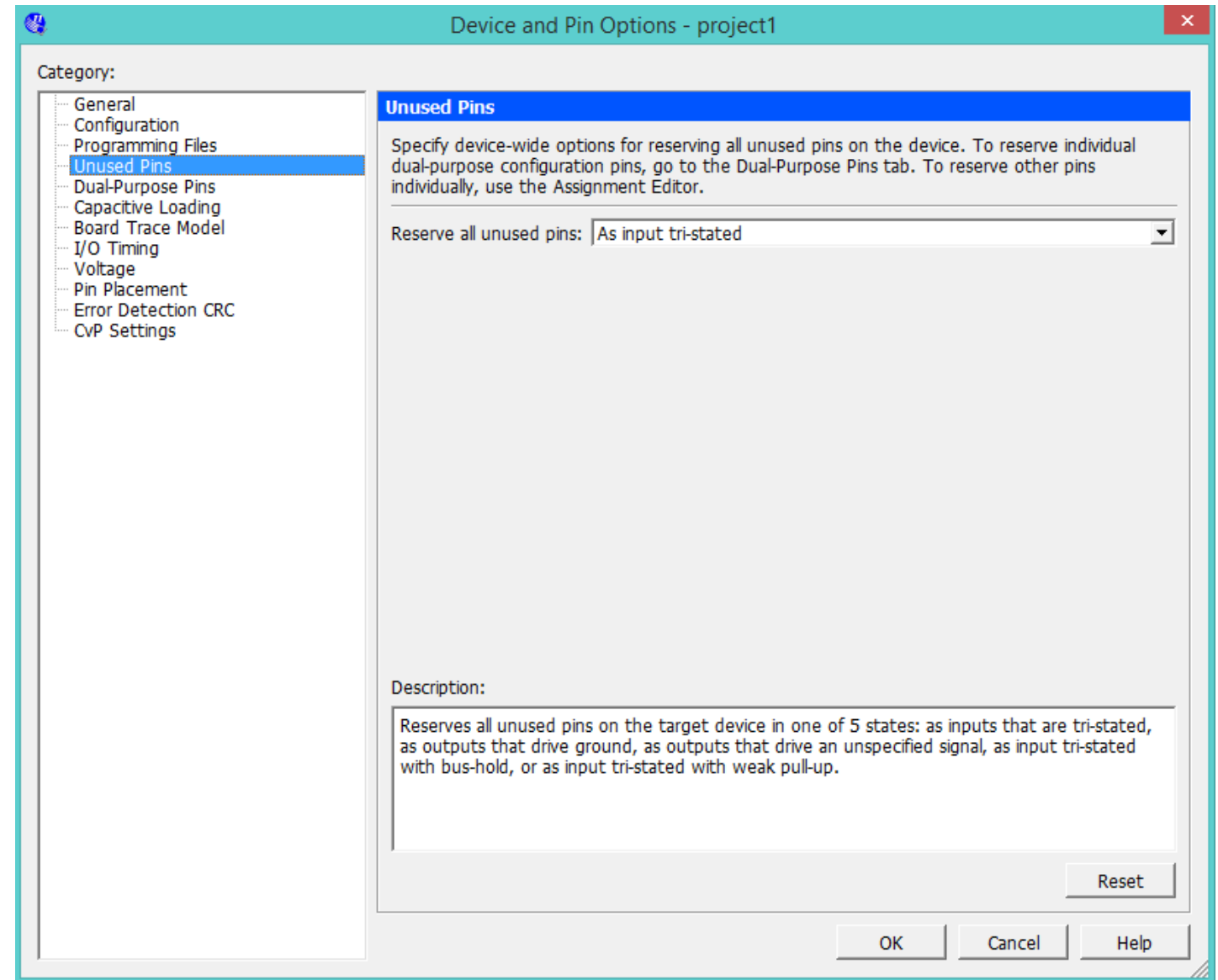
Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength
in a	Input	PIN_ab12	3A	B3A_N0	PIN_AH28	3.3-V LVTTTL		16mA (default)
in b	Input	PIN_ac12	3A	B3A_N0	PIN_AC25	3.3-V LVTTTL		16mA (default)
out y	Output	PIN_v16	4A	B4A_N0	PIN_AD25	3.3-V LVTTTL		16mA (default)
<<new node>>								

0% 00:00:00

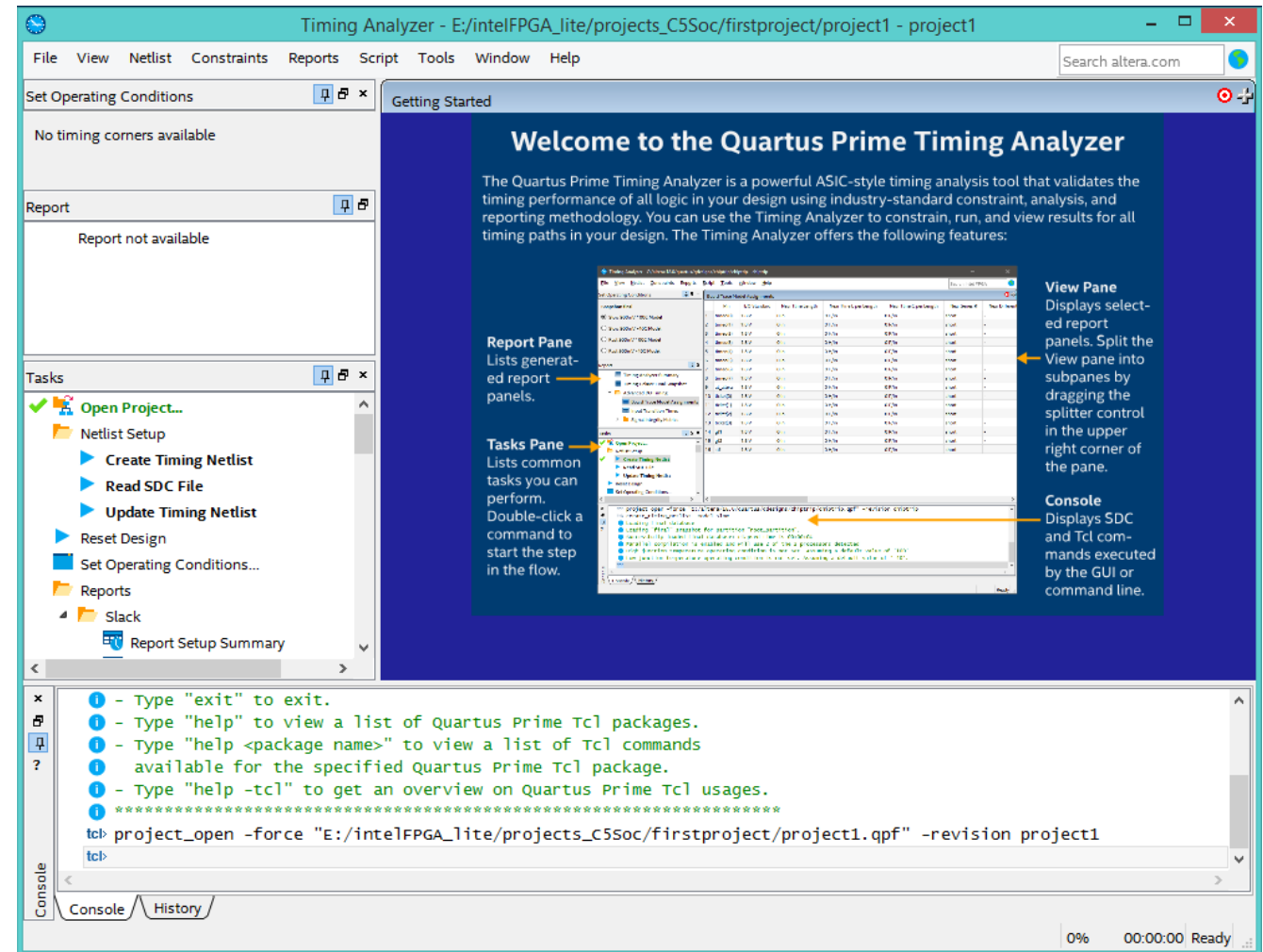
Quartus Prime

- Assign unused pins
 - Under Assignments menu
 - Choose Device...
 - Click Device and Pin Options...
 - Select Unused Pins in the left pane
 - Select As input tri-stated in the right pane



Quartus Prime

- Specify Timing Constraints
 - Under Tools menu
 - Choose Timing Analyzer
 - In the new window
 - Choose Netlist Setup → Create Timing Netlist
 - Create a new SDC file
 - Choose File → New SDC File
 - Or open an existing SDC File
 - The SDC file opens in the Quartus Prime window
 - Right click on the SDC file area and choose Insert Constraint
 - Or use the Constraints menu on the Timing Analyzer



Quartus Prime

- Specify Timing Constraints

- For a clock

- Choose Create Clock...

- Specify a name

- Give the clock period

- Specify rising and falling instants
 - Leave them blank for 50% duty cycle clock

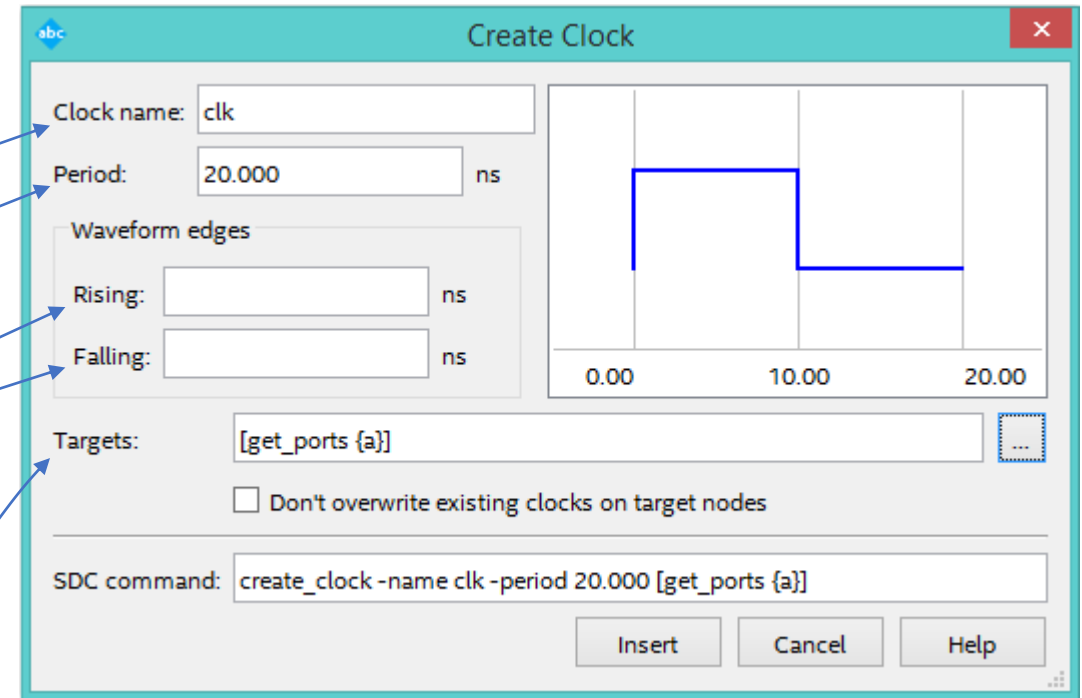
- Identify the target pin

- Click Insert

- If using the Constraints menu on the Timing Analyzer

- Click Run

- Then write the SDC file with Constraints → Write SDC File...

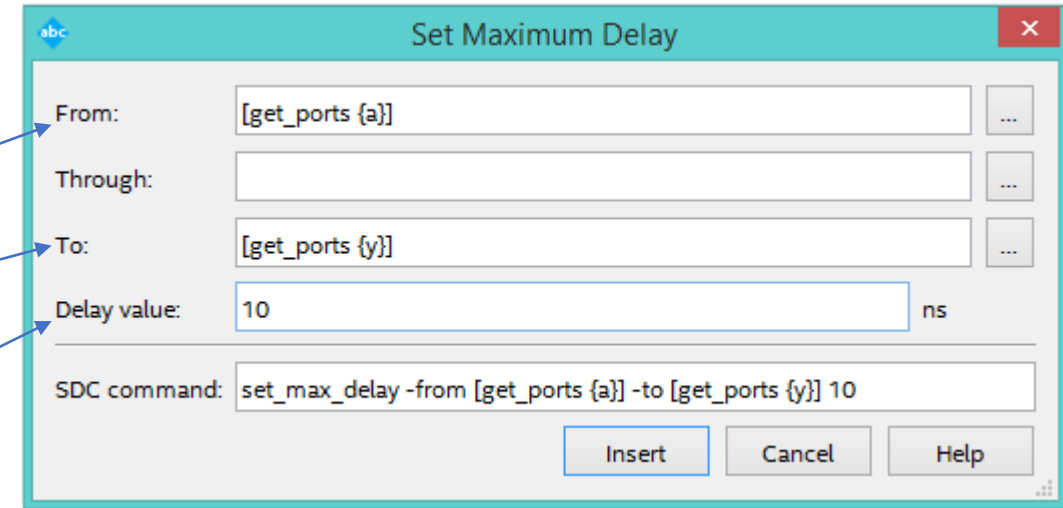


For combinational logic circuits, like the simple AND gate, you don't need to specify a constraint for the clock

- A clock does not exist!

Quartus Prime

- Specify Timing Constraints
 - For combinational logic
 - Choose Set Maximum Delay...
 - Specify the input port
 - Specify the output port
 - Specify the maximum propagation delay
 - Click Insert
 - If using the Constraints menu on the Timing Analyzer
 - Click Run
 - Then write the SDC file with Constraints → Write SDC File...



Quartus Prime

- Check Timing Analysis
 - In the Timing Analyzer
 - Check the Report Datasheet under the Reports
 - If timing constraints are not met, check also the Timing Analyzer in the Compilation Report in Quartus
 - For a sequential circuit, check the Fmax Summary
 - Changing the pin assignments affects performance
 - Changing the timing constraints affects performance
 - When timing constraints are not met check the Timing Closure Recommendations
 - Slack is the error

The screenshot shows the Quartus Prime interface with three panels. The 'Set Operating Conditions' panel has four radio buttons: 'Slow 1100mV 85C Model' (selected), 'Slow 1100mV 0C Model', 'Fast 1100mV 85C Model', and 'Fast 1100mV 0C Model'. The 'Report' panel shows a tree view with 'Datasheet Report' expanded, containing 'Slow 1100mV 85C Model', 'Propagation Delay', and 'Minimum Propagation Delay'. The 'Tasks' panel shows a list of tasks with 'Update Timing Netlist' checked. A blue arrow points from the 'Report Datasheet' text in the list to the 'Report Datasheet' task in the Tasks panel.

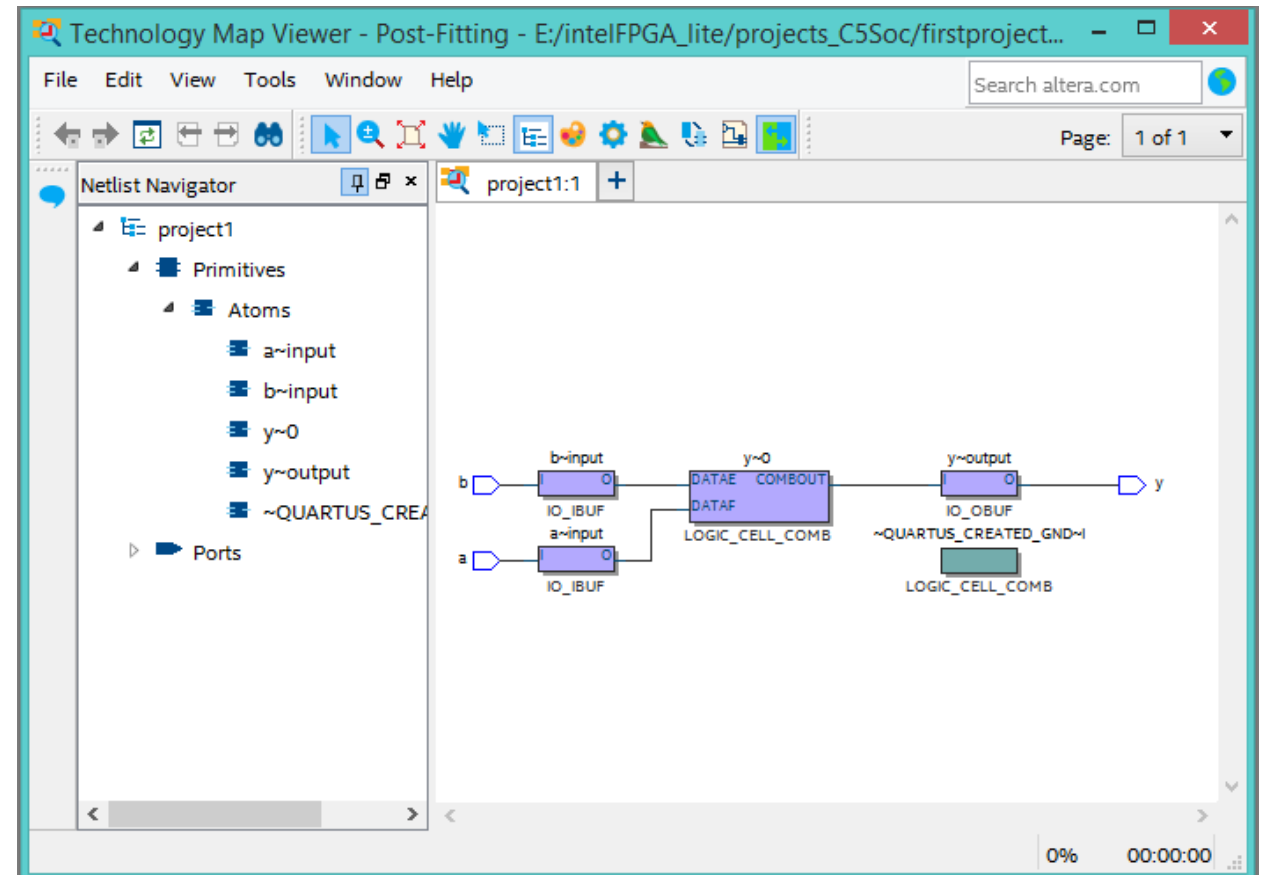
	Input Port	Output Port	RR	RF	FR	FF
1	a	y	6.729			7.325
2	b	y	6.851			7.426

The screenshot shows the Quartus Prime interface with two panels. The 'Table of Contents' panel shows a tree view with 'Timing Analyzer' expanded, containing 'Summary', 'Parallel Compilation', 'SDC File List', 'Clocks', 'Slow 1100mV 85C Model', 'Fmax Summary', and 'Timing Closure Recommendations'. A blue arrow points from the 'Timing Closure Recommendations' text in the list to the 'Timing Closure Recommendations' panel. The 'Timing Closure Recommendations' panel has a blue header and a 'Summary [hide details]' section. Below it, a text block states: 'This design contains failing setup paths with a worst-case slack of -0.426 ns. Run setup timing. For recommendations for any particular path, click the appropriate link.' Below this is a 'Top Failing Paths [hide details]' section with a table.

	Slack	From	To	Recommendations
1	-0.426	b	y	Report recommendations for this path
2	-0.325	a	y	Report recommendations for this path

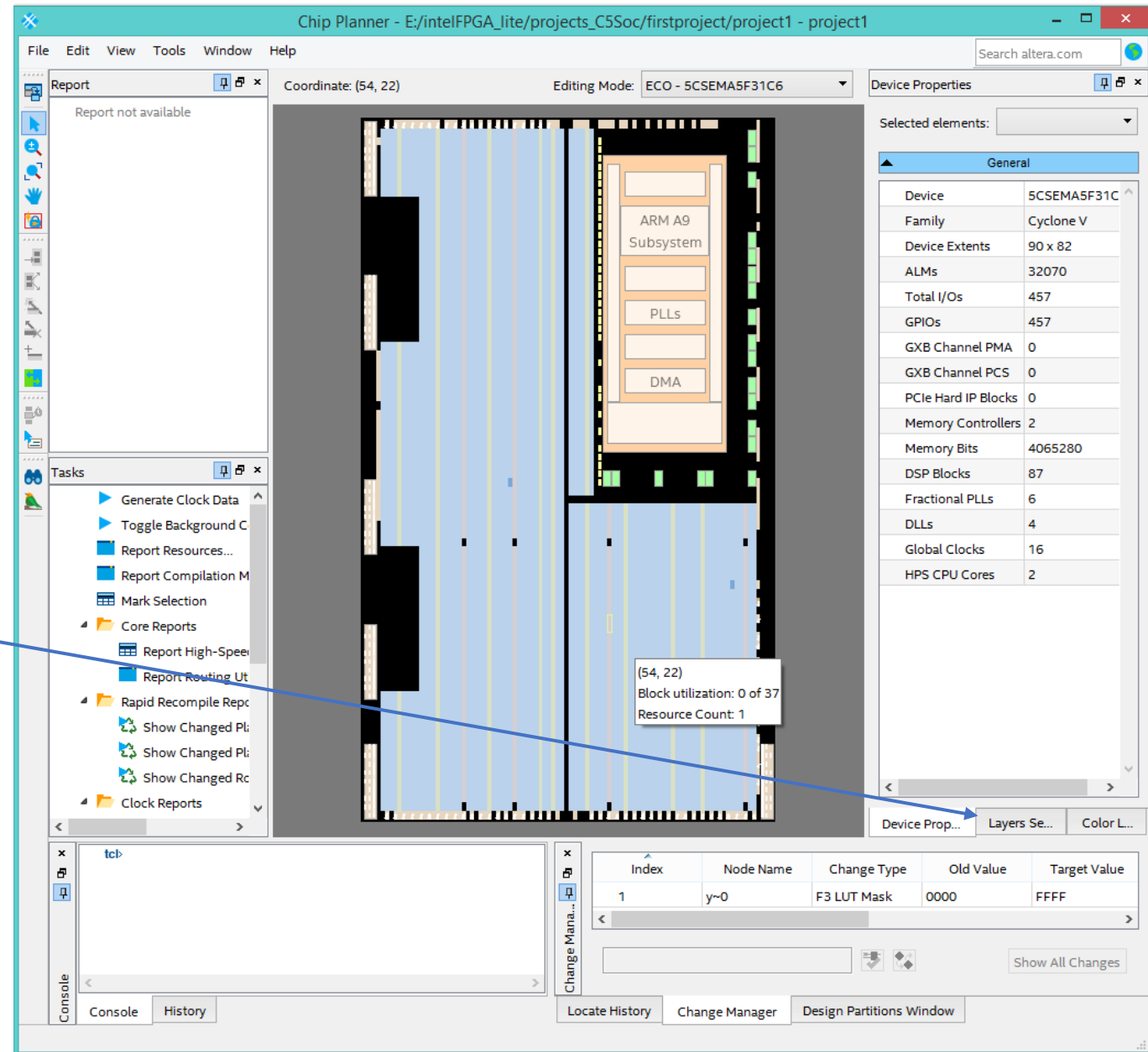
Quartus Prime

- Place & Route
 - Under Tools menu
 - Under Netlist Viewers
 - Technology Map Viewer (Post-Mapping)
 - Technology Map Viewer (Post-Fitting)
 - Right click on an object
 - Choose Locate Node
 - Can locate the node in various tools
 - Pin Planner
 - Chip Planner
 - Design File
 - ...



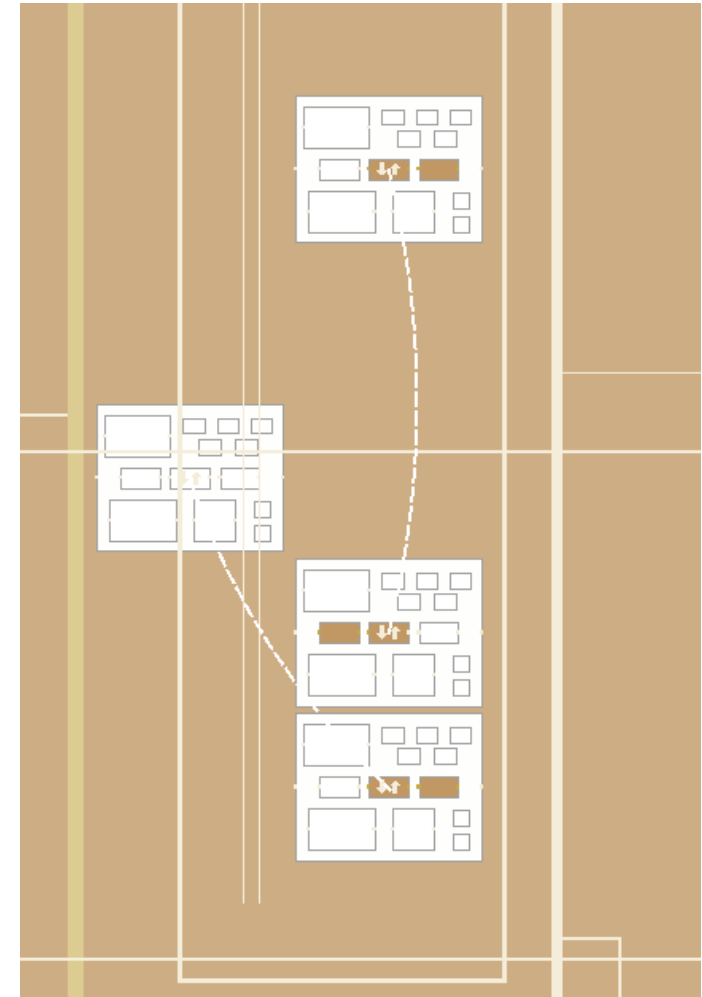
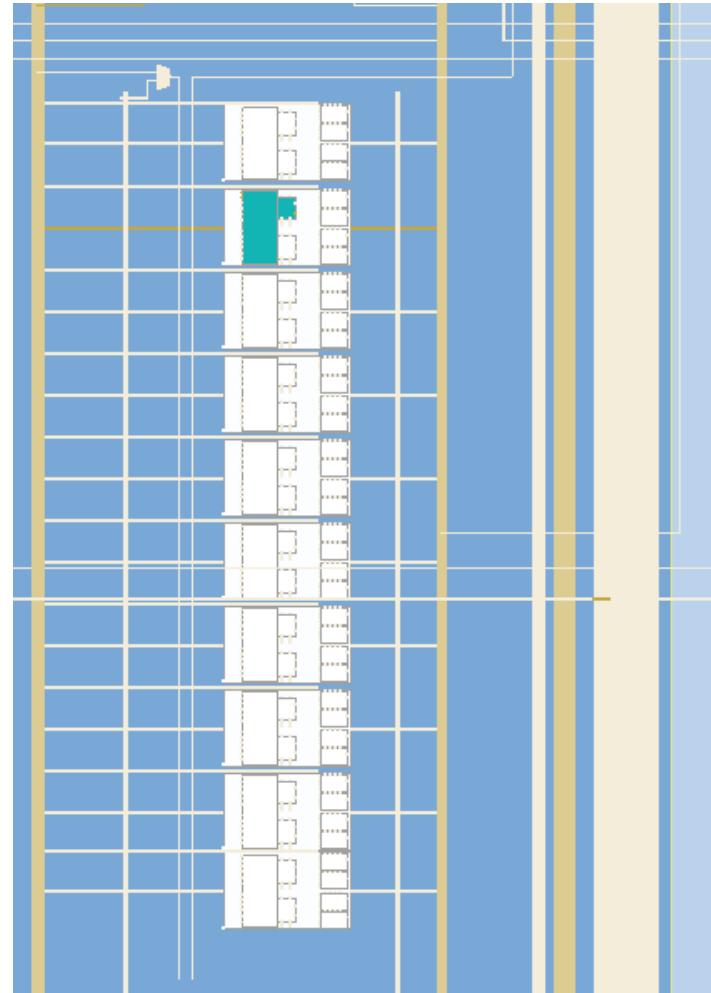
Quartus Prime

- Floorplan
 - Under Tools menu
 - Choose Chip Planner
 - You can zoom in different areas of the chip
 - You can select different resources to show
 - Under Layers Settings
 - Logic Element utilization
 - Routing utilization
 - Select additional details



Quartus Prime

- Floorplan
 - Zoom on a Logic Array Block and Input/Output Block
 - The second Logic Element is used
 - Three I/O Elements are used
 - Additional routing details enabled



Quartus Prime

- Floorplan
 - Double click on a Logic Element
 - See how it is used
 - The LUT content is in the column on the right
 - Input and Output ports are listed at the bottom
 - Blocks used are highlighted

The screenshot shows the 'Resource Property Editor' window in Quartus Prime, titled 'E:/intelFPGA_lite/projects_C5Soc/firstproject/project1 - project1'. The window displays the logic resource configuration for a specific logic element, identified as 'LABCELL_X83_Y27_N6'.

The 'Node Name' table shows the selected node:

Node Name	Location
<input checked="" type="checkbox"/> project1 y~0 LABCELL_X83_Y27_N6	

The 'Logic Resource(s)' section shows a logic diagram with various logic elements and connections. The selected logic element is highlighted in blue.

The 'Properties/Modes' table shows the configuration for the selected logic element:

Properties/Modes	Values
F0 LUT Mask	FFFF
F1 LUT Mask	0000
F2 LUT Mask	0000
F3 LUT Mask	0000
Full Node Name	project1 y~0
Location String	LABCELL_X83_Y27
Latch Type	none
F0 LUT Equation	vcc
F1 LUT Equation	gnd
F2 LUT Equation	gnd
F3 LUT Equation	gnd
Combout Equation	(E & (F))
Sumout Equation	N/A
Carryout Equation	N/A
Shareout Equation	N/A

The 'Input Port Name' table shows the input ports and their signal names:

Input Port Name	Signal Name	Inverted
Top Combinational		
!DATAC	<Disconnected>	False
!DATAE	project1 b~input	False
!DATAF	project1 a~input	False

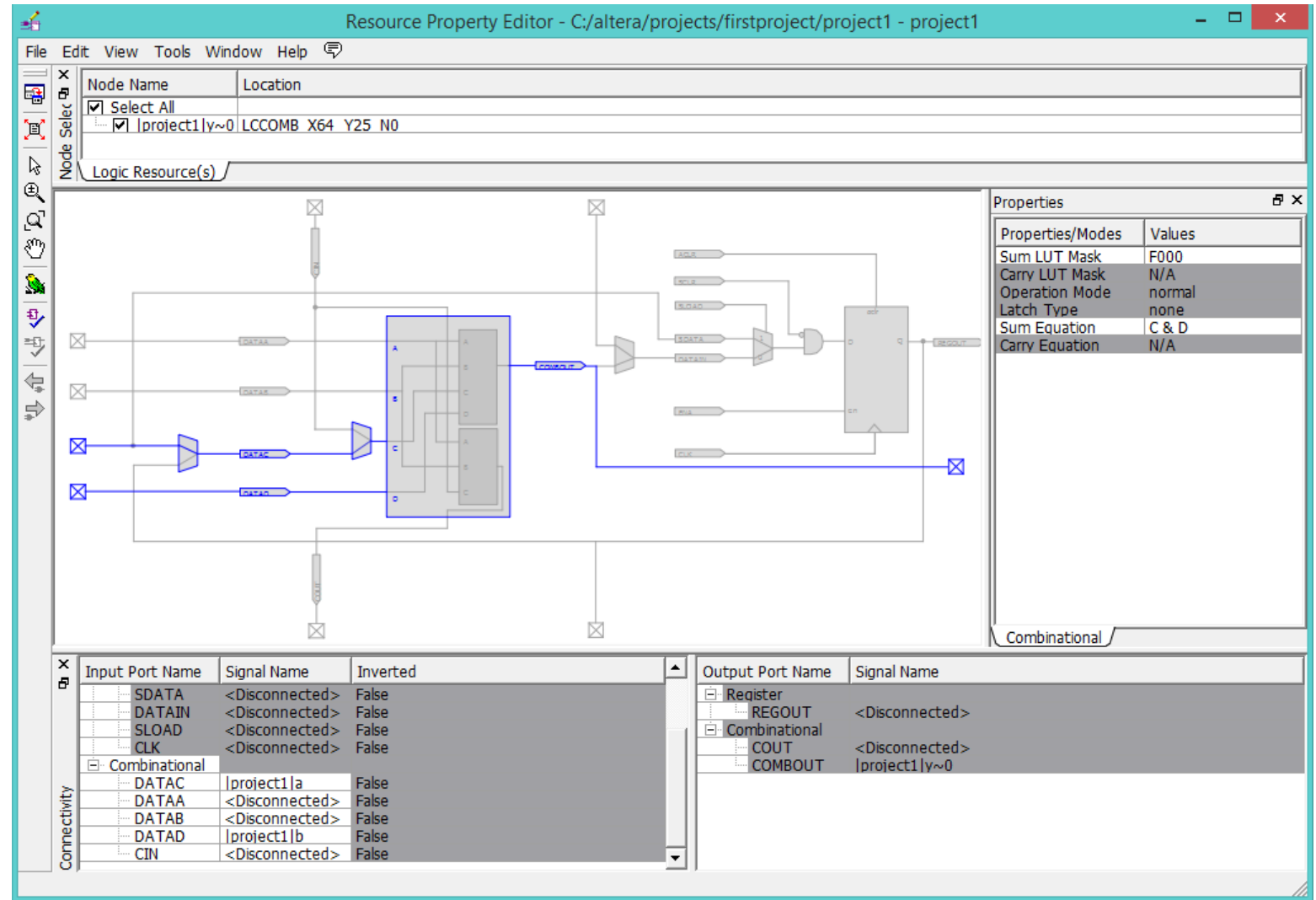
The 'Output Port Name' table shows the output ports and their signal names:

Output Port Name	Signal Name
Top Combinational	
SUM_OUT	<Disconnected>
COUT	<Disconnected>
SHAREOUT	<Disconnected>

Quartus II

- Floorplan
 - Double click on a Logic Element
 - With a Cyclone II FPGA
 - LE similar to a Cyclone 10 LP
 - See how it is used
 - The picture on the right is from Quartus 11.1sp1
 - With Quartus 18 it looks slightly different

This is an older version of Quartus using a *vintage* Cyclone II FPGA, which has a different logic element compared to the Cyclone V



Quartus Prime

- Floorplan

- Double click on an Input/Output Element
 - See how it is used
 - Input
 - Output
 - The picture on the right is for input *b*
 - It is an output of the I/O Element

The screenshot shows the 'Resource Property Editor' window for a project named 'project1'. The window is divided into several sections:

- Node Name / Location:** A table with one entry:

Node Name	Location
project1 b~input	IOIBUF_X89_Y25_N55
- I/O(s):** A large diagram showing the internal structure of the I/O element, including various logic blocks and connections.
- Properties/Modes:** A table listing various properties and their values:

Properties/Modes	Values
I/O Mode	input
DDIO Mode	none
Weak Pull Up	off
I/O Standard	3.3-V LVTTL
D1 Delay Chain	N/A
D3 Delay Chain 0	N/A
D3 Delay Chain 1	0
D4 Delay Chain	N/A
D5 Delay Chain	N/A
D5 OCT Delay Chain	N/A
D5 OE Delay Chain	N/A
T11_0 Delay Chain	0
T11_1 Delay Chain	0
- Pad / Input Buffer:** Two tables at the bottom showing port configurations.

Input Port Name	Signal Name	Inverted
Pad		
PADIN	<Disconnected>	False
Output Buffer		
IN	<Disconnected>	False

Output Port Name	Signal Name
Pad	
PADOUT	project1 b
Output Buffer	
OUTN	<Disconnected>

A blue arrow points from the text 'It is an output of the I/O Element' to the 'PADOUT' entry in the 'Output Port Name' table, which is connected to the signal 'project1|b'.

Quartus Prime

- Floorplan

- Double click on an Input/Output Element
 - See how it is used
 - Input
 - Output
 - The picture on the right is for output y
 - It is an input of the I/O Element

The screenshot shows the 'Resource Property Editor' window in Quartus Prime. The title bar indicates the project path: 'E:/intelFPGA_lite/projects_C5Soc/firstproject/project1 - project1'. The window has a menu bar (File, Edit, View, Tools, Window, Help) and a search bar (Search altera.com). The main area is divided into several sections:

- Node Name / Location:** A table showing the selected node:

Node Name	Location
<input checked="" type="checkbox"/> project1 y~output	IOBUF_X89_Y25_N5
- I/O(s):** A large diagram showing the internal structure of the I/O element, including various logic blocks and signal paths. A blue line points from the 'It is an input of the I/O Element' text to a specific input port in this diagram.
- Properties/Modes:** A table listing various properties and their values:

Properties/Modes	Values
I/O Mode	output
DDIO Mode	none
Weak Pull Up	off
I/O Standard	3.3-V LVTTL
Current Strength	16mA
D1 Delay Chain	N/A
D3 Delay Chain 0	N/A
D3 Delay Chain 1	N/A
D4 Delay Chain	N/A
D5 Delay Chain	0
D5 OCT Delay Chain	N/A
D5 OE Delay Chain	31
T11_0 Delay Chain	0
T11_1 Delay Chain	0
- Input Port Name / Signal Name / Invert:** A table showing the input configuration:

Input Port Name	Signal Name	Invert
Pad		
PADIN	project1 y~output	False
Output Buffer		
- Output Port Name / Signal Name:** A table showing the output configuration:

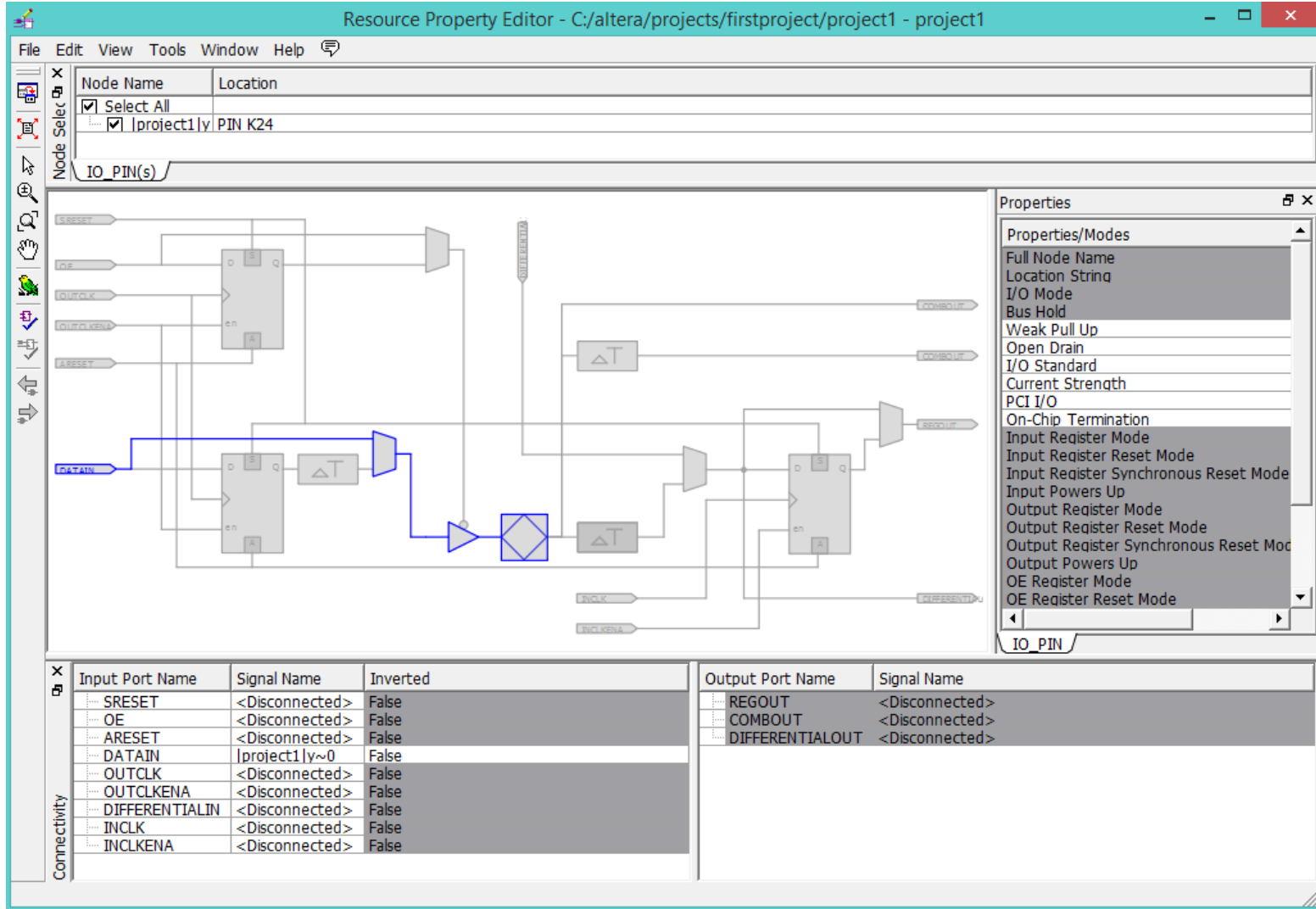
Output Port Name	Signal Name
Pad	
PADOUT	project1 y
Output Buffer	
OUTN	<Disconnected>

Quartus II

- Floorplan

- Double click on an Input/Output Element
 - With a Cyclone II FPGA
 - IOE similar to a Cyclone 10 LP
 - See how it is used
 - The picture on the right is from Quartus 11.1sp1
 - With Quartus 18 it looks slightly different

This is an older version of Quartus using a *vintage* Cyclone II FPGA, which has a different logic element compared to the Cyclone V

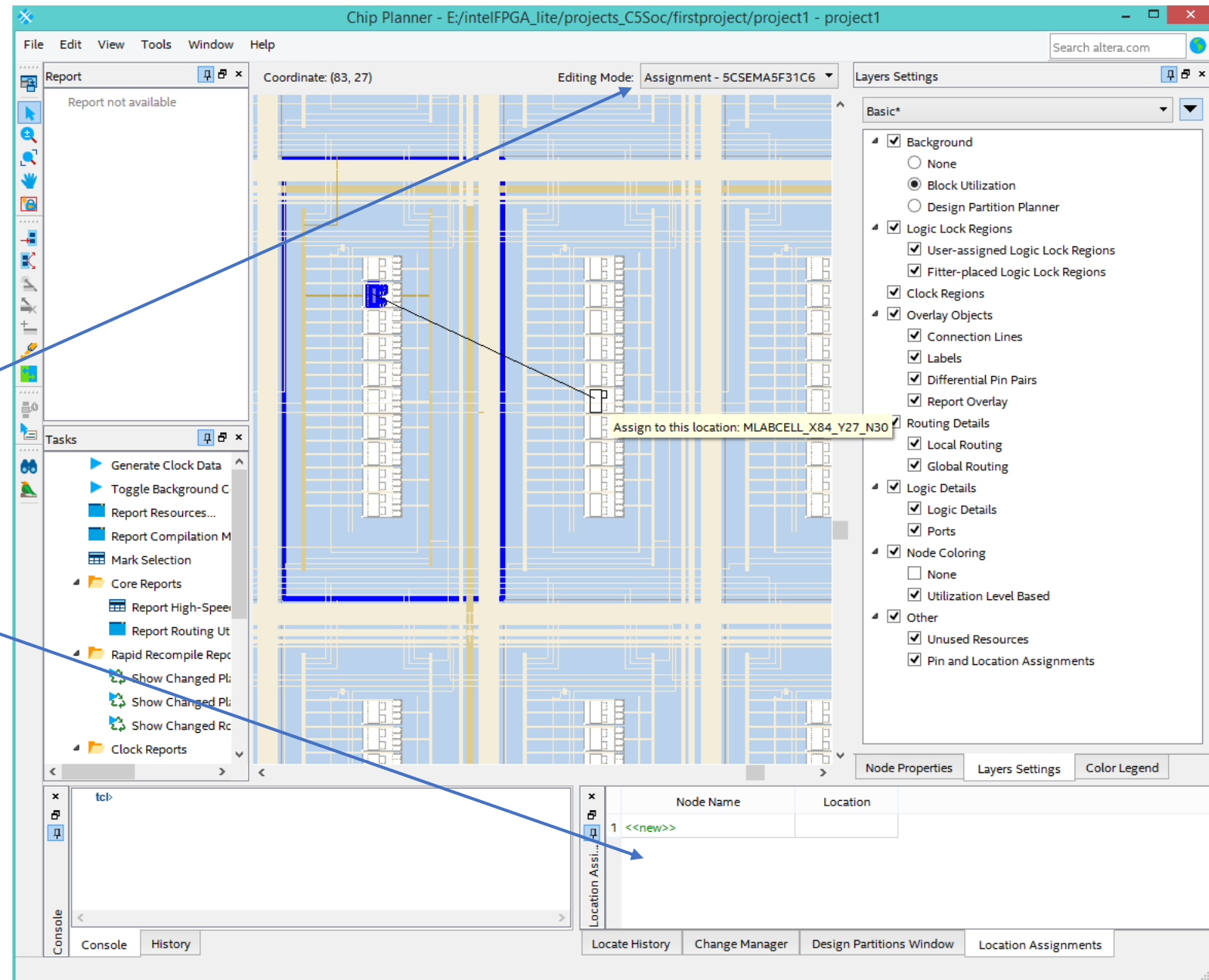


Quartus Prime

- Floorplan

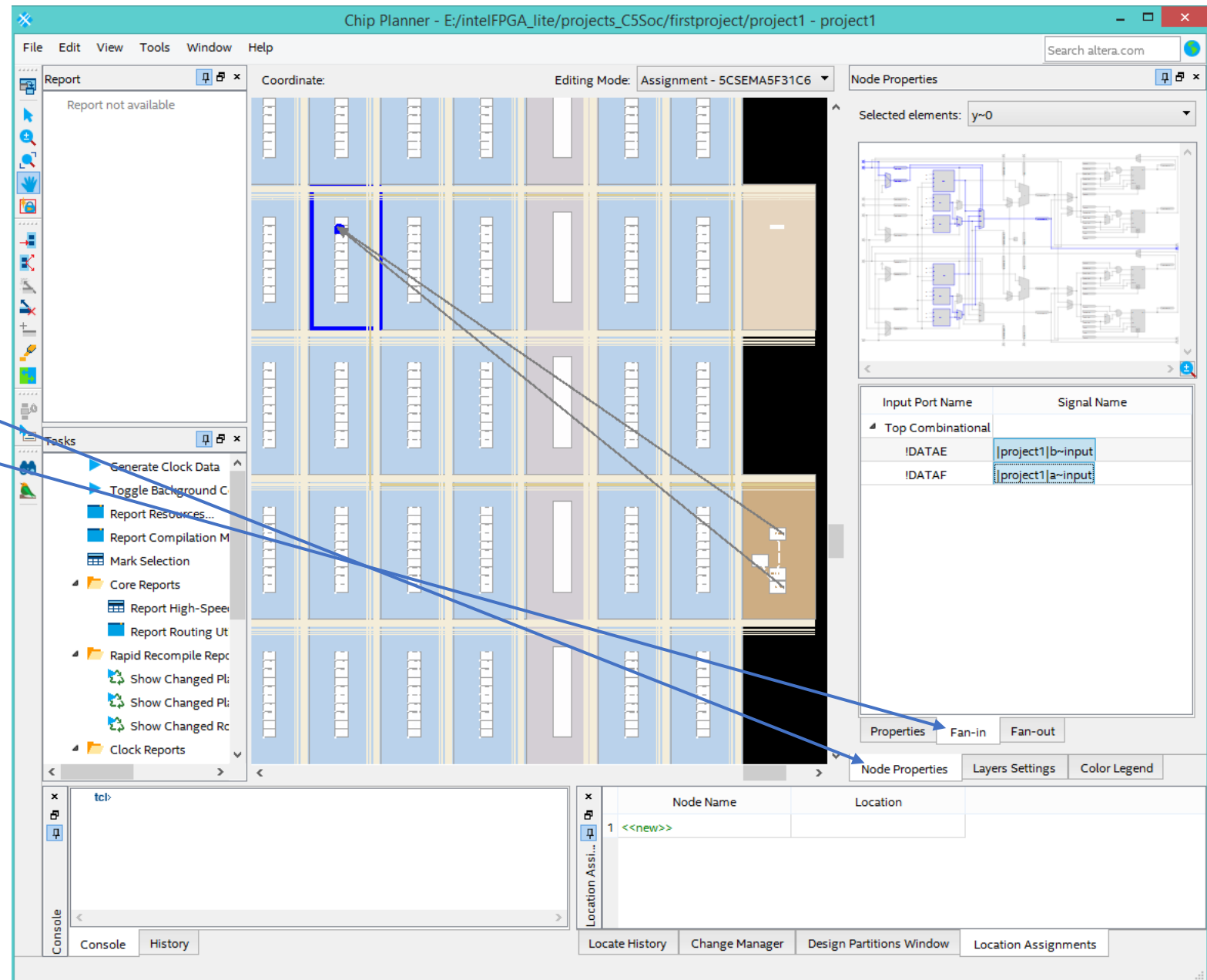
- You can drag objects to new locations

- Set the Editing Mode to Assignment
- Drag the object
- The new assignment will appear at the bottom
- If you open the Assignment Editor in Quartus under the Assignment menu you see the new location
- Recompile to get the new floorplan



Quartus Prime

- Floorplan
 - You can highlight connections
 - Select a Logic Element
 - Click on Node Properties
 - Click on Fan-in or Fan-out
 - Click on signal names

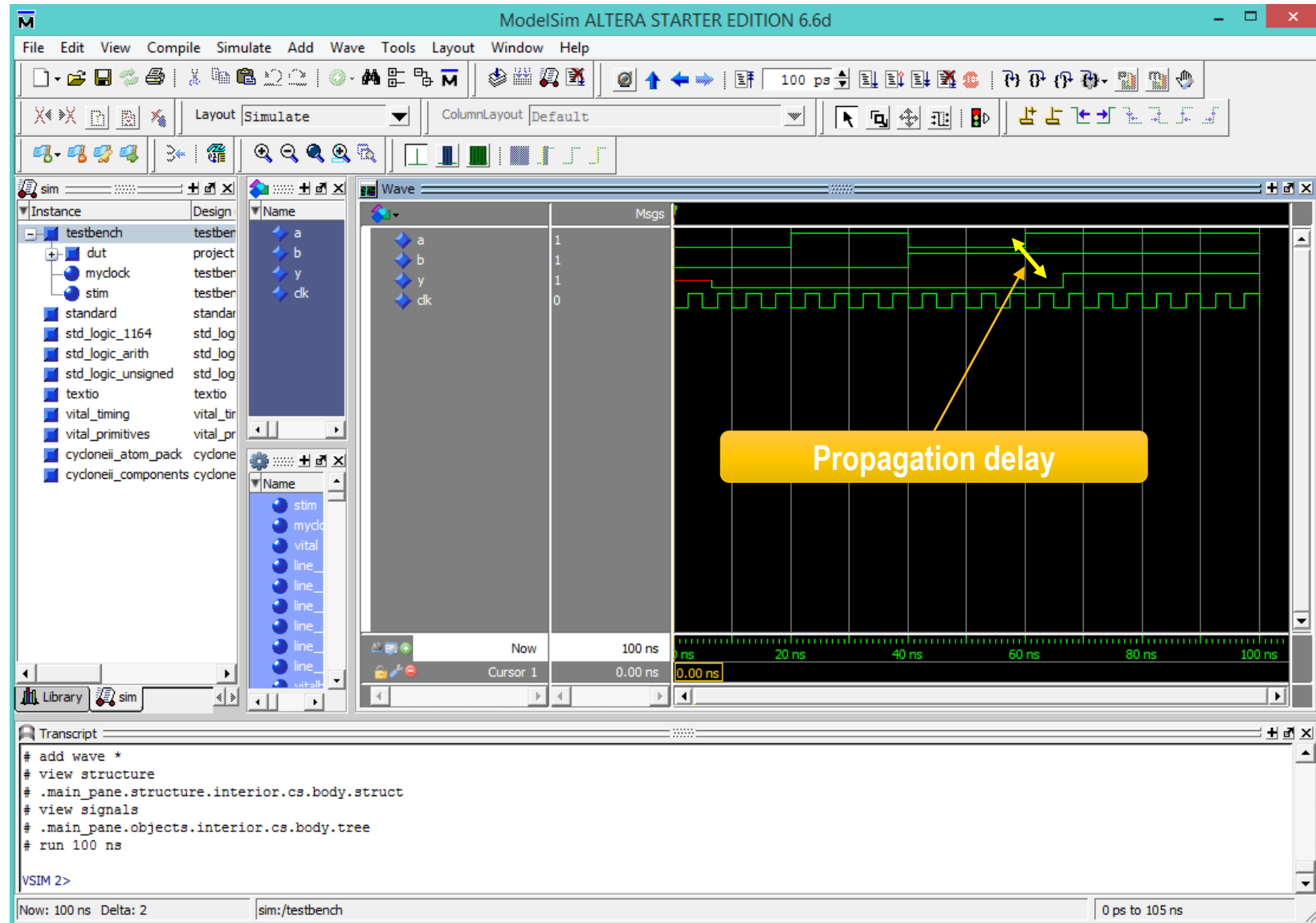


Quartus Prime

- Floorplan
 - Every time you make a change
 - Recompile your project
 - Check timing analysis and datasheet reports
 - Timing strongly depends on
 - Technology Mapping and Placing
 - How to map a function on the available resources
 - Routing
 - Length of the interconnections
 - If you use ECO (Engineering Change Orders) mode instead of Assignment mode
 - The full compilation is not necessary
 - But changes are not reflected in many other steps of the design flow
 - If you recompile, chances are that your changes will be reverted

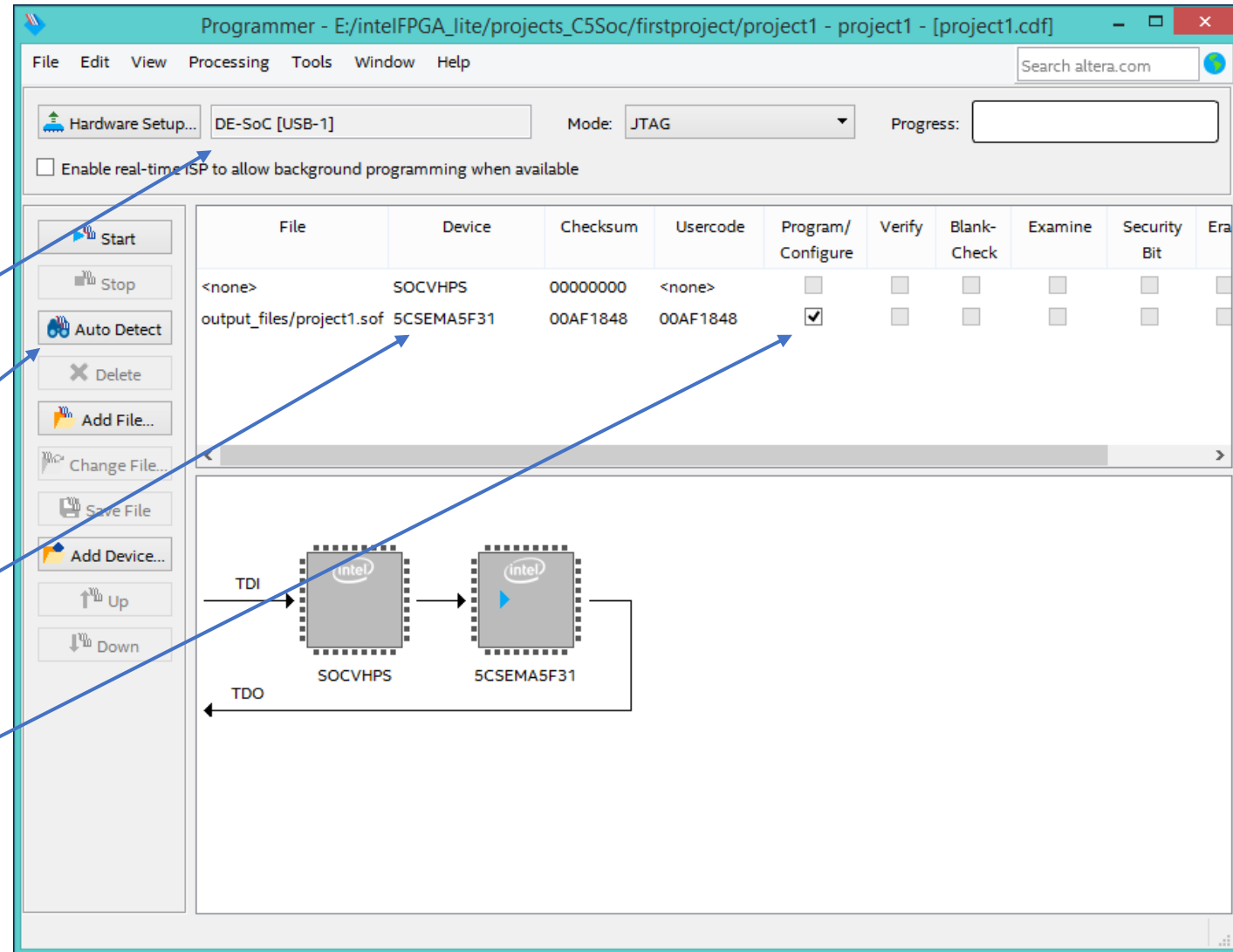
Quartus II

- Run Simulator
 - Under Tools menu
 - Choose Run EDA Simulation Tool
 - Select EDA Gate Level Simulation...
 - Choose the Slow Model and click Run
 - If there are no errors, the simulation starts
 - You now see all estimated delays
 - This is on Quartus 11 with the Cyclone II FPGA
 - No timing model for Cyclone V and 10 LP



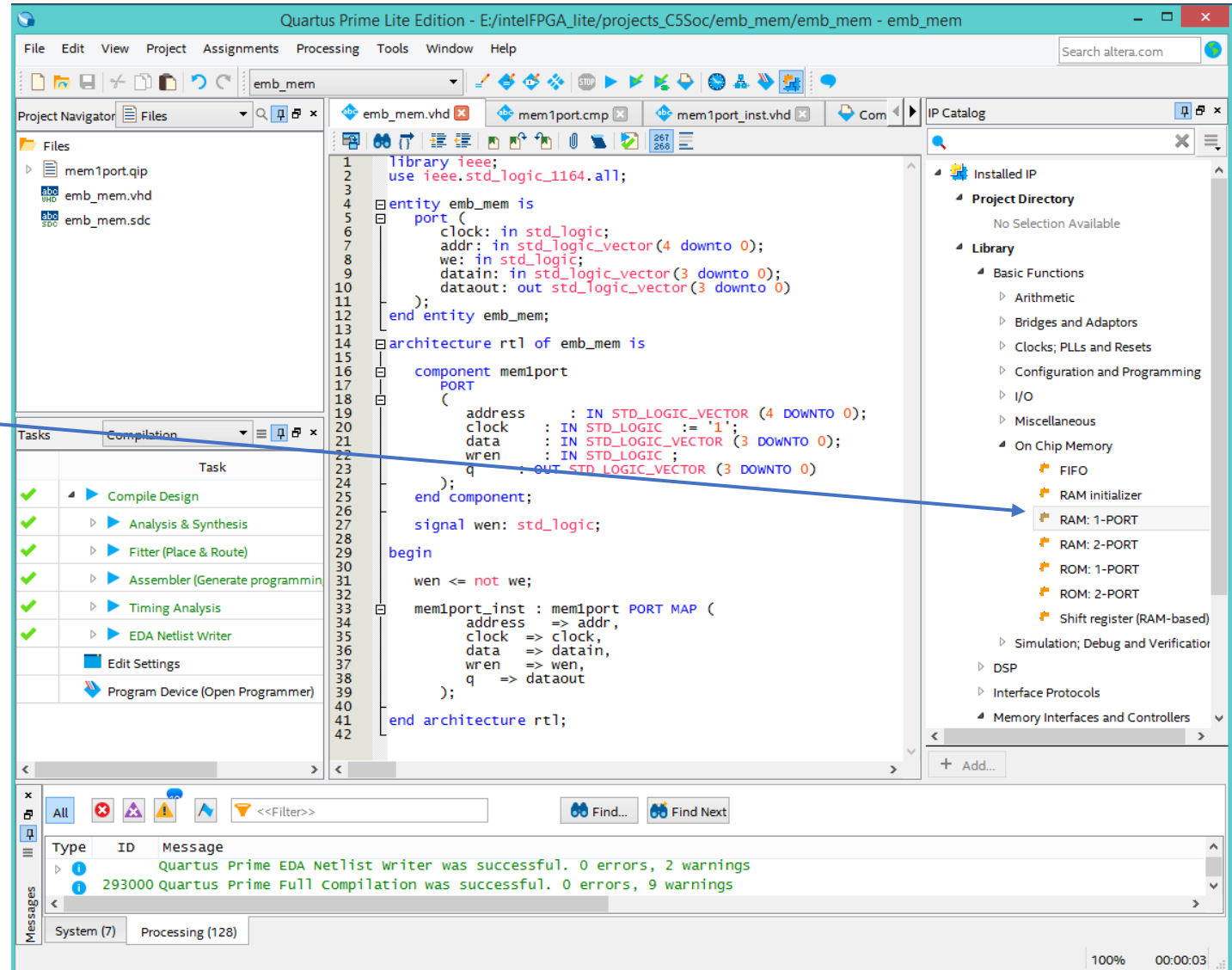
Quartus Prime

- Run Programmer
 - Under Tools menu
 - Choose Programmer
 - Check the Hardware Setup
 - It should be DE-SoC
 - Click Auto Detect and select the 5CSEMA5 device and then overwrite any existing settings
 - Right click on the row for 5CSEMA5 and choose Change File
 - Look for the .sof programmer file under output_files in the project directory
 - Select Program/Configure
 - Click Start
 - ENJOY!



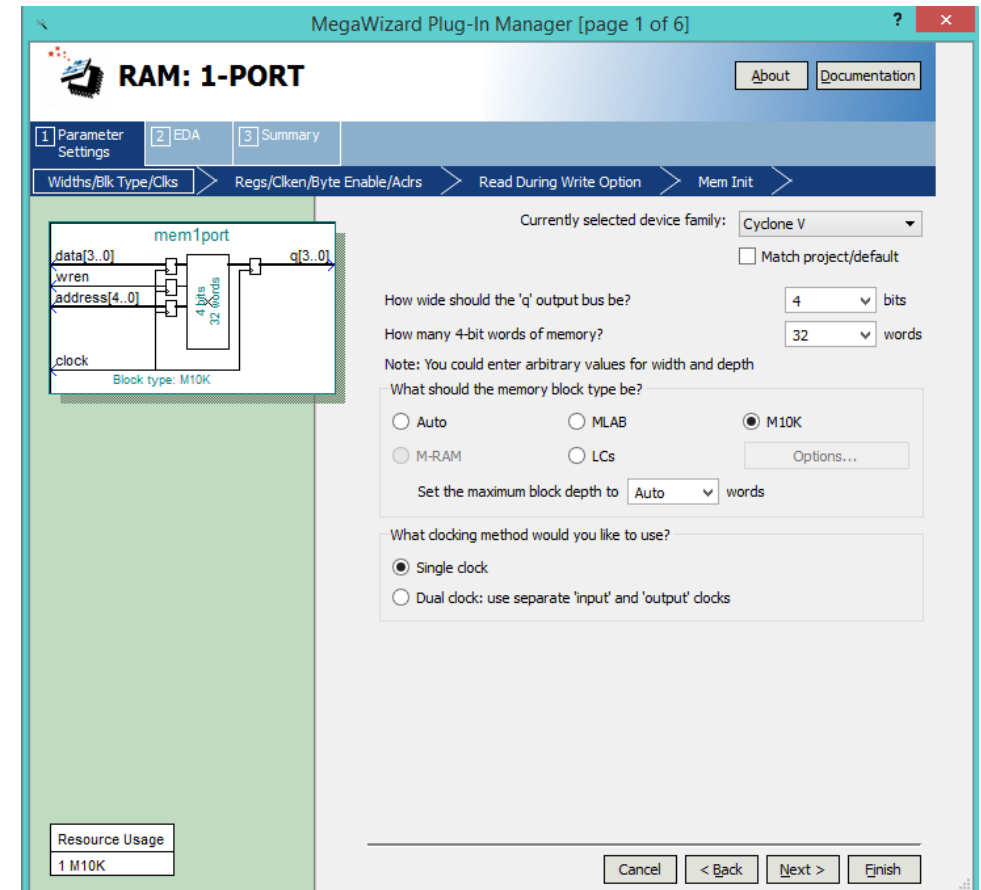
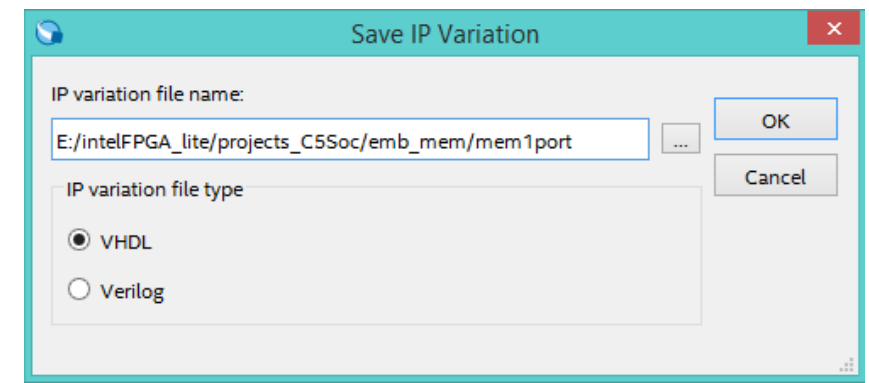
Quartus Prime

- Adding IP components
 - Look for the component in the IP Catalog
 - RAM: 1-PORT
 - PLL Intel FPGA IP
 - LPM_MULT
 - Right click on it to see Details
 - Double click to add the component



Quartus Prime

- Adding IP components
 - Create an IP Variation
 - You can create many of them with different names
 - Each variation may have different options
 - Set options and parameters in the MegaWizard Plug-In Manager
 - There are often many options
 - Some are not easy to understand
 - Usually leave default values
 - Unless you know what you are doing
 - Select the Instantiation template file
 - Useful when creating the system
 - Click Finish
 - Add Quartus Prime IP file to the project



Quartus Prime

- Adding IP components
 - Create a VHDL file with your top-level entity
 - The top-level is not the IP component
 - Declare the component at the beginning of the architecture
 - The file with extension .cmp already contains the component declaration
 - Just copy from it
 - Instantiate the component in your architecture
 - If you selected the Instantiation template file, then open the inst.vhd file
 - Copy the instantiation template
 - Assign the corresponding signals to the ports
 - You can even instantiate more than one component
 - Write a testbench and simulate
 - Program the FPGA and try it out on hardware