Politecnico di Torino

Computer Engineering Master's Degree Course (LM-32)

Report #1

Quartus Prime for FPGA programming

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1 Introduction

The **FPGA (Field-Programmable Gate Array) design flow** is an extremely important concept to be understood given the transition from theoretical digital logic to real world implementation. Now, while an AND gate is the most simple and trivial digital building block, its implementation on a real commercial grade hardware such as the **Intel Cyclone V** is a multi-faceted problem as one has to take into account synthesis, physical placement and timing issues. The aim of this project is to gain a holistic perspective on the modern digital design cycle with the help of **VHDL/Verilog** and professional CAD design tools. In this, we seek to explore the true meaning of the relationship between **logical design** and **physical performance** as opposed to simplistic functional verification.

Key Objectives

In the design, we undertake 3 major phases of design. They include:

- **Functional Verification:** The logic is verified through the use of a testbench and simulation to confirm that the design is working. This is done through the development of an RTL description.
- **Physical Implementation:** This involves the use of the *Pin Planner* and *Chip Planner* to perform logic distribution map and I/O block distribution map on the DE1-SoC board and to visualize the mapping of the design to the board.
- **Timing Optimization:** This takes into account the **Propagation Delay** (t_{pd}) and involves trying different pin assignments and various timing constraints.

As demonstrated in this project, the comparison of different hardware configurations like automatic and manual pin placement, and different distances between input-output pins shows how the physical routing and the rules of synthesis affect the performance and the robustness of the digital circuit.

2 Projects

2.1 Project #1: AND Gate Design and Timing Analysis

The design and production of a basic **AND logic gate** are tackled using a hardware description language (**VHDL** or **Verilog**). The first step involves initializing a new project and preparing the source files, which contain both the logic description for the gate and a corresponding **testbench**. After performing a syntax check and compiling the project, the design logic is verified via **simulation** to ensure it behaves as intended before hardware implementation.

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.ALL;
3
4  ENTITY myAnd IS
5          PORT(
6                  a: IN std_logic;
7                  b: IN std_logic;
8                  y: OUT std_logic);
9  END ENTITY myAnd;
10
11 ARCHITECTURE df OF myAnd IS
12 BEGIN
13         y <= a AND b;
14 END ARCHITECTURE df;
```

Once the design has passed validation, pin assignments are defined using the *Pin Planner*, and the physical implementation is examined through the *Chip Planner* to visualize how logic elements and I/O blocks are utilized. **Timing analysis** is a crucial phase of the project; it involves assessing the effects of pin assignments, timing constraints, and logic placement on the gate's **propagation**

delay (t_{pd}).
Several test configurations are evaluated, including automatic pin assignment (with and without timing constraints), manual clustering of pins, and manual dispersion of assigned pins. In specific cases, explicit timing constraints are applied and progressively tightened to study how synthesis and fitting tools adapt the placement.
Finally, the design is programmed onto the **Intel Cyclone V FPGA** on the **DE1-SoC board** for real-world hardware verification.

2.2 Propagation delay measurement

Input 1 pin	Input 2 pin	Output pin	Constraints (t_{pd})	Worst case (t_{pd})
PIN_AH28	PIN_AC25	PIN_AD25	5.965	6.162
PIN_AH28	PIN_AC25	PIN_AD25	5.965	5.965
PIN_AA18	PIN_Y17	PIN_AK22	5.965	5.965
PIN_AD9	PIN_C13	PIN_10	5.965	5.965
PIN_AD9	PIN_C13	PIN_10	5.965	5.965