SoC Verification

ELEN 613

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Hello!

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BSEE : Boston University
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    Electromagnetic / Antenna Theory
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    DFT & Partial Scan Techniques
Employment
    Lockheed Martin : Microwave/ Simulation
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Class
    Wednesday 7:10->9   O'Conner Hall 106
Office Hours
    45 minutes before class

Course Objective

A typical System-On-Chip consists of 1 or more embedded processors, on-chip bus, off-the-shelf peripherials (camera, display, wifi, Bluetooth, dsp, ethernet,…) , memory (DDR), low-power management, and other custom components.

Over 70% of the time is spent verifying SoC chips before fabrication. Functional bugs found later in the manufacturing cycle will be very costly, and may require a re-spin

This course presents several logical-verification techniques that is commonly used in industry today to ensure there are no bug-escapes

The techniques covered in this class will use the SystemVerilog design and verification language and will include code coverage, functional coverage, assertions, constraint random stimulus generation, and UVM (Universal Verification Methodology)

Expected Learning Outcomes

Understand verification techniques such as coverage, assertions, test stimulus, and UVM
Learn how to verify Verilog building blocks such as ALU, memory, FIFO's
Demonstrate how to write a testbench for a typical logic block
Verify a reference SoC design with a custom peripheral

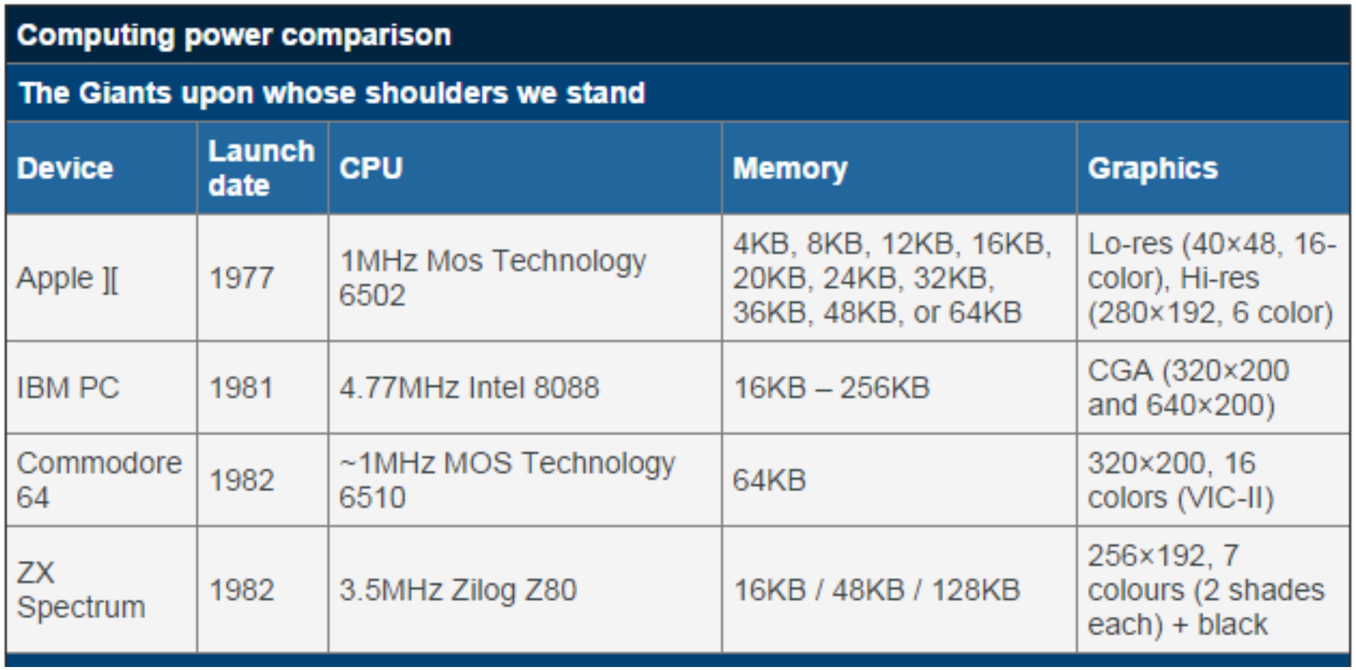
Course Outline

SoC Verification Overview
SystemVerilog Intro
Assertion-Based Verification (SVA)
Constraint-Based Random Testing
Functional Coverage
OOP + Classes in SV
General Verification Methodology
Verification Planning
UVM (Universal Verification Methodology)

Misc

- Grading Policy
  - 2-Take home Quizzes : 40%
  - Project : 60%
- Lectures to be posted on Camino!
- Design Center : Account Required

Computing Power
the old



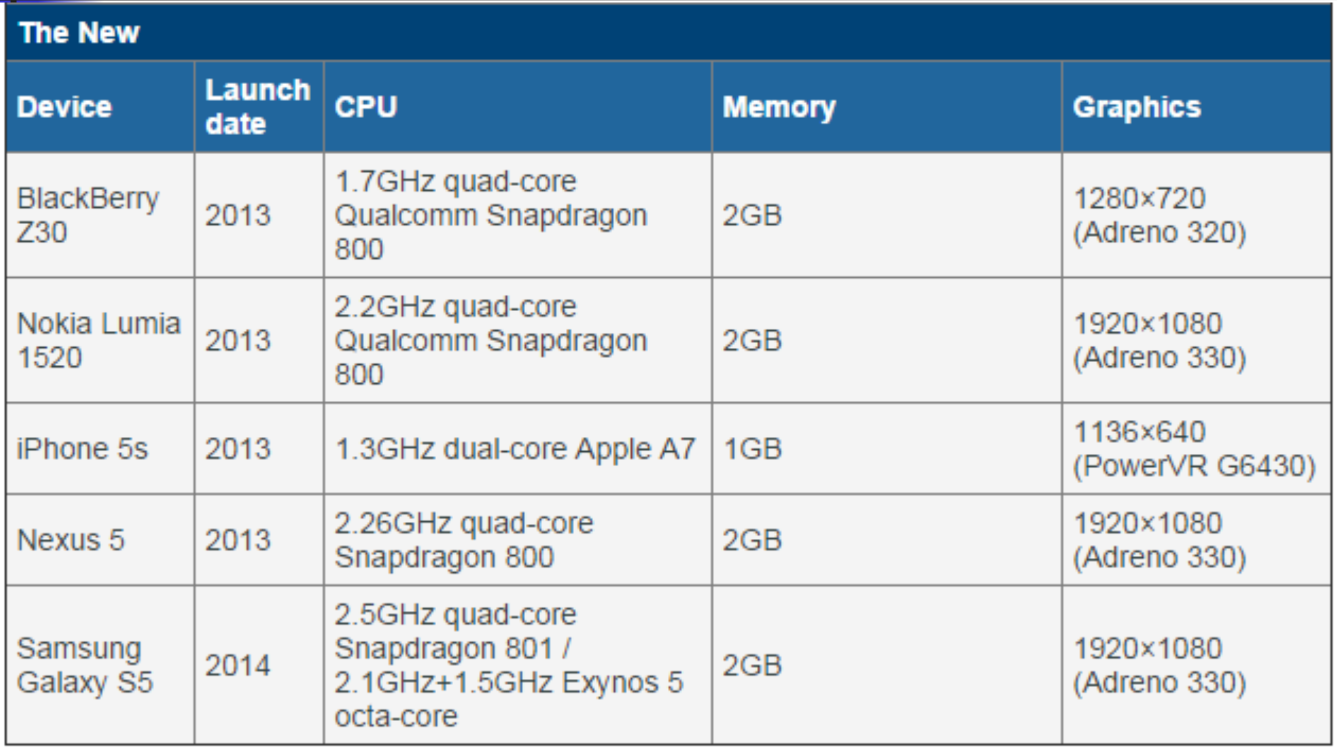
Computing power comparison

The Giants upon whose shoulders we stand

Device	Launch date	CPU	Memory	Graphics
Apple][	1977	1MHz Mos Technology 6502	4KB, 8KB, 12KB, 16KB, 20KB, 24KB, 32KB, 36KB, 48KB, or 64KB	Lo-res (40×48, 16-color), Hi-res (280×192, 6 color)
IBM PC	1981	4.77MHz Intel 8088	16KB – 256KB	CGA (320×200 and 640×200)
Commodore 64	1982	~1MHz MOS Technology 6510	64KB	320×200, 16 colors (VIC-II)
ZX Spectrum	1982	3.5MHz Zilog Z80	16KB / 48KB / 128KB	256×192, 7 colours (2 shades each) + black

Computing Power

the new



The New

Device	Launch date	CPU	Memory	Graphics
BlackBerry Z30	2013	1.7GHz quad-core Qualcomm Snapdragon 800	2GB	1280×720 (Adreno 320)
Nokia Lumia 1520	2013	2.2GHz quad-core Qualcomm Snapdragon 800	2GB	1920×1080 (Adreno 330)
iPhone 5s	2013	1.3GHz dual-core Apple A7	1GB	1136×640 (PowerVR G6430)
Nexus 5	2013	2.26GHz quad-core Snapdragon 800	2GB	1920×1080 (Adreno 330)
Samsung Galaxy S5	2014	2.5GHz quad-core Snapdragon 801 / 2.1GHz+1.5GHz Exynos 5 octa-core	2GB	1920×1080 (Adreno 330)

Evolution of IC Design

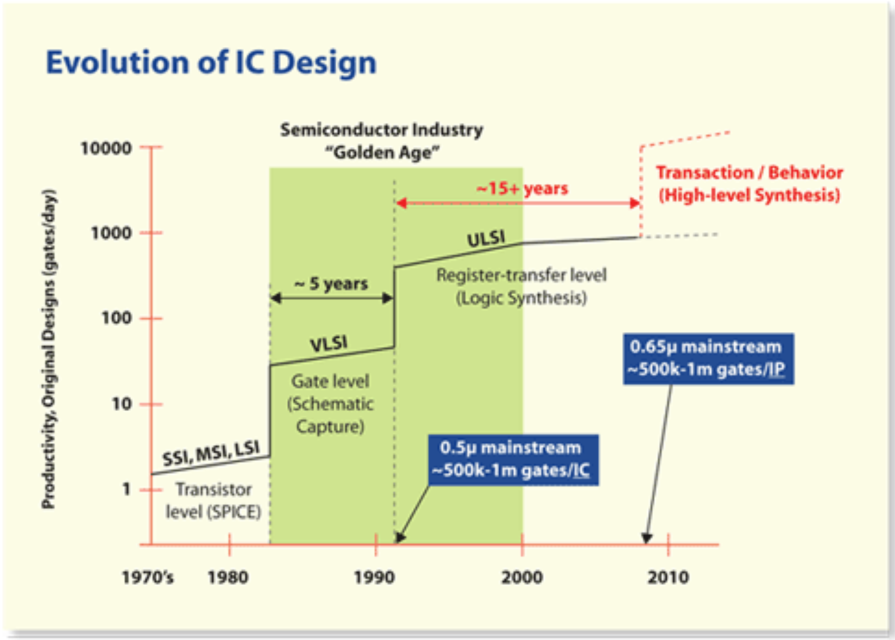
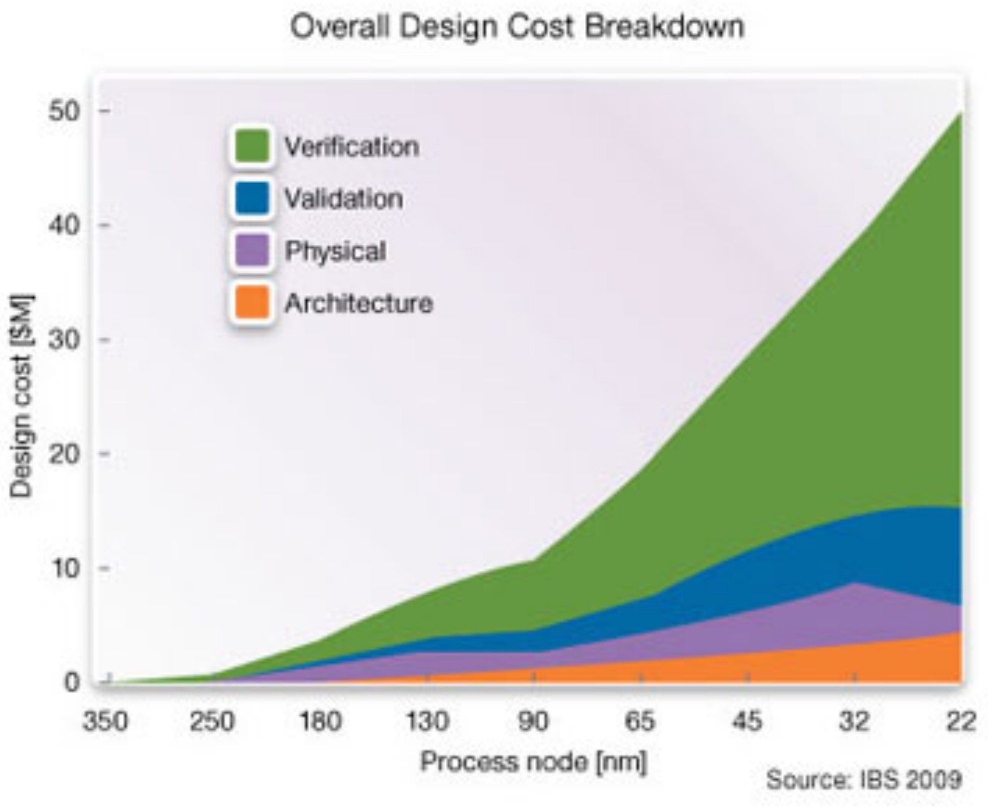


Figure 1. This chart shows the evolution of IC design from the mid-1970s to the present. The mid-1980s to 2000 was the semiconductor industry's period of fastest innovation, growth, and value-creation. This was driven in very large part by an over-100x increase in designer productivity.

Design Cost


Overall Design Cost Breakdown
Verification
Validation
Physical
Architecture
Design cost [$M]
0
10
20
30
40
50
350
250
180
130
90
65
45
32
22
Process node [nm]
Source: IBS 2009

Validation vs Verification

- Validation
  - Are we building the right product for today’s market?
- Verification
  - Is the product that we are build equivalent to the original spec?

Why Verify ?

82% of designs with re-spins resulting from logic and functional flows had design errors.

47% of designs with re-spins resulting from logic and functional flaws had incorrect or incomplete specification

32% of designs with re-spins resulting from logic and functional flaws had changes in specifications.

14% of all chips that failed had bugs in reused components or imported IP

Types of Verification

- Formal
  - Vector-less, uses formal mathematical properties to ascertain correctness against reference
- Dynamic
  - Vector-based scheme to verify a design against some reference model

Types of Verification

Logical Design Verification
Physical Verification
Timing Verification
Power Verification
Test Verification

Verification Complexity

SoC design
Growing number of features, modes, configurations
Power states
Increasing number of re-useable IP
HW/SW interaction
Increasing state-space
# of interfaces
..

How to reduce complexity?

Reduce chip complexity
Reduce number of designs
Increase resources
Increase productivity of engineers
Increase verification productivity
Increase size of compute farms

Design Challenges

- Create products fast
  - Time to market
  - Time to volume
- Create differentiation
- Put lots of features in your product

What is HDL?

- HDL = “Hardware Description Language”
- Describes hardware of digital systems in a text form
  - Logic diagrams
  - Boolean expressions
- Language is specialized to model digital circuits
  - Concurrency
  - Timing

What can I do with HDL??

- Logic Synthesis
  - “process of transforming a circuit from one level of abstraction to another”
  - Deriving a set of components and their interconnects with same functionality
  - Similar to compiling C code down to assembler code
    - Instead of object code, you get gates

What can I do with HDL??

- Logic Simulation
  - Reads in HDL code, interprets it and predicts how the digital circuit will perform in actual hardware
  - Allow one to test out the functional correctness of the circuit before fabricating it

HDL's in use today

- Standard HDL's from IEEE
  - Verilog
    - Developed initially by Gateway and then donated to standards committee by Cadence
  - VHDL (Very High Speed Integrated Circuit Hardware Description Language)
    - Developed initially as a Department of Defense language, but now used in industry also

What is HVL?

- HVL = “Hardware Verification Language”
- Language tailored to building re-usable, flexible testbenches
  - Higher level data-types
  - Testbench – DUT connectivity
  - Constrained random stimulus generation
  - Functional coverage
  - Assertions

- Vera, Specman “E”, TestBuilder,…

Origins of SystemVerilog

1983/85 – Automated Integrated Design Systems (later as Gateway Design Automation)
1989/90 – acquired by Cadence Design Systems
1990/91 – opened to the public in 1990 (because of VHDL pressure) - OVI (Open Verilog International) was born
1992 – the first simulator by another company, more to follow
1993 – IEEE working group to produce the IEEE Verilog standard 1364
May 1995 – IEEE Standard 1364-1995
2001 – IEEE Standard 1364-2001 – revised version
2005 – IEEE Standard 1364-2005 – clarifications; Verilog-AMS
2005 – IEEE Standard 1800-2005 – SystemVerilog 2005
2009 – Verilog and SystemVerilog merged – IEEE Standard 1800-2009
2013 – IEEE Standard 1800-2012 – SystemVerilog 2012
2017 – IEEE Standard 1800-2017 – SystemVerilog 2017

SystemVerilog Intro

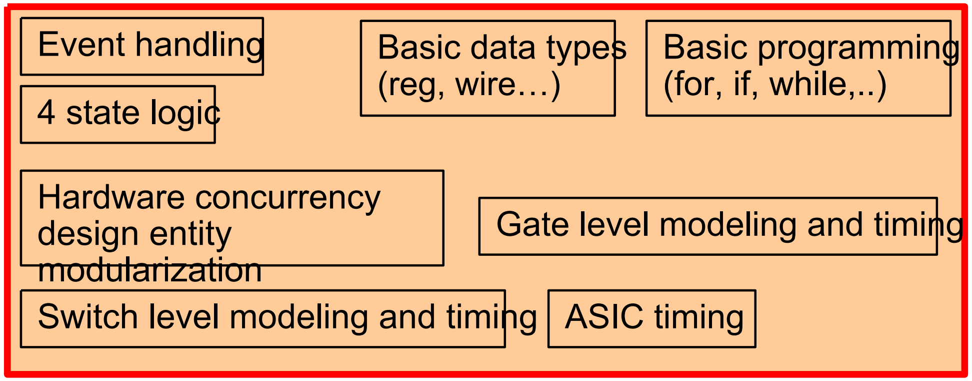
SystemVerilog is a superset of Verilog language

All usage, coding style that you learned in Verilog class still apply

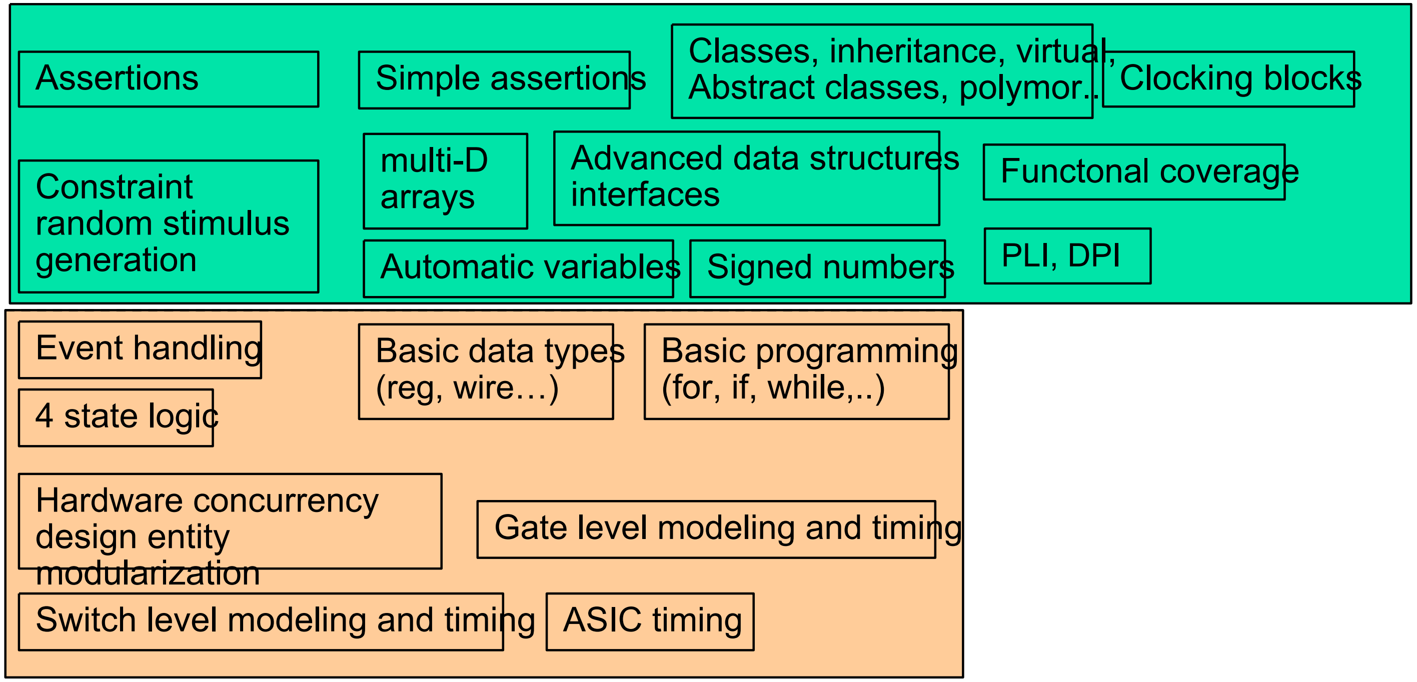
Part of SystemVerilog language is synthesizable for modeling hardware

Race conditions still exist in SystemVerilog, but there are addition coding styles/constructs that help prevent them

Verilog 1995/2001


Event handling
4 state logic
Basic data types (reg, wire…)
Basic programming (for, if, while,..)
Hardware concurrency design entity modularization
Gate level modeling and timing
Switch level modeling and timing
ASIC timing

SystemVerilog


Assertions
Simple assertions
Classes, inheritance, virtual, Abstract classes, polymor..
Clocking blocks
Constraint random stimulus generation
multi-D arrays
Advanced data structures interfaces
Functonal coverage
Automatic variables
Signed numbers
PLI, DPI
Event handling
4 state logic
Basic data types (reg, wire…)
Basic programming (for, if, while,..)
Hardware concurrency design entity modularization
Gate level modeling and timing
Switch level modeling and timing
ASIC timing

Data Types in Verilog

- Nets
  - Represents physical connections between gates, modules,..
  - Doesn’t store a value
  - It’s value determined by the value of its drivers (gate or continuous assignment), If no driver, then it’s high-impedance
  - net can be written by one or more continuous assignments, by primitive outputs, or through module ports.
  - The resultant value of multiple drivers is determined by the resolution function of the net type.
  - A net cannot be procedurally assigned
  - Built-in nettypes
    - wire tri tri0 supply0
    - wand triand tri1 supply1
    - wor trior trireg uwire

Data Types in Verilog

- Variables
  - Abstraction of a data storage element
  - Written to in initial & always blocks
  - Stores a value from one assignment to the next
  - Variables can be written by one or more procedural statements, including procedural continuous assignments. The last write determines the value.
  - Alternatively, variables can be written by one continuous assignment or one port.

Variable data types

shortint 2-state data type, 16-bit signed integer
int 2-state data type, 32-bit signed integer
longint 2-state data type, 64-bit signed integer
byte 2-state data type, 8-bit signed integer or ASCII character
bit 2-state data type, user-defined vector size, unsigned
logic 4-state data type, user-defined vector size, unsigned
reg 4-state data type, user-defined vector size, unsigned
integer 4-state data type, 32-bit signed integer
time 4-state data type, 64-bit unsigned integer

Unsized literal constants

An unsized single-bit value can be specified by preceding the single-bit value with an apostrophe ('), but without the base specifier. All bits of the unsized value shall be set to the value of the specified bit. In a

'0, '1, 'X, 'x, 'Z, 'z // sets all bits to specified value

logic [1023:0] x = ‘1; //easier in SV

Different than

logic [1023:0] x = ‘h1;

Format String

Argument	Description
%c or %C	Display in ASCII character format
%l or %L	Display library binding information
%v or %V	Display net signal strength
%m or %M	Display hierarchical name
%p or %P	Display as an assignment pattern
%s or %S	Display as a string
%t or %T	Display in current time format
%u or %U	Unformatted 2 value data
%z or %Z	Unformatted 4 value data

Writing '{en:'h0, data:'hde}
Reading '{en:'h1, data:'hef}

Logic , reg

In pre-SystemVerilog version, variables could only be driven procedurally

Reminder : reg != register

In SystemVerilog, variables can be written to procedural or through one-continuous assignment

logic == reg

Recommended to use “logic” (better name), but reg is equivalent

Examples

```
logic x;
initial x = 1’b1;

logic y;
assign y = x;

reg z;
assign z = !y;
```

Better Example

```
logic [7:0] count;
always @(posedge clk, negedge rst)
  if (!rst) count <= 8’b0000_0000;
  else
   count <= count + 1’b0;
```

Structures

structure represents a collection of data types that can be referenced as a whole , or the individual data
types that make up the structure can be referenced by name. By default, structures are unpacked

- Meaning: that there is an implementation-dependent packing of the data types. Unpacked structures can contain any data type.

Structures

```
typedef struct packed {
 logic [9:0]  head;
 logic [9:0]  tail;
 logic [9:0]  cnt;
 } t_fifo;

typedef struct packed {
  logic en;
  logic[7:0] data ;
  }  t_fifo_data;
```

Fifo example

```
module fifo  (output full, output empty, output t_fifo_data  dout, input t_fifo_data din,
                                              input clk, input reset, input push, input pop);
 t_fifo_data mem[1023:0];
 t_fifo fifo;
 assign dout = mem[fifo.tail];
 assign empty = (fifo.cnt == 0);
 assign full = (fifo.cnt == 1023);
always @(posedge clk or negedge reset) if (!reset) begin
          fifo.head <= 0;
          fifo.tail <= 0;
          fifo.cnt <= 0;
        end
        else if (pop && (!empty)) begin
          fifo.tail <= (fifo.tail + 1);
          fifo.cnt <= (fifo.cnt - 1);
        end
        else if (push && (!full)) begin
          mem[fifo.head] <= din;
          fifo.head <= (fifo.head + 1);
          fifo.cnt <= (fifo.cnt + 1);
        end
endmodule
```

Assignment for Next Week

Write a simple testbench that writes 4 random elements, then reads them, and checks that they are identical

Do Not Submit

Assignment to Structs

```
typedef struct {
   int addr;
   int crc;
   byte data[4];
} T_packet1;

// Use C-like means to initialize structure
T_packet1 pi = '{1,2,'{2,3,4,5}};

// Alternatively
pi.addr = 1;
Pi.crc = 2;
Pi.data[0] = 2;
```

Enumerated Types

Use for State Machine

```
typedef enum {red, yellow, green} t_light;
t_light light;
// by default enum's are of type int (can override)

always @(posedge clk) begin
    case (light)
      red : light <= yellow;
      yellow : light <= green;
      green : light <= red;
    endcase
end
```

Enumerated Types

```
initial $monitor ("light is %s %d " , light.name(),light);
```

```
light is red            0
light is yellow           1
light is green           2
```

More Examples

```
typedef enum {blue=8, red=4, yellow=2, green=1} t_
light;
t_light light;

$display(light.name());
light = 8;    //  ???

light = blue;
$display(light.name());
end
```

Methods for Enum

First
Last
Next
Prev
Num
name

Casting

Verilog = weakly typed language
SystemVerilog = more strongly typed

Similar to C-style casting

```
light = t_light'(8);
```

mem [1023:0] ↙ more modern

logic [7:0] mem [1024] ↖ old style

↙ 3-D

logic [7:0] mem1 [1023:0][7:0]

Arrays in SystemVerilog

Packed/Unpacked Arrays
Dynamic Arrays
Associative Arrays
Queues

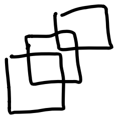
Packed/ Unpacked Arrays

Logic [1:0][2:0][3:0] packed1;

Logic [7:0] mem [127:0];

Logic [1:0][2:0] arr [3:0][4:0];
initial arr[3][4][2]=0;

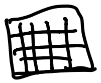
arr[3]



arr is 4D

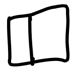
$\boxed{\%p}$

arr[3][4]



2 bit vector

arr[3][4][2]=



Dynamic Arrays

```
int ar2[][];
initial begin
 ar2 = new[44];
 ar2[0]=new[44];
 $display (ar2.size());
 $display (ar2[0].size());
end
```

Associative Arrays

similar to hash

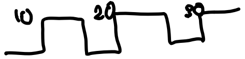
Useful for modeling sparse array
Index can be wildcard,datatype, or string type

```
 integer array1[*];
 integer array2[string];
 t_fifo_data array3[*];
```

array2["packet"] = ~~~

Queues

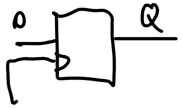
A queue is a variable-size, ordered collection of homogeneous elements.
t_fifo_data q1[$];
Built-in methods
Size,insert,delete,pop_front,pop_back,
push_front,push_back



Solutions only for TB ⇔ DUT

TB
initial
#10 d=1

instead use non-blocking: d<=1;
so d=1 will update at late phase so clk will always happen first

DUT


Clocking Blocks

Motiviation

Interaction between testbench and DUT must be handled correctly or non-deterministic results may occur

```
always #5 clk = !clk;
```

```
always @(posedge clk)
   q <= d;
```

```
initial #55 d = $random
```

Clocking Blocks

The clocking block separates the timing and synchronization details from the procedural statements
Thus, the timing for sampling and driving clocking block signals is implicit and relative to the clocking block's clock
.

Simple Example

```
clocking cb1 @(posedge clk ) ;
  input #1 full,empty,dout; ← for reading
  output #1 push,pop,din; ← for driving
endclocking
```

clocking block in reference to interface or TB that is driving signals

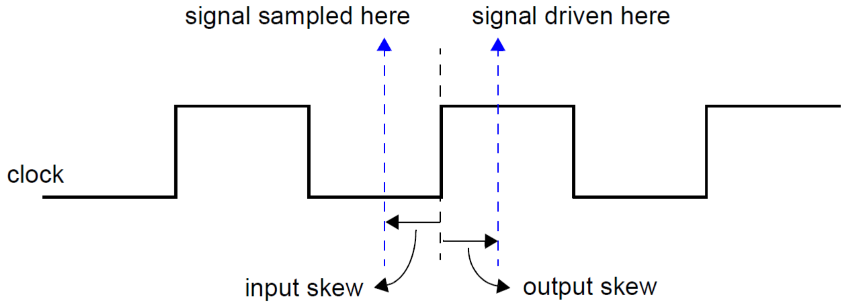


Figure 14-1—Sample and drive times including skew with respect to the positive edge of the clock

Skew

Default input skew is “#1step”
Default output skew is 0

#1step
- A 1step input skew allows input signals to sample their steady-state values in the time step immediately before the clock event

Using a clocking block

write('{1'b1, 8'hFF})

```
task write(input t_fifo_data x);
   cb1.din <= x;   // nba only here
   cb1.push <= 1'b1;
   @(cb1);   posedge clk
   cb1.push <= 1'b0;
endtask
```

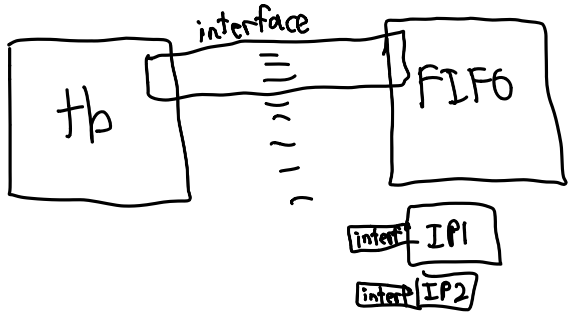
Note: all drives are synchronous

Stable
No design activity → cb1.din <=

NBA
update → din <=

Interfaces

- New Hierarchy construct for Verilog
- At its lowest level, an interface is a named bundle of nets or variables
- Additional power of the interface comes from its ability to encapsulate functionality as well as connectivity,



Interface Example

```
interface t_fifo_intf(input clk,reset);
  logic full, empty;
  t_fifo_data dout,din;
  logic push,pop;
endinterface
```

Fifo with Interface

```
module fifo  ( t_fifo_intf fifo_intf);

    t_fifo_data mem[1023:0];
    t_fifo fifo;

     assign fifo_intf.dout = mem[fifo.tail];
     assign fifo_intf.empty = (fifo.cnt == 0);
     assign fifo_intf.full = (fifo.cnt == 1023);
always @(posedge fifo_intf.clk or negedge fifo_intf.reset)
    if (!fifo_intf.reset) begin
      fifo.head <= 0;
      fifo.tail <= 0;
      fifo.cnt <= 0;
     end
     else if (fifo_intf.pop && (!fifo_intf.empty)) begin
      fifo.tail <= (fifo.tail + 1);
      fifo.cnt <= (fifo.cnt - 1);
     end
     else if (fifo_intf.push && (!fifo_intf.full)) begin
      mem[fifo.head] <= fifo_intf.din;
      fifo.head <= (fifo.head + 1);
      fifo.cnt <= (fifo.cnt + 1);
     end
endmodule
```

This compiles fine, but
What is the issue here
When we try and synthesize?

Testbench for fifo

```
module tb();
logic reset,clk;

t_fifo_intf fifo_intf(clk,reset);
initial begin
  clk=0;
end
  always #5 clk = !clk;

fifo DUT (.fifo_intf(fifo_intf) );

endmodule
```

```
task reset_dut();
   reset = 1'b0;
   fifo_intf.cb1.push <= 1'b0;
   fifo_intf.cb1.pop <= 1'b0;
   @(fifo_intf.cb1);
   reset = 1'b1;
   @(fifo_intf.cb1);
endtask
task write(input t_fifo_data x);
   fifo_intf.cb1.din <= x;
   fifo_intf.cb1.push <= 1'b1;
   @(fifo_intf.cb1);
   fifo_intf.cb1.push <= 1'b0;
endtask
task read(output t_fifo_data x);
  fifo_intf.cb1.pop <= 1'b1;
   @(fifo_intf.cb1);
  fifo_intf.cb1.pop <= 1'b0;
  $display("%p",fifo_intf.cb1.dout);
endtask
```

Full Example

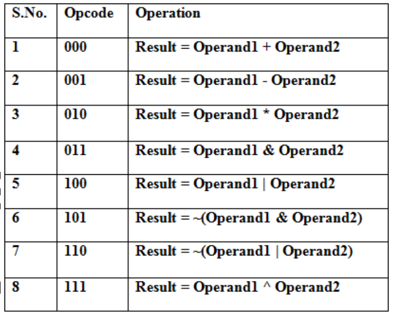
```
typedef struct packed {
 logic [9:0]  head;
 logic [9:0]  tail;
 logic [9:0]  cnt;
 } t_fifo;

typedef struct packed {
  logic en;
  logic[7:0] data ;
  }  t_fifo_data;

interface t_fifo_intf(input clk,reset);
  logic full, empty;
  t_fifo_data dout,din;
  logic push,pop;

  clocking cb1 @(posedge clk ) ;
    input #1 full,empty,dout;
    output #1  push,pop,din;
  endclocking

  modport dut(input clk,reset,output full,empty, input din, output dout, input push,pop); endinterface

module fifo  ( t_fifo_intf.dut fifo_intf);

      t_fifo_data mem[1023:0];
      t_fifo fifo;
        assign fifo_intf.dout = mem[fifo.tail];
        assign fifo_intf.empty = (fifo.cnt == 0);
        assign fifo_intf.full = (fifo.cnt == 1023);



always @(posedge fifo_intf.clk or negedge fifo_intf.reset) if (!fifo_intf.reset) begin
          fifo.head <= 0;
          fifo.tail <= 0;
          fifo.cnt <= 0;
        end
        else if (fifo_intf.pop && (!fifo_intf.empty)) begin
          fifo.tail <= (fifo.tail + 1);
          fifo.cnt <= (fifo.cnt - 1);
        end
        else if (fifo_intf.push && (!fifo_intf.full)) begin
          mem[fifo.head] <= fifo_intf.din;
          fifo.head <= (fifo.head + 1);
          fifo.cnt <= (fifo.cnt + 1);
        end
endmodule
//module fifo  (output full, output empty, output t_fifo_data  dout, input t_fifo_data din,
//                                              input clk, input reset, input push, input pop);
```

```
module tb();
logic reset,clk;

t_fifo_intf fifo_intf(clk,reset);
initial begin
  clk=0;
end
  always #5 clk = !clk;

   fifo DUT (.fifo_intf(fifo_intf) );

task reset_dut();
   reset = 1'b0;
   fifo_intf.cb1.push <= 1'b0;
   fifo_intf.cb1.pop <= 1'b0;
   @(fifo_intf.cb1);
   reset = 1'b1;
   @(fifo_intf.cb1);
endtask
task write(input t_fifo_data x);
   fifo_intf.cb1.din <= x;
   fifo_intf.cb1.push <= 1'b1;
   @(fifo_intf.cb1);
   fifo_intf.cb1.push <= 1'b0;
endtask
task read(output t_fifo_data x);
  fifo_intf.cb1.pop <= 1'b1;
   @(fifo_intf.cb1);
  fifo_intf.cb1.pop <= 1'b0;
  $display("%p",fifo_intf.cb1.dout);
endtask

t_fifo_data tmp;
initial begin
  reset_dut();
  write( '{1,1} );
  read(tmp);
  $finish;
end

endmodule
```

Assignment for Next Week

Write the SV code for an 8-bit ALU
Use ENUMS

Write the SV testbench us
interfaces/clocking blocks



S.No.	Opcode	Operation
1	000	Result = Operand1 + Operand2
2	001	Result = Operand1 - Operand2
3	010	Result = Operand1 * Operand2
4	011	Result = Operand1 & Operand2
5	100	Result = Operand1 | Operand2
6	101	Result = ~(Operand1 & Operand2)
7	110	Result = ~(Operand1 | Operand2)
8	111	Result = Operand1 ^ Operand2