Report

On

Verification of 10G Ethernet Mac Core

Final Project: Verification and Functional Coverage of 10G Ethernet Mac Core

ELEN: 613 SOC Verification

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Professor

Dr. Bruce Greene

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At



By

Jonathan (Johnny) Trinh

Student ID: W00001252098

Introduction:

In this project, we used the Universal Verification Methodology (UVM) to verify a 10G Ethernet Mac Core. We were given specs that included wishbone, xgmii, transmit, and receive signals. A basic covergroup was provided and additional coverpoints were written (i.e. packet length). We learned to employ object-oriented like programming to drive signals from the transmit side (via a driver) and monitor them (on both transmit and receive).

Procedure:

We set up the original environment with 'uvmgen' and generated an interface, driver, monitor, and sequencer for each agent (transmit and receive). A wishbone interface was also added to place down the DUT in the environment. The primary structure employed was a driver on the transmit side, that drove some stimulus onto the DUT. At the same time, a monitor was being used to see what was transmitted. The receive agent is passive so only the monitor was being used. A "data" class acts as a carrier or vehicle for the information going from the transmit to the receive. It packages the data from the transmit for each packet, and sends it to the receive where the data is unravelled from the dynamic array employed in the data class. With 20000 transactions occurring, we get the following:

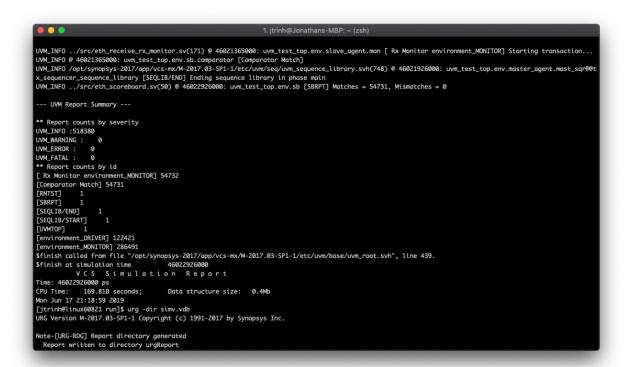


Figure 1: Screenshot of the VCS Simulation showing 54371 Matches When generating the functional coverage for the environment_test, the test shows about a 41% coverage. This default test satisfies a portion of the coverpoints, but not all in the covergroup.

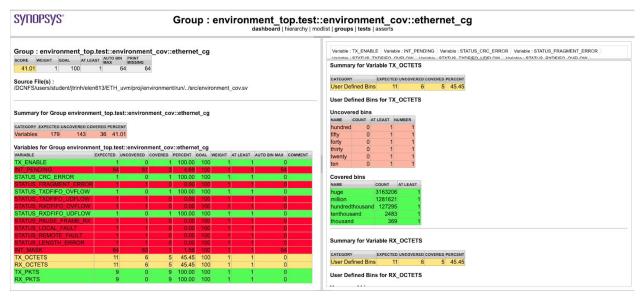


Figure 2: Screenshot of the Functional Coverage Report of Environment Test

Issues to Address:

While the environment_test that came with UVM took us as far as 40% in terms of coverage, much higher coverage was needed. To achieve such a goal, directed tests were to be written.

Approaches Taken:

Within the test module, an additional test was written, where the base_sequence class was subclassed and added to the sequence library. This test, however, used a different "data" class that was defined by "eth_data_oversized" which represents a packet that is too large. This "eth_data_oversized" (defined in eth_transmit_eth_data.sv) is a subclass of the regular "eth_data" class and has constraints that bring it outside the boundary of what is defined in the specifications.

The alternative is to simply define an inline constraint within virtual task body using the *uvm_do_with* function and specify the narrower constraint.

Further Thoughts:

Unfortunately, out of the 11 bins for TX_OCTETS and/or RX_OCTETS, only five were covered. These numbers represents the number of bytes transmitted and since the "large" bins were hit, it would be better to write a directed test with a smaller packet size (or perhaps limit the dynamic allocation to a certain size within the eth_data class). Additionally to address the overflow/underflow issues, one can transmit without enabling the receive side (since there was a signal called *pkt_rx_ren* or the enable). This allows the FIFO to fill up and overflow. Inversely,

the DUT can receive while the FIFO is empty causing an underflow error. Achieving both requires a derived class of the monitor that overrides the receive function to simply not receive (in the first case) or receive faster than then transmitting (in the second case).

Takeaways:

- 1. UVM is a very robust tool for systematically generating every object needed (i.e. drivers, monitors, etc.) though many files need to be touched to maintain consistency.
- 2. Creation of an environment as well as a new one for every directed test can save changing original code
- 3. The object-oriented paradigm is extremely prevalent within UVM and is useful for writing separate test cases (whether it be creating a derived class of data, drivers, monitors, etc.)