Bianca Louise V. Manganaan

FIXED BIAS CIRCUIT

Example 7.2 For the fixed bias circuit in figure 7.15, $R_B = 750K\Omega$, $R_C = 2.2K\Omega$, $V_{CC} = 16$ V and β of the Si transistor is 199. Determine the following:

(a) DC operating voltages and currents of the transistor amplifier (I_{BQ}, I_{CQ}, I_{EQ} and V_{CEQ})
(b) amplification factor, α
(c) collector saturation level of the transistor
(d) maximum DC collector-emitter voltage of the transistor
(e) region of operation for the transistor

a. $I_{BQ} = V_{cc} - V_{ce} / R_c = (16 - 0.7) / 750000 = 0.0000204$

$I_{CQ} = Beta(I_B) = (199)(0.0000204) = 0.0040596$

$I_{EQ} = I_{BQ} + I_{CQ} = 0.0040596 + 0.0000204 = 0.00408$

$V_{CEQ} = V_{CC} - I_C R_C = 16 - 0.0040596(2200) = 7.07$

b. alpha = beta / (beta + 1) = 199/(199+1) = 0.995
c. $I_{C(sat)} = V_{cc} / R_c = 16 / 2200 = 0.00727$
d. $V_{CE(off)} = V_{CC} = 16V$
e. $0 < I_{CQ} < 0.00727$ & $0 < V_{CEQ} < 16$; Transistor is in the active region

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FIXED BIAS CIRCUIT

Example 7.2 For the fixed bias circuit in figure 7.15, $R_B = 750K\Omega$, $R_C = 2.2K\Omega$, $V_{CC} = 16$ V and β of the Si transistor is 199. Determine the following:

(a) DC operating voltages and currents of the transistor amplifier (I_{BQ}, I_{CQ}, I_{EQ} and V_{CEQ})
(b) amplification factor, α
(c) collector saturation level of the transistor
(d) maximum DC collector-emitter voltage of the transistor
(e) region of operation for the transistor

EMITTER STABILIZED BIAS CIRCUIT

Example 7.3 Design a BJT emitter-stabilized bias circuit to have a saturation level of 20mA and a quiescent operating point midway between the cut-off and saturation region. Use a 15 V dc supply, an NPN silicon transistor with $\beta = 199$ and a collector resistance which is one-fifth of the emitter base resistance.

$I_{CQ} = 0.5\ I_{C(sat)} = 0.5(0.020) = 0.01A$

$V_{CEQ} = 0.5\ V_{CE(off)} = 0.5(15) = 7.5$

$I_{BQ} = I_{CQ}/Beta = 0.01 / 199 = 0.00005025125$

$I_{EQ} = 0.01 + 0.00005025125 = 0.01005025125$

$V_{CE} = V_{CC} - I_CR_C - I_ER_E$

$R_E = (V_{cc} - V_{CE})/ (0.2I_C + I_E) = (15-7.5)/ (0.2(0.01) + 0.01005025125) = 622.3936$

$R_c = 0.2R_E = 124,48$

$R_B = (V_{CC} - 0.7 - I_B(Beta+1)R_E)/I_B = (15 - 0.7 - 0.01005025125(622.3936)) / 0.00005025125$

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FIXED BIAS CIRCUIT

Example 7.2 For the fixed bias circuit in figure 7.15, $R_B = 750K\Omega$, $R_C = 2.2K\Omega$, $V_{CC} = 16$ V and β of the Si transistor is 199. Determine the following:

(a) DC operating voltages and currents of the transistor amplifier (I_{BQ}, I_{CQ}, I_{EQ} and V_{CEQ})
(b) amplification factor, α
(c) collector saturation level of the transistor
(d) maximum DC collector-emitter voltage of the transistor
(e) region of operation for the transistor

= 160091.30

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FIXED BIAS CIRCUIT

Example 7.2 For the fixed bias circuit in figure 7.15, $R_B = 750K\Omega$, $R_C = 2.2K\Omega$, $V_{CC} = 16$ V and β of the Si transistor is 199. Determine the following:

(a) DC operating voltages and currents of the transistor amplifier (I_{BQ}, I_{CQ}, I_{EQ} and V_{CEQ})
(b) amplification factor, α
(c) collector saturation level of the transistor
(d) maximum DC collector-emitter voltage of the transistor
(e) region of operation for the transistor

VOLTAGE DIVIDER BIAS CIRCUIT

Example 7.4 For the voltage divider bias circuit in figure 7.24, $R_{B1} = 13K\Omega$, $R_{B2} = 2.2K\Omega$, $R_C = 6.8K\Omega$, $R_E = 1.5K\Omega$, $V_{CC} = 15$ V, $V_{CE(sat)} = 0.3$V and β of the Si transistor is 80. Determine the following:

(a) DC base voltage and DC emitter voltage of the transistor amplifier
(b) DC operating voltages and currents of the transistor amplifier (I_{BQ}, I_{CQ}, I_{EQ} and V_{CEQ})
(c) Collector saturation level of the transistor
(d) Maximum DC collector-emitter voltage of the transistor
(e) Region of operation of the transistor

a. $V_B = V_{CC} \times (R_{B2} / R_{B1} + R_{B2}) = 15 \times (2200/(13000+2200)) = 2.171$

   $V_E = V_B - V_{BE} = 2.17 - 0.7 = 1.47$

b. $I_{EQ} = V_E / R_E = 1.47 / 1500 = 0.00098$

   $I_{BQ} = 0$

   $I_{CQ} = 0.00098$

   $V_{CEQ} = V_{CC} - I_C R_C - I_E R_E = 15 - 0.00098(6800) - 0.00098(1500) = 6.866$

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FIXED BIAS CIRCUIT

Example 7.2 For the fixed bias circuit in figure 7.15, $R_B = 750K\Omega$, $R_C = 2.2K\Omega$, $V_{CC} = 16$ V and β of the Si transistor is 199. Determine the following:

(a) DC operating voltages and currents of the transistor amplifier (I_{BQ}, I_{CQ}, I_{EQ} and V_{CEQ})
(b) amplification factor, α
(c) collector saturation level of the transistor
(d) maximum DC collector-emitter voltage of the transistor
(e) region of operation for the transistor

c. $I_{C(sat)} = V_{CC} - V_{CE(sat)}$,/ $(R_C + R_E) = (15 - 0.3) / (6800 + 1500) = 0.001771$

d. $V_{CE(off)} = V_{CC} = 15$

e. $0 < I_{CQ} < 0.001771$ & $0.3 < V_{CEQ} < 15$; transistor operates in the active region