1. Description

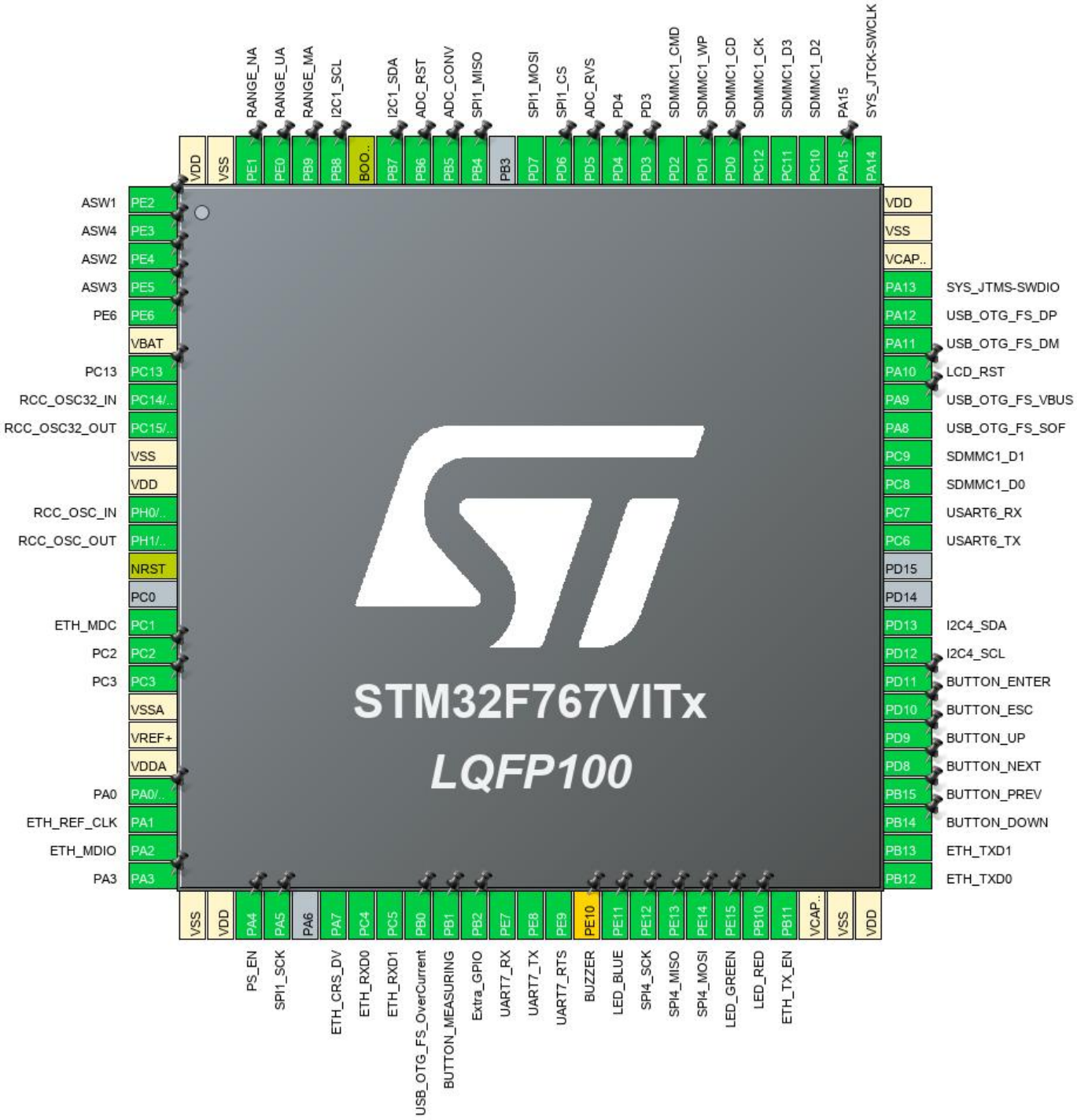
1.1. Project

Project Name	DP_STM32F767VIT_LQFP100
Board Name	custom
Generated with:	STM32CubeMX 5.6.0
Date	06/01/2020

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767VITx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	ASW1
2	PE3 *	I/O	GPIO_Output	ASW4
3	PE4 *	I/O	GPIO_Output	ASW2
4	PE5 *	I/O	GPIO_Output	ASW3
5	PE6 *	I/O	GPIO_Output	PE6
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	PC13
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0/OSC_IN	I/O	RCC_OSC_IN	
13	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
16	PC1	I/O	ETH_MDC	
17	PC2 *	I/O	GPIO_Output	PC2
18	PC3 *	I/O	GPIO_Output	PC3
19	VSSA	Power		
20	VREF+	Power		
21	VDDA	Power		
22	PA0/WKUP *	I/O	GPIO_Output	PA0
23	PA1	I/O	ETH_REF_CLK	
24	PA2	I/O	ETH_MDIO	
25	PA3 *	I/O	GPIO_Output	PA3
26	VSS	Power		
27	VDD	Power		
28	PA4 *	I/O	GPIO_Output	PS_EN
29	PA5	I/O	SPI1_SCK	
31	PA7	I/O	ETH_CRS_DV	
32	PC4	I/O	ETH_RXD0	
33	PC5	I/O	ETH_RXD1	
34	PB0	I/O	GPIO_EXTI0	USB_OTG_FS_OverCurrent
35	PB1	I/O	GPIO_EXTI1	BUTTON_MEASURING
36	PB2	I/O	GPIO_EXTI2	Extra_GPIO
37	PE7	I/O	UART7_RX	
38	PE8	I/O	UART7_TX	

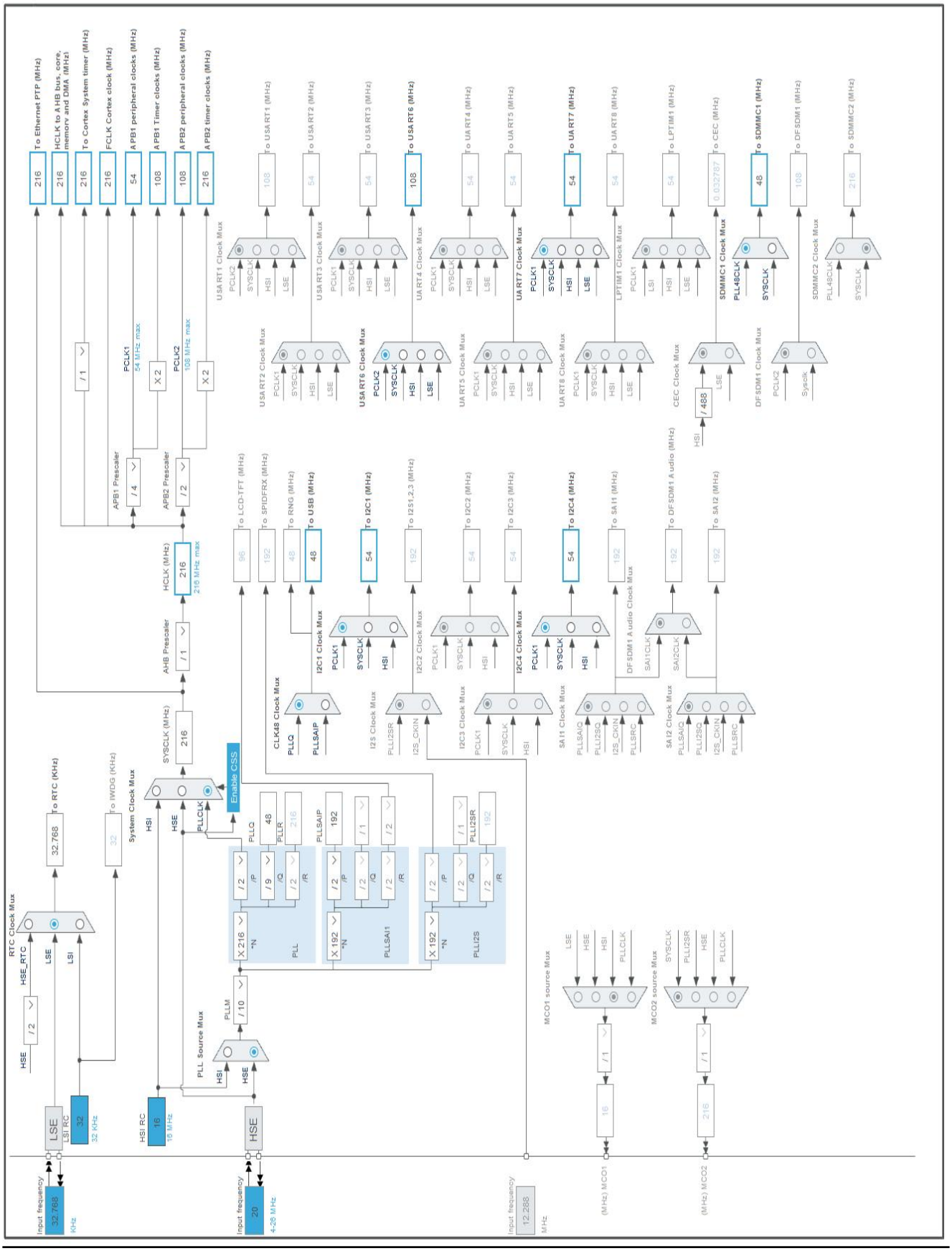
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	PE9	I/O	UART7_RTS	
40	PE10 **	I/O	TIM1_CH2N	BUZZER
41	PE11 *	I/O	GPIO_Output	LED_BLUE
42	PE12	I/O	SPI4_SCK	
43	PE13	I/O	SPI4_MISO	
44	PE14	I/O	SPI4_MOSI	
45	PE15 *	I/O	GPIO_Output	LED_GREEN
46	PB10 *	I/O	GPIO_Output	LED_RED
47	PB11	I/O	ETH_TX_EN	
48	VCAP_1	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	ETH_TXD0	
52	PB13	I/O	ETH_TXD1	
53	PB14	I/O	GPIO_EXTI14	BUTTON_DOWN
54	PB15	I/O	GPIO_EXTI15	BUTTON_PREV
55	PD8	I/O	GPIO_EXTI8	BUTTON_NEXT
56	PD9	I/O	GPIO_EXTI9	BUTTON_UP
57	PD10	I/O	GPIO_EXTI10	BUTTON_ESC
58	PD11	I/O	GPIO_EXTI11	BUTTON_ENTER
59	PD12	I/O	I2C4_SCL	
60	PD13	I/O	I2C4_SDA	
63	PC6	I/O	USART6_TX	
64	PC7	I/O	USART6_RX	
65	PC8	I/O	SDMMC1_D0	
66	PC9	I/O	SDMMC1_D1	
67	PA8	I/O	USB_OTG_FS_SOF	
68	PA9 *	I/O	GPIO_Output	USB_OTG_FS_VBUS
69	PA10 *	I/O	GPIO_Output	LCD_RST
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15 *	I/O	GPIO_Output	PA15
78	PC10	I/O	SDMMC1_D2	
79	PC11	I/O	SDMMC1_D3	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
80	PC12	I/O	SDMMC1_CK	
81	PD0 *	I/O	GPIO_Input	SDMMC1_CD
82	PD1 *	I/O	GPIO_Output	SDMMC1_WP
83	PD2	I/O	SDMMC1_CMD	
84	PD3	I/O	GPIO_EXTI3	PD3
85	PD4	I/O	GPIO_EXTI4	PD4
86	PD5 *	I/O	GPIO_Input	ADC_RVS
87	PD6 *	I/O	GPIO_Output	SPI1_CS
88	PD7	I/O	SPI1_MOSI	
90	PB4	I/O	SPI1_MISO	
91	PB5 *	I/O	GPIO_Output	ADC_CONV
92	PB6 *	I/O	GPIO_Output	ADC_RST
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
95	PB8	I/O	I2C1_SCL	
96	PB9 *	I/O	GPIO_Output	RANGE_MA
97	PE0 *	I/O	GPIO_Output	RANGE_UA
98	PE1 *	I/O	GPIO_Output	RANGE_NA
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	DP_STM32F767VIT_LQFP100
Project Folder	C:\Users\Michal-Dell\Disk Google\DP\05_SW\DP_STM32F767VIT_LQFP100
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767VITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

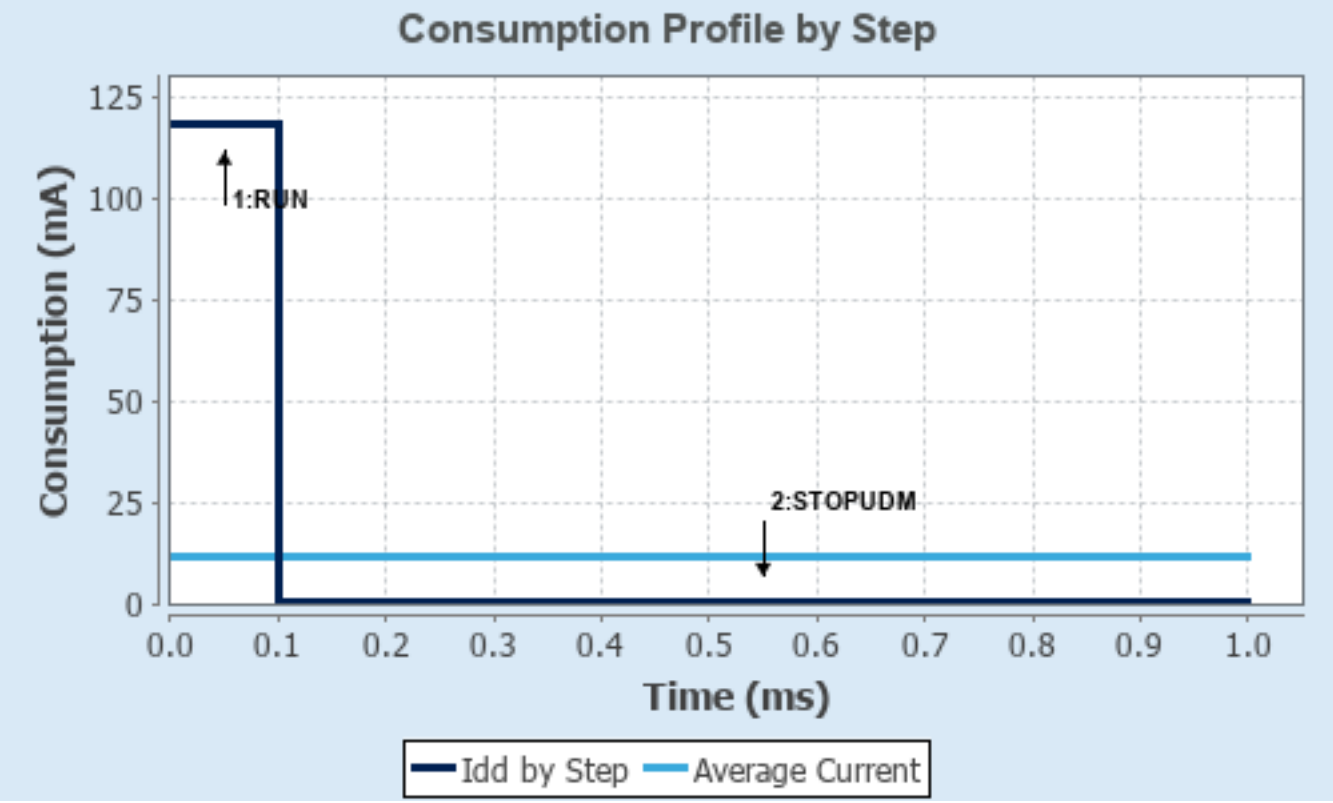
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	88.26	104.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
125
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCLERATOR	**Enabled ***
Instruction Prefetch	**Enabled ***
CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.2. ETH

Mode: RMII

7.2.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

7.2.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Interrupt Source Flag register Offset	**0x001D ***
PHY Link down inturrupt	**0x000B ***

7.3. GPIO

7.4. I2C1

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0

Analog Filter	Enabled
Timing	**0x6000030D ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. I2C4

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x6000030D ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.7. RTC

mode: Activate Clock Source

mode: Activate Calendar

7.7.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	**12 ***
Minutes	**32 ***
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	**February ***
Date	**8 ***
Year	**14 ***

7.8. SDMMC1

Mode: SD 4 bits Wide bus

7.8.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

7.9. SPI1

Mode: Full-Duplex Master

7.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**54.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.10. SPI4

Mode: Full-Duplex Master

7.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***

Baud Rate	**6.75 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.11. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.12. TIM4

Clock Source : Internal Clock

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**108 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.13. TIM5

mode: Clock Source

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**108 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xFFFFFFFF-1 ***
Internal Clock Division (CKD)	No Division

auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.14. TIM7

mode: Activated

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.15. TIM14

mode: Activated

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**54000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF-1 ***
Internal Clock Division (CKD)	**Division by 2 ***
auto-reload preload	Disable

7.16. UART7

Mode: Asynchronous

Hardware Flow Control (RS232): RTS Only

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	**1500000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	**8 Samples ***
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.17. USART6

Mode: Asynchronous

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	**2000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	**8 Samples ***
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable

MSB First	Disable

7.18. USB_OTG_FS

Mode: Host_Only

mode: Activate_SOF

7.18.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Signal start of frame	Enabled

7.19. FATFS

mode: SD Card

mode: USB Disk

mode: User-defined

7.19.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	**Enabled with static working buffer on the BSS ***
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	3
MAX_SS (Maximum Sector Size)	**4096 ***
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

7.19.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance	SDMMC1
Use dma template	Disabled
BSP code for SD	Generic

USBH:

USBH instance	USB Host MSC FS
Use dma template	Disabled

7.20. USB_HOST

Class for FS IP: Mass Storage Host Class

7.20.1. Parameter Settings:

Host Configuration:

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	2
USBH_MAX_NUM_INTERFACES (Maximun number of interfaces)	2
USBH_MAX_NUM_SUPPORTED_CLASS (Maximun number of supported class)	1
USBH_MAX_NUM_CONFIGURATION (Maximun number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximun size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximun size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	0: No debug message

CMSIS_RTOS:

USBH_USE_OS (Enable the support of an RTOS)	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C4	PD12	I2C4_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PD13	I2C4_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI4	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE13	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE14	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
UART7	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE9	UART7_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Single Mapped Signals	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	BUZZER
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	ASW1
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	ASW4
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	ASW2
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	ASW3
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PE6
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PC13
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PC2
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PC3
	PA0/WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PA0
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PA3
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	PS_EN
	PB0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	USB_OTG_FS_OverCurrent
	PB1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	BUTTON_MEASURING
	PB2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	Extra_GPIO
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LED_BLUE
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LED_GREEN
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LED_RED
	PB14	GPIO_EXTI14	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	BUTTON_DOWN
	PB15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	BUTTON_PREV
	PD8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	BUTTON_NEXT
	PD9	GPIO_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	BUTTON_UP
	PD10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	BUTTON_ESC

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	BUTTON_ENTER
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS_VBUS
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RST
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PA15
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SDMMC1_CD
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	SDMMC1_WP
	PD3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	PD3
	PD4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	PD4
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	ADC_RVS
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_CS
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	ADC_CONV
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	ADC_RST
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	RANGE_MA
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	RANGE_UA
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	RANGE_NA

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_RX	DMA2_Stream0	Peripheral To Memory	**Very High ***
SPI1_TX	DMA2_Stream3	Memory To Peripheral	**Very High ***
UART7_TX	DMA1_Stream1	Memory To Peripheral	**High ***
USART6_RX	DMA2_Stream1	Peripheral To Memory	**Very High ***
USART6_TX	DMA2_Stream6	Memory To Peripheral	**Very High ***

SPI1_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_TX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART7_TX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_TX: DMA2_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte
Peripheral Burst Size:	Single
Memory Burst Size:	Single

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	1	0
EXTI line1 interrupt	true	1	0
EXTI line2 interrupt	true	1	0
EXTI line3 interrupt	true	1	0
EXTI line4 interrupt	true	1	0
DMA1 stream1 global interrupt	true	2	0
EXTI line[9:5] interrupts	true	1	0
SPI1 global interrupt	true	3	0
EXTI line[15:10] interrupts	true	1	0
DMA2 stream0 global interrupt	true	2	0
DMA2 stream1 global interrupt	true	2	0
DMA2 stream3 global interrupt	true	2	0
USB On The Go FS global interrupt	true	0	0
DMA2 stream6 global interrupt	true	0	0
USART6 global interrupt	true	3	0
UART7 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
SDMMC1 global interrupt	unused		
TIM5 global interrupt	unused		
TIM7 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
SPI4 global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current

10. Software Pack Report