Flow Summary

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Flow Status	Successful - Tue May 16 00:43:54 2
Quartus Prime Version	22.1std.1 Build 917 02/14/2023 SC
Revision Name	CPUP1_Arqui
Top-level Entity Name	top
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	2,136 / 32,070 (7 %)
Total registers	777
Total pins	29 / 457 (6 %)
Total virtual pins	0
Total block memory bits	2,241,400 / 4,065,280 (55 %)
Total DSP Blocks	2 / 87 (2 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

Analysis & Synthesis Resource Usage Summary

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	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	1936
2		
3	Combinational ALUT usage for logic	3343
1	-- 7 input functions	33
2	-- 6 input functions	450
3	-- 5 input functions	1375
4	-- 4 input functions	1029
5	-- <=3 input functions	456
4		
5	Dedicated logic registers	679
6		
7	I/O pins	29
8	Total MLAB memory bits	0
9	Total block memory bits	2241400
10		
11	Total DSP Blocks	2
12		
13	Maximum fan-out node	clk~input
14	Maximum fan-out	883
15	Total fan-out	24469
16	Average fan-out	5.61

Analysis & Synthesis Resource Utilization by Entity

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	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	
1	|top	3343 (0)	679 (0)	2241400	2	29	0	|top
1	|dmem:datmem|	72 (0)	7 (1)	2241400	0	0	0	|top|dm
2	|imem:instmem|	24 (24)	0 (0)	0	0	0	0	|top|ime
3	|ripp:processor|	3064 (0)	567 (0)	0	2	0	0	|top|ripp
4	|vga_top:vga|	183 (0)	105 (0)	0	0	0	0	|top|vga
1	|SYNC:sync|	148 (148)	76 (76)	0	0	0	0	|top|vga
2	|clockDivider:clock_convertor|	35 (35)	29 (29)	0	0	0	0	|top|vga

Analysis & Synthesis RAM Summary

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Name	Type	Mode	Port A Depth	Port A Width	Port B Depth	Port B Width	Size	
datmem|altsyncram:RAM_rtl...60s1:auto_generated|ALTSYNCRAM	AUTO	Simple Dual Port	40025	32	40025	32	1280800	db/CPUP1_Arq
datmem|altsyncram:RAM_rtl...2tu1:auto_generated|ALTSYNCRAM	AUTO	Simple Dual Port	40025	32	40025	32	1280800	db/CPUP1_Arq

	Statistic	Number Used
1	Two Independent 18x18	1
2	Sum of two 18x18	1
3	Total number of DSP blocks	2
4		
5	Fixed Point Unsigned Multiplier	3

General Register Statistics

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	Statistic	Value
1	Total registers	679
2	Number of registers using Synchronous Clear	115
3	Number of registers using Synchronous Load	72
4	Number of registers using Asynchronous Clear	280
5	Number of registers using Asynchronous Load	0
6	Number of registers using Clock Enable	389
7	Number of registers using Preset	0