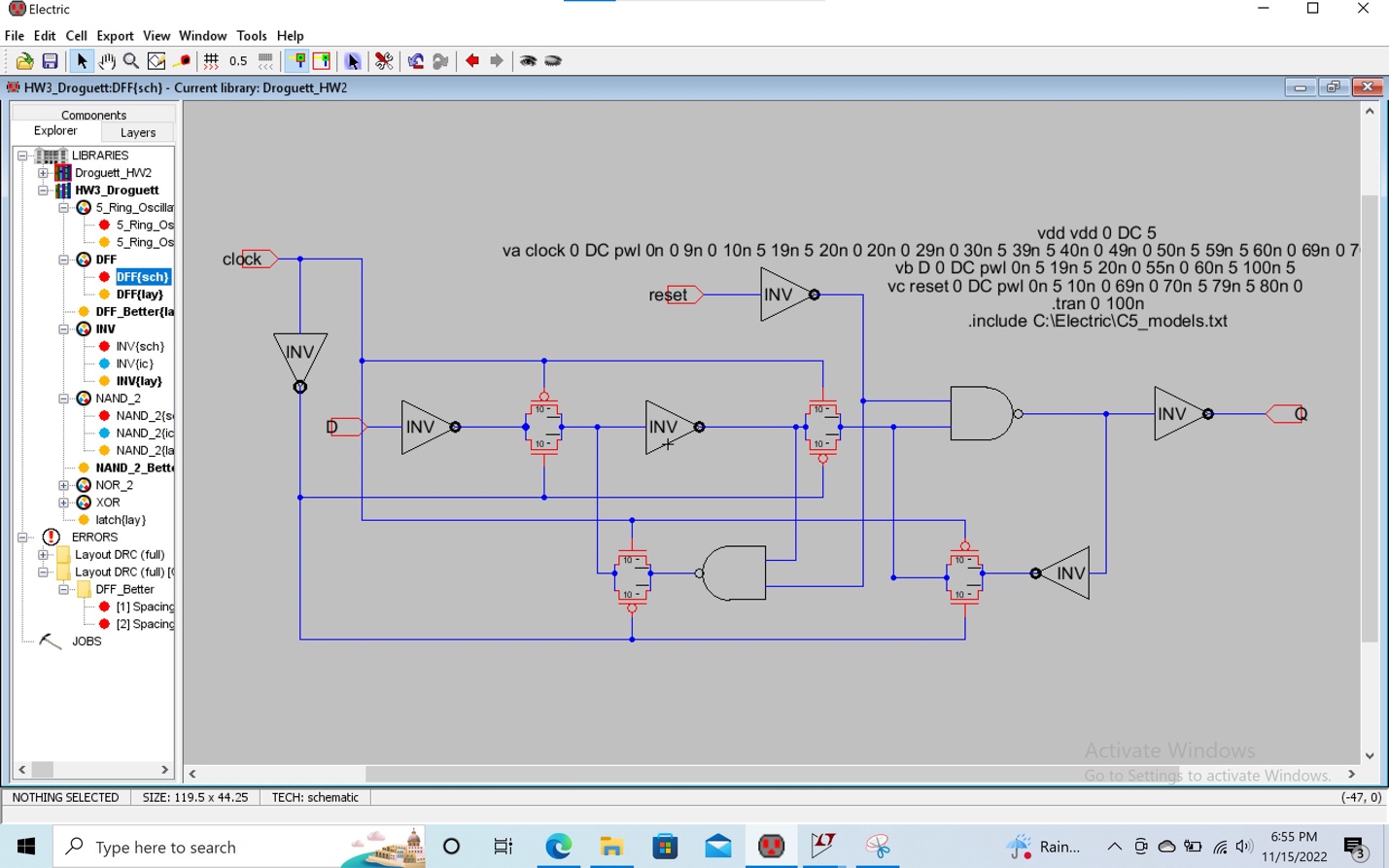
Cristobal Droguett

EECE 574

Milestone 1

DFF Schematic

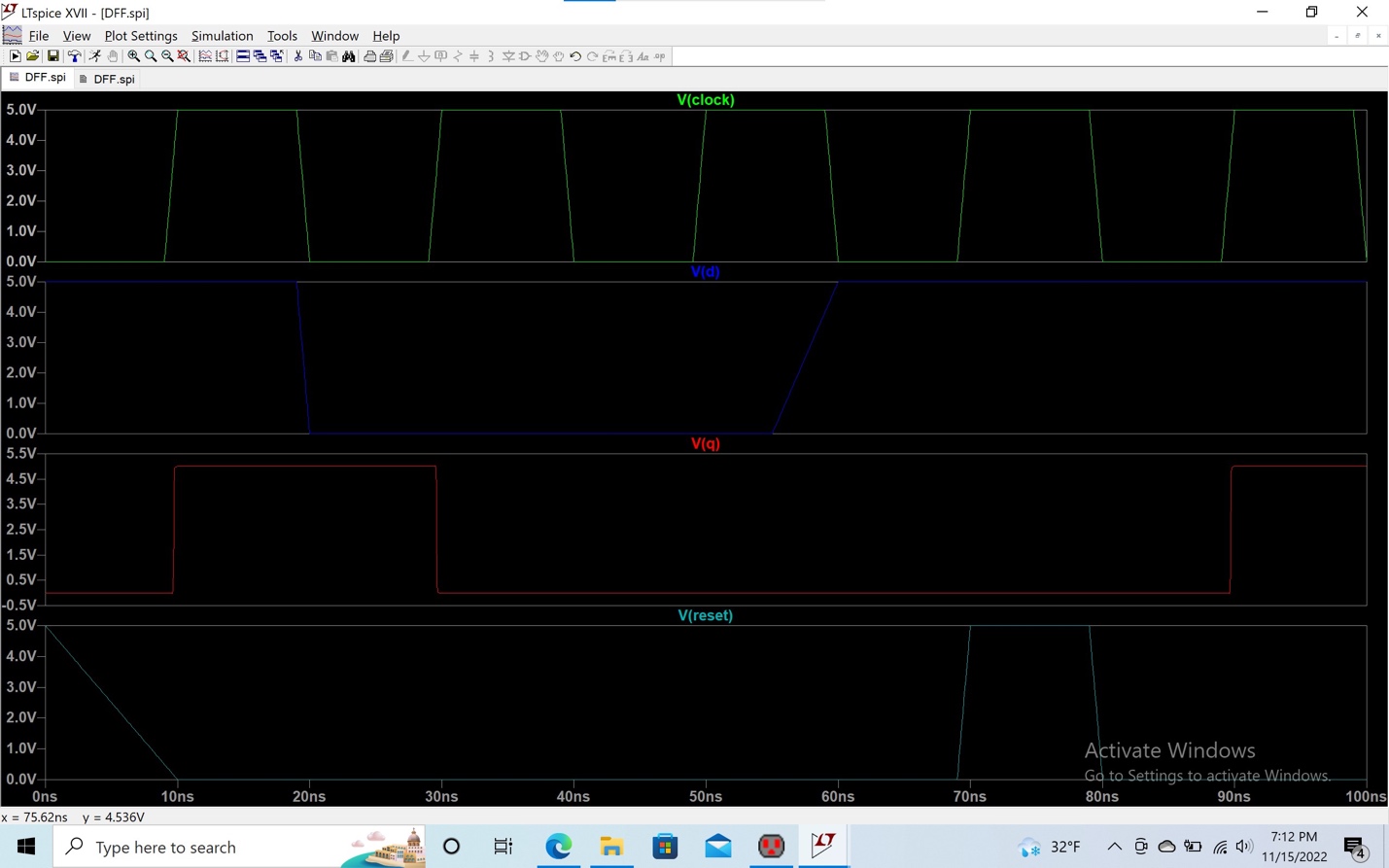


Passing DRC

Diagram, schematic

Description automatically generated

Schematic Simulation



DFF Layout

Graphical user interface

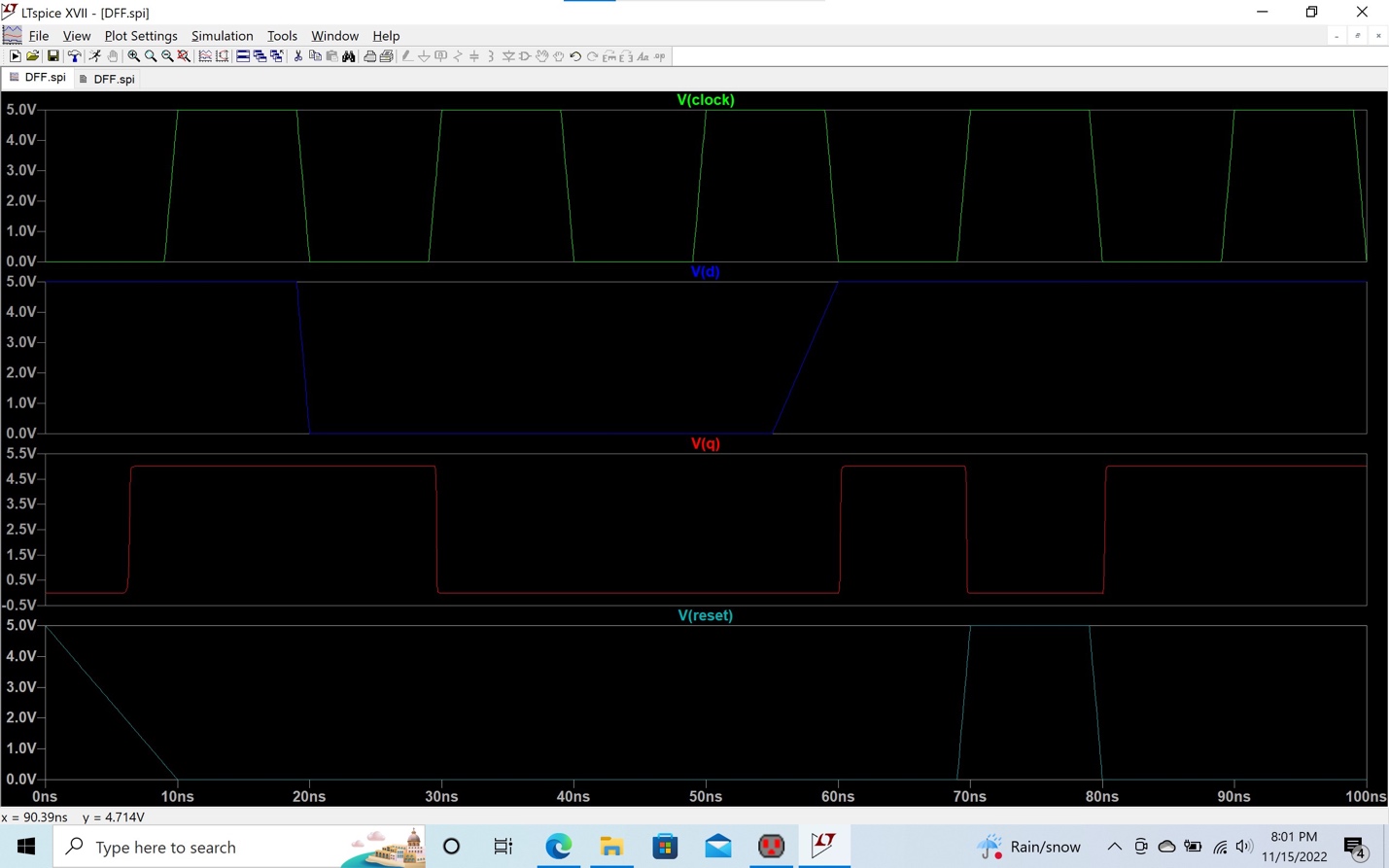
Description automatically generated

Passing ERC and DRC

Graphical user interface

Description automatically generated

Layout Simulation



The output Q for the layout is a little different than the output Q for the schematic. The output Q goes high around 10ns earlier than it goes high in the schematic simulation. Also, Q goes high right before the reset signal goes high whereas in the schematic simulation this doesn’t happen. For some reason Q is not sampling D at the rising edges of the clock like it had in the schematic. I can conclude that the layout just does not provide good simulation readings.

NRC Check

Graphical user interface, text

Description automatically generated

Another issue I had was with the NRC check. I was not able to get my schematic and layout to pass the NRC check. I have an issue where there is an unequal number of parts in my schematic and layout. Again, I am not sure how this could be possible because for my layout I build it mimicking my schematic so I am not sure how there can be a different number of parts. I then have almost double the wires in the schematic versus the layout. I am not sure how this happened, but I will investigate it prior to moving towards the next milestone.