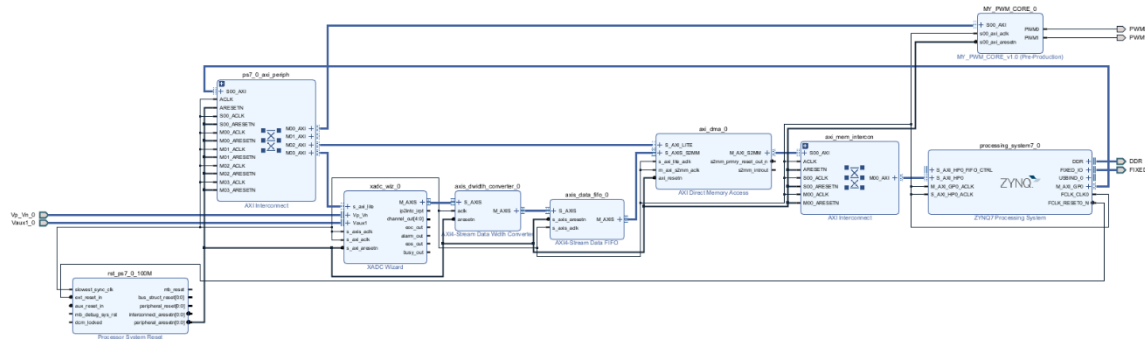


Explanation of the IP Blocks in the Design



This Vivado block diagram integrates multiple IP (Intellectual Property) cores that handle various functionalities such as PWM generation, data acquisition (ADC), AXI communication, and DMA-based data transfer. Below is a breakdown of each IP core in the design.

ZYNQ Processing System (`processing_system7_0`)

- Configures and controls all peripherals using the AXI interface.
- Processes ADC data from the current sensor.
- Manages memory (DDR) and handles AXI transactions.

AXI Interconnect (`axi_mem_intercon`, `ps7_0_axi_periph`)

- Manages AXI transactions between the ZYNQ Processing System (PS) and peripherals (PWM, ADC, and DMA).
- Ensures smooth data movement between memory-mapped AXI and AXI-Stream interfaces.
- Connects multiple AXI masters/slaves (e.g., Processor ↔ PWM Core, DMA ↔ DDR).

XADC Wizard (`xadc_wiz_0`)

- Reads analog input signals from Vp_vn and Vaux1 (current sensor output).
- Converts analog voltage to digital values.
- Outputs data over an AXI-Stream interface (`M_AXIS`) to be further processed.

AXI-Stream Data Width Converter (`axis_dwidth_converter_0`)

- Converts ADC data width (the number of bits used to represent a digital sample of an analog signal) to match downstream components.
- Ensures compatibility between XADC Wizard and FIFO/DMA.
- Helps maintain data integrity when transferring high-speed sampled data.

AXI-Stream Data FIFO (`axis_data_fifo_0`)

- Temporarily buffers ADC data before passing it to AXI DMA.
- Helps smooth out variations in data flow and prevents data loss.
- Uses handshaking signals to control data flow.

AXI Direct Memory Access (`axi_dma_0`)

- Transfers ADC data from FIFO to DDR memory.
- Operates in AXI-Stream to Memory-Mapped mode (`S2MM`).
- Uses AXI-Lite interface (`S_AXI_LITE`) for configuration.
- Ensures high-speed data movement without excessive CPU load.

PWM Core (`MY_PWM_CORE_0`)

- Generates two PWM signals (`PWM0` , `PWM1`), one is inverted and phase shifted.
- Uses an AXI interface (`S00_AXI`) to receive duty cycle updates.
- Drives the H-Bridge, which controls a motor or inductive load.
- Can be adjusted dynamically by the processor based on current sensor feedback.

Processor System Reset (`rst_ps7_0_100M`)

- Manages global resets for all peripherals.
- Ensures proper initialization of the system at startup.
- Handles clock domain synchronization.