Register File Circuit Diagram

LoadEnable

DECODER
4x16

decenable

Output de Decoder

$address_0$ $address_1$ $address_2$ $address_3$

Address0 Address1 Address2 Address3

Bus De Address
viene de salida
de un multiplexer

$OutdeDec_0$ $OutdeDec_1$ $OutdeDec_2$ $OutdeDec_3$ $OutdeDec_4$ $OutdeDec_5$ $OutdeDec_6$ $OutdeDec_7$ $OutdeDec_8$ $OutdeDec_9$ $OutdeDec_{10}$ $OutdeDec_{11}$ $OutdeDec_{12}$ $OutdeDec_{13}$ $OutdeDec_{14}$ $OutdeDec_{15}$

REGISTER R0
REGISTER R1
REGISTER R2
REGISTER R3
REGISTER R4
REGISTER R5
REGISTER R6
REGISTER R7
REGISTER R8
REGISTER R9
REGISTER R10
REGISTER R11
REGISTER R12
REGISTER R13
REGISTER R14
REGISTER R15

CLK
CLEAR
ENABLE

Q_{31} Q_1 Q_0
D_{31} D_1 D_0
DIn_{31} DIn_1 DIn_0
In_{31} In_1 In_0

MUX1

A_{31} A_1 A_0 B_{31} B_1 B_0 C_{31} C_1 C_0 D_{31} D_1 D_0 E_{31} E_1 E_0 F_{31} F_1 F_0 G_{31} G_1 G_0 H_{31} H_1 H_0 I_{31} I_1 I_0 J_{31} J_1 J_0 K_{31} K_1 K_0 L_{31} L_1 L_0 M_{31} M_1 M_0 N_{31} N_1 N_0 O_{31} O_1 O_0 P_{31} P_1 P_0

sel_0 sel_1 sel_2 sel_3

O_0 O_1 O_{31}

$RFOut1_0$ $RFOut1_1$ $RFOut1_{31}$

MUX2

$RFOut2_0$ $RFOut2_1$ $RFOut2_{31}$