Documentatie

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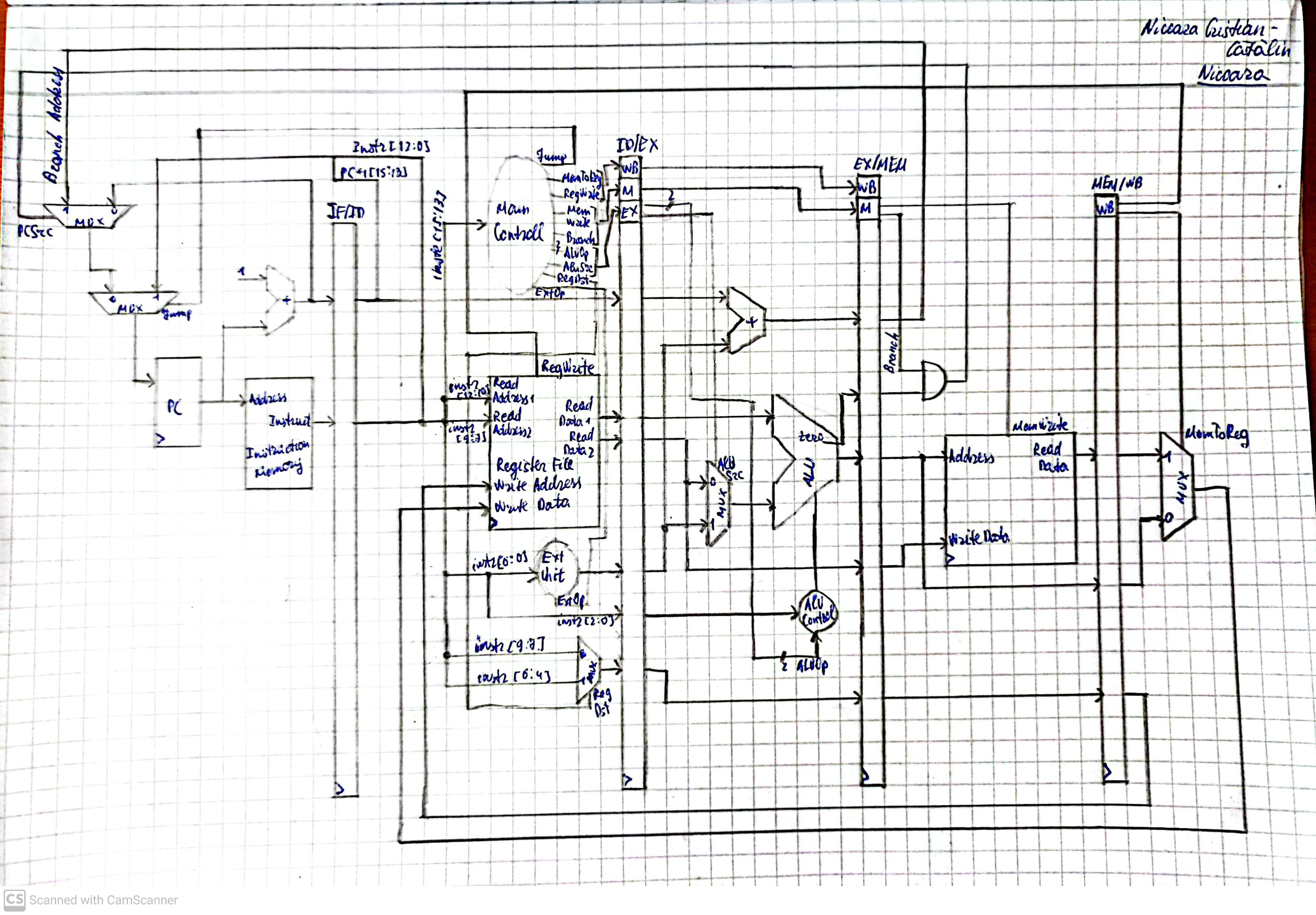
1. *Instructiuni suplimentare*

Intructiunile suplimentare alese sunt : MUL, XOR, XORI, SUBI. Pentru procesorulpipeline nu am facut modificari asupra lor.

1. *Tabelul cu descrieirea registrilor pipeline*

|  |  |  |  |
| --- | --- | --- | --- |
| **IF/ID** | **ID/EX** | **EX/MEM** | **MEM/WB** |
| instr\_if\_id(16) | pc\_next\_id\_ex(16) | MemToReg\_ex\_mem(1) | RegWrite\_mem\_wb(1) |
| pc\_next\_if\_if(16) | rd1\_id\_ex(16) | RegWrite\_ex\_mem(1) | MemToReg\_mem\_wb(1) |
| final\_wa\_if\_id(3) | rd2\_id\_ex(16) | MemWrite\_ex\_mem(1) | MemData\_mem\_wb(16) |
|  | ext\_imm\_id\_ex(16) | Branch\_ex\_mem(1) | ALURes\_out\_mem\_wb(16) |
|  | func\_id\_ex(3) | zero\_ex\_mem(1) | final\_wa\_mem\_wb(3) |
|  | sa\_id\_ex(1) | final\_wa\_ex\_mem(3) |  |
|  | ALUSrc\_id\_ex(1) | branchAdress\_ex\_mem(16) |  |
|  | Branch\_id\_ex(1) | AluRes\_ex\_mem(16) |  |
|  | MemWrite\_id\_ex(1) | AluRes\_out\_ex\_mem(16) |  |
|  | MemToReg\_id\_ex(1) | MemData\_ex\_mem(16) |  |
|  | zero\_id\_ex(1) |  |  |
|  | RegWrite\_id\_ex(1) |  |  |
|  | ALUOp\_id\_ex(2) |  |  |
|  | final\_wa\_id\_ex(3) |  |  |
|  | AluRes\_id\_ex(16) |  |  |
|  | branchAdress\_id\_ex(16) |  |  |

1. *Schema procesorului MIPS Pipeline*



1. *Analiza*

**Cod original:**

0 ADDI R2,R0,50 – Se observa un hazard RAW dupa registrul R2 cu instructiunea urmatoare

1 ADDI R2,R2,1 – Se observa un hazard RAW dupa registrul R2 cu intructiunea BEQ

2 ADDI R1,R0,1 – Se observa un hazard RAW dupa registrul R1 cu instructiunea BEQ

3 BEQ R1,R2,8 – Se observa un hazard de control (HC1)

4 ADDI R7,R1,1 – Se observa un hazard RAW dupa registrul R7 cu instructiunea BEQ

5 XORI R6,R1,1 – Se observa un hazard RAW dupa registrul R6 cu instructiunea BEQ

6 BEQ R7,R6,2 – Se observa hazard de control (HC2)

7 ADD R5,R5,R1

8 J 10 – Se observa hazard de control (HC3)

9 ADD R4,R4,R1

10 ADDI R1,R1,1

11 J 3 - Se observa hazard de control (HC4)

12 SW R4,2(R0)

13 SW R5,3(R0)

**Cod rectificat:**

0 ADDI R2,R0,50 14 ADDI R0,R0,R0

1 ADDI R0,R0,0 15 BEQ R7,R6,5

2 ADDI R0,R0,0 16 ADDI R0,R0,R0

3 ADDI R2,R2,1 17 ADDI R0,R0,R0

4 ADDI R1,R0,1 18 ADDI R0,R0,R0

5 ADDI R0,R0,R0 19 J 22

6 ADDI R0,R0,R0 20 ADD R5,R5,R1

7 BEQ R1,R2,17 21 ADD R4,R4,R1

8 ADDI R0,R0,R0 22 ADDI R1,R1,1

9 ADDI R0,R0,R0 23 J 7

10 ADDI R0,R0,R0 24 ADDI R0,R0,0

11 ADDI R7,R1,1 25 SW R4,2(R0)

12 XORI R6,R1,1 26 SW R5,3(R0)

13 ADDI R0,R0,R0

**!** Pentru a rezolva hazardul de control de la linia 8 din codul original, am facut swap intre liniile 7 si 8.

**!!** Am pus cate doua NoOp la hazardurile RAW, deoarce am schimbat in blocul de registre ca scrierea sa se faca la falling\_edge().

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instr\Clk | CC1 | CC2 | CC3 | CC4 | CC5 | CC6 | CC7 | CC8 | CC8 | CC10 | CC11 |
| ADDI R2,R0,50 | IF | ID | EX | MEM | **WB**(R2) |  |  |  |  |  |  |
| ADDI R2,R2,1 |  | IF | **ID**(R2) | EX | MEM | **WB**(R2) |  |  |  |  |  |
| ADDI R1,R0,1 |  |  | IF | ID | EX | MEM | **WB**(R1) |  |  |  |  |
| BEQ R1,R2,8 |  |  |  | IF | **ID**(R1,R2) | EX | **MEM**(HC1) | WB |  |  |  |
| ADDI R7,R1,1 |  |  |  |  | **IF**(HC1) | ID | EX | MEM | **WB**(R7) |  |  |
| XORI R6,R1,1 |  |  |  |  |  | **IF**(HC1) | ID | EX | MEM | **WB**(R6) |  |
| BEQ R7,R6,2 |  |  |  |  |  |  | **IF**(HC1) | **ID**(R7,R6) | EX | **MEM**(HC2) | WB |

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instr\Clk | CC8 | CC9 | CC10 | CC11 | CC12 | CC13 | CC14 | CC15 | CC16 | CC17 | CC18 |
| ADD R5,R5,R1 | **IF**(HC2) | ID | EX | MEM | WB |  |  |  |  |  |  |
| J 10 |  | **IF**(HC2) | **ID**(HC2,HC3) | EX | MEM | WB |  |  |  |  |  |
| ADD R4,R4,R1 |  |  |  | ID | EX | MEM | WB |  |  |  |  |
| ADDI R1,R1,1 |  |  |  | IF | ID | EX | MEM | WB |  |  |  |
| J 3 |  |  |  |  | IF | **ID**(HC4) | EX | MEM | WB |  |  |
| SW R4,2(R0) |  |  |  |  |  | **IF**(HC4) | ID | EX | MEM | WB |  |
| SW R5,3(R0) |  |  |  |  |  |  | IF | ID | EX | MEM | WB |

1. *Testare*

Am testat procesorul pe placa si mergea bine.