Cristian Tirelli

Contacts

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Research Interest

My research focuses on compilers and optimization techniques for hardware accelerators, with a particular emphasis on Coarse-Grained Reconfigurable Arrays (CGRAs) and circuit-level synthesis. I am especially interested in mapping problems, structural representations of computation, and the trade-offs between solution quality and scalability. My work combines formal methods, algorithm design, and low-level hardware reasoning to make specialized architectures more programmable and efficient.

Education

Università della Svizzera italiana (USI) Lugano, CH
PhD** student under the supervision of **Laura Pozzi *May 2021 – Present*

University of California Los Angeles (UCLA) Los Angeles, USA
Visiting researcher** under the supervision of **Jason Cong** and **Tony Nowatzki *Sept. 2023 – May 2024*

University of Cassino and Southern Lazio (UNICAS) Cassino, IT
Master's degree in computer engineering obtained with **110 cum laude** *Feb. 2018 – May 2020*
Thesis project on the cryptanalysis of a fast variant of the QUAD cryptosystem and the study of regularity properties for those kind of high-degree nonlinear systems.

Work Experience

Visiting Researcher (UCLA) Los Angeles, USA
Visiting researcher under the supervision of **Jason Cong** and **Tony Nowatzki** *Sept. 2023 – May 2024*
Integration of Systolic Array Compiler into Chipyard toolchain. Development of a decision making algorithm leveraging simple hardware abstractions. Research on scalable mapping techniques for CGRAs accelerators.

PhD Student (USI) Lugano, CH
PhD student under the supervision of **Laura Pozzi** *May 2021 – Present*
Research focus on compilers and optimization techniques for hardware accelerators. Published several paper in top conferences and journals, and developed multiple CGRA compilers

Spike Reply June 2020 – April 2021
Security Consultant *Milan, IT*
Responsible for various penetration testing activities, primarily focused on web applications. This role involved gaining technical expertise with a range of technologies and tools, while improving reporting and communication skills with clients. Additionally, mentored and trained new employees to support their integration and skill development.

Crypt-Security Oct. 2018 – Feb. 2019
Cryptography Consultant *Rome, IT*
Responsible for analyzing custom security algorithms, evaluating their mathematical properties and theoretical security. Cryptographic weaknesses were identified, and improvements were proposed to enhance speed, security, and statistical properties.

Projects

SAT Based Compiler for CGRAs

***GitHub**: SAT-MapIt*

- Developed a compiler for Coarse Grained Reconfigurable Arrays (CGRAs), with back-end support for CGRA-X-HEEP developed by EPFL. Proposed a SAT based approach used to completely abstract the Modulo Scheduling problem for CGRAs.
- The toolchain was built on top of Clang, with modifications to its front-end to support loop extraction via a custom pragma. An LLVM IR pass was implemented to gather the necessary information for optimization and transformation. Finally, a custom back-end has been developed to support code generation and register allocation, specifically tailored to our target architecture.

Monomorphism Based Compiler for CGRAs

***GitHub**: Mono-MapIt*

- Developed a compiler for Coarse Grained Reconfigurable Arrays (CGRAs), with greater scalability properties compared to SAT-MapIt. Proposed a novel approach to decouple time a space dimensions to further improve the State of the Art of CGRA compilers.
- The toolchain was built on top of Clang, with modifications to its front-end to support loop extraction via a custom pragma. An LLVM IR pass was implemented to gather the necessary information for optimization and transformation.

SubXPAT

***GitHub**: SubXPAT*

- Made several contribution to the SubXPAT project. Responsible of the subgraph extraction algorithm.

Technical Expertise

Programming Languages: C, C++, Python, Assembly (x86, ARM)

Skills: Compilers, Polyhedral Compilation, Optimizations, Computer Architecture, Graph Theory, Optimization, Algorithms, Data Structure

Tools & Libraries: Clang, CMake, GCC, LLVM, MLIR, Z3, IDA Pro, Ghidra, x86dbg, VMware, Burp Suite, Wireshark

Teaching Assistant

Computer Architectures and Logic Design Spring Semester 2025

- Correct and prepare assignments, hold lab activities, supervise exams and assist students throughout the course.

Programming Fundamentals for Data Science Fall Semester 2024 & 2025

- Correct and prepare assignments, hold lab activities, supervise exams and assist students throughout the course.

Automata & Formal Languages Fall Semester 2021 & 2022

- Correct assignments, supervise exams and assist students throughout the course.

Information Security Spring Semester 2021 & 2022

- Create and grade assignments and exams. Prepare lab activities, help students during the course, and supervise exams.

Student Supervision

Bachelor Thesis

Università della Svizzera italiana, Switzerland

Student: Marco Biasion (2023)

Thesis: Register Spilling for Coarse-Grained Reconfigurable Array Architectures

Master Thesis

Università della Svizzera italiana, Switzerland & University of Erlangen–Nuremberg, Germany

Student: Uslu Muhammet (2023)

Thesis: Compiler Techniques for Optimizing Energy Efficiency in Deep Neural Networks on Systolic Arrays: A Simulation-Based Approach

PhD Supervision

École Polytechnique Fédérale de Lausanne (EPFL), Switzerland
Student: Yuxuan Wang (2024)
Topic: Optimizing CGRA memory transfers

Internship Projects

Università della Svizzera italiana, Switzerland
Student: Arnaud Fauconnet (2024)
Topic: Statistical Analysis of CGRA mappings

Master Thesis

Università della Svizzera italiana, Switzerland & Politecnico di Milano, Italy
Student: Andrea Ortenzi (2025)
Thesis: Optimizing Machine Learning Workloads: unleashing FPGA tensor cores through MLIR

Funding and Academic Service

- Authored and awarded a PhD Mobility Grant of 20,000 CHF from the Swiss National Science Foundation (SNSF), supporting my research stay as a visiting scholar at UCLA.
- Served as a sub-reviewer for TCAD'23, TCAD'24, SSCL'25, TETC'25.
- Member of the artifact evaluation committee for CASES'25
- Member of the hiring committee for an assistant professor position in security at USI.

List of Publications

[1] **Cristian Tirelli**, Lorenzo Ferretti, and Laura Pozzi. *SAT-MapIt: A SAT-based Modulo Scheduling Mapper for Coarse Grain Reconfigurable Architectures.* Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (2023), 1–6.

[2] **Cristian Tirelli**, Lorenzo Ferretti, and Laura Pozzi. *SAT-MapIt: An Open Source Modulo Scheduling Mapper for Coarse Grain Reconfigurable Architectures.* Proceedings of the 20th ACM International Conference on Computing Frontiers

[3] **Cristian Tirelli**, Juan Sapriza, Rubén Rodríguez Álvarez, Lorenzo Ferretti, Benoît Denkinger, Giovanni Ansaloni, José Miranda Calero, David Atienza, Laura Pozzi. *SAT-based Exact Modulo Scheduling Mapping for Resource-Constrained CGRAs.* Journal on Emerging Technologies in Computing Systems (2024), 1–24.

[4] **Cristian Tirelli**, Rodrigo Otoni, and Laura Pozzi. *Monomorphism-based CGRA Mapping via Space and Time Decoupling.* Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (2025), 1–6.

[5] Yuxuan Wang, **Cristian Tirelli**, Lara Orlandic, Juan Sapriza, Rubén Rodríguez Álvarez, Giovanni Ansoloni, Laura Pozzi, David Atienza. *An MLIR-based Compilation Framework for CGRA Application Deployment.* International Symposium on Applied Reconfigurable Computing (2025), 1–6.

[6] Yuxuan Wang, **Cristian Tirelli**, Giovanni Ansoloni, Laura Pozzi, David Atienza. *An MLIR-based Compilation Framework for Control Flow Management on CGRAs..* arXiv preprint arXiv:2508.02167 (2025). 1–26.