Kyle Elder

Professor Georgiou

CSE-313

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Homework #2

**4.5b**- **Question:** The binary value within each location can be interpreted in many ways. We have seen that binary values can represent unsigned numbers, 2’s complement signed numbers, floating point numbers, and so forth.

**Answer:**

**1.**

0001111001000011 = 7747

1111000000100101 = -4059

**2.**

0000 0000 0110 0101 = e

**3.**

0000 0110 1101 1001 1111 1110 1101 0011 = 1.10110011111111011010011 \* 2^-114

**4.**

0001111001000011 = 7747

1111000000100101 = 61477

**4.8**- **Question:** If there are 225 opcodes and 120 registers,

a. What is the minimum number of bits required to represent the OPCODE?

b. What is the minimum number of bits required to represent the Destination Register?

c. What is maximum number of UNUSED bits in the instruction encoding?

**Answer:**

a. The minimum number of bits required to represent the OPCODE is 8.

b. The minimum number of bits required to represent the Destination Register is 7.

c. The maximum number of UNUSED bits in the instruction encoding is 3.

**4.11**- **Question: A.** State the phases of the instruction cycle and briefly describe what operations occur in each phase.

**Answer:**

Fetch- Obtains the next instruction from memory and loads it into the instruction register of the control unit.

Decode- Examines the instruction in order to figure out what the microarchitecture is being asked to do.

Evaluate Address- Computes the address of the memory location that is needed to process the instruction.

Fetch Operands- Obtains the source operands needed to process the instruction.

Execute- Carries out the execution of the instruction.

Store Result- Final phase of an instruction’s execution. The result is written to its designated destination

**5.5**- **Question:**

**A.** What is an addressing mode?

**B.** Name three places an instruction’s operands might be located.

**C.** List the five addressing modes of the LC-3, and for each one state where the operand is located.

**D.** What addressing mode is used by the ADD instruction shown in Section 5.1.2?

**Answer:**

**A.** A mechanism for specifying where the operand is located.

**B.** The operands are located in a register, in memory, or as an Immediate.

**C.** Immediate: Locate in instruction

Register: Located in a register

Direct Memory Address: Look at operands to locate in memory

Indirect Memory Address: Look at operands to locate in memory

Base + Offset Address: Look at operands to locate in memory.

**D.** Register addressing mode.

**5.9**- We would like to have an instruction that does nothing. Many ISAs actually have an opcode devoted to doing nothing. It is usually called NOP, for NO OPERATION. The instruction is fetched, decoded, and executed. The execution phase is to do nothing! Which of the following three instructions could be used for NOP and have the program still work correctly? What does the ADD instruction do that the others do not do?

**Answer:**

**A.** 0001 001 001 1 00000- **Incorrect**

This add instruction takes a destination register and sets a condition code.

**B.** 0000 111 000000001- **Cannot be used for NOP**

**C.** 0000 000 000000000- **Can be used for NOP**

**5.15**- State the contents of R1, R2, R3, and R4 after the program starting at location x3100 halts.

**Answer:**

**R1-** LEA x3100+1+x20 = **x3121**

**R2-** LD x3101+1+x20 = M[x3122] = **x4566**

**R3-** LDI x3102+1+x20 = x3123 = M[M[x3123]] = **x4567 = xABCD**

**R4-** LDR x3102+1+x20 = x3123 = M[R2+1] = M[4567] = **xABCD**

**5.23**

**Question: Supposed the following LC-3 program is loaded into memory starting at location x30FF. If the program is executed, what is the value in R2 at the end of execution?**

**Answer:**

X30FF 1110 001 000000001 = LEA R1, #1 = x30FF+1+1 = x3101

X3100 0110 010 001 00 0010 = LDR R2, R1, #2 = M[R1+2] = x1482

X3101 1111 0000 0010 0101 = TRAP x25 “HALT”

X3102 0001 010 001 000001 = ADD R2, R1, #1

X3103 0001 010 010 000010 = ADD R2, R1, #2

**R2 = x1482**