Kyle Elder

Professor Georgiou

CSE-313

3/5/12

Homework #3

**7.4**- **Question:** Create the symbol table entries generated by the assembler when translating the following routine into machine code:

**Label Memory Address**

TEST x301F

FINISH x3027

SAVE3 x3029

SAVE4 x302A

**Answer:**

**7.9**- **Question:** What is the purpose of the .END pseudo-op? How does it differ from the HALT instruction?

**Answer:**

The HALT instruction can’t be executed and shows the program where to stop assembling.

.END is interpreted as the end of the program. Anything after the .END pseudo-op is not processed by the assembler.

**7.10**- **Question:** The following program fragment has an error in it. Identify the error and explain how to fix it.

ADD R3, R3, #30

ST R3, A

HALT

A .FILL #0

Will this error be detected when this code is assembled or when this code is run on the LC-3?

**Answer:**

The max value that can be added to a register on one line is 15. The easiest solution is to replace the first line with **ADD R3, R3, #15** and do it again on the next line. This error will be detected when this code is assembled.

**7.13**- **Question:**

The following program adds the values stored in memory locations A, B, and C, and stores the result into memory. There are two errors in the code. For each, describe the error and indicate whether it will be detected at assembly time or at run time.

**Answer:**

Line 3 tries to add R1 before it’s initialized. The error will be detected at run time.

Line 8 tries to store R1 into SUM, but SUM hasn’t been created. Since the Label hasn’t been created, this error will be detected at assembly time.

**8.2**- **Question:** Why is a Ready bit not needed if synchronous I/O is used?

**Answer:**

The ready bit isn’t necessary because the processor knows when data is input and output. It does these at constant intervals, in which data is taken by the computer and output to the device.

**8.5**- **Question:** What is the purpose of bit[15] in the KBSR?

**Answer:**

Bit[15] is the ready bit in the KBSR. The ready bit lets the processor know that input has occurred.

**8.10- Question:** What problem could occur if the display hardware does not check the DSR before writing to the DDR?

**Answer:**

If the ready bit is 1, the data in the DDR wasn’t displayed yet. Since it didn’t check the DSR before writing to the DDR, the DDR could not have a value written in it.

**8.14- Question:** An LC-3 load instruction specifies the address xFE02. How do we know whether to load from the KBDR or from memory location xFE02?

**Answer:**

Addresses in between xFE00-xFFFF are reserved for input and output. Since xFE02 is within that range, we know that it is in the KBDR.