

Regarding the usage of our schematics and alike documentation for Trenz module TE0726

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Schematics and other handouts serve for informational purposes only!



Title:		Legal Notices Modules	
A4	Number:	TE0726 41C94-A	Rev. 04
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Filename: Legal Notices Modules.SchDoc			

REV	Description	
-01	Initial revision	
-02	1. CSI CLK line moved to MRCC pin, CSI lanes swap -> DONE 2. CSI camera GPIO moved to MIO GPIO -> DONE 3. RPi GPIO 14,15 moved from MIO to PL -> DONE 4. add C for SD Card VCC (required by SD spec) 47uF ->DONE 5. add C for RPi camera - prevent voltage drop at camera init - 47uF ? or R + 47uf ->DONE 6. fix MODE pin strapping -> DONE 7. LED change 0603 (cheaper) -> DONE 8. add POWER connector 2 pin -> DONE (2pin 2.54mm) 9. change HDMI ESD to ESD+EMI -> DONE (replaced on EMI4192) 10. fix HDMI HPD and backpower? how? -> fix reset 11. DSI find solution for LS mode 12. fix XADC power caps -> DONE 13. change LPDDR2 ->> DDR3L -> DONE	
-03	1. make variants: a) default with DDR3L 128Mb; b) TE0726-03M with DDR3L 512Mb; c) TE0726-03L with DDR3L 128Mb, without usb's, eth_phy, connectors usb, RJ-45, CSI,DSI,HDMI, jack 3.5mm -> done 2. replace FTDI on 56pins package -> done 3. move LED's as raspberry pi 3 -> done 4. replace POWER connector on right angle connector -> done (not fitted) 5. make correct connection PUDC pin -> done 6. optimize BOM, replace on cheaper components -> done (replace HDMI, DSI/CSI connector, USB stacked connectors, RJ-45, power connector)	
-03a	1. VBUS Resistor R94 replaced by 10k ohm (was 12k1)	VY (08.04.2019)
-04	1. EOL components U16, U17 , U19, U20 (EN5311QI) were replaced by MPM3834CGPA; 2. Added MIC bias power L12, C114 , R151 (Page 16); 3. Added Legal notices (Page 1); 4. Added power diagram (Page 4); 5. Added S1 switch and R152 for "JTAG only mode" enable (Page 8); 6. The signals were renamed: - SPI-DQ0/M0 ---> SPI-DQ0/M3, - SPI-DQ3/M3 ---> SPI-DQ3/M0 according to AMD Table 6-4 (Page 8); 7. ECC function has been added for U8 (Page 11); 7.1 Added I2C level shifter U12 for DDR3 ECC function (Page 11); 7.2 Added Buffers U24, U25 to match the level of signals (Page 6); 7.3. Added Diode D7, resistors R155, R160. 8. EOL components L1, L2, L3, L4, L6, L7, L9, L10 BKP0603HS121-T replaced by MPZ0603S121HT000. 9. EOL components D8, D9 SP5001-04TTG replaced by EMI8042MUTAG. 10. Resistors R80-R82 replaced by 10k ohm (was 1k43). 11. Added Testpoints TP15 - TP20. 12. The type of testpoints TP1 - TP14 was updated. Diameter changed from 0.8 mm to 1 mm. 13. CEC function is not supported. L11 was removed. C127, D5, R140, R42 are DNP. 14. Power-up sequencing was updated for new DC-DC supplies. 15. Capacitors C29, C32, C33 replaced by 470nF (was 100nF).	VG (06.10.2023)
-04a	1. Removed Digilent licence (MISC1).	ED (16.06.2025)



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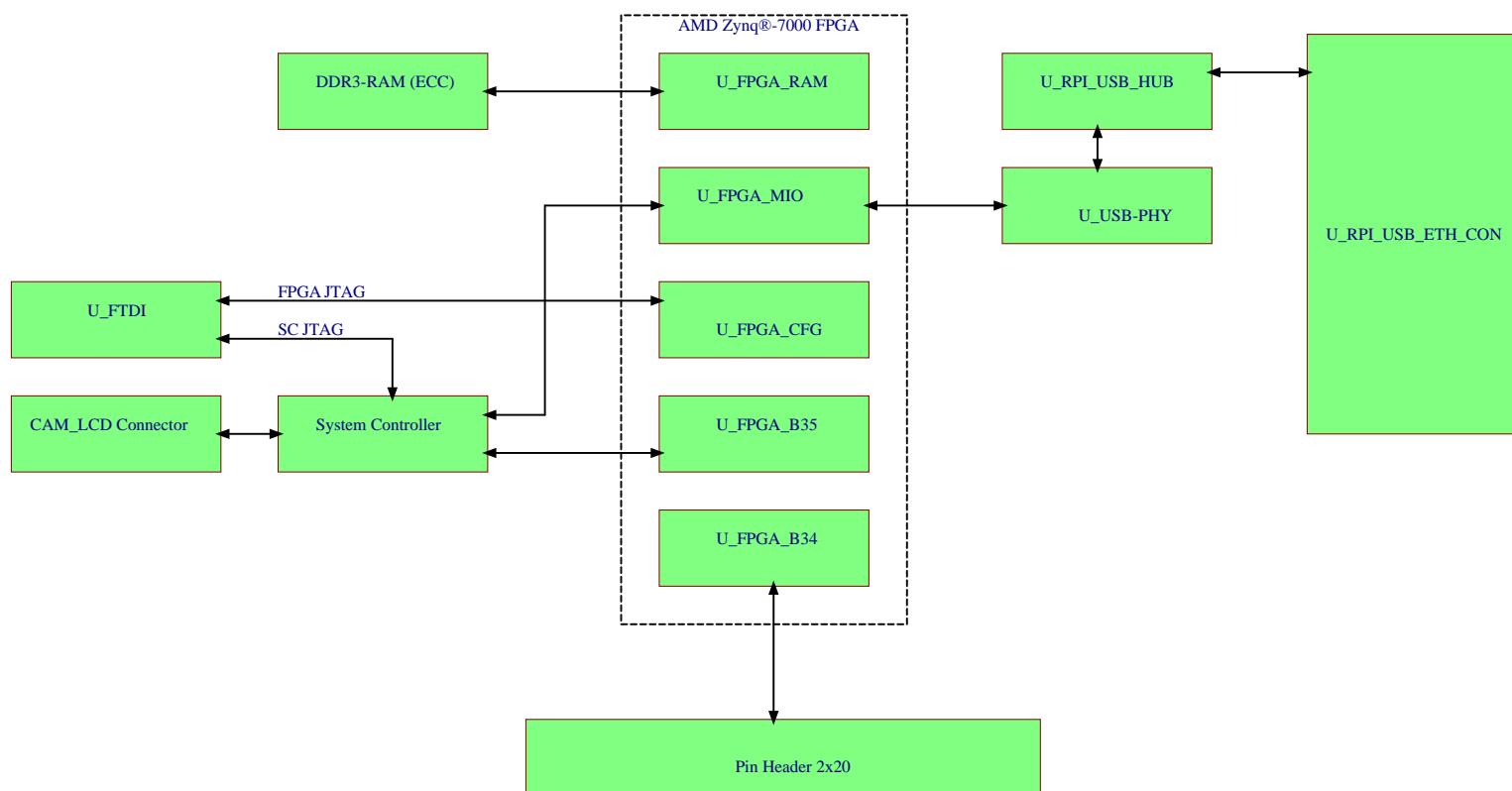
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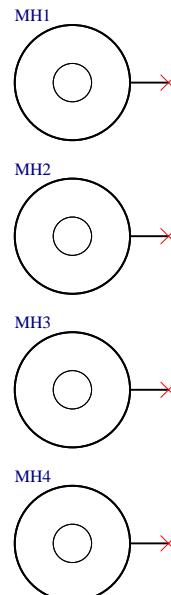
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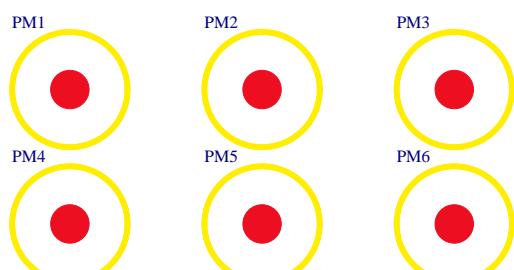
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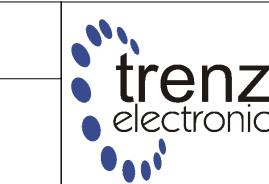


U_Power Diagram



Serial
Serial
Serialnumber 6,3 x 6.3mm

Drawn by Checked by	VG IG
Assembly variant Created by	41C94-A VG
Modified by Modified at	2023-09-28 VG



MECH1
TE Address Overlay
LOGO ADDRESS

LOGO1
TE Logo PRINT Layer
LOGO PRINT

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

Title: Overview

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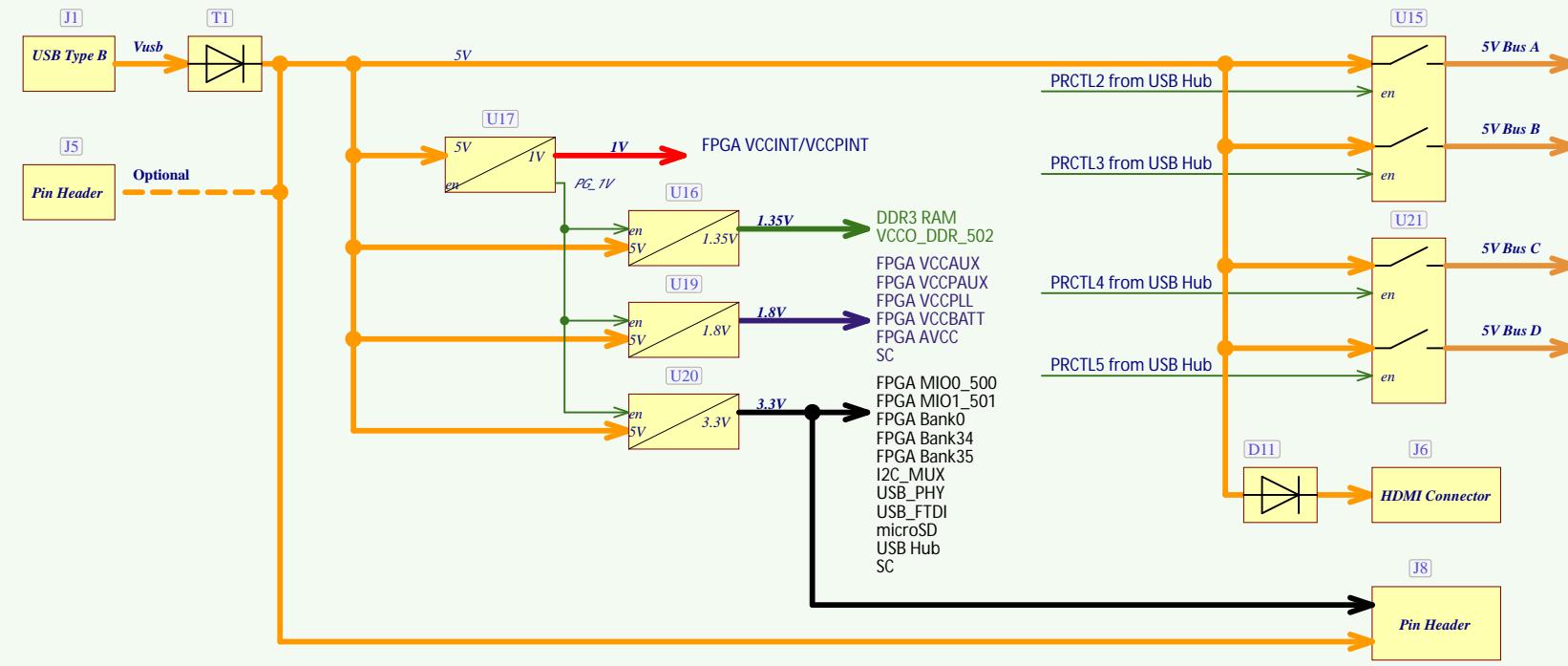
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A Power-on sequencing:

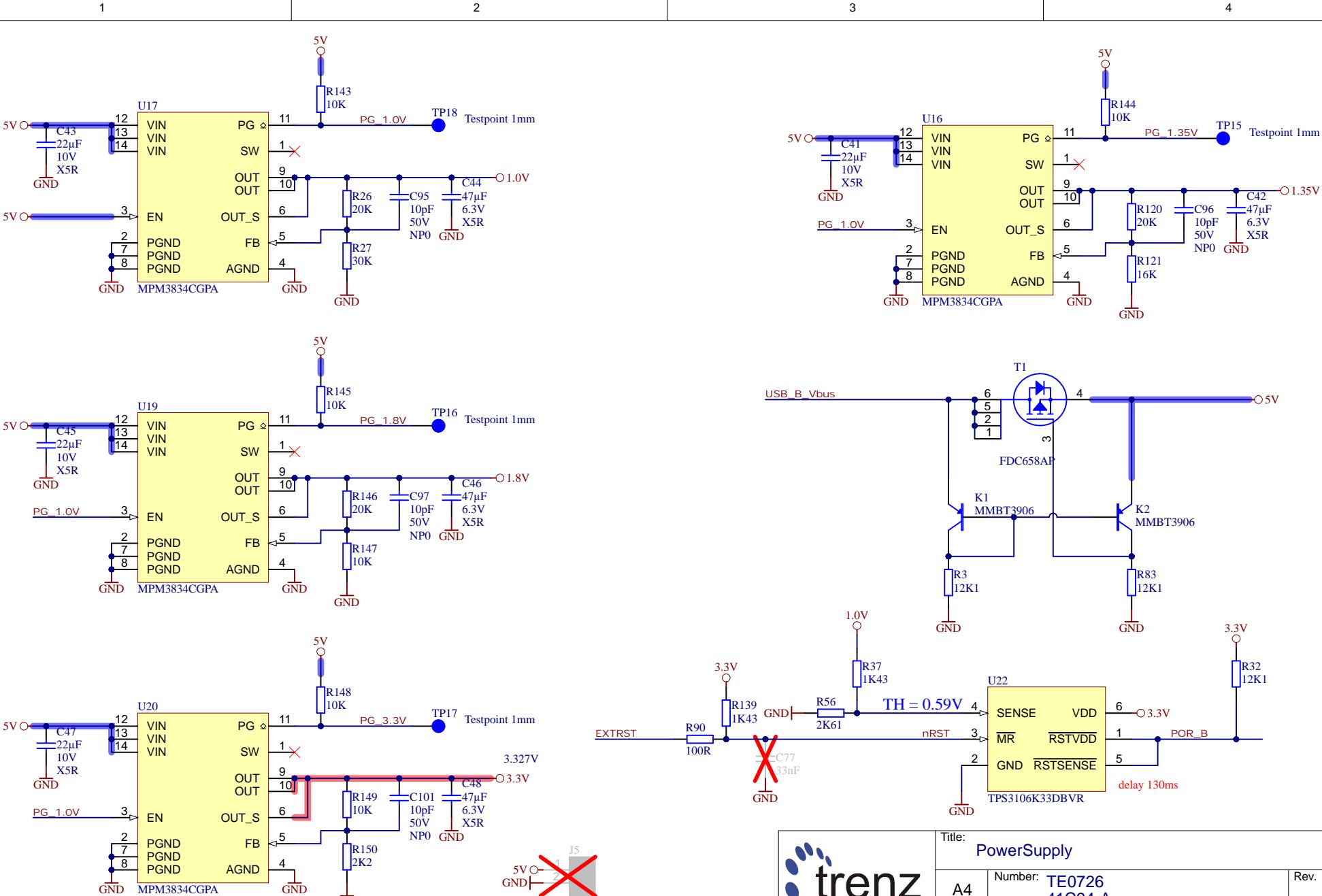


B Supported Voltage Ranges:

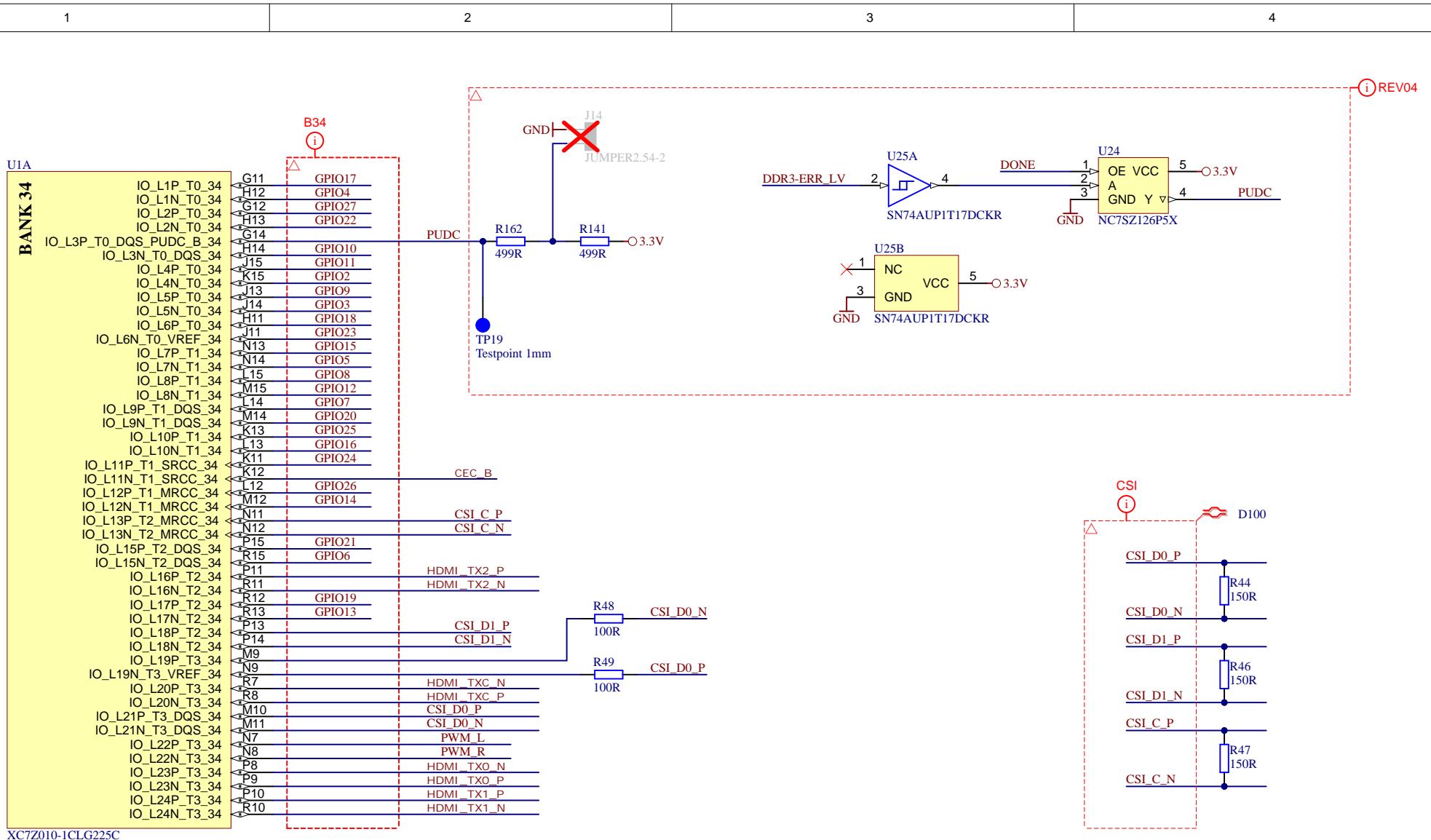
Power Rail	Direction	Range	Tolerance	Description	Note
5V	OUT	5V	+/-5%	Micromodule Power	-
USB_B_Vbus	IN	5V	+/-5%	Micromodule Power	-
3.3V	OUT	3.3V	+/-3%	Micromodule Power	-



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Title: **FPGA B34**

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i REV04

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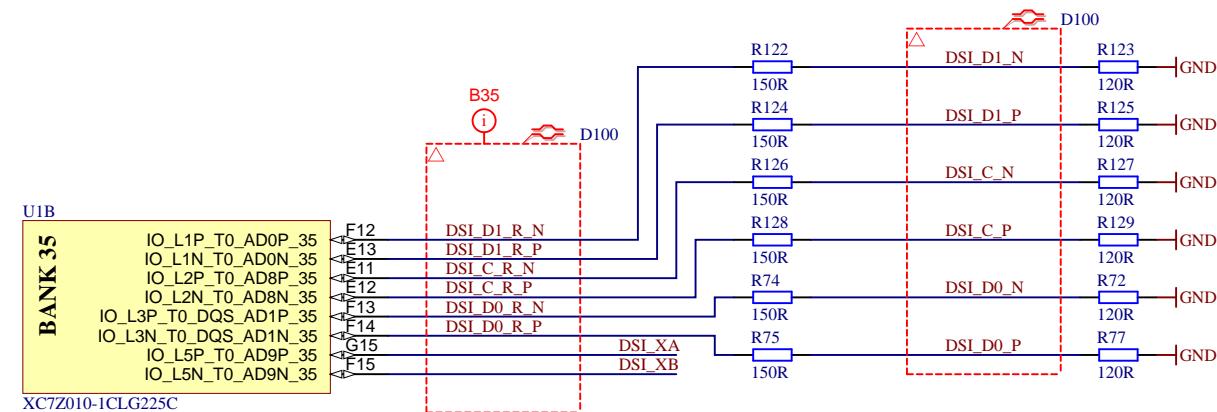
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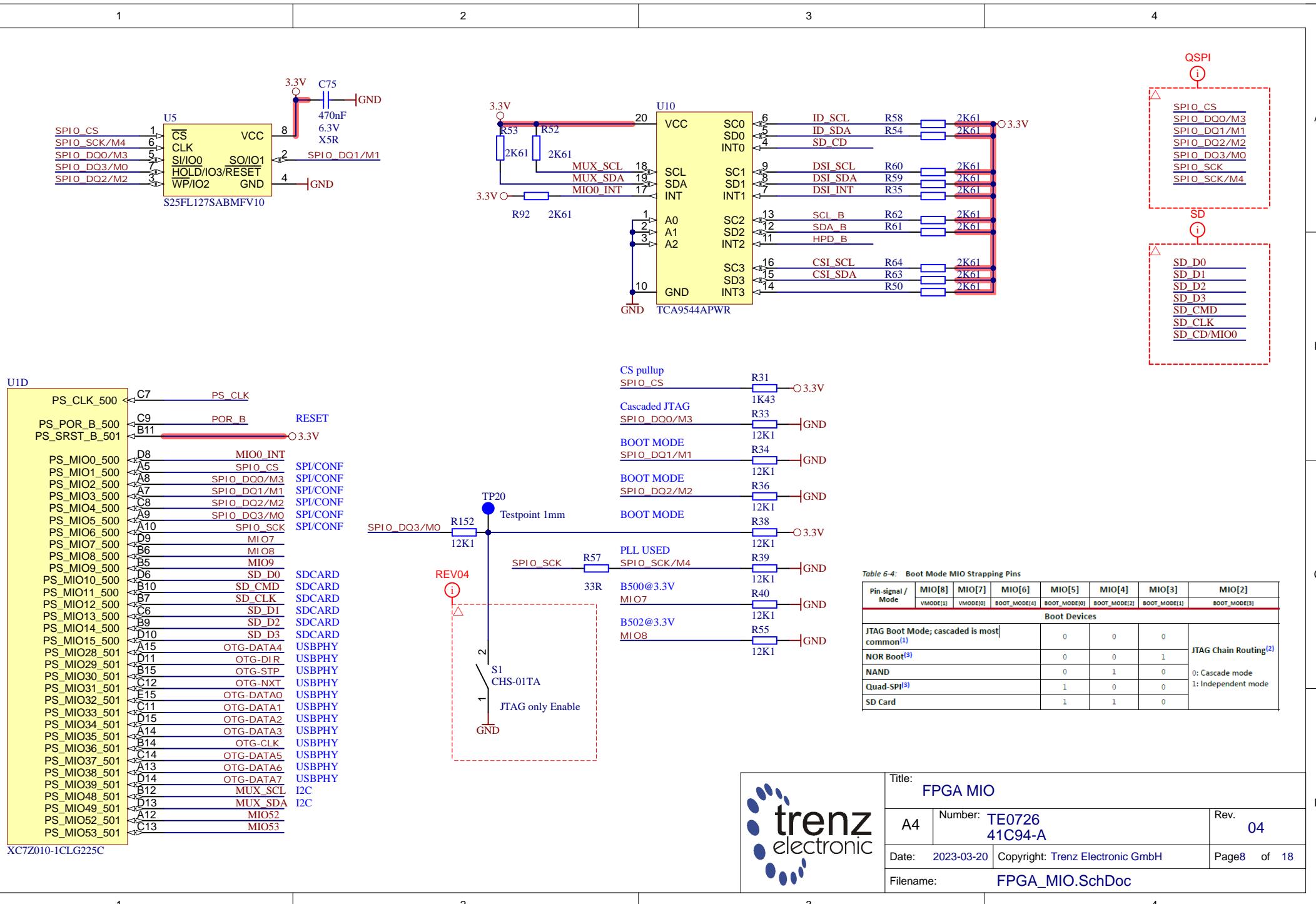
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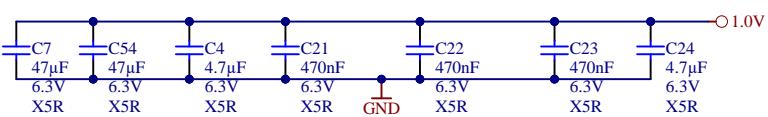
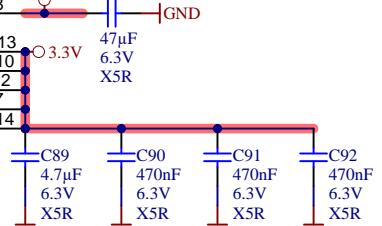
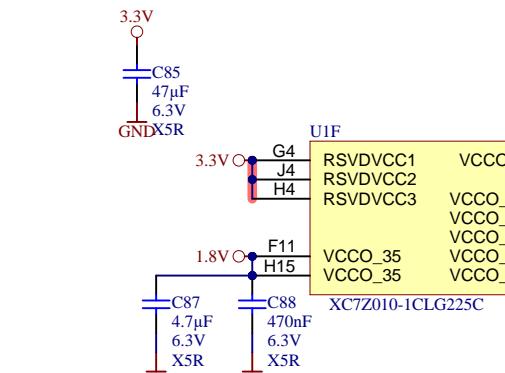
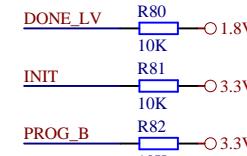
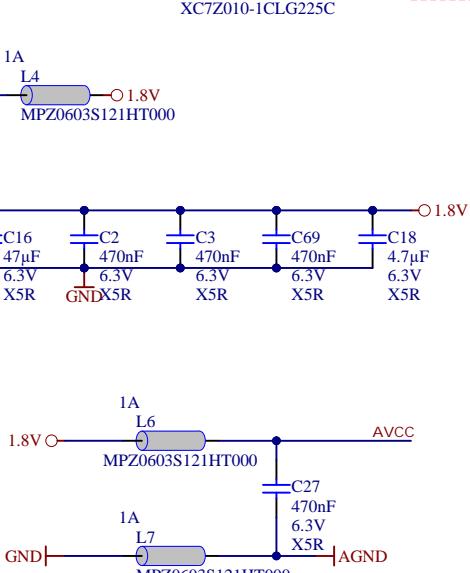
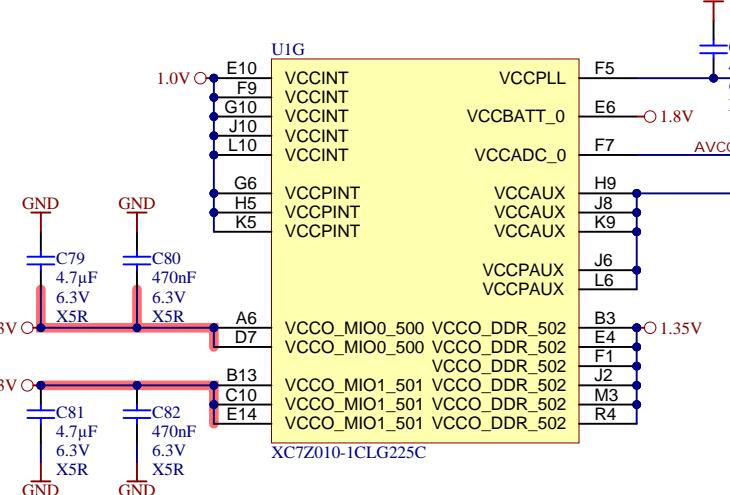
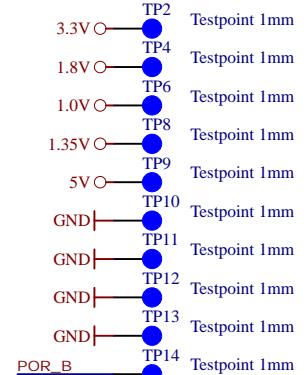
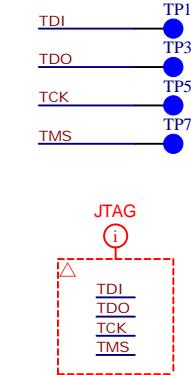
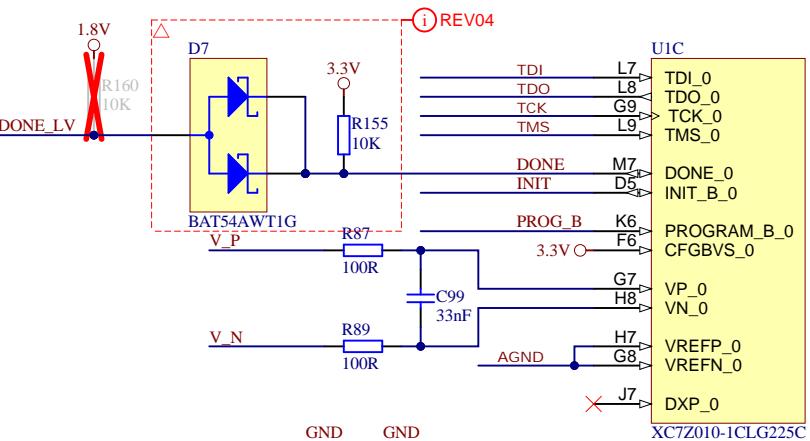
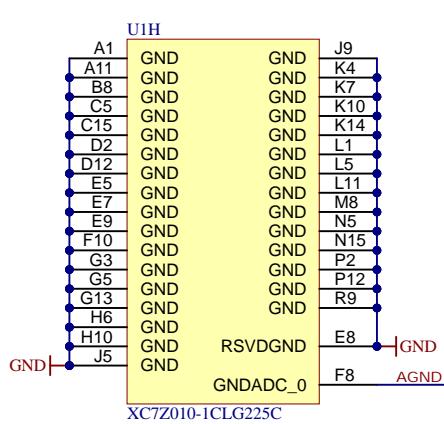
D

D



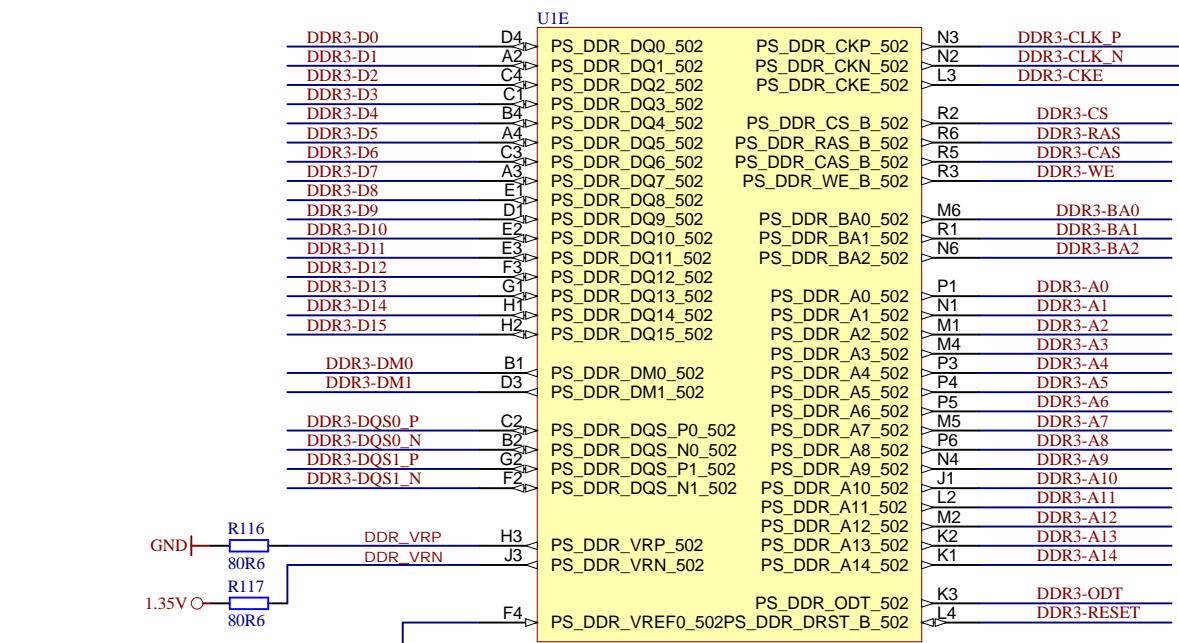
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 Trenz onic	Title: FPGA PWR		
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A



B

C

D

LANE_0

DDR3-D0, DDR3-D1, DDR3-D2, DDR3-D3, DDR3-D4, DDR3-D5, DDR3-D6, DDR3-D7, DDR3-DM0
DDR3-DQS0_P, DDR3-DQS0_N

LANE_1

DDR3-D8, DDR3-D9, DDR3-D10, DDR3-D11, DDR3-D12, DDR3-D13, DDR3-D14, DDR3-D15, DDR3-DM1
DDR3-DQS1_P, DDR3-DQS1_N

ADDR_CTRL_CMD

DDR3-CLK_P, DDR3-CLK_N	DDR3-BA0, DDR3-A1, DDR3-A8
DDR3-CKE	DDR3-BA1, DDR3-A2, DDR3-A10
DDR3-CS	DDR3-BA2, DDR3-A3, DDR3-A11
DDR3-ODT	DDR3-A4, DDR3-A12, DDR3-A10
	DDR3-A5, DDR3-A13, DDR3-A12
	DDR3-A6, DDR3-A14, DDR3-A9
	DDR3-A7

DDR_D80

DDR3-DQS0_P, DDR3-DQS0_N
DDR3-DQS1_P, DDR3-DQS1_N
DDR3-CLK_P, DDR3-CLK_N

DDR_S40

DDR3-D0, DDR3-D1, DDR3-D2, DDR3-D3, DDR3-D4, DDR3-D5, DDR3-D6, DDR3-D7, DDR3-BA0	DDR3-D8, DDR3-D9, DDR3-D10, DDR3-D11, DDR3-D12, DDR3-D13, DDR3-D14, DDR3-D15, DDR3-BA1	DDR3-DM0, DDR3-DM1, DDR3-ODT, DDR3-CKE, DDR3-CS, DDR3-RAS, DDR3-CAS, DDR3-WE, DDR3-BA1	DDR3-A0, DDR3-A1, DDR3-A8, DDR3-A1, DDR3-A10, DDR3-A2, DDR3-A11, DDR3-A3, DDR3-A11, DDR3-A4, DDR3-A12, DDR3-A5, DDR3-A6, DDR3-A7, DDR3-A8
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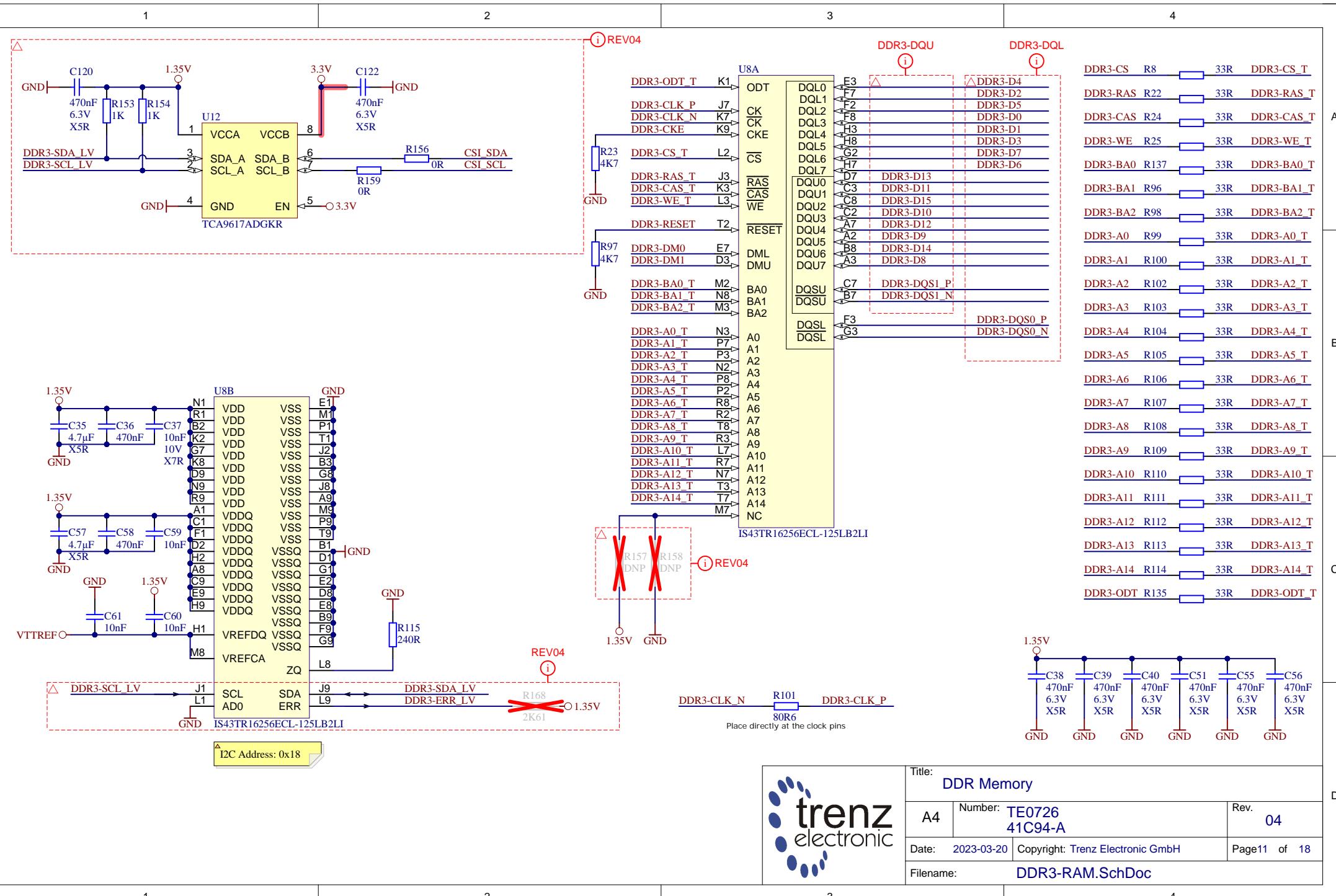
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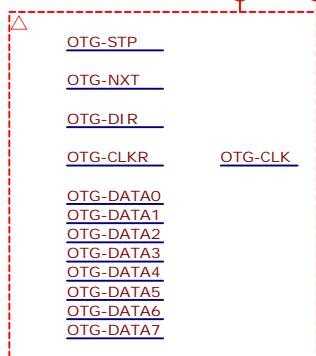
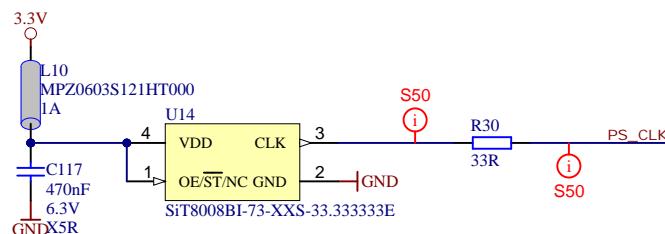
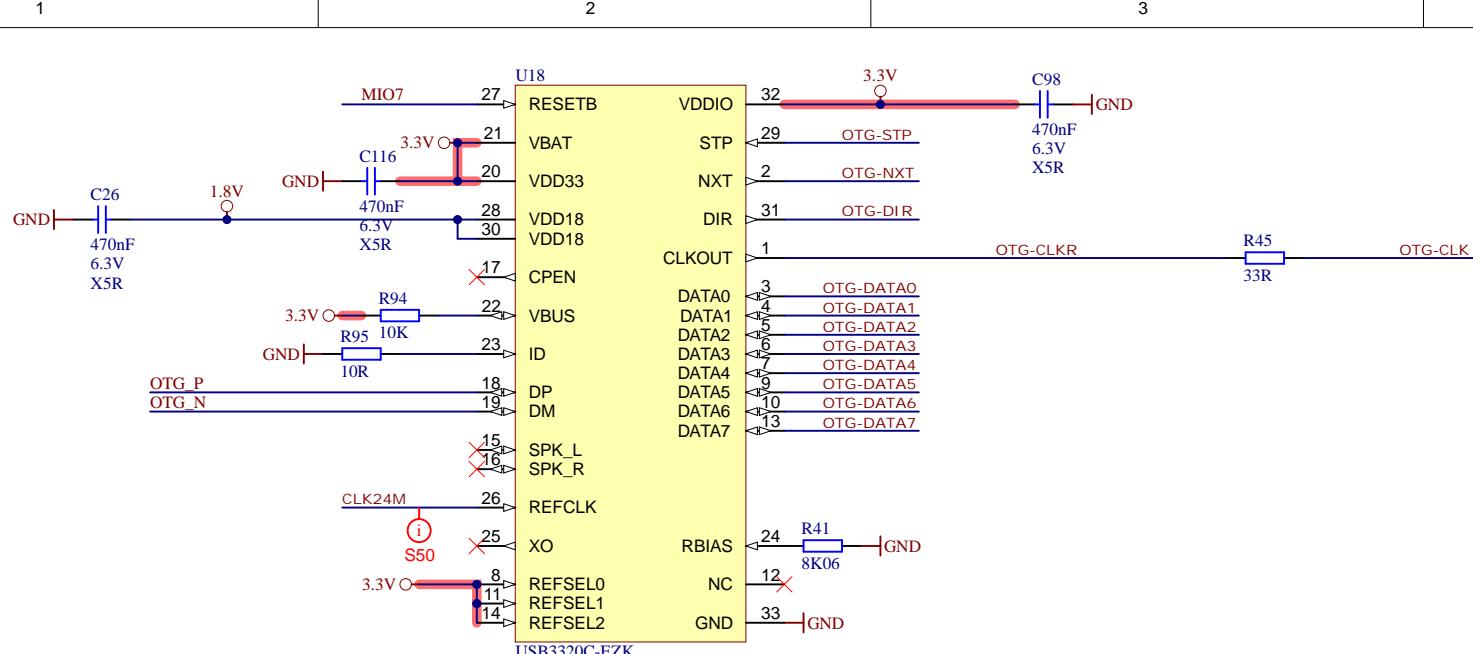
Rev. 04

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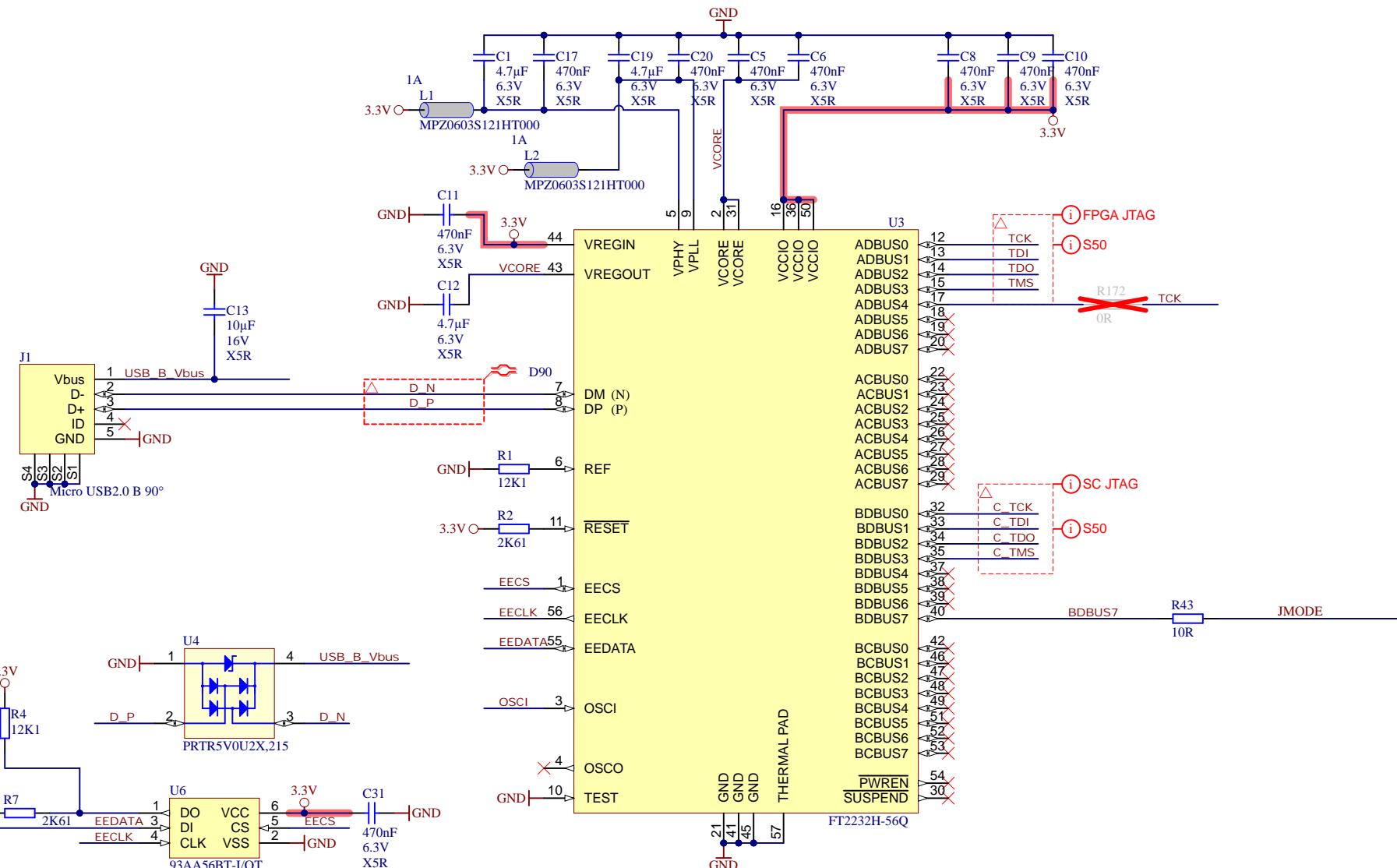
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Filename: FPGA_RAM.SchDoc





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Title: FTDI		
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A

A

B

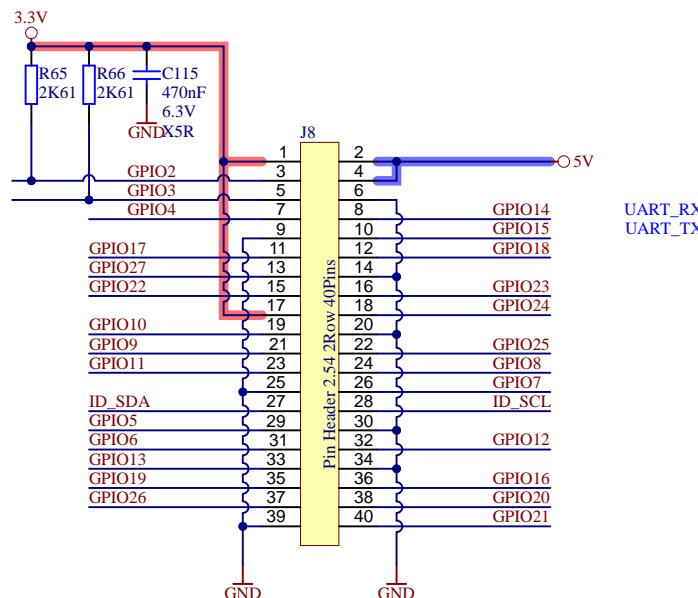
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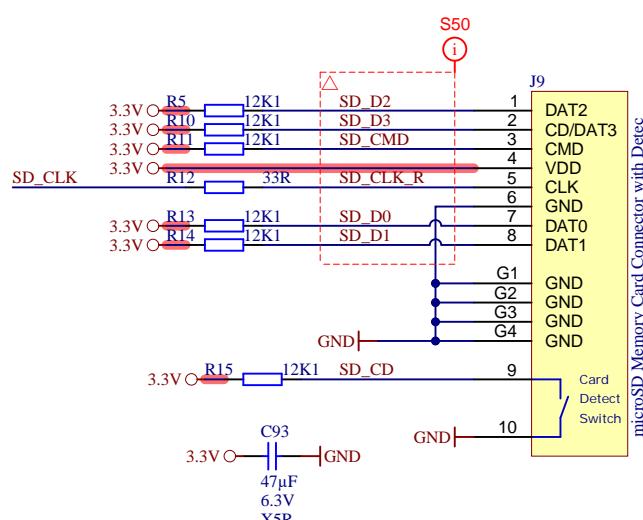
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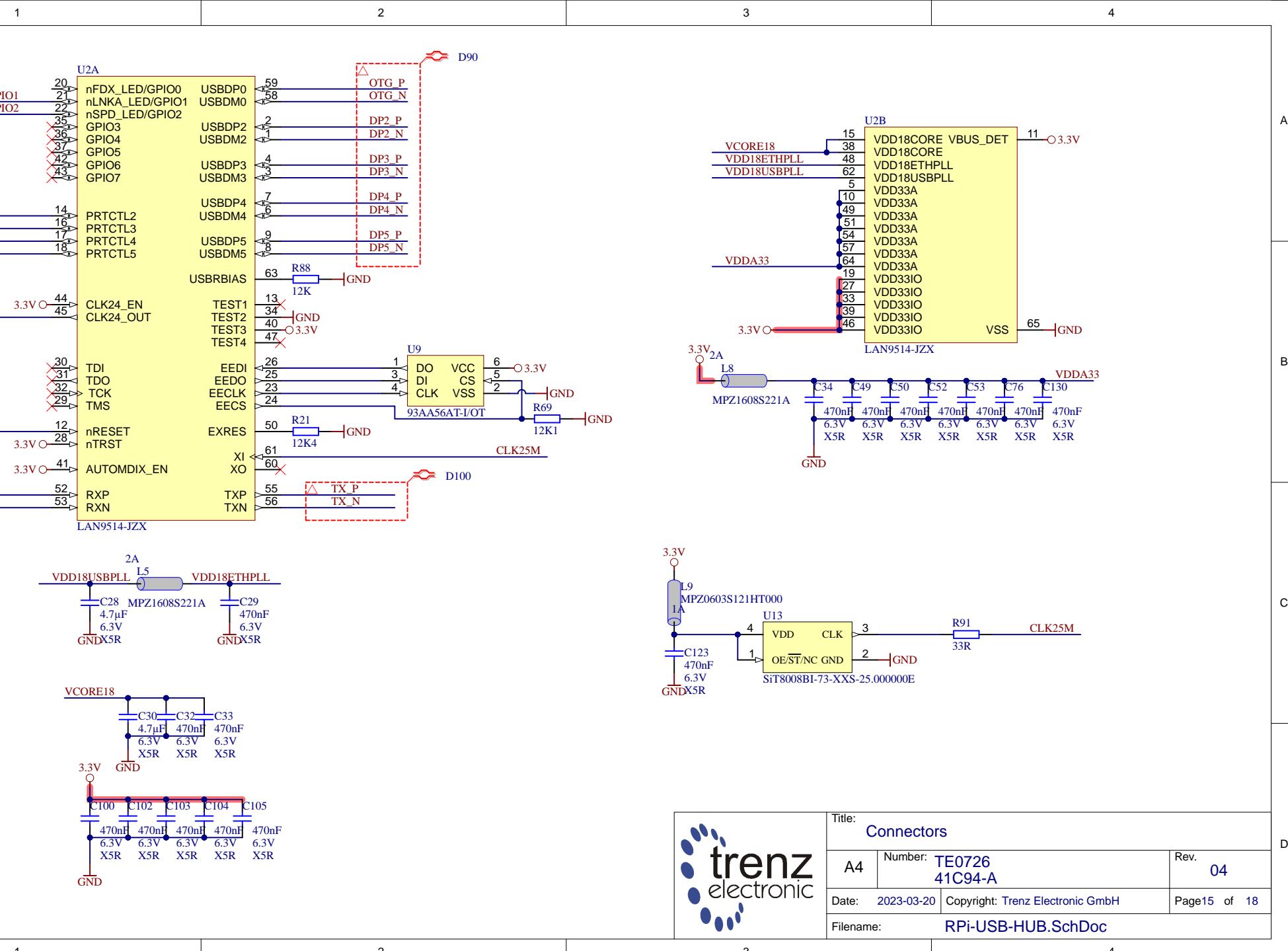
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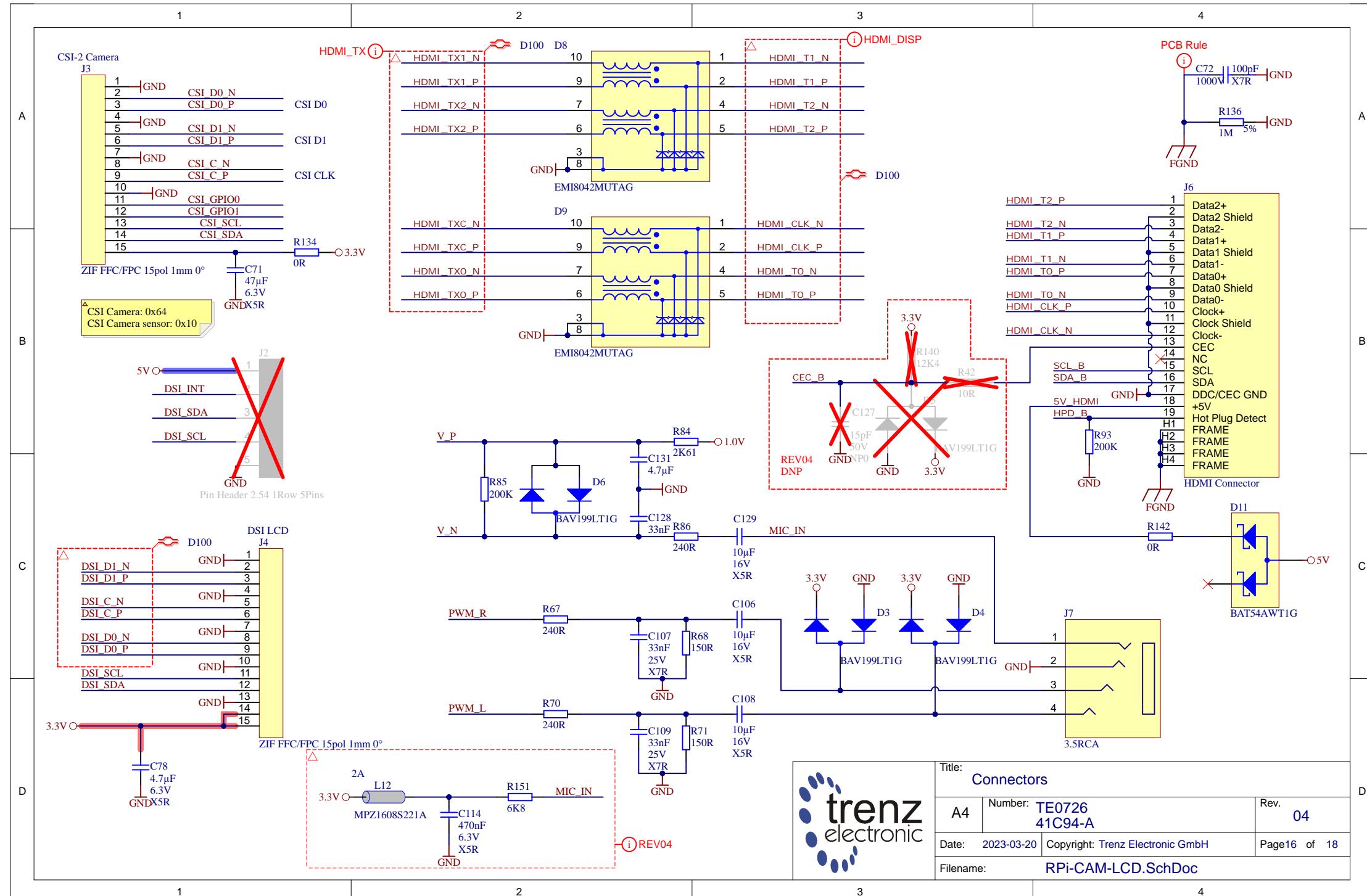


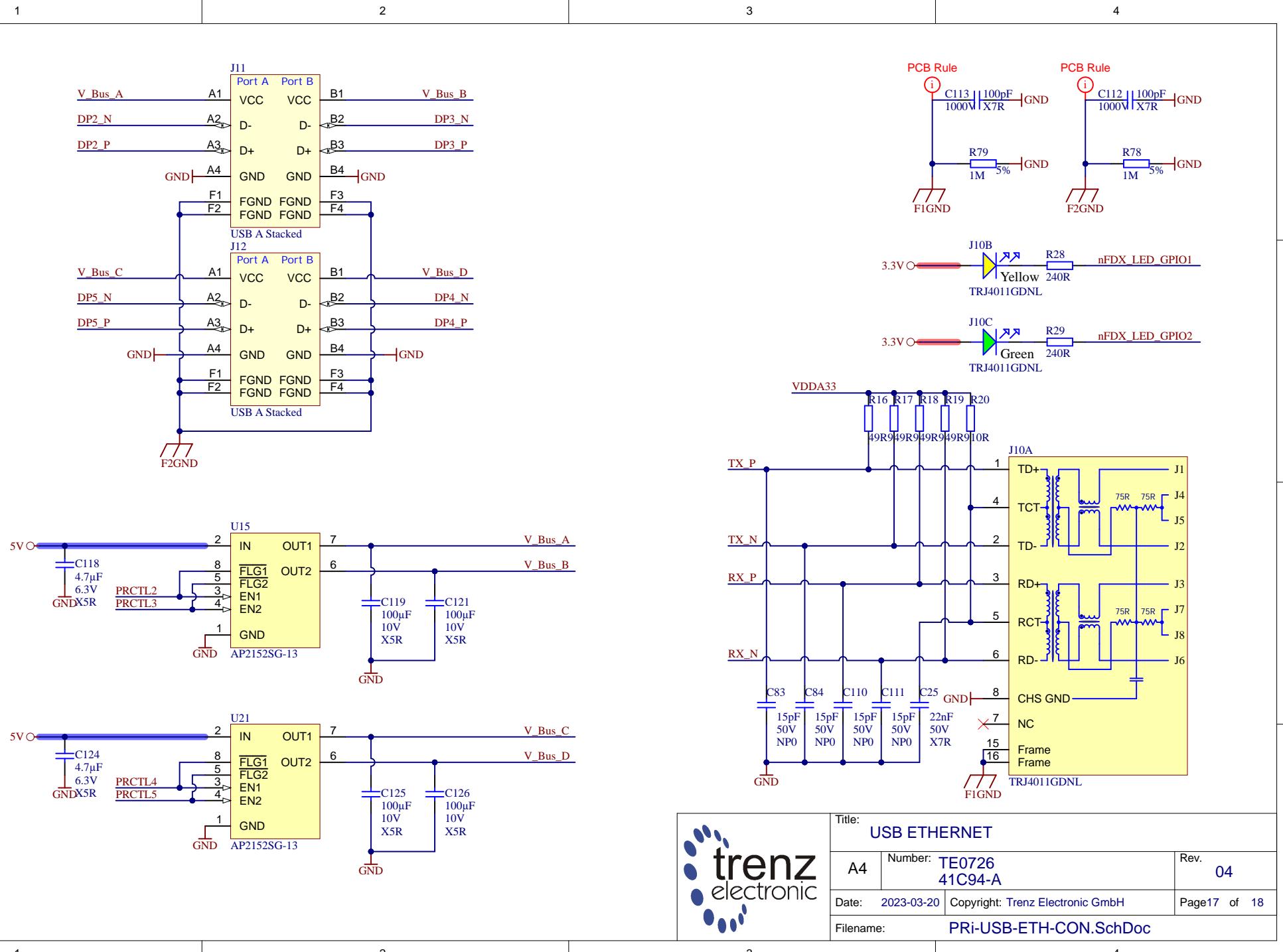
JUMPER 2.54-2



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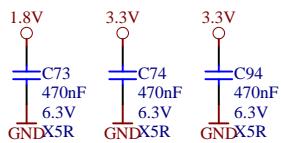
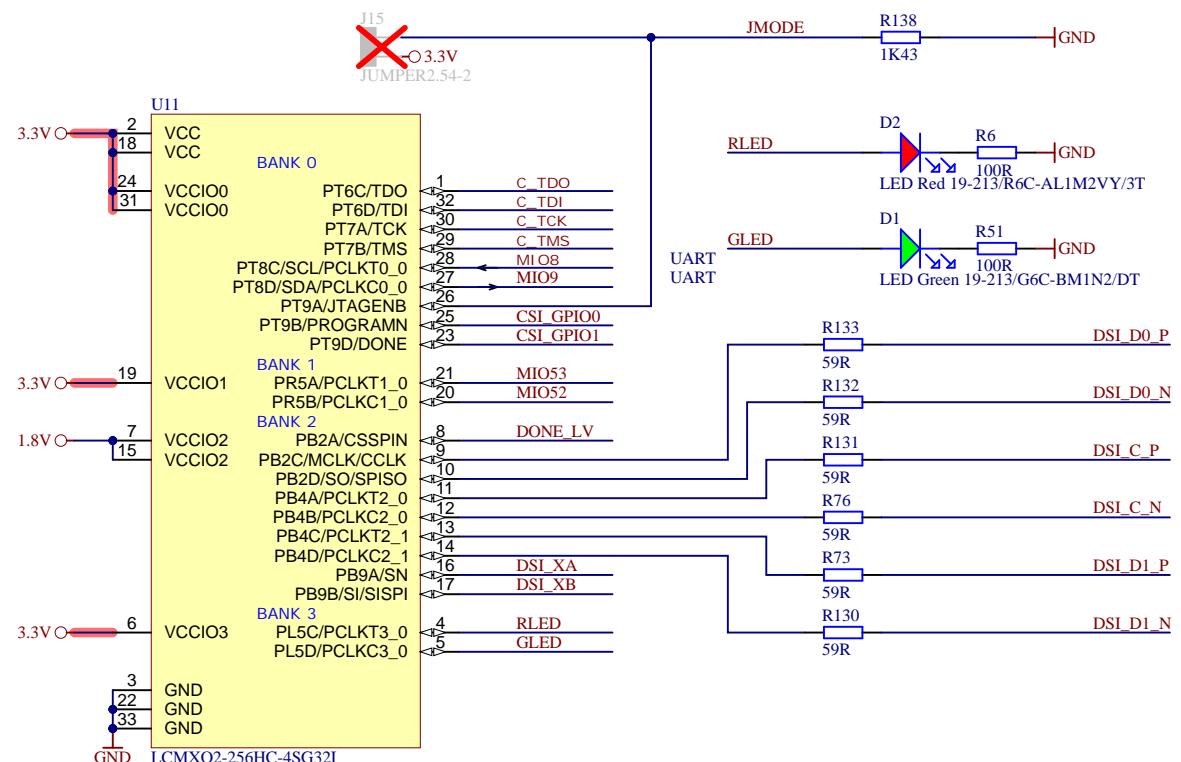
B

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D



Title: CPLD		
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