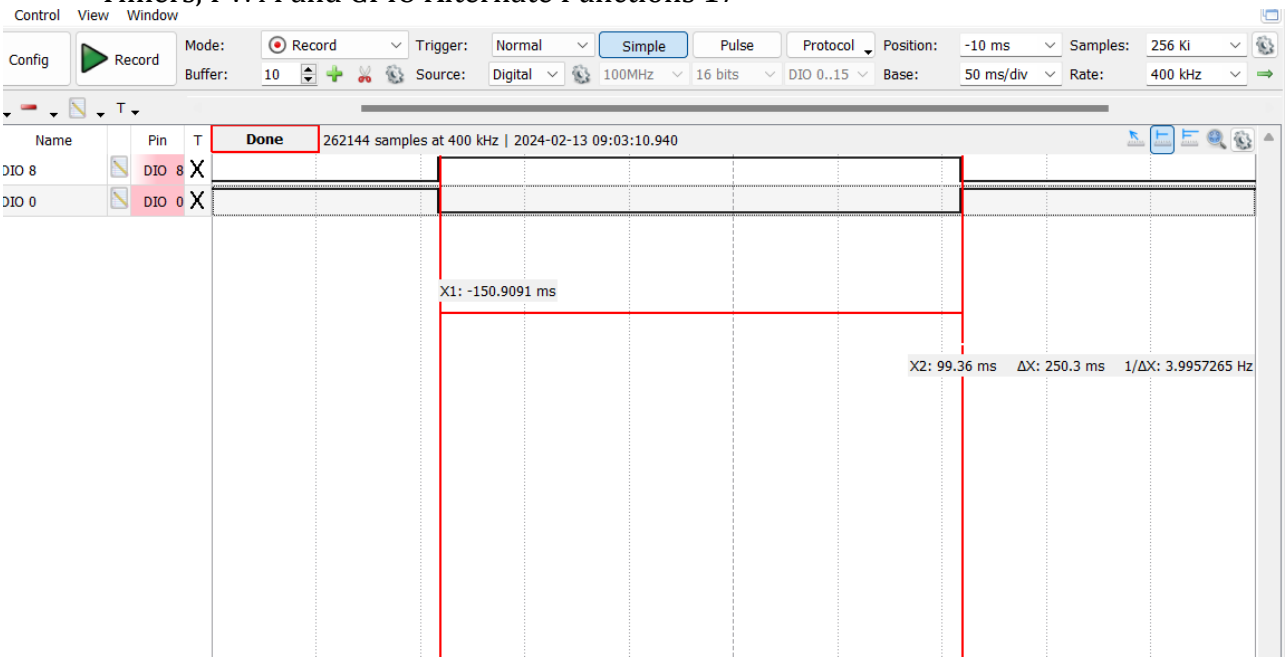
1. Using a timer clock source of 8 MHz, calculate PSC and ARR values to get a 60 Hz interrupt. • This is tricky because precisely 60 Hz is impossible with our system; instead, think about the process and minimize the error. Many combinations of PSC and ARR values work—not just one!

   I chose a PSC value of 59. This gave me an ARR value of 2222.2. I chose this because the denominator would be 60 times 60 which results in a low offset.

2. Look through the Table 13 "STM32F072x8/xB pin definitions" in the chip datasheet and list all pins that can have the timer 3 capture/compare channel 1 alternate function. • If the pin is included on the LQFP64 package that we are using, list the alternate function number that you would use to select it.

   PB4 AF1
   PE3
   PC6 AF0
   PA6 AF1

3. List your measured value of the timer UEV interrupt period from first experiment. Timers, PWM and GPIO Alternate Functions 17



4. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 1.

Active duty cycle increases mode 1 as values increased.

5. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 2.

Active duty cycle would decrease in mode 2 as values increased.

6. Include at least one logic analyzer screenshot of a PWM capture.

7. What PWM mode is shown in figure 3.6 of the lab manual (PWM mode 1 or 2)?
   PWM mode 2