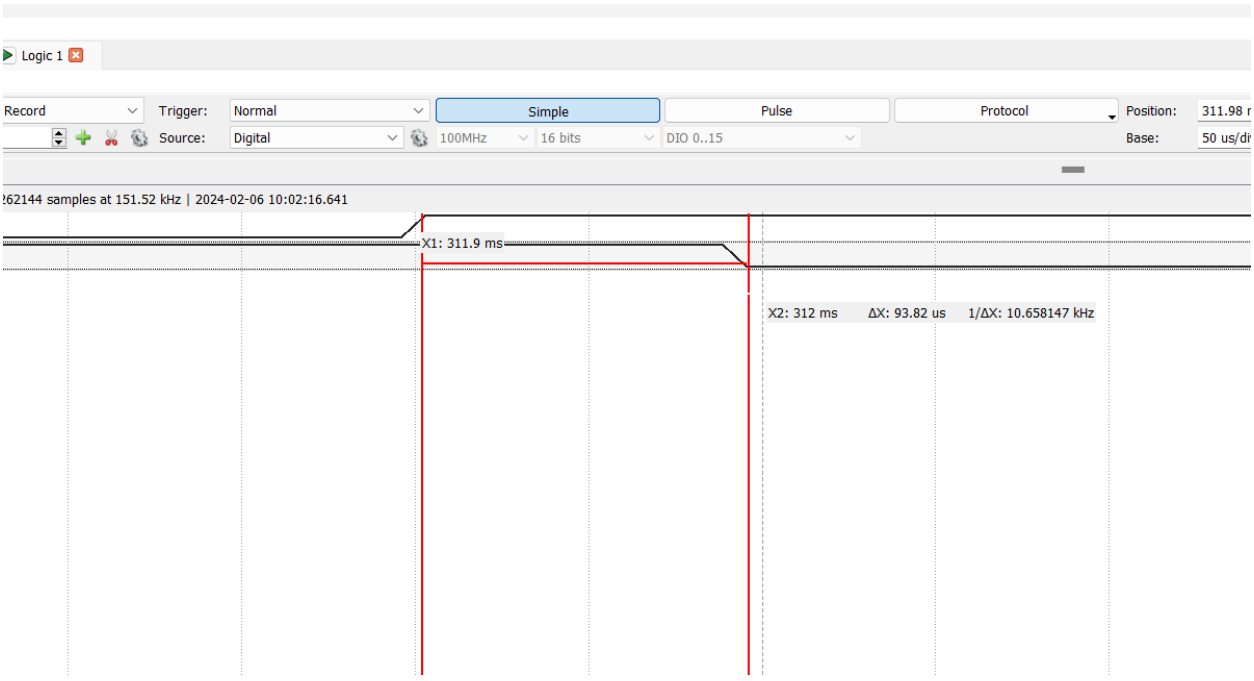
1. Why can’t you use both pins PA0 and PC0 for external interrupts at the same time?
   These share a mux and thus map to the same interrupt.
2. What software priority level gives the highest priority? What level gives the lowest?
   0 is the highest priority and 3 is the lowest priority
3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?

   Including non implemented bits it should use 8 bits.

4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.
   93.82 micro seconds



5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?
   The handlers will keep running and looping until the flags are cleared as it thinks the flags were set again.