

**Hacettepe University**  
**Computer Engineering Department**

**\* BBM233 – Logic Design Lab. – Design Homework \***

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**Group Number** : 12

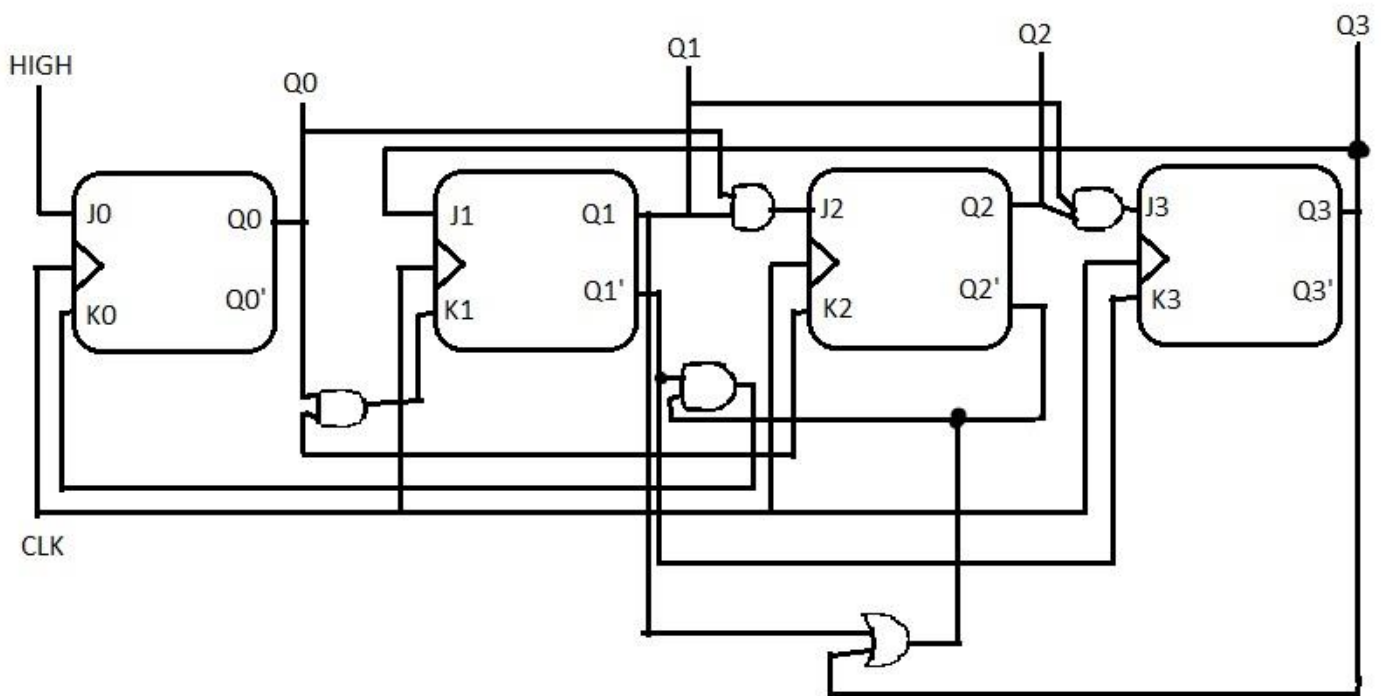
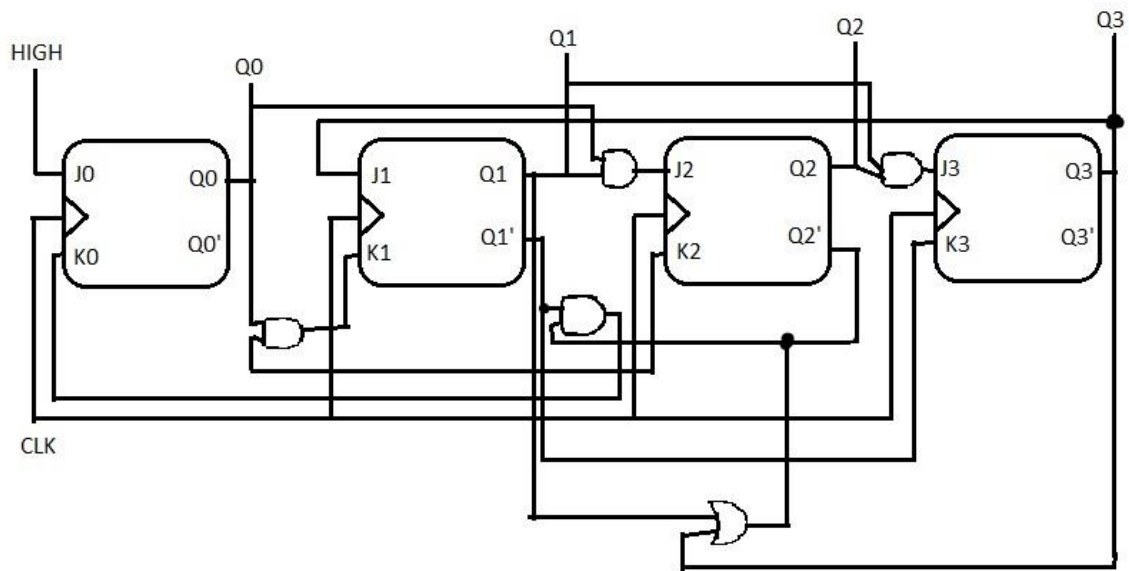
**Subject** : Prime Number Counter Design with JK FFs in Verilog

**Data Due** : 20/01/2018

**Main Program** : design\_hw\_pnc.v

**Test Program** : design\_hw\_tb.v

## I. DESIGN & DESCRIPTION



## II. IMPLEMENTATION & DETAILS

Then by following our design, we implement our code as below;

```
module jkffs(J,K,clock,Q,Qbar);

    input J,K,clock;
    output Q,Qbar;

    reg Q,Qbar;
    initial begin Q=1'b0; Qbar=1'b1; end
    always @(posedge clock)
        begin
            case({J,K})
                {1'b0,1'b0}:begin Q=Q; Qbar=Qbar; end
                {1'b0,1'b1}: begin Q=1'b0; Qbar=1'b1; end
                {1'b1,1'b0}:begin Q=1'b1; Qbar=1'b0; end
                {1'b1,1'b1}: begin Q=~Q; Qbar=~Qbar; end
            endcase
        end
endmodule

module primeCounter(
    input x,
    output [3:0]ot,
    input clk
);

    wire q0,q1,q2,q3;

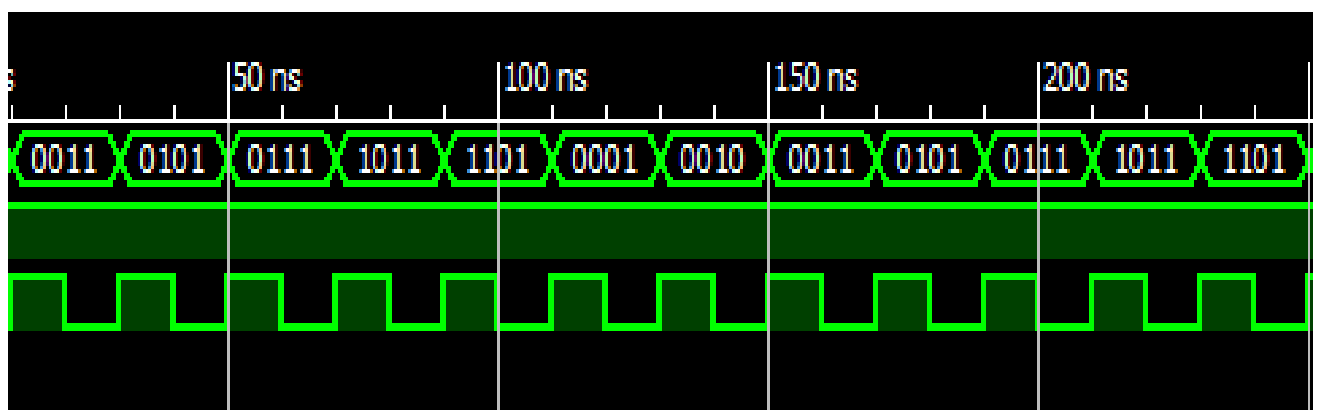
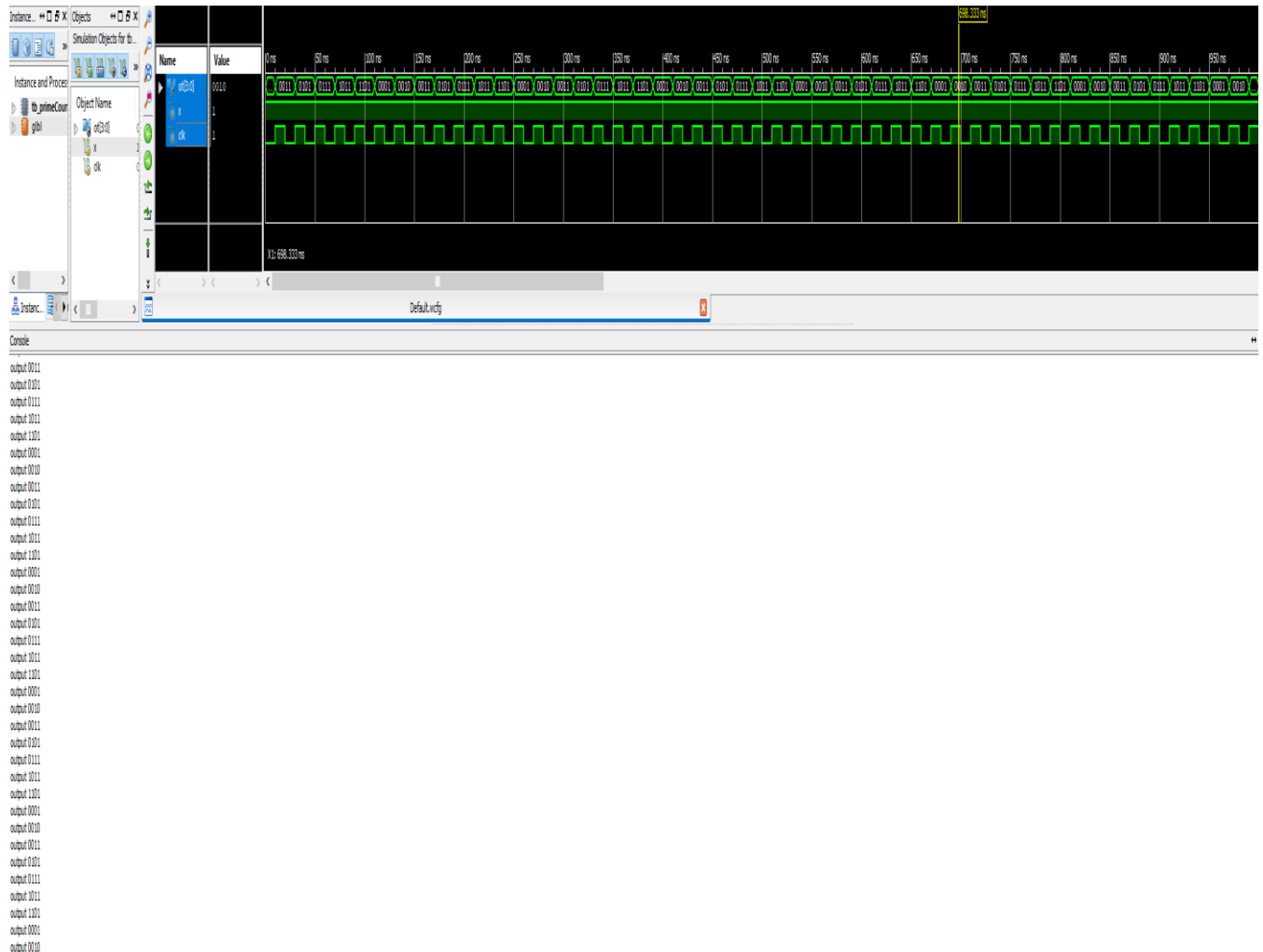
    jkffs f1(.J(1), .K(q1*q2), .clock(clk), .Q(ot[0]), .Qbar(q0));
    jkffs f2(.J(q3), .K(ot[0]*q2), .clock(clk), .Q(ot[1]), .Qbar(q1));
    jkffs f3(.J(ot[0]*ot[1]), .K(ot[1]+ot[3]), .clock(clk), .Q(ot[2]), .Qbar(q2));
    jkffs f4(.J(ot[2]*ot[1]), .K(q1), .clock(clk), .Q(ot[3]), .Qbar(q3));
endmodule
```

Actually f1's should J(x) we have no time to change this.

X is high from our design schema.

### III. SAMPLE WAVEFORMS & TRUTH TABLE

We tried our code by test bench considering changes of clock(clk) values, it works correctly...



output 00 11  
output 0 10 1  
output 0 1 1 1  
output 10 1 1  
output 1 10 1  
output 000 1  
output 00 10  
output 00 1 1  
output 0 10 1  
output 0 1 1 1  
output 10 1 1  
output 1 10 1  
output 000 1  
output 00 10  
output 00 1 1  
output 0 10 1  
output 0 1 1 1  
output 10 1 1  
output 1 10 1  
output 000 1  
output 00 10  
output 00 1 1  
output 0 10 1  
output 0 1 1 1  
output 10 1 1  
output 1 10 1  
output 000 1  
output 00 10  
output 00 1 1  
output 0 10 1  
output 0 1 1 1

# Kmaps

PRESENT STATE				NEXT STATE			
Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	1
0	1	0	1	0	1	1	1
0	1	1	1	1	0	1	1
1	0	1	1	1	1	0	1
1	1	0	1	0	0	0	1