Hacettepe University
Department of Computer Engineering

BBM231 – Digital Design Homework

Subject : Computer Structure

Development Lng. : Verilog

Deadline : **30/11/2017**

Advisors : R.A. Hüseyin Temuçin

HOMEWORK

In this homework, you will design and implement a simple 4-bit multiplier, using half adder and full adder components in a combinatorial approach. In the design, as you know how to do it, you are expected to design a full adder using the half adder components. Next, you need to design a 4-bit adder circuit using multiple full adder components together. Schematic designs of half adder, full adder and 4-bit adder circuits are given below.

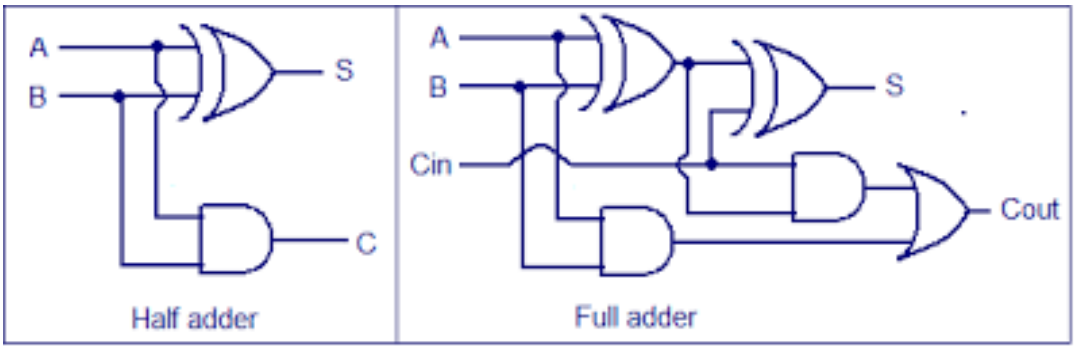

Figure 1: Half adder and full adder gate level design

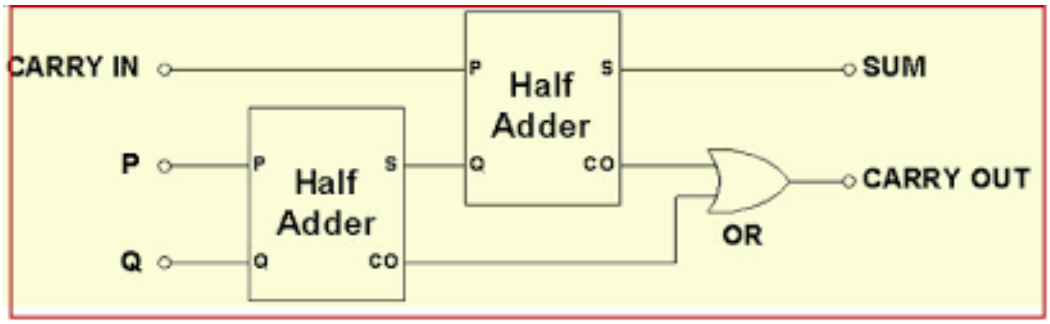

Figure 2: Schematic design of full adder using half adder components

NOTES

- Save all your work until the experiment is graded.
- The assignment must be original, INDIVIDUAL work. Shared source codes will be considered as cheating. Also the students who share their works will be punished in the same way.
- You can ask your questions via piazza class group http://piazza.com/hacettepe.edu.tr/fall2017/bbm231/home. Discussion of the solution on the newsgroups will be considered “group work”, which means “cheating”.
- You are expected to follow the course’s group and you will be held responsible for the announcements made there.
- Cheaters will not be tolerated.