Hacettepe University
Computer Engineering Department
BBM234 Computer Organization

Homework 1-Answers

Assigned date : 25.2.2016
Due date : 9.3.2016 (Section 1)
: 11.3.2016 (Section 2)

You should hand in your homework in class. If you are not able to attend the class in the due date, you can slide your homework under my office door.
Don't email your homework! Stamp your homework papers. Do not put them in the plastic bags.
LATE HOMEWORKS WILL NOT BE ACCEPTED…

Questions: (Each one is 20 points.)

Q1. Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock cycle of 15 ns (nanosecond) and M2 has a clock cycle of 10 ns. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction class	Machine M1- Cycle / Instruction class	Machine M2- Cycle / Instruction class	Instruction Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

a) Calculate the average CPI for each machine, M1, and M2.
b) For a program with 10 billion instructions executing on M1 and M2, what are the execution times on M1 and M2?

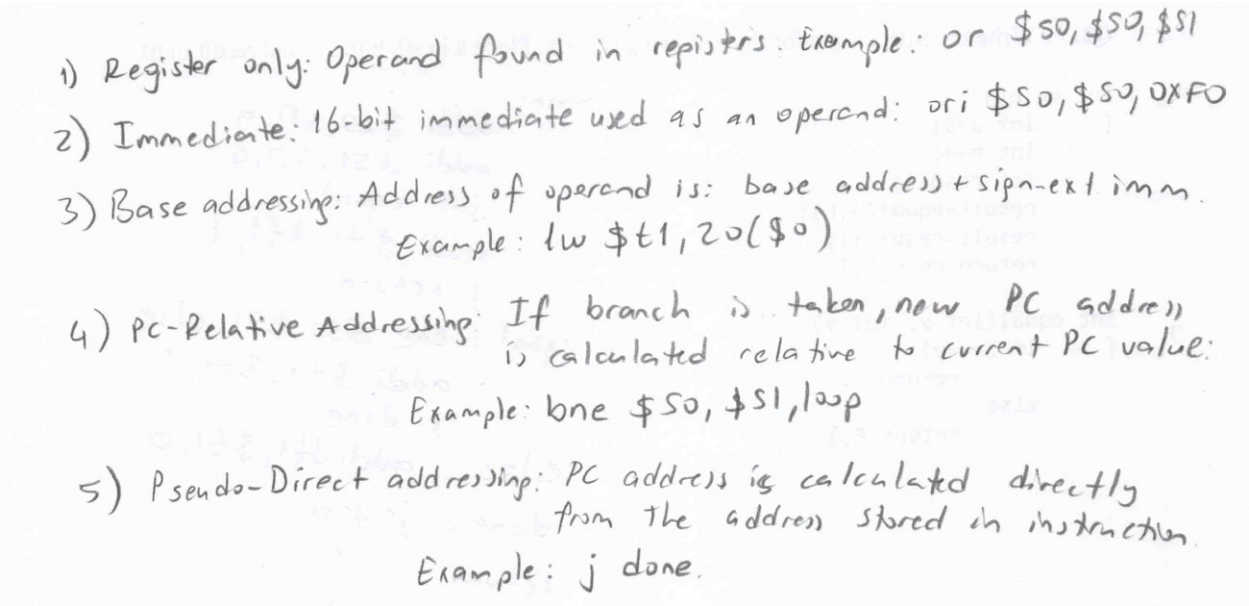
A2.

a) CPI(M1)=1*0.60+2*0.30+4*0.10=1.6
CPI(M2)=2*0.60+3*0.30+4*0.10=2.5

b) Exec_Time(M1)=Number of instructions*CPI*ClockTime=$10*10^9*1.6*15*10^{-9}$=240s
Exec_Time(M2)=Number of instructions*CPI*ClockTime=$10*10^9*2.4*10*10^{-9}$=250s

Q2. Which addressing modes are used in MIPS architectures? Explain them using the following instructions. Which class of addressing modes do the following instructions belong to?

- bne $s0, $s1, loop
- lw $t1, 20($0)
- j done
- or $s0, $s0, $s1
- ori $s0, $s0, 0xF0



Q3. Aşağıdaki programın çalışma sürelerini single cycle ve multi cycle işlemcide hesaplamak istiyoruz. İşlemcilerin clock süreleri sırasıyla C_{SC}=8ns, C_{MC}=3ns olsun.

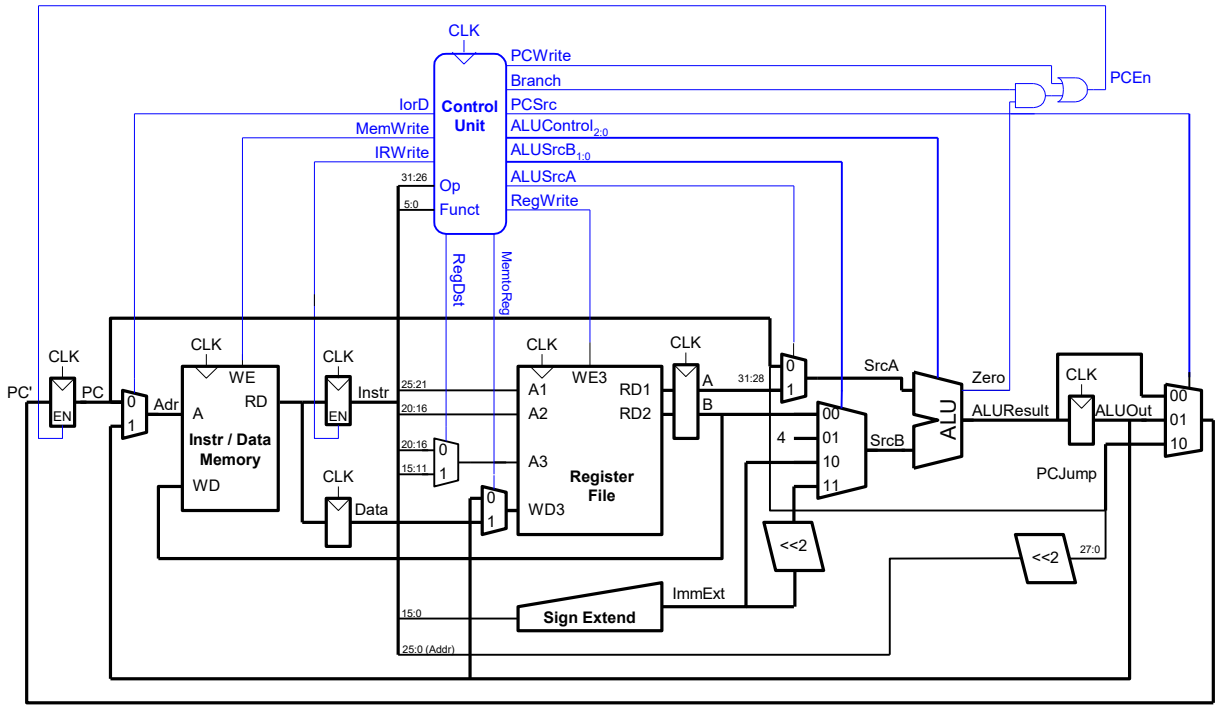
		Komut kaç Kez çalışır	Multi-cycle clock süresi	Multi-cycle Toplam cc
	addi $s1, $0, 2	1	4	4
loop:	beq $s1, $0, done	3	3	9
	sll $t1, $s1, 2	2	4	6
	lw $t2, 0($t1)	2	5	10
	add $t2, $t2, $s1	2	4	8
	sw $t2, 0($t1)	2	4	8
	addi $s1, $s1, -1	2	4	8
	j loop	2	3	6
done:	j main	1	3	3
			Toplam:	62

a) Yukarıdaki program, single cycle işlemcide kaç saniyede biter? Hesaplayın.

Number of istructions=17

CPU Time=No.of Instructions*CPI*ClockTime =17*1*8ns=136ns

b) Multi cycle işlemcide kaç saniyede biter? Hesaplayın.



Şekil 1: Multi cycle işlemci

Program 62 clock cycleda biter (Yukarıda hesaplanmıştır)

CPU Time=Clock sayısı*Clock süresi=62*3ns=186ns

Q4. You are given the following MIPS assembly code for a procedure called proc1.

```
proc1:  add  $s1, $0, $0
        add  $v0, $0, $0
count:  beq  $a0, $0, done
        andi $s0, $a0, 0x1
        beq  $s0, $0, shift
        addi $s1, $s1, 1
shift:  srl  $a0, $a0, 1
        jal  proc1
done:   add  $v0, $v0, $s1
        jr   $ra
```

(a) proc1 function does not successfully return when it is called from the main function. Fix the code so that it successfully returns. (Hint: You should modify one of the instructions.) [5]

When jal proc1 instruction executes, we loose the content of register ra, which is the return address to the main. We should change this instruction to "j count" so that the loop can executes again.

(b) Using the corrected code, write the return value ($v0) for given values of $a0. Write your answer in decimal. [10]

a0	0x000F	v0	4
a0	0x0013	v0	3

(c) Describe in words what proc1 does. [5]

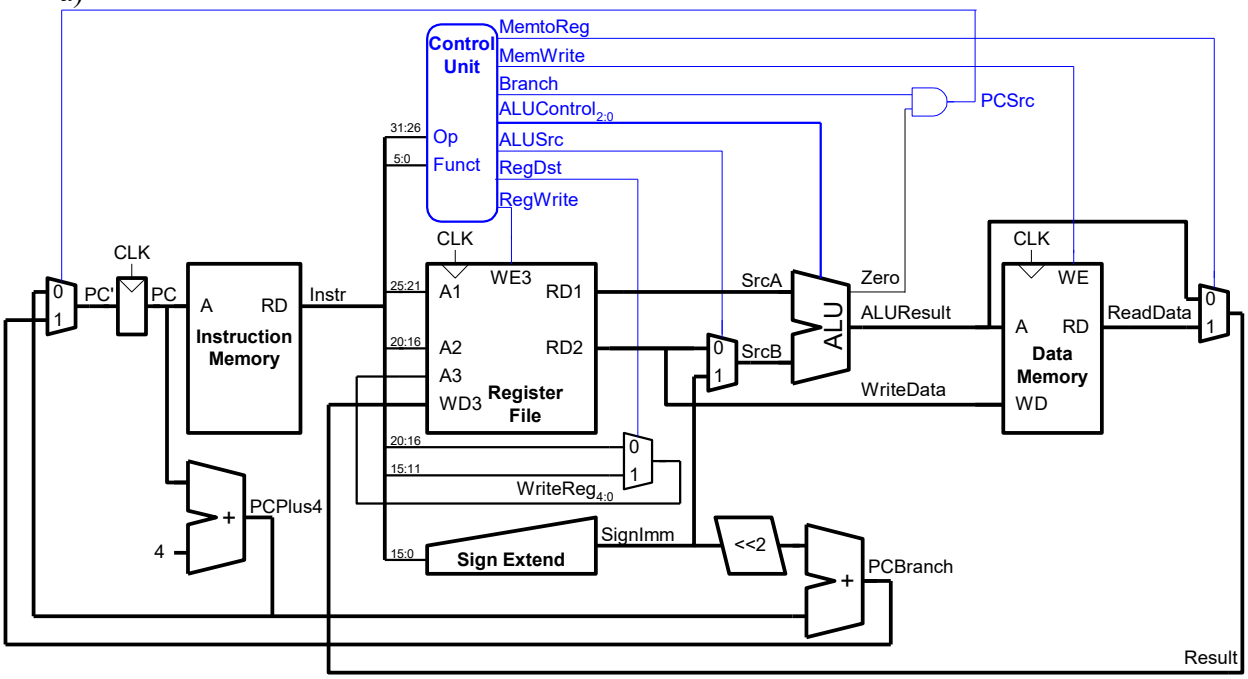
It counts the number of 1's in register a0.

A5. We would like to add bne instruction to the single cycle architecture given below. bne instruction is a branch instruction and it loads branch target address (BTA) to the PC (PC=BTA) is [rs]!=[rt].

a) Show the necessary changes on data-path on Figure 1 and explain your changes. Your new architecture should be able to execute both beq and bne instructions.[12]

b) Fill the control signals in Table I. Add new control signal/signals to the table if necessary. [8]

a)



Şekil 1: Single cycle işlemci

PCSrc sinyalini, Branch, zero ve yeni eklenecek bne kontrol sinyali ile bulmak gerekir. Truth table aşağıda verilmiştir. PCsrc = 1 ise PC=BTA olacaktır.

Branch	Zero	Bne	PCsrc
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Data pathdeki AND fonksiyonunu PCsrc'nin yeni fonksiyonu ile değiştirmek gerekecektir.

PCsrc=(Zero XOR bne) AND Branch

b)

Tablo I: **bne** komutunun kontrol sinyalleri

Inst.	**Op31:26**	**RegWrite**	**RegDst**	**AluSrc**	**Branch**	**MemWrite**	**MemtoReg**	**ALUOp1:0**	**Bne**
bne	000101	0	X	0	1	0	X	01 (Çıkarma)	1