

# 1. Description

# 1.1. Project

Project Name	Altum
Board Name	custom
Generated with:	STM32CubeMX 6.7.0
Date	03/02/2023

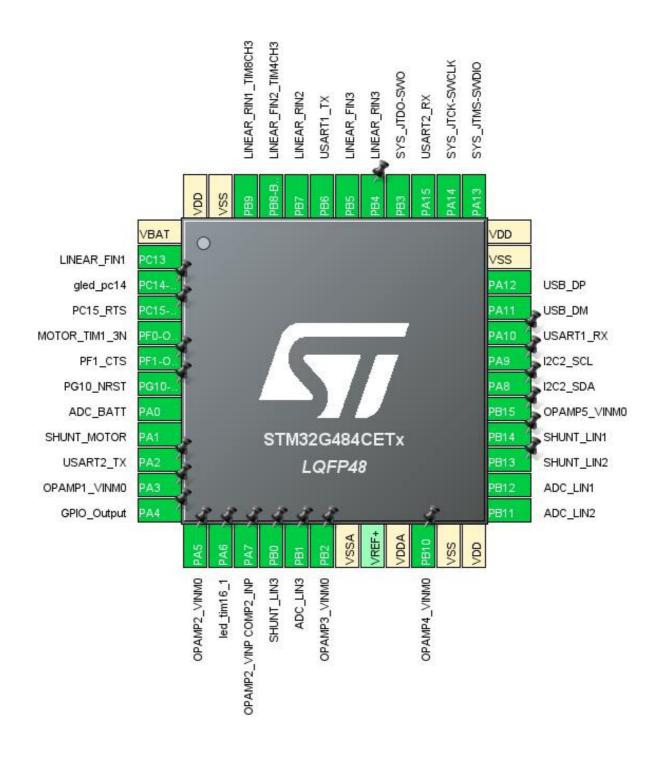
# 1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G484CETx
MCU Package	LQFP48
MCU Pin number	48

# 1.3. Core(s) information

Core(s)	ARM Cortex-M4

# 2. Pinout Configuration



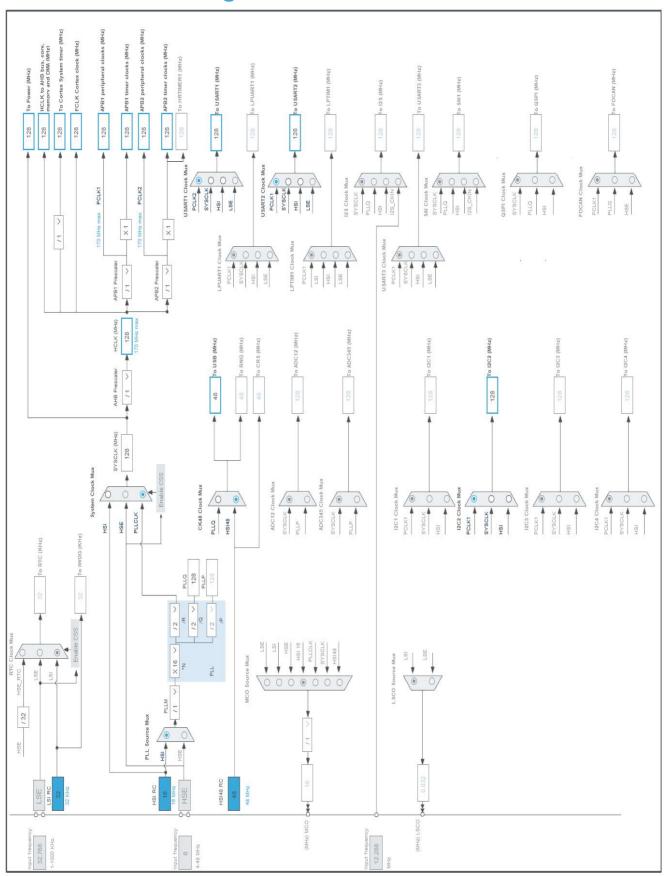
# 3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP48	(function after reset)		Function(s)	
1	VBAT	Power		
2	PC13	I/O	TIM8_CH4N	LINEAR_FIN1
3	PC14-OSC32_IN *	I/O	GPIO_Output	gled_pc14
4	PC15-OSC32_OUT *	I/O	GPIO_Output	PC15_RTS
5	PF0-OSC_IN	I/O	TIM1_CH3N	MOTOR_TIM1_3N
6	PF1-OSC_OUT *	I/O	GPIO_Output	PF1_CTS
7	PG10-NRST *	I/O	GPIO_Output	PG10_NRST
8	PA0	I/O	ADC1_IN1	ADC_BATT
9	PA1	I/O	OPAMP1_VINP	SHUNT_MOTOR
10	PA2	I/O	USART2_TX	
11	PA3	I/O	OPAMP1_VINM0	
12	PA4 *	I/O	GPIO_Output	
13	PA5	I/O	OPAMP2_VINM0	
14	PA6	I/O	TIM16_CH1	led_tim16_1
15	PA7	I/O	OPAMP2_VINP, COMP2_INP	
16	PB0	I/O	COMP4_INP, OPAMP3_VINP	SHUNT_LIN3
17	PB1	I/O	ADC1_IN12	ADC_LIN3
18	PB2	I/O	OPAMP3_VINM0	
19	VSSA	Power		
21	VDDA	Power		
22	PB10	I/O	OPAMP4_VINM0	
23	VSS	Power		
24	VDD	Power		
25	PB11	I/O	ADC1_IN14	ADC_LIN2
26	PB12	I/O	ADC1_IN11	ADC_LIN1
27	PB13	I/O	COMP5_INP, OPAMP4_VINP	SHUNT_LIN2
28	PB14	I/O	COMP7_INP, OPAMP5_VINP	SHUNT_LIN1
29	PB15	I/O	OPAMP5_VINM0	
30	PA8	I/O	I2C2_SDA	
31	PA9	I/O	I2C2_SCL	
32	PA10	I/O	USART1_RX	
33	PA11	I/O	USB_DM	

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
34	PA12	I/O	USB_DP	
35	VSS	Power		
36	VDD	Power		
37	PA13	I/O	SYS_JTMS-SWDIO	
38	PA14	I/O	SYS_JTCK-SWCLK	
39	PA15	I/O	USART2_RX	
40	PB3	I/O	SYS_JTDO-SWO	
41	PB4	I/O	TIM3_CH1	LINEAR_RIN3
42	PB5	I/O	TIM3_CH2	LINEAR_FIN3
43	PB6	I/O	USART1_TX	
44	PB7	I/O	TIM4_CH2	LINEAR_RIN2
45	PB8-BOOT0	I/O	TIM4_CH3	LINEAR_FIN2_TIM4CH3
46	PB9	I/O	TIM8_CH3	LINEAR_RIN1_TIM8CH3
47	VSS	Power		
48	VDD	Power		

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



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# 5. Software Project

# 5.1. Project Settings

Name	Value
Project Name	Altum
Project Folder	C:\Users\bartc\STM32CubeIDE\workspace_2\Altum
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.5.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

# 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

# 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2
6	MX_ADC5_Init	ADC5
7	MX_COMP2_Init	COMP2
8	MX_COMP4_Init	COMP4
9	MX_COMP5_Init	COMP5
10	MX_COMP7_Init	СОМР7
11	MX_DAC1_Init	DAC1

Rank	Function Name	Peripheral Instance Name
12	MX_DAC2_Init	DAC2
13	MX_DAC3_Init	DAC3
14	MX_DAC4_Init	DAC4
15	MX_OPAMP1_Init	OPAMP1
16	MX_OPAMP2_Init	OPAMP2
17	MX_OPAMP3_Init	OPAMP3
18	MX_OPAMP4_Init	OPAMP4
19	MX_OPAMP5_Init	OPAMP5
20	MX_USART1_UART_Init	USART1
21	MX_I2C2_Init	I2C2
22	MX_TIM1_Init	TIM1
23	MX_TIM2_Init	TIM2
24	MX_TIM3_Init	TIM3
25	MX_TIM4_Init	TIM4
26	MX_TIM8_Init	TIM8
27	MX_TIM16_Init	TIM16
28	MX_TIM20_Init	TIM20
29	MX_USART2_UART_Init	USART2
30	MX_USB_Device_Init	USB_DEVICE

# 6. Power Consumption Calculator report

# 6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
мси	STM32G484CETx
Datasheet	DS12288_Rev0

# 6.2. Parameter Selection

Temperature	25
Vdd	3.0

# 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

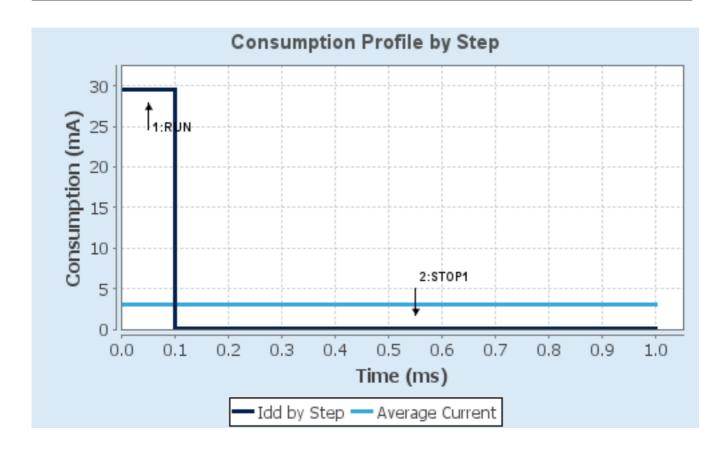
# 6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/DualBank/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	29.5 mA	80.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	123.36	129.98
Category	In DS Table	In DS Table

# 6.5. Results

Sequence Time	1 ms	Average Current	3.02 mA
Battery Life	1 month, 16 days,	Average DMIPS	212.5 DMIPS
	9 hours		

# 6.6. Chart



# 7. Peripherals and Middlewares Configuration

7.1. ADC1

IN1: IN1 Single-ended IN11: IN11 Single-ended

mode: IN12

IN14: IN14 Single-ended mode: VOPAMP1 Channel 7.1.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Clock Prescaler Synchronous clock mode divided by 4

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Gain Compensation 0

Scan Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Low Power Auto WaitDisabledContinuous Conversion ModeDisabledDiscontinuous Conversion ModeDisabledDMA Continuous RequestsDisabled

Overrun behaviour Overrun data preserved

ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

ChannelChannel 1Sampling Time2.5 CyclesOffset NumberNo offset

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode false

7.2. ADC2

mode: VOPAMP2 Channel mode: VOPAMP3 Channel 7.2.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Clock Prescaler Synchronous clock mode divided by 4

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Gain Compensation

Scan Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Low Power Auto WaitDisabledContinuous Conversion ModeDisabledDiscontinuous Conversion ModeDisabledDMA Continuous RequestsDisabled

Overrun behaviour Overrun data preserved

ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Vopamp2

Sampling Time 2.5 Cycles
Offset Number No offset

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode

false

#### 7.3. ADC5

#### mode: VOPAMP5 Channel

### 7.3.1. Parameter Settings:

#### ADC\_Settings:

Clock Prescaler Synchronous clock mode divided by 4

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Gain Compensation 0

Scan Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Low Power Auto WaitDisabledContinuous Conversion ModeDisabledDiscontinuous Conversion ModeDisabledDMA Continuous RequestsDisabled

Overrun behaviour Overrun data preserved

ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel Vopamp5

Sampling Time 2.5 Cycles
Offset Number No offset

ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

**Analog Watchdog 1:** 

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:** 

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:** 

Enable Analog WatchDog3 Mode false

7.4. COMP2

mode: Input [+]

Input [-]: DAC1 OUT2

7.4.1. Parameter Settings:

**Basic Parameters:** 

Trigger Mode None
Hysteresis Level None

**Output Configuration:** 

Blanking Source None

Output Polarity COMP output on GPIO isn't inverted

7.5. COMP4

mode: Input [+]

Input [-]: DAC3 OUT2

7.5.1. Parameter Settings:

**Basic Parameters:** 

Trigger Mode None
Hysteresis Level None

**Output Configuration:** 

Blanking Source None

Output Polarity COMP output on GPIO isn't inverted

7.6. COMP5

mode: Input [+]

Input [-]: DAC4 OUT1

7.6.1. Parameter Settings:

**Basic Parameters:** 

Trigger Mode None
Hysteresis Level None

**Output Configuration:** 

Blanking Source None

Output Polarity COMP output on GPIO isn't inverted

#### 7.7. COMP7

mode: Input [+]

Input [-]: DAC2 OUT1

#### 7.7.1. Parameter Settings:

#### **Basic Parameters:**

Trigger Mode None
Hysteresis Level None

**Output Configuration:** 

Blanking Source None

Output Polarity COMP output on GPIO isn't inverted

#### 7.8. DAC1

OUT1 mode: OUT1 Connected to on chip-peripherals only OUT2 mode: OUT2 Connected to on chip-peripherals only

## 7.8.1. Parameter Settings:

#### **DAC Out1 Settings:**

Mode selected Normal Mode
Output Buffer Disable

DAC High Frequency Mode Automatic

DMA Double Data Disable
Signed Format Disable
Trigger None
Trigger2 None

User Trimming Factory trimming

#### **DAC Out2 Settings:**

Mode selected Normal Mode
Output Buffer Disable

DAC High Frequency Mode Automatic

DMA Double Data Disable
Signed Format Disable
Trigger None
Trigger2 None

User Trimming Factory trimming

#### 7.9. DAC2

**OUT1 mode: OUT1 Connected to on chip-peripherals only** 

## 7.9.1. Parameter Settings:

#### **DAC Out1 Settings:**

Mode selected Normal Mode
Output Buffer Disable

DAC High Frequency Mode Automatic

DMA Double Data Disable
Signed Format Disable
Trigger None
Trigger2 None

User Trimming Factory trimming

#### 7.10. DAC3

mode: OUT2 mode

#### 7.10.1. Parameter Settings:

### **DAC Out2 Settings:**

Mode selected Normal Mode
Output Buffer Disable

DAC High Frequency Mode Automatic

DMA Double Data Disable
Signed Format Disable
Trigger None
Trigger2 None

User Trimming Factory trimming

#### 7.11. DAC4

mode: OUT1 mode

## 7.11.1. Parameter Settings:

## **DAC Out1 Settings:**

Mode selected Normal Mode
Output Buffer Disable

DAC High Frequency Mode Automatic

DMA Double Data Disable

Signed Format Disable

Trigger None

Trigger2 None

User Trimming Factory trimming

# 7.12. I2C2 I2C: I2C

## 7.12.1. Parameter Settings:

### Timing configuration:

Custom Timing Disabled

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz) 100

Rise Time (ns) 0
Fall Time (ns) 0
Coefficient of Digital Filter 0

Analog Filter Enabled

Timing 0x20A0C4DF \*

#### **Slave Features:**

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

#### 7.13. OPAMP1

Mode: PGA Internally connected\_IO

#### 7.13.1. Parameter Settings:

#### **Basic Parameters:**

Power Mode Normal
PGA Gain 2 or -1
User Trimming Disable

7.14. OPAMP2

Mode: PGA Internally connected\_IO

7.14.1. Parameter Settings:

**Basic Parameters:** 

Power Mode Normal
PGA Gain 16 or -15 \*
User Trimming Disable

7.15. OPAMP3

Mode: PGA Internally connected\_IO

7.15.1. Parameter Settings:

**Basic Parameters:** 

Power Mode Normal
PGA Gain 2 or -1
User Trimming Disable

7.16. OPAMP4

Mode: PGA Internally connected\_IO

7.16.1. Parameter Settings:

**Basic Parameters:** 

Power Mode Normal
PGA Gain 2 or -1
User Trimming Disable

7.17. OPAMP5

Mode: PGA Internally connected\_IO

7.17.1. Parameter Settings:

**Basic Parameters:** 

Power Mode Normal

PGA Gain 16 or -15 \*

User Trimming Disable

#### 7.18. RCC

## 7.18.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value (64
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

**Peripherals Clock Configuration:** 

Generate the peripherals clock configuration TRUE

#### 7.19. SYS

**Debug: Trace Asynchronous Sw** 

#### 7.20. TIM1

Clock Source: Internal Clock
Channel3: PWM Generation CH3N

## 7.20.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)

Counter Mode

Dithering

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

R \*

Repetition Counter (RCR - 16 bits value) 0

auto-reload preload Disable

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

**Break And Dead Time management - BRK Configuration:** 

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

**BRK Sources Configuration** 

- Digital Input Disable - COMP1 Disable - COMP2 Disable Disable - COMP3 - COMP4 Disable - COMP5 Disable - COMP6 Disable - COMP7 Disable

**Break And Dead Time management - BRK2 Configuration:** 

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

**BRK2 Sources Configuration** 

- Digital Input Disable - COMP1 Disable - COMP2 Disable - COMP3 Disable Disable - COMP4 - COMP5 Disable - COMP6 Disable - COMP7 Disable

**Break And Dead Time management - Output Configuration:** 

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

**Clear Input:** 

Clear Input Source Disable

**PWM Generation Channel 3N:** 

Mode PWM mode 1

Pulse (16 bits value) 0
Output compare preload Enable

Fast Mode Disable
CHN Polarity High
CHN Idle State Reset

7.21. TIM2

**Clock Source: Internal Clock** 

7.21.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Dithering Disable
Counter Period (AutoReload Register - 32 bits value) 4294967295
Internal Clock Division (CKD) No Division auto-reload preload Disable

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

7.22. TIM3

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2

7.22.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Dithering Disable

Counter Period (AutoReload Register - 16 bits value) 1000 \*

Internal Clock Division (CKD) No Division auto-reload preload Disable

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

**Clear Input:** 

Clear Input Source Disable

**PWM Generation Channel 1:** 

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

**PWM Generation Channel 2:** 

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.23. TIM4

Clock Source: Internal Clock
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3

7.23.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value)

Counter Mode

Dithering

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

No Division

Disable

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

**Clear Input:** 

Clear Input Source Disable

**PWM Generation Channel 2:** 

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

**PWM Generation Channel 3:** 

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

#### 7.24. TIM8

Clock Source: Internal Clock
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4N

#### 7.24.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Dithering Disable
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 16 bits value) 0
auto-reload preload Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

#### **Break And Dead Time management - BRK Configuration:**

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

**BRK Sources Configuration** 

Disable - Digital Input - COMP1 Disable - COMP2 Disable Disable - COMP3 - COMP4 Disable - COMP5 Disable - COMP6 Disable - COMP7 Disable

#### **Break And Dead Time management - BRK2 Configuration:**

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

**BRK2 Sources Configuration** 

- Digital Input Disable - COMP1 Disable - COMP2 Disable - COMP3 Disable - COMP4 Disable - COMP5 Disable - COMP6 Disable - COMP7 Disable

#### **Break And Dead Time management - Output Configuration:**

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

**Clear Input:** 

Clear Input Source Disable

**PWM Generation Channel 3:** 

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

**PWM Generation Channel 4N:** 

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CHN Polarity High
CHN Idle State Reset

#### 7.25. TIM16

mode: Activated

**Channel1: PWM Generation CH1** 

#### 7.25.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Dithering Disable
Counter Period (AutoReload Register - 16 bits value ) 65535

Internal Clock Division (CKD)

No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

#### **Break And Dead Time management - BRK Configuration:**

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

**BRK Sources Configuration** 

- Digital Input Disable Disable - COMP1 - COMP2 Disable Disable - COMP3 - COMP4 Disable - COMP5 Disable - COMP6 Disable - COMP7 Disable

#### **Break And Dead Time management - Output Configuration:**

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

#### **PWM Generation Channel 1:**

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

#### 7.26. TIM20

**Clock Source: Internal Clock** 

## 7.26.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Dithering Disable
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 16 bits value)

0

auto-reload preload Disable

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx\_EGR)

#### 7.27. USART1

## **Mode: Asynchronous**

## 7.27.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 57600 \*

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling16 SamplesSingle SampleDisableClockPrescaler1

Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

**Advanced Features:** 

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

#### 7.28. USART2

**Mode: Asynchronous** 

## 7.28.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 100000 \*

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

**Advanced Features:** 

Auto Baudrate Disable Disable TX Pin Active Level Inversion **RX Pin Active Level Inversion** Disable Disable Data Inversion Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

#### 7.29. USB

mode: Device (FS)

## 7.29.1. Parameter Settings:

#### **Basic Parameters:**

Speed Full Speed 12MBit/s

Physical interface Internal Phy
Sof Enable Disabled

**Power Parameters:** 

Low PowerDisabledLink Power ManagementDisabledBattery ChargingDisabled

#### 7.30. USB\_DEVICE

## Class For FS IP: Communication Device Class (Virtual Port Com)

#### 7.30.1. Parameter Settings:

#### **Basic Parameters:**

USBD\_MAX\_NUM\_INTERFACES (Maximum number of supported interfaces)

1
USBD\_MAX\_NUM\_CONFIGURATION (Maximum number of supported configuration)

1
USBD\_MAX\_STR\_DESC\_SIZ (Maximum size for the string descriptors)

512
USBD\_SELF\_POWERED (Enabled self power)

Enabled

USBD\_DEBUG\_LEVEL (USBD Debug Level) 0: No debug message

USBD\_LPM\_ENABLED (Link Power Management) 1: Link Power Management supported

**Class Parameters:** 

USB CDC Rx Buffer Size 2048
USB CDC Tx Buffer Size 2048

#### 7.30.2. Device Descriptor:

#### **Device Descriptor:**

VID (Vendor IDentifier) 1155

LANGID\_STRING (Language Identifier) English(United States)

MANUFACTURER\_STRING (Manufacturer Identifier) STMicroelectronics

#### **Device Descriptor FS:**

PID (Product IDentifier) 22336

PRODUCT\_STRING (Product Identifier) STM32 Virtual ComPort

CONFIGURATION\_STRING (Configuration Identifier)

INTERFACE\_STRING (Interface Identifier)

CDC Interface

#### \* User modified value

# 8. System Configuration

# 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	ADC_BATT
	PB1	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	ADC_LIN3
	PB11	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	ADC_LIN2
	PB12	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	ADC_LIN1
COMP2	PA7	COMP2_INP	Analog mode	No pull-up and no pull-down	n/a	
COMP4	PB0	COMP4_INP	Analog mode	No pull-up and no pull-down	n/a	SHUNT_LIN3
COMP5	PB13	COMP5_INP	Analog mode	No pull-up and no pull-down	n/a	SHUNT_LIN2
COMP7	PB14	COMP7_INP	Analog mode	No pull-up and no pull-down	n/a	SHUNT_LIN1
I2C2	PA8	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PA9	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
OPAMP1	PA1	OPAMP1_VINP	Analog mode	No pull-up and no pull-down	n/a	SHUNT_MOTOR
	PA3	OPAMP1_VINM0	Analog mode	No pull-up and no pull-down	n/a	
OPAMP2	PA5	OPAMP2_VINM0	Analog mode	No pull-up and no pull-down	n/a	
	PA7	OPAMP2_VINP	Analog mode	No pull-up and no pull-down	n/a	
OPAMP3	PB0	OPAMP3_VINP	Analog mode	No pull-up and no pull-down	n/a	SHUNT_LIN3
	PB2	OPAMP3_VINM0	Analog mode	No pull-up and no pull-down	n/a	
OPAMP4	PB10	OPAMP4_VINM0	Analog mode	No pull-up and no pull-down	n/a	
	PB13	OPAMP4_VINP	Analog mode	No pull-up and no pull-down	n/a	SHUNT_LIN2
OPAMP5	PB14	OPAMP5_VINP	Analog mode	No pull-up and no pull-down	n/a	SHUNT_LIN1
	PB15	OPAMP5_VINM0	Analog mode	No pull-up and no pull-down	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	
TIM1	PF0-OSC_IN	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_TIM1_3N
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINEAR_RIN3
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINEAR_FIN3
TIM4	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINEAR_RIN2
	РВ8-ВООТО	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINEAR_FIN2_TIM4CH3
TIM8	PC13	TIM8_CH4N	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINEAR_FIN1
	PB9	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINEAR_RIN1_TIM8CH3
TIM16	PA6	TIM16_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	led_tim16_1
USART1	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	
GPIO	PC14- OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	gled_pc14
	PC15- OSC32_OU T	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PC15_RTS
	PF1- OSC_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PF1_CTS
	PG10-NRST	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PG10_NRST
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel1	Peripheral To Memory	Low
USART2_RX	DMA2_Channel1	Peripheral To Memory	Low
ADC1	DMA1_Channel2	Peripheral To Memory	Low
ADC2	DMA1_Channel3	Peripheral To Memory	Low
ADC5	DMA1_Channel4	Peripheral To Memory	Low

## USART1\_RX: DMA1\_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Byte
Memory Data Width: Byte

## USART2\_RX: DMA2\_Channel1 DMA request Settings:

Mode: Circular \*
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Byte
Memory Data Width: Byte

## ADC1: DMA1\_Channel2 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Half Word
Memory Data Width: Half Word

### ADC2: DMA1\_Channel3 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Half Word

Memory Data Width: Half Word

# ADC5: DMA1\_Channel4 DMA request Settings:

Mode: Normal

Peripheral Increment: Disable

Memory Increment: Enable \*

Peripheral Data Width: Half Word

Memory Data Width: Half Word

# 8.3. NVIC configuration

# 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
USB low priority interrupt remap	true	0	0
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	true	0	0
DMA2 channel1 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupt	unused		
USB high priority interrupt remap	unused		
TIM1 break interrupt and TIM15 global interrupt		unused	
TIM1 update interrupt and TIM16 global interrupt		unused	
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt		unused	
TIM2 global interrupt	unused		
TIM3 global interrupt		unused	
TIM4 global interrupt	unused		
I2C2 event interrupt / I2C2 wake-up interrupt through EXTI line 24	unused		
I2C2 error interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
TIM8 break interrupt	unused		
TIM8 update interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM8 trigger and commutation interrupts		unused	
TIM8 capture compare interrupt		unused	
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts		unused	
TIM7 global interrupt, DAC2 and DAC4 channel underrun error interrupts		unused	
ADC5 global interrupt		unused	
COMP1, COMP2 and COMP3 interrupts through EXTI lines 21, 22 and 29		unused	
COMP4, COMP5 and COMP6 interrupts through EXTI lines 30, 31 and 32		unused	
COMP7 interrupt through EXTI line 33		unused	
TIM20 break interrupt		unused	
TIM20 update interrupt		unused	
TIM20 trigger and commutation interrupts	unused		
TIM20 capture compare interrupt	unused		
FPU global interrupt		unused	

# 8.3.2. NVIC Code generation

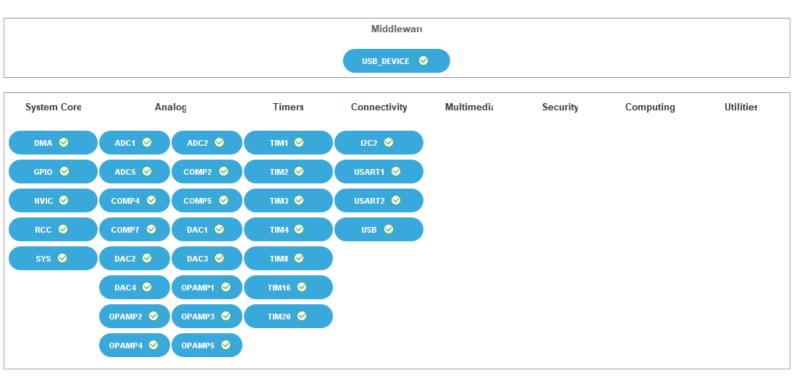
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
USB low priority interrupt remap	false	true	true
USART2 global interrupt / USART2 wake- up interrupt through EXTI line 26	false	true	true
DMA2 channel1 global interrupt	false	true	true

# \* User modified value

# 9. System Views

9.1. Category view

9.1.1. Current



# 10. Docs & Resources

Type Link

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IBIS models https://www.st.com/resource/en/ibis\_model/stm32g4\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32g4\_svd.zip

Description

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Description

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m32g4\_series\_product\_overview.pdf

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