## Project Use Case Scenarios #3 – <PROJECT TITLE HERE>

Names of Team Members, Team Member Role, UCI email addresses:

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### Updated Visual Representation of Project

Include your updated visual from the initial project proposal here (should be your own interpretation of the prototype). At this point, no more hand-drawn images. No AI Generated images.

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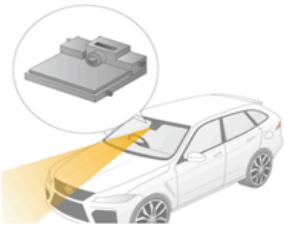
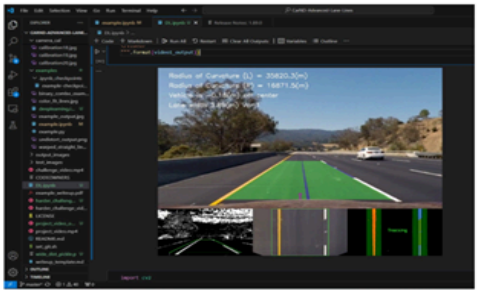


This is a sensing camera in a car that provides DAS or ADAS. It is used for Lane keep assist, Lane center assist.

We are going to use a dash cam as our source camera. We are then going to either record the video of the lane or going to send the video real time to the FPGA


the FPGA is going to process the video and give us the output.

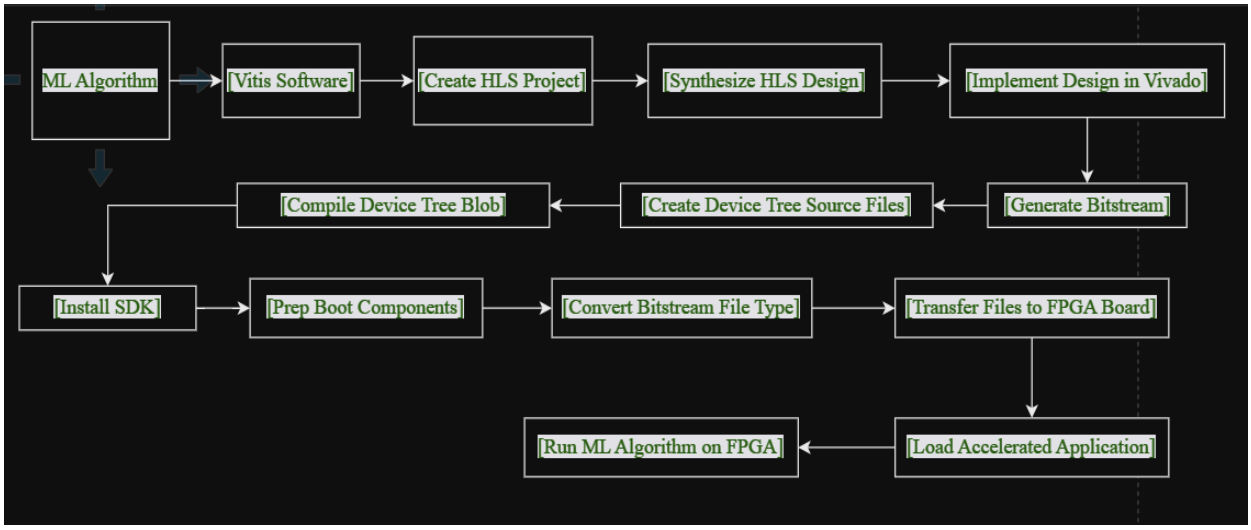
For our initial idea of the project, we will compare the metrics decided between FPGA and multicore. Depending on time and work we might also try using GPU.



Since we can not actuate an actual car, we will try to see if the correction to keep car centered can be provided

### Updated Use Case Scenarios

Show more details (break down flowchart boxes, tasks, etc. into manageable chunks that can be completed in days – not weeks/months)




For advanced lane detection: Compute the camera calibration matrix and distortion coefficients given a set of chessboard images.

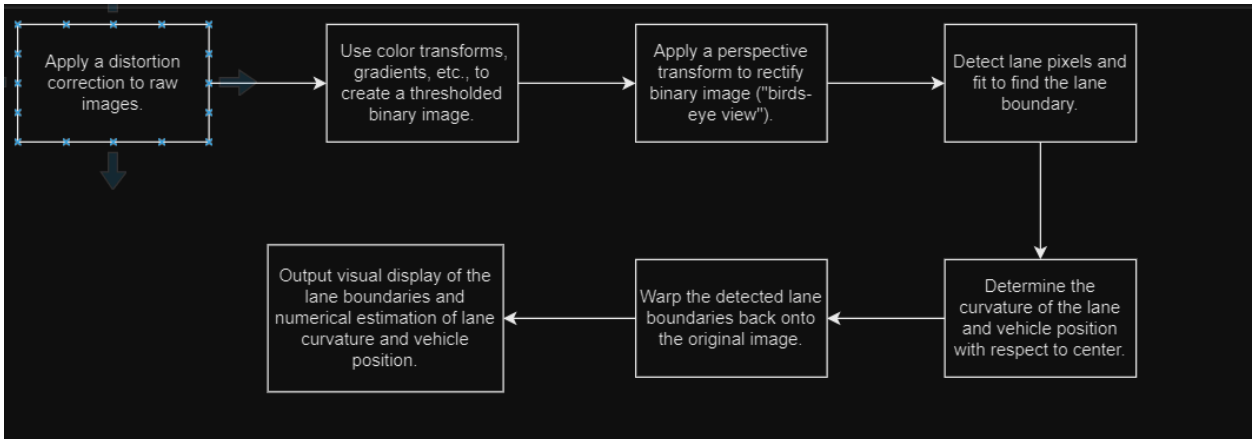



**Table 3 Internal configuration of each camera**

| Equipment name | Circuit configuration |
|---|---|
| Sensing camera<br>Driver monitoring camera | Image sensor → SoC → MCU → Another ECU (ADAS,AD,etc.) |
| Surround view camera | Image sensor → FPGA → MCU → Another ECU (ADAS,IVI,etc.)<br>Another ECU (Surround view ECU) |

## Updated Timeline of TAsks and Planned WorkLoad Split for use case scenarios

- Which planned timeline tasks from draft #2 were successfully completed?

  Setting up the Xilinx Kria Kv260 board.

tutorials of vitis software, embedded.

Finished working on OpenLane dataset to navigate curve roads

Installing SDKs on the Xilinx board

- Which ones were not completed? How will you adjust accordingly during the next 2 weeks?

  dataset hunting to find the best suitable one for edge computing using the fpga board.

  the ICS server crashed. Department has ordered a new server which should arrive this week.

  We will then install vitis on it. Vitis needs 32GB ram and roughly 200GB of storage, which is not suitable for our multi core laptops.

  Once that is handled we will move to the flowchart mentioned above, but will not need to use vivado software.

## Additional Comments / Concerns

If there are comments/concerns you'd like to discuss with your advisor or the instructional team, state them here for reference.