

## PROJECT USE CASE SCENARIOS #1 – FPGA BASED ML EDGE

Names of Team Members, Team Member Role, UCI email addresses:

1. Vishwanath Singh ([vishws1@uci.edu](mailto:vishws1@uci.edu)) Manish Sudhir Sudumbrekar ([msudumbr@uci.edu](mailto:msudumbr@uci.edu))

### UPDATED VISUAL REPRESENTATION OF PROJECT

Include your updated visual from the initial project proposal here (should be your own interpretation of the prototype).



Used from the capstone project pitch provided by professor Eli. We mainly work with the FPGA board and might not require Rpi, since working on the technology is the goal now. The visual may vary when the application is determined.

As of now work is mostly on software development and understanding the working of vitis tool and xilinx board. therefore there are no changes to the image that we could think of with the help of our mentor

### USE CASE SCENARIOS

1. driver assistance system, lane detections
  - identifying objects in lane. (to know if there is an object but no to determine what object it is)
  - identifying objects in adjacent lanes
  - identifying different kind of lines(solid line, double solid yellow, dashed line, double solid white)
  - identifying pedestrian crossing

### TIMELINE OF TASKS AND PLANNED WORKLOAD SPLIT FOR USE CASE SCENARIOS

Taking note by professor into account changes have been made.

- Week 3:
  - Task 5: dataset hunting to find the best suitable one for edge computing using the fgpa board. (2 days)
  - Task 6: setup of the xilinx board. (3 days)
- Week 4:

Task 7: understanding the programming of xilinx kria kv260. (2 days)

(3 days)

- Week 5:

Task 8: learning to work with vitis tool and how to convert models into HDL and upload it onto the xilinx board.

#### ADDITIONAL COMMENTS / CONCERNS

If there are comments/concerns you'd like to discuss with your advisor or the instructional team, state them here for reference.