PROJECT PROGRESS AND STATUS PLAN #1 – <FPGA BASED ML EDGE>

Names of Team Members, Team Member Role, UCI email addresses:

1. Vishwanath Singh (vishws1@uci.edu), Manish Sudumbreaker (msudumbr@uci.edu)

MEETING SUMMARY

Date & summary of latest meeting with your advisor.

Tuesday (Week 2)

Topic of discussion: Setting up Vitis Software and programming the accelerator to be ML model optimized.

What are your planned meeting days/times for this quarter?

Tuesdays 11am

SHORT-TERM GOALS

What short-term goals have you completed from Fall quarter? What did you not complete/what is the status (are you still doing those goals/have they changed/summarize)?

- We have completed working on the machine learning model for our FPGA.
- FPGA setup finished early spring quarter.

- Unable to program accelerator on Xilinx Kria kv260 yet. Still working on it.

- Program the accelerator as early as possible and optimize it for the ML algorithm that we have.

- Test the prototype using a dashcam in a car, around UCI Campus

Do you have new/additional short-term goals for this quarter?

- Learning how to alter accelerators within the Vitis AI.
- Optimize it for ML algorithms based on bias and weights

LONG-TERM GOALS

What is your current end of Fall goal based on your current progress w/ short-term goals? What are your current prototype goals for December? Are your current goals/tasks reasonable and sufficient toward meeting your December goals?

Finish testing of Lane detection algorithms on the FPGA and compare the compute parameters.

Test in car around UCI campus and see scope for improvement. (Similar working concept as last quarter)