PROJECT PROGRESS AND STATUS PLAN #2 – <FPGA BASED ML EDGE>

Names of Team Members, Team Member Role, UCI email addresses:

1. Vishwanath Singh(vishws1@uci.edu), Manish Sudumbrekar(msudumbr@uci.edu).

MEETING FORMAT AND SCHEDULE

How often will you be meeting with your advisor(s) and grad student mentor(s)? Which advisors/mentors? What format will you be meeting with them?

Meeting with Prof Eli Bozorgzadeh once a week, every Thursday at 10 am. The format of the meeting will be in person meetings.

SHORT-TERM GOALS

What is the team's current short-term goal (within the next 2-3 weeks) How can each individual team member contribute to this goal (you may want to discuss this amongst yourselves & propose to your advisor, or discuss it during your first meeting if time allows)

1. Finalising the dataset for our application and if the data is clean and usable.
2. Working on AMD vitis and getting hands on experience with the Xilinx board.
3. Sample examples such as smart camera applications have been tested for the board.
4. Using and training sample datasets on Vitis and figuring out the ML accelerators.

USE CASE SCENARIOS/PROOF-OF-CONCEPT DRAFT DISCUSSION SUMMARY

Summary of initial discussion (it’s okay if the draft is not yet complete)

Use Cases discussed and preferred:

1. Automobile :
    a. Lane Detection
    b. Road Segmentation
2. Drone :
    a. Bird’s eye view of vehicles.
3. Surveillance :
    a. Fire detection
    b. Rain and Snow traffic surveillance
4. Medical :
    a. Bone fracture detection
    b. Portable MRI’s/imagery

BUSINESS CANVAS MODEL DISCUSSION SUMMARY

Summary of initial discussion (it's okay if the draft is not yet complete)

Key Partners:

Key Suppliers: AMD, DigiKey

Key Activities performed by Partners: Providing necessary hardware components, technical support, and potential collaboration in research and development.

Key Activities:

FPGA ML accelerator implementation.

Optimization of accelerator allocation and request processing policies.

Transmission of images from end devices to the FPGA edge node.

Value Propositions:

Energy-efficient acceleration of vision algorithms for edge computing systems.

Enhanced performance and efficiency compared to GPU-based accelerators.

Potential cost savings and increased processing speed.

Customer Relationships:

Establishing and maintaining relationships with customers through technical support, updates on project progress, and addressing any concerns or issues.

Integration with the rest of the business model through customer feedback and continuous improvement.

Customer Segments:

Potential customers include companies or organizations involved in edge computing, IoT (Internet of Things), and image processing applications.

Key Resources:

Physical resources: FPGA devices, embedded devices, development boards, development software.

Intellectual resources: FPGA design tools, ML algorithms, optimization algorithms.

Human resources: Researchers, developers, technical experts.

Channels:

Channels for reaching customer segments may include direct sales, partnerships with technology distributors, and

online marketing.

Integration of channels with customer routines may involve providing tutorials, technical documentation, and customer support services.

Cost Structure:

Fixed costs: Salaries, hardware purchases, development tools.

Variable costs: Maintenance, marketing, customer support.

Economies of scale: Bulk purchases of hardware components, efficient resource utilization.

Revenue Streams:

Revenue from the sale of FPGA devices and related hardware components.

Potential revenue from licensing ML algorithms or offering subscription-based services.

Advertising revenue from marketing the project and related services.