Suggestions for Hardware Evaluation of Cryptographic Algorithms

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hardware evaluations for crypto algorithms.

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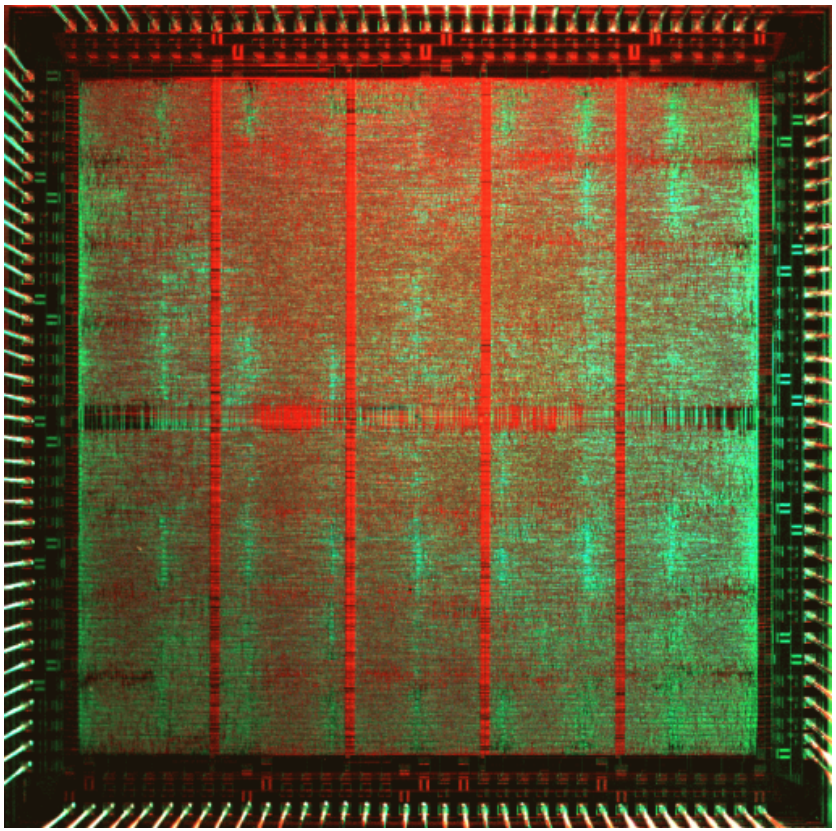
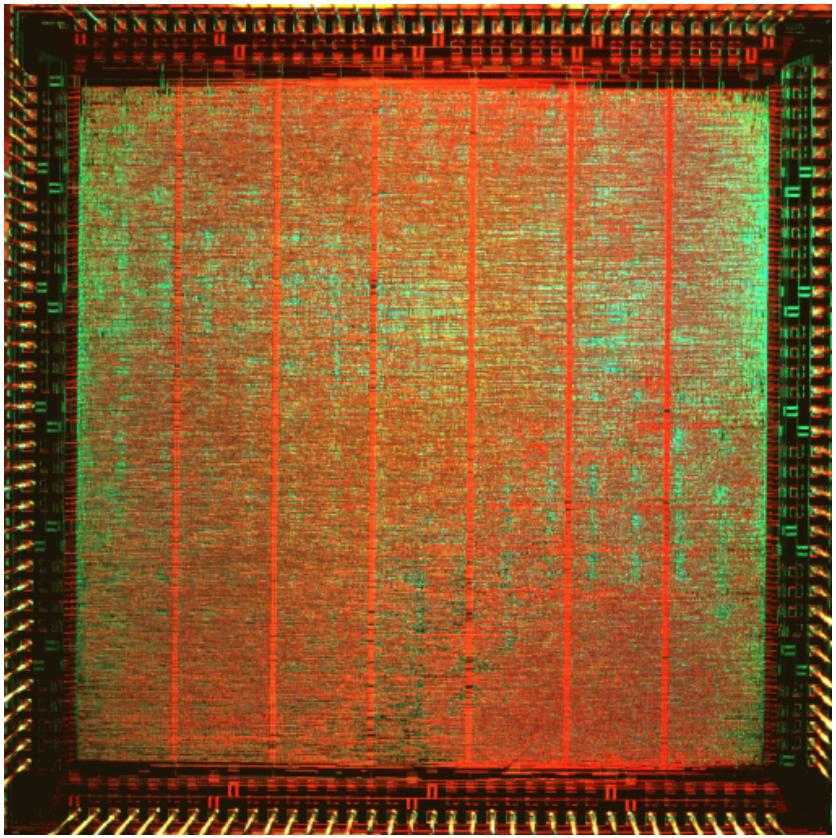
- Is costly (time/money)
  not many are performed
- Different goals, technologies, metrics
- **Studies are** therefore **not comparable**

My Experience: AES

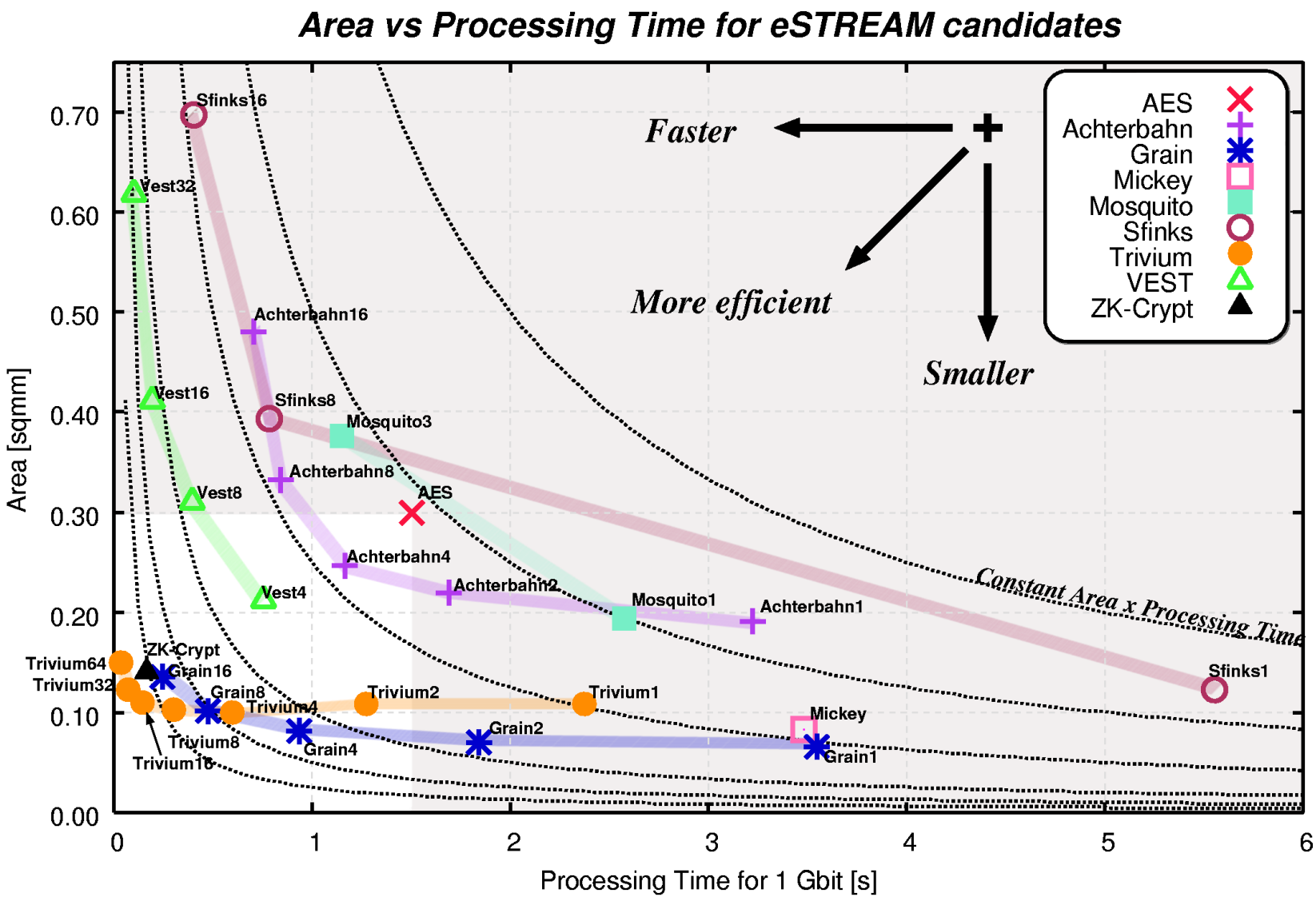




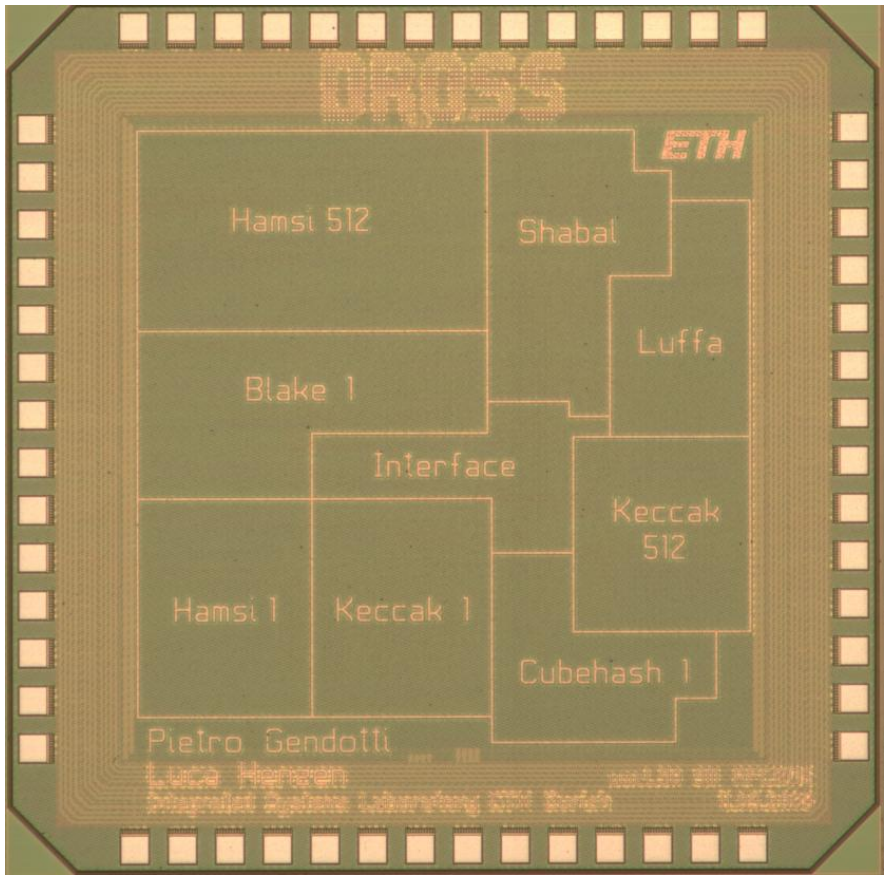
Rijndael and Serpent

http://dx.doi.org/10.1007/3-540-36400-5_12

My Experience: E-stream



My Experience: SHA-3



Collaboration with K. Gaj

http://dx.doi.org/10.1007/978-3-642-15031-9_17

So What is Wrong?

Some observations

- **Hardware design needs constraints!**
  Hardware **design** is an exercise in finding the best circuit that **satisfies** given **constraints**.

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  - Results are not comparable between studies
  - **Can not make conlusions**

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  Hardware **design** is an exercise in finding the best circuit that **satisfies** given **constraints**.
- **Until now**
  - Implementers choose **some** constraints arbitrarily
  - Results are not comparable between studies
  - **Can not make conlusions**
- **Any constraint is better than none**
  The exact constraint is not very important.

What do we suggest ?

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Four suggestions

- Define a **standard testbench**.
- Specify a target **application** scenario.
- State **reference** IC **technology** and FPGA device for comparisons.
- Submitters should **include HDL** code.

#1: Standard Testbench

The call should include a standard testbench for hardware implementations which should read the same KAT files as software models.

Why a Standard Testbench ?

Testbench determines the interface

- I/O bit-widths
- Processing order
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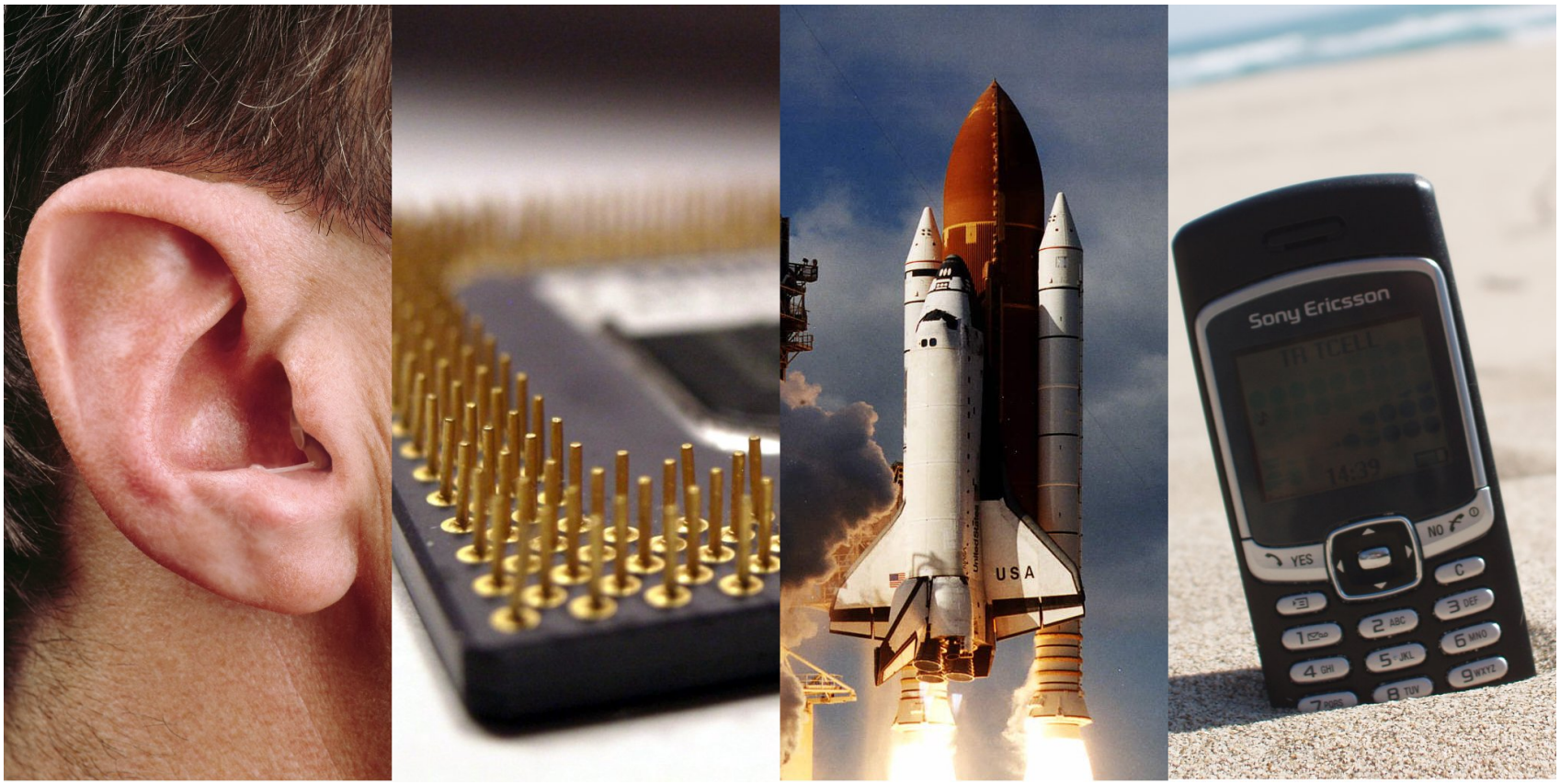
Removes ambiguity about auxillary (non-vital) functions, which may have non-negligable impact on results

#2: Define Application Scenario

The call should include define an application scenario for hardware designs that sets clear constraints for the circuits.

Hardware Design Targets Differ



Scenario Examples

Some suggestions

- **Sensor Node**
  - Messages of 32 to 512 bits
  - Throughput 100 kbits/s
  - Key change every 3 months
  - **Priority** energy consumption
  - Second priority small area

Scenario Examples

Some suggestions

- **Sensor Node**
- **Embedded core**
  - Messages of 32 bits to 4 Mbits
  - Throughput 100 Mbits/s
  - Key change every 10ms
  - **Priority** energy/bit
  - Second priority small area

Scenario Examples

Some suggestions

- **Sensor Node**
- **Embedded core**
- **Data Center**
  - Messages of 2^{10} bits to 2^{64} bits
  - Throughput 10 Gbits/s
  - Key change every 2^{14} bits
  - **Priority** throughput per area
  - Second priority power

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Defining more than one scenario

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Suggestion: **One** rather conservative scenario

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Actual applications will vary

- **The goal is to achieve uniform results**
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  Consistency is more important.
- **Not possible to account for everything!**
  It should not be the goal of the call to do so.
- **Free to evaluate different options**
  Every evaluation should use standard, but free to explore other options.

#3: Choose a Reference Technology

The call should determine a reference technology and standard cell library for ASIC implementations and a reference FPGA device to be used for comparisons.

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Significant differences depending on:

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  Performance of UMC != ST != TSMC

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Fix all these parameters !

Some common gates in GE

Foundry	Tech [nm]	Library	Scan FF [GE]	Full Adder [GE]	OR4 [GE]	AND3 [GE]
man A	28	lib A	7.67	9.00	5.33	1.67
man A	45	lib A	**7.33**	**6.33**	2.67	2.00
man A	45	lib A2	5.67	5.33	2.33	1.67
man A	65	lib A	4.75	5.50	2.50	1.75
man B	65	lib B	5.75	5.25	2.00	1.75
man B	90	lib C	**5.75**	**8.25**	2.25	1.75
man B	130	lib C	6.25	5.50	n.a.	1.75
man C	130	lib D	7.00	8.00	2.33	2.00
man A	130	lib A	6.00	5.33	2.33	2.00
man D	150	lib E	7.67	5.67	2.00	1.67
man B	180	lib C	6.33	6.33	n.a.	2.00
man B	180	lib F	6.33	5.33	2.00	1.67
man B	250	lib F	9.00	5.33	2.00	1.67
man E	250	lib H	6.00	5.33	2.33	1.67
man F	350	lib G	6.67	5.00	2.00	2.00
man F	800	lib G	5.00	n.a.	2.00	1.67

Synthesis Results Comparison

Foundry	Tech [nm]	Lib	Example design Com. Chip [mm^2]	[kGE]	[%]
man A	28	lib A	0.175	358	94%
man A	45	lib A	**0.240**	**352**	93%
man A	45	lib A2	**0.318**	**300**	79%
man A	65	lib A	0.577	278	**73%**
man B	65	lib B	0.434	302	80%
man B	90	lib C	1.015	324	85%
man B	130	lib C	1.585	310	82%
man C	130	lib D	1.722	379	**100%**
man A	130	lib A	1.929	319	84%
man D	150	lib E	2.849	315	83%
man B	180	lib C	**3.335**	**356**	94%
man B	180	lib F	**2.972**	**307**	81%
man B	250	lib F	8.103	341	90%
man E	250	lib H	8.207	304	80%
man F	350	lib G	15.917	292	77%
man F	800	lib G	146.544	284	75%

Comparison of Multiple Designs

Foundry	Tech [nm]	Lib	Math [%]	AES [%]	Skein [%]	Comm [%]
man A	28	lib A	99%	100%	94%	94%
man A	45	lib A	93%	97%	92%	93%
man A	45	lib A2	79%	80%	75%	79%
man A	65	lib A	**73%**	**76%**	**71%**	**73%**
man B	65	lib B	81%	85%	78%	80%
man B	90	lib C	84%	79%	84%	85%
man B	130	lib C	81%	91%	81%	82%
man C	130	lib D	100%	100%	100%	100%
man A	130	lib A	**84%**	**101%**	**87%**	**84%**
man D	150	lib E	85%	86%	84%	83%
man B	180	lib C	93%	98%	90%	94%
man B	180	lib F	81%	91%	81%	81%
man B	250	lib F	92%	91%	88%	90%
man E	250	lib H	84%	82%	78%	80%
man F	350	lib G	77%	77%	73%	77%
man F	800	lib G	73%	75%	80%	75%

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Points to consider

- **Should be widely available**
  MOSIS, CMP or Europractice

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- **Should be widely available**
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- **Affordable**
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- **Not necessarily the latest technology**
  - No inherent advantage for comparisons
  - Models usually not so reliable
  - Suffer from more second and third effects
  - Expensive

Also Define FPGA Device

No Longer Platform Independent

- **Many, specific resources available**
  Constantly increasing
- **Compilers get better everyday**
  More resources can be utilized automatically
- **Should just select one for comparison**
  Allow all resources to be utilized.

#4: HDL code

Every submission should include a functional HDL implementation (Verilog/VHDL).

Why Provide HDL Code

If Hardware performance is important, designers should also invest time/effort to know how their algorithm performs in hardware.

Why Provide HDL Code (II)

Advantages

- **Basis for comparisons**
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Problems

- **More work**
- **Not everyone is a hardware designer**
  Look for collaborations, i.e. Blake

Other Issues

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- **Side Channel Analysis**
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- **Automation (like eBASH)**
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- **Limitations on Comparisons**
  Take care not to inadvertently publish EDA performance tables.

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