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CS 219-1002: Computer Organization
1 April 2021

CS 219 – Assignment #7

Purpose: Become familiar with MIPS cache implementation
Points: 100

Reading/References:

Chapter 5

Assignment:

Answer the following questions:

1) Describe the key features of a program that would exhibit the following traits with regard to ***data*** accesses: [12 pts, 3 pts each]

a) low temporal locality and low spatial locality
Low temporal locality is whenever the CPU accesses a variable and does not access the variable again shortly after. Low spatial locality is whenever the CPU accesses an array element and it does not access the next array element shortly after.
b) high temporal locality
High temporal locality is whenever the CPU accesses a variable and it accesses the variable again shortly after.
c) low spatial locality
Low spatial locality is when the CPU accesses an array element and it does not access the next array element shortly after.
d) high spatial locality
High spatial locality is when the CPU accesses an array element and it accesses the next array element shortly after.

2) Describe the key features of a program that would exhibit the following traits with regard to ***instruction*** fetches: [12 pts, 3 pts each]

a) low temporal locality
Low temporal locality is whenever the CPU executes an instruction and it does not access the same instruction in the loop shortly after.
b) high temporal locality
High temporal locality is whenever the CPU executes an instruction and it accesses the same instruction in the shortly after.

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c) low spatial locality
Low spatial locality is whenever the CPU executes an instruction involving an array element and it does not execute the instruction involving the next array element in the loop shortly after or there are a lot of jumps to far away places.
d) high spatial locality
High spatial locality is whenever the CPU executes an instruction involving an array element and it executes the instruction involving the next array element shortly after or there are little to no branches or jumps at all.

3) A new processor can use either a write-through or write-back cache, selectable through software. [8 pts, 4 pts each]

a) Assume the processor will run data-intensive applications with a large number of load and store operations. Explain which cache write policy should be used.
A write-back cache should be used because processors can generate writes as fast or faster than the writes can be handled by main memory. The new value is written only to the block in the cache and the modified block is written to the lower level of the hierarchy when it is replaced.

b) Consider the same question but this time for a safety-critical system in which data integrity is more important than memory performance. Explain which cache write policy should be used.
In this situation, a write-through cache should be used because the data integrity can be kept by updating both the cache and the next lower level of the memory hierarchy.

4) Here is a series of address references given as words addresses:
1, 2, 3, 4, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, 4, 5, and 11.

a) Assuming a direct-mapped cache with 8 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the contents of the cache (including previous, over-written values). You do not need to show the tag field. When done, include the hit ratio. [3 pts]

1, 2, 3, 4, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, 4, 5, and 11.

blue = hit

Cache Set	v	Address
000	1	16,64,48
001	1	1
010	1	2
011	1	3,11,19,11,3,27,11

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100	1	4
101	1	21,13,5
110	1	22,6
111	0	NA

Hit ratio = 2 / 20 = 10%

b) Show the hits and misses and cache contents (including previous, overwritten values) for a direct-mapped cache with four-word blocks and a total size of 8 words. You do not need to show the tag field. When done, include the hit ratio. [3 pts]

1, 2, 3, 4, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, 4, 5, and 11.

blue = hit

Cache Set	v	Address
00	1	[0,1,2,3][8,9,10,11][16,17,18,19][64,65,66,67] [48,49,50,51][16,17,18,19][8,9,10,11][0,1,2,3] [24,25,26,27][8,9,10,11]
01	1	[4,5,6,7][20,21,22,23][12,13,14,15][20,21,22,23] [4,5,6,7]

Hit ratio = 5 / 20 = 25%

5) Here is a series of address references given as words addresses:
3, 7, 10, 13, 64, 48, 19, 2, 3, 11, 16, 21, 11, 3, 22, 4, 27, 6, 12, 3, 16, 17, 44, 21, and 12.

a) Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the contents of the cache (including previous, overwritten values). You do not need to show the tag field. When done, include the hit ratio. [7 pts]

3, 7, 10, 13, 64, 48, 19, 2, 3, 11, 16, 21, 11, 3, 22, 4, 27, 6, 12, 3, 16, 17, 44, 21, and 12.

blue = hit

Cache Set	v	Address
0000	1	64,48,16
0001	1	17
0010	1	2,
0011	1	3,19,3
0100	1	4

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0101	1	21
0110	1	22,6
0111	1	7
1000	0	NA
1001	0	NA
1010	1	10
1011	1	11,27
1100	1	12,44,12
1101	1	13
1110	0	NA
1111	0	NA

Hit ratio: 2 / 25 = 8%

b) Show the hits and misses and cache contents (including previous, overwritten values) for a direct-mapped cache with four-word blocks and a total size of 16 words. You do not need to show the tag field. When done, include the hit ratio. [7 pts]

3, 7, 10, 13, 64, 48, 19, 2, 3, 11, 16, 21, 11, 3, 22, 4, 27, 6, 12, 3, 16, 17, 44, 21, and 12.

blue = hit

Cache Set	v	Address
00	1	[0,1,2,3][64,65,66,67][16,17,18,19][0,1,2,3] [16,17,18,19]
01	1	[20,21,22,23]
10	1	[4,5,6,7][8,9,10,11][48,49,50,51]
11	1	[12,13,14,15][44,45,46,47][12,13,14,15]

Hit ratio: 2 / 25 = 8%

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6) Here is a series of address references given as words addresses:
5, 18, 1, 2, 3, 11, 16, 21, 8, 9, 13, 19, 11, 3, 10, 22, 4, 27, 6, 24, 16, 11, 49, 13, and 21.

a) Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the contents of the cache (including previous, overwritten values). You do not need to show the tag field. When done, include the hit ratio. [9 pts]

5, 18, 1, 2, 3, 11, 16, 21, 8, 9, 13, 19, 11, 3, 10, 22, 4, 27, 6, 24, 16, 11, 49, 13, and 21.

blue = hit

Cache Set	v	Address
0000	1	16
0001	1	1,49
0010	1	18,2
0011	1	3,19,3
0100	1	4
0101	1	5,21
0110	1	22,6
0111	0	NA
1000	1	8,24
1001	1	9
1010	1	10
1011	1	11,27, 11
1100	0	NA
1101	1	13
1110	0	NA
1111	0	NA

Hit ratio: 4 / 25 = 16%

b) Show the hits and misses and cache contents (including previous, overwritten values) for a direct-mapped cache with four-word blocks and a total size of 16 words. You do not need to show the tag field. When done, include the hit ratio. [9 pts]

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5, 18, 1, 2, 3, 11, 16, 21, 8, 9, 13, 19, 11, 3, 10, 22, 4, 27, 6, 24, 16, 11, 49, 13, and 21.
blue = hit

Cache Set	v	Address
00	1	[16,17,18,19][0,1,2,3][16,17,18,19][0,1,2,3] [16,17,18,19][48,49,50,51]
01	1	[4,5,6,7][20,21,22,23][4,5,6,7][20,21,22,23]
10	1	[8,9,10,11][24,25,26,27][8,9,10,11]
11	1	[12,13,14,15]

Hit ratio: 10 / 25 = 40%

7) Here is a series of address references given as words addresses:
7, 8, 2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, 7, 3, and 11.
black = hit

Show the hits and misses and cache contents (including previous, over-written values) for a two-way set-associative cache with one-word blocks and a total size of 16 words. You do not need to show the tag field. Assume LRU replacement. When done, include the hit ratio. [9 pts]

Block 0 Block 1

Set #	v	Address
000	1	8,64
001	0	NA
010	1	2
011	1	3,19,3
100	1	4
101	1	21
110	1	22
111	1	7

Set #	v	Address
000	1	16,48
001	0	NA
010	0	NA
011	1	11,11,27, 11
100	0	NA
101	1	13
110	1	6
111	0	NA

Hit Ratio: 3 / 20 = 15%

8) Here is a series of address references given as words addresses:

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13, 64, 48, 19, 2, 3, 11, 16, 21, 11, 3, 22, 4, 27, 6, 12, 4, 7,8, and 24.
black = hit

Show the hits and misses and cache contents (including previous, over-written values) for a two-way set-associative cache with one-word blocks and a total size of 16 words. You do not need to show the tag field. Assume LRU replacement. When done, include the hit ratio. [9 pts]

Block 0 Block 1

Set #	v	Address
000	1	64,16,24
001	0	NA
010	1	2
011	1	19,11,27
100	1	4
101	1	13,21
110	1	22
111	1	7

Set #	v	Address
000	1	48,8
001	0	NA
010	0	NA
011	1	3
100	1	12
101	0	NA
110	1	6
111	0	NA

Hit ratio: 3 / 20 = 15%

9) As discussed in class, associativity typically improves the miss ratio. However, this is not always true. Provide an explanation or an example of a short series of address references for which a two-way set-associative cache with LRU replacement would experience more misses than a direct-mapped cache of the same size. [6 pts]

Consider a 32 entry direct mapped cache vs 16 entry 2-way associative cache (sizes do not matter, chosen to help illustrate).
Then consider address references of 1, 17, 33.

```
A: 1  % 32 = 1        A: 1  % 16 = 1
B: 17 % 32 = 17       B: 17 % 16 = 1
C: 33 % 32 = 1        C: 33 % 16 = 1
```

After repeating the address references and mapping the cache contents, it is evident that after the first mapping of 1, 17, 33, the hit ratio is approximately 33% or ⅓. For the 16 entry 2-way associative cache, due to two-way set-associative cache with LRU replacement, the hit ratio after the first mapping of 1, 17, 33 is 0%.

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10) Given a direct-mapped cache that will contain 32,768 bytes of data and four-word blocks (where each word is 4 bytes) and assuming 32-bit addressing;

a) How many ***additional bits*** are required for the overhead associated with the 32,768 bytes of data? [4 pts]
Assuming 32-bit addressing with 4 word-blocks, 4 bits are used for the offset, 11 bits are used for the line (2^{11} = 2048 lines of cache from 32,768 / 16 bytes), and 17 bits are used for the tag. The overhead consists of the 1 valid bit and 17 bits for the tag for a total of 18 bits. To calculate the additional bits for the overhead associated with 32,768 bytes of data, it is 18 bits * 2048 lines of cache = 36,864 bits.

b) What is the overhead (additional space required) for the 32,768 bytes of data, expressed as a percentage? [2 pts]
To compute the percentage:
32,768 bytes * 8 = 262,144 bits

262,144 bits + 36,864 bits = 299,008 bits (total)

36,864 (overhead) / 299,008 (total) = 0.12328 * 100 = 12.3%

Must show work for full credit.