UNIVERSITY OF NEVADA LAS VEGAS. DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING LABORATORIES.

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Instructor's comments:

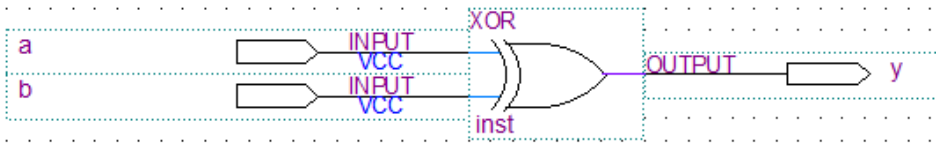
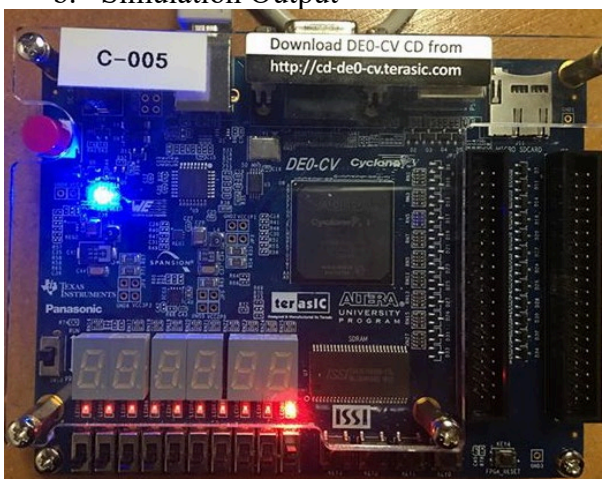
1. Introduction / Theory of Operation

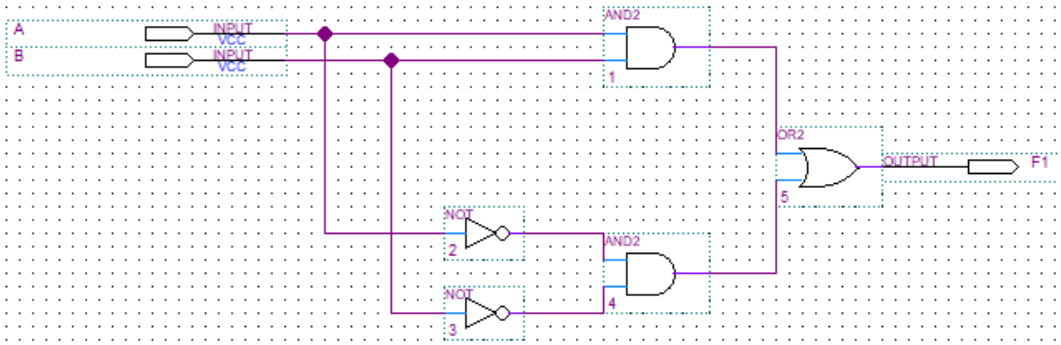
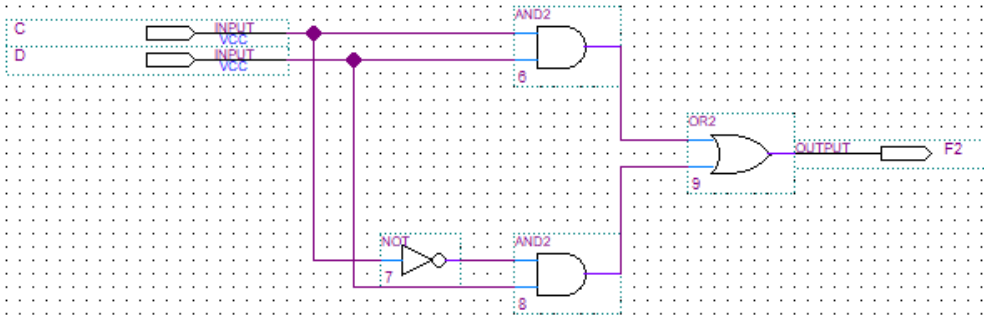
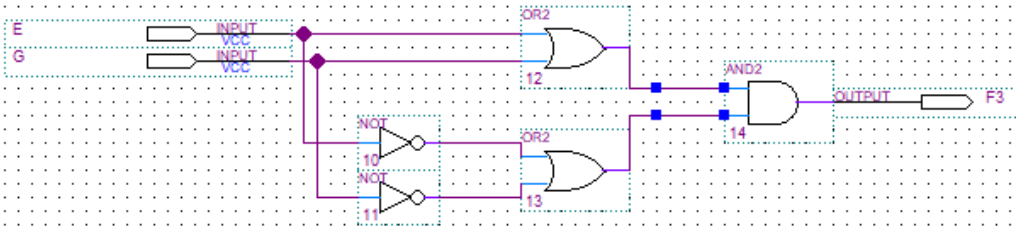
Lab 5 is an introduction to DE0 Board, where we are supposed to get familiar with the DE0 board installation, properties, and usage. In this lab, we also program simple circuits using Altera Quartus.

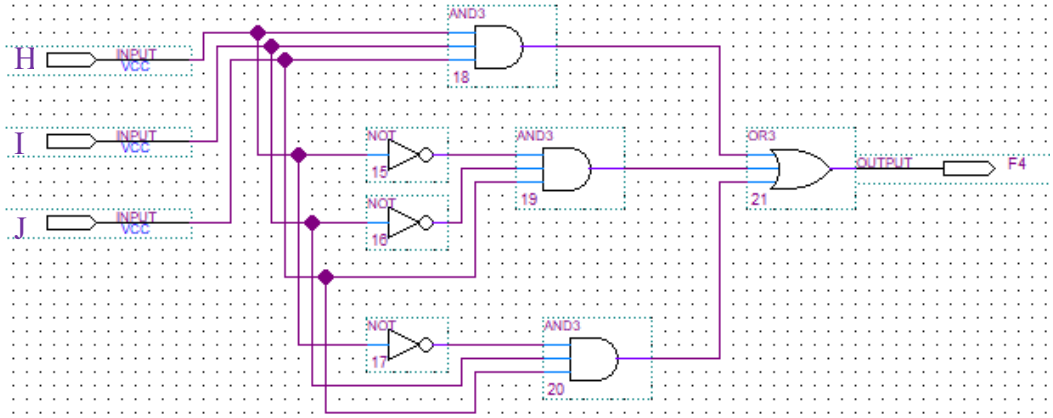
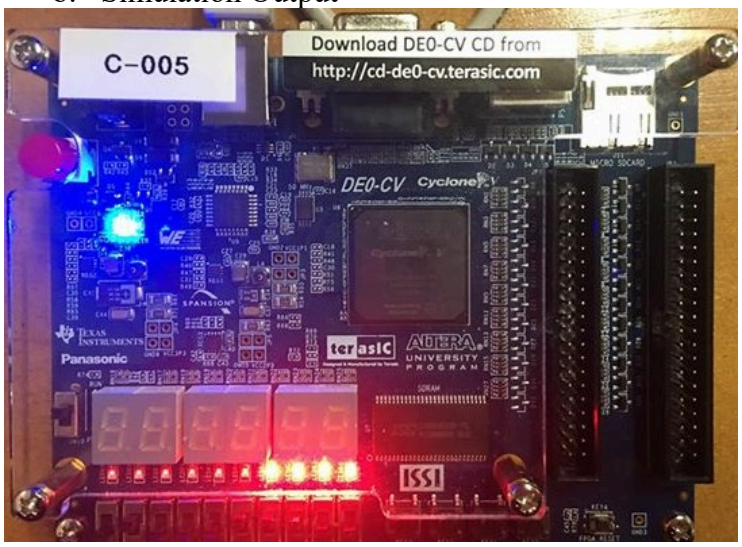
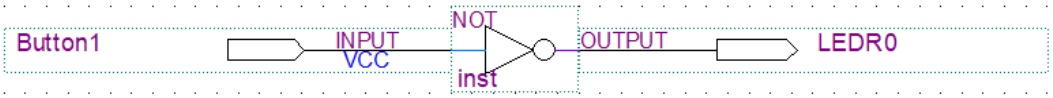
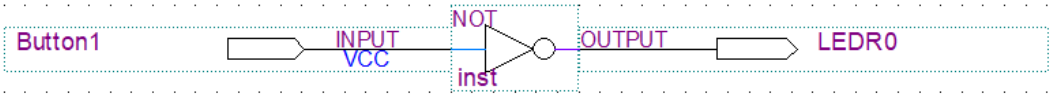
2. Prelab report

My prelab report will be attached with the submission.

3. Results of the experiments

Exp.	Experiment Results
1	a. Quartus Schematic  b. Simulation Output  c. The initial setup of the DE0 board by plugging in the USB-Blaster was the most difficult part of installation of the DE0 board because it was not

	appearing in the "Other devices" drop-down in the Device Manager. In order to solve this issue, we decided to be patient with the software and tried plugging in the USB-Blaster again until it worked properly. All other aspects of installing and assigning the pins to the DE0 board were quite straightforward and satisfactory when the circuits worked and lit up the LED.
2	a. Quartus Schematic F1= AB + A'B'  F2 = CD + C'D  F3 = (E+G)(E'+G') 

	F4 = HIJ + H'I'J + H'JI  b. Simulation Output 
3	a. Quartus Schematic  b. Name of the pins of pushbutton and LED The name of the pin for the pushbutton is KEY0, PIN_U7, Push-button[0] and LEDR0, PIN_AA2, LED[0].
4	a. Quartus Schematic  b. Pin numbers used, along with GPIO bank name The pin number used for the pushbutton is PIN_U7 and GPIO 1 PIN_A12. c. Names of pins (assignments) for button and GPIO pin used KEY0 for the pushbutton and GPIO_1[1].

4. Answer the questions

1) The SOF file is associated with Quartus II. SOF stands for Quartus II SRAM Object File. They are binary files containing data for configuring SRAM-based devices (FPGA) using the Intel Quartus software Program Device. The programmer looks into the SOF file and gets the programming bit stream for the device.
2) The RUN position allows the FPGA to be programmed using the Quartus II Programmer to select a configuration bit stream file with the .sof filename extension. It configures the FPGA in JTAG mode. The PROG position allows the EPCS64 chip to be programmed using the Quartus II Programmer to select a configuration bit stream file with the .pof filename extension. It configures the AS mode.
3) The DE0-CV presents a robust hardware design platform built around the Altera Cyclone V FPGA, which is optimized for the lowest cost and power requirement for transceiver applications with industry-leading programmable logic for ultimate design flexibility. By leveraging all of these capabilities, the DE0-CV is the perfect solution for showcasing, evaluating, and prototyping the true potential of the Altera Cyclone V FPGA.

5. Conclusions

Prior to this lab, we only knew how to program circuits on a breadboard and some wires. After this lab, we realized that it is much more convenient to program circuits using the DE0-CV board because there are much more pins and much more organized. The pins all have their own buttons and the LED already have resistors. It is also much easier to figure out which input is on or off because of the slide switches. The problem we encountered was how to make the four functions show up on the DE0-CV board at the same time. In order to solve this issue, we realized that we could design four circuits on one block/schematic file and the only obstacle to overcome would be how to keep organized throughout the lab.