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Instructor's comments:

Introduction / Theory of operation

Lab 5 is an introduction to the DE0 Board, which requires that we get familiar with the DE0 board installation, properties, and usage. In order to get familiar with the DE0 board, we must program a simple circuit using Altera Quartus.

Prelab main content

The DE0-CV board presents a hardware design platform built around the Altera V FPGA. The purpose of the DE0-CV board is to showcase, evaluate, and prototype the Altera Cyclone V FPGA. The package contains the DE0-CV board, a Type A to B USB Cable, and a 5V DC Power Supply. The Cyclone V FPGA contains sufficient power, cost, and performance levels for high-volume applications.

The DE0-CV board comes with a Control Panel program that allows users to access various components on the board from a host computer, verify the functionality of components on the board, and debug while developing RTL code. The host computer communicates with the board through the USB connection.

The DE0-CV computer contents are implemented in the Altera Cyclone V FPGA chip. The FPGA implements two Nios II processors and several peripheral ports such as memory, timer modules, video-in/out, PS/2, and parallel ports connected to switches and lights.

The Altera Nios II processor is a 32 bit CPU that can be implemented in an Altera FPGA device. The DE0-CV Computer includes two fast Nios II processors.

The DE0-CV Computer has an SDRAM port, as well as two memory modules implemented using the on-chip memory inside the FPGA. The SDRAM Controller in the FPGA provides an interface to the 64MB synchronous dynamic RAM (SDRAM). The on-chip memory is a 256-Kbyte memory implemented inside the FPGA is used as a pixel buffer for the video-out port. The on-chip memory character buffer is an 8-Kbyte memory implemented inside the FPGA that is used as a character buffer for the video-out port.

There are several parallel ports implemented that support input, output, and bidirectional transfers of data between the Nios II processor and I/O peripherals. The red LED parallel port

contains red lights $LEDR_{9-0}$ that are driven by an output parallel port. This 10-bit write-only Data register can be written using word accesses and the upper bits not used in the registers are ignored. The 7-segment displays parallel port each comprises a 32-bit write-only Data register. The data can be written into the registers by using word operations, which directly controls the segments of each display. The SW_{9-0} slider switches on the DE0-CV board are connected to an input parallel port and comprises a 10-bit read-only Data register. The pushbutton key parallel port is connected to the KEY_{3-0} pushbutton switches and comprises three 4-bit registers that can be accessed using word operations. The read-only Data register provides the values of the switches KEY_{3-0}. The expansion parallel port includes two bidirectional parallel ports that are connected to JP1 and JP2 40-pin headers. These parallel ports include four 32-bit registers, D_{31-0}, assigned to the pins on the connector. Only 32 of 36 data pins that appear on each connector can be used. The parallel ports have a convenient platform for experimenting with Nios II assembly language or C code.

The DE0-CV includes an SD-card port. The instructions for using the SD-card device can be found in the manual for the DE0-CV Development and Education board.

The JTAG port implements a communication link between DE0-CV board and host computer. The link is used by Altera Quartus II software to transfer FPGA programming files to DE0-CV board, and by Altera Monitor Program.

The DE0-CV Computer includes a timer module implemented in the FPGA that can be used by the Nios II processor. This interval timer can be loaded with a preset value, then counts down using 100-MHz clock. The programming interface includes six 16-bit registers.