UNIVERSITY OF NEVADA LAS VEGAS. DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING LABORATORIES.

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Instructor's comments:

Introduction / Theory of operation

Lab 7 is about 2-bit ALU and 7-segment display, where we design 1-bit and 2-bit arithmetic logic units and implement the circuits on the DE2 board. We will also learn how to use DE2's 7-segment display.

Prelab main content

1) 7-segment display truth table:

Inputs				Outputs						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0

K-map for a:

Y		AB			
		00	01	11	10
CD	00	1	0	1	1
	01	0	1	1	1
	11	X	X	X	X
	01	1	1	X	X

a = A + C + BD + B'D'

K-map for b:

Y		AB			
		00	01	11	10
CD	00	1	1	1	1
	01	1	0	1	0
	11	X	X	X	X
	01	1	1	X	X

b = B’ + C’D’ + CD

K-map for c:

Y		AB			
		00	01	11	10
CD	00	1	1	1	0
	01	1	1	1	1
	11	X	X	X	X
	01	1	1	X	X

c = B + C’ + D

K-map for d:

Y		AB			
		00	01	11	10
CD	00	1	0	1	1
	01	0	1	0	1
	11	X	X	X	X
	01	1	1	X	X

d = B’D’ + CD’ + BC’D + B’C + A

K-map for e:

Y		AB			
		00	01	11	10
CD	00	1	0	0	1
	01	0	0	0	1
	11	X	X	X	X
	01	1	0	X	X

e = B’D’ + CD’

K-map for f:

Y		AB			
		00	01	11	10
CD	00	1	0	0	0
	01	1	1	0	1
	11	X	X	X	X
	01	1	1	X	X

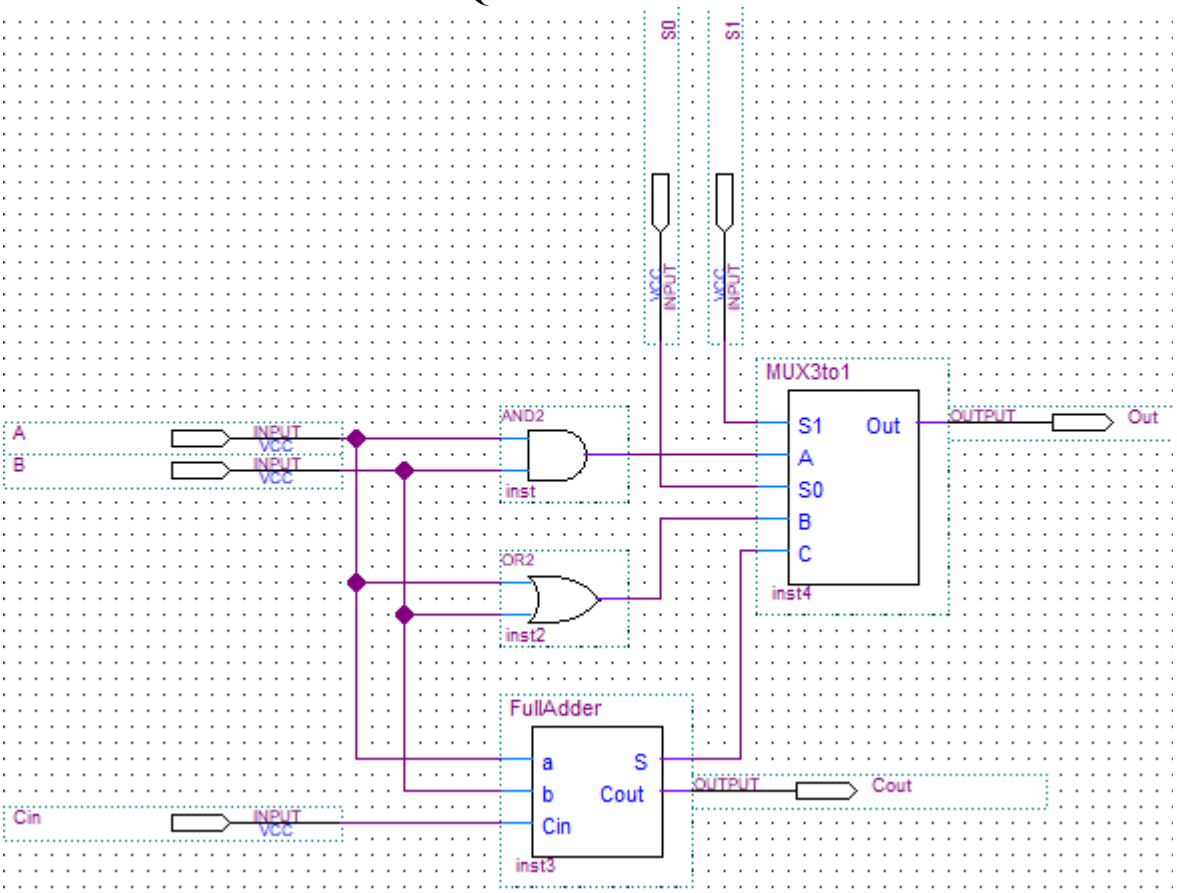
f = A + C’D’ + BC’ + BD’

K-map for g:

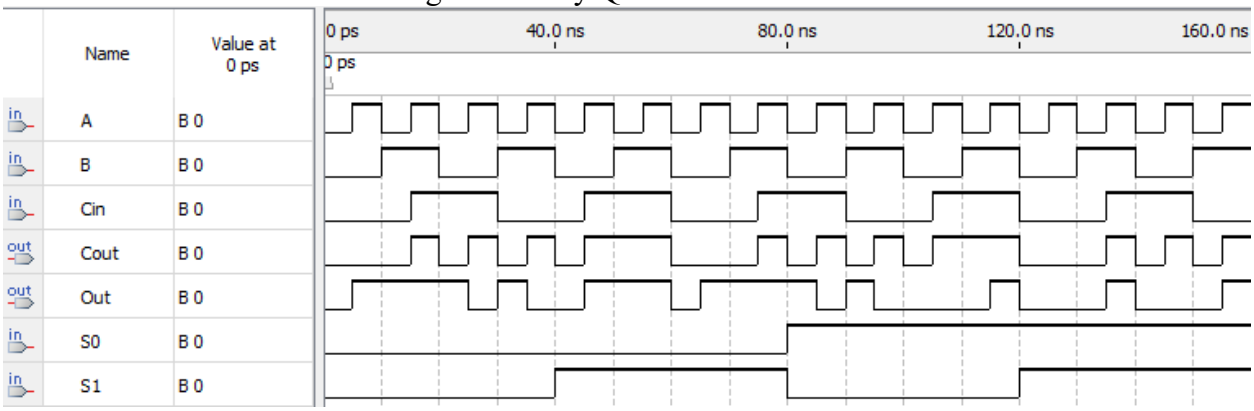
Y		AB			
		00	01	11	10
CD	00	0	0	1	1
	01	1	1	0	1
	11	X	X	X	X
	01	1	1	X	X

g = A + BC’ + B’C + CD’

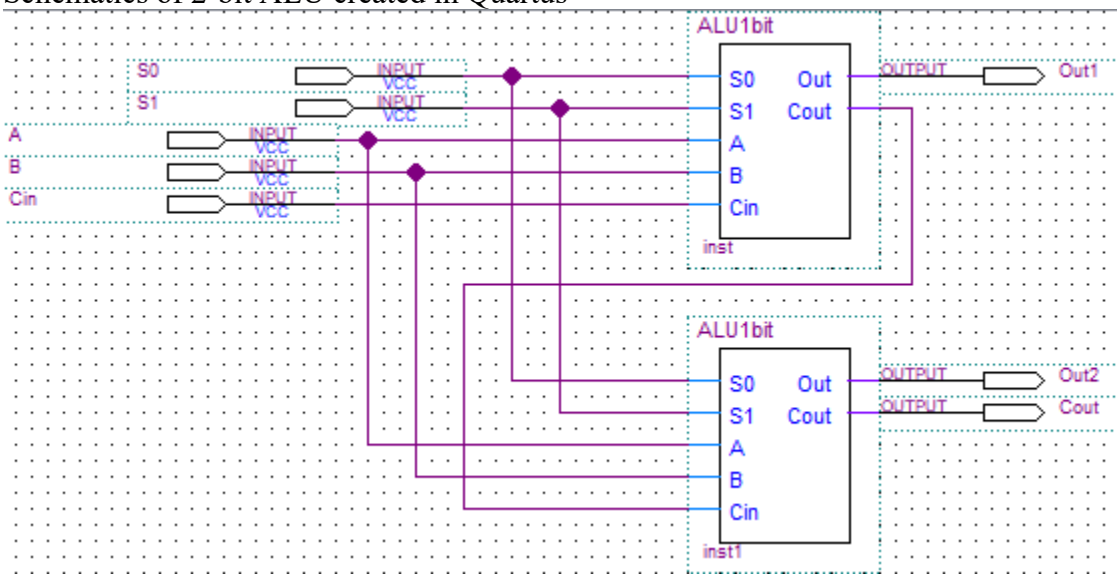
2) Schematics of 1-bit ALU created in Quartus



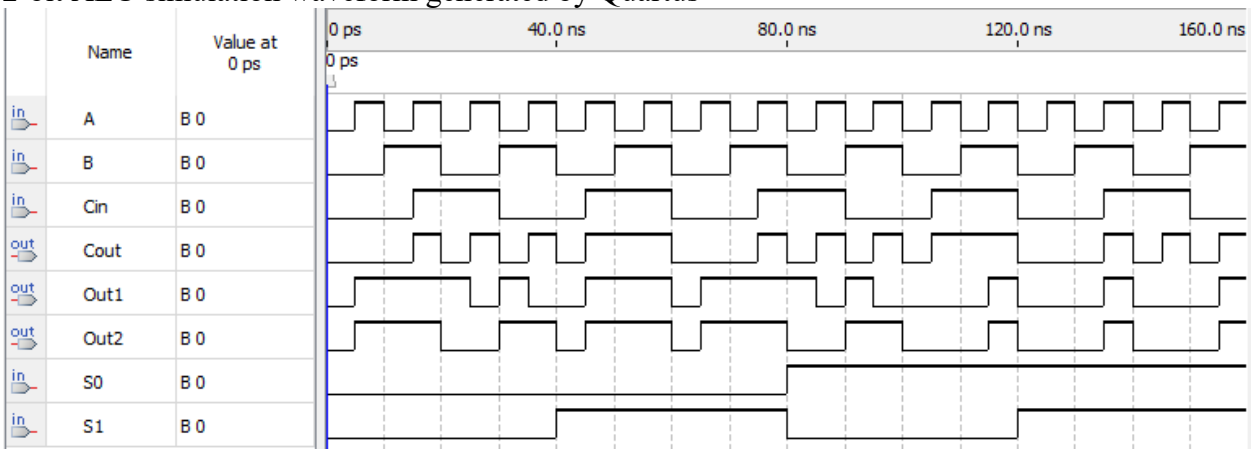
3) 1-bit ALU simulation waveform generated by Quartus



4) Schematics of 2-bit ALU created in Quartus



5) 2-bit ALU simulation waveform generated by Quartus



6) A bitwise operation operates on one or more bit patterns at the level of their individual bits. It is a simple and fast action that is supported by the processor and is used to manipulate values. An example is bitwise AND where the result of 6 & 3 is 2.