

Class:	CPE100L - 1002	Semester:	Spring 2020
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		Document topic:	Prelab 8
Instructor's comments:			

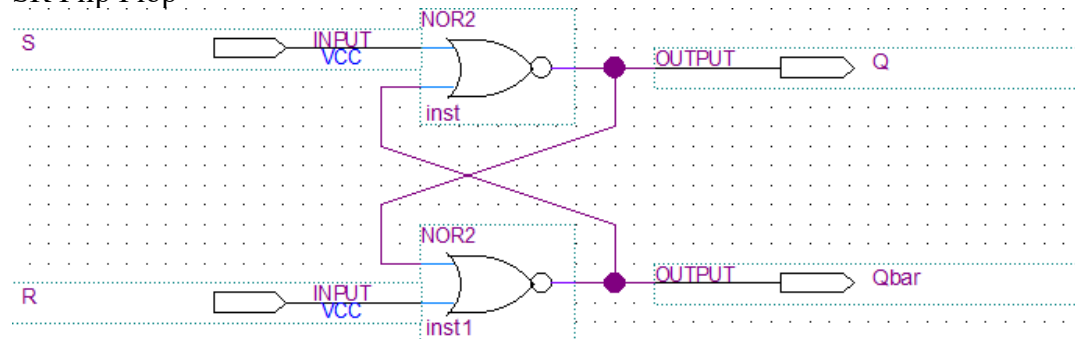
## Introduction / Theory of operation

Lab 8 is about getting familiar with sequential elements, such as flip-flops, which state depends on input signals and previous flip-flop states.

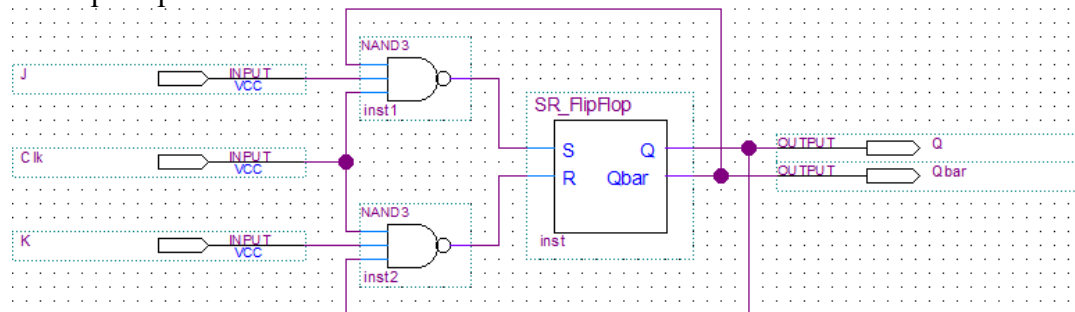
## Prelab main content

### 1) Schematics created in Quartus

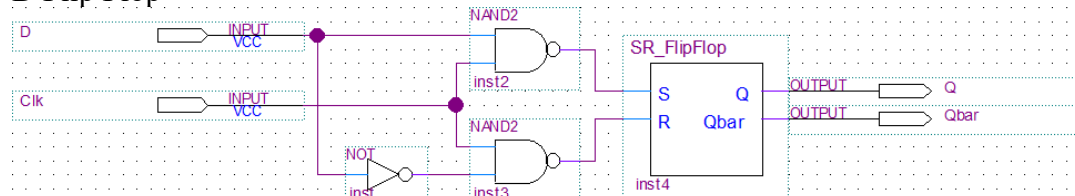
#### SR Flip Flop



#### JK Flip Flop



#### D Flip Flop



The diagram shows a logic circuit for a 2-bit memory element. It has two inputs: 'In' and 'Clk', both connected to a 'VCC' supply. The circuit consists of several NAND gates (labeled NAND2) and a NOT gate (labeled NOT1). The 'In' input is connected to the top input of NAND2 (inst2) and the top input of NAND2 (inst4). The 'Clk' input is connected to the bottom input of NAND2 (inst2) and the bottom input of NAND2 (inst3). The output of the NOT1 gate is connected to the bottom input of NAND2 (inst1). The outputs of NAND2 (inst1) and NAND2 (inst3) are connected to the inputs of NAND2 (inst4). The output of NAND2 (inst2) is connected to the input of NAND2 (inst1). The output of NAND2 (inst4) is connected to the 'OUTPUT' port, which is also connected to the 'Out' output.

## SR Flip Flop

