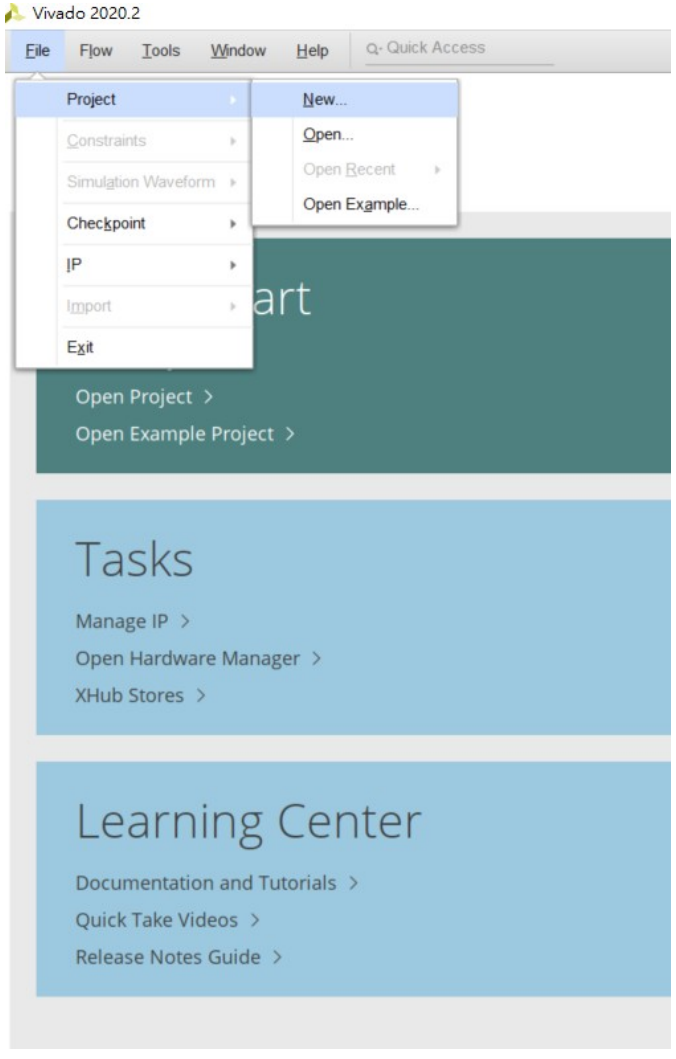
Lab0: Create a Project in Vivado and Verilog Practice

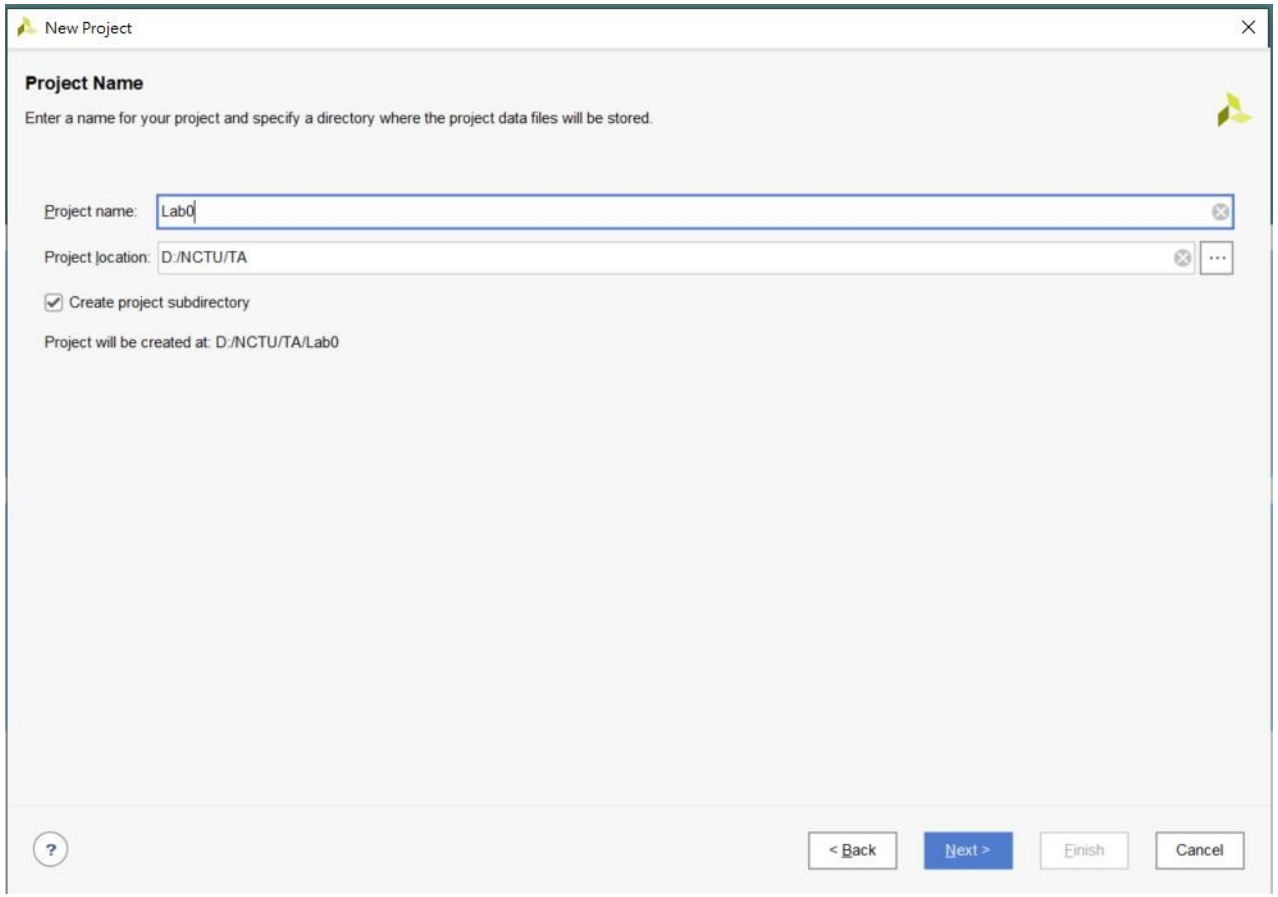
Step1

- Create a new project



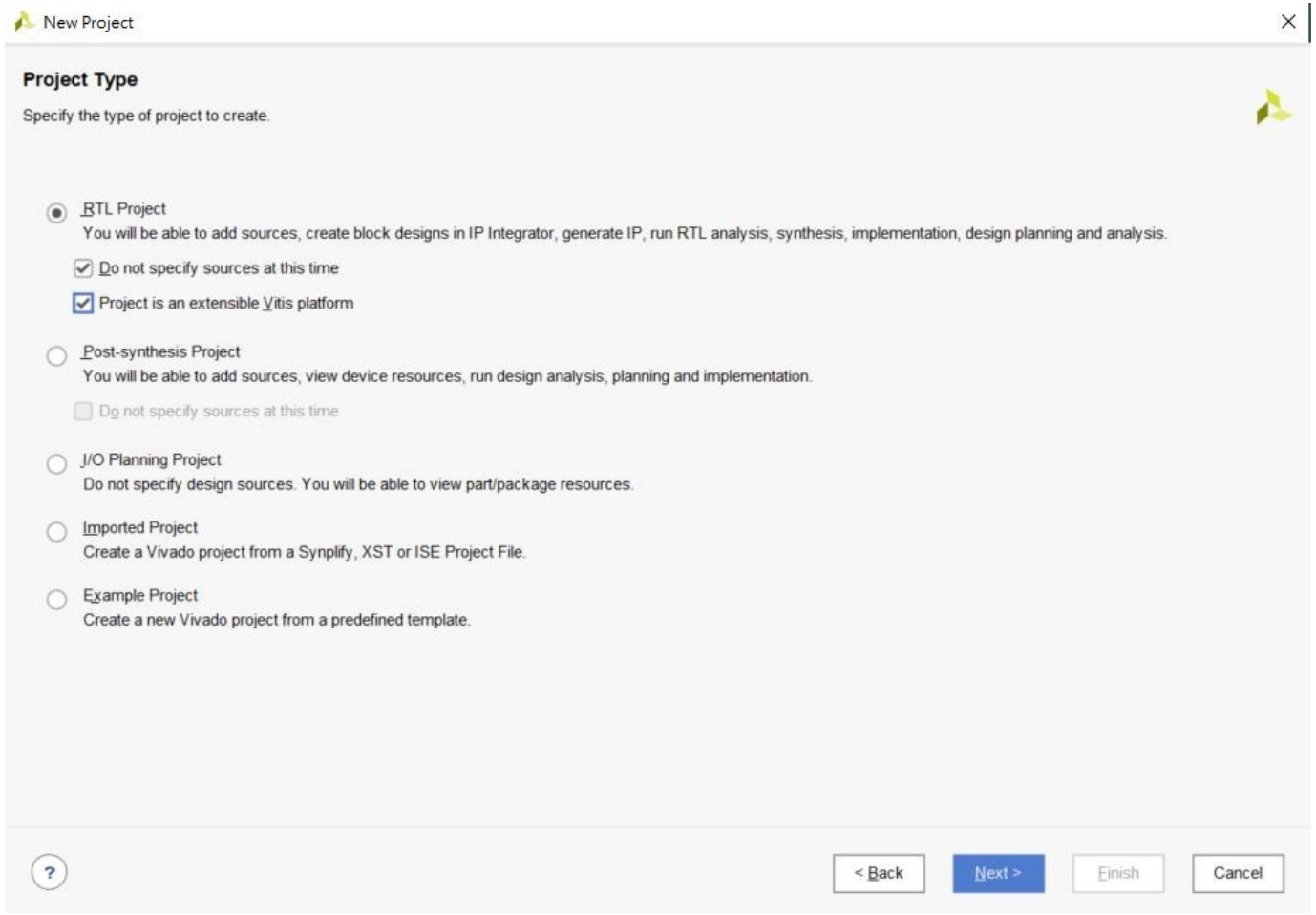
Step2

- Input project name and location



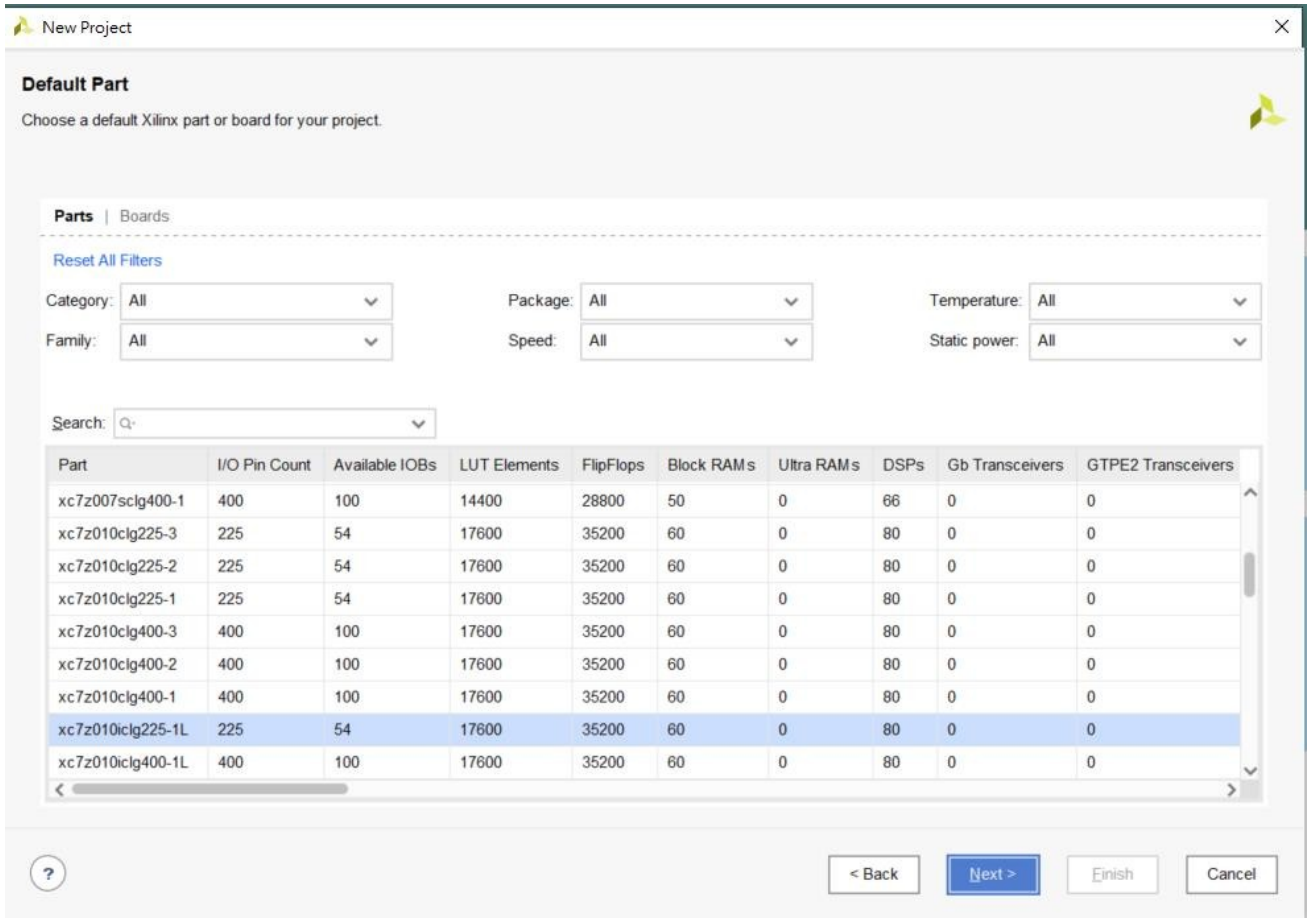
Step3

- RTL project

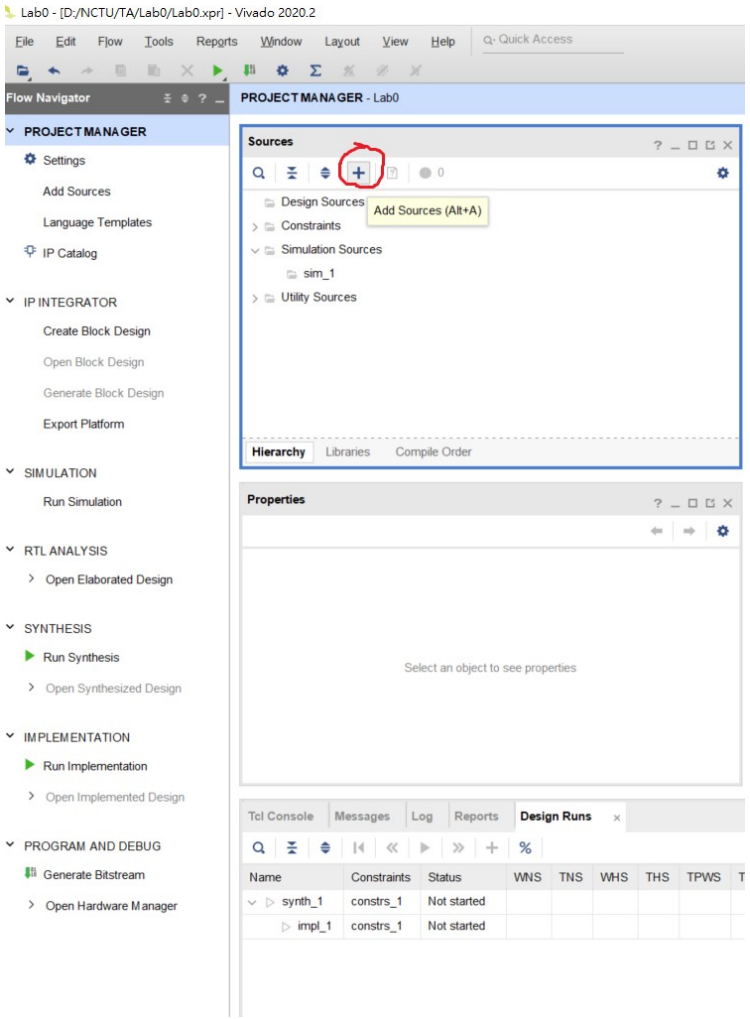


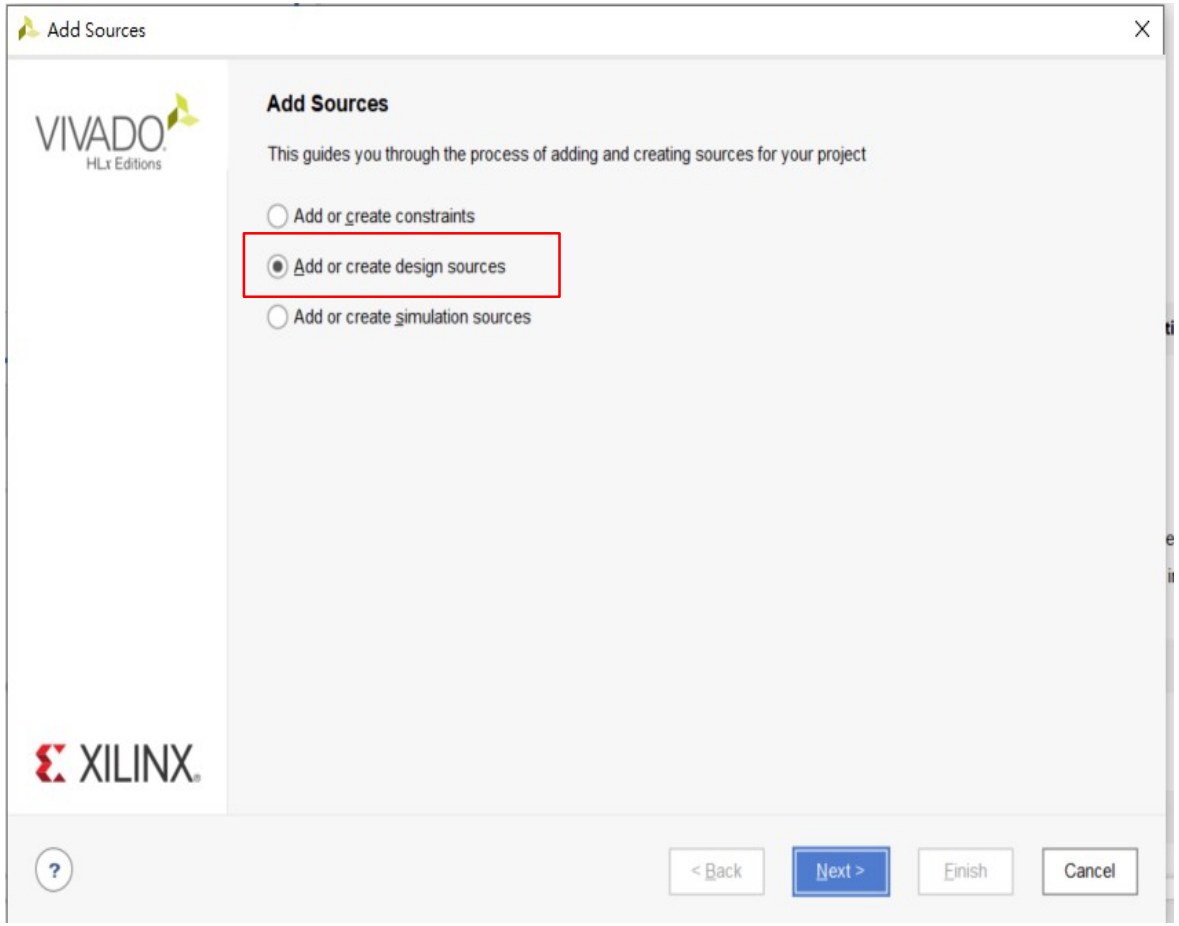
Step4

- Select parts or boards arbitrarily since we don’t need to implement the design on the FPGA.



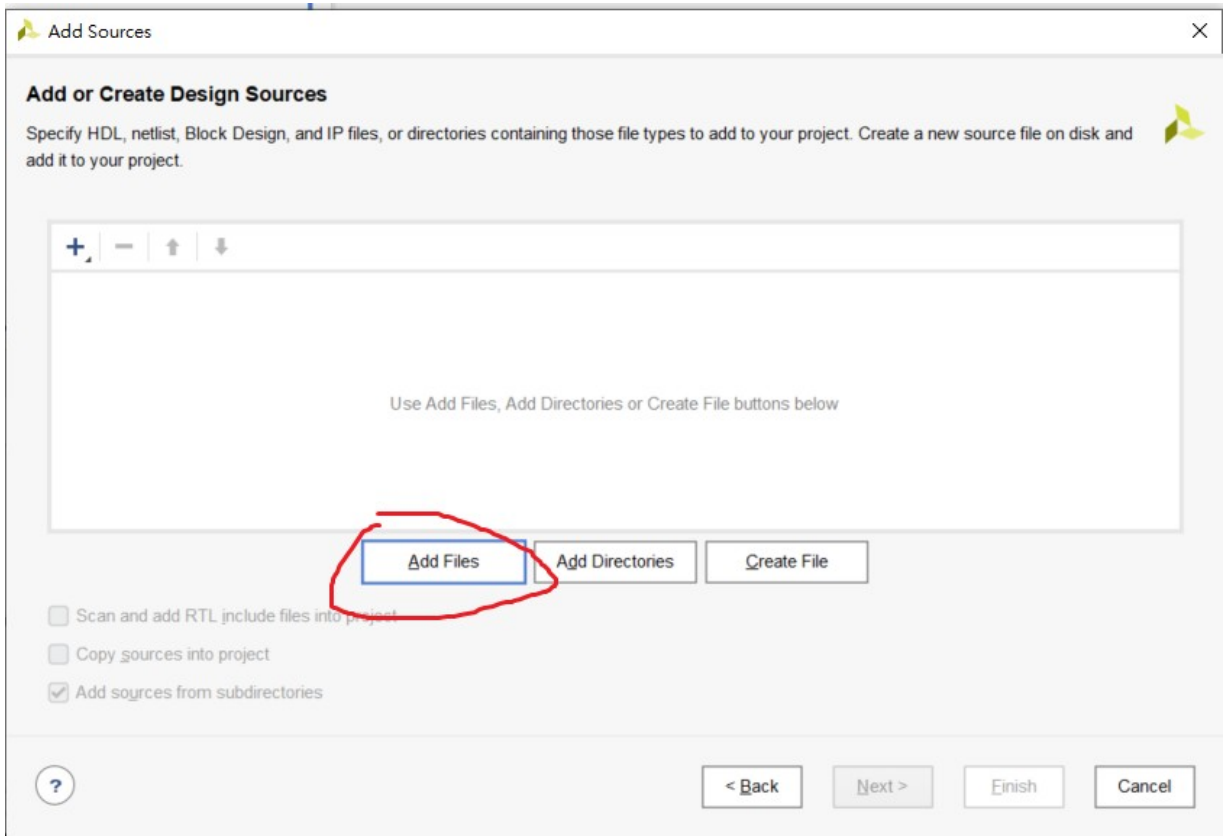
Add Source Files (.v files) Except testbench.v





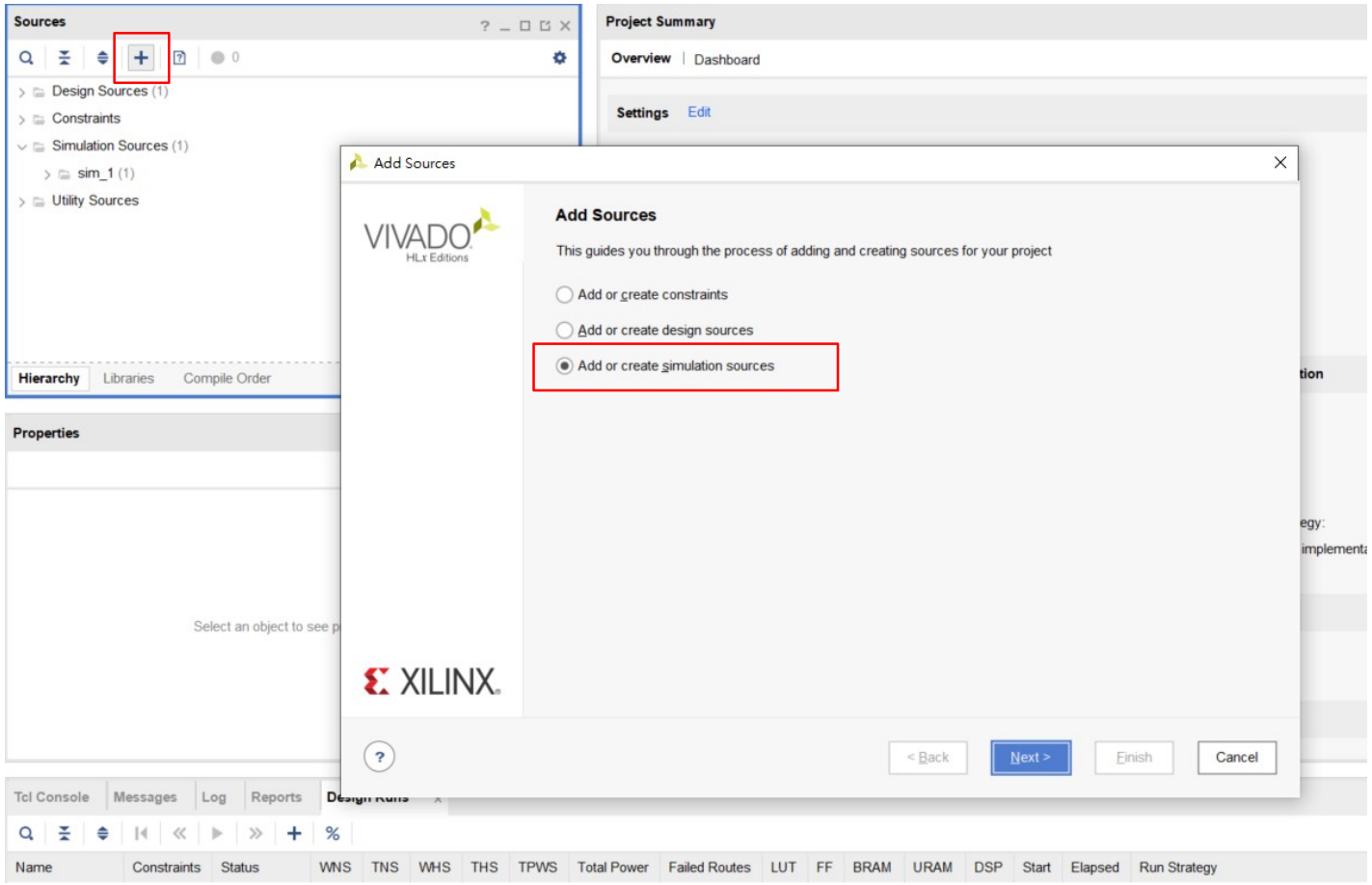
Add Source Files (.v files) Except testbench.v

- Add design sources (not including testbench.v) and finish.



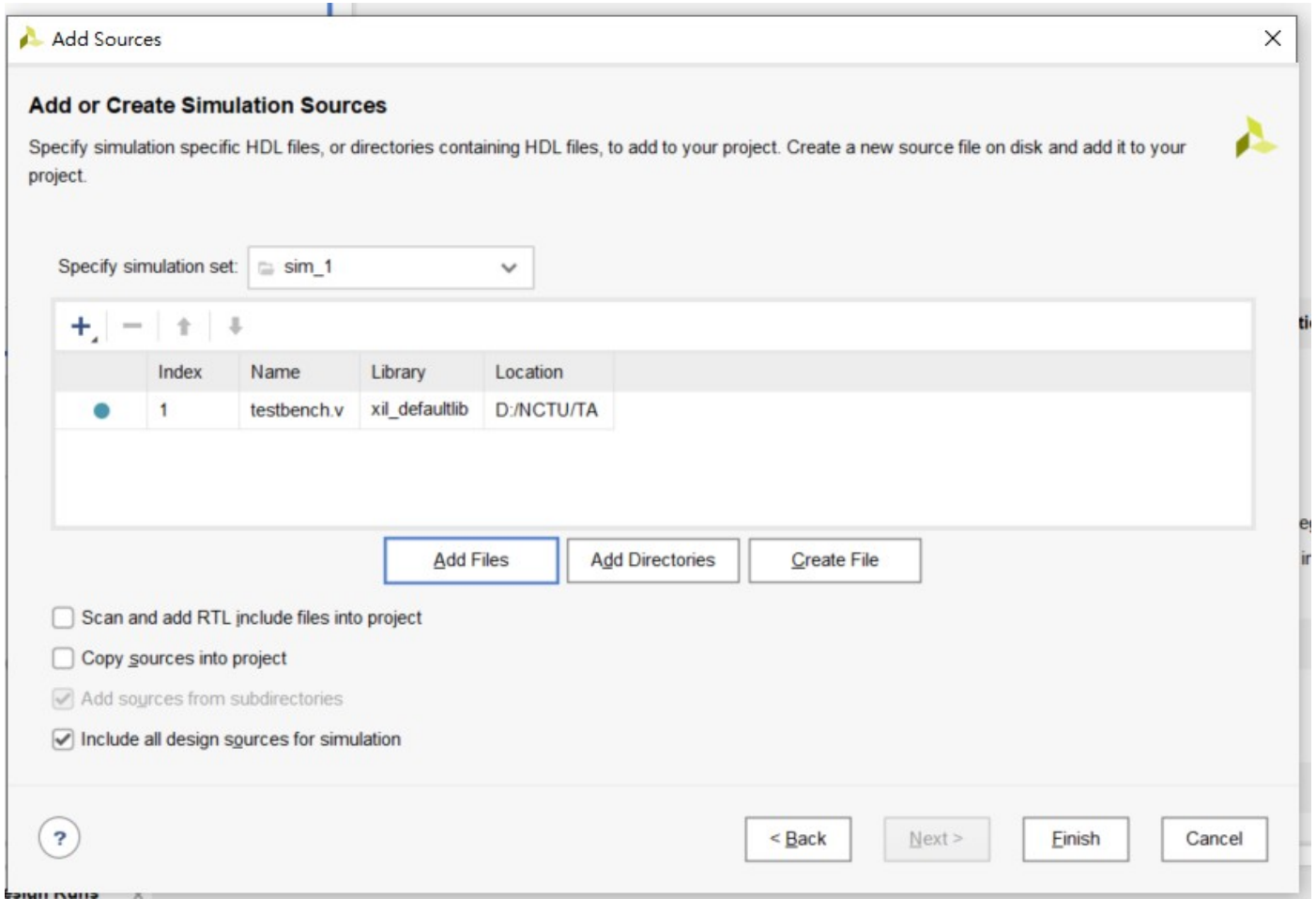
Add Simulation Sources

- Press add sources and select Add or create simulation sources



Add Simulation Sources

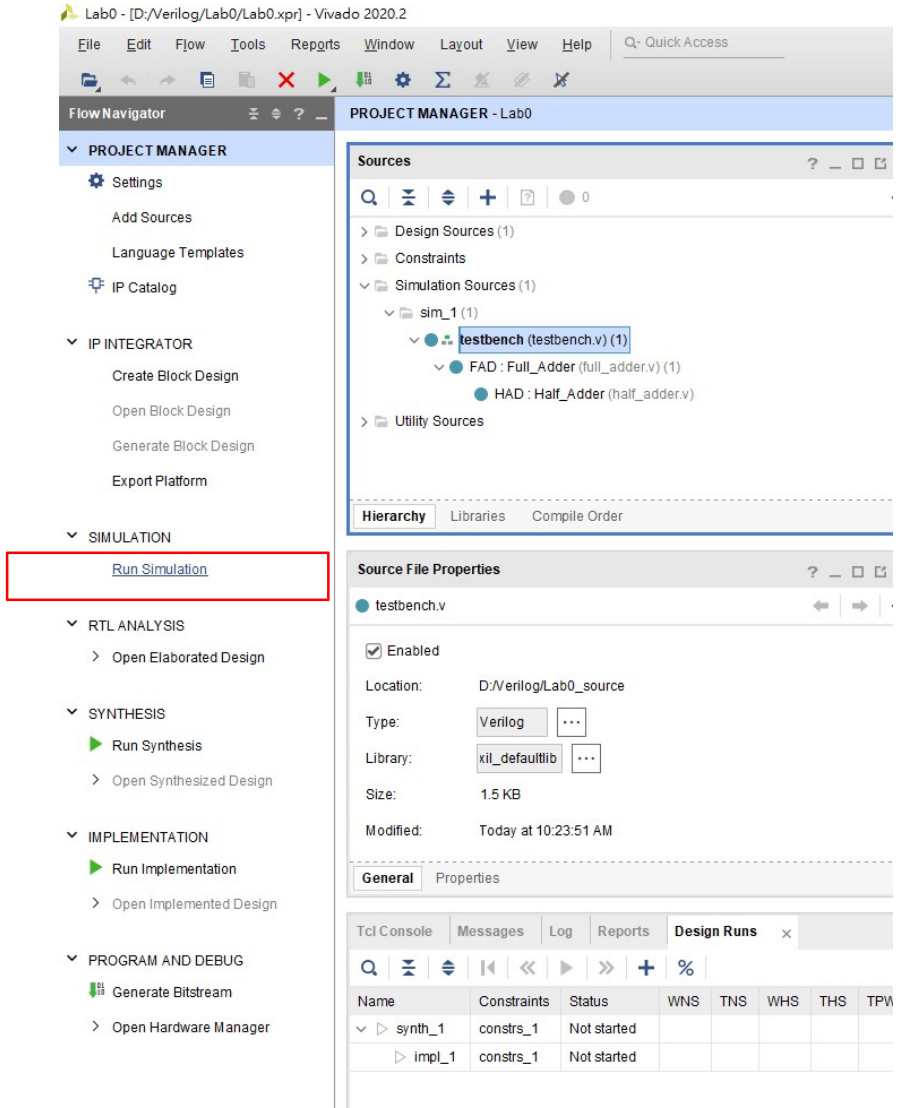
- Add testbench.v and finish

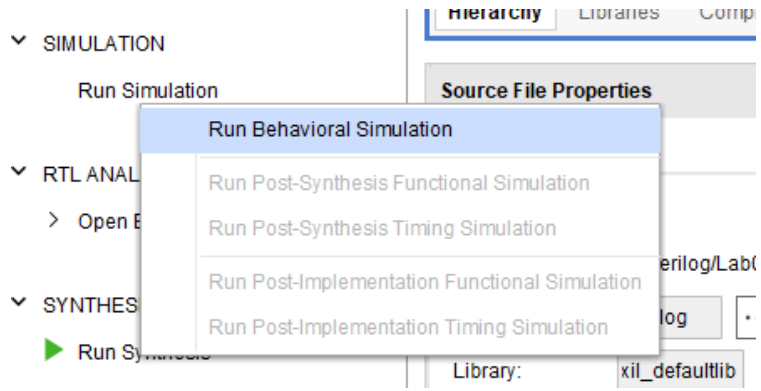


How to Run Simulation

- After adding testbench into project, you can execute the behavioral simulation. It can helps you debug with the signal waveform and check the correctness of your design.

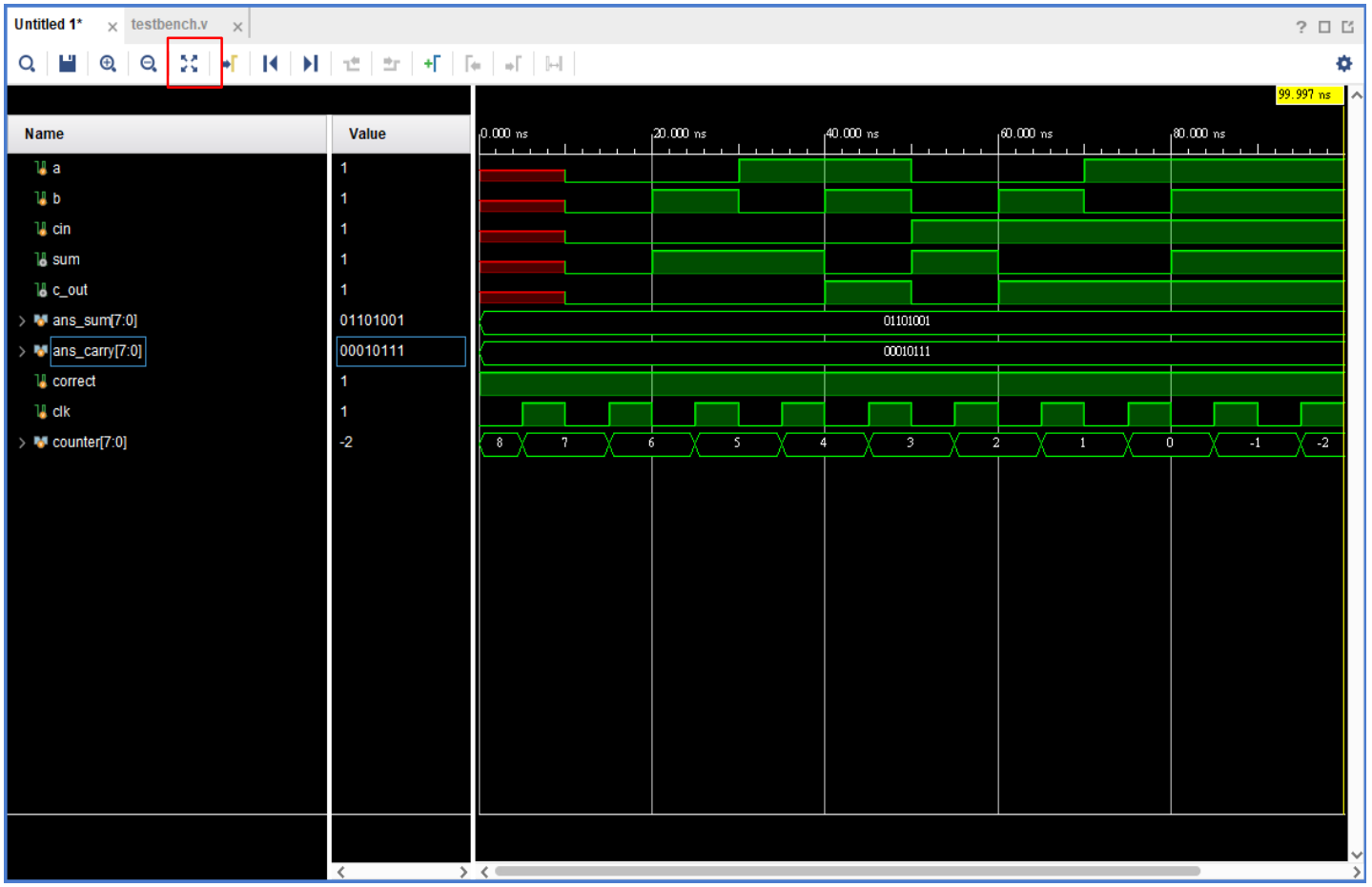
How to Run Simulation

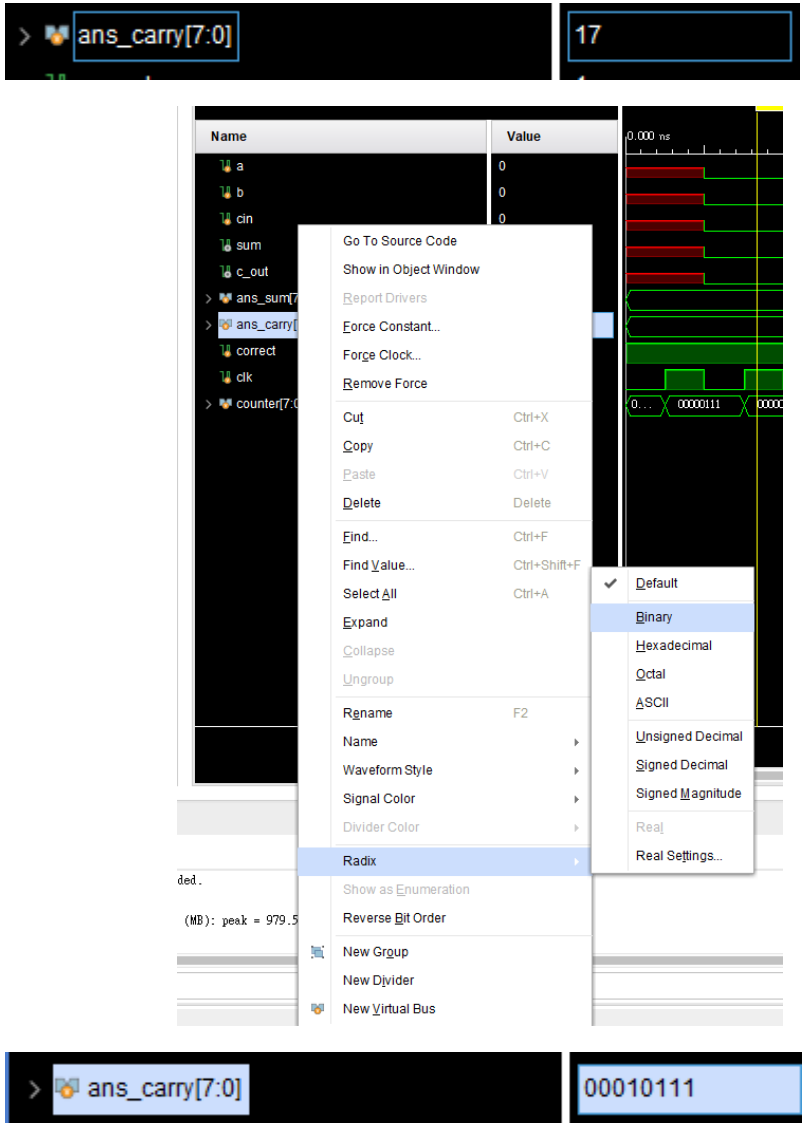




Useful Information

This bottom can make your waveform fit your screen size.



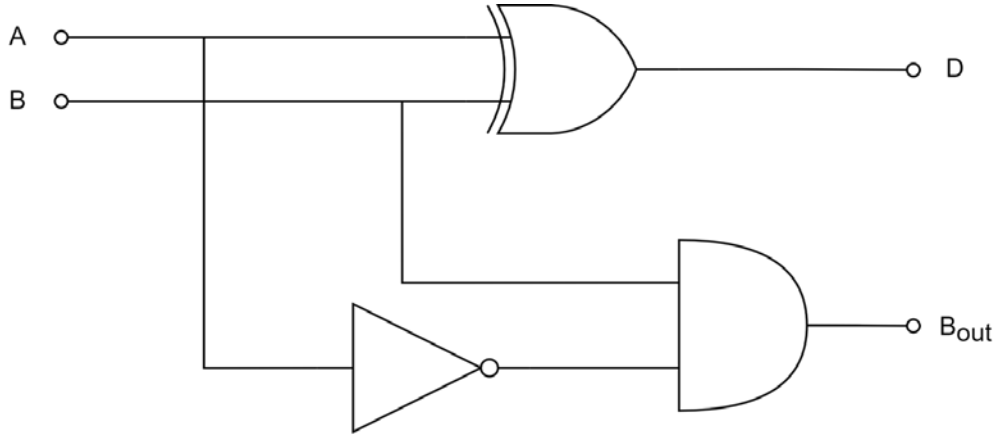


This function can help you change the radix of the signal

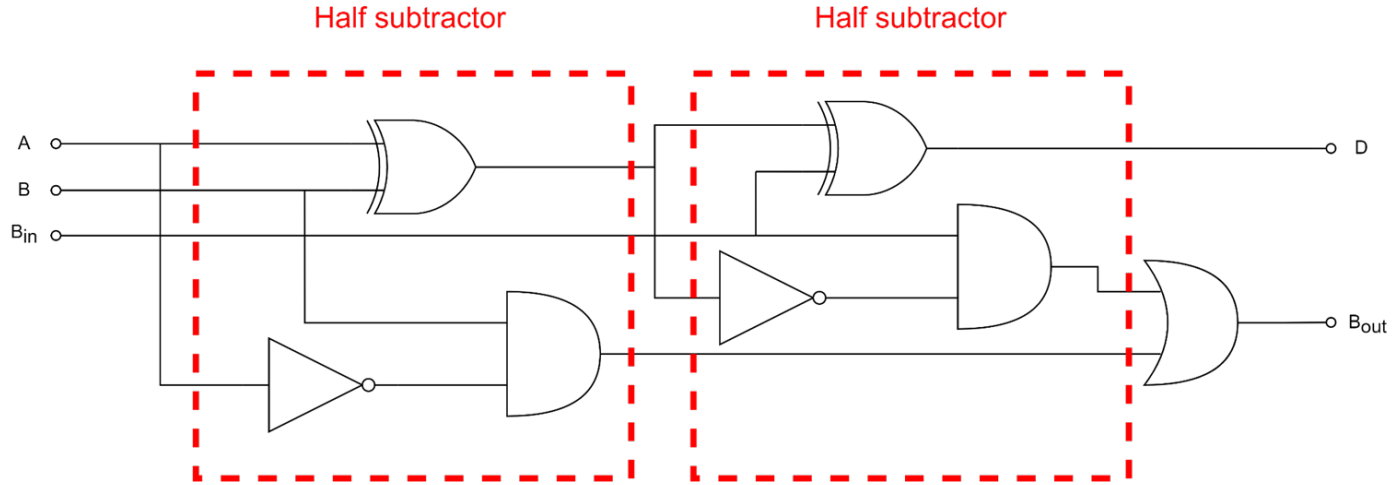
Lab0: Half Subtractor and Full Subtractor

- Implement the half subtractor and full subtractor without using ‘-’ operation.
- We want you to practice how to implement the signal connection with the given circuit. We will give you example design sources and testbench.v.

Half Subtractor and Full Subtractor Circuit



Half Subtractor



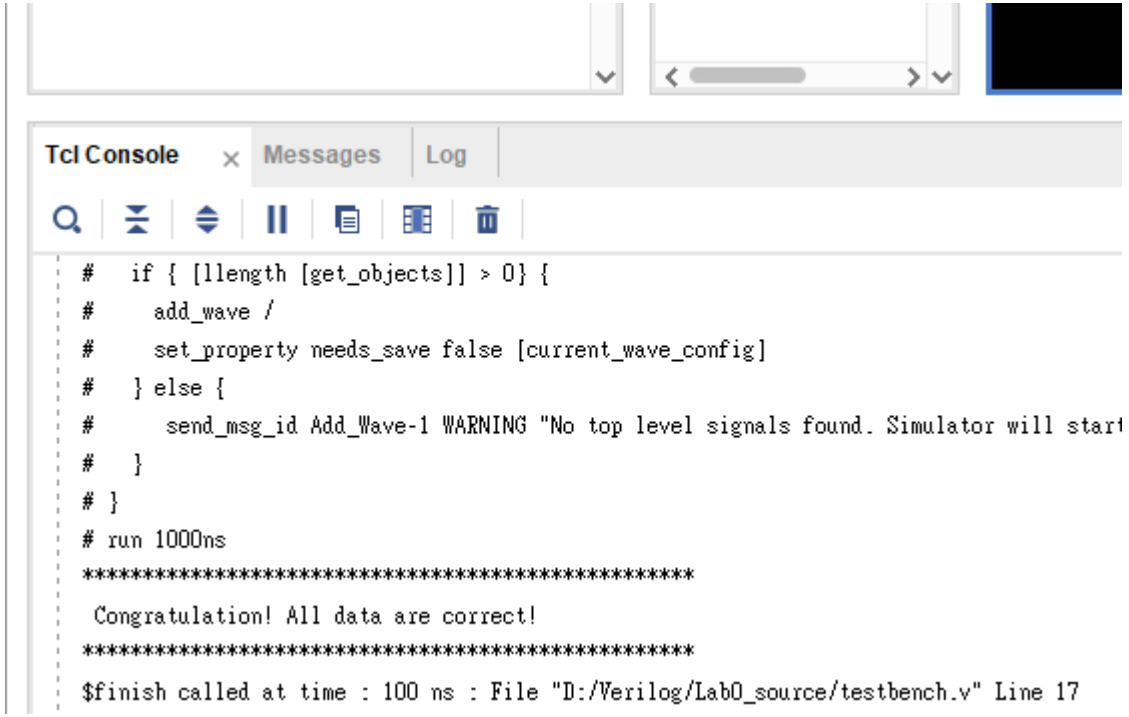
Full Subtractor

Truth Table for Full Subtractor

Input			Output	
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Check Correctness

- We have enumerated all input cases in testbench.v.
- After simulation with our testbench.v, if your design is correct, you will see the message in the console.



Grading policy

- If the simulation result shows “Congratulation! All data are correct!”, you’ll get 100.
- Otherwise, you’ll get 0 point.

Submission

- Due date: 2022/03/02 23:55
- Put all your design sources(*half_substractor.v* and *full_substractor.v* in this lab)into one directory named "your_student_id" and zip the directory named "your_student_id.zip". You only need to submit "your_student_id.zip".
- If your submission doesn't meet the required format, you'll get 10 points punishment.
- 30% score deduction for late submission within one week (before 2022 3/9 23:55). Over one week, you'll get no points.
- If you have any questions, feel free to ask on the Facebook discussion forum. Thank you.