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1.1 Introduction

- In electric circuit we have to provide a path through which charge can flow easily by the movements of electrons.

1.1.1 Conductors

- Materials through which charge flows readily are called conductors.
- A conductor has a very low resistance to the flow of charge.
- Ex. Silver, gold, copper, aluminum and such metals.
- Copper is used mostly for the conductive paths on electric circuit boards and for the fabrication of electric wires.

1.1.2 Insulators

- Materials that do not allow charge to move easily. Electric current cannot be made to flow through it.
- An insulator has very high resistance to the flow of charge.
- Ex: glass, plastic, ceramics and rubber.
- Insulating materials wrapped around the conducting core of the wire.

1.1.3 Semiconductors

- Semiconductors lie in the middle between conductors and insulators
- Semiconductor has moderate resistance to the flow of charge.
- Ex. Elemental semiconductors are Silicon, germanium whereas gallium arsenide is an example of compound semiconductors which are developed.

1.1.4 P-Type Semiconductors

- Silicon that has been doped with a trivalent impurities like aluminum, boron and gallium is called a p-type semiconductor, where the p stands for positive.
- Since holes outnumber free electrons, the holes are referred to as the majority carriers and the free electrons are known as the minority carriers.

1.1.5 N-Type Semiconductors

- Silicon that has been doped with a trivalent impurities like arsenic, antimony and phosphorus is called an n-type semiconductor, where the n stands for negative.
- Since free electrons outnumber the holes in an n-type semiconductor, the free electrons are called as the majority carriers and the holes are called as the minority carriers.

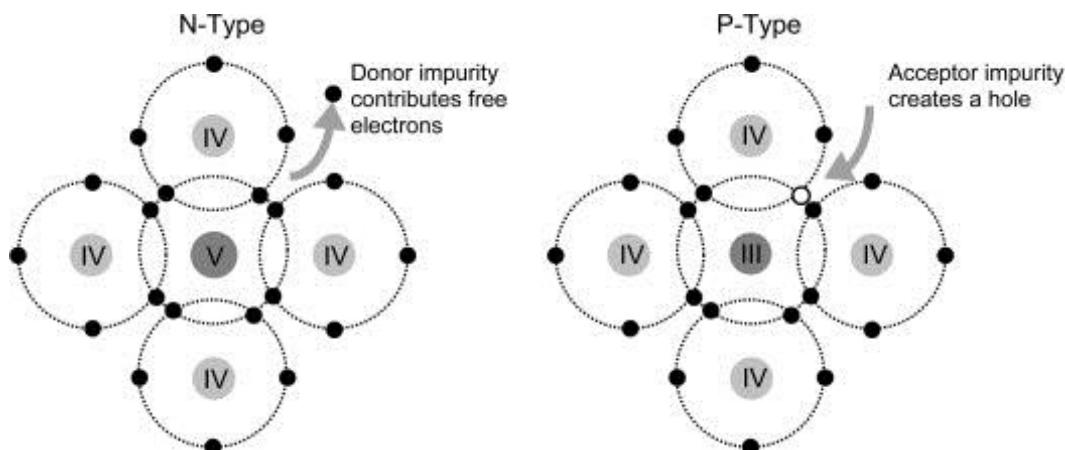


Figure-1 N-Type and P-Type Semiconductor's Atomic Level Arrangements

1.2 The Diode

- By itself, a piece of n-type semiconductor is about as useful as a carbon resistor; the same can be said for a p-type semiconductor.
- But when a manufacturer dopes a crystal so that one-half of it is p-type and the other half is n-type, something new comes into existence.
- The border between p-type and n-type is called the pn junction.
- The pn junction has led to all kinds of inventions, including diodes, transistors, and integrated circuits.
- Understanding the pn junction enables you to understand all kinds of semiconductor devices.

1.2.1 The Unbiased Diode

- As discussed in the preceding section, each trivalent atom in a doped silicon crystal produces one hole.
- For this reason, we can visualize a piece of p-type semiconductor as shown on the left side of Figure-2. Each circled minus sign is the trivalent atom, and each plus sign is the hole in its valence orbit.
- Similarly, we can visualize the pentavalent atoms and free electrons of an n-type semiconductor as shown on the right side of Figure-2. Each circled plus sign represents a pentavalent atom, and each minus sign is the free electron it contributes to the semiconductor.
- Notice that each piece of semiconductor material is electrically neutral because the number of pluses and minuses are equal.

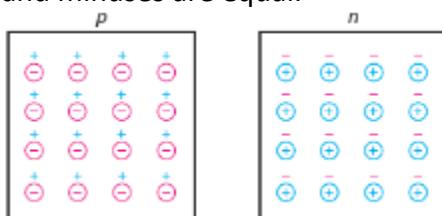


Figure-2 Two Types of Semiconductor

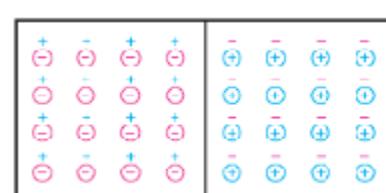


Figure-3 The P-N Junction

- A manufacturer can produce a single crystal with p-type material on one side and n-type on the other side, as shown in Figure-3.

- The junction is the border where the p-type and the n-type regions meet, and junction diode is another name for a pn crystal.
- The word diode is a contraction of two electrodes, where **di** stands for “two.”

1.2.2 The Depletion Layer

- Because of their repulsion for each other, the free electrons on the n side of Figure-3 tend to diffuse (spread) in all directions.
- Some of the free electrons diffuse across the junction. When a free electron enters the p region, it becomes a minority carrier.
- With so many holes around it, this minority carrier has a short lifetime.
- Soon after entering the p region, the free electron recombines with a hole.
- When this happens, the hole disappears and the free electron becomes a valence electron.
- Each time an electron diffuses across a junction, it creates a pair of ions.
- When an electron leaves the n side, it leaves behind a pentavalent atom that is short one negative charge; this pentavalent atom becomes a positive ion.
- After the migrating electron falls into a hole on the p side, it makes a negative ion out of the trivalent atom that captures it. Figure-4 shows these ions on each side of the junction.
- The circled plus signs are the positive ions, and the circled minus signs are the negative ions.
- The ions are fixed in the crystal structure because of covalent bonding, and they cannot move around like free electrons and holes.
- Each pair of positive and negative ions at the junction is called a dipole.
- The creation of a dipole means that one free electron and one hole have been taken out of circulation.
- As the number of dipoles builds up, the region near the junction is emptied of carriers. We call this charge-empty region the depletion layer (see Figure-5).

1.2.3 Barrier Potential

- Each dipole has an electric field between the positive and negative ions. Therefore, if additional free electrons enter the depletion layer, the electric field tries to push these electrons back into the n region.
- The strength of the electric field increases with each crossing electron until equilibrium is reached.
- To a first approximation, this means that the electric field eventually stops the diffusion of electrons across the junction.
- In Figure-4, the electric field between the ions is equivalent to a difference of potential called the barrier potential.
- At 25°C, the barrier potential equals approximately 0.3 V for germanium diodes and 0.7 V for silicon diodes.

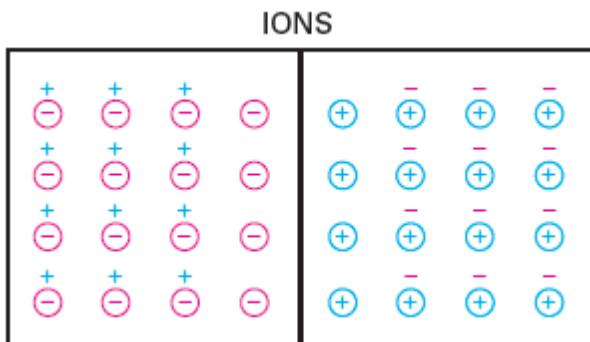


Figure-4 Creation of ions at junction

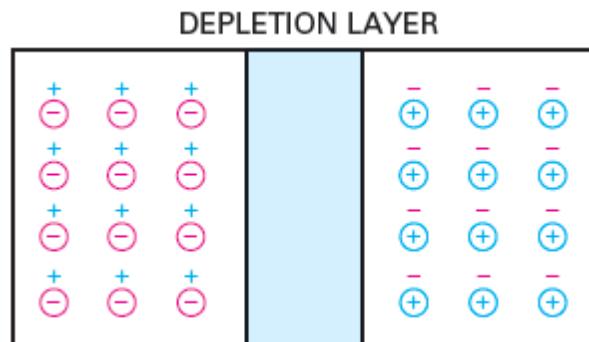


Figure-5 Depletion layer

1.2.4 Forward Bias

- Figure-6 shows a dc source across a diode. The negative source terminal is connected to the n-type material, and the positive terminal is connected to the p-type material. This connection produces what is called forward bias.

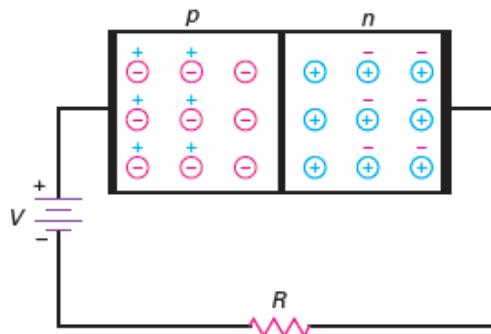


Figure-6 Forward bias

1.2.4.1 Flow of Free Electrons

- In Figure-6, the battery pushes holes and free electrons toward the junction.
- If the battery voltage is less than the barrier potential, the free electrons do not have enough energy to get through the depletion layer.
- When they enter the depletion layer, the ions will push them back into the n region. Because of this, there is no current through the diode.
- When the dc voltage source is greater than the barrier potential, the battery again pushes holes and free electrons toward the junction. This time, the free electrons have enough energy to pass through the depletion layer and recombine with the holes.
- If you visualize all the holes in the p region moving to the right and all the free electrons moving to the left, you will have the basic idea.
- Somewhere in the vicinity of the junction, these opposite charges recombine. Since free electrons continuously enter the right end of the diode and holes are being continuously created at the left end, there is a continuous current through the diode.

1.2.4.2 The Flow of One Electron

- Let us follow a single electron through the entire circuit.

- After the free electron leaves the negative terminal of the battery, it enters the right end of the diode. It travels through the n region until it reaches the junction.
- When the battery voltage is greater than 0.7 V, the free electron has enough energy to get across the depletion layer.
- Soon after the free electron has entered the p region, it recombines with a hole.
- In other words, the free electron becomes a valence electron. As a valence electron, it continues to travel to the left, passing from one hole to the next until it reaches the left end of the diode.
- When it leaves the left end of the diode, a new hole appears and the process begins again. Since there are billions of electrons taking the same journey, we get a continuous current through the diode.
- A series resistor is used to limit the amount of forward current.

1.2.4.3 What to Remember?

- Current flows easily in a forward-biased diode. As long as the applied voltage is greater than the barrier potential, there will be a large continuous current in the circuit.
- In other words, if the source voltage is greater than 0.7 V, a silicon diode allows a continuous current in the forward direction.

1.2.5 Reverse Bias

- Turn the dc source around and you get Figure-7. This time, the negative battery terminal is connected to the p side and the positive battery terminal to the n side.
- This connection produces what is called reverse bias.

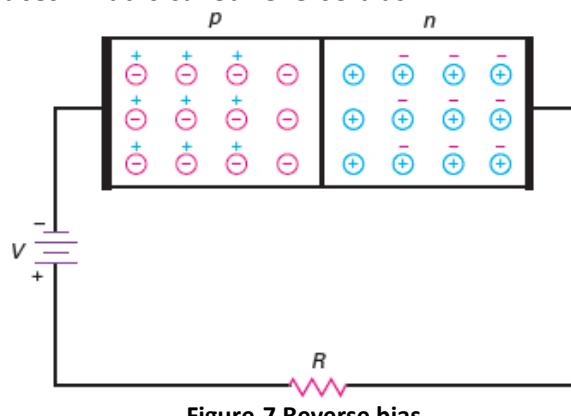


Figure-7 Reverse bias

1.2.5.1 Depletion Layer Widens

- The negative battery terminal attracts the holes, and the positive battery terminal attracts the free electrons. Because of this, holes and free electrons flow away from the junction. Therefore, the depletion layer gets wider.
- How wide does the depletion layer get in Figure-8?
- When the holes and electrons move away from the junction, the newly created ions increase the difference of potential across the depletion layer. The wider the depletion layer, the greater the difference of potential.

- The depletion layer stops growing when its difference of potential equals the applied reverse voltage. When this happens, electrons and holes stop moving away from the junction.

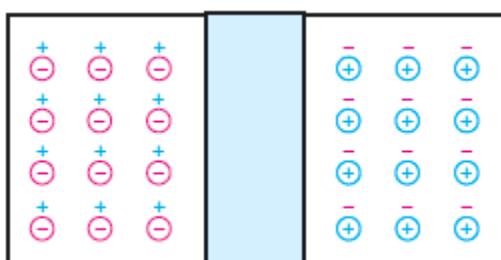


Figure-8 Depletion layer

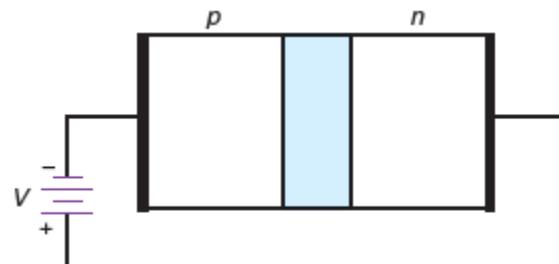


Figure-9 increasing reverse bias widens depletion layer

- Sometimes the depletion layer is shown as a shaded region like that of Figure-9. The width of this shaded region is proportional to the reverse voltage. As the reverse voltage increases, the depletion layer gets wider.

1.2.5.2 Minority-Carrier Current

- Is there any current after the depletion layer stabilizes? Yes. A small current exists with reverse bias. Recall that thermal energy continuously creates pairs of free electrons and holes. This means that a few minority carriers exist on both sides of the junction.
- Most of these recombine with the majority carriers. But those inside the depletion layer may exist long enough to get across the junction.
- When this happens, a small current flows in the external circuit.
- Figure 10 illustrates the idea. Assume that thermal energy has created a free electron and hole near the junction.
- The depletion layer pushes the free electron to the right, forcing one electron to leave the right end of the crystal. The hole in the depletion layer is pushed to the left. This extra hole on the p side lets one electron enter the left end of the crystal and fall into a hole.
- Since thermal energy is continuously producing electron-hole pairs inside the depletion layer, a small continuous current flows in the external circuit.
- The reverse current caused by the thermally produced minority carriers is called the saturation current. In equations, the saturation current is symbolized by I_s . The name saturation means that we cannot get more minority-carrier current than is produced by the thermal energy.
- In other words, increasing the reverse voltage will not increase the number of thermally created minority carriers.

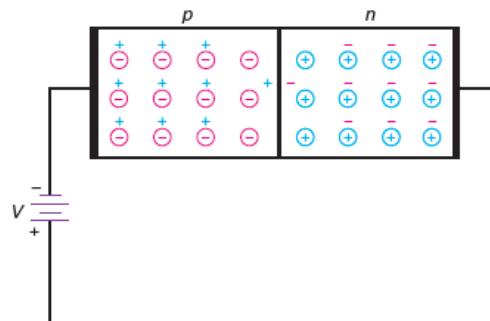


Figure-10 Thermal production of free electron and hole in depletion layer produces reverse minority-saturation current

1.2.5.3 Surface-Leakage Current

- Besides the thermally produced minority-carrier current, does any other current exist in a reverse-biased diode? Yes. A small current flows on the surface of the crystal. Known as the surface-leakage current, it is caused by surface impurities and imperfections in the crystal structure.

1.2.5.4 What to Remember

- The reverse current in a diode consists of a minority-carrier current and a surface-leakage current.
- In most applications, the reverse current in a silicon diode is so small that you don't even notice it.
- The main idea to remember is this: Current is approximately zero in a reverse-biased silicon diode.

1.3 V-I Characteristics of Diode

- An ordinary resistor is a linear device because the graph of its current versus voltage is a straight line.
- A diode is different. It is a nonlinear device because the graph of its current versus voltage is not a straight line.
- The reason is the barrier potential. When the diode voltage is less than the barrier potential, the diode current is small. When the diode voltage exceeds the barrier potential, the diode current increases rapidly.

1.3.1 The Schematic Symbol and Case Styles

- Figure-11 shows the pn structure and schematic symbol of a diode.
- The p side is called the anode, and the n side the cathode.
- The diode symbol looks like an arrow that points from the p side to the n side, from the anode to the cathode.
- Figure-12 shows some of the many typical diode case styles. Many, but not all, diodes have the cathode lead (K) identified by a colored band.

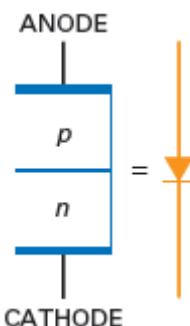


Figure-11 Schematic symbol



Figure-12 Diode case styles

1.3.2 Basic Diode Circuit

- Figure 13 shows a diode circuit. In this circuit, the diode is forward biased.
- How do we know? Because the positive battery terminal drives the p side through a resistor, and the negative battery terminal is connected to the n side. With this connection, the circuit is trying to push holes and free electrons toward the junction.

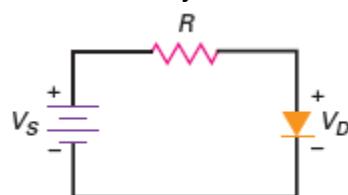


Figure-13 Forward Bias Circuit

1.3.3 The Forward Region

- Figure 13 is a circuit that you can set up in the laboratory. After you connect this circuit, you can measure the diode current and voltage.
- You can also reverse the polarity of the dc source and measure diode current and voltage for reverse bias.
- If you plot the diode current versus the diode voltage, you will get a graph that looks like Figure 14.
- For instance, when the diode is forward biased, there is no significant current until the diode voltage is greater than the barrier potential.
- On the other hand, when the diode is reverse biased, there is almost no reverse current until the diode voltage reaches the breakdown voltage. Then, avalanche produces a large reverse current, destroying the diode.

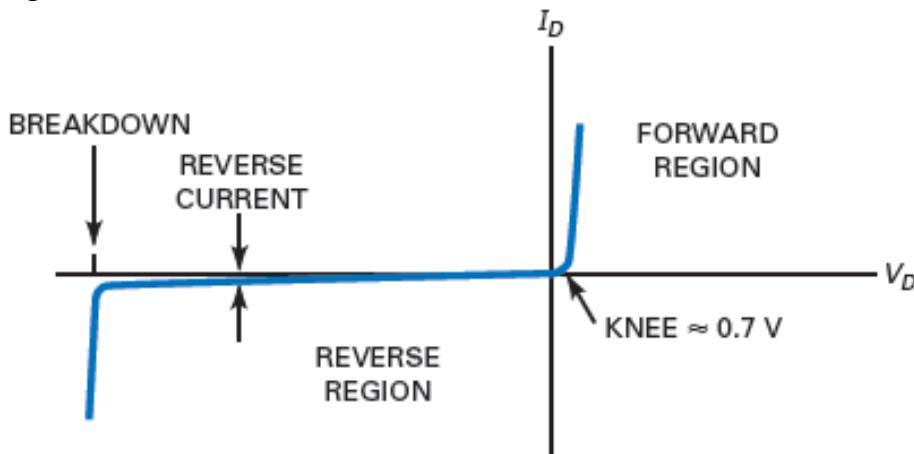


Figure-14 Diode Curve

1.3.4 Knee Voltage

- In the forward region, the voltage at which the current starts to increase rapidly is called the knee voltage of the diode. The knee voltage equals the barrier potential.
- Analysis of diode circuits usually comes down to determining whether the diode voltage is more or less than the knee voltage. If it's more, the diode conducts easily. If it's less, the diode conducts poorly.
- We define the knee voltage of a silicon diode as: $V_K \approx 0.7 V$ ----- (1)
- Even though germanium diodes are rarely used in new designs, you may still encounter germanium diodes in special circuits or in older equipment.
- For this reason, remember that the knee voltage of a germanium diode is approximately 0.3 V. This lower knee voltage is an advantage and accounts for the use of a germanium diode in certain applications.

1.3.5 Bulk Resistance

- Above the knee voltage, the diode current increases rapidly. This means that small increases in the diode voltage cause large increases in diode current.
- After the barrier potential is overcome, all that impedes the current is the ohmic resistance of the p and n regions.
- In other words, if the p and n regions were two separate pieces of semiconductor, each would have a resistance that you could measure with an ohmmeter, the same as an ordinary resistor.
- The sum of the ohmic resistances is called the bulk resistance of the diode.

It is defined as: $R_B = R_P + R_N$ ----- (2)

- The bulk resistance depends on the size of the p and n regions and how heavily doped they are. Often, the bulk resistance is less than 1Ω .

1.3.6 Maximum DC Forward Current

- If the current in a diode is too large, the excessive heat can destroy the diode.
- For this reason, a manufacturer's data sheet specifies the maximum current a diode can safely handle without shortening its life or degrading its characteristics.
- The maximum forward current is one of the maximum ratings given on a data sheet. This current may be listed as I_{max} , $I_{F(max)}$, I_O , etc., depending on the manufacturer. For instance, a **1N456** has a maximum forward current rating of **135 mA**. This means that it can safely handle a continuous forward current of **135 mA**.

1.3.7 Power Dissipation

- You can calculate the power dissipation of a diode the same way as you do for a resistor. It equals the product of diode voltage and current.

As a formula: $P_D = V_D I_D$ ----- (3)

- The power rating is the maximum power the diode can safely dissipate without shortening its life or degrading its properties. In symbols, the definition is: $P_{max} = V_{max} I_{max}$ ----- (4)
- Where V_{max} is the voltage corresponding to I_{max} . For instance, if a diode has a maximum voltage and current of 1 V and 2 A, its power rating is 2 W.

Example 1

A diode has a power rating of 5 W. If the diode voltage is 1.2 V and the diode current is 1.75 A, what is the power dissipation? Will the diode be destroyed?

SOLUTION

$$P_D = (1.2 \text{ V}) (1.75 \text{ A}) = 2.1 \text{ W}$$

This is less than the power rating, so the diode will not be destroyed.

PRACTICE PROBLEM 1

Referring to Example 1, what is the diode's power dissipation if the diode voltage is 1.1 V and the diode current is 2 A?

1.4 The Ideal Diode

- Figure 15 shows a detailed graph of the forward region of a diode. Here you see the diode current I_D versus diode voltage V_D . Notice how the current is approximately zero until the diode voltage approaches the barrier potential.
- Somewhere in the vicinity of **0.6** to **0.7 V**, the diode current increases. When the diode voltage is greater than **0.8 V**, the diode current is significant and the graph is almost linear.
- Depending on how a diode is doped and its physical size, it may differ from other diodes in its maximum forward current, power rating, and other characteristics.
- If we need an exact solution, we have to use the graph of the particular diode.

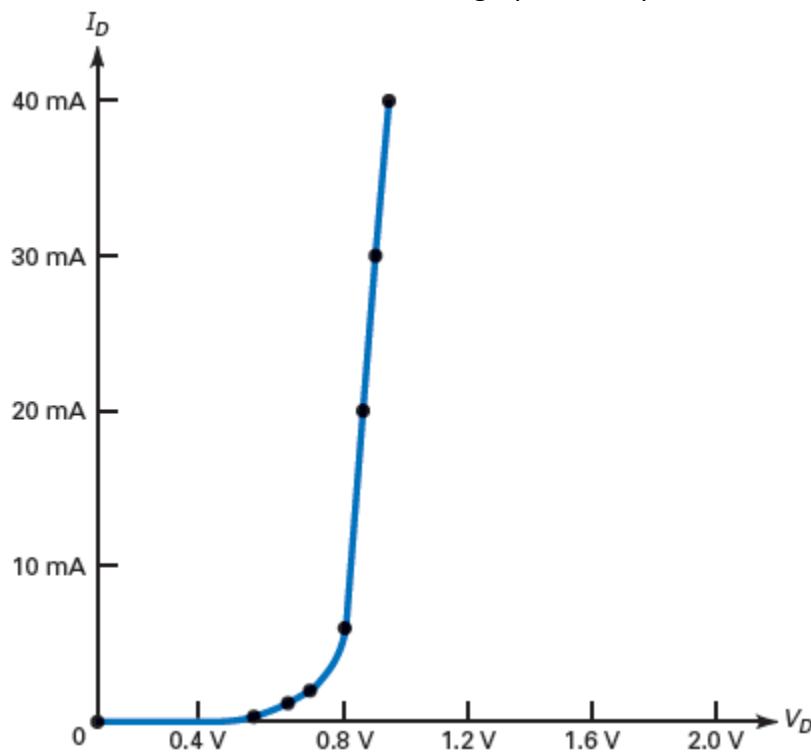


Figure-15 Graph of Forward Current

- Although the exact current and voltage points will differ from one diode to the next, the graph of any diode is similar to Figure 15.
- All silicon diodes have a knee voltage of approximately **0.7 V**.

- Most of the time, we do not need an exact solution. This is why we can and should use **approximations** for a diode. We will begin with the simplest approximation, called an **ideal diode**. In the most basic terms, what does a diode do? It conducts well in the forward direction and poorly in the reverse direction.
- Ideally, a diode acts like a perfect conductor (zero resistance) when forward biased and like a perfect insulator (infinite resistance) when reverse biased.
- Figure 16 shows the current-voltage graph of an ideal diode. It echoes what we just said: zero resistance when forward biased and infinite resistance when reverse biased.
- It is impossible to build such a device, but this is what manufacturers would produce if they could.
- Is there any device that acts like an ideal diode? Yes. An ordinary switch has zero resistance when closed and infinite resistance when open.
- Therefore, an ideal diode acts like a switch that closes when forward biased and opens when reverse biased. Figure 17 summarizes the switch idea.

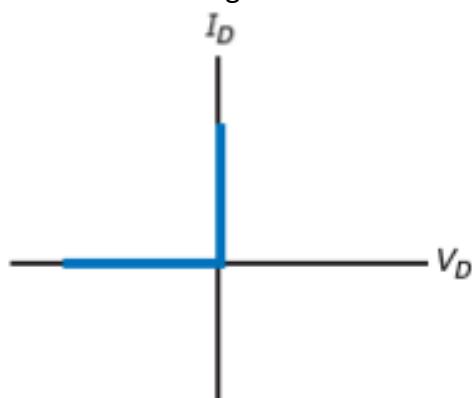


Figure-16 Ideal diode curve

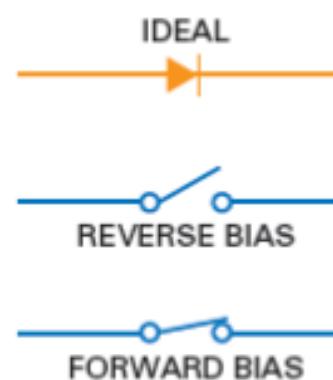


Figure-17 ideal diode acts like a switch

Example 2

Use the ideal diode to calculate the load voltage and load current in Figure 18.

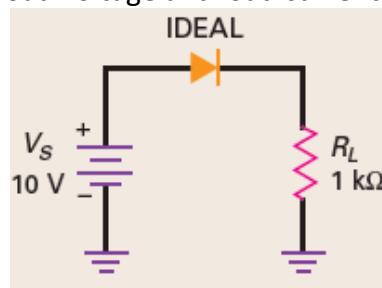


Figure-18

SOLUTION

Since the diode is forward biased, it is equivalent to a closed switch. Visualize the diode as a closed switch. Then, you can see that all of the source voltage appears across the load resistor:

$$V_L = 10 \text{ V}$$

With Ohm's law, the load current is:

$$I_L = 10V/1K\Omega = 10 \text{ mA}$$

PRACTICE PROBLEM 2

In above example, find the ideal load current if the source voltage is 5 V.

Example 3

Calculate the load voltage and load current in Figure-19 using an ideal diode.

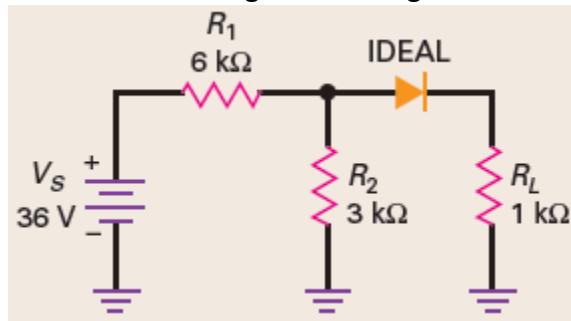


Figure-19

SOLUTION

One way to solve this problem is to Thevenize the circuit to the left of the diode. Looking from the diode back toward the source, we see a voltage divider with $6\text{ k}\Omega$ and $3\text{ k}\Omega$. The Thevenin voltage is 12 V, and the Thevenin resistance is $2\text{ k}\Omega$. Figure-20 shows the Thevenin circuit driving the diode.

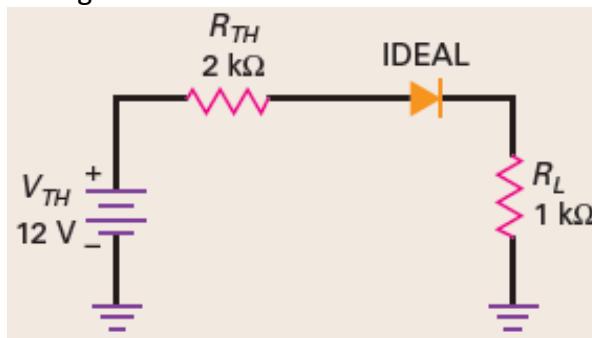


Figure-20

Now that we have a series circuit, we can see that the diode is forward biased. Visualize the diode as a closed switch. Then, the remaining calculations are:

$$I_L = 12V/3k\Omega = 4\text{ mA}$$

$$V_L = (4\text{ mA})(1\text{ k}\Omega) = 4\text{ V}$$

You don't have to use Thevenin's theorem. You can analyze Figure-19 by visualizing the diode as a closed switch. Then, you have $3\text{ k}\Omega$ in parallel with $1\text{ k}\Omega$, equivalent to $750\text{ }\Omega$. Using Ohm's law, you can calculate a voltage drop of 32 V across the $6\text{ k}\Omega$. The rest of the analysis produces the same load voltage and load current.

PRACTICE PROBLEM 3

Using Figure-19, change the 36 V source to 18 V and solve for the load voltage and load current using an ideal diode.

1.5 The Second Approximation

- The ideal approximation is all right in most troubleshooting situations. But we are not always troubleshooting. Sometimes, we want a more accurate value for load current and load voltage. This is where the second approximation comes in.

- Figure-21 shows the graph of current versus voltage for the second approximation. The graph says that no current exists until 0.7 V appears across the diode. At this point, the diode turns on. Thereafter, only 0.7 V can appear across the diode, no matter what the current.
- Figure-22 shows the equivalent circuit for the second approximation of a silicon diode. We think of the diode as a switch in series with a barrier potential of 0.7 V. If the Thevenin voltage facing the diode is greater than 0.7 V, the switch will close. When conducting, then the diode voltage is 0.7 V for any forward current.
- On the other hand, if the Thevenin voltage is less than 0.7 V, the switch will open. In this case, there is no current through the diode.

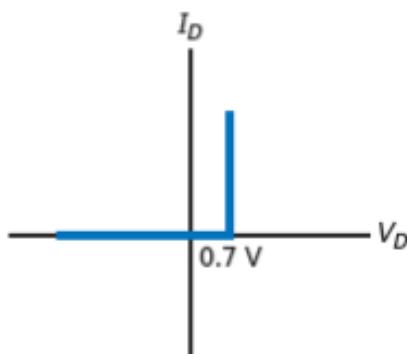


Figure- 21 Diode curve for second approximation

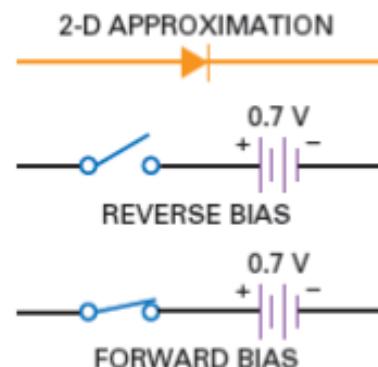


Figure-22 Equivalent circuit for second approximation

Example 4

Use the second approximation to calculate the load voltage, load current, and diode power in Figure-23.

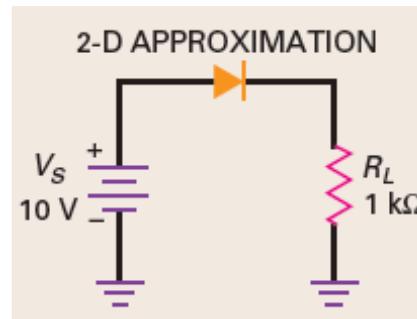


Figure-23

SOLUTION

Since the diode is forward biased, it is equivalent to a battery of 0.7 V. This means that the load voltage equals the source voltage minus the diode drop:

$$V_L = 10 \text{ V} - 0.7 \text{ V} = 9.3 \text{ V}$$

With Ohm's law, the load current is:

$$I_L = 9.3 \text{ V} / 1 \text{ k}\Omega = 9.3 \text{ mA}$$

The diode power is

$$PD = (0.7 \text{ V}) (9.3 \text{ mA}) = 6.51 \text{ mW}$$

PRACTICE PROBLEM 4

Using Figure-23, change the source voltage to 5 V and calculate the new load voltage, current, and diode power.

1.6 The Third Approximation

- In the third approximation of a diode, we include the bulk resistance R_B . Figure-24 shows the effect that R_B has on the diode curve.
- After the silicon diode turns on, the voltage increases linearly with an increase in current. The greater the current, the larger the diode voltage because of the voltage drop across the bulk resistance.

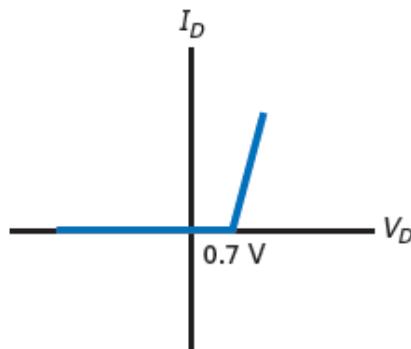


Figure-24 Diode curve for third approximation

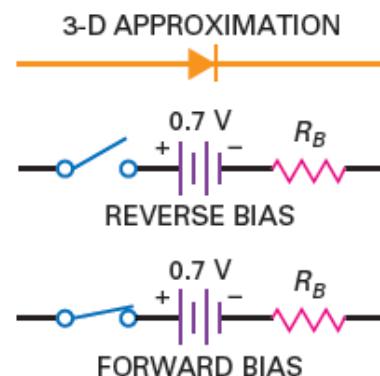


Figure-25 Equivalent circuit for third approximation

- The equivalent circuit for the third approximation is a switch in series with a barrier potential of 0.7 V and a resistance of R_B (see Figure-25). When the diode voltage is larger than 0.7 V, the diode conducts. During conduction, the total voltage across the diode is:

$$V_D = 0.7 \text{ V} + I_D R_B \quad \dots \dots \dots (5)$$

- Often, the bulk resistance is less than 1Ω , and we can safely ignore it in our calculations. A useful guideline for ignoring bulk resistance is this definition:

$$\text{Ignore bulk: } R_B < 0.01 R_{TH} \quad \dots \dots \dots (6)$$

- This says to ignore the bulk resistance when it is less than 1/100 of the Thevenin resistance facing the diode. When this condition is satisfied, the error is less than 1 percent. The third approximation is rarely used by technicians because circuit designers usually satisfy Eq. (6).

Example 5

The 1N4001 of Figure-26 has a bulk resistance of 0.23Ω . What is the load voltage, load current, and diode power?

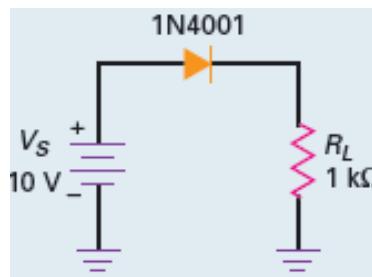


Figure-26

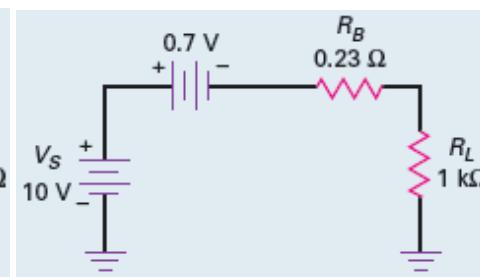


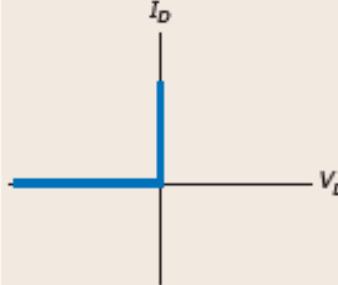
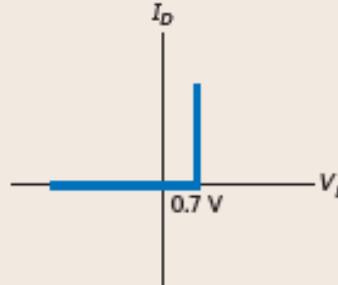
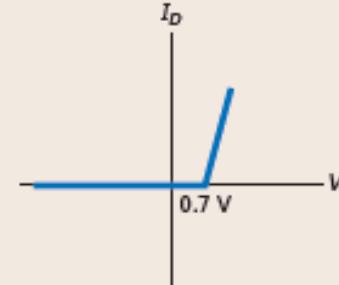
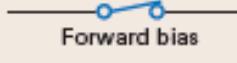
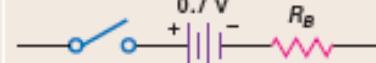
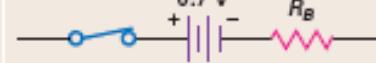
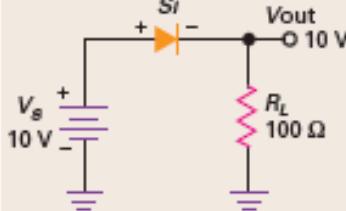
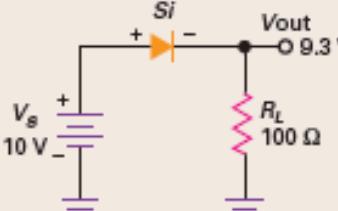
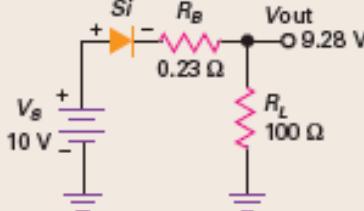
Figure-27

SOLUTION

Replacing the diode with its third approximation, we get Figure-27. The bulk resistance is **small enough to ignore because it is less than 1/100 of the load resistance**. In this case, we can use the second

approximation to solve the problem then we found a load voltage, load current, and diode power of 9.3 V, 9.3 mA, and 6.51 mW.

Summary of Diode Approximations

	First or ideal	Second or practical	Third
When used	Troubleshooting or quick analysis	Analysis at technician level	High-level or engineering-level analysis
Diode curve			
Equivalent circuit	 Reverse bias  Forward bias	 Reverse bias  Forward bias	 Reverse bias  Forward bias
Circuit example			

1.7 Testing of Diode with Multimeter (Troubleshooting)

- You can quickly check the condition of a diode with an ohmmeter on a medium to high resistance range. Measure the dc resistance of the diode in either direction, and then reverse the leads and measure the dc resistance again.
- The forward current will depend on which ohmmeter range is used, which means that you get different readings on different ranges.
- The main thing to look for, however, is a high ratio of reverse to forward resistance. For typical silicon diodes used in electronics work, the ratio should be higher than **1000:1**. Remember to use a high enough resistance range to avoid the possibility of diode damage.
- Normally, the $R \times 100$ or $R \times 1K$ ranges will provide proper safe measurements.

- Using an ohmmeter to check diodes is an example of go/no-go testing. You're really not interested in the exact dc resistance of the diode; all you want to know is whether the diode has a low resistance in the forward direction and a high resistance in the reverse direction.
- Diode troubles are indicated for any of the following: extremely low resistance in both directions (diode shorted); high resistance in both directions (diode open); somewhat low resistance in the reverse direction (called a leaky diode).
- When set to the ohms or resistance function, most digital multimeters (DMMs) do not have the required voltage and current output capability to properly test pn-junction diodes. Most DMMs do, however, have a special diode test range.
- When the meter is set to this range, it supplies a constant current of approximately 1 mA to whatever device is connected to its leads. When forward biased, the DMM will display the pn junction's forward voltage V_F shown in Figure-28. This forward voltage will generally be between **0.5 V** and **0.7 V** for normal silicon pn-junction diodes.
- When the diode is reverse biased by the test leads, the meter will give an over-range indication such as "**OL**" or "**1**" on the display as shown in Figure-29. A **shorted diode** would display a voltage of less than **0.5 V** in both directions.
- An open diode would be indicated by an **over-range** display in both directions. A leaky diode would display a voltage less than **2.0 V** in both directions.

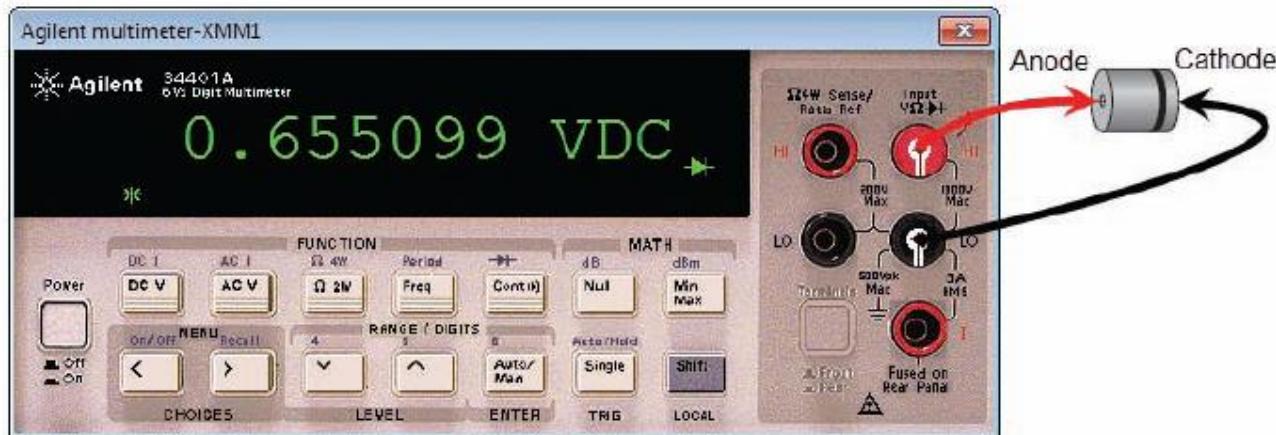


Figure-28

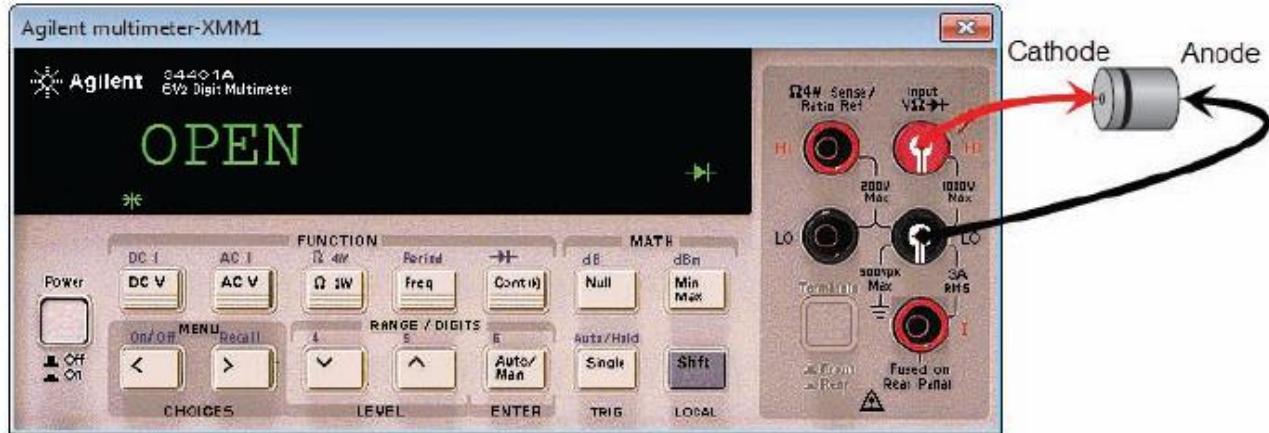


Figure-29

1.8 Surface-Mount Diodes

- Surface-mount (**SM**) diodes can be found anywhere there is a need for diode applications. **SM** diodes are small, efficient, and relatively easy to test, remove, and replace on the circuit board.
- Although there are a number of **SM** package styles, two basic styles dominate the industry: **SM** (surface mount) and **SOT** (small outline transistor).
- The **SM** package has two **L-bend** leads and a colored band on one end of the body to indicate the cathode lead. Figure-30 shows a typical set of dimensions.

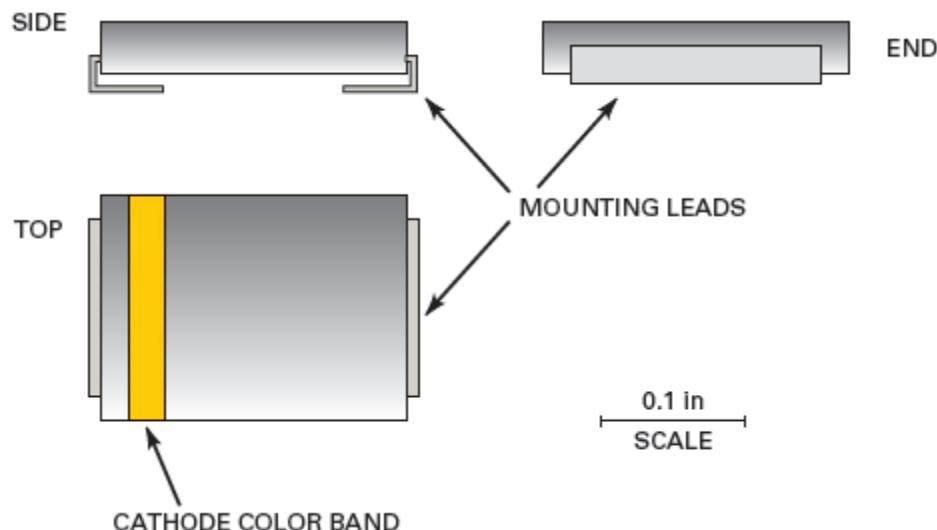


Figure-30 The two-terminal SM-style package used for SM diodes

- The length and width of the **SM** package are related to the current rating of the device. The larger the surface area, the higher the current rating. So an **SM** diode rated at **1 A** might have a surface area given by **0.181** by **0.115 in**. The **3 A** version, on the other hand, might measure **0.260** by **0.236 in**. The thickness tends to remain at about **0.103 in** for all current ratings.
- Increasing the surface area of an **SM**-style diode increases its ability to dissipate heat. Also, the corresponding increase in the width of the mounting terminals increases the thermal conductance to a virtual heat sink made up of the solder joints, mounting lands, and the circuit board itself.
- **SOT-23** packages have three gull-wing terminals (see Figure-31).

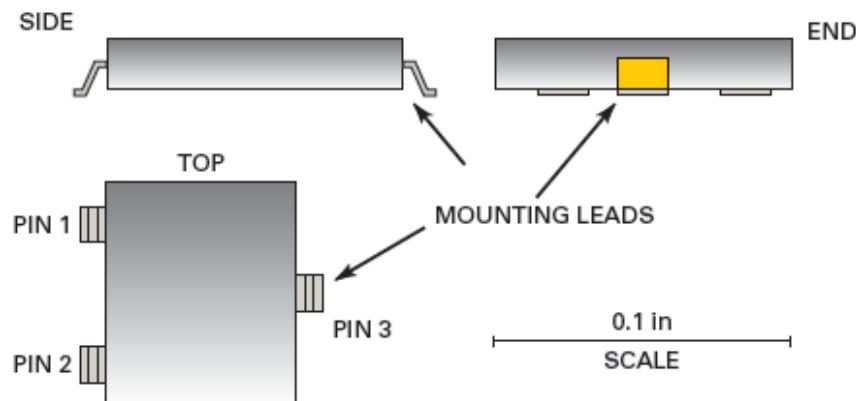


Figure-31 The SOT-23 is a three-terminal transistor package commonly used for SM diodes

- The terminals are numbered counter-clockwise from the top, pin 3 being alone on one side. However, there are no standard markings indicating which two terminals are used for the cathode and the anode.
- To determine the internal connections of the diode, you can look for clues printed on the circuit board, check the schematic diagram, or consult the diode manufacturer's data book.
- Some **SOT-style** packages include two diodes, which have a common-anode or common-cathode connection at one of the terminals.
- Diodes in **SOT-23** packages are small, no dimension being greater than **0.1 in**. Their small size makes it difficult to dissipate larger amounts of heat, so the diodes are generally rated at less than **1 A**.
- The small size also makes it impractical to label them with identification codes. As with many of the tiny **SM** devices, you have to determine the pin configuration from other clues on the circuit board and schematic diagram.

1.9 Why to study Diode Circuits?

- Most electronic systems, like HDTVs, audio power amplifiers, and computers, need a dc voltage to work properly. Since the power-line voltage is alternating and normally too high of a value, we need to reduce the ac line voltage and then convert it to a relatively constant dc output voltage.
- The section of the electronic system that produces this dc voltage is called the power supply.
- Within the power supply are circuits that allow current to flow in only one direction. These circuits are called rectifiers. Other circuits will filter and regulate the dc output.
- This section discusses rectifier circuits, filters, and an introduction to voltage regulators, clippers, clampers, and voltage multipliers.

1.10 The Half-Wave Rectifier

- Figure-31 shows a half-wave rectifier circuit. The ac source produces a sinusoidal voltage. Assuming an ideal diode, the positive half-cycle of source voltage will forward-bias the diode. Since the switch is closed, as shown in Figure-32, the positive half-cycle of source voltage will appear across the load resistor.
- On the negative half-cycle, the diode is reverse biased. In this case, the ideal diode will appear as an open switch, as shown in Figure-33, and no voltage appears across the load resistor.

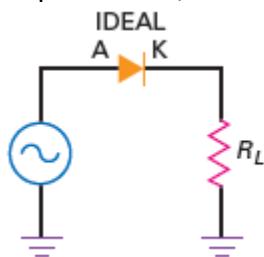


Figure-31 Ideal half-wave rectifier

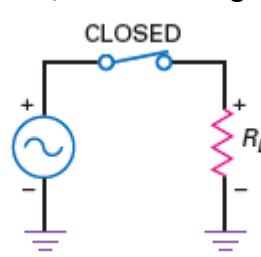


Figure-32 on positive half-cycle

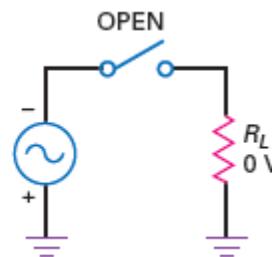


Figure-33 on negative half-cycle

1.10.1 Ideal Waveforms

- Figure-34 shows a graphical representation of the input voltage waveform.

- It is a sine wave with an instantaneous value of V_{in} and a peak value of $V_p(in)$. A pure sinusoid like this has an average value of zero over one cycle because each instantaneous voltage has an equal and opposite voltage half a cycle later.
- If you measure this voltage with a dc voltmeter, you will get a reading of zero because a dc voltmeter indicates the average value.
- In the half-wave rectifier of Figure-31, the diode is conducting during the positive half-cycles but is non-conducting during the negative half-cycles. Because of this, the circuit **clips off the negative half-cycles**, as shown in Figure-35.

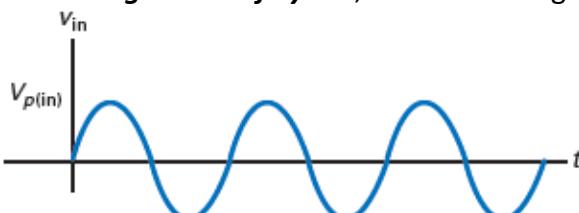


Figure-34 Input to half-wave rectifier



Figure-35 output of positive half-wave rectifier

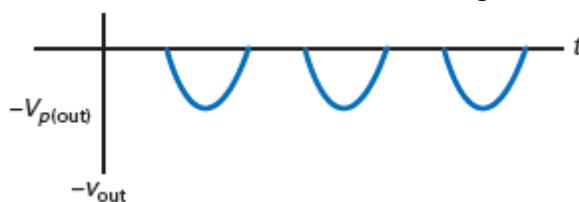


Figure-36 output of negative half-wave rectifier

- We call a waveform like this a half-wave signal. This half-wave voltage produces a unidirectional load current. This means that it flows in only one direction.
- If the diode were reversed, it would become forward biased when the input voltage was negative. As a result, the output pulses would be negative. This is shown in Figure-36.
- Notice how the negative peaks are offset from the positive peaks and follow the negative alternations of the input voltage.
- A half-wave signal like the one in Figure-35 is a pulsating dc voltage that increases to a maximum, decreases to zero, and then remains at zero during the negative half-cycle.
- This is not the kind of dc voltage we need for electronics equipment. What we need is a constant voltage, the same as you get from a battery.
- To get this kind of voltage, we need to filter the half-wave signal (discussed later in this chapter).
- When you are troubleshooting, you can use the ideal diode to analyze a half-wave rectifier. It's useful to remember that the peak output voltage equals the peak input voltage:

$$\text{Ideal half wave: } V_p(out) = V_p(in) \quad \dots \quad (7)$$

1.10.2 DC Value of Half-Wave Signal

- The dc value of a signal is the same as the average value. If you measure a signal with a dc voltmeter, the reading will equal the average value. In basic courses, the dc value of a half-wave signal is derived. The formula is:

$$\text{Half wave: } V_{dc} = \frac{V_p}{\pi} \quad \dots \quad (8)$$

- The proof of this derivation requires calculus because we have to work out the average value over one cycle.
- Since $1/\pi \approx 0.318$, you may see Eq. (8) written as:

$$V_{dc} \approx 0.318V_p$$
- When the equation is written in this form, you can see that the dc or average value equals 31.8 percent of the peak value. For instance, if the peak voltage of the half-wave signal is 100 V, the dc voltage or average value is 31.8 V.

1.10.3 Output Frequency

- The output frequency is the same as the input frequency. This makes sense when you compare Figure-35 with Figure-34. Each cycle of input voltage produces one cycle of output voltage. Therefore, we can write:

$$\text{Half wave: } f_{out} = f_{in} \quad \dots \quad (9)$$
- We will use this derivation later with filters.

1.10.4 Second Approximation

- We don't get a perfect half-wave voltage across the load resistor. Because of the barrier potential, the diode does not turn on until the ac source voltage reaches approximately 0.7 V.
- When the peak source voltage is much greater than 0.7 V, the load voltage will resemble a half-wave signal. For instance, if the peak source voltage is 100 V, the load voltage will be close to a perfect half-wave voltage.
- If the peak source voltage is only 5 V, the load voltage will have a peak of only 4.3 V.
- When you need to get a better answer, use this derivation:

$$\text{2d half wave: } V_{p(out)} = V_{p(in)} - 0.7 \text{ V} \quad \dots \quad (10)$$

1.10.5 Higher Approximations

- Most designers will make sure that the bulk resistance is much smaller than the Thevenin resistance facing the diode. Because of this, we can ignore bulk resistance in almost every case.
- If you must have better accuracy than you can get with the second approximation, you should use a computer and a circuit simulator like Multisim.

Example 6

Figure-37 shows a half-wave rectifier that you can build on the lab bench or on a computer screen with Multisim. An oscilloscope is across the $1 \text{ k}\Omega$. Set the oscilloscope's vertical input coupling switch or setting to dc. This will show us the half-wave load voltage. Also, a multimeter is across the $1 \text{ k}\Omega$ to read the dc load voltage. Calculate the theoretical values of peak load voltage and the dc load voltage. Then, compare these values to the readings on the oscilloscope and the multimeter.

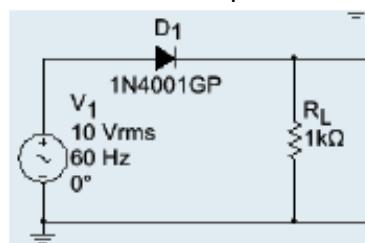


Figure-37

SOLUTION

- Figure-37 shows an ac source of 10 V and 60 Hz. Schematic diagrams usually show ac source voltages as effective or rms values. Recall that the effective value is the value of a dc voltage that produces the same heating effect as the ac voltage.
- Since the source voltage is **10 Vrms**, the first thing to do is calculate the peak value of the ac source. You know from earlier courses that the rms value of a sine wave equals:

$$V_{rms} = 0.707V_p$$

- Therefore, the peak source voltage in Figure-37 is:

$$V_p = \frac{V_{rms}}{0.707} = \frac{10\text{ V}}{0.707} = 14.1\text{ V}$$

- With an ideal diode, the peak load voltage is:

$$V_p(\text{out}) = V_p(\text{in}) = 14.1\text{ V}$$

- The dc load voltage is:

$$V_{dc} = \frac{V_p}{\pi} = \frac{14.1\text{ V}}{\pi} = 4.49\text{ V}$$

- With the second approximation, we get a peak load voltage of:

$$V_p(\text{out}) = V_p(\text{in}) - 0.7\text{ V} = 14.1\text{ V} - 0.7\text{ V} = 13.4\text{ V}$$

And a dc load voltage of:

$$V_{dc} = \frac{V_p}{\pi} = \frac{13.4\text{ V}}{\pi} = 4.27\text{ V}$$

PRACTICE PROBLEM 5

Using Figure-37, change the ac source voltage to **15 V**. Calculate the second approximation dc load voltage Vdc.

1.11 The Transformer

- Power companies in the United States supply a nominal line voltage of **120 Vrms** and a frequency of 60 Hz. The actual voltage coming out of a power outlet may vary from **105** to **125 Vrms**, depending on the time of day, the locality, and other factors.
- Line voltage is too high for most of the circuits used in electronics equipment. This is why a transformer is commonly used in the power-supply section of almost all electronics equipment.
- The transformer steps the line voltage down to safer and lower levels that are more suitable for use with diodes, transistors, and other semiconductor devices.

1.11.1 Basic Idea

- Figure-38 shows a transformer. Here, you see line voltage applied to the primary winding of a transformer. Usually, the power plug has a third prong to ground the equipment. Because of the turn's ratio **N₁/N₂**, the secondary voltage is stepped down when **N₁** is greater than **N₂**.

1.11.2 Phasing Dots

- Recall the meaning of the phasing dots shown at the upper ends of the windings. Dotted ends have the same instantaneous phase.

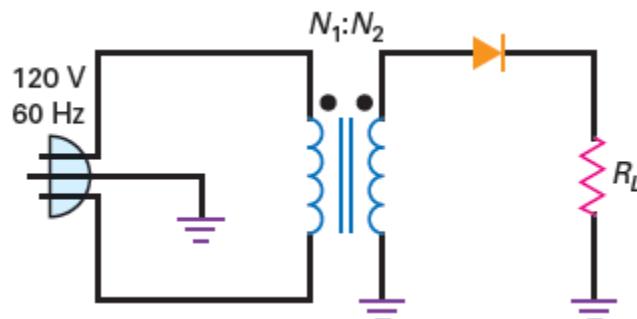


Figure-38 Half-wave rectifier with transformer

- In other words, when a positive half-cycle appears across the primary, a positive half-cycle appears across the secondary. If the secondary dot were on the ground end, the secondary voltage would be **180°** out of phase with the primary voltage.
- On the positive half-cycle of primary voltage, the secondary winding has a positive half-sine wave across it and the diode is forward biased.
- On the negative half-cycle of primary voltage, the secondary winding has a negative half-cycle and the diode is reverse biased. Assuming an ideal diode, we will get a half-wave load voltage.

1.11.3 Turns Ratio

- Recall from your earlier course work the following derivation:

$$V_2 = V_1 \frac{N_2}{N_1} \quad \text{----- (11)}$$

- This says that the secondary voltage equals the primary voltage divided by the turn's ratio.
- In other words the secondary voltage equals the inverse turns ratio times the primary voltage.
- You can use either formula for rms, peak values, and instantaneous voltages.
- Most of the time, we will use Eq. (11) with rms values because ac source voltages are almost always specified as rms values.
- The terms step up and step down are also encountered when dealing with transformers. These terms always relate the secondary voltage to the primary voltage.
- This means that a step-up transformer will produce a secondary voltage that is larger than the primary, and a step-down transformer will produce a secondary voltage that is smaller than the primary.

Example 7

What are the peak load voltage and dc load voltage in Figure-39?

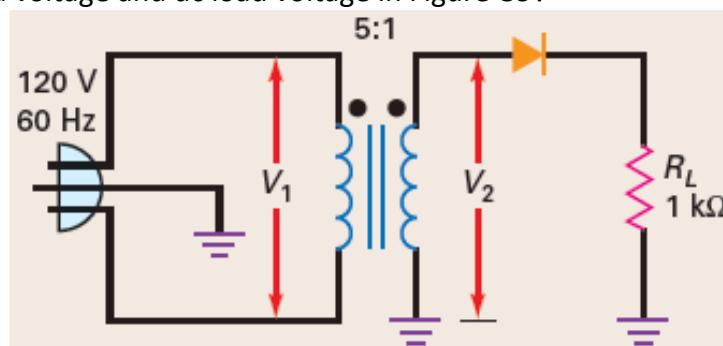


Figure-39

SOLUTION

The transformer has a turn's ratio of 5:1. This means that the rms secondary voltage is one-fifth of the primary voltage:

$$V_2 = \frac{120 V}{5} = 24 V$$

And the peak secondary voltage is:

$$V_p = \frac{24 V}{0.707} = 34 V$$

With an ideal diode, the peak load voltage is:

$$V_p (\text{out}) = 34 V$$

The dc load voltage is:

$$V_{dc} = \frac{V_p}{\pi} = \frac{34 V}{\pi} = 10.8 V$$

With the second approximation, the peak load voltage is:

$$V_p(\text{out}) = 34 V - 0.7 V = 33.3 V$$

And the dc load voltage is:

$$V_{dc} = \frac{V_p}{\pi} = \frac{33.3 V}{\pi} = 10.6 V$$

PRACTICE PROBLEM 6

Using Figure-39, change the transformer's turns ratio to **2:1** and solve for the ideal dc load voltage.

1.12 The Full-Wave Rectifier

- Figure-40 shows a full-wave rectifier circuit. Notice the grounded center tap on the secondary winding. The full-wave rectifier is equivalent to two half-wave rectifiers. Because of the center tap, each of these rectifiers has an input voltage equal to half the secondary voltage.

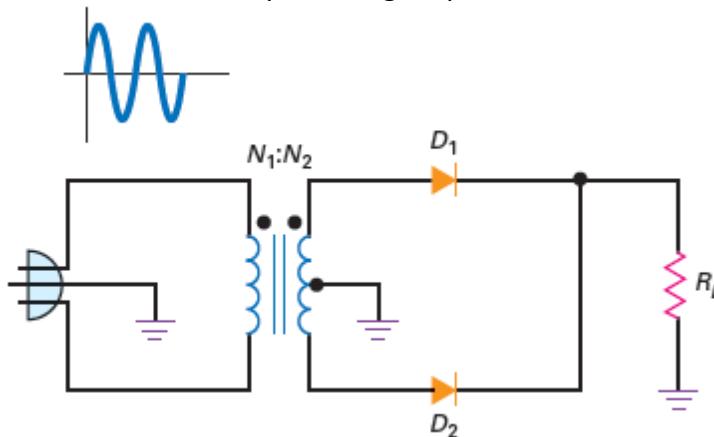


Figure-40 Full-wave rectifier

- Diode D1 conducts on the positive half-cycle, and diode D2 conducts on the negative half-cycle. As a result, the rectified load current flows during both half-cycles.
- The full-wave rectifier acts the same as two back-to-back half-wave rectifiers.
- Figure-41 shows the equivalent circuit for the positive half-cycle. As you see, D1 is forward biased. This produces a positive load voltage as indicated by the plus-minus polarity across the load resistor.

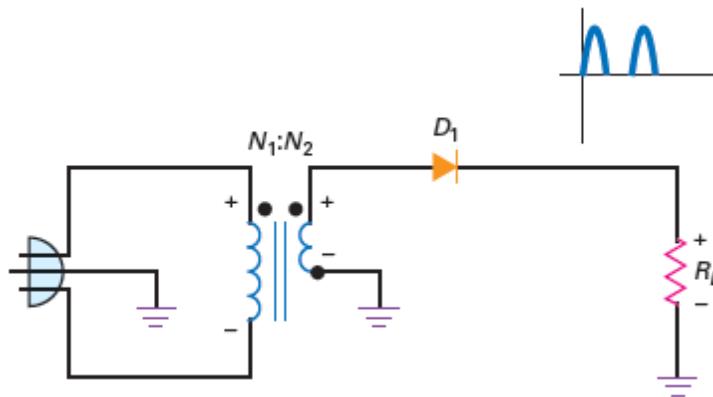


Figure-41 Equivalent circuit for positive half-cycle

- Figure-42 shows the equivalent circuit for the negative half-cycle. This time, D_2 is forward biased. As you can see, this also produces a positive load voltage.

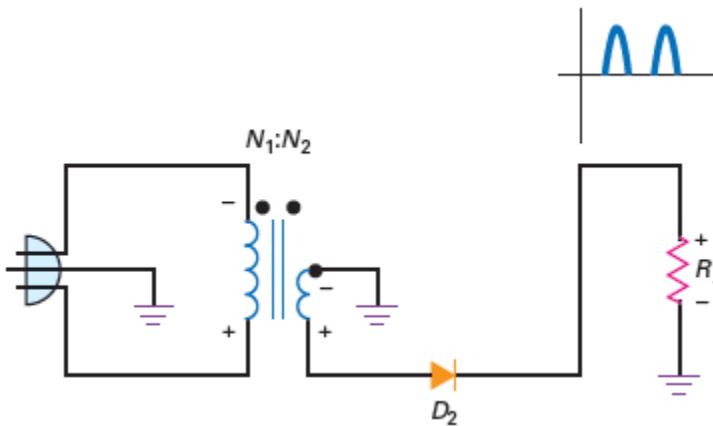


Figure-42 Equivalent circuit for negative half-cycle

- During both half-cycles, the load voltage has the same polarity and the load current is in the same direction. The circuit is called a full-wave rectifier because it has changed the ac input voltage to the pulsating dc output voltage shown in Figure-43. This waveform has some interesting properties that we will now discuss.

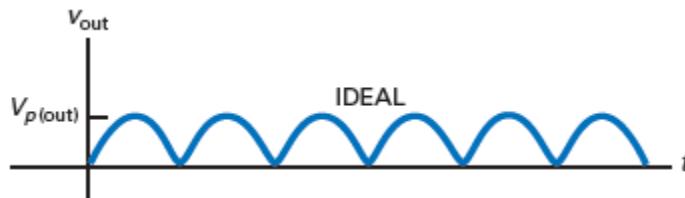


Figure-43 Full-wave output

1.12.1 DC or Average Value

- Since the full-wave signal has twice as many positive cycles as the half-wave signal, the dc or average value is twice as much, given by:

$$\text{Full wave: } V_{dc} = \frac{2V_p}{\pi} \quad \dots \quad (12)$$

- Since $2/\pi = 0.636$, you may see Eq. (12) written as:

$$V_{dc} \approx 0.636V_p$$

- In this form, you can see that the dc or average value equals **63.6** percent of the peak value. For instance, if the peak voltage of the full-wave signal is **100 V**, the dc voltage or average value is **63.6 V**.

1.12.2 Output Frequency

- With a half-wave rectifier, the output frequency equals the input frequency. But with a full-wave rectifier, something unusual happens to the output frequency.
- The ac line voltage has a frequency of 60 Hz. Therefore, the input period equals:

$$T_{in} = \frac{1}{f} = \frac{1}{60 \text{ Hz}} = 16.7 \text{ ms}$$

- Because of the full-wave rectification, the period of the full-wave signal is half the input period:

$$T_{out} = 0.5(16.7 \text{ ms}) = 8.33 \text{ ms}$$

(If there is any doubt in your mind, compare Figure-43 to Figure-35.) When we calculate the output frequency, we get:

$$fout = \frac{1}{T_{out}} = \frac{1}{8.33 \text{ ms}} = 120 \text{ Hz}$$

- The frequency of the full-wave signal is double the input frequency. This makes sense. A full-wave output has twice as many cycles as the sine-wave input has.
- The full-wave rectifier inverts each negative half-cycle so that we get double the number of positive half-cycles. The effect is to double the frequency. As a derivation:

$$\text{Full wave: } fout = 2fin \quad \text{----- (13)}$$

1.12.3 Second Approximation

- Since the full-wave rectifier is like two back-to-back half-wave rectifiers, we can use the second approximation given earlier. The idea is to subtract **0.7 V** from the ideal peak output voltage.

Example 8

Figure-44 shows a full-wave rectifier that you can build on a lab bench or on a computer screen with Multisim. Calculate the peak input and output voltages.

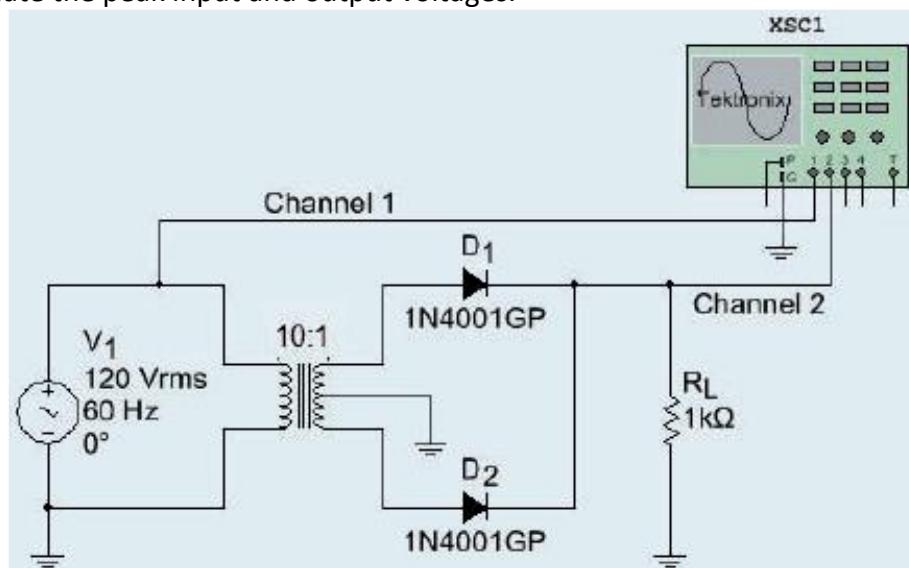


Figure-44

SOLUTION

The peak primary voltage is:

$$V_{P(1)} = \frac{V_{rms}}{0.707} = \frac{120\text{ V}}{0.707} = 170\text{ V}$$

Because of the 10:1 step-down transformer, the peak secondary voltage is:

$$V_{P(2)} = V_{P(1)} \frac{N_2}{N_1} = \frac{170\text{ V}}{10} = 10\text{ V}$$

The full-wave rectifier acts like two back-to-back half-wave rectifiers. Because of the center tap, the input voltage to each half-wave rectifier is only half the secondary voltage:

$$V_{P(in)} = 0.5(17\text{ V}) = 8.5\text{ V}$$

Ideally, the output voltage is:

$$V_{P(out)} = 8.5\text{ V}$$

Using the second approximation:

$$V_{P(out)} = 8.5\text{ V} - 0.7\text{ V} = 7.8\text{ V}$$

1.13 The Bridge Rectifier

- Figure-45 shows a bridge rectifier circuit. The bridge rectifier is similar to a full-wave rectifier because it produces a full-wave output voltage.
- Diodes D1 and D2 conduct on the positive half-cycle, and D3 and D4 conduct on the negative half-cycle. As a result, the rectified load current flows during both half-cycles.
- Figure-46 shows the equivalent circuit for the positive half-cycle. As you can see, D1 and D2 are forward biased. This produces a positive load voltage as indicated by the plus-minus polarity across the load resistor.
- As a memory aid, visualize D2 shorted. Then, the circuit that remains is a half-wave rectifier, which we are already familiar with.
- Figure-47 shows the equivalent circuit for the negative half-cycle. This time, D3 and D4 are forward biased. This also produces a positive load voltage.
- If you visualize D3 shorted, the circuit looks like a half-wave rectifier. So the bridge rectifier acts like two back-to-back half-wave rectifiers.
- During both half-cycles, the load voltage has the same polarity and the load current is in the same direction. The circuit has changed the ac input voltage to the pulsating dc output voltage shown in Figure-48. Note the advantage of this type of full-wave rectification over the center-tapped version in the previous section: ***The entire secondary voltage can be used.***
- Figure-49 shows bridge rectifier packages that contain all four diodes.

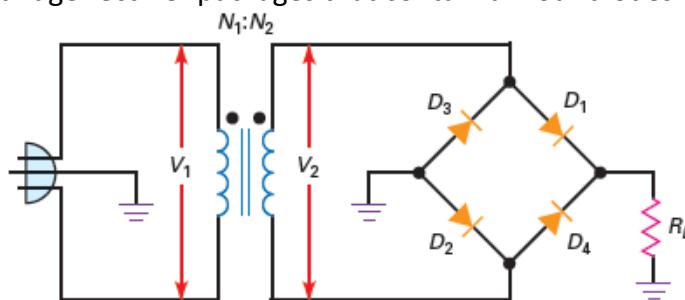


Figure-45 Bridge rectifier

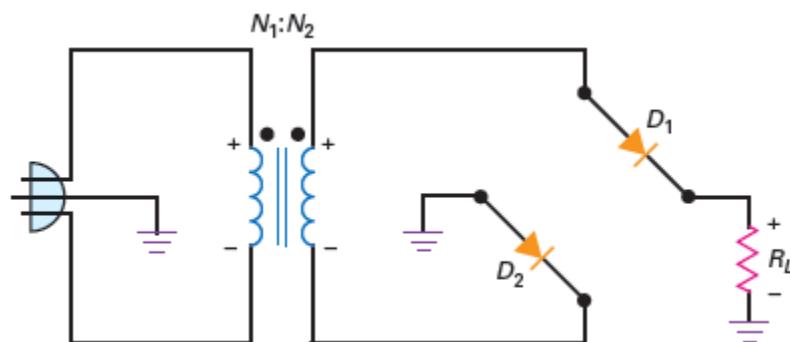


Figure-46 Equivalent circuit for positive half-cycle

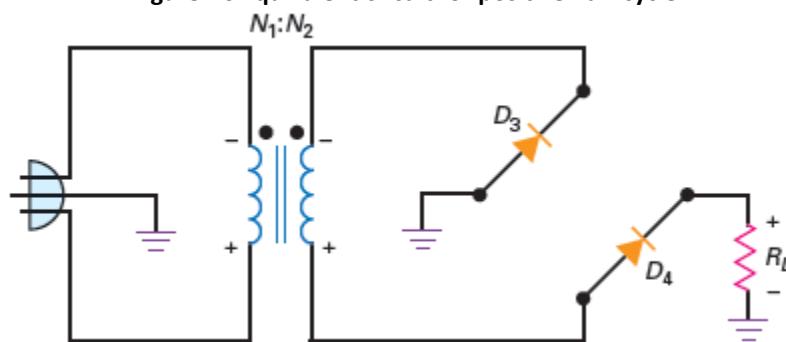


Figure-47 Equivalent circuit for negative half-cycle

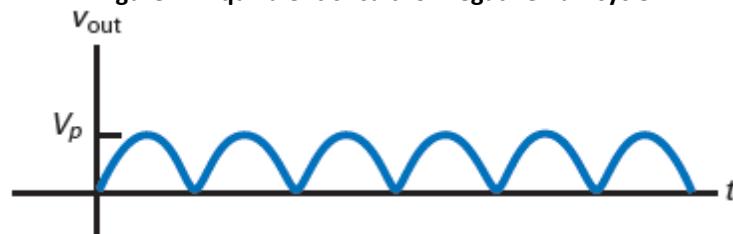


Figure-48 Full-wave output

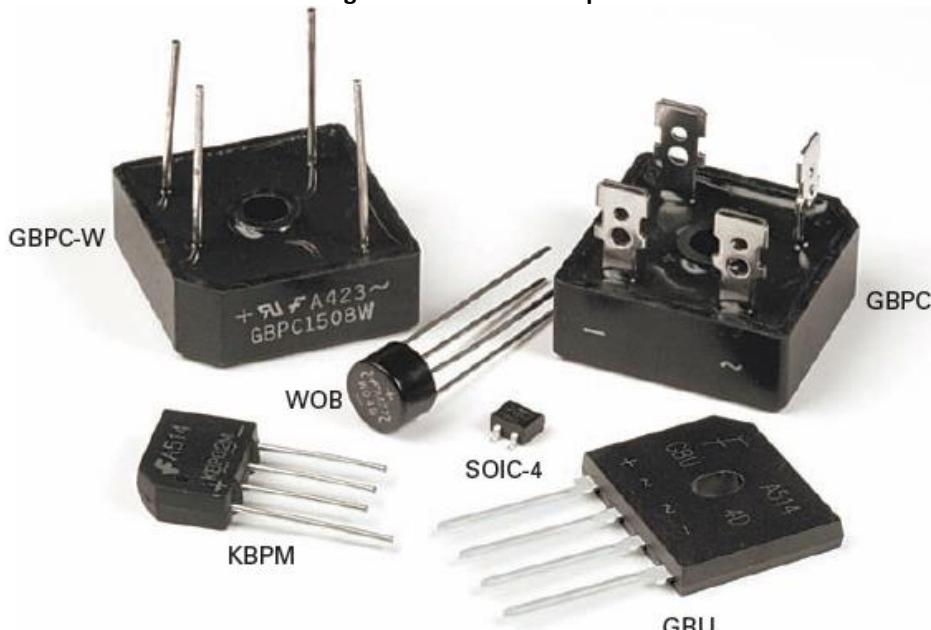


Figure-49 bridge rectifier packages

1.13.1 Average Value and Output Frequency

- Because a bridge rectifier produces a full-wave output, the equations for average value and output frequency are the same as those given for a full-wave rectifier:

$$\text{Full wave: } V_{dc} = \frac{2V_p}{\pi}$$

And

$$\text{Full wave: } f_{out} = 2f_{in}$$

- The average value is 63.6 percent of the peak value, and the output frequency is 120 Hz, given a line frequency of 60 Hz.
- One advantage of a bridge rectifier is that all the secondary voltage is used as the input to the rectifier.
- Given the same transformer, we get twice as much peak voltage and twice as much dc voltage with a bridge rectifier as with a full-wave rectifier.
- Doubling the dc output voltage compensates for having to use two extra diodes. As a rule, you will see the bridge rectifier used a lot more than the full-wave rectifier.
- Incidentally, the full-wave rectifier was in use for many years before the bridge rectifier was used. For this reason, it has retained the name full-wave rectifier even though a bridge rectifier also has a full-wave output.
- To distinguish the full-wave rectifier from the bridge rectifier, some literature may refer to a full-wave rectifier as a conventional full-wave rectifier, a two-diode full-wave rectifier, or a center-tapped full-wave rectifier.

1.13.2 Second Approximation and Other Losses

- Since the bridge rectifier has two diodes in the conducting path, the peak output voltage is given by:

$$2d \text{ bridge: } V_{p(out)} = V_{p(in)} - 1.4 \text{ V} \quad (14)$$

- As you can see, we have to subtract two diode drops from the peak to get a more accurate value of peak load voltage. Summary Table compares the three rectifiers and their properties.

	Half-wave	Full-wave	Bridge
Number of diodes	1	2	4
Rectifier input	$V_{p(2)}$	$0.5V_{p(2)}$	$V_{p(2)}$
Peak output (ideal)	$V_{p(2)}$	$0.5V_{p(2)}$	$V_{p(2)}$
Peak output (2d)	$V_{p(2)} - 0.7 \text{ V}$	$0.5V_{p(2)} - 0.7 \text{ V}$	$V_{p(2)} - 1.4 \text{ V}$
DC output	$V_{p(out)}/\pi$	$2V_{p(out)}/\pi$	$2V_{p(out)}/\pi$
Ripple frequency	f_{in}	$2f_{in}$	$2f_{in}$

* $V_{p(2)}$ = peak secondary voltage; $V_{p(out)}$ = peak output voltage.

1.14 The Choke-Input Filter

- At one time, the choke-input filter was widely used to filter the output of a rectifier. Although not used much anymore because of its cost, bulk, and weight, this type of filter has instructional value and helps make it easier to understand other filters.

1.14.1 Basic Idea

- Look at Figure-50. This type of filter is called a choke-input filter. The ac source produces a current in the inductor, capacitor, and resistor. The ac current in each component depends on the inductive reactance, capacitive reactance, and the resistance. The inductor has a reactance given by:

$$X_L = 2\pi fL$$

- The capacitor has a reactance given by:

$$X_C = \frac{1}{2\pi fC}$$

- As you learned in previous courses, the choke (or inductor) has the **primary characteristic of opposing a change in current**. Because of this, a choke-input filter ideally reduces the ac current in the load resistor to zero.
- To a second approximation, it reduces the ac load current to a very small value. Let us find out why?
- The first requirement of a well-designed choke-input filter is to have X_C at the input frequency be much smaller than R_L . When this condition is satisfied, we can ignore the load resistance and use the equivalent circuit of Figure-51.

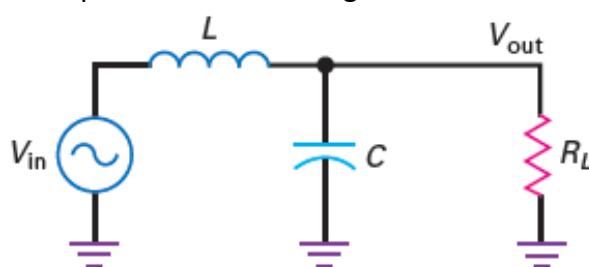


Figure-50 Choke-input filter

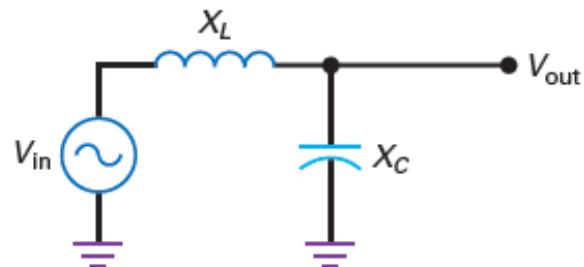


Figure-51 AC-equivalent circuit

- The second requirement of a well-designed choke-input filter is to have X_L be much greater than X_C at the input frequency. When this condition is satisfied, the ac output voltage approaches zero.
- On the other hand, since the choke approximates a **short circuit** at **0 Hz** and the capacitor **approximates an open** at **0 Hz**, the dc current can be passed to the load resistance with minimum loss.
- In Figure-51, the circuit acts like a reactive voltage divider. When X_L is much greater than X_C , almost all the ac voltage is dropped across the choke. In this case, the ac output voltage equals:

$$V_{out} \approx \frac{X_C}{X_L} V_{in} \quad \dots \quad (15)$$

- For instance, if $X_L = 10 \text{ k}\Omega$, $X_C = 100 \Omega$, and $V_{in} = 15 \text{ V}$, the ac output voltage is:

$$V_{out} \approx \frac{100\Omega}{10k\Omega} 15 \text{ V} = 0.15 \text{ V}$$

- In this example, the choke-input filter reduces the ac voltage by a factor of 100.

1.14.2 Filtering the Output of a Rectifier

- Figure-52 shows a choke-input filter between a rectifier and a load. The rectifier can be a half-wave, full-wave, or bridge type. What effect does the choke input filter have on the load voltage?
- The easiest way to solve this problem is to use the superposition theorem. Recall what this theorem says: **If you have two or more sources, you can analyze the circuit for each source separately and then add the individual voltages to get the total voltage.**

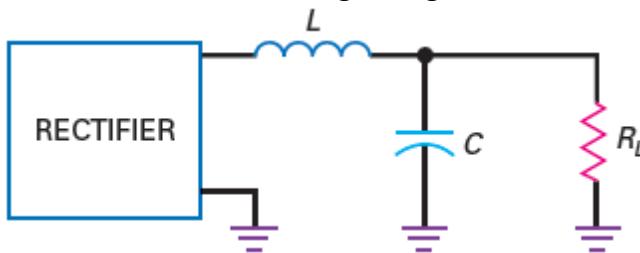


Figure-52 Rectifier with Choke-input filter

- The rectifier output has two different components: a dc voltage (the average value) and an ac voltage (the fluctuating part), as shown in Figure-53.

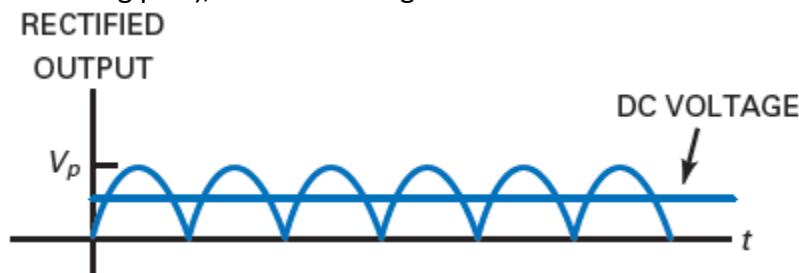


Figure-53 Rectifier output has dc and ac components

- Each of these voltages acts like a separate source. As far as the ac voltage is concerned, X_L is much greater than X_C , and this results in very little ac voltage across the load resistor. Even though the ac component is not a pure sine wave, Eq. (15) is still a close approximation for the ac load voltage.
- The circuit acts like Figure-54 as far as dc voltage is concerned. At **0 Hz**, the inductive reactance is zero and the capacitive reactance is infinite. Only the series resistance of the inductor windings remains.

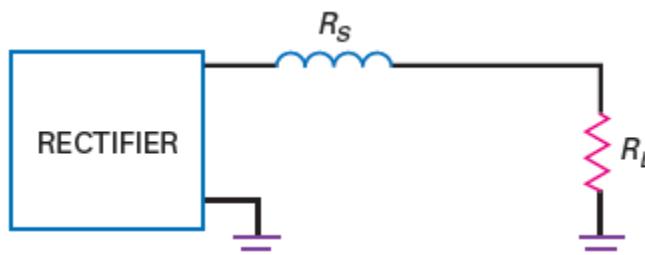


Figure-54 DC-equivalent circuit

- Making R_S much smaller than R_L causes most of the dc component to appear across the load resistor.

- That's how a choke-input filter works: Almost all of the dc component is passed on to the load resistor, and almost all of the ac component is blocked.
- In this way, we get an almost perfect dc voltage, one that is almost constant, like the voltage out of a battery. Figure-55 shows the filtered output for a full-wave signal.

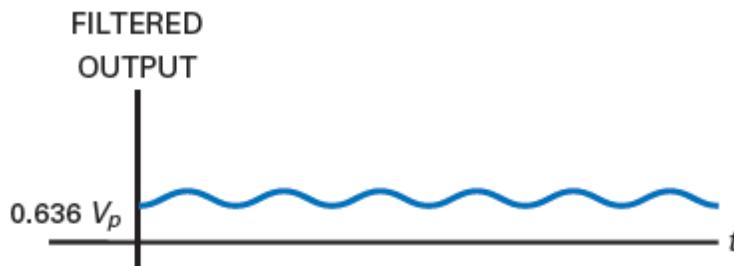


Figure-55 filter output is a dc voltage with small ripple

- The only deviation from a perfect dc voltage is the small ac load voltage shown in Figure-55. This small ac load voltage is called ripple. With an oscilloscope, we can measure its peak-to-peak value.
- To measure the ripple value, set the oscilloscope's vertical input coupling switch or setting to ac instead of dc. This will allow you to see the ac component of the waveform while blocking the dc or average value.

1.14.3 Main Disadvantage

- A **power supply** is the circuit inside electronics equipment that converts the ac input voltage to an almost perfect dc output voltage. It includes a rectifier and a filter.
- The trend nowadays is toward low-voltage, high-current power supplies. Because line frequency is only 60 Hz, large inductances have to be used to get enough reactance for adequate filtering. But large inductors have large winding resistances, which create a serious design problem with large load currents.
- In other words, too much dc voltage is dropped across the choke resistance. Furthermore, bulky inductors are not suitable for modern semiconductor circuits, where the emphasis is on lightweight designs.

1.14.4 Switching Regulators

- One important application does exist for the choke-input filter. A switching regulator is a special kind of power supply used in computers, monitors, and an increasing variety of equipment.
- The frequency used in a switching regulator is much higher than 60 Hz.
- Typically, the frequency being filtered is above 20 kHz. At this much higher frequency, we can use much smaller inductors to design efficient choke-input filters.

1.15 The Capacitor-Input Filter

- The choke-input filter produces a dc output voltage equal to the average value of the rectified voltage. The capacitor-input filter produces a dc output voltage equal to the peak value of the rectified voltage. This type of filter is the most widely used in power supplies.

1.15.1 Basic Idea

- Figure-56a shows an ac source, a diode, and a capacitor. The key to understanding a capacitor-input filter is understanding what this simple circuit does during the first quarter-cycle.
- Initially, the capacitor is uncharged. During the first quarter-cycle of Figure-56b, the diode is forward biased.
- Since it ideally acts like a closed switch, the capacitor charges, and its voltage equals the source voltage at each instant of the first quarter-cycle. The charging continues until the input reaches its maximum value. At this point, the capacitor voltage equals V_p .

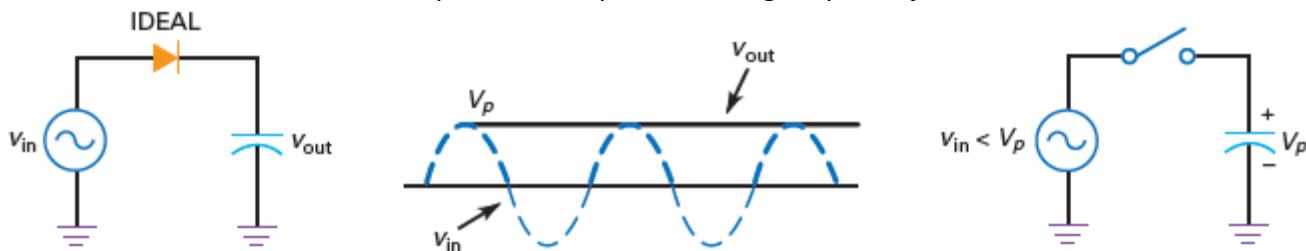


Figure-56 (a) Unloaded capacitor-input filter (b) output is pure dc voltage (c) capacitor remains charged when diode is off

- After the input voltage reaches the peak, it starts to decrease. As soon as the input voltage is less than V_p , the diode turns off. In this case, it acts like the open switch of Figure-56c. During the remaining cycles, the capacitor stays fully charged and the diode remains open.
- This is why the output voltage of Figure-56b is constant and equal to V_p . Ideally, all that the capacitor-input filter does is charge the capacitor to the peak voltage during the first quarter-cycle. This peak voltage is constant, the perfect dc voltage we need for electronics equipment.
- There's only one problem: There is no load resistor.

1.15.2 Effect of Load Resistor

- For the capacitor-input filter to be useful, we need to connect a load resistor across the capacitor, as shown in Figure-57a. As long as the **RLC** time constant is much greater than the period, the capacitor remains almost fully charged and the load voltage is approximately V_p .
- The only deviation from a perfect dc voltage is the small ripple seen in Figure-57b. The smaller the peak-to-peak value of this ripple, the more closely the output approaches a perfect dc voltage.

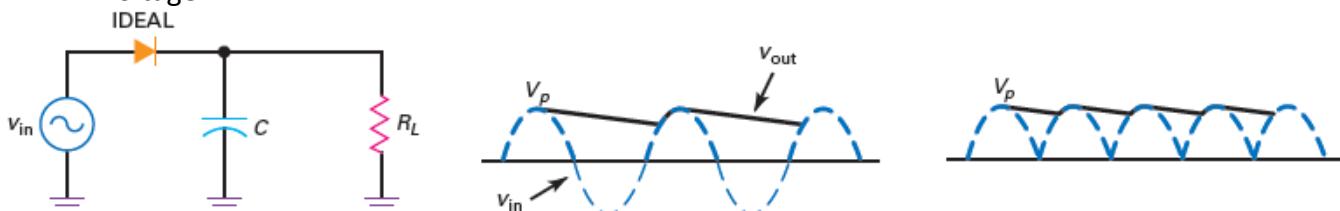


Figure-57 (a) Loaded capacitor-input filter (b) output is a dc voltage with small ripple (c) full-wave output has less ripple

- Between peaks, the diode is off and the capacitor discharges through the load resistor. In other words, the capacitor supplies the load current.
- Since the capacitor discharges only slightly between peaks, the peak-to-peak ripple is small.
- When the next peak arrives, the diode conducts briefly and recharges the capacitor to the peak value. A key question is: What size should the capacitor be for proper operation?

- Before discussing capacitor size, consider what happens with the other rectifier circuits.

1.15.3 Full-Wave Filtering

- If we connect a full-wave or bridge rectifier to a capacitor-input filter, the peak-to-peak ripple is cut in half. Figure-57c shows why.
- When a full-wave voltage is applied to the RC circuit, the capacitor discharges for only half as long. Therefore, the peak-to-peak ripple is half the size it would be with a half-wave rectifier.

1.15.4 The Ripple Formula

- Here is a derivation we will use to estimate the peak-to-peak ripple out of any capacitor-input filter:

$$V_R = \frac{I}{fC} \quad \text{--- (16)}$$

Where, ***V_R* = peak-to-peak ripple voltage**

***I* = dc load current**

***f* = ripple frequency**

***C* = capacitance**

- This is an approximation, not an exact derivation. We can use this formula to estimate the peak-to-peak ripple. When a more accurate answer is needed, one solution is to use a computer with a circuit simulator like Multisim.
- For instance, if the dc load current is **10 mA** and the capacitance is **200 μF**, the ripple with a bridge rectifier and a capacitor-input filter is:

$$V_R = \frac{10 \text{ mA}}{(120 \text{ Hz})(200 \mu\text{F})} = 0.417 \text{ Vp-p}$$

- When using this derivation, remember two things. First, the ripple is in peak-to-peak (p-p) voltage. This is useful because you normally measure ripple voltage with an oscilloscope. Second, the formula works with half-wave or full-wave voltages. Use 60 Hz for half wave, and 120 Hz for full wave.
- You should use an oscilloscope for ripple measurements if one is available. If not, you can use an ac voltmeter, although there will be a significant error in the measurement.
- Most ac voltmeters are calibrated to read the rms value of a sine wave. Since the ripple is not a sine wave, you may get a measurement error of as much as 25 percent, depending on the design of the ac voltmeter.
- But this should be no problem when you are troubleshooting, since you will be looking for much larger changes in ripple.
- If you do use an ac voltmeter to measure the ripple, you can convert the peak-to-peak value given by Eq. (16) to an rms value using the following formula for a sine wave:

$$V_{rms} = \frac{V_{p-p}}{2\sqrt{2}}$$

- Dividing by 2 converts the peak-to-peak value to a peak value, and dividing by $\sqrt{2}$ gives the rms value of a sine wave with the same peak-to-peak value as the ripple voltage.

1.15.5 Exact DC Load Voltage

- It is difficult to calculate the exact dc load voltage in a bridge rectifier with a capacitor-input filter.
- To begin with, we have the two diode drops that are subtracted from the peak voltage. Besides the diode drops, an additional voltage drop occurs, as follows: The diodes conduct heavily when recharging the capacitor because they are on for only a short time during each cycle.
- This brief but large current has to flow through the transformer windings and the bulk resistance of the diodes. In our examples, we will calculate either the ideal output or the output with the second approximation of a diode, remembering that the actual dc voltage is slightly lower.

Example 9

What is the dc load voltage and ripple in Figure-58?

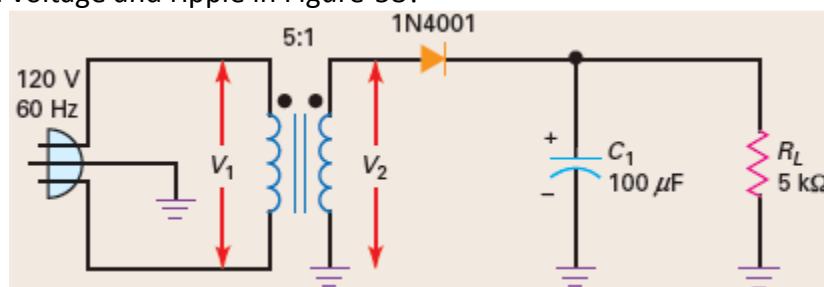


Figure-58

SOLUTION

The rms secondary voltage is:

$$V_2 = \frac{120 \text{ V}}{5} = 24 \text{ V}$$

The peak secondary voltage is:

$$V_p = \frac{24 \text{ V}}{0.707} = 34 \text{ V}$$

Assuming an ideal diode and small ripple, the dc load voltage is:

$$V_L = 34 \text{ V}$$

To calculate the ripple, we first need to get the dc load current:

$$I_L = \frac{V_L}{R_L} = \frac{34 \text{ V}}{5 \text{ k}\Omega} = 6.8 \text{ mA}$$

Now we can use Eq. (16) to get:

$$V_R = \frac{6.8 \text{ mA}}{(60 \text{ Hz})(100 \mu\text{F})} = 1.13 V_{P-P} \approx 1.1 V_{P-P}$$

- We rounded the ripple to two significant digits because it is an approximation and cannot be accurately measured with an oscilloscope with greater precision.
- Here is how to improve the answer slightly: There is about **0.7 V** across a silicon diode when it is conducting. Therefore, the peak voltage across the load will be closer to **33.3 V** than to **34 V**. The ripple also lowers the dc voltage slightly.
- So the actual dc load voltage will be closer to **33 V** than to **34 V**. But these are minor deviations. Ideal answers are usually adequate for troubleshooting and preliminary analysis.
- A final point about the circuit. The plus and minus signs on the filter capacitor indicates a polarized capacitor, one whose plus side must be connected to the positive rectifier output.

- In Figure-59, the plus sign on the capacitor case is correctly connected to the positive output voltage. You must look carefully at the capacitor case when you are building or troubleshooting a circuit to find out whether it is polarized or not.
- If you reverse the polarity of the rectifier diodes and build a negative power-supply circuit, be sure to connect the capacitor's negative side to the negative output voltage point and the positive capacitor side to circuit ground.
- Power supplies often use polarized electrolytic capacitors because this type can provide high values of capacitance in small packages. As discussed in earlier courses, electrolytic capacitors must be connected with the correct polarity to produce the oxide film. **If an electrolytic capacitor is connected in opposite polarity, it becomes hot and may explode.**

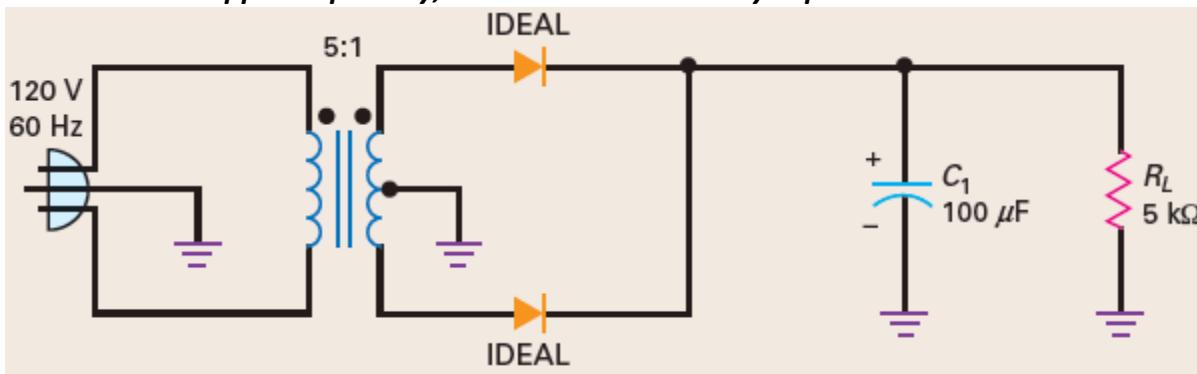


Figure-59 Full-wave rectifier and capacitor-input filter

Example 10

What is the dc load voltage and ripple in Figure-59?

SOLUTION

Since the transformer is 5:1 step-down like the preceding example, the peak secondary voltage is still **34 V**. Half this voltage is the input to each half wave section. Assuming an ideal diode and small ripple, the dc load voltage is:

$$V_L = 17 \text{ V}$$

The dc load current is:

$$I_L = \frac{17 \text{ V}}{5 \text{ k}\Omega} = 3.4 \text{ mA}$$

Now, Eq. (16) gives:

$$V_R = \frac{3.4 \text{ mA}}{(120 \text{ Hz})(100 \mu\text{F})} = 0.283 \text{ V}_{P-P} \approx 0.28 \text{ V}_{P-P}$$

Because of the **0.7 V** across the conducting diode, the actual dc load voltage will be closer to **16 V** than to **17 V**.

PRACTICE PROBLEM 7

Using Figure-59, change R_L to **2 kΩ** and calculate the new ideal dc load voltage and ripple.

Example 11

What is the dc load voltage and ripple in Figure-60? Compare the answers with those in the two preceding examples.

SOLUTION

Since the transformer is **5:1** step-down as in the preceding example, the peak secondary voltage is still **34 V**. Assuming an ideal diode and small ripple, the dc load voltage is:

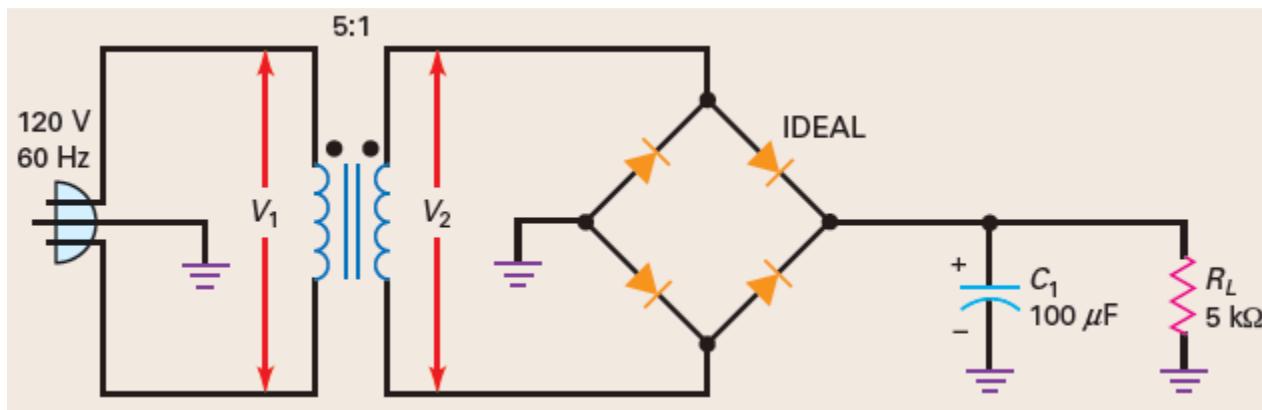


Figure-60 Bridge rectifier and capacitor-input filter

$$V_L = 34 \text{ V}$$

The dc load current is:

$$I_L = \frac{34 \text{ V}}{5 \text{ k}\Omega} = 6.8 \text{ mA}$$

Now, Eq. (16) gives:

$$V_R = \frac{6.8 \text{ mA}}{(120 \text{ Hz})(100 \mu\text{F})} = 0.566 \text{ V}_{P-P} \approx 0.57 \text{ V}_{P-P}$$

Because of the 1.4 V across two conducting diodes and the ripple, the actual dc load voltage will be closer to 32 V than to 34 V. We have calculated the dc load voltage and ripple for the three different rectifiers. Here are the results:

Half-wave: 34 V and 1.13 V

Full-wave: 17 V and 0.288 V

Bridge: 34 V and 0.566 V

For a given transformer, the bridge rectifier is better than the half-wave rectifier because it has less ripple, and it's better than the full-wave rectifier because it produces twice as much output voltage. Of the three, the bridge rectifier has emerged as the most popular.

1.16 Peak Inverse Voltage and Surge Current

- The peak inverse voltage (PIV) is the maximum voltage across the non-conducting diode of a rectifier. This voltage must be less than the breakdown voltage of the diode; otherwise, the diode will be destroyed.
- The peak inverse voltage depends on the type of rectifier and filter. The worst case occurs with the capacitor-input filter.
- As discussed earlier, data sheets from various manufacturers use many different symbols to indicate the maximum reverse voltage rating of a diode.
- Sometimes, these symbols indicate different conditions of measurement. Some of the data sheet symbols for the maximum reverse voltage rating are **PIV**, **PRV**, **V_B**, **V_{BR}**, **V_R**, **V_{RRM}**, **V_{RWM}**, and **V_{R(max)}**.

1.16.1 Half-Wave Rectifier with Capacitor-Input Filter

- Figure-61 shows the critical part of a half-wave rectifier. This is the part of the circuit that determines how much reverse voltage is across the diode.

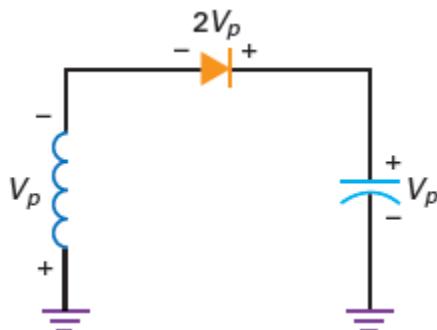


Figure-61 Peak inverse voltage in half-wave rectifier

- The rest of the circuit has no effect and is omitted for the sake of clarity. In the worst case, the peak secondary voltage is on the negative peak and the capacitor is fully charged with a voltage of V_p . Apply Kirchhoff's voltage law, and you can see right away that the peak inverse voltage across the non-conducting diode is:

$$PIV = 2 V_p \quad \text{----- (17)}$$

- For instance, if the peak secondary voltage is **15 V**, the peak inverse voltage is **30 V**. As long as the breakdown voltage of the diode is greater than this, the diode will not be damaged.

1.16.2 Full-Wave Rectifier with Capacitor-Input Filter

- Figure-62 shows the essential part of a full-wave rectifier needed to calculate the peak inverse voltage.

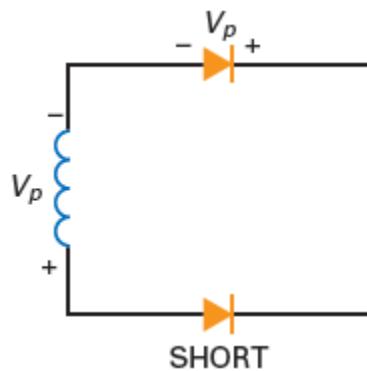


Figure-62 Peak inverse voltage in full-wave rectifier

- Again, the secondary voltage is at the negative peak. In this case, the lower diode acts like a short (closed switch) and the upper diode is open. Kirchhoff's law implies:

$$PIV = V_p \quad \text{----- (18)}$$

1.16.3 Bridge Rectifier with Capacitor-Input Filter

- Figure-63 shows part of a bridge rectifier. This is all you need to calculate the peak inverse voltage. Since the upper diode is shorted and the lower one is open, the peak inverse voltage across the lower diode is:

$$PIV = V_p \quad \text{----- (19)}$$

- Another advantage of the bridge rectifier is that it has the lowest peak inverse voltage for a given load voltage. To produce the same load voltage, the full-wave rectifier would need twice as much secondary voltage.

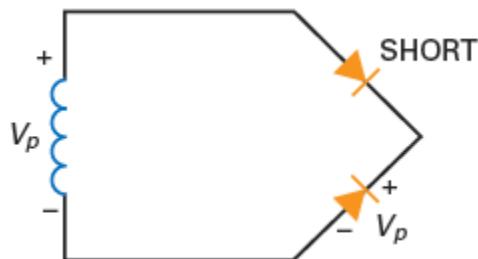


Figure-63 peak inverse voltage in bridge wave rectifier

1.16.4 Surge Resistor

- Before the power is turned on, the filter capacitor is uncharged. At the first instant the power is applied, this capacitor looks like a short. Therefore, the initial charging current may be very large.
- All that exists in the charging path to impede the current is the resistance of the transformer windings and the bulk resistance of the diodes. The initial rush of current when the power is turned on is called the surge current.
- Ordinarily, the designer of the power supply will select a diode with enough current rating to withstand the surge current. The key to the surge current is the size of the filter capacitor.
- Occasionally, a designer may decide to use a surge resistor rather than select another diode.
- Figure-64 illustrates the idea. A small resistor is inserted between the bridge rectifier and the capacitor-input filter.

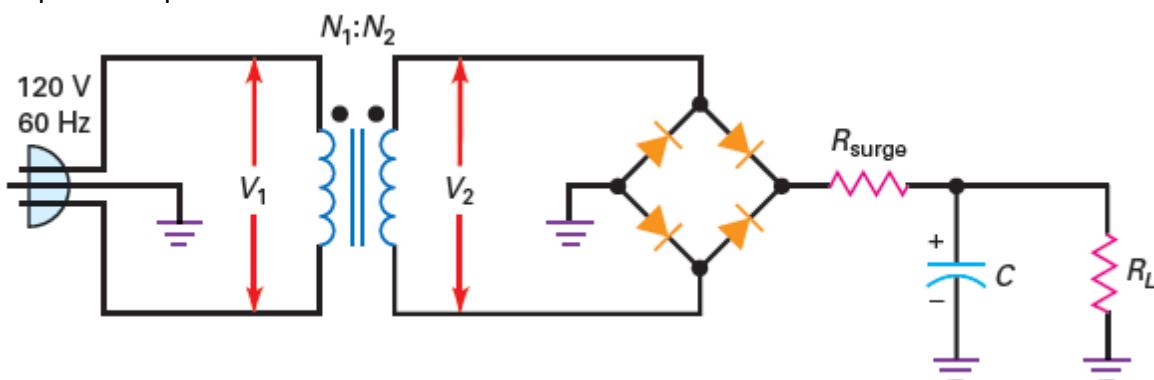


Figure-64 Surge resistor limits surge current

- Without the resistor, the surge current might destroy the diodes. By including the surge resistor, the designer reduces the surge current to a safe level.
- Surge resistors are not used very often and are mentioned just in case you see one used in a power supply.

Example 4-10

What is the peak inverse voltage in Figure-64 if the turn's ratio is 8:1? A **1N4001** has a breakdown voltage of **50 V**. Is it safe to use a **1N4001** in this circuit?

SOLUTION

The rms secondary voltage is:

$$V_2 = \frac{120 V}{8} = 15 V$$

The peak secondary voltage is:

$$V_P = \frac{15 V}{0.707} = 21.2 V$$

The peak inverse voltage is:

$$PIV = 21.2 V$$

The **1N4001** is more than adequate, since the peak inverse voltage is much less than the breakdown voltage of **50 V**.

PRACTICE PROBLEM 8

Using Figure-64, change the transformer's turns ratio to 2:1. Which 1N4000 series of diodes should you use?

1.17 Design of Unregulated DC Power-Supply

- You have a basic idea of how power-supply circuits work. In the preceding sections, you have seen how an ac input voltage is rectified and filtered to get a dc voltage. There are a few additional ideas you need to know about.

1.17.1 Commercial Transformers

- The use of turn's ratios with transformers applies only to ideal transformers. Iron core transformers are different. In other words, the transformers you buy from a parts supplier are not ideal because the windings have resistance, which produces power losses.
- Furthermore, the laminated core has eddy currents, which produce additional power losses. Because of these unwanted power losses, the turn's ratio is only an approximation. In fact, the data sheets for transformers rarely list the turn's ratio. Usually, all you get is the secondary voltage at a rated current.
- For instance, Figure-65 shows an F-25X, an industrial transformer whose data sheet gives only the following specifications: for a primary voltage of 115 V ac, the secondary voltage is 12.6 V ac when the secondary current is 1.5 A.



Figure-65 Rating on real transformer

- If the secondary current is less than 1.5 A in Figure-65, the secondary voltage will be more than 12.6 V ac because of lower power losses in the windings and laminated core.
- If it is necessary to know the primary current, you can estimate the turns ratio of a real transformer by using this definition:

$$\frac{N_1}{N_2} = \frac{V_1}{V_2}$$

- For instance, the F25X has $V_1 = 115 V$ and $V_2 = 12.6 V$. The turns ratio at the rated load current of 1.5 A is:

$$\frac{N_1}{N_2} = \frac{115}{12.6} = 9.13$$

- This is an approximation because the calculated turn's ratio decreases when the load current decreases.

1.17.2 Calculating Fuse Current

- When troubleshooting, you may need to calculate the primary current to determine whether a fuse is adequate or not. The easiest way to do this with a real transformer is to assume that the input power equals the output power: $P_{in} = P_{out}$
- For instance, Figure-66 shows a fused transformer driving a filtered rectifier. Is the 0.1-A fuse adequate?
- Here is how to estimate the primary current when troubleshooting. The output power equals the dc load power:

$$P_{out} = V \times I = (15 \text{ V})(1.2 \text{ A}) = 18 \text{ W}$$

- Ignore the power losses in the rectifier and the transformer. Since the input power must equal the output power:

$$P_{in} = 18 \text{ W}$$

- Since $P_{in} = V_1 I_1$, we can solve for the primary current:

$$I_1 = \frac{18 \text{ W}}{115 \text{ V}} = 0.156 \text{ A}$$

- This is only an estimate because we ignored the power losses in the transformer and rectifier. The actual primary current will be higher by about **5 to 20** percent because of these additional losses. In any case, the fuse is inadequate. It should be at least 0.25 A.

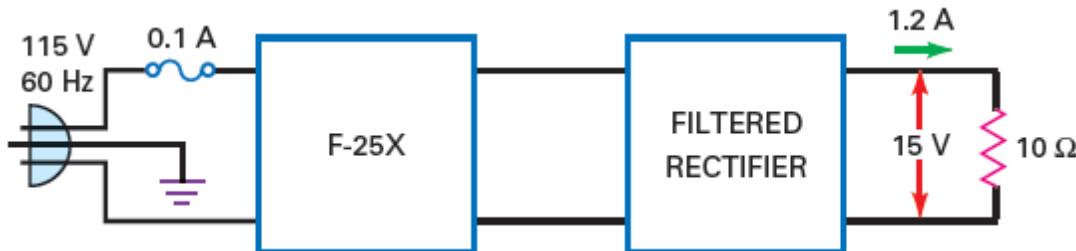


Figure-66 Calculating fuse current

1.17.3 Slow-Blow Fuses

- Assume that a capacitor-input filter is used in Figure-66. If an ordinary 0.25-A fuse is used in Figure-66, it will blow out when you turn the power on. The reason is the surge current, described earlier.
- Most power supplies use a slow-blow fuse, one that can temporarily withstand overloads in current. For instance, a 0.25-A slow-blow fuse can withstand

2 A for 0.1 s
1.5 A for 1 s
1 A for 2 s

And so on. With a slow-blow fuse, the circuit has time to charge the capacitor. Then, the primary current drops down to its normal level with the fuse still intact.

1.17.4 Calculating Diode Current

- Whether a half-wave rectifier is filtered or not, the average current through the diode has to equal the dc load current because there is only one path for current.
- As a derivation:

$$\text{Half wave: } I_{\text{diode}} = I_{\text{dc}} \quad (20)$$

- On the other hand, the average current through a diode in the full-wave rectifier equals only half the dc load current because there are two diodes in the circuit, each sharing the load.
- Similarly, each diode in a bridge rectifier has to withstand an average current of half the dc load current. As a derivation:

$$\text{Full wave: } I_{\text{diode}} = 0.5 I_{\text{dc}} \quad (21)$$

- Summary Table compares the properties of the three capacitor-input filtered rectifiers.

	Half-wave	Full-wave	Bridge
Number of diodes	1	2	4
Rectifier input	$V_{P(2)}$	$0.5V_{P(2)}$	$V_{P(2)}$
DC output (ideal)	$V_{P(2)}$	$0.5V_{P(2)}$	$V_{P(2)}$
DC output (2d)	$V_{P(2)} - 0.7 \text{ V}$	$0.5V_{P(2)} - 0.7 \text{ V}$	$V_{P(2)} - 1.4 \text{ V}$
Ripple frequency	f_{in}	$2f_{\text{in}}$	$2f_{\text{in}}$
PIV	$2V_{P(2)}$	$V_{P(2)}$	$V_{P(2)}$
Diode current	I_{dc}	$0.5I_{\text{dc}}$	$0.5I_{\text{dc}}$

* $V_{P(2)}$ = Peak secondary voltage; $V_{P(\text{out})}$ = Peak output voltage; I_{dc} = dc load current.

1.17.5 RC Filters

- Before the 1970s, passive filters (R, L, and C components) were often connected between the rectifier and the load resistance. Nowadays, you rarely see passive filters used in semiconductor power supplies, but there might be special applications, such as audio power amplifiers, in which you might encounter them.

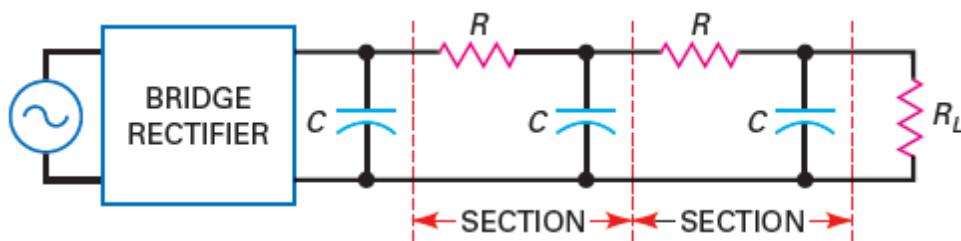


Figure-67 RC filtering

- Figure-67 shows a bridge rectifier and a capacitor-input filter. Usually, a designer will settle for a peak-to-peak ripple of as much as 10 percent across the filter capacitor. The reason for not trying

to get even lower ripple is because the **filter capacitor would become too large**. Additional filtering is then done by RC sections between the filter capacitor and the load resistor.

- The RC sections are examples of a passive filter, one that uses only **R**, **L**, or **C** components. By deliberate design, R is much greater than X_C at the ripple frequency. Therefore, the ripple is reduced before it reaches the load resistor.
- Typically, **R** is at least **10** times greater than X_C . This means that each section attenuates (reduces) the ripple by a factor of at least **10**.
- The disadvantage of an **RC** filter is the loss of dc voltage across each **R**. Because of this, the **RC** filter is suitable only for very light loads (small load current or large load resistance).

1.17.6 LC Filter

- When the load current is large, the **LC** filters of Figure-68 are an improvement over **RC** filters. Again, the idea is to drop the ripple across the series components, in this case, the inductors. By making X_L much greater than X_C , we can reduce the ripple to a very low level.

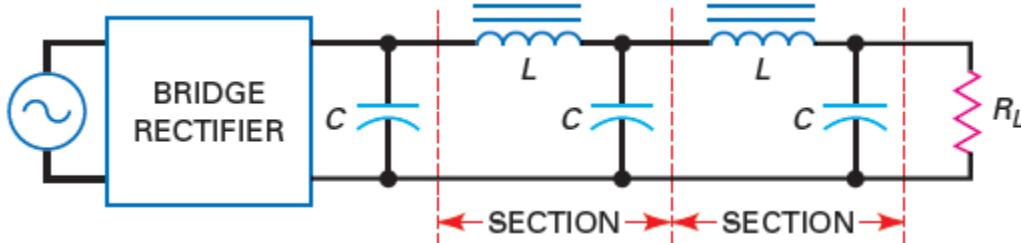


Figure-68 LC Filtering

- The dc voltage drop across the inductors is much smaller than it is across the resistors of **RC** sections because the winding resistance is smaller.
- The **LC** filter was very popular at one time. Now, it's becoming obsolete in typical power supplies because of the size and cost of inductors. For low-voltage power supplies, the **LC** filter has been replaced by an integrated circuit (**IC**).
- This is a device that contains diodes, transistors, resistors, and other components in a miniaturized package to perform a specific function.
- Figure-69 illustrates the idea. An IC voltage regulator, one type of integrated circuit, is between the filter capacitor and the load resistor. This device not only reduces the ripple, it also holds the output voltage constant.

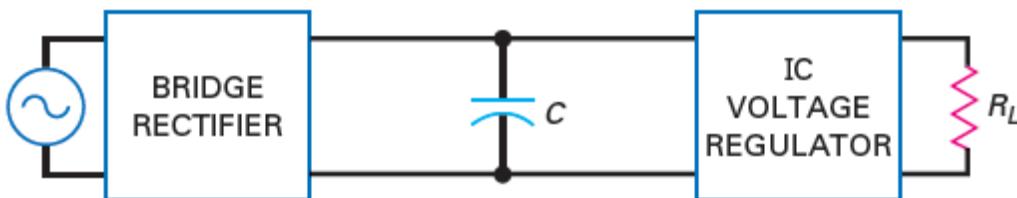


Figure-69 Voltage-regulator filtering

- Figure-70 shows an example of a three-terminal voltage regulator. The **LM7805** IC provides for a five-volt fixed **positive** output voltage, as long as the input voltage to the **IC** is at least 2 to 3 volts greater than the required output voltage.
- Other regulators in the **78XX** series can regulate a range of output values, such as 9 V, 12 V, and 15 V.

- The **79XX** series provides regulated **negative** output values. Because of their low cost, IC voltage regulators are now the standard method used for ripple reduction.

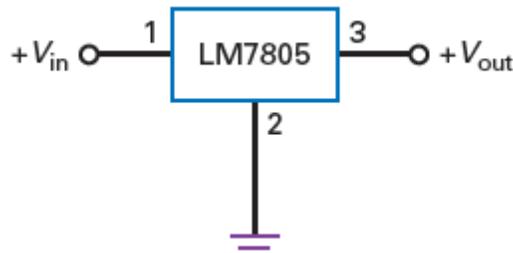


Figure-70 Three-terminal voltage regulator

1.18 Clippers and Limiters

- The diodes used in low-frequency power supplies are rectifier diodes. These diodes are optimized for use at **60 Hz** and have power ratings greater than **0.5 W**.
- The typical rectifier diode has a forward current rating in amperes. Except for power supplies, rectifier diodes have little use because most circuits inside electronics equipment are running at much higher frequencies.

1.18.1 Small-Signal Diodes

- In this section, we will be using small-signal diodes. These diodes are optimized for use at high frequencies and have power ratings less than **0.5 W**. The typical small-signal diode has a current rating in milli-amperes.
- It is this smaller and lighter construction that allows the diode to work at higher frequencies.

1.18.2 The Positive Clipper

- A clipper is a circuit that removes either positive or negative parts of a waveform. This kind of processing is useful for signal shaping, circuit protection, and communications.
- Figure-71a shows a positive clipper. The circuit removes all the positive parts of the input signal. This is why the output signal has only negative half-cycles.

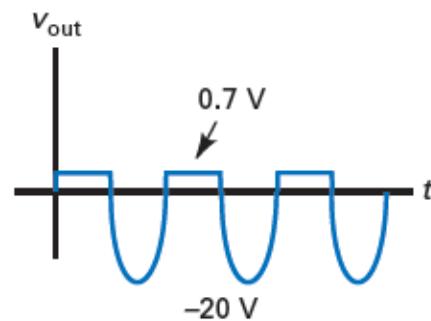
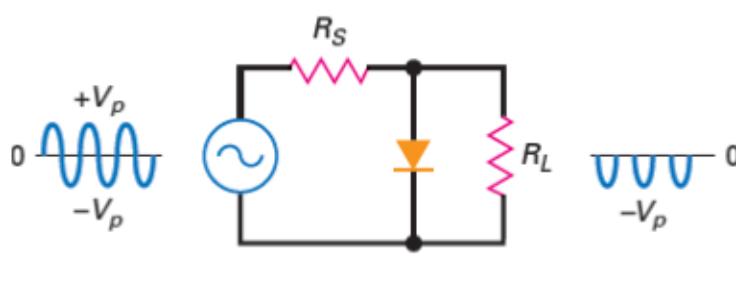


Figure-71 (a) Positive clipper; (b) output waveform

- Here is how the circuit works: During the positive half-cycle, the diode turns on and looks like a short across the output terminals. Ideally, the output voltage is zero. On the negative half-cycle, the diode is open. In this case, a negative half-cycle appears across the output.
- By deliberate design, the series resistor is much smaller than the load resistor. This is why the negative output peak is shown as **2V_p** in Figure-71a.

- To a second approximation, the diode voltage is 0.7 V when conducting. Therefore, the clipping level is not zero, but 0.7 V. For instance, if the input signal has a peak value of **20 V**, the output of the clipper will look like Figure-71b.

1.18.3 Defining Conditions

- Small-signal diodes have a smaller junction area than rectifier diodes because they are optimized to work at higher frequencies. As a result, they have more bulk resistance. The data sheet of a small-signal diode like the **1N914** lists a forward current of **10 mA** at **1 V**. Therefore, the bulk resistance is:

$$R_B = \frac{1 \text{ V} - 0.7 \text{ V}}{10 \text{ mA}} = 30\Omega$$

- Why is bulk resistance important? Because the clipper will not work properly unless the series resistance **RS** is much greater than the bulk resistance.
- Furthermore, the clipper won't work properly unless the series resistance **RS** is much smaller than the load resistance. For a clipper to work properly, we will use this definition:

Stiff clipper: $100R_B < R_S < 0.01R_L$ ----- (22)

- This says that the series resistance must be 100 times greater than the bulk resistance and 100 times smaller than the load resistance. When a clipper satisfies these conditions, we call it a stiff clipper.
- For instance, if the diode has a bulk resistance of 30 Ω, the series resistance should be at least 3 kΩ and the load resistance should be at least 300 kΩ.

1.18.4 The Negative Clipper

- If we reverse the polarity of the diode as shown in Figure-72a, we get a negative clipper. As you would expect, this removes the negative parts of the signal. Ideally, the output waveform has nothing but positive half-cycles.

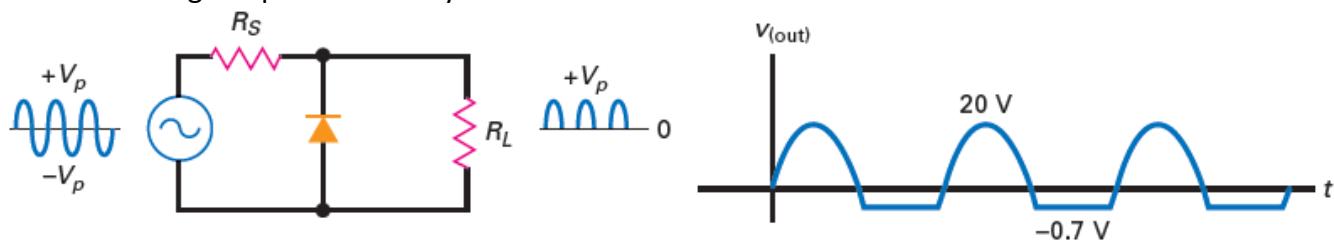


Figure-72 (a) Negative clipper; (b) output waveform

- The clipping is not perfect. Because of the diode offset voltage (another way of saying barrier potential), the clipping level is at **20.7 V**. If the input signal has a peak of 20 V, the output signal will look like Figure-72b.

1.18.5 The Limiter or Diode Clamp

- The clipper is useful for wave-shaping, but the same circuit can be used in a totally different way. Take a look at Figure-73a. The normal input to this circuit is a signal with a peak of only 15 mV. Therefore, the normal output is the same signal because neither diode is turned during the cycle. What good is the circuit if the diodes don't turn on? Whenever you have a sensitive circuit, one

that cannot have too much input, you can use a positive-negative limiter to protect its input, as shown in Figure-73b. If the input signal tries to rise above 0.7 V, the output is limited to 0.7 V.

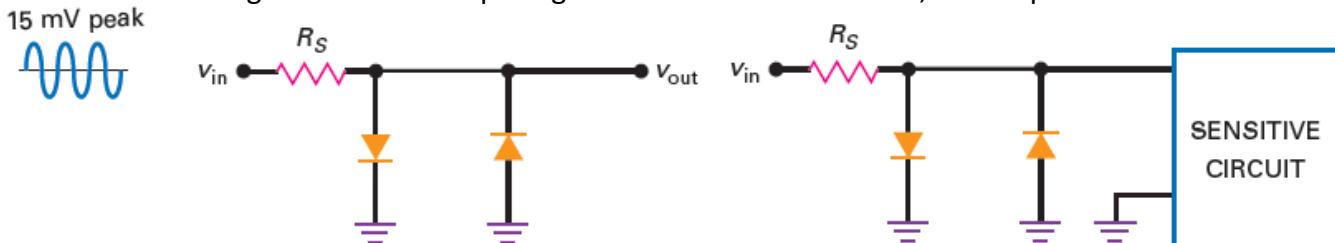


Figure-73 (a) Diode clamp; (b) protecting a sensitive circuit

- On the other hand, if the input signal tries to drop below 20.7 V, the output is limited to 20.7 V. In a circuit like this, normal operation means that the input signal is always smaller than 0.7 V in either polarity.
- A more familiar example of a sensitive circuit is a moving-coil meter. By including a limiter, we can protect the meter movement against excessive input voltage or current.
- The limiter of Figure-73a is also called a diode clamp. The term suggests clamping or limiting the voltage to a specified range. With a diode clamp, the diodes remain off during normal operation. The diodes conduct only when something is abnormal, when the signal is too large.

1.18.6 Biased Clippers

- The reference level (same as the clipping level) of a positive clipper is ideally zero, or 0.7 V to a second approximation. What can we do to change this reference level?
- In electronics, bias means applying an external voltage to change the reference level of a circuit. Figure-74a is an example of using bias to change the reference level of a positive clipper.
- By adding a dc voltage source in series with the diode, we can change the clipping level. The new V must be less than V_p for normal operation. With an ideal diode, conduction starts as soon as the input voltage is greater than V .
- To a second approximation, it starts when the input voltage is greater than $V + 0.7 \text{ V}$.
- Figure-74b shows how to bias a negative clipper. Notice that the diode and battery have been reversed. Because of this, the reference level changes to $-V - 0.7 \text{ V}$. The output waveform is negatively clipped at the bias level.

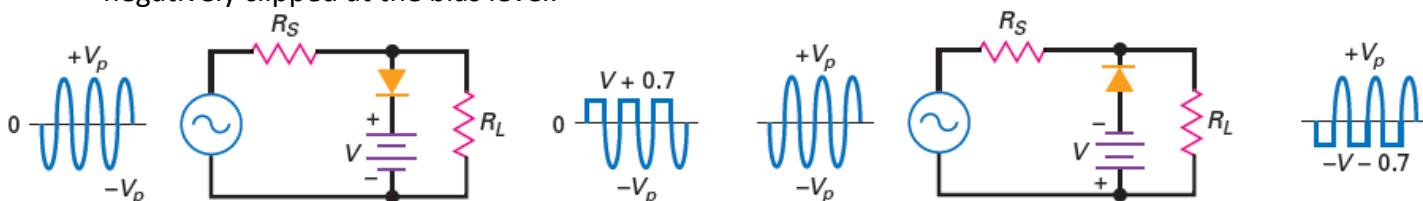


Figure-74 (a) Biased positive clipper; (b) biased negative clipper

1.18.7 Combination Clipper

- We can combine the two biased clippers as shown in Figure-75. Diode D_1 clips off positive parts above the positive bias level, and diode D_2 clips off parts below the negative bias level.
- When the input voltage is very large compared to the bias levels, the output signal is a square wave, as shown in Figure-75.

- This is another example of the signal shaping that is possible with clippers.

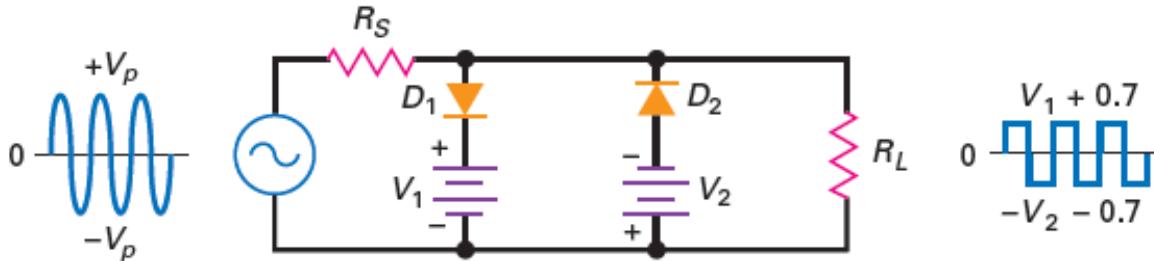


Figure-75 Biased positive-negative clipper

1.18.8 Variations

- Using batteries to set the clipping level is impractical. One approach is to add more silicon diodes because each produces a bias of 0.7 V. For instance, Figure-76a shows three diodes in a positive clipper.
- Since each diode has an offset of around 0.7 V, the three diodes produce a clipping level of approximately +2.1 V. The application does not have to be a clipper (wave-shaping). We can use the same circuit as a diode clamp (limiting) to protect a sensitive circuit that cannot tolerate more than a 2.1 V input.
- Figure-76b shows another way to bias a clipper without batteries.

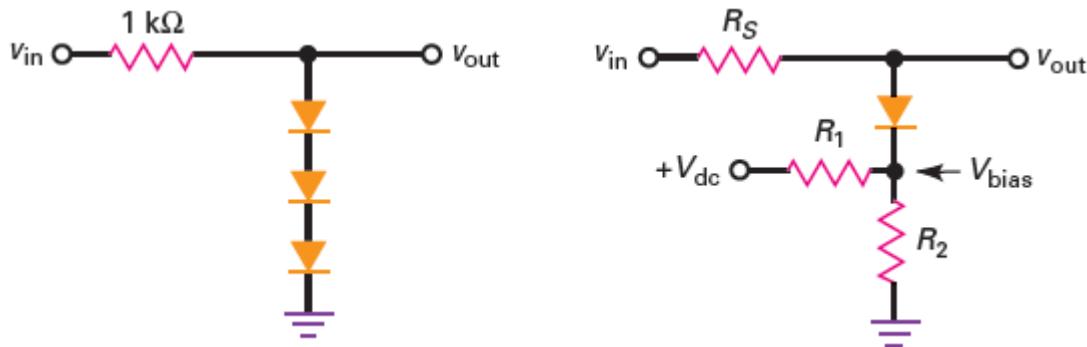


Figure-76 (a) Clipper using three-diode off set; (b) Voltage divider biases clipper

- This time, we are using a voltage divider (R_1 and R_2) to set the bias level. The bias level is given by:

$$V_{bias} = \frac{R_2}{R_1+R_2} V_{dc} \quad \dots \dots \dots (23)$$

- In this case, the output voltage is clipped or limited when the input is greater than $V_{bias} + 0.7$ V.
- Figure-77 a shows a biased diode clamp. It can be used to protect sensitive circuits from excessive input voltages. The bias level is shown as +5 V.
- It can be any bias level you want it to be. With a circuit like this, a destructively large voltage of +100 V never reaches the load because the diode limits the output voltage to a maximum value of +5.7 V.
- Sometimes a variation like Figure-77b is used to remove the offset of the limiting diode D_1 . Here is the idea: Diode D_2 is biased slightly into forward conduction so that it has approximately 0.7 V across it.

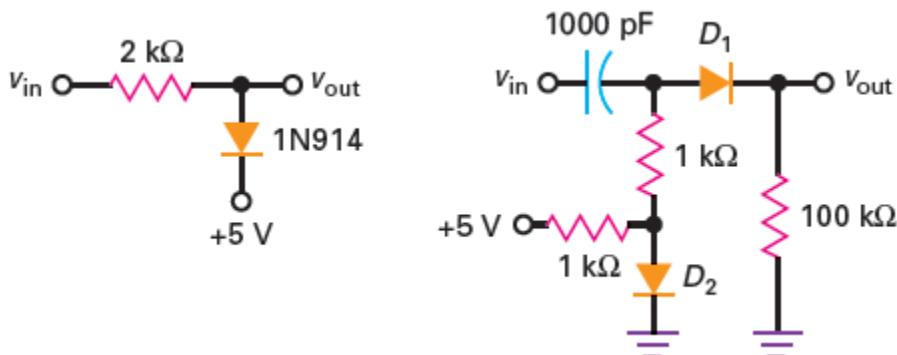


Figure-77 (a) diode clamp protects above 5.7 V; (b) diode D_2 biases D_1 to remove off set voltage

- This 0.7 V is applied to $1\text{ k}\Omega$ in series with D_1 and $100\text{ k}\Omega$. This means that diode D_1 is on the verge of conduction. Therefore, when a signal comes in, diode D_1 conducts near 0 V.

1.19 Clampers

- The diode clamp, which was discussed in the preceding section, protects sensitive circuits. The clamper is different, so don't confuse the similar-sounding names. A clamper adds a dc voltage to the signal.

1.19.1 Positive Clamper

- Figure-78a shows the basic idea for a positive clamper. When a positive clamper has a sine-wave input, it adds a positive dc voltage to the sine wave.
- Stated another way, the positive clamper shifts the ac reference level (normally zero) up to a dc level.

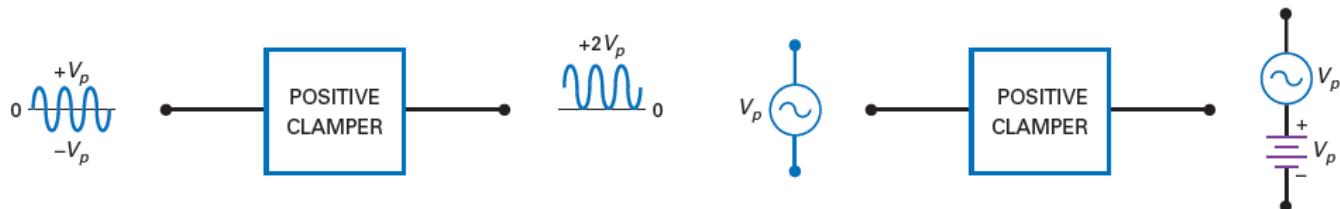


Figure-78 (a) Positive clamper shifts waveform upward; (b) positive clamper adds a dc component to signal

- The effect is to have an ac voltage centered on a dc level. This means that each point on the sine wave is shifted upward, as shown on the output wave.
- Figure-78b shows an equivalent way of visualizing the effect of a positive clamper. An ac source drives the input side of the clamper. The Thevenin voltage of the clamper output is the superposition of a dc source and an ac source.
- The ac signal has a dc voltage of V_p added to it. This is why the entire sine wave of Figure-78a has shifted upward so that it has a positive peak of $2V_p$ and a negative peak of zero.
- Figure-79a is a positive clamper. Ideally, here is how it works. The capacitor is initially uncharged. On the first negative half-cycle of input voltage, the diode turns on (Figure-79b). At the negative peak of the ac source, the capacitor has fully charged and its voltage is V_p with the polarity shown.
- Slightly beyond the negative peak, the diode shuts off (Figure-79c). The RLC time constant is deliberately made much larger than the period T of the signal.

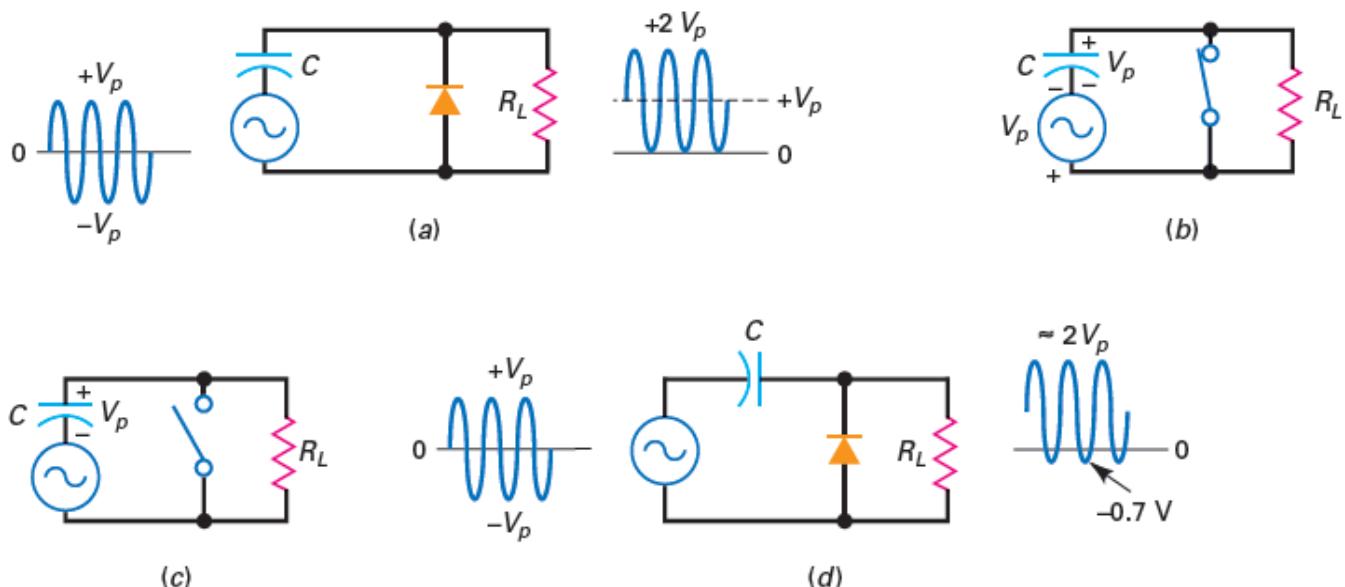


Figure-79 (a) Ideal positive clamper; (b) at the positive peak (c) beyond the positive peak; (d) clamper is not quite perfect

- We will define much larger as at least 100 times greater:

$$\text{Stiff clamper: } R_L C > 100T \quad (24)$$

- For this reason, the capacitor remains almost fully charged during the off time of the diode. To a first approximation, the capacitor acts like a battery of Vp volts.
- This is why the output voltage in Figure-79a is a positively clamped signal. Any clamper that satisfies Eq. (24) is called a stiff clamper.
- The idea is similar to the way **a half-wave rectifier with a capacitor-input filter works**. The first quarter-cycle charges the capacitor fully. Then, the capacitor retains almost all of its charge during subsequent cycles. The small charge that is lost between cycles is replaced by diode conduction.
- In Figure-79c, the charged capacitor looks like a battery with a voltage of Vp . This is the dc voltage that is being added to the signal. After the first quarter cycle, the output voltage is a positively clamped sine wave with a reference level of zero; that is, it sits on a level of **0 V**.
- Figure-79d shows the circuit as it is usually drawn. Since the diode drops 0.7 V when conducting, the capacitor voltage does not quite reach Vp . For this reason, the clamping is not perfect, and the negative peaks have a reference level of **-0.7 V**.

1.19.2 Negative Clamper

- What happens if we turn the diode in Figure-79d around? We get the negative clamper of Figure-80. As you can see, the capacitor voltage reverses, and the circuit becomes a negative clamper.
- Again, the clamping is less than perfect because the positive peaks have a reference level of **0.7V** instead of **0 V**. As a memory aid, notice that the diode points in the direction of shift.
- In Figure-80, the diode points downward, the same direction as the shift of the sine wave. This tells you that it's a negative clamper. In Figure-79a, the diode points up, the waveform shifts up, and you have positive clamper.

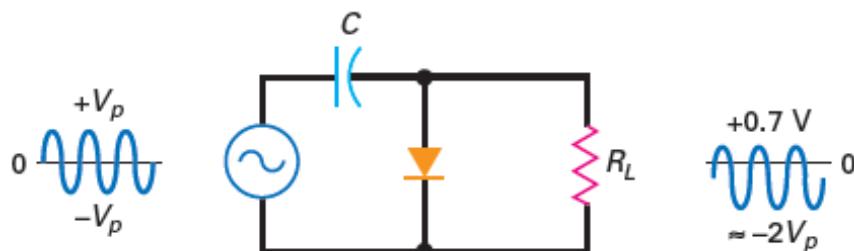


Figure-80 Negative clamper

- Both positive and negative clampers are widely used. For instance, television receivers use a clamper to change the reference level of video signals. Clampers are also used in radar and communication circuits.

1.19.3 Peak-to-Peak Detector

- A half-wave rectifier with a capacitor-input filter produces a dc output voltage approximately equal to the peak of the input signal. When the same circuit uses a small-signal diode, it is called a peak detector.
- Typically, peak detectors operate at frequencies that are much higher than 60 Hz. The output of a peak detector is useful in measurements, signal processing, and communications.
- If you cascade a clamper and a peak detector, you get a peak-to-peak detector (see Figure-81). As you can see, the output of a clamper is used as the input to a peak detector.

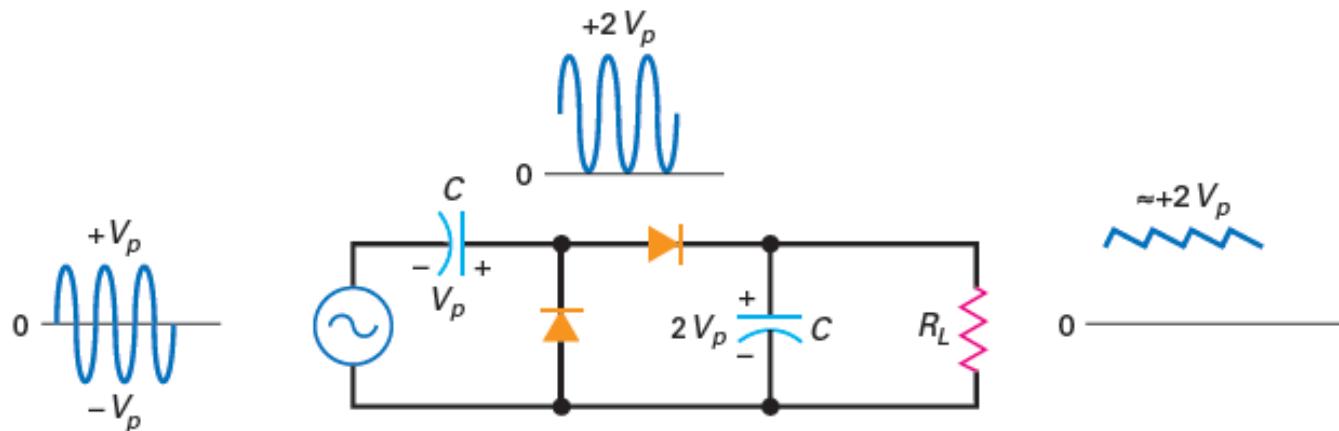


Figure-81 Peak-to-peak detector

- Since the sine wave is positively clamped, the input to the peak detector has a peak value of **2Vp**. This is why the output of the peak detector is a dc voltage equal to **2Vp**.
- As usual, the RC time constant must be much greater than the period of the signal. By satisfying this condition, you get good clamping action and good peak detection. The output ripple will therefore be small.
- One application is in measuring non-sinusoidal signals. An ordinary ac voltmeter is calibrated to read the rms value of an ac signal. If you try to measure a non-sinusoidal signal, you will get an incorrect reading with an ordinary ac voltmeter.
- However, if the output of a peak-to-peak detector is used as the input to a dc voltmeter, it will indicate the peak-to-peak voltage. If the non-sinusoidal signal swings from **-20 to +50 V**, the reading is **70 V**.

1.20 Voltage Multipliers

- A peak-to-peak detector uses small-signal diodes and operates at high frequencies. By using rectifier diodes and operating at 60 Hz, we can produce a new kind of power supply called a voltage doubler.

1.20.1 Voltage Doubler

- Figure-82 is a voltage doubler. The configuration is the same as a peak-to-peak detector, except that we use rectifier diodes and operate at 60 Hz.

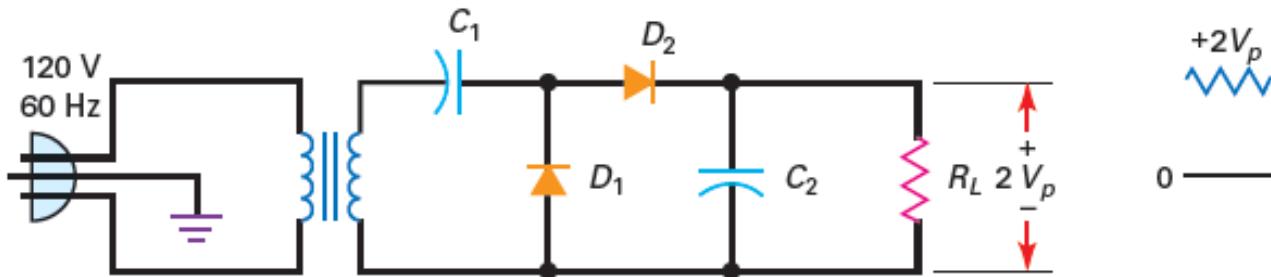


Figure-82 Voltage Doubler

- The clamper section adds a dc component to the secondary voltage. The peak detector then produces a dc output voltage that is two times the secondary voltage.
- Why bother using a voltage doubler when you can change the turn's ratio to get more output voltage?
- The answer is that you don't need to use a voltage doubler at lower voltages. The only time you run into a problem is when you are trying to produce very high dc output voltages.
- For instance, line voltage is **120 V** rms, or **170 V** peak. If you are trying to produce 3400 V dc, you will need to use a **1:20** step-up transformer.
- Here is where the problem comes in. Very high secondary voltages can be obtained only with bulky transformers. At some point, a designer may decide that it would be simpler to use a voltage doubler and a smaller transformer.

1.20.2 Voltage Tripler

- By connecting another section, we get the voltage Tripler of Figure-83. The first two sections act like a doubler.

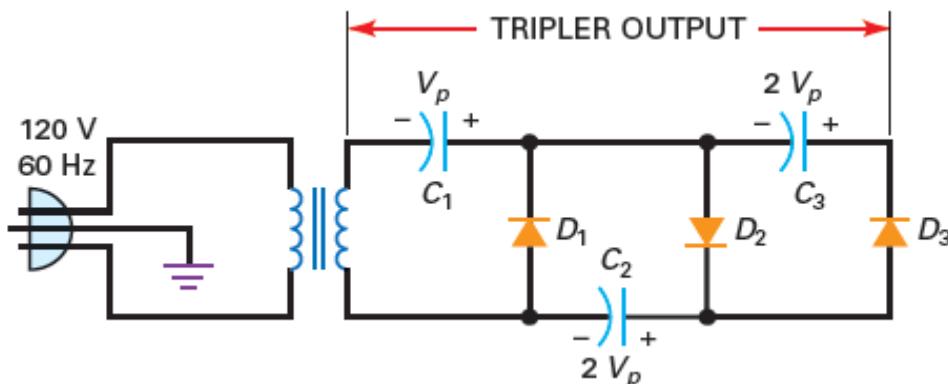


Figure-83 Voltage Tripler

- At the peak of the negative half-cycle, D_3 is forward biased. This charges C_3 to $2V_p$ with the polarity shown in Figure-83.
- The tripler output appears across C_1 and C_3 . The load resistance can be connected across the tripler output. As long as the time constant is long, the output equals approximately $3 V_p$.

1.20.3 Voltage Quadrupler

- Figure-84 is a voltage quadrupler with four sections in cascade (one after another). The first three sections are a tripler, and the fourth makes the overall circuit a quadrupler.
- The first capacitor charges to V_p . All others charge to $2V_p$. The quadrupler output is across the series connection of C_2 and C_4 . We can connect a load resistance across the quadrupler output to get an output of $4V_p$.

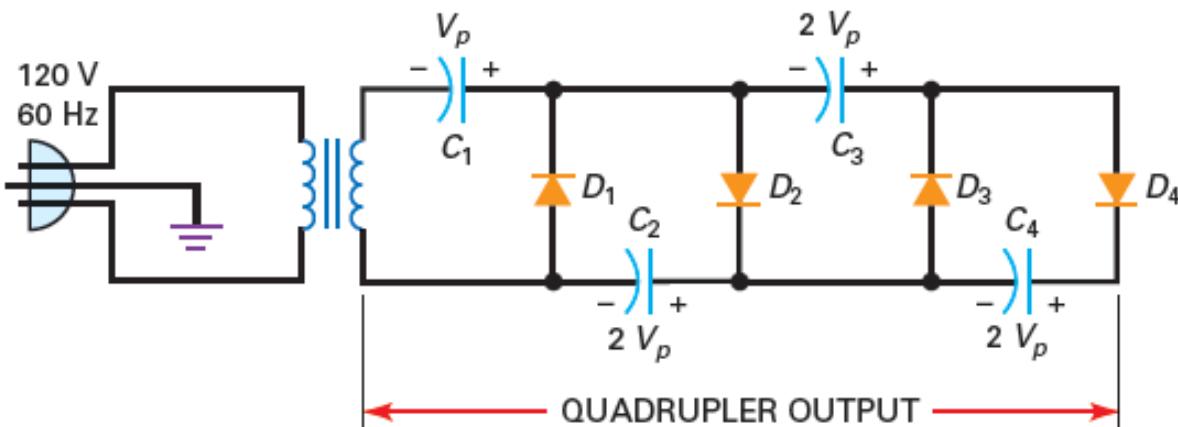


Figure-84 Voltage Quadrupler

- Theoretically, we can add sections indefinitely, but the ripple gets much worse with each new section.
- Increased ripple is another reason why voltage multipliers (doublers, triplers, and quadruplers) are not used in low-voltage power supplies.
- As stated earlier, voltage multipliers are almost always used to produce high voltages, well into the hundreds or thousands of volts. Voltage multipliers are the natural choice for high-voltage and low-current devices like the cathode-ray tube (CRT) used in television receivers, oscilloscopes, and computer monitors.

1.20.4 Variations

- All of the voltage multipliers shown in Figures 82, 83 and 84 use load resistances that are floating. This means that neither end of the load is grounded.
- Figures-85a, b, and c show variations of the voltage multipliers. Figure-85a merely adds grounds to Figure-82.
- On the other hand, Figures-85b and c are redesigns of the tripler (Figure-83) and quadrupler (figure-84). In some applications, you may see floating-load designs used (such as in the CRT); in others, you may see the grounded-load designs used.

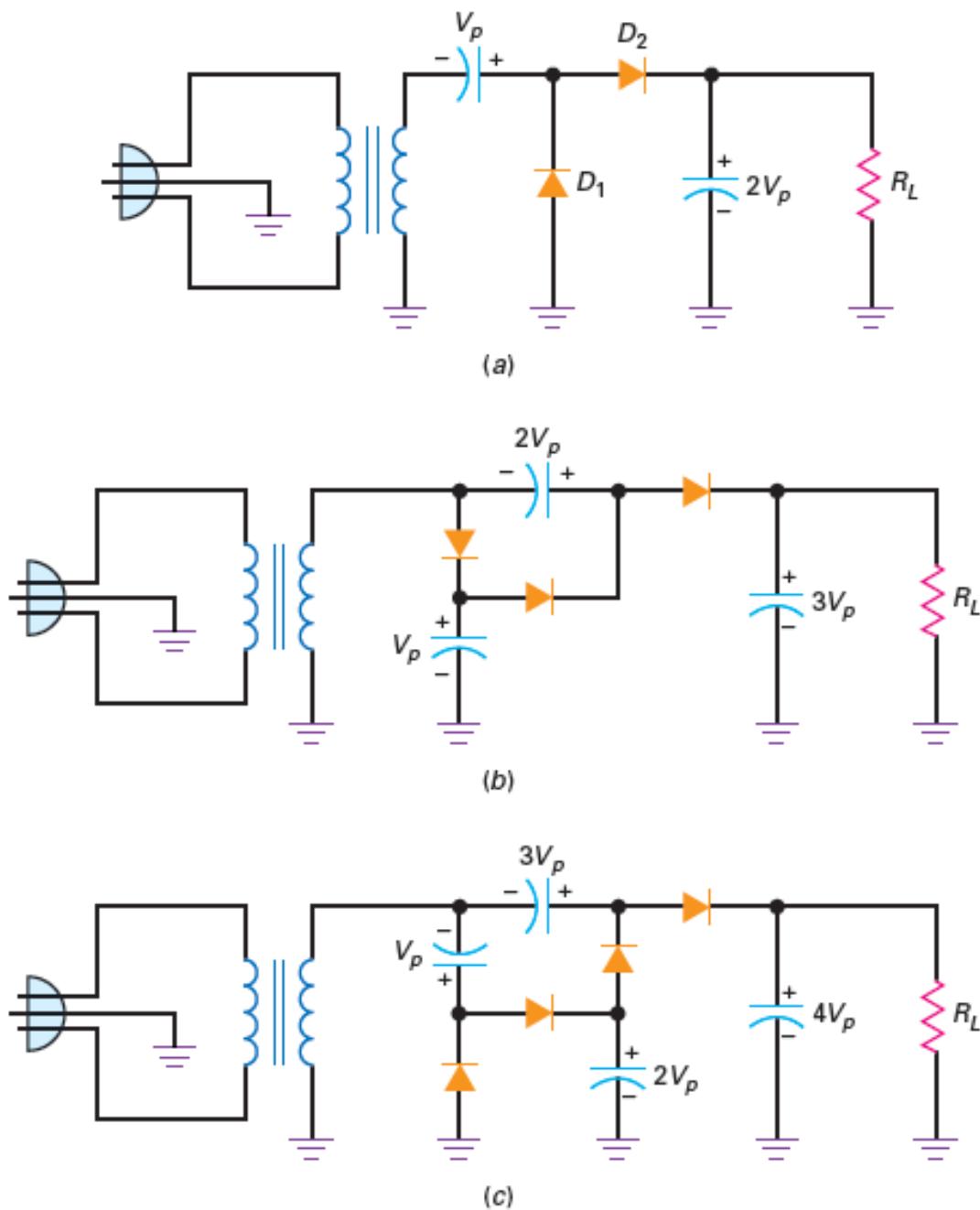


Figure-85 Voltage multipliers with grounded loads (a) Doubler; (b) tripler; (c) quadrupler

1.20.5 Full-Wave Voltage Doubler

- Figure-86 shows a full-wave voltage doubler. On the positive half-cycle of the source, the upper capacitor charges to the peak voltage with the polarity shown. On the next half-cycle, the lower capacitor charges to the peak voltage with the indicated polarity.
- For a light load, the final output voltage is approximately $2V_p$. The voltage multipliers discussed earlier are half-wave designs; that is, the output ripple frequency is 60 Hz.

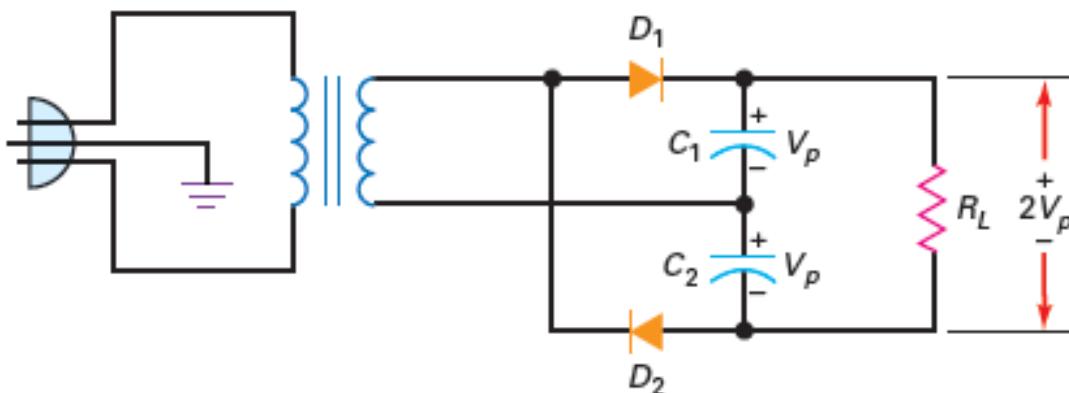


Figure-86 full-wave doubler

- On the other hand, the circuit of Figure-86 is called a full-wave voltage doubler because one of the output capacitors is being charged during each half-cycle. Because of this, the output ripple is 120 Hz.
- This ripple frequency is an advantage because it is easier to filter.
- Another advantage of the full-wave doubler is that the **PIV** rating of the diodes need only be greater than **Vp**.

1.21 Question Bank

- 1) Explain following terms:
 - a. Unbiased Diode
 - b. The Depletion Layer
 - c. Barrier Potential

2) Explain V-I characteristic of P N junction. (Most IMP)

OR

Explain V-I characteristic of normal rectifier diode. (Most IMP)

OR

Explain V-I characteristic of Avalanche diode. (Most IMP)

- 3) Describe first (ideal), second & third approximations of diode.
- 4) Describe how to troubleshoot diode with the help of multimeter.
- 5) Write a short note on Surface Mount Diodes.
- 6) Describe the circuit that produce half output with circuit diagram, waveforms and required derivations.

OR

Explain half wave rectifier with circuit diagram, waveforms and required derivations.

- 7) Describe the circuit that uses center tap transformer for rectification with circuit diagram, waveforms and required derivations.

OR

Explain full wave rectifier with center tap transformer using circuit diagram, waveforms and required derivations.

OR

Describe the circuit that uses two diodes for full wave rectification with circuit diagram, waveforms and required derivations.

- 8) **Describe the circuit that suits best for rectification with circuit diagram, waveforms and required derivations. (Most IMP)**

OR

Explain bridge rectifier using circuit diagram, waveforms and required derivations. (Most IMP)

OR

Describe the circuit that uses four diodes for full wave rectification with circuit diagram, waveforms and required derivations. (Most IMP)

- 9) Describe choke and capacitor input filter with its advantages and disadvantages.

- 10) Explain all steps for design of unregulated DC power supply.

- 11) **Explain all types (biased/unbiased) of clipper/limiter circuits with appropriate waveforms.(Most IMP)**

- 12) Explain diode clamp circuits used for protection purpose.

- 13) Describe all types of clamper circuits.

- 14) Explain voltage multiplier circuits in detail.

Unit-2
Bipolar Junction Transistor & it's Biasing

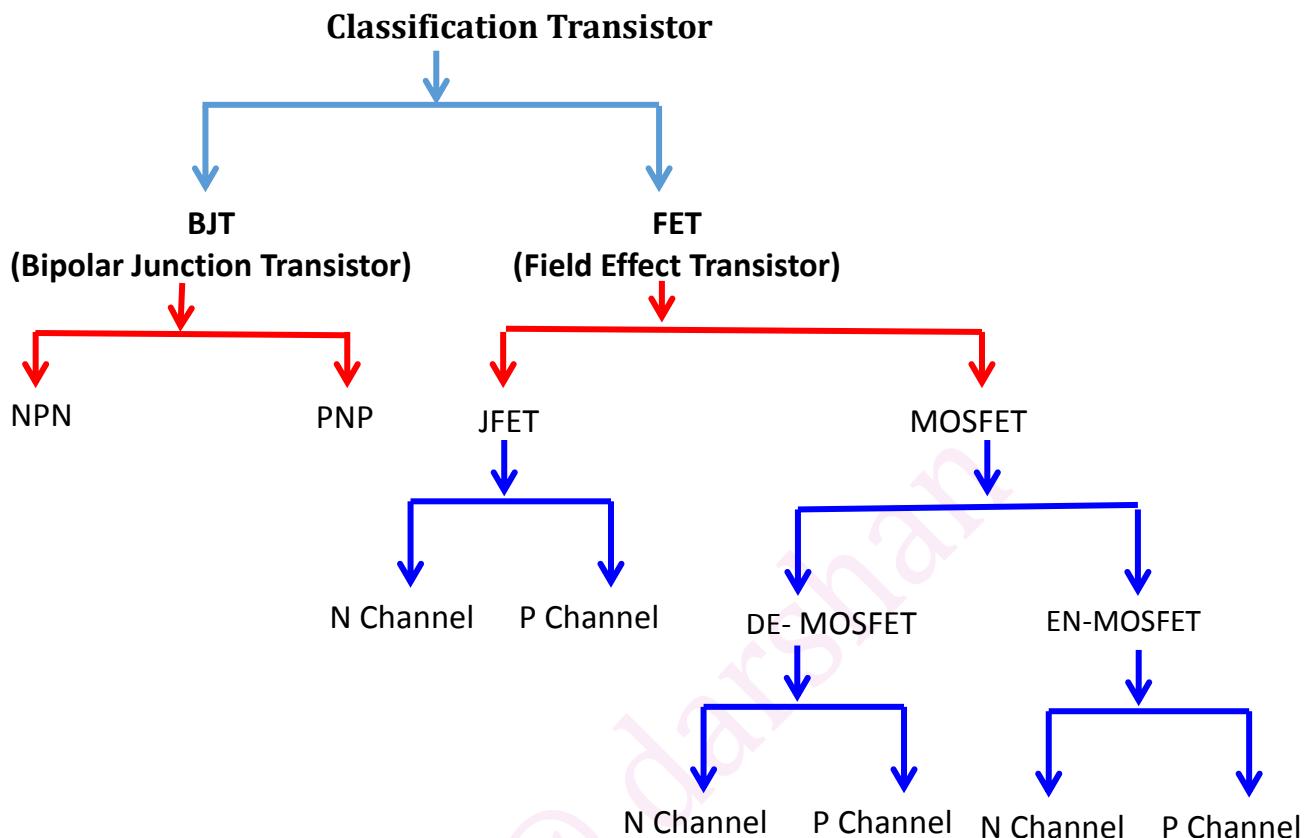
Basic Electronics

(3110016)

2nd Semester
Computer/Electrical Engineering

2.1 Classification of Transistor

Transistor can be classified as follow in different ways.



2.2 Construction of Bipolar Junction Transistor (BJT)

BJT is introduced in 1948 by Shockley, BJT is an electronic component mainly used for **switching** and **amplification** purpose.

BJT is called **bipolar** because the main flow of electrons through them takes place in two types of semiconductor material P type and N type, as the main current goes from emitter to collector (or vice versa). In other words, two types of charge carriers *electrons* and *holes* comprise this main current through the transistor so it is called bipolar.

Transistor implies *transfer of resistance* because it transfers current from low resistance input path to high resistance output path.

BJT is called a **current controlled device** where small current at the base side is used to control the large current at other terminals.

BJT comes in two types called

- NPN transistor and
- PNP transistor

This transistor comes with two PN junctions.

- PN junction exists between emitter and base is called **emitter-base junction**
- PN junction exists between collector and base is called **collector-base junction**.

It is composed of three terminals called Emitter (E), Base (B) and Collector(C)

All three terminals of the BJT are different in terms of their doping concentrations.

Emitter:

- *It is heavily doped*
- *Moderate in size*
- *It emits/injects charge carriers into base for conduction of current*

Base:

- *It is lightly doped*
- *Small/Thin in size*
- *It passes most of charge carrier to collector. It provides channel/path to charge carrier between emitter & collector*

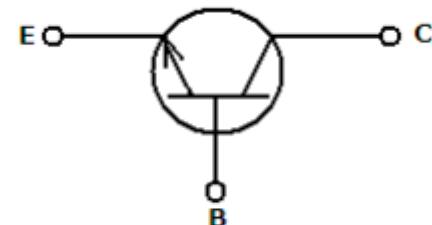
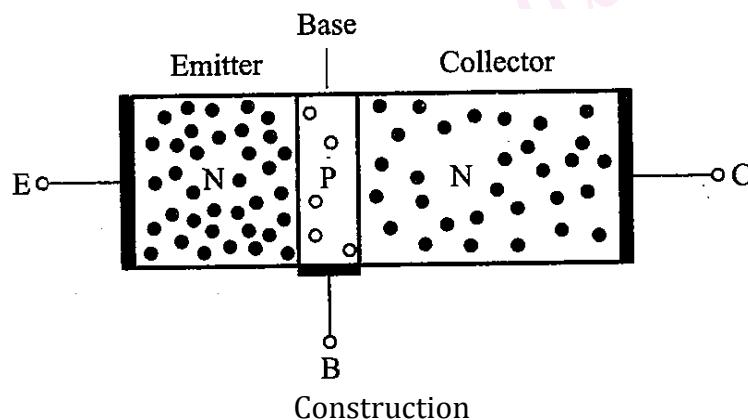
Collector:

- *It is moderately doped*
- *Large in size*
- *It collects charge carriers from base which has been emitted by emitter.*

Transistor Construction:

(1) NPN Transistor:

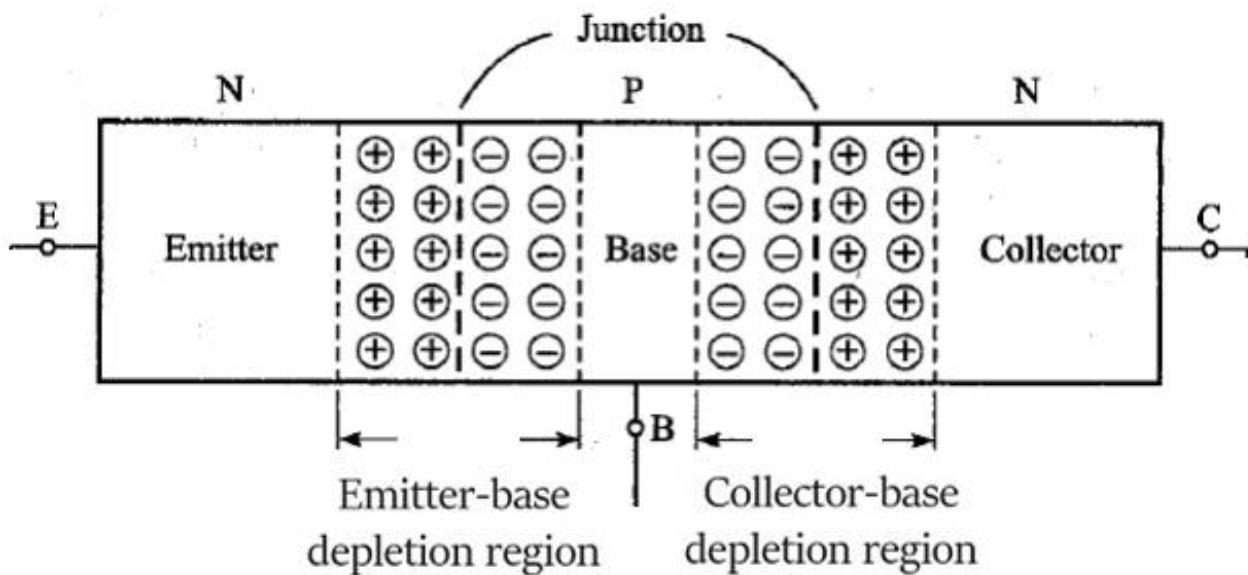
When single p-type semiconductor layer is sandwiched between two n-type semiconductor layers, an NPN transistor is formed.



Unbiased NPN transistor:

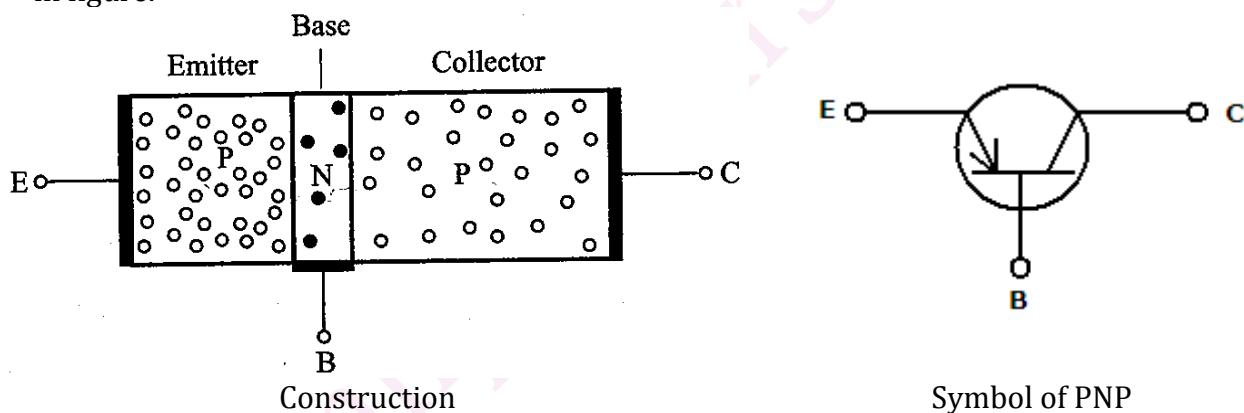
When no voltage is applied to a transistor, it is said to be an unbiased transistor. At the left side n-region (emitter) and right side n-region (collector), free electrons are the majority carriers and holes are the minority carriers whereas in p-region (base), holes are the majority carriers and free electrons are the minority carriers.

The free electrons in the n regions will spread in all directions. Some of the free electrons from the n region will diffuse across the junction and recombine with the holes in the p region. The result is two depletion layers, as shown in Figure.



(2) PNP Transistor:

When single n-type semiconductor layer is sandwiched between two p-type semiconductor layers, an PNP transistor is formed. Construction and symbol of PNP transistor is as shown in figure.

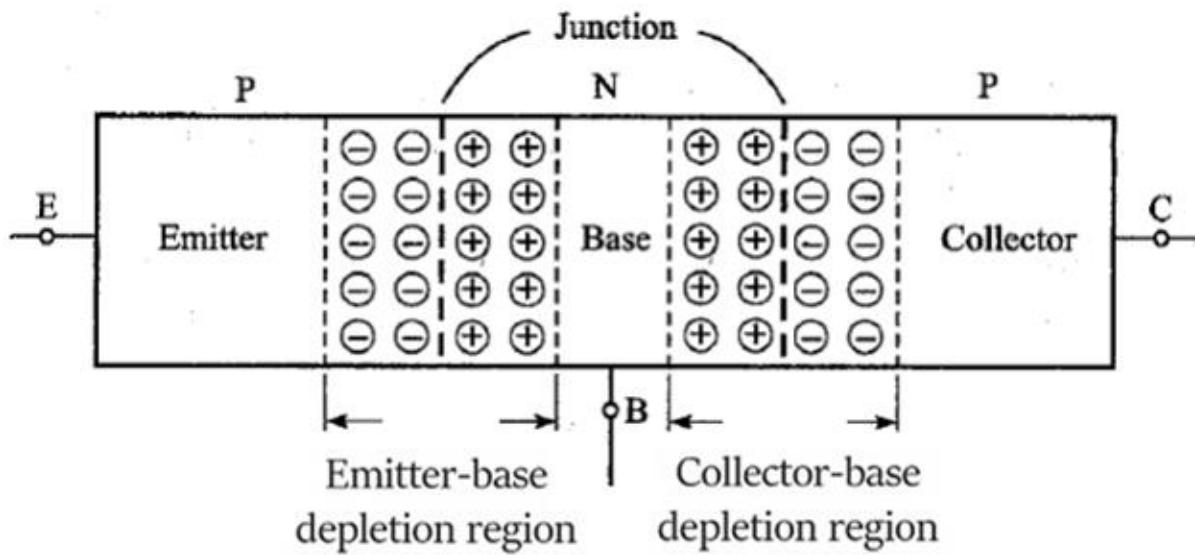


Unbiased PNP transistor:

When no voltage is applied to a pnp transistor, it is said to be an unbiased pnp transistor. At the left side p-region (emitter) and right side p-region (collector), holes are the majority carriers and free electrons are the minority carriers whereas in n-region (base), free electrons are the majority carriers and holes are the minority carriers.

Therefore, the holes at the left side p-region (emitter) and right side p-region (collector) experience a repulsive force from each other. As a result, the holes at the left side and right side p-regions (emitter and collector) will move into the n-region (base).

During this process, the holes meet the free electrons in the n-region (base) and recombines with them. As a result, depletion region (positive and negative ions) is formed at the emitter to base junction and base to collector junction.



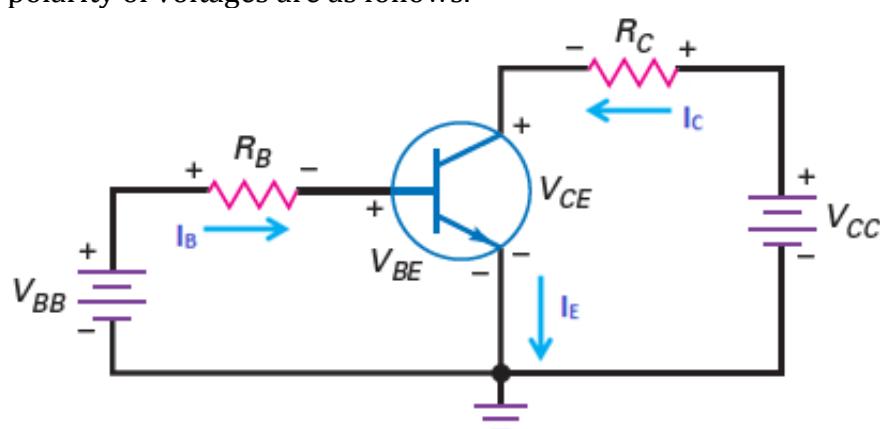
2.3 Operating region of Bipolar Junction Transistor (BJT)

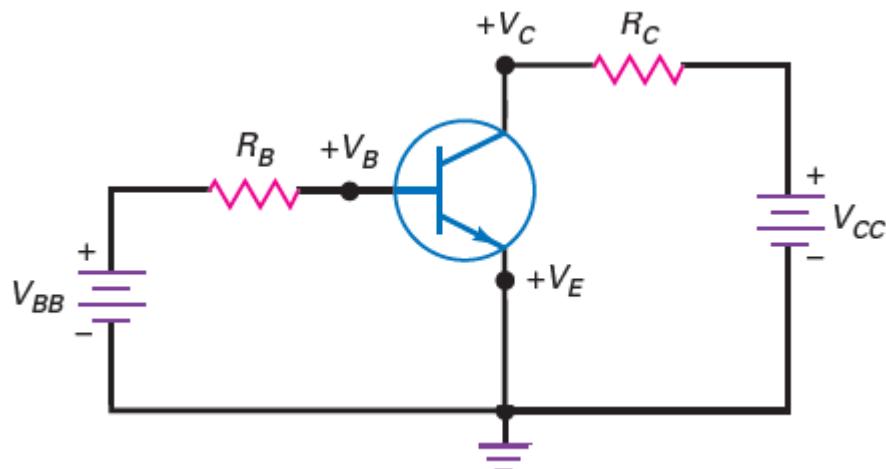
A transistor has two junctions, emitter-base junction and a collection-base junction. There are four possible ways of biasing these two junctions.

Condition		Emitter Base Junction (E-B Junction)	Collector base Junction (C-B Junction)	Operating Region
1	FR	Forward Biased	Reverse Biased	Active
2	FF	Forward Biased	Forward Biased	Saturation
3	RR	Reverse Biased	Reverse Biased	Cutoff
4	RF	Reverse Biased	Forward Biased	Inverted(Not Used)

2.4 Various Voltages and Currents in Bipolar Junction Transistor (BJT)

In transistor notation used for various voltages and currents as well as direction of various currents and polarity of voltages are as follows.



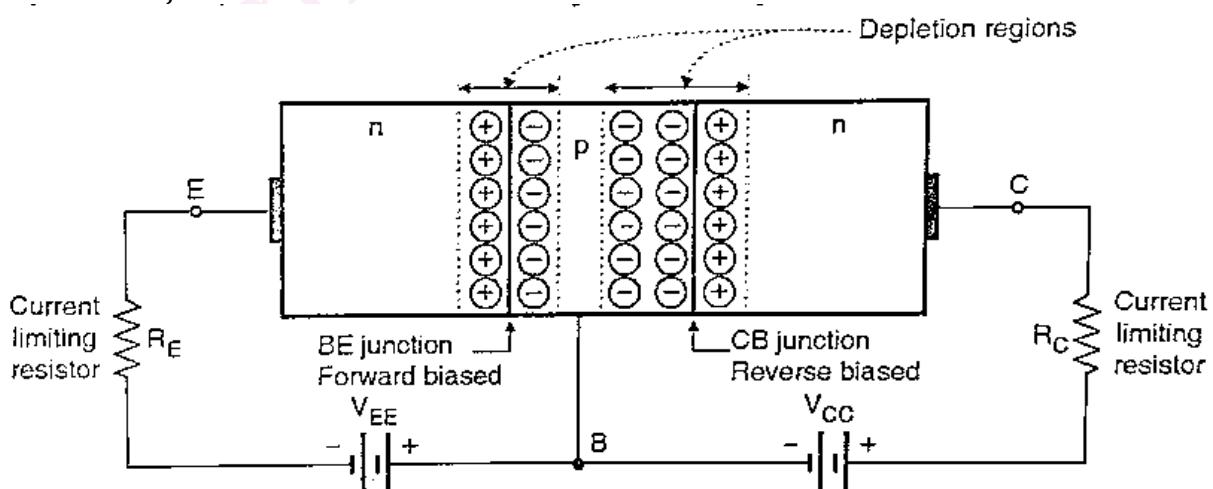


V_{CC}	Collector Battery Voltage	I_C	Collector Current
V_{EE}	Emitter Battery Voltage	I_E	Emitter Current
V_{BB}	Base Battery Voltage	I_B	Base Current
V_C	Collector Terminal Voltage	V_{BE}	Voltage across Emitter-Base Jn.
V_E	Emitter Terminal Voltage	V_{CB}	Voltage across Collector-Base Jn.
V_B	Base Terminal Voltage	V_{CE}	Voltage across Collector-Emitter Jn.

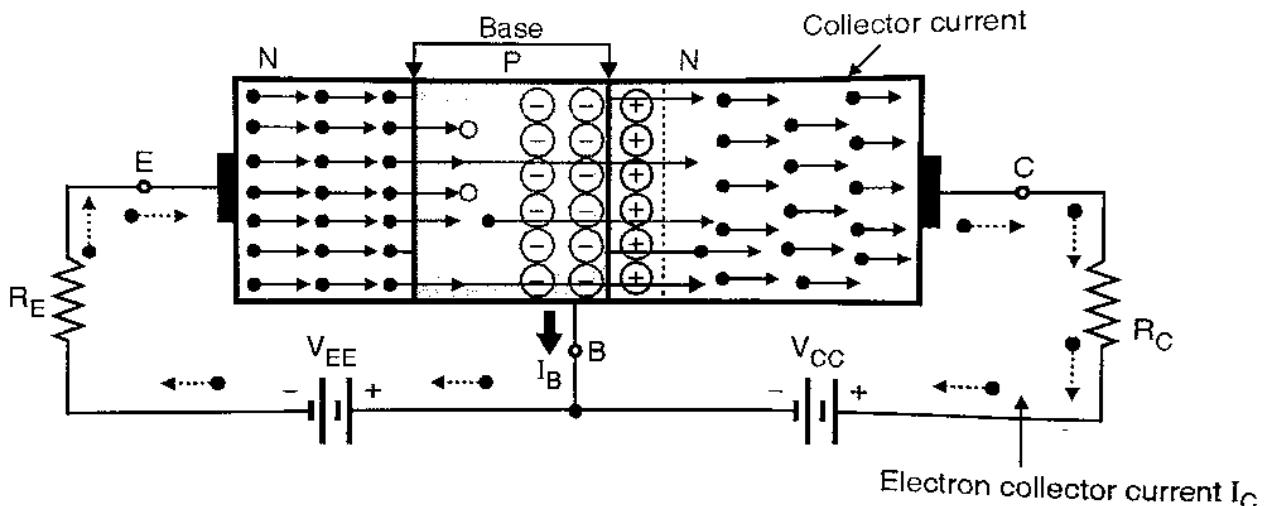
$$I_E = I_C + I_B$$

2.5 Working of Bipolar Junction Transistor (BJT) in Active region.

As shown in figure npn transistor is biased in Active region. **Emitter-Base junction is forward biased and collector base junction is reverse biased**. The left source V_{EE} forward-biases the emitter base junction and the right source V_{CC} reverse-biases the collector base junction.



The heavily doped emitter, emit or inject its free electrons into the base. The lightly doped base passes emitter-injected electrons on to the collector. The collector is so named because it collects or gathers most of the electrons from the base.



If V_{EE} is greater than the emitter-base barrier potential then emitter electrons will enter the base region, as shown in Figure. Theoretically, these free electrons can flow in either of two directions. Either they can flow through base and towards positive terminal of battery V_{EE} . Otherwise, the free electrons can flow into the collector.

But as the base is lightly doped and very thin, free electrons entered into base gets very less amount of time for recombination in the base region. For this reason almost all the emitter-injected electrons pass through the base to the collector. Only a few free electrons will recombine with holes in the lightly doped base and will flow through the base and toward the positive side of the V_{EE} supply.

Almost all the free electrons go into the collector, as shown in Figure. Once they are in the collector, they feel the attraction of the V_{CC} source voltage. Because of this, the free electrons flow through the collector and through R_C until they reach the positive terminal of the collector supply voltage.

Thus V_{EE} forward-biases the emitter diode, forcing the free electrons in emitter to enter the base. The thin and lightly doped base gives almost all these electrons enough time to diffuse into the collector. These electrons flow through the collector, through R_C , and into the positive terminal of the V_{CC} voltage source. Even though CB junction is reverse biased electron from emitter could able to reach to collector.

Emitter efficiency (emitter injection ratio):

It is defined as the ration of charge carriers injected by emitter into the base to total emitter current. It is denoted by symbol γ (gamma).

$$\gamma = \frac{\text{charge carrier injected by emitter at EB junction}}{\text{Total emitter current}} = \frac{I_{nE}}{I_{nE} + I_{pE}} = \frac{I_{nE}}{I_E}$$

For NPN transistor total emitter current is due to emitted electrons I_{nE} as well as due to minority charge carrier hole I_{pE} . Current due to minority charge carriers is very small. Typical value of γ is 0.995

Base Transportation factor β^* :

It is defined as the ratio of charge carriers reaching/arriving at collector to the number of emitted charge carriers. It is denoted by symbol β^* or β '(Beta).

$$\beta^* = \frac{\text{injected charge carriers reaching/arriving at collector}}{\text{charge carriers emitted by emitter}} = \frac{I_{nC}}{I_{nE}}$$

For NPN transistor charge carriers (electrons) emitted by emitter is I_{nE} and charge carriers (electrons) reaching at collector is I_{nC} . Typical value of β^* is 0.995.

Large signal current gain α^* :

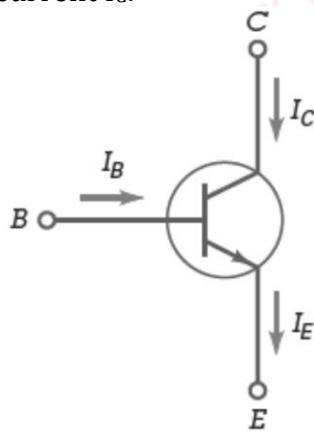
It is defined as the ratio of collector current increment to total emitter current. It is denoted by symbol α^* or α '(Alpha).

$$\alpha^* = \frac{\text{collector current increment}}{\text{total emitter current}} = \frac{I_C - I_{CBO}}{I_{nE} + I_{pE}} = \frac{I_{nC}}{I_E}$$

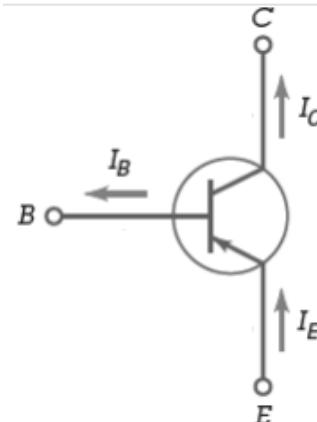
For NPN transistor total emitter current is due to emitted electrons I_{nE} as well as due to minority charge carrier hole I_{pE} . Increment in collector current is $I_C - I_{CBO}$, where I_{CBO} is collector to base leakage current when emitter is open (due to minority charge carrier in collector). Typical value of α^* is 0.9 to 0.995.

2.6 Different Current components in Transistor and their relationship:

There are three different currents in a transistor: emitter current I_E , base current I_B , and collector current I_C .



Direction of currents in NPN transistor



Direction of currents in PNP transistor

Because the emitter is the source of the electrons, it has the largest current. Since most of the emitter electrons flow to the collector, the collector current is almost as large as the emitter current. The base current is very small by comparison, often less than 1 percent of the collector current.

Relation of Currents:

As per Kirchhoff's current law. It says that the sum of all currents into a point or junction equals the sum of all currents out of the point or junction. When applied to a transistor, Kirchhoff's current law gives us this important relationship:

$$I_E = I_B + I_c$$

This says that the emitter current is the sum of the collector current and the base current. Since the base current is so small, the collector current approximately equals the emitter current.

$$I_c \approx I_E$$

and the base current is much smaller than the collector current:

$$I_B \ll I_c$$

Current Gain in transistor and it's relation:

Current Gain Alpha (α_{dc}) :

The current gain alpha dc (α_{dc}) is defined as the ratio of dc collector current to dc emitter current.

$$\alpha_{dc} = \frac{I_c}{I_E}$$

Since the collector current almost equals the emitter current, the dc alpha is slightly less than 1. For instance, in a low-power transistor, the dc alpha is typically greater than 0.99. Even in a high-power transistor, the dc alpha is typically greater than 0.95.

Current Gain Beta (β_{dc}) :

The current gain Beta dc (β_{dc}) is defined as the ratio of dc collector current to dc base current.

$$\beta_{dc} = \frac{I_c}{I_B}$$

The dc beta is also known as the current gain because a small base current controls a much larger collector current. The current gain is a major advantage of a transistor and has led to all kinds of applications.

For low-power transistors (under 1 W), the current gain is typically 100 to 300. High-power transistors (over 1 W) usually have current gains of 20 to 100.

Relation between current gain α_{dc} and β_{dc}

The emitter current equation is

$$I_E = I_B + I_c \quad \text{---- (1)}$$

Dividing equation (1) by I_c

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1 \quad \text{---- (2)}$$

$$\frac{1}{\alpha_{dc}} = \frac{1 + \beta_{dc}}{\beta_{dc}}$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} \quad \text{---- (3)}$$

Equation (3) indicates α_{dc} in terms of β_{dc}

Rearranging equation (2) again

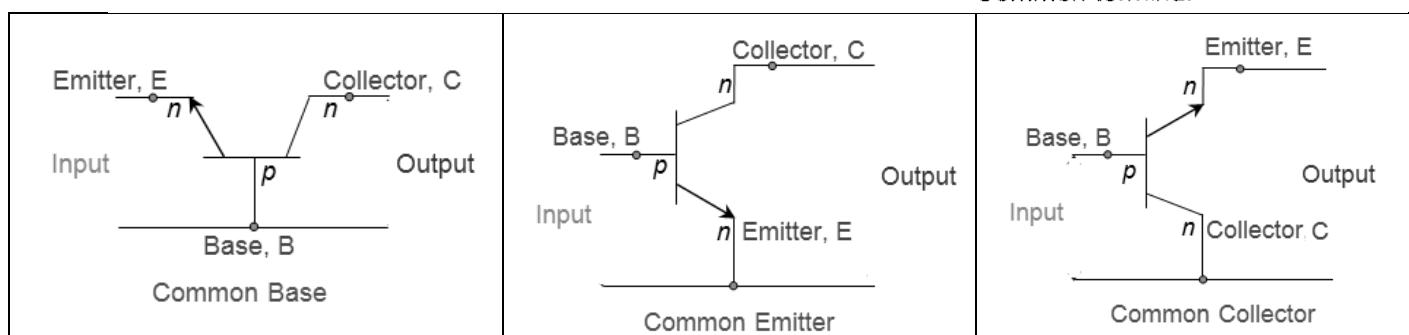
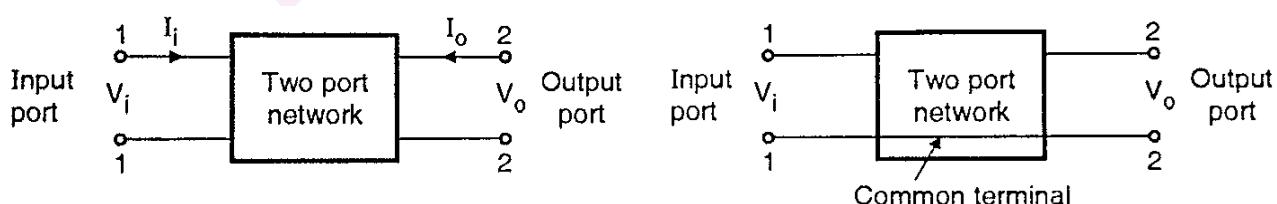
$$\frac{1}{\beta_{dc}} = \frac{1}{\alpha_{dc}} - 1$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} \quad \text{---- (4)}$$

Equation (4) indicates β_{dc} in terms of α_{dc}

2.7 Types of Transistor Configurations

Transistor has three terminals namely emitter (E), base (B), and collector (C). But to connect a transistor in the circuit, we need four terminals, two terminals for input and other two terminals for output. If one of the three terminals is used as common to both input and output then transistor can be considered as two port network.



When a transistor is to be connected in a circuit, one terminal is used as the input terminal, the other terminal is used as the output terminal and the third terminal is common to the input and output. That means here input is applied between the input terminal and common terminal, and the corresponding output is taken between the output terminal and common terminal.

Depending upon the terminal which is used as a common terminal to the input and output terminals, the transistor can be connected in the following three configurations. They are:

- (i) Common base (CB) configuration
- (ii) Common emitter (CE) configuration
- (iii) Common collector (CC) configuration

In every configuration, the base-emitter junction is always forward biased and the collector-base junction is always reverse biased to operate the transistor as a current amplifier.

Common base (CB) configuration

In common base configuration, emitter is the input terminal, collector is the output terminal, and base is the common terminal. The base terminal is grounded in the common base configuration. So the common base configuration is also known as grounded base configuration.

Common emitter (CE) configuration

In common emitter configuration, base is the input terminal, collector is the output terminal, and emitter is the common terminal. The emitter terminal is grounded in the common emitter configuration. So the common emitter configuration is also known as grounded emitter configuration.

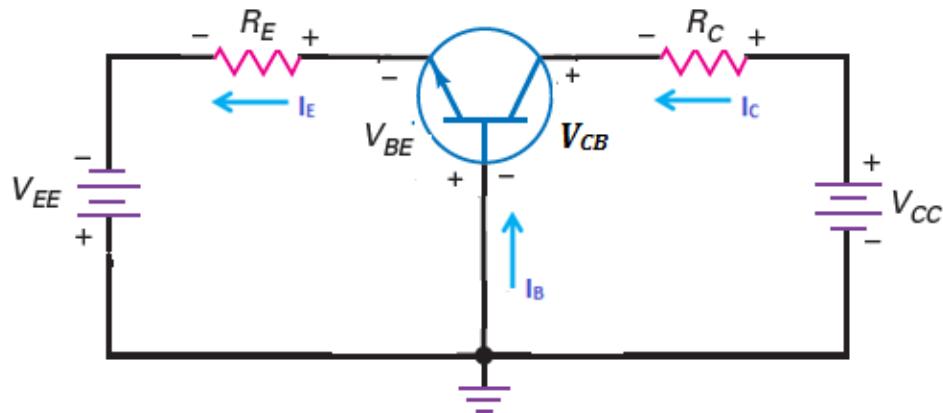
Common collector (CC) configuration

In common collector configuration, base is the input terminal, emitter is the output terminal, and collector is the common terminal. The collector terminal is grounded in the common collector configuration. So the common collector configuration is also known as grounded collector configuration

2.8 Common Base Configuration of Transistor (CB Configuration)

In common base configuration, emitter is the input terminal, collector is the output terminal, and base is the common terminal between input and output.

As shown in figure EB junction is forward biased and CB junction is reverse biased. To forward bias EB junction V_{EE} battery is connected and to reverse bias CB junction V_{CC} battery is connected as shown in figure. Resistance R_E and R_C are current limiting resistors.



Current Gain and different current components in CB configuration:

Current Gain α_{dc} :

It is defined as the ratio of output current I_C to Input current I_E . It is denoted by α_{dc} or α . It is represented by equation

$$\alpha_{dc} = \frac{I_{C(inj)}}{I_E} = \frac{I_C - I_{CBO}}{I_E} \quad \text{---- (1)}$$

In equation (1)

$I_{C(inj)}$ is injected charge carrier into the collector from emitter

I_{CBO} is reverse leakage current between collector to base when emitter is open. Which is very small. If we neglect I_{CBO} then α_{dc} is approximated to

$$\alpha_{dc} \cong \frac{I_C}{I_E} \quad \text{---- (2)}$$

Collector current I_C :

From equation (1), collector current can be written as

$$I_C = \alpha_{dc} I_E + I_{CBO} \quad \text{---- (3)}$$

as I_{CBO} is very small, If we neglect I_{CBO} then collector current I_C is approximated to

$$I_C \cong \alpha_{dc} I_E$$

Emitter current I_E :

Emitter current is sum of Base current I_B and collector current I_C

$$I_E = I_C + I_B \quad \text{---- (4)}$$

Base current I_B :

$$I_B = I_E - I_C \quad \text{---- (5)}$$

Putting the value of I_C in equation (5) from equation (3)

$$I_B = I_E - \alpha_{dc} I_E - I_{CBO}$$

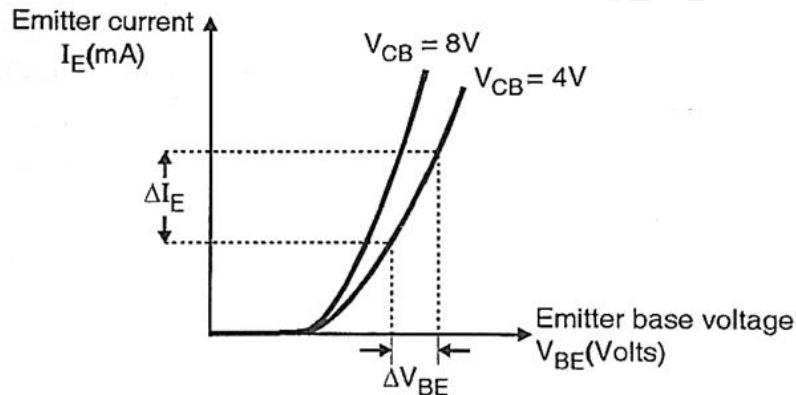
$$I_B = I_E(1 - \alpha_{dc}) - I_{CBO}$$

---- (6)

$$I_B \cong I_E(1 - \alpha_{dc})$$

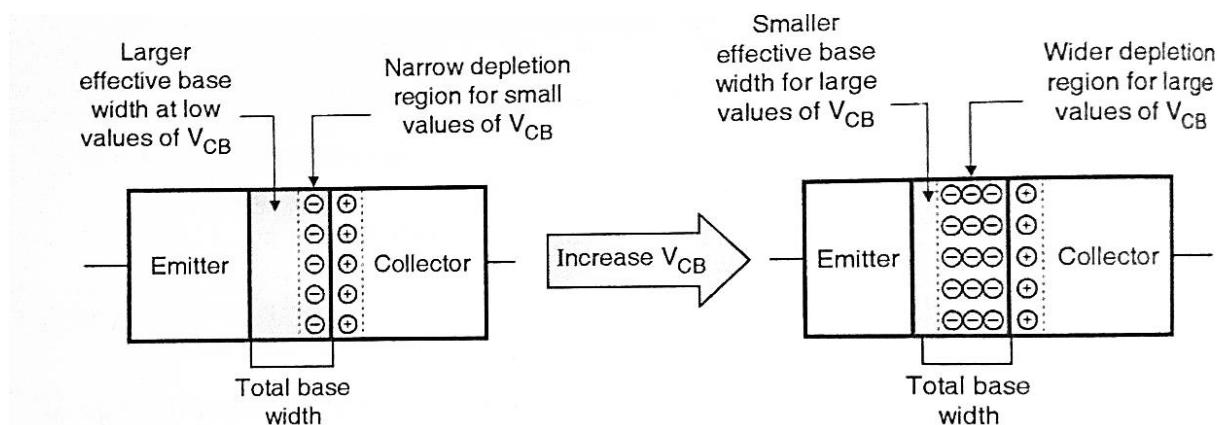
Input Characteristic of CB configuration:

Input characteristic is the relation between transistors input current I_E and input voltage V_{BE} , keeping the output voltage V_{CB} constant.



Base width modulation/Early effect:

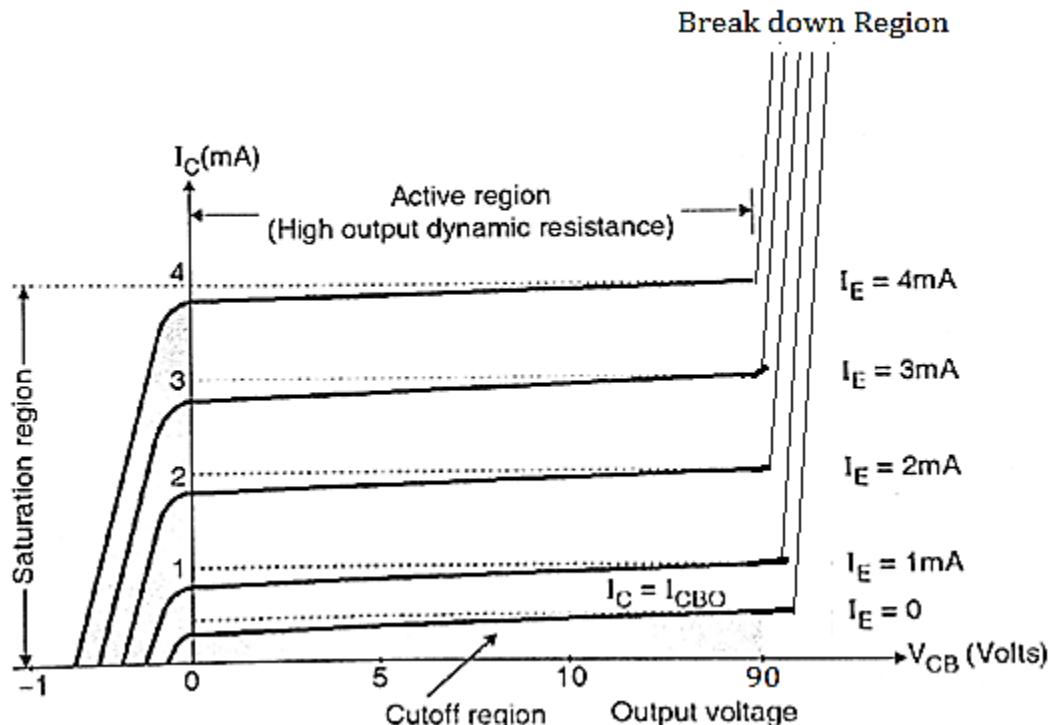
In CB configuration of transistor, if we increase V_{CB} , then depletion layer at CB junction will increase, which results in decrease in effective base width. Hence concentration gradient at EB junction will increase, which allows more electrons from emitter to diffuse into the base. So emitter current I_B will increase. Thus when collector base voltage V_{CB} is increases, emitter current I_E will also increases.



The change in effective base width due to change in V_{CB} is called Base width modulation or Early effect.

Output Characteristic of CB configuration:

Output characteristic is the relation between transistors output current I_C and output voltage V_{CB} , keeping the input current I_E constant.

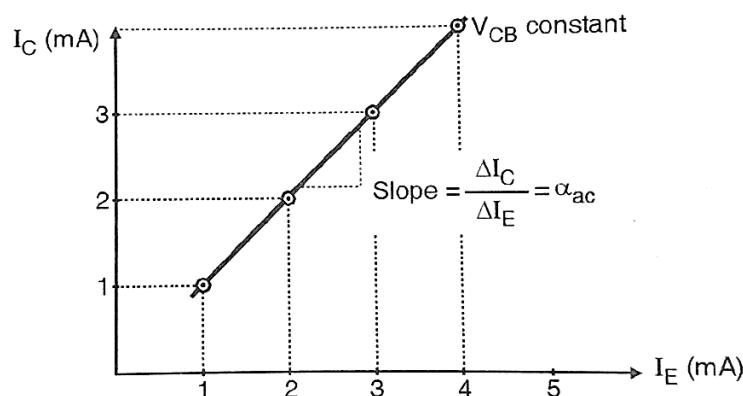


If an excessive reverse-bias voltage is applied to the collector-base junction, the device breakdown may occur.

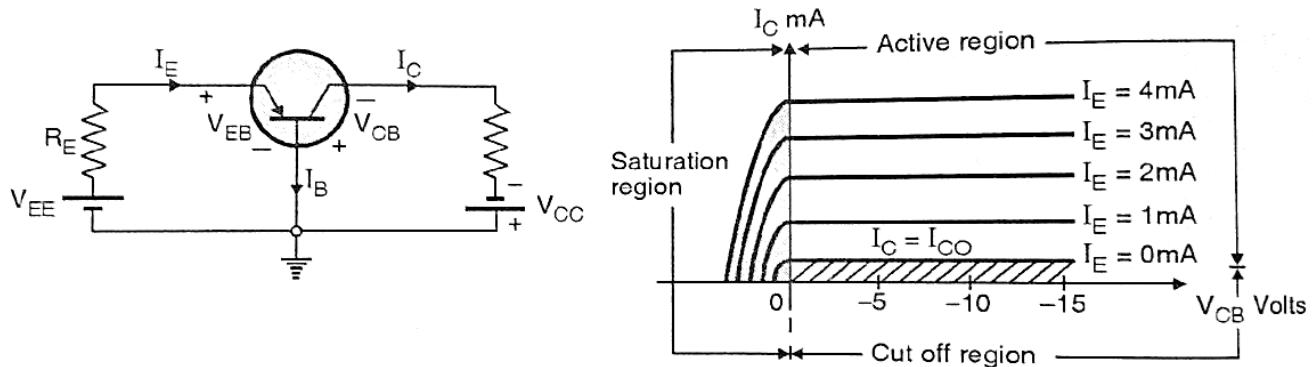
As reverse bias voltage V_{CB} is increases, collector-base depletion region also increases. If an excessive reverse-bias voltage is applied then collector-base depletion region penetrating into the base until it makes contact with emitter-base depletion region. This condition is known as *punch through* or *reach through* effect. A Very large currents can flow when it occurs and possible destroying the device.

Transfer Characteristic of CB configuration

Transfer characteristic is the relation between transistors output current I_C and input current I_E for constant V_{CB} voltage. It is linear as shown in figure.



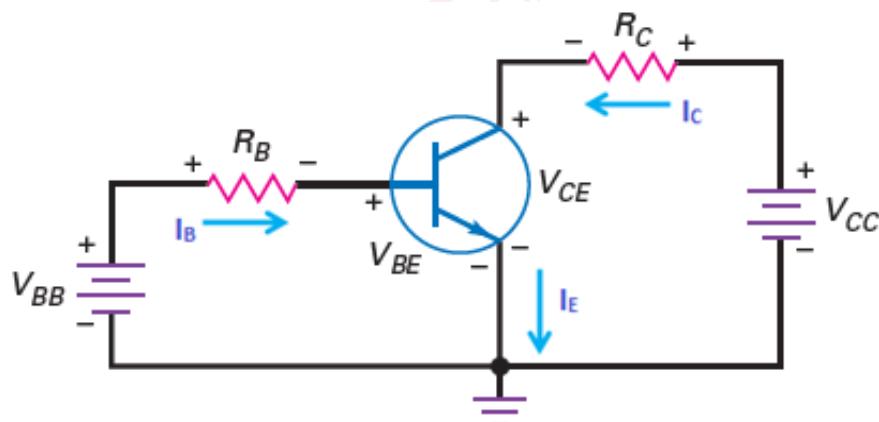
Circuit diagram and output characteristic of CB configuration using PNP transistor:



2.9 Common Emitter Configuration of Transistor (CE Configuration)

In common emitter configuration, base is the input terminal, collector is the output terminal, and emitter is the common terminal between input and output.

As shown in figure EB junction is forward biased and CB junction is reverse biased. To forward bias EB junction V_{BB} battery is connected and to reverse bias CB junction V_{CC} battery is connected as shown in figure. Resistance R_B and R_C are current limiting resistors.



Current Gain and different current components in CE configuration:

Current Gain β_{dc} :

It is defined as the ratio of output current I_C to Input current I_B . It is denoted by β_{dc} or β . It is represented by equation

$$\beta_{dc} = \frac{I_{C(inj)}}{I_B} = \frac{I_C - I_{CEO}}{I_B} \quad \text{-----(1)}$$

In equation (1)

$I_{C(inj)}$ is injected charge carrier into the collector from emitter

I_{CEO} is reverse leakage current between collector to emitter when base is open. Which is very small. If we neglect I_{CEO} then β_{dc} is approximated to

$$\beta_{dc} \cong \frac{I_C}{I_B}$$

---- (2)

Collector current I_C :

From equation (1), collector current can be written as

$$I_C = \beta_{dc} I_B + I_{CEO}$$

---- (3)

as I_{CEO} is very small, If we neglect I_{CEO} then collector current I_C is approximated to

$$I_C \cong \beta_{dc} I_B$$

Emitter current I_E :

Emitter current is sum of Base current I_B and collector current I_C

$$I_E = I_C + I_B \quad \text{---- (4)}$$

Putting the value of I_C in equation (4) from equation (3)

$$I_E = \beta_{dc} I_B + I_{CEO} + I_B$$

$$I_E = I_B(1 + \beta_{dc}) + I_{CEO}$$

---- (5)

$$I_E \cong I_B(1 + \beta_{dc})$$

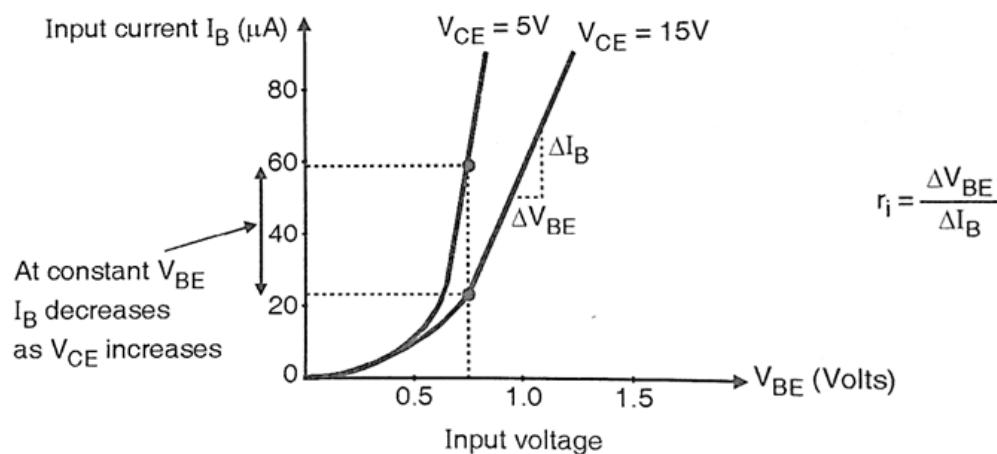
Base current I_B :

Base current I_B is

$$I_B = I_E - I_C \quad \text{---- (6)}$$

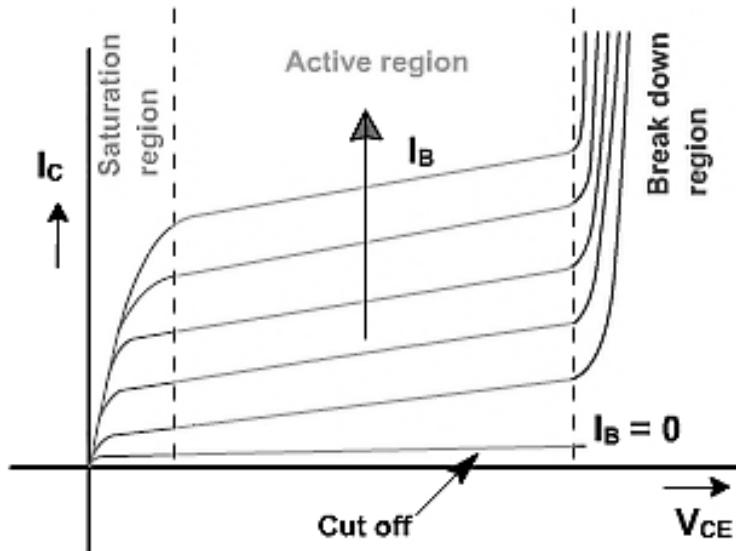
Input Characteristic of CE configuration:

Input characteristic is the relation between transistors input current I_B and input voltage V_{BE} , keeping the output voltage V_{CE} constant.



Output Characteristic of CE configuration:

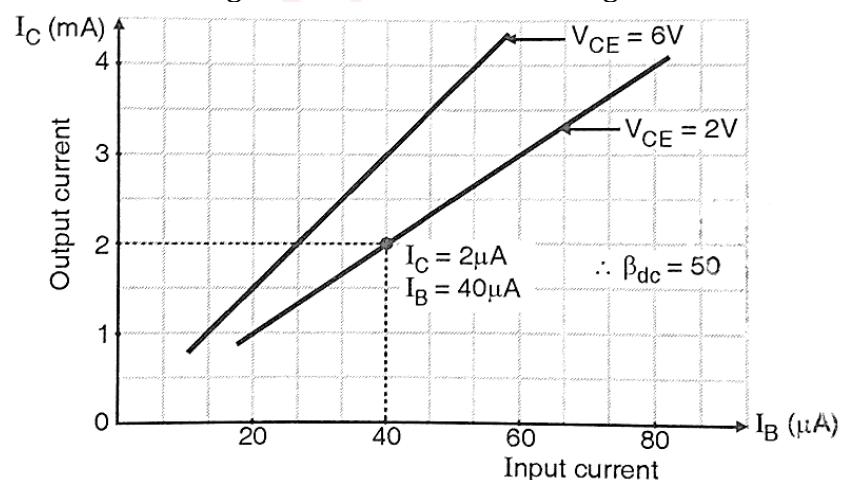
Output characteristic is the relation between transistors output current I_C and output voltage V_{CE} , keeping the input current I_B constant.



If an excessive reverse-bias voltage is applied to the collector-emitter junction, the device breakdown may occur.

Transfer Characteristic of CE configuration

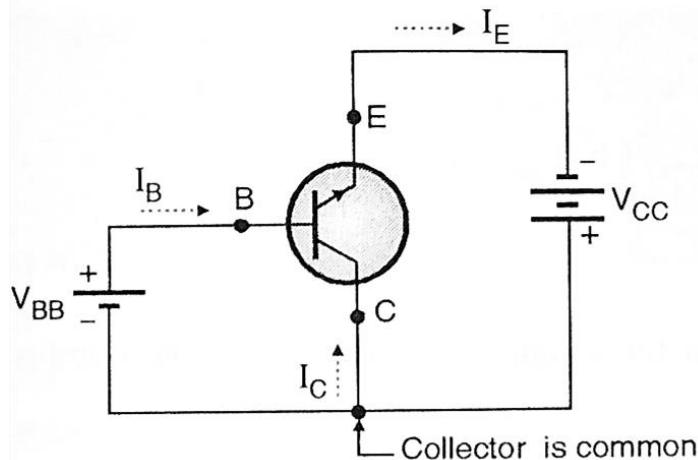
Transfer characteristic is the relation between transistors output current I_C and input current I_B for constant V_{CB} voltage. It is linear as shown in figure.



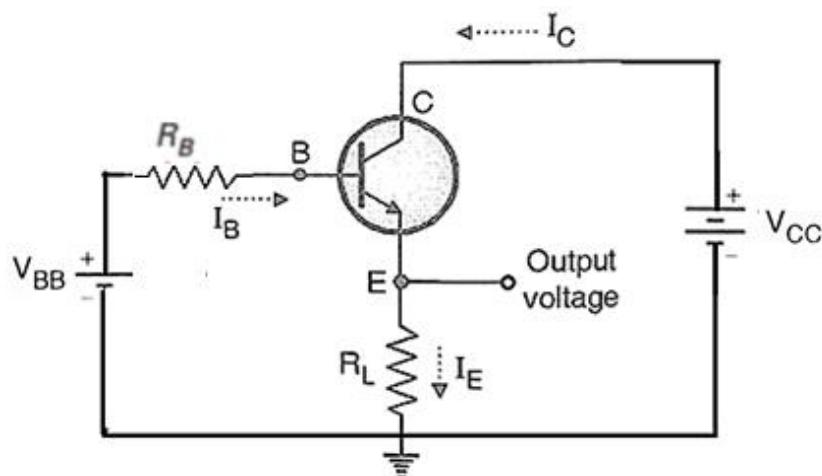
2.10 Common Collector Configuration of Transistor (CC Configuration)

In common collector configuration, base is the input terminal, emitter is the output terminal, and collector is the common terminal between input and output.

As shown in figure EB junction is forward biased and CB junction is reverse biased. To forward bias EB junction V_{BB} battery is connected and to reverse bias CB junction V_{CC} battery is connected as shown in figure. Resistance R_B and R_E are current limiting resistors.



The above circuit can be redrawn as follow:



Current Gain and different current components in CE configuration:

Current Gain γ_{dc} :

It is defined as the ratio of output current I_E to Input current I_B . It is denoted by γ_{dc} or γ . It is represented by equation

$$\gamma_{dc} = \frac{I_E}{I_B} = \frac{I_C + I_B}{I_B} \quad \text{-----(1)}$$

In equation (1)

$$I_C \cong \beta_{dc} I_B$$

Hence,

$$\gamma_{dc} \cong 1 + \beta_{dc} \quad \text{-----(2)}$$

Collector current I_C :

As we know that collector current can be written as

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

or

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{---- (3)}$$

as I_{CEO} is very small, If we neglect I_{CEO} then collector current I_C is approximated to

$$I_C \cong \beta_{dc} I_B$$

Emitter current I_E :

Emitter current is sum of Base current I_B and collector current I_C

$$I_E = I_C + I_B \quad \text{---- (4)}$$

Putting the value of I_C in equation (4) from equation (3)

$$I_E = \beta_{dc} I_B + I_{CEO} + I_B$$

$$I_E = I_B(1 + \beta_{dc}) + I_{CEO}$$

---- (5)

$$I_E \cong I_B(1 + \beta_{dc})$$

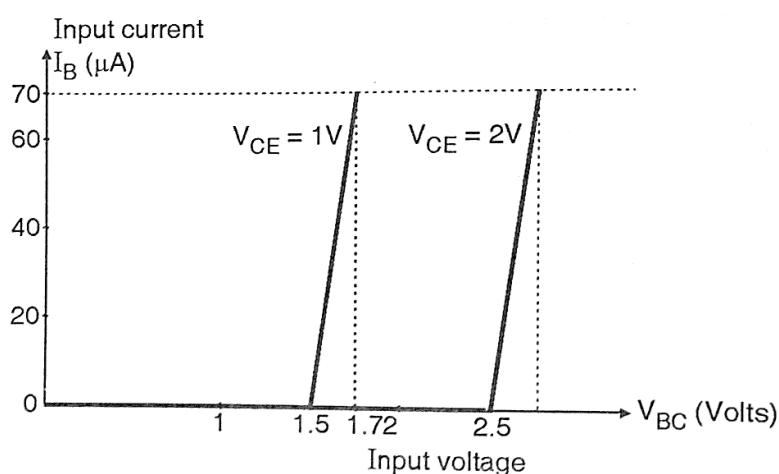
Base current I_B :

Base current I_B is

$$I_B = I_E - I_C \quad \text{---- (6)}$$

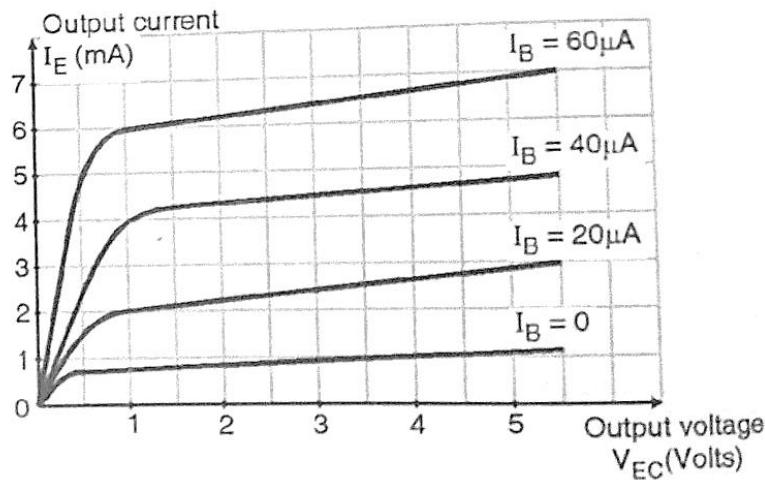
Input Characteristic of CC configuration:

Input characteristic is the relation between transistors input current I_B and input voltage V_{BC} , keeping the output voltage V_{CE} constant.



Output Characteristic of CC configuration:

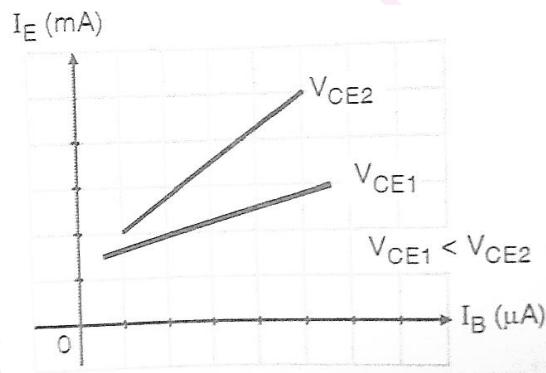
Output characteristic is the relation between transistors output current I_E and output voltage V_{EC} , keeping the input current I_B constant.



If an excessive reverse-bias voltage is applied to the collector-emitter junction, the device breakdown may occur.

Transfer Characteristic of CC configuration

Transfer characteristic is the relation between transistors output current I_E and input current I_B for constant V_{CE} voltage. It is linear as shown in figure.



2.11 Relation between current gain α , β and γ

The emitter current equation is

$$I_E = I_B + I_C \quad \dots \dots (1)$$

Dividing equation (1) by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \dots \dots (2)$$

$$\frac{1}{\alpha} = \frac{1 + \beta}{\beta}$$

$$\alpha = \frac{\beta}{1 + \beta}$$

---- (3)

Equation (3) indicates α in terms of β

Rearranging equation (2) again

$$\frac{1}{\beta} = \frac{1}{\alpha} - 1$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

---- (4)

Equation (4) indicates β in terms of α

Also the emitter current equation is

$$I_E = I_B + I_c$$

---- (5)

Dividing equation (7) by I_B

$$\frac{I_E}{I_B} = \frac{I_B}{I_B} + \frac{I_C}{I_B}$$

$$\gamma = 1 + \beta$$

---- (6)

2.12 Relation between leakage current I_{CBO} and I_{CEO}

Emitter current is

$$I_E = I_B + I_c$$

In CB configuration, collector current is

$$I_C = \alpha I_E + I_{CBO} \quad \text{--- (1)}$$

Putting the value of emitter current $I_E = I_B + I_c$ in equation (1)

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$(1 - \alpha) I_C = \alpha I_B + I_{CBO}$$

Hence,

$$I_C = \left(\frac{\alpha}{1 - \alpha} \right) (I_B) + \left(\frac{I_{CBO}}{1 - \alpha} \right)$$

--- (2)

But in equation (2)

$$\frac{\alpha}{1 - \alpha} = \beta$$

and

$$1 - \alpha = 1 - \frac{\beta}{1 + \beta} = \frac{1}{1 + \beta}$$

$$\frac{1}{1 - \alpha} = 1 + \beta$$

Now, equation (2) can be written as

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

--- (3)

In CE configuration, collector current is

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (4)}$$

Comparing equation (3) and (4)

$$I_{CEO} = (1 + \beta) I_{CBO}$$

---- (5)

2.13 Comparison between CB, CE and CC configuration of transistor

Sr. No.	Parameters	CB	CE	CC
1	Common terminal between input and output	Base	Emitter	Collector
2	Input current	I _E	I _B	I _B
3	Output current	I _C	I _C	I _E
4	Current Gain	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\gamma_{dc} = \frac{I_E}{I_B}$
		Low	High	High
5	Input voltage	V _{EB}	V _{BE}	V _{CB}
6	Output voltage	V _{CB}	V _{CE}	V _{EC}
7	Voltage gain	Medium	High	Low
8	Input Impedance	Very low (20 Ω)	Medium (1 KΩ)	Very high (1 MΩ)
9	Output impedance	Very high (1 MΩ)	High (40 KΩ)	Very low (50 Ω)
10	Power gain	Medium	Very High	Medium
11	Leakage current	Low	High	High
12	Signal Phase	In phase with input	Out of phase with input	In phase with input
13	Application	Preamplifier	Audio Amplifier	Impedance matching

2.14 Why CE configuration is most preferred?

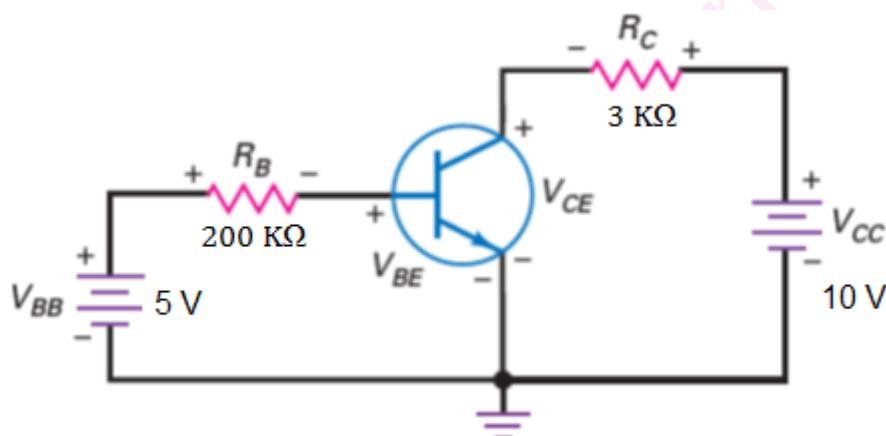
Out of three configuration of transistor, CE configuration is most popular and widely used because of following reason

- (i) It has high current and voltage gain.
- (ii) Power gain is high.
- (iii) Input and Output impedance are moderate/high. Hence many such stage of CE configuration can be coupled/cascaded to gather without any additional impedance matching circuit.

2.15 Examples

Example-1

For NPN transistor connected in CE configuration as shown in figure, calculate transistor currents and α . Given data are $\beta = 100$, $I_{CO} = 2 \times 10^{-8}$ mA.



Base Current:

Apply KVL law at input loop.

$$V_{BB} = I_B R_B + V_{BE}$$

Assuming $V_{BE} = 0.7$ V

$$5 = I_B (200 \times 10^3) + 0.7$$

$I_B = 21.5 \mu\text{A}$

--- (1)

Collector Current:

$$I_C = \beta I_B + I_{CO}$$

Putting the value of I_B from equation (1)

$$I_C = 100 \times (21.5 \times 10^{-6}) + 2 \times 10^{-8}$$

$I_C = 2.15 \text{ mA}$

---- (2)

Emitter Current:

$$I_E = I_B + I_C$$

Putting the value of I_B and I_C from equation (1) and (2)

$$I_E = (21.5 \times 10^{-6}) + 2.15 \times 10^{-3}$$

$I_E = 2.17 \text{ mA}$

---- (3)

Current Gain α :

$$\alpha = \frac{I_C}{I_E} = \frac{2.15}{2.17} = 0.99$$

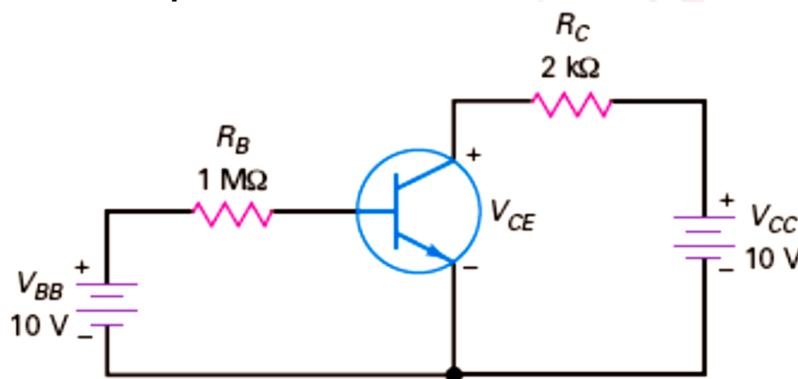
--- (4)

Also

$$\alpha = \frac{\beta}{1 + \beta} = \frac{100}{1 + 100} = 0.99$$

Example-2

For NPN transistor connected in CE configuration as shown in figure, calculate transistor currents I_B , I_C , V_{CE} , and P_D if $\beta = 300$.



Base Current:

Apply KVL law at input loop.

$$V_{BB} = I_B R_B + V_{BE}$$

Assuming $V_{BE} = 0.7 \text{ V}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10 - 0.7}{1 \times 10^6} = 9.3 \times 10^{-6}$$

$I_B = 9.3 \mu\text{A}$

--- (1)

Collector Current:

$$I_C = \beta I_B$$

Putting the value of I_B from equation (1)

$$I_C = 300 \times (9.3 \times 10^{-6})$$

$I_C = 2.79 \text{ mA}$

---- (2)

Collector to Emitter voltage V_{CE} :

Apply KVL law at output loop.

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

Putting the value of I_B and I_C from equation (1) and (2)

$$V_{CE} = 10 - 2.79 \times 10^{-3} \times 2 \times 10^3$$

$V_{CE} = 4.42 \text{ volt}$

----- (3)

Power dissipation P_D :

$P_D = V_{CE} I_C = 4.42 \times 2.79 \times 10^{-3} = 12.3 \times 10^{-3}$

darshan
--- (4)

$P_D = 12.3 \text{ mW}$

Transistor Biasing & Thermal Stability

2.16 Transistor Biasing & Need of biasing

What is Biasing?

Use of DC potential (DC Battery/power supply) to establish the operating condition of transistor is called biasing.

Transistor can be operated in either of three regions

Condition	(E-B Junction)	(C-B Junction)	Operating Region	Application
FR	Forward Biased	Reverse Biased	Active	Amplifier
FF	Forward Biased	Forward Biased	Saturation	Switch
RR	Reverse Biased	Reverse Biased	Cutoff	Switch

In order to operate in either of region, DC battery/power supply is required to be connected with correct polarity.

Biasing in electronics means establishing predetermined voltages or currents at various points of an electronic circuit for the purpose of establishing proper operating conditions in electronic components.

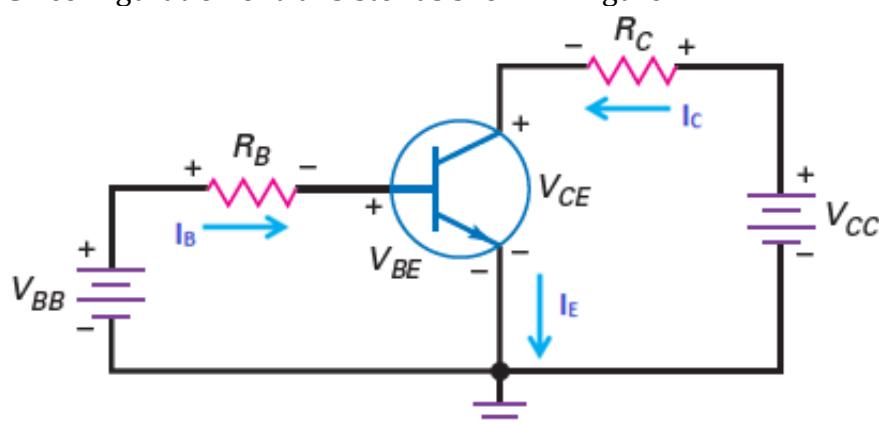
Need of Biasing :

- (i) To stabilize the operating point Q.
- (ii) To set operating point Q, at center of DC load line.
- (iii) To reduce the value of stability factor (S)
- (iv) Stabilize the collector current against temperature variations.
- (v) To operate the transistor in active region as an amplifier OR To operate the transistor as a switch

2.17 DC Load line and Operating point Q

The DC load line represents the desirable combinations of the collector current I_C and the collector-emitter voltage V_{CE} . It is drawn when no signal is given to the input, and the transistor biased with DC supply.

Consider the CE configuration of transistor as shown in figure.



For the given circuit, applying KVL low at output loop,

$$V_{CC} = I_C R_C + V_{CE} \quad \text{---- (1)}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

Rearranging equation (1)

$$I_C = \left(-\frac{1}{R_C} \right) (V_{CE}) + \left(\frac{V_{CC}}{R_C} \right) \quad \text{---- (2)}$$

Equation (2) is like the equation of straight line i.e. $y = mx + C$

The straight line represented by equation (2) is called **DC Load Line**.

In equation (2) when $V_{CE} = 0$,

$$I_C = \frac{V_{CC}}{R_C}$$

This is maximum possible current through transistor. Hence

$$I_{C(max)} = \frac{V_{CC}}{R_C} \quad \text{---- (3)}$$

Equation (3) is maximum possible current through transistor. So it is called **Saturation** point. Hence

$$I_{C(saturation)} = \frac{V_{CC}}{R_C}$$

Now, in equation (2) when $I_C = 0$,

$$V_{CE} = V_{CC}$$

This is maximum possible voltage across transistor. Hence

$$V_{CE(max)} = V_{CC}$$

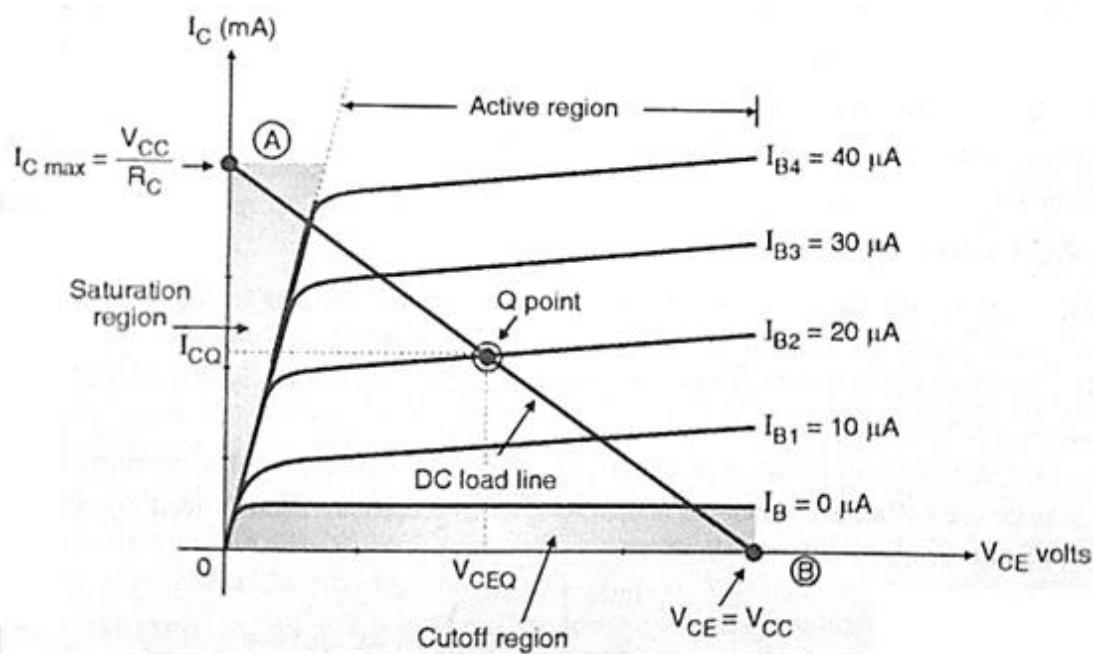
---- (4)

Equation (4) is maximum possible voltage across transistor. So it is called **cut-off** point. Hence

$$V_{CE(cut-off)} = V_{CC}$$

Line joining the Saturation and cut-off point is called **DC Load Line**. It is a straight line as shown in figure. Any point/value corresponding to I_C and V_{CE} will be on this DC Load Line

The DC Load Line is shown with output characteristic of transistor.



Q point (Quiescent point)

The Q point is also called **operating point** OR Bias point OR Quiescent point.

It is the point on DC Load Line, which represents the DC current I_{CQ} through transistor and voltage V_{CEQ} across transistor in quiescent or steady state/DC condition.

The co-ordinates of Q point are I_{CQ} and V_{CEQ} .

$$Q = (I_{CQ}, V_{CEQ})$$

The position of Q point on dc load line depends on application of transistor. When transistor is used as an amplifier, operating point Q should be set at the center of dc load line to avoid distortion in output waveform.

Position of Q point on dc load line is determined based on its application,

Application	Position of Q point
ON switch	At cut-off point/Region
OFF switch	At saturation point/Region
Amplifier	At center of dc load line/ In Active Region

2.18 Factors affecting the stability of Q point

Ideally Q point must be stable. It should not shift upward or downward on dc load line. But practically, Q point is unstable and changes its position on dc load line. The factors affecting the stability of Q point are

- (i) Change in temperature
- (ii) Change in value of β_{dc}
- (iii) Variation in transistor parameters from one device to another.

(1) Q point instability due to Temperature.

As temperature changes, current through transistor will also change. Due to change in junction temperature of transistor its parameter like V_{BE} , β_{dc} and I_{CBO} will change. Which in turn results in change in operating point Q (I_{CQ} , V_{CEQ}).

(2) Q point instability due to change in β_{dc}

Collector current of transistor is related with β_{dc} , as per equation $I_C = \beta I_B$. Hence if β_{dc} changes then collector current will also change. Which in turn results in change in operating point Q (I_{CQ} , V_{CEQ}).

(3) Q point instability due to variation in transistor parameter

Parameters like β_{dc} of two transistors with same number, type and manufacturer are slightly different in value. So when one transistor is replaced by another transistor, its collector current will also change. Which in turn results in change in operating point Q (I_{CQ} , V_{CEQ}).

2.19 Stability factor:

Stability factor indicates the stability of Q point against the variation/change in transistor parameters. Stability of Q point in transistor depends on following three parameters.

- (i) Reverse Leakage current I_{CO}
- (ii) Current gain β_{dc}
- (iii) Base to emitter voltage V_{BE}

Stability factor S:

It is defined as the ratio of change in collector current due to change in reverse saturation current/leakage current I_{CO} , when β_{dc} and V_{BE} are constant.

$$S = \frac{\Delta I_C}{\Delta I_{CO}}$$

For constant β_{dc} and V_{BE}

Stability factor S' :

It is defined as the ratio of change in collector current due to change in V_{BE} , when β_{dc} and I_{CO} are constant

$$S' = \frac{\Delta I_C}{\Delta V_{BE}}$$

For constant β_{dc} and I_{CO}

Stability factor S'' :

It is defined as the ratio of change in collector current due to change in β_{dc} , when V_{BE} and I_{CO} are constant

$$S'' = \frac{\Delta I_C}{\Delta \beta_{dc}}$$

For constant V_{BE} and I_{CO}

Ideally the value of stability factor should be Zero. Practically it should be small as possible.

2.20 Bias Stabilization Techniques/Biasing Circuits:

Bias stabilization is a process of stabilizing the Q point. Hence biasing circuit is required to be designed to keep operating point stable on dc load line.

Requirement of biasing circuits

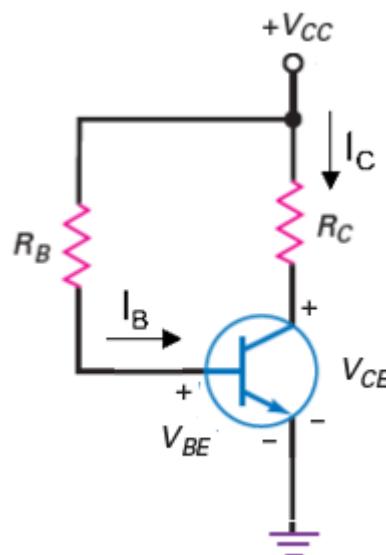
- (i) To establish the operating point Q at the middle of load line.
- (ii) Stabilize collector current against variation in temperature.
- (iii) To make operating point Q independent of transistor parameter.

Various biasing circuits

- (i) Fixed Bias circuit.
- (ii) Collector to Base Bias circuit.
- (iii) Voltage Divider Bias circuit.

2.21 Fixed Bias Circuit (Single Base Resistor Bias/Base Bias):

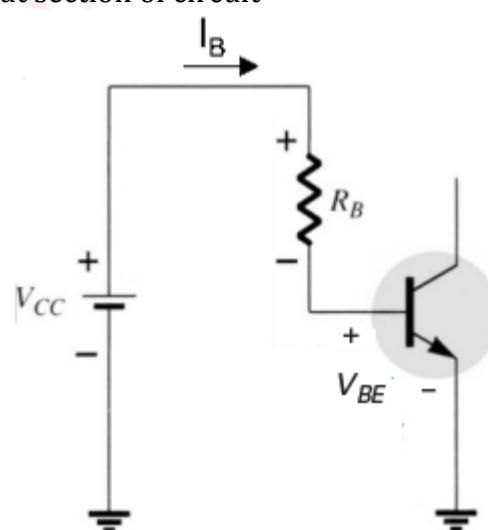
The fixed-bias configuration is the simplest of transistor biasing arrangement. Fixed bias circuit is as shown in figure



Steps to find Q point:

Input section:

DC equivalent circuit can be drawn as follow.
 Let us consider only the input section of circuit



If we apply KVL law at input loop then,

$$V_{CC} = I_B R_B + V_{BE} \quad \text{---- (1)}$$

from equation (1), base current is given as

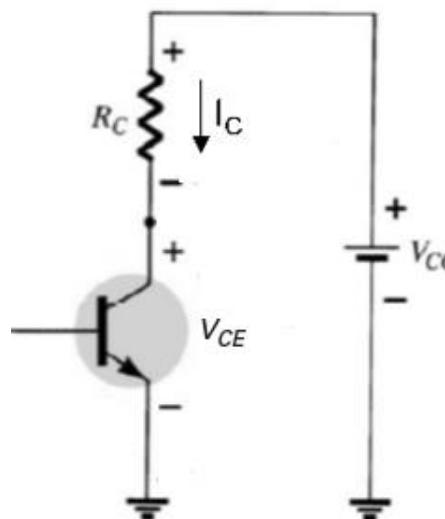
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \text{--- (2)}$$

Since V_{BE} is very small, it can be neglected compared to V_{CC} then equation (2) can be approximated to

$$I_B \cong \frac{V_{CC}}{R_B}$$

Output section:

Let us consider only the output section of circuit



The collector current in terms of Base current is derived by equation

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (3)}$$

If we apply KVL law at output loop then,

$$V_{CC} = I_C R_C + V_{CE} \quad \text{---- (4)}$$

from equation (4), collector to emitter voltage is given as

$$V_{CE} = V_{CC} - I_C R_C \quad \text{--- (5)}$$

Equation (3) and (5) are the equation of operating point Q

$$I_{CQ} = \beta_{dc} I_B + I_{CEO}$$

$$V_{CEQ} = V_{CC} - I_C R_C$$

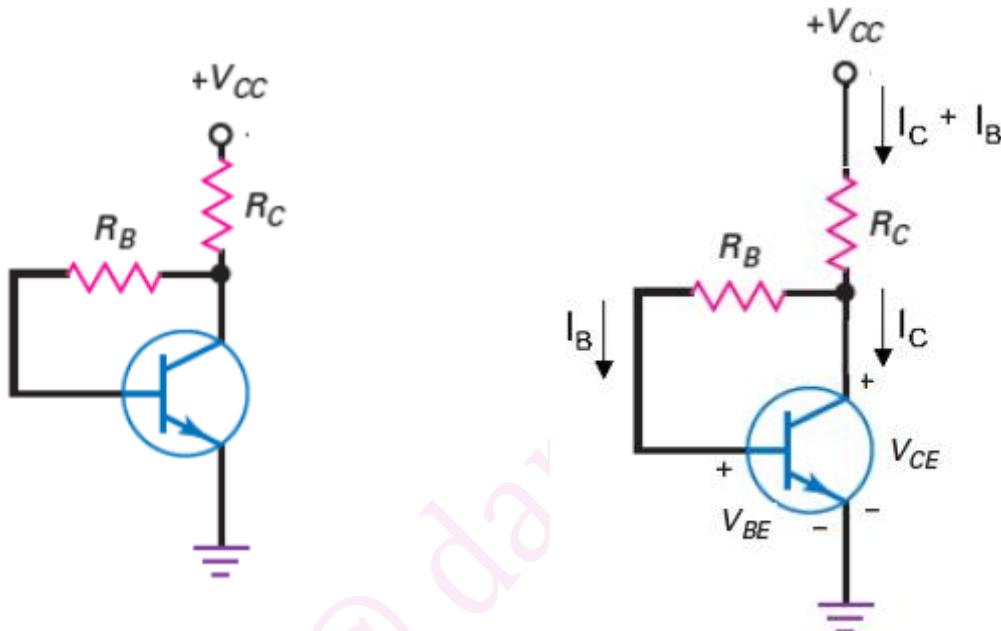
Stabilization of Q point in Fixed bias circuit:

- The fixed bias circuit is simple and easy to design. But still it is seldom used because it can not stabilize operating point Q.

- if temperature increases then leakage current I_{CEO} will change, which will result in change in I_{CQ} corresponding to Q point.
- Also if transistor is replaced by another transistor then β_{dc} may change which results in change in I_{CQ} corresponding to Q point.

2.22 Collector to Base Bias Circuit:

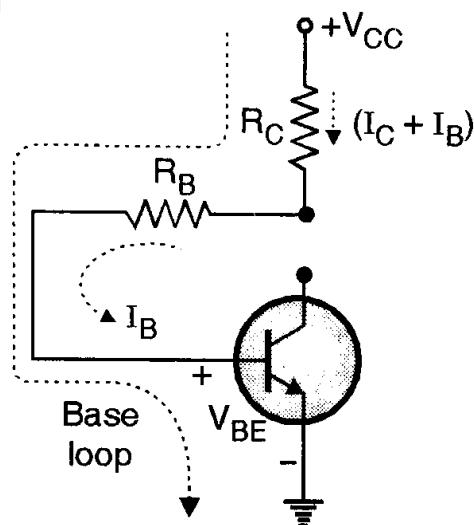
In collector to base bias configuration, base resistor R_B is connected to the collector terminal instead of battery V_{CC} . collector to base bias circuit is as shown in figure.



Steps to find Q point:

Input section:

Let us consider only the input loop/section of circuit



If we apply KVL law at input loop then,

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE} \quad \text{--- (1)}$$

$$V_{CC} = I_C R_C + (R_C + R_B) I_B + V_{BE}$$

from equation (1), base current is given as

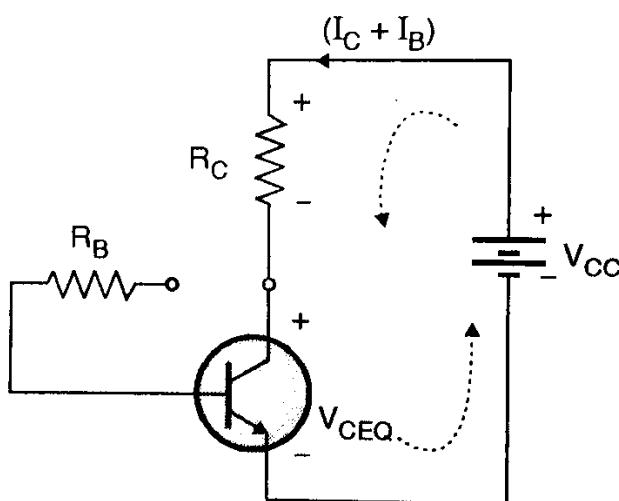
$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B} \quad \text{--- (2)}$$

Since V_{BE} is very small, it can be neglected compared to V_{CC} then equation (2) can be approximated to

$$I_B \cong \frac{V_{CC} - I_C R_C}{R_C + R_B}$$

Output section:

Let us consider only the output section of circuit



The collector current in terms of Base current is derived by equation

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (3)}$$

If we apply KVL law at output loop then,

$$V_{CC} = (I_C + I_B) R_C + V_{CE} \quad \text{--- (4)}$$

from equation (4), collector to emitter voltage is given as

$$V_{CE} = V_{CC} - (I_C + I_B) R_C \quad \text{--- (5)}$$

Also,

$$V_{CE} = V_{CC} - I_C R_C - I_B R_C \quad \text{--- (6)}$$

As Current $I_B \ll I_C$, equation (6) can be approximated to

$$V_{CE} \cong V_{CC} - I_C R_C \quad \text{--- (7)}$$

If we replace the value of equation (7) in equation (2) then Base current can be written as

$$I_B \cong \frac{V_{CE} - V_{BE}}{R_C + R_B}$$

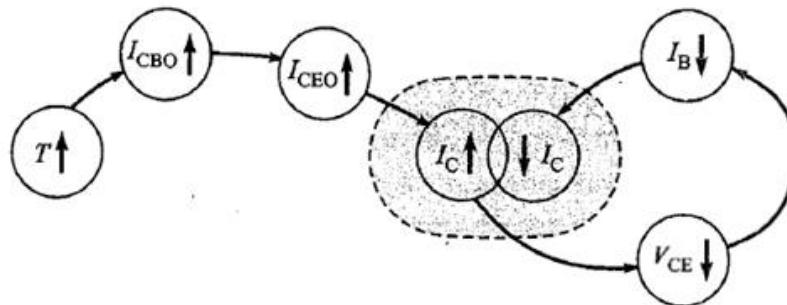
Equation (3) and (5) are the equation of operating point Q

$$I_{CQ} = \beta_{dc} I_B + I_{CEO}$$

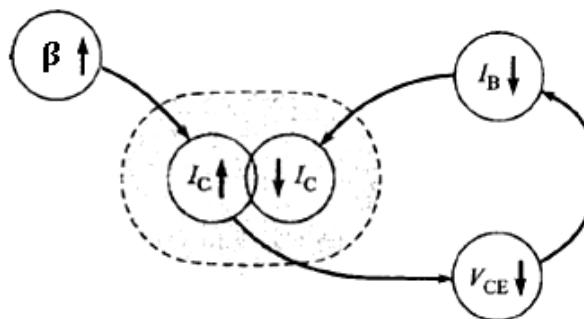
$$V_{CEQ} = V_{CC} - (I_C + I_B) R_C$$

Stabilization of Q point in collector to base bias circuit:

- if temperature increases then leakage current I_{CEO} will increase, which will result in increase in I_{CQ} . If collector current I_C increases then V_{CE} will decrease (because $V_{CE} \cong V_{CC} - I_C R_C$). When V_{CE} decreases, it also decreases base current I_B . Decrease in base current forces collector current to decrease. Hence increase of collector current due to temperature will be stabilized by decrease in base current.



- if transistor is replaced by another transistor then β_{dc} may change which results in change in I_{CQ} corresponding to Q point. If collector current I_C increases then V_{CE} will decrease (because $V_{CE} \cong V_{CC} - I_C R_C$). When V_{CE} decreases, it also decreases base current I_B . Decrease in base current forces collector current to decrease. Hence increase of collector current due to change in β_{dc} will be stabilized by decrease in base current.

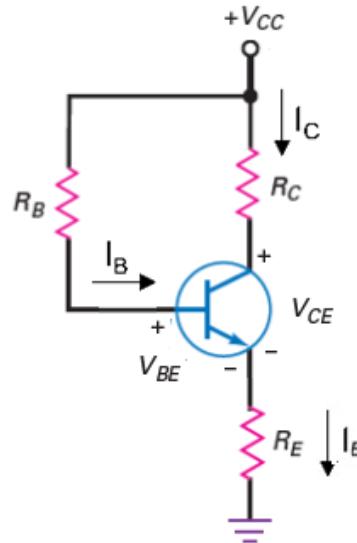


Limitation of collector to base bias circuit:

- Collector to base bias circuit is seldom used because base resistor provides negative feedback, which reduces the gain of not only DC but also AC input signal.

2.23 Emitter feedback Bias Circuit (Bias circuit with emitter resistor):

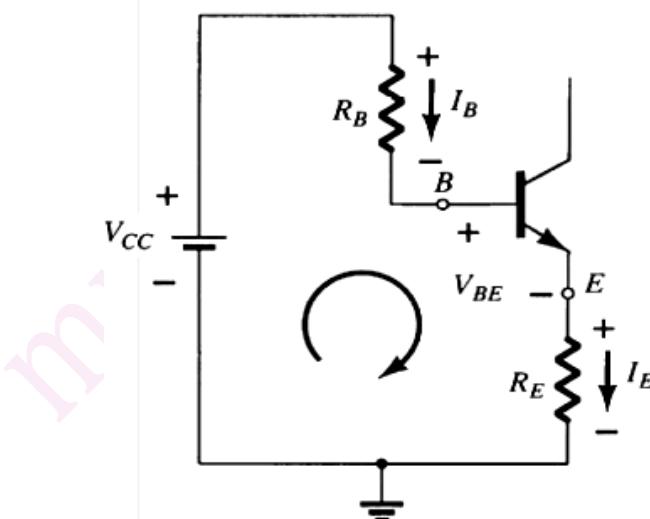
In emitter feedback bias three resistors R_B , R_C , and R_E are connected as shown in figure. Emitter resistor provides negative feedback. This circuit can able to stabilize operating point Q..



Steps to find Q point:

Input section:

Let us consider only the input loop/section of circuit



If we apply KVL law at input loop then,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \quad \text{---- (1)}$$

from equation (1), base current is given as

$$I_B = \frac{V_{CC} - I_E R_E - V_{BE}}{R_B}$$

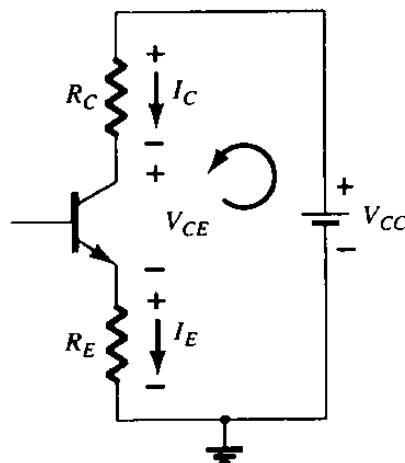
--- (2)

Since V_{BE} is very small, it can be neglected compared to V_{CC} then equation (2) can be approximated to

$$I_B \cong \frac{V_{CC} - I_E R_E}{R_B}$$

Output section:

Let us consider only the output section of circuit



The collector current in terms of Base current is derived by equation

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \text{--- (3)}$$

If we apply KVL law at output loop then,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \quad \text{--- (4)}$$

from equation (4), collector to emitter voltage is given as

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad \text{--- (5)}$$

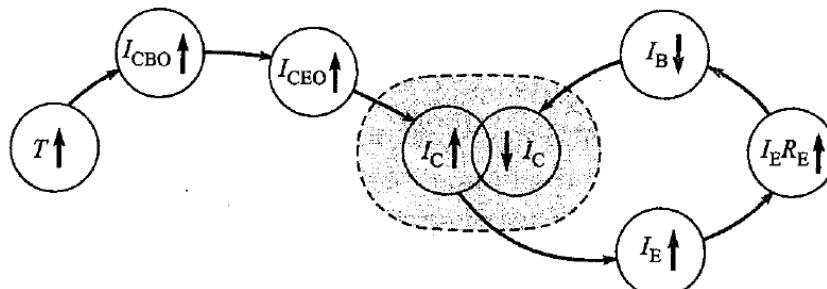
Equation (3) and (5) are the equation of operating point Q

$$I_{CQ} = \beta_{dc} I_B + I_{CEO}$$

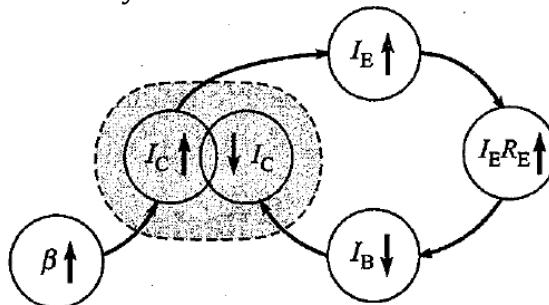
$$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$$

Stabilization of Q point in collector to base bias circuit:

- if temperature increases then leakage current I_{CEO} will increase, which will result in increase in I_{CQ} . If collector current I_C increases then I_E will increase. When I_E increases, it results in decreases in base current I_B . Decrease in base current forces collector current to decrease. Hence increase of collector current due to temperature will be stabilized by decrease in base current.



- if transistor is replaced by another transistor then β_{dc} may change which results in change in I_{CQ} corresponding to Q point. If collector current I_C increases then I_E will increase. When I_E increases, it results in decreases in base current I_B . Decrease in base current forces collector current to decrease. Hence increase of collector current due to change in β_{dc} will be stabilized by decrease in base current.

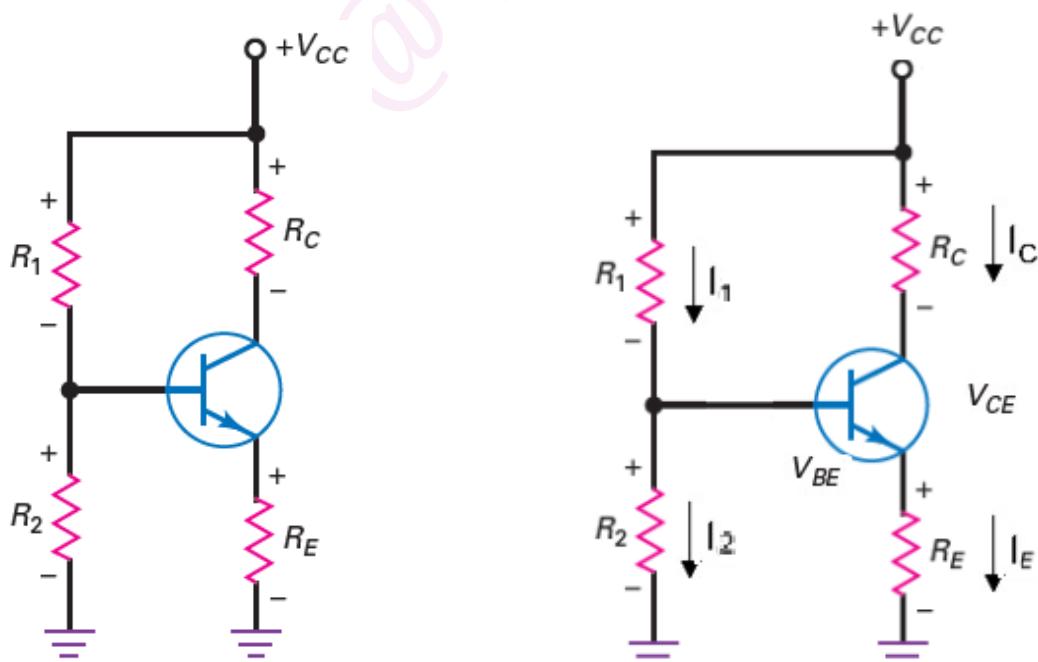


Limitation of collector to base bias circuit:

In emitter bias, emitter resistor provides negative feedback, which reduces the gain of not only DC but also AC input signal but reduction in AC gain can be avoided by connecting one capacitor in parallel with emitter resistor.

2.24 Voltage Divider Bias Circuit (Self Bias):

It is most widely used biasing circuit. It stabilize the operating point Q against change in temperature as well as transistor current gain β_{dc} . Voltage divider bias circuit is as shown in figure. The base circuit contains a voltage divider (R_1 and R_2). Because of this, the circuit is called voltage-divider bias.



Resistor R_1 and R_2 forms voltage divider network. To simplify the circuit, it can be converted to Thevenin's equivalent circuit.

Thevenin's equivalent circuit can be derived by finding out Thevenin equivalent Resistor R_{TH} and Voltage V_{TH} .

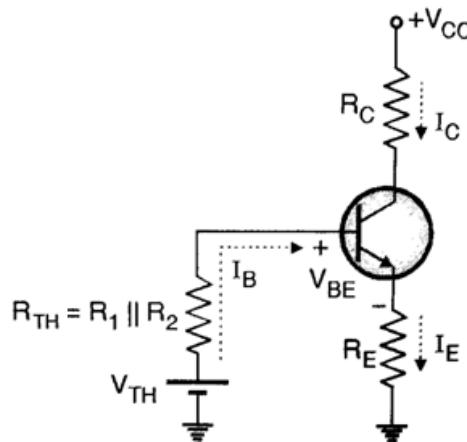
Thevenin's equivalent Resistor

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

Thevenin's equivalent Voltage

$$V_{TH} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

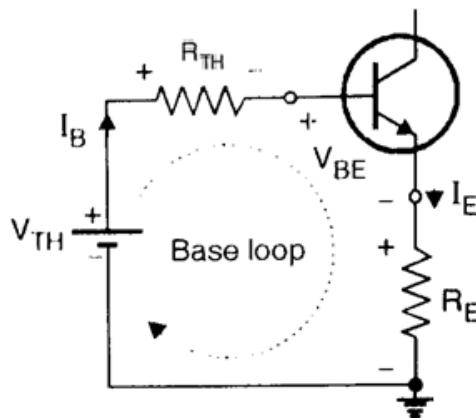
Now Thevenin's equivalent circuit is



Steps to find Q point:

Input section:

Let us consider only the input loop/section of Thevenin's equivalent circuit



If we apply KVL law at input loop then,

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E \quad \text{---- (1)}$$

But, $I_E = (1 + \beta_{dc})I_B$

$$V_{TH} = I_B R_{TH} + V_{BE} + (1 + \beta_{dc})I_B R_E \quad \text{---- (2)}$$

from equation (2), base current is given as

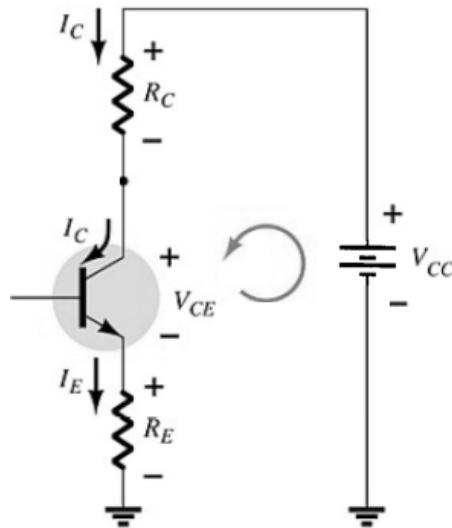
$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1 + \beta_{dc}) R_E} \quad \text{---- (3)}$$

Since V_{BE} is very small, it can be neglected compared to V_{TH} . Also $\beta_{dc} \gg 1$, then equation (3) can be approximated to

$$I_B \cong \frac{V_{TH}}{R_{TH} + \beta_{dc} R_E}$$

Output section:

Let us consider only the output section of circuit



The collector current in terms of Base current is derived by equation

$I_C = \beta_{dc} I_B + I_{CEO}$

--- (4)

If we apply KVL law at output loop then,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \quad \text{---- (5)}$$

from equation (5), collector to emitter voltage is given as

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

--- (6)

Equation (4) and (6) are the equation of operating point Q

$$I_{CQ} = \beta_{dc} I_B + I_{CEO}$$

$$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$$

2.25 Bias Compensation Techniques:

Bias stabilization and compensation techniques are used to stabilize the operating point Q against variation in Temperature, I_{CO} , β_{dc} , and V_{BE} .

Stabilization techniques refer to the use of resistive biasing circuits.

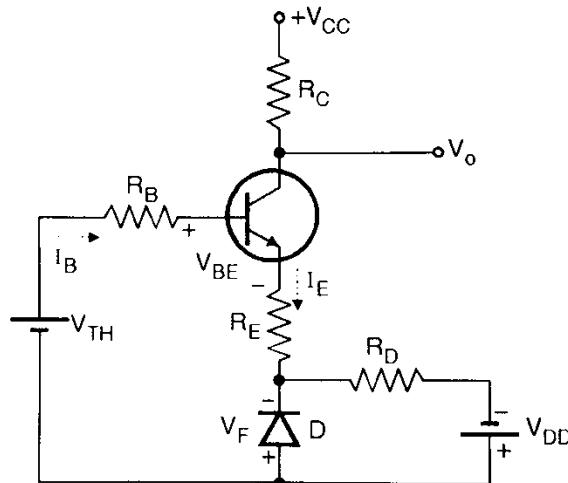
Compensation techniques refer to the use of temperature sensitive device such as Diode, Thermistor, Sensistor.

Types of bias compensation techniques includes

- (i) Compensation for changes in V_{BE} .
- (ii) Compensation for changes in I_{CO} .

(1) Diode compensation for V_{BE}

As shown in figure Diode and transistor used are of same material and type. Also diode and transistor have same temperature co-efficient.



Applying KVL law at input base loop,

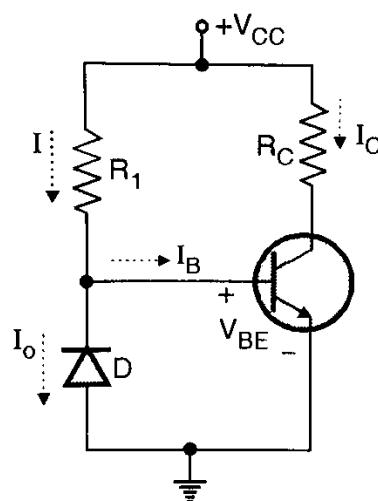
$$V_{TH} = I_B R_B + V_{BE} + I_E R_E - V_F \quad \text{--- (1)}$$

But material used for diode is same as that for transistor and have same temperature co-efficient. Hence change in voltage across diode V_F is same as change in V_{BE} across transistor due to change in Temperature. So in equation (1), V_F and V_{BE} will be cancel out.

Thus change in V_{BE} due to temperature is compensated by change in V_F and collector current corresponding to Q point, becomes insensitive to variation in transistor parameter V_{BE} .

(2) Diode compensation for I_{CO}

The diode compensation circuit shown in figure offers stabilization against variation in I_{CO} . Diode and transistor are of same type and material. Therefore reverse saturation current of diode I_O will increase with temperature at the same rate as leakage current of transistor I_{CO} will change.



As diode is reverse biased, current through resistor R_1 is

$$I_1 = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} = \text{constant}$$

The base current $I_B = I - I_O$. Now substitute the value of I_B in equation of collector current

$$I_C = \beta_{dc} I_B + (1 + \beta_{dc}) I_{CO}$$

$$I_C = \beta_{dc}(I - I_O) + (1 + \beta_{dc}) I_{CO}$$

$$I_C = \beta_{dc}I - \beta_{dc}I_O + (1 + \beta_{dc}) I_{CO} \quad \text{---(1)}$$

In equation (1), reverse leakage current of diode (I_O) is same as leakage current of transistor (I_{CO}), because material used for diode and transistor is same.

Also,

$$\beta_{dc}I_O \approx (1 + \beta_{dc}) I_{CO}$$

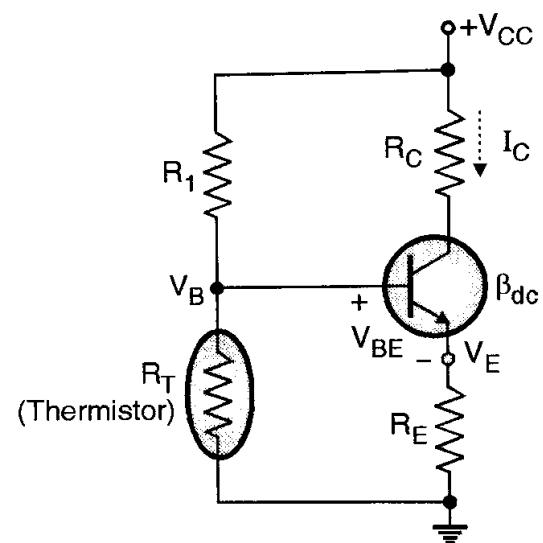
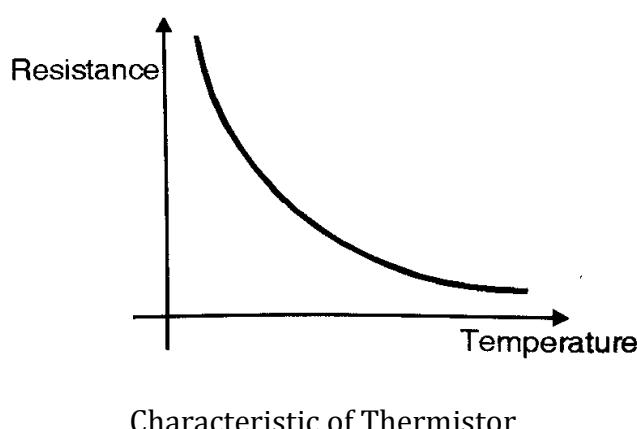
Hence equation (1) can be now written as

$$I_C = \beta_{dc}I$$

As current I is constant, collector current I_C will also remain constant irrespective of change in temperature. Thus compensation provided against change in I_{CO} due change in temperature.

(3) Bias compensation using Thermistor

Thermistor is temperature dependent resistor. It's resistance decreases exponentially as temperature increases. So thermistor has negative temperature co-efficient of resistance. As shown in figure, thermistor R_T is connected along with R_1 and forms voltage divider network.



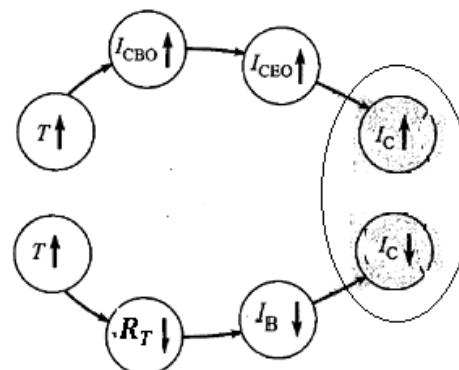
Now voltage V_B at base can be derived as

$$V_B = \frac{R_T V_{CC}}{R_1 + R_T}$$

Also, $V_E = I_E R_E$ and $V_{BE} = V_B - V_E$

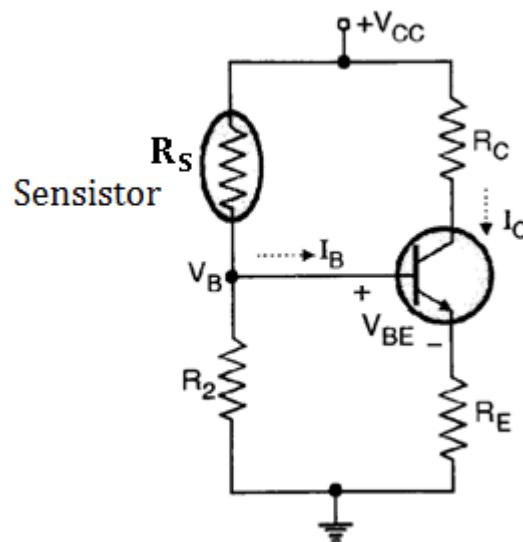
Now as temperature increase, collector current I_C tends to increase. At the same time increase in temperature, causes resistance of thermistor R_T to decrease. Hence base voltage V_B and V_{BE} decrease. This will force the base current I_B to decrease. Reduction in base current I_B will reduce collector current.

Hence increase in collector current due to temperature is compensated by decrease in collector current due to thermistor.



(4) Bias compensation using Sensistor

Sensistor is temperature dependent resistor. Its resistance increases exponentially as temperature increases. So sensistor has positive temperature co-efficient of resistance. As shown in figure, sensistor R_S is connected along with R_2 and forms voltage divider network.



Now voltage V_B at base can be derived as

$$V_B = \frac{R_2 V_{CC}}{R_2 + R_T}$$

Also, $V_E = I_E R_E$ and $V_{BE} = V_B - V_E$

Now as temperature increase, collector current I_C tends to increase. At the same time increase in temperature, causes resistance of sensistor R_S to increase. Hence base voltage V_B and V_{BE} decrease. This will force the base current I_B to decrease. Reduction in base current I_B will reduce collector current.

Hence increase in collector current due to temperature is compensated by decrease in collector current due to sensistor.

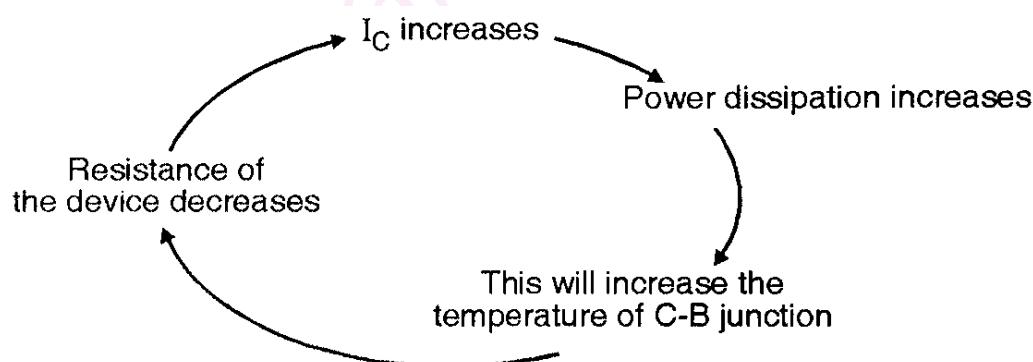
2.26 Thermal Runaway.

Maximum power a transistor can dissipate without getting damaged depends on the maximum temperature that a collector-base junction can withstand. Rise in temperature across collector –base junction can due to cumulative internal heating process.

The collector current in transistor is represented by equation

$$I_C = \beta_{dc} I_B + I_{CEO}$$

- If collector current increases, then power dissipation at collector-base junction also increases.
- Increase in power dissipation results in increase in temperature at C-B junction.
- As transistor has negative temperature co-efficient of resistance, increase in temperature at C-B junction, decreases resistance.
- The reduced resistance will increase the collector current.



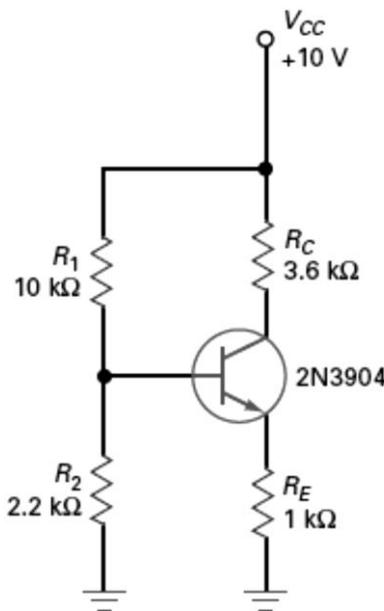
This becomes cumulative process which will finally results in damage/burning-off to transistor due to excessive internal heating. This process is known as **Thermal Runaway**.

Thermal runaway can be avoided by

- (i) Limiting collector current beyond certain maximum rating level.
- (ii) Limiting power dissipation below maximum permissible level.
- (iii) Using Heat Sink.

2.27 Example-3

What is the collector-emitter voltage for transistor shown in figure.



For voltage divider bias circuit , to find out V_{CB} , we need to derive voltage V_C and V_E

For voltage divider .

$$V_{BB} = \frac{2.2 \text{ K}\Omega \times V_{CC}}{2.2 \text{ K}\Omega + 10 \text{ K}\Omega}$$

$$V_{BB} = \frac{2.2 \times 10^3 \times 10}{12.2 \times 10^3} = 1.8 \text{ volt}$$

Assuming $V_{BE} = 0.7 \text{ V}$

$$V_{BB} = V_{BE} + I_E R_E = V_{BE} + V_E$$

$$V_E = V_{BB} - V_{BE}$$

$$V_E = 1.8 - 0.7 = 1.1 \text{ volt}$$

Emitter current is

$$I_E = \frac{V_E}{R_E} = \frac{1.1}{1 \times 10^3} = 1.1 \text{ mA}$$

Collector Current is almost same as emitter current

Now collector voltage can be derived as

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 10 - 1.1 \times 10^{-3} \times 3.6 \times 10^3 = 10 - 3.96 = 6.04$$

Hence,

$$V_{CE} = V_C - V_E = 6.04 - 1.1 = 4.94 \text{ volt}$$

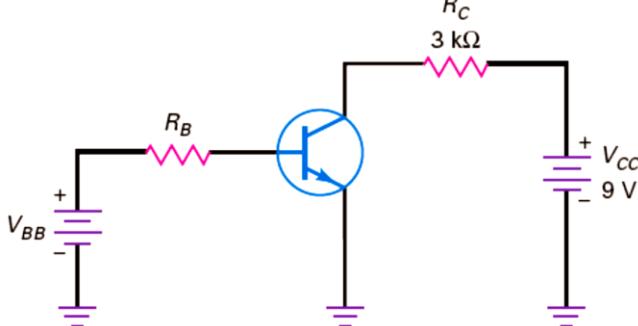
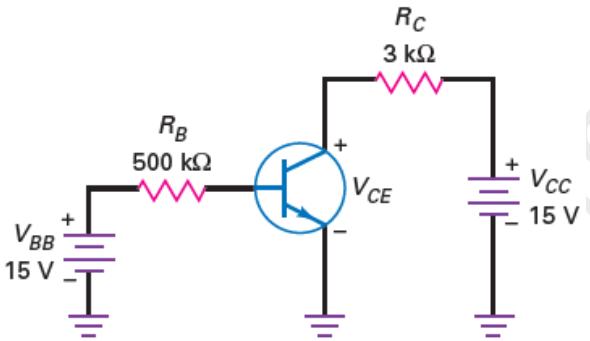
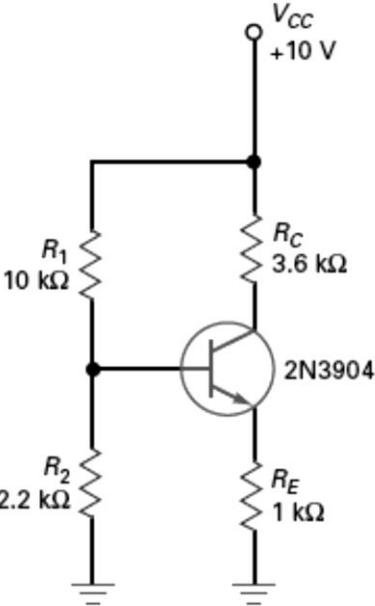
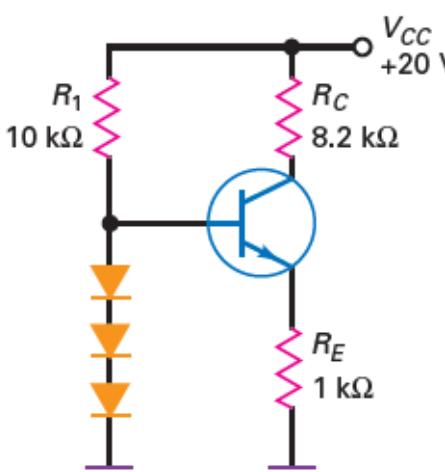
Exercise: Question Bank Unit-2

		Marks
Q:1	Classify the Transistors	4
Q:2	Draw the construction and symbol of NPN and PNP transistor and explain unbiased transistor in detail. Also give details of different operating region of transistor	7
Q:3	Explain working of Bipolar Junction Transistor in Active region	7
Q:4	Define following terms: (i) Emitter efficiency (ii) Base transportation factor (iii) Large signal current gain	3
Q:5	<i>Explain Common Base configuration (CB) of transistor in detail with necessary derivation, input characteristic and output characteristic.</i>	7
Q:6	<i>Using NPN transistor draw the circuit diagram of Common Emitter configuration (CE configuration) of transistor and explain it in detail with necessary derivation, input characteristic and output characteristic.</i>	7
Q:7	Explain Common Collector configuration (CC) of transistor in detail with necessary derivation, input characteristic and output characteristic.	7
Q:8	<i>What is Base width modulation or Early effect in transistor? Explain it in detail for CB configuration</i>	4
Q:9	Explain punch through or Reach through effect in transistor for CE configuration	4
Q:10	<i>Establish the relationship between current gain α, β and γ</i>	4
Q:11	Establish the relationship between leakage current I_{CBO} and I_{CEO}	4
Q:12	<i>Compare CB, CE and CC configuration of transistor</i>	7
Q:13	<i>Why CE configuration of transistor is most preferred?</i>	3
Q:14	What do you mean by Biasing? What is the need of biasing circuits?	4
Q:15	<i>Explain the concept DC Load line and Operating point Q. Also derive the equation of operating point Q for CE configuration.</i>	7
Q:16	Which are the factors that affects the stability of Q point?	4
Q:17	Define Stability factor S, S' and S''	3
Q:18	Explain Base Bias OR Fixed Bias circuit in detail with necessary circuit diagram and also derive the equations of Q point for Fixed bias	7
Q:19	<i>Explain Collector to Base Bias circuit in detail with necessary circuit diagram and also derive the equations of Q point.</i>	7

Q:20	Explain Emitter feedback Bias circuit in detail with necessary circuit diagram and also derive the equations of Q point.	7
Q:21	Explain Voltage Divider Bias OR Self Bias OR Universal Biasing circuit in detail with necessary circuit diagram and also derive the equations of Q	7
Q:22	What is the difference between bias stabilization techniques and Bias Compensation Techniques. Explain different bias compensation techniques.	7
Q:23	Write short note on Thermal Runaway	4

Tutorials/Examples

		Marks
Q:1	For NPN transistor connected in CE configuration as shown in figure, calculate transistor currents and α . Given data are $\beta = 100$, $I_{CO} = 2 \times 10^{-8}$ mA. 	7
Q:2	For NPN transistor connected in CE configuration as shown in figure, calculate transistor currents I_B , I_C , V_{CE} , and P_D if $\beta = 300$. 	7
Q:3	Derive stability factor S for CB and CE configuration of transistor.	4
Q:4	Find out ends of DC load line for the circuit shown in figure. Also draw the DC load line for given circuit. 	4

Q:5	<p>Calculate the saturation and cutoff values for circuit shown in figure and Draw the load lines</p> 	4
Q:6	<p>Calculate Q Point for given circuit. if $\beta = 100$.</p> 	7
Q:7	<p>What is the collector-emitter voltage for transistor shown in figure.7</p>  <p>Figure . 7</p>	4
Q:8	<p>Calculate I_C, V_{CE}, V_C and V_E for the circuit shown in figure.8. all the diodes and transistor are made from silicon material</p>  <p>Figure . 8</p>	7
Q:9	<p>Find out LED current for the circuit shown in figure.9.</p>	4
Q:10	<p>Find out LED current for the circuit shown in figure.10.</p>	4

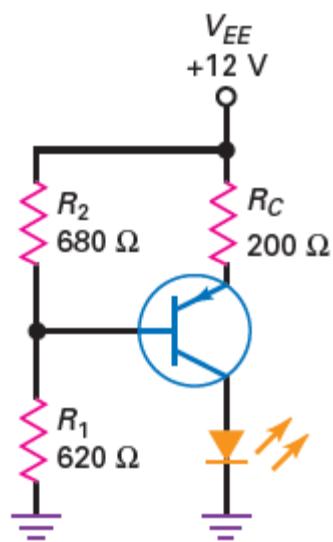


Figure . 9

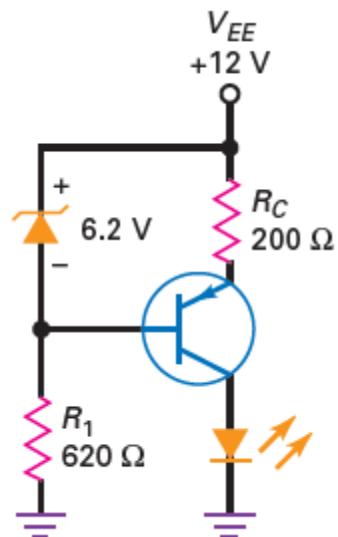


Figure . 10

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1.1 Introduction

- Rectifier diodes are the most common type of diode. They are used in power supplies to convert ac voltage to dc voltage. But rectification is not all that a diode can do.
- Now we will discuss diodes used in other applications. The chapter begins with the Zener diode, which is optimized for its breakdown properties.
- Zener diodes are very important because they are the key to voltage regulation. The chapter also covers optoelectronic diodes, including light-emitting diodes (LEDs), Schottky diodes, Varactors, and other diodes.

1.2 The Zener Diode

- Small-signal and rectifier diodes are never intentionally operated in the breakdown region because this may damage them. A Zener diode is different; it is a silicon diode that the manufacturer has optimized for operation in the breakdown region.
- The Zener diode is the backbone of voltage regulators, circuits that hold the load voltage almost constant despite large changes in line voltage and load resistance.

1.2.1 I-V Graph

- Figure-1a shows the schematic symbol of a Zener diode; Figure-1b is an alternative symbol. In either symbol, the lines resemble a **Z**, which stands for “Zener.”
- By varying the doping level of silicon diodes, a manufacturer can produce Zener diodes with breakdown voltages from about **2 to over 1000 V**. These diodes can operate in any of three regions: forward, leakage, and breakdown.
- Figure-1c shows the **I-V** graph of a Zener diode. In the forward region, it starts conducting around 0.7 V, just like an ordinary silicon diode. In the leakage region (between zero and breakdown), it has only a small reverse current.
- In a Zener diode, the breakdown has a very sharp knee, followed by an almost vertical increase in current. Note that the voltage is almost constant, approximately equal to V_z over most of the breakdown region.
- Data sheets usually specify the value of V_z at a particular test current I_{zT} .
- Figure-1c also shows the maximum reverse current I_{zM} . As long as the reverse current is less than I_{zM} , the diode is operating within its safe range.
- If the current is greater than I_{zM} , the diode will be destroyed. To prevent excessive reverse current, a current-limiting resistor must be used (discussed later).

1.2.2 Zener Resistance

- In the third approximation of a silicon diode, the forward voltage across a diode equals the knee voltage plus the additional voltage across the bulk resistance.
- Similarly, in the breakdown region, the reverse voltage across a diode equals the breakdown voltage plus the additional voltage across the bulk resistance.
- In the reverse region, the bulk resistance is referred to as the Zener resistance. This resistance equals the inverse of the slope in the breakdown region.
- In other words, the more vertical the breakdown region, the smaller the Zener resistance.

- In Figure-1c, the Zener resistance means that an increase in reverse current produces a slight increase in reverse voltage. The increase in voltage is very small, typically only a few tenths of a volt.
- This slight increase may be important in design work, but not in troubleshooting and preliminary analysis. Unless otherwise indicated, our discussions will ignore the Zener resistance. Figure-1d shows typical Zener diodes.

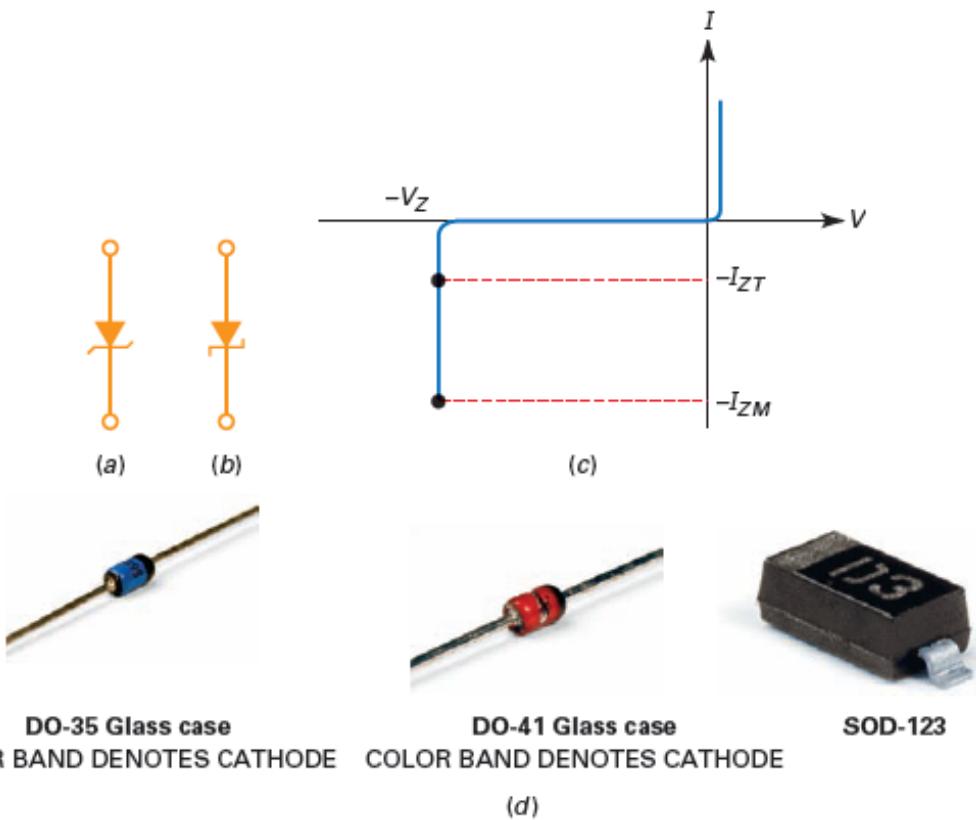


Figure-1 (a) Schematic symbol; (b) alternative symbol; (c) graph of current versus voltage; (d) typical Zener diodes

1.2.3 Zener Regulator

- A Zener diode is sometimes called a voltage-regulator diode because it maintains a constant output voltage even though the current through it changes. For normal operation, you have to reverse-bias the Zener diode, as shown in Figure-2a.

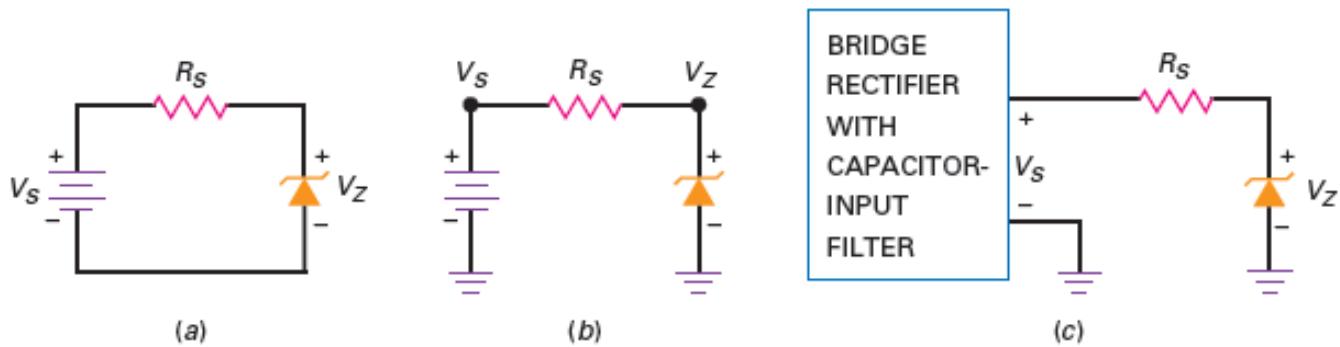


Figure-2 Zener regulator. (a) Basic circuit; (b) same circuit with grounds; (c) power supply drives regulator

- Furthermore, to get breakdown operation, the source voltage V_s must be greater than the Zener breakdown voltage V_z . A series resistor R_s is always used to limit the Zener current to less than its maximum current rating. Otherwise, the Zener diode will burn out, like any device with too much power dissipation.
- Figure-2b shows an alternative way to draw the circuit with grounds. Whenever a circuit has grounds, you can measure voltages with respect to ground.
- For instance, suppose you want to know the voltage across the series resistor of Figure-2b. Here is the one way to find it when you have a built-up circuit.
- First, measure the voltage from the left end of R_s to ground. Second, measure the voltage from the right end of R_s to ground. Third, subtract the two voltages to get the voltage across R_s . If you have a floating **VOM** or **DMM**, you can connect directly across the series resistor.
- Figure-2c shows the output of a power supply connected to a series resistor and a Zener diode. This circuit is used when you want a dc output voltage that is less than the output of the power supply. A circuit like this is called a Zener voltage regulator, or simply a Zener regulator.

1.2.4 Ohm's Law Again

- In Figure-2, the voltage across the series or current-limiting resistor equals the difference between the source voltage and the Zener voltage. Therefore, the current through the resistor is:

$$I_s = \frac{V_s - V_z}{R_s} \quad (1)$$

- Once you have the value of series current, you also have the value of Zener current. This is because Figure-2 is a series circuit. Note that I_s must be less than I_{zm} .

1.2.5 Ideal Zener Diode

- For troubleshooting and preliminary analysis, we can approximate the breakdown region as vertical. Therefore, the voltage is constant even though the current changes, which is equivalent to ignoring the Zener resistance.
- Figure-3 shows the ideal approximation of a Zener diode. This means that a Zener diode operating in the breakdown region ideally acts like a battery.

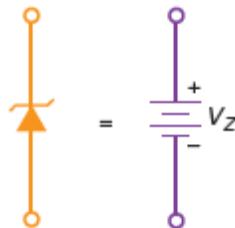


Figure-3 Ideal approximation of a Zener diode.

- In a circuit, it means that you can mentally replace a Zener diode by a voltage source of V_z , provided the Zener diode is operating in the breakdown region.

Example-1

Suppose the Zener diode of Figure-4a has a breakdown voltage of 10 V. What are the minimum and maximum Zener currents?

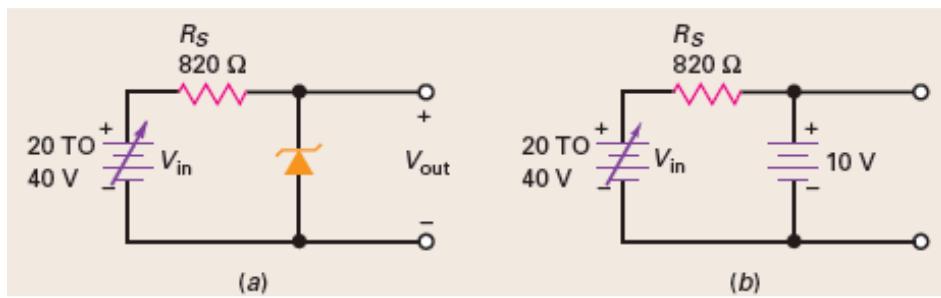


Figure-4 Example-1

SOLUTION

The applied voltage may vary from 20 to 40 V. Ideally, a Zener diode acts like the battery shown in Figure-4b. Therefore, the output voltage is 10 V for any source voltage between 20 and 40 V.

The minimum current occurs when the source voltage is minimum. Visualize 20 V on the left end of the resistor and 10 V on the right end. Then you can see that the voltage across the resistor is 20 V - 10 V, or 10 V. The rest is

Ohm's law:

$$I_S = \frac{10 \text{ V}}{820 \Omega} = 12.2 \text{ mA}$$

The maximum current occurs when the source voltage is 40 V. In this case, the voltage across the resistor is 30 V, which gives a current of

$$I_S = \frac{30 \text{ V}}{820 \Omega} = 36.6 \text{ mA}$$

In a voltage regulator like Figure-4a, the output voltage is held constant at 10 V, despite the change in source voltage from 20 to 40 V. The larger source voltage produces more Zener current, but the output voltage holds rock-solid at 10 V.

(If the Zener resistance is included, the output voltage increases slightly when the source voltage increases.)

PRACTICE PROBLEM -1

Using Figure-4, what is the Zener current I_S if $V_{in} = 30 \text{ V}$?

1.3 The Loaded Zener Regulator

- Figure-5a shows a loaded Zener regulator, and Figure-5b shows the same circuit with grounds. The Zener diode operates in the breakdown region and holds the load voltage constant. Even if the source voltage changes or the load resistance varies, the load voltage will remain fixed and equal to the Zener voltage.

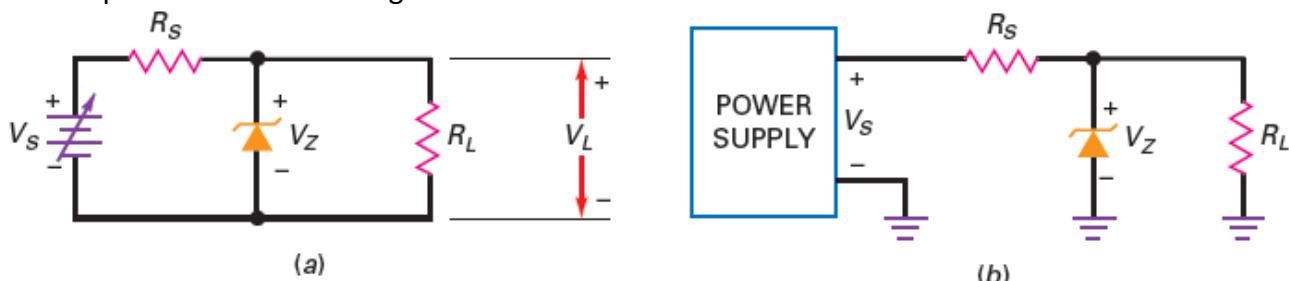


Figure-5 Loaded Zener regulator. (a) Basic circuit; (b) practical circuit

1.3.1 Breakdown Operation

- How can you tell whether the Zener diode of Figure-5 is operating in the breakdown region? Because of the voltage divider, the Thevenin voltage facing the diode is:

$$V_{TH} = \frac{R_L}{R_S + R_L} V_S \quad \text{--- (2)}$$

- This is the voltage that exists when the Zener diode is disconnected from the circuit. This Thevenin voltage has to be greater than the Zener voltage; otherwise, breakdown cannot occur.

1.3.2 Series Current

- Unless otherwise indicated, in all subsequent discussions we assume that the Zener diode is operating in the breakdown region. In Figure-5, the current through the series resistor is given by:

$$I_S = \frac{V_S - V_Z}{R_S}$$

- This is Ohm's law applied to the current-limiting resistor. It is the same whether or not there is a load resistor. In other words, if you disconnect the load resistor, the current through the series resistor still equals the voltage across the resistor divided by the resistance.

1.3.3 Load Current

- Ideally, the load voltage equals the Zener voltage because the load resistor is in parallel with the Zener diode. As an equation:

$$V_L = V_Z \quad \text{--- (3)}$$

- This allows us to use Ohm's law to calculate the load current:

$$I_L = \frac{V_L}{R_L} \quad \text{--- (4)}$$

1.3.4 Zener Current

- With Kirchhoff's current law:

$$I_S = I_Z + I_L \quad \text{--- (5)}$$

- The Zener diode and the load resistor are in parallel. The sum of their currents has to equal the total current, which is the same as the current through the series resistor.
- We can rearrange the foregoing equation to get this important formula:

$$I_Z = I_S - I_L \quad \text{--- (6)}$$

- This tells you that the Zener current no longer equals the series current, as it does in an unloaded Zener regulator. Because of the load resistor, the Zener current now equals the series current minus the load current.

1.3.5 Zener Effect

- When the breakdown voltage is greater than 6 V, the cause of the breakdown is the avalanche effect. The basic idea is that minority carriers are accelerated to high enough speeds to dislodge other minority carriers, producing a chain or avalanche effect that results in a large reverse current.

- The Zener effect is different. When a diode is heavily doped, the depletion layer becomes very narrow. Because of this, the electric field across the depletion layer (voltage divided by distance) is very intense.
- When the field strength reaches approximately 300,000 V/cm, the field is intense enough to pull electrons out of their valence orbits. The creation of free electrons in this way is called the Zener effect (also known as high-field emission).
- This is distinctly different from the avalanche effect, which depends on high-speed minority carriers dislodging valence electrons.
- When the breakdown voltage is less than 4 V, only the Zener effect occurs. When the breakdown voltage is greater than 6 V, only the avalanche effect occurs. When the breakdown voltage is between 4 and 6 V, both effects are present.
- The Zener effect was discovered before the avalanche effect, so all diodes used in the breakdown region came to be known as Zener diodes. Although you may occasionally hear the term avalanche diode, the name Zener diode is in general use for all breakdown diodes.

Example-2

Is the Zener diode of Figure-6a operating in the breakdown region?

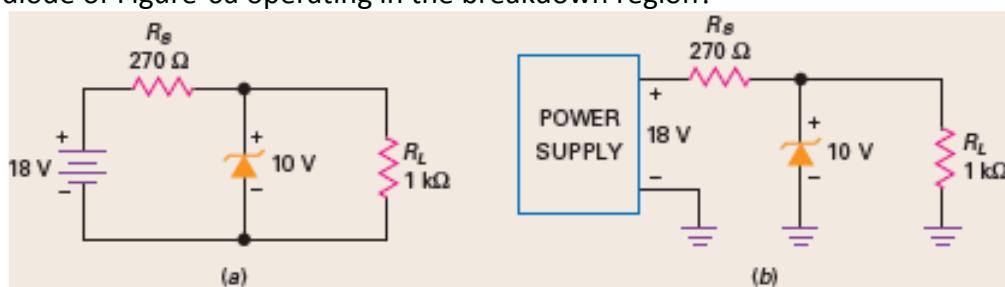


Figure-6 Example-2

SOLUTION

With Eq. (2):

$$V_{TH} = \frac{1 \text{ k}\Omega}{270 \Omega + 1 \text{ k}\Omega} (18 \text{ V}) = 14.2 \text{ V}$$

Since this Thevenin voltage is greater than the Zener voltage, the Zener diode is operating in the breakdown region.

Example-3

What does the Zener current equal in Figure-6b?

SOLUTION

You are given the voltage on both ends of the series resistor. Subtract the voltages, and you can see that 8 V is across the series resistor. Then Ohm's law gives:

$$I_S = \frac{8 \text{ V}}{270 \Omega} = 29.6 \text{ mA}$$

Since the load voltage is 10 V, the load current is:

$$I_L = \frac{10 \text{ V}}{1 \text{ k}\Omega} = 10 \text{ mA}$$

The Zener current is the difference between the two currents:

$$I_Z = I_S - I_L = 29.6 \text{ mA} - 10 \text{ mA} = 19.6 \text{ mA}$$

PRACTICE PROBLEM 5-3

Using Figure-6b, change the power supply to 15 V and calculate I_s , I_L , and I_z .

1.4 Light-Emitting Diodes (LEDs)

- Optoelectronics is the technology that combines optics and electronics. This field includes many devices based on the action of a pn junction. Examples of optoelectronic devices are light-emitting diodes (LEDs), photodiodes, optocouplers, and laser diodes. Our discussion begins with the LED.

1.4.1 Light-Emitting Diode

- LEDs have replaced incandescent lamps in many applications because of the LED's lower energy consumption, smaller size, faster switching and longer lifetime.
- Figure-7 shows the parts of a standard low-power LED. Just as in an ordinary diode, the LED has an anode and a cathode that must be properly biased.
- The outside of the plastic case typically has a flat spot on one side which indicates the cathode side of the LED. The material used for the semiconductor die will determine the LED's characteristics.

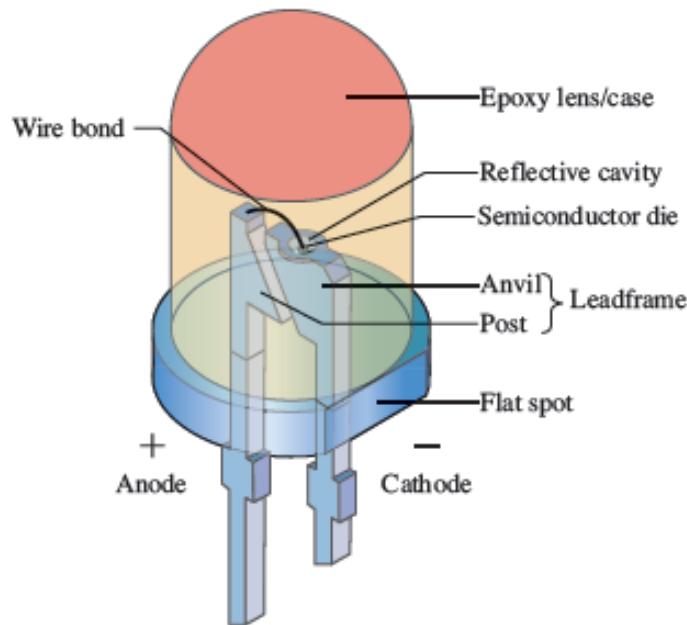


Figure-7 Parts of an LED

- Figure-8a shows a source connected to a resistor and an LED. The outward arrows symbolize the radiated light. In a forward-biased LED, free electrons cross the pn junction and fall into holes.
- As these electrons fall from a higher to a lower energy level, they radiate energy in the form of photons.
- In ordinary diodes, this energy is radiated in the form of heat. But in an LED, the energy is radiated as light. This effect is referred to as electroluminescence.
- The color of the light, which corresponds to the wavelength energy of the photons, is primarily determined by the energy band gap of the semiconductor materials that are used.

- By using elements like gallium, arsenic, and phosphorus, a manufacturer can produce LEDs that radiate red, green, yellow, blue, orange, white or infrared (invisible) light.
 - LEDs that produce visible radiation are useful as indicators in applications such as instrumentation panels, internet routers, and so on.
 - The infrared LED finds applications in security systems, remote controls, industrial control systems, and other areas requiring invisible radiation.

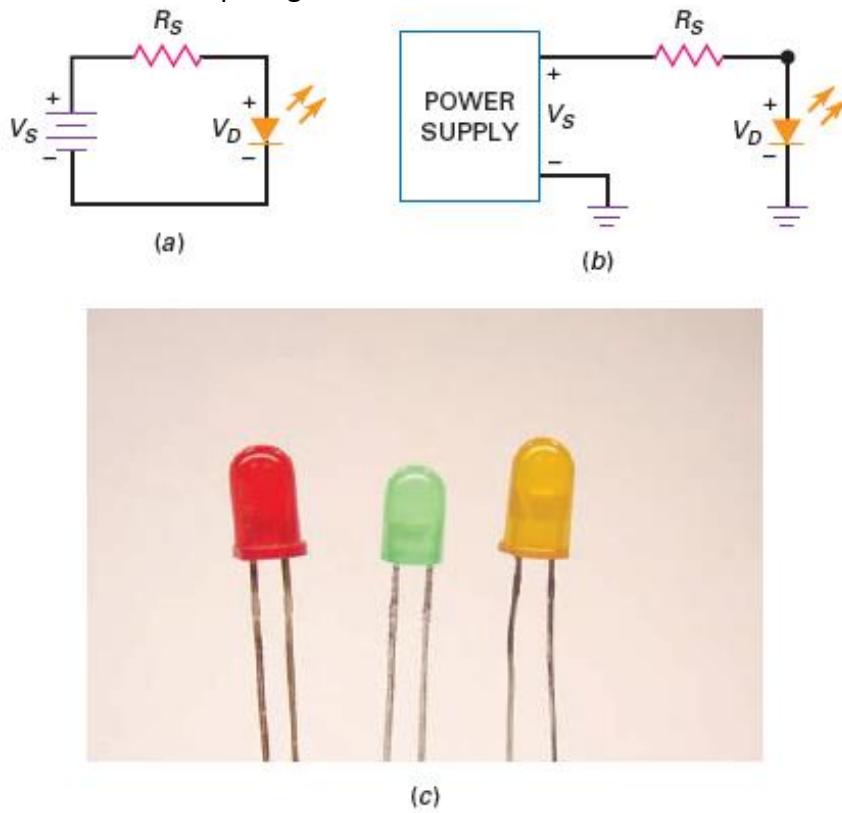


Figure-8 LED indicator. (a) Basic circuit; (b) practical circuit; (c) typical LEDs

1.4.2 LED Voltage and Current

- The resistor of Figure-8b is the usual current-limiting resistor that prevents the current from exceeding the maximum current rating of the diode. Since the resistor has a node voltage of V_s on the left and a node voltage of V_D on the right, the voltage across the resistor is the difference between the two voltages. With Ohm's law, the series current is:

$$I_S = \frac{V_S - V_D}{R_S} \quad \dots \quad (7)$$

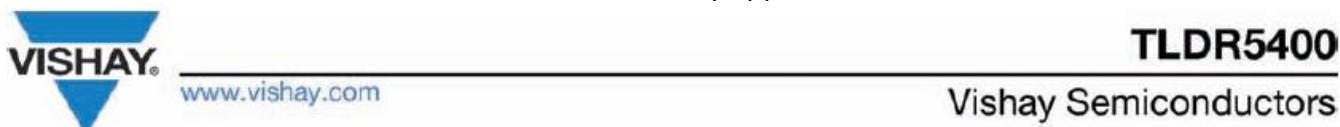
- For most commercially available low-power LEDs, the typical voltage drop is from 1.5 to 2.5 V for currents between 10 and 50 mA. The exact voltage drop depends on the LED current, color, tolerance, along with other factors.
 - Unless otherwise specified, we will use a nominal drop of 2 V when troubleshooting or analyzing low-power LED circuits in this book. Figure-8c shows typical low-power LEDs with housings made to help radiate the respective color.

1.4.3 LED Brightness

- The brightness of an LED depends on the current. The amount of light emitted is often specified as its luminous intensity I_V and is rated in candelas (**cd**).
- Low-power LEDs generally have their ratings given in millicandolas (**mcd**). For instance, a TLDR5400 is a red LED with a forward voltage drop of 1.8 V and an I_V rating of 70 mcd at 20 mA. The luminous intensity drops to 3 mcd at a current of 1 mA. When V_S is much greater than V_D in Eq. (7), the brightness of the LED is approximately constant.
- If a circuit like Figure-8b is mass-produced using a TLDR5400, the brightness of the LED will be almost constant if V_S is much greater than V_D . If V_S is only slightly more than V_D , the LED brightness will vary noticeably from one circuit to the next.
- The best way to control the brightness is by driving the LED with a current source. This way, the brightness is constant because the current is constant.
- When we discuss transistors (they act like current sources), we will show how to use a transistor to drive an LED.

1.4.4 LED Specifications and Characteristics

- A partial datasheet of a standard TLDR5400 5 mm T-1¾ red LED is shown in Figure-9. This type of LED has thru-hole leads and can be used in many applications.



High Intensity LED, Ø 5 mm Tinted Diffused Package



19220

APPLICATIONS

- Bright ambient lighting conditions
- Battery powered equipment
- Indoor and outdoor information displays
- Portable equipment
- Telecommunication indicators
- General use

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^\circ\text{C}$, unless otherwise specified)

TLDR5400

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage ⁽¹⁾		V_R	6	V
DC forward current		I_F	50	mA
Surge forward current	$t_p \leq 10 \mu\text{s}$	I_{FSM}	1	A
Power dissipation		P_V	100	mW
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	- 40 to + 100	°C

Note

⁽¹⁾ Driving the LED in reverse direction is suitable for a short term application

OPTICAL AND ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified) TLDR5400, RED						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Luminous intensity	$I_F = 20 \text{ mA}$	I_V	35	70	-	mcd
Luminous intensity	$I_F = 1 \text{ mA}$	I_V	-	3	-	mcd
Dominant wavelength	$I_F = 20 \text{ mA}$	λ_d	-	648	-	nm
Peak wavelength	$I_F = 20 \text{ mA}$	λ_p	-	650	-	nm
Spectral line half width		$\Delta\lambda$	-	20	-	nm
Angle of half intensity	$I_F = 20 \text{ mA}$	ϕ	-	± 30	-	deg
Forward voltage	$I_F = 20 \text{ mA}$	V_F	-	1.8	2.2	V
Reverse current	$V_R = 6 \text{ V}$	I_R	-	-	10	μA
Junction capacitance	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$	C_j	-	30	-	pF

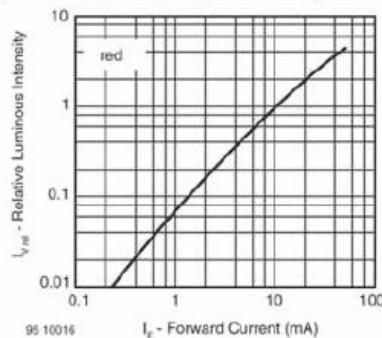


Fig. 6 - Relative Luminous Intensity vs. Forward Current

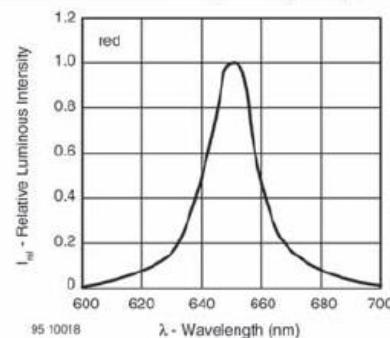


Fig. 4 - Relative Intensity vs. Wavelength

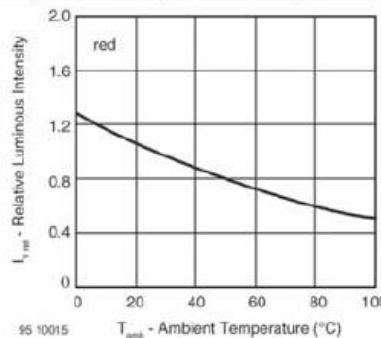


Fig. 8 - Relative Luminous Intensity vs. Ambient Temperature

Figure-9 TLDR5400 Partial Datasheet. Datasheets courtesy of Vishay Intertechnology

- The Absolute Maximum Rating table specifies that the LED's maximum forward current I_F is 50 mA and its maximum reverse voltage is only 6 V. To extend the life of this device, be sure to use an appropriate safety factor.
- The LED's maximum power rating is 100 mW at an ambient temperature of 25°C and must be derated at higher temperatures.
- The Optical and Electrical Characteristics table indicates that this LED has a typical luminous intensity I_V of 70 mcd at 20 mA and drops to 3 mcd at 1 mA. Also specified in this table, the dominant wavelength of the red LED is 648 nanometers and the light intensity drops off to approximately 50 percent when viewed at a 30° angle.
- The Relative Luminous Intensity versus Forward Current graph displays how the light intensity is effected by the LED's forward current.
- The graph of Relative Luminous Intensity versus Wavelength visually displays how the luminous intensity reaches a peak at a wavelength of approximately 650 nanometers. What happens when the ambient temperature of the LED increases or decreases?
- The graph of Relative Luminous Intensity versus Ambient Temperature shows that an increase in ambient temperature has a substantial negative effect on the LED's light output. This becomes important when LEDs are used in applications with large temperature variations.

1.4.5 High-Power LEDs

- Typical power dissipation levels of the LEDs discussed up to this point are in the low milliwatt range.

- As an example, the TLDR5400 LED has a maximum power rating of 100 mW and generally operates at approximately 20 mA with a typical forward voltage drop of 1.8 V. This results in a power dissipation of 36 mW.
- High-power LEDs are now available with continuous power ratings of 1 W and above. These power LEDs can operate in the hundreds of mAs to over 1 A of current. An increasing array of applications are being developed including automotive interior, exterior, and forward lighting, architectural indoor and outdoor area lighting, along with digital imaging and display backlighting.
- Figure-10 shows an example of a high-power LED emitter that has the benefit of high luminance for directional applications such as down lights and indoor area lighting.



Figure-10 LUXEON TX High-Power Emitter

- LEDs, such as this, use much larger semiconductor die sizes to handle the large power inputs. Because this device will need to dissipate over 1 W of power, it is critical to use proper mounting techniques to a heat sink. Otherwise, the LED will fail within a short period of time.
- Efficiency of a light source is an essential factor in most applications. Because an LED produces both light and heat, it is important to understand how much electrical power is used to produce the light output.
- A term used to describe this is called luminous efficacy. Luminous efficacy of a source is the ratio of output luminous flux (lm) to electrical power (W) given in lm/W.
- Figure-11 shows a partial table for LUXEON TX high-power LED emitters giving their typical performance characteristics.
- Notice that the performance characteristics are rated at 350 mA, 700 mA, and 1,000 mA. With a test current of 700 mA, the LIT2-30700000000000 emitter has a typical luminous flux output of 245 lm.
- At this forward current level, the typical forward voltage drop is 2.80 V. Therefore, the amount of power dissipated is

$$P_D = I_F \times V_F = 700 \text{ mA} \times 2.8 \text{ V} = 1.96 \text{ W}$$

- The efficacy value for this emitter would be found by:

$$\text{Efficacy} = \frac{\text{lm}}{\text{W}} = \frac{245 \text{ lm}}{1.96 \text{ W}} = 125 \text{ lm/W}$$

- As a comparison, the luminous efficacy of a typical incandescent bulb is 16 lm/W and a compact fluorescent bulb has a typical rating of 60 lm/W. When looking at the overall efficiency of these types of LEDs, it is important to note that electronic circuits, called drivers, are required to control the LED's current and light output. Since these drivers also use electrical power, the overall system efficiency is reduced.

Product Selection Guide for LUXEON TX Emitters, Junction Temperature = 85°C

Table I.

Base Part Number	Nominal ANSI CCT	Typical Performance Characteristics											
		Min CRI	Min Luminous Flux (lm)	Typical Luminous Flux (lm)			Typical Forward Voltage (V)			Typical Efficacy (lm/W)			
			700 mA	700 mA	350 mA	700 mA	1000 mA	350 mA	700 mA	1000 mA	350 mA	700 mA	1000 mA
LIT2-30700000000000	3000K	70	230	135	245	327	2.71	2.80	2.86	142	125	114	
LIT2-40700000000000	4000K	70	250	147	269	360	2.71	2.80	2.86	155	137	126	
LIT2-50700000000000	5000K	70	260	151	275	369	2.71	2.80	2.86	159	140	129	
LIT2-57700000000000	5700K	70	260	151	275	369	2.71	2.80	2.86	159	140	129	
LIT2-65700000000000	6500K	70	260	151	275	369	2.71	2.80	2.86	159	140	129	
LIT2-27800000000000	2700K	80	200	118	216	289	2.71	2.80	2.86	124	110	101	
LIT2-30800000000000	3000K	80	210	124	227	304	2.71	2.80	2.86	131	116	106	
LIT2-35800000000000	3500K	80	220	130	238	319	2.71	2.80	2.86	137	121	112	
LIT2-40800000000000	4000K	80	230	136	247	331	2.71	2.80	2.86	143	126	116	
LIT2-50800000000000	5000K	80	230	135	247	332	2.71	2.80	2.86	142	126	116	

Notes for Table I:

I. Philips Lumileds maintains a tolerance of $\pm 6.5\%$ on luminous flux and ± 2 on CRI measurements.

Courtesy of Philips Lumileds

Figure-11 Partial data sheet for LUXEON TX emitters

1.5 Other Optoelectronic Devices

- Besides standard low-power through high-power LEDs, there are many other optoelectronic devices which are based on the photonic action of a pn junction.
- These devices are used to source, detect and control light in an enormous variety of electronic applications.

1.5.1 Seven-Segment Display

- Figure-12a shows a seven-segment display. It contains seven rectangular LEDs (A through G). Each LED is called a segment because it forms part of the character being displayed. Figure-12b is a schematic diagram of the seven-segment display. External series resistors are included to limit the currents to safe levels.
- By grounding one or more resistors, we can form any digit from 0 through 9. For instance, by grounding A, B, and C, we get a 7. Grounding A, B, C, D, and G produces a 3.
- A seven-segment display can also display capital letters A, C, E, and F, plus lowercase letters b and d. Microprocessor trainers often use seven-segment displays that show all digits from 0 through 9, plus A, b, C, d, E, and F.

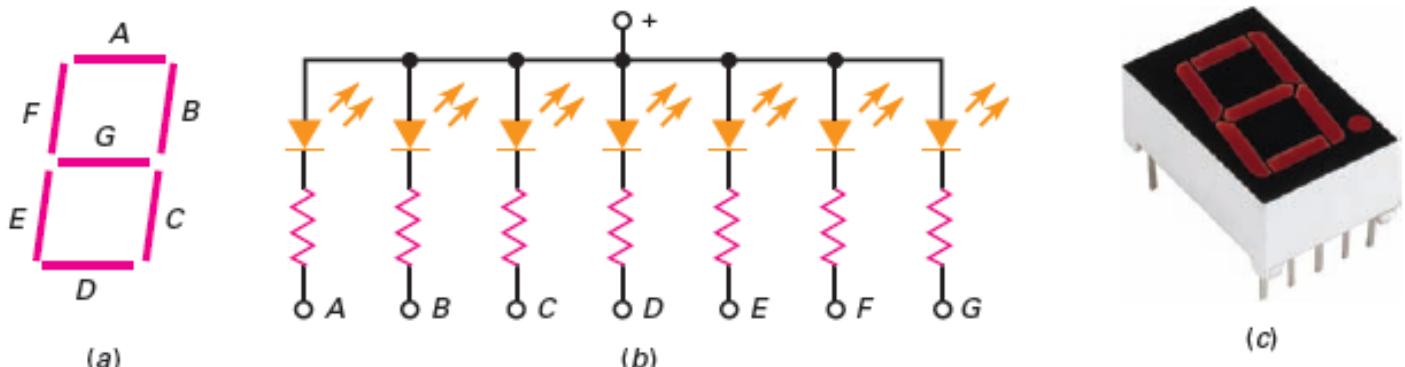


Figure-12 Seven-segment indicator. (a) Physical layout of segments; (b) schematic diagram; (c) Actual display with decimal point. Courtesy of Fairchild Semiconductor

- The seven-segment indicator of Figure-12b is referred to as the common-anode type because all anodes are connected together. Also available is the common-cathode type, in which all cathodes are connected together.
- Figure-12c shows an actual seven-segment display with pins for fitting into a socket or for soldering to a printed-circuit board. Notice the extra dot segment used for a decimal point.

1.5.2 Photodiode

- As previously discussed, one component of reverse current in a diode is the flow of minority carriers. These carriers exist because thermal energy keeps dislodging valence electrons from their orbits, producing free electrons and holes in the process.
- The lifetime of the minority carriers is short, but while they exist, they can contribute to the reverse current. When light energy bombards a pn junction, it can dislodge valence electrons. The more light striking the junction, the larger the reverse current in a diode.
- A photodiode has been optimized for its sensitivity to light. In this diode, a window lets light pass through the package to the junction. The incoming light produces free electrons and holes. The stronger the light, the greater the number of minority carriers and the larger the reverse current.
- Figure-13 shows the schematic symbol of a photodiode. The arrows represent the incoming light. Especially important, the source and the series resistor reverse-bias the photodiode. As the light becomes brighter, the reverse current increases. With typical photodiodes, the reverse current is in the tens of microamperes.

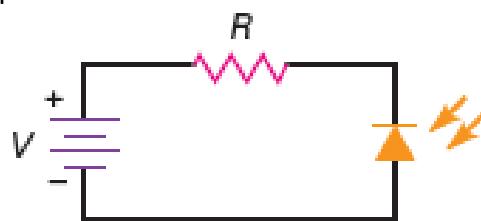


Figure-13 Incoming light increases reverse current in photodiode

1.5.3 Optocoupler

- An Optocoupler (also called an optoisolator) combines an LED and a photodiode in a single package. Figure-14 shows an Optocoupler.

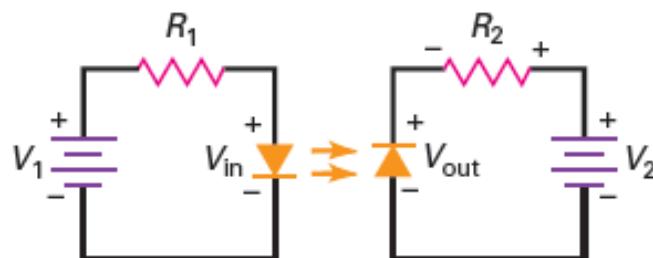


Figure-14 Optocoupler combines an LED and a photodiode

- It has an LED on the input side and a photodiode on the output side. The left source voltage and the series resistor set up a current through the LED. Then the light from the LED hits the photodiode, and this sets up a reverse current in the output circuit.
- This reverse current produces a voltage across the output resistor. The output voltage then equals the output supply voltage minus the voltage across the resistor.
- When the input voltage is varying, the amount of light is fluctuating. This means that the output voltage is varying in step with the input voltage. This is why the combination of an LED and a photodiode is called an Optocoupler.
- The device can couple an input signal to the output circuit. Other types of optocouplers use phototransistors, photo-thyristors, and other photo devices in their output circuit side.
- The key advantage of an Optocoupler is the electrical isolation between the input and output circuits. With an Optocoupler, the only contact between the input and the output is a beam of light. Because of this, it is possible to have an insulation resistance between the two circuits in the thousands of mega-ohms.
- Isolation like this is useful in high-voltage applications in which the potentials of the two circuits may differ by several thousand volts.

1.6 The Schottky Diode

- As frequency increases, the action of small-signal rectifier diodes begins to deteriorate. They are no longer able to switch off fast enough to produce a well-defined half-wave signal. The solution to this problem is the Schottky diode.
- Before describing this special-purpose diode, let us look at the problem that arises with ordinary small-signal diodes.

1.6.1 Charge Storage

- Figure-15a shows a small-signal diode, and Figure-15b illustrates its energy bands. As you can see, conduction-band electrons have diffused across the junction and traveled into the p region before recombining (path A).
- Similarly, holes have crossed the junction and traveled into the n region before recombination occurs (path B). The greater the lifetime, the farther the charges can travel before recombination occurs.
- For instance, if the lifetime equals $1 \mu s$, free electrons and holes exist for an average of $1 \mu s$ before recombination takes place. This allows the free electrons to penetrate deeply into the p region, where they remain temporarily stored at the higher energy band.

- Similarly, the holes penetrate deeply into the n region, where they are temporarily stored in the lower energy band.

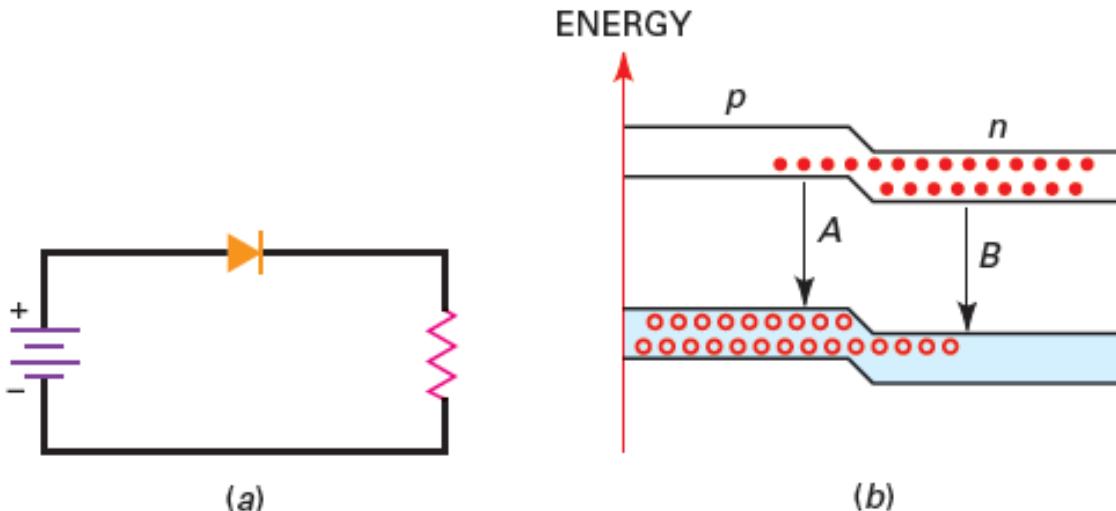


Figure-15 Charge storage. (a) Forward bias creates stored charges; (b) stored charges in high and low energy bands

- The greater the forward current, the larger the number of charges that have crossed the junction. The greater the lifetime, the deeper the penetration of these charges and the longer the charges remain in the high and low energy bands.
- The temporary storage of free electrons in the upper energy band and holes in the lower energy band is referred to as charge storage.

1.6.2 Charge Storage Produces Reverse Current

- When you try to switch a diode from on to off, charge storage creates a problem. Why? Because if you suddenly reverse-bias a diode, the stored charges will flow in the reverse direction for a while.
- The greater the lifetime, the longer these charges can contribute to reverse current. For example, suppose a forward-biased diode is suddenly reverse biased, as shown in Figure-16a.

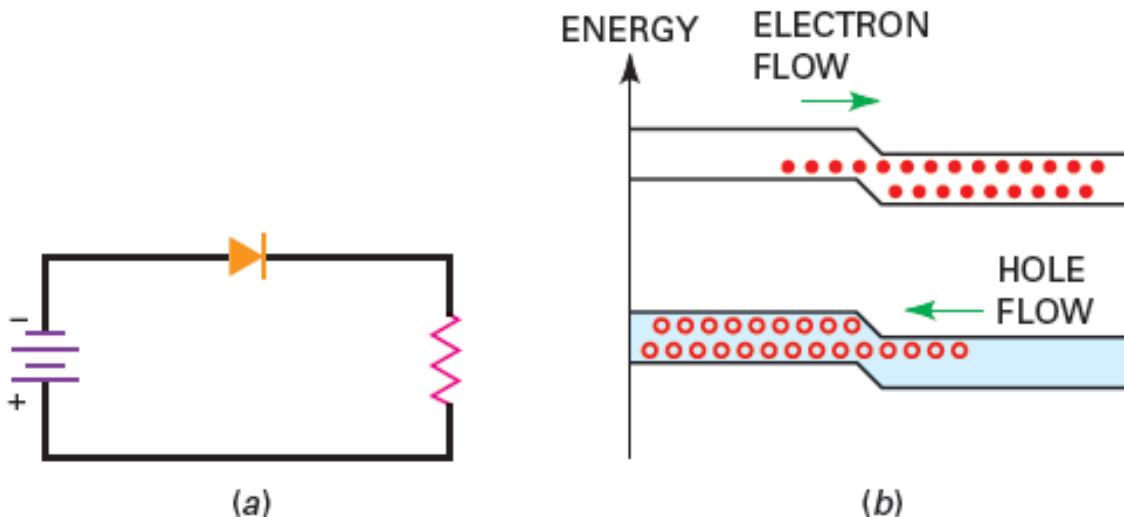


Figure-16 Stored charges allow a brief reverse current. (a) Sudden reversal of source voltage; (b) flow of stored charges in reverse direction

- Then a large reverse current can exist for a while because of the flow of stored charges in Figure-16b. Until the stored charges either cross the junction or recombine, the reverse current will continue.

1.6.3 Reverse Recovery Time

- The time it takes to turn off a forward-biased diode is called the reverse recovery time t_{rr} . The conditions for measuring t_{rr} vary from one manufacturer to the next.
- As a guide, t_{rr} is the time it takes for the reverse current to drop to 10 percent of the forward current.
- For instance, the 1N4148 has a t_{rr} of 4 ns. If this diode has a forward current of 10 mA and it is suddenly reverse biased, it will take approximately 4 ns for the reverse current to decrease to 1 mA. Reverse recovery time is so short in small-signal diodes that you don't even notice its effect at frequencies below 10 MHz or so. It's only when you get well above 10 MHz that you have to take t_{rr} into account.

1.6.4 Poor Rectification at High Frequencies

- What effect does reverse recovery time have on rectification? Take a look at the half-wave rectifier shown in Figure-17a.

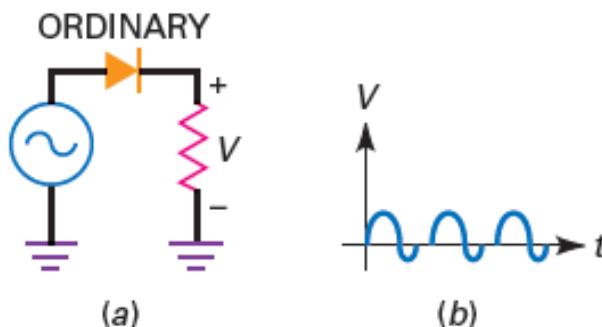


Figure-17 Stored charges degrade rectifier behavior at high frequencies. (a) Rectifier circuit with ordinary small-signal diode; (b) tails appear on negative half-cycles at higher frequencies

- At low frequencies, the output is a half-wave rectified signal. As the frequency increases well into megahertz, however, the output signal begins to deviate from the half-wave shape, as shown in Figure-17b.
- Some reverse conduction (called tails) is noticeable near the beginning of the reverse half-cycle. The problem is that the reverse recovery time has become a significant part of the period, allowing conduction during the early part of the negative half-cycle.
- For instance, if $t_{rr} = 4$ ns and the period is 50 ns, the early part of the reverse half-cycle will have tails similar to those shown in Figure-17b. As the frequency continues to increase, the rectifier becomes useless.

1.6.5 Eliminating Charge Storage

- The solution to the problem of tails is a special-purpose device called a Schottky diode. This kind of diode uses a metal such as gold, silver, or platinum on one side of the junction and doped silicon (typically n-type) on the other side.

- Because of the metal on one side of the junction, the Schottky diode has no depletion layer. The lack of a depletion layer means that there are no stored charges at the junction.
- When a Schottky diode is unbiased, free electrons on the n side are in smaller orbits than are the free electrons on the metal side. This difference in orbit size is called the Schottky barrier, approximately 0.25 V.
- When the diode is forward biased, free electrons on the n side can gain enough energy to travel in larger orbits. Because of this, free electrons can cross the junction and enter the metal, producing a large forward current. Since the metal has no holes, there is no charge storage and no reverse recovery time.

1.6.6 Hot-Carrier Diode

- The Schottky diode is sometimes called a hot-carrier diode. This name came about as follows. Forward bias increases the energy of the electrons on the n side to a higher level than that of the electrons on the metal side of the junction.
- This increase in energy inspired the name hot carrier for the n-side electrons. As soon as these high-energy electrons cross the junction, they fall into the metal, which has a lower-energy conduction band.

1.6.7 High-Speed Turnoff

- The lack of charge storage means that the Schottky diode can switch off faster than an ordinary diode can. In fact, a Schottky diode can easily rectify frequencies above 300 MHz. When it is used in a circuit like Figure-18a, the Schottky diode produces a perfect half-wave signal like Figure-18b even at frequencies above 300 MHz.

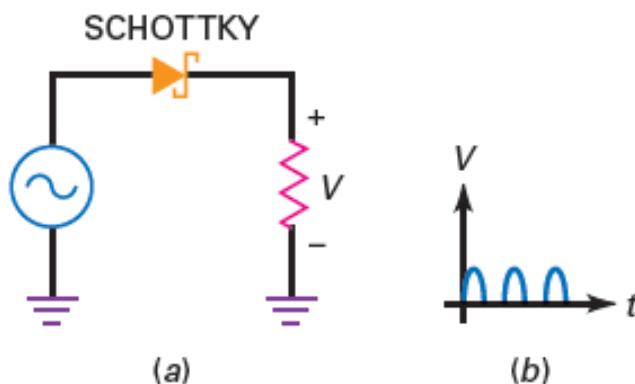


Figure-18 Schottky diodes eliminate tails at high frequencies. (a) Circuit with Schottky diode; (b) half-wave signal at 300 MHz

- Figure-18a shows the schematic symbol of a Schottky diode. Notice the cathode side. The lines look like a rectangular S, which stands for Schottky. This is how you can remember the schematic symbol.

1.6.8 Applications

- The most important application of Schottky diodes is in digital computers. The speed of computers depends on how fast their diodes and transistors can turn on and off. This is where the Schottky diode comes in.

- Because it has no charge storage, the Schottky diode has become the backbone of low-power Schottky TTLs, a group of widely used digital devices.
- A final point. Since a Schottky diode has a barrier potential of only 0.25 V, you may occasionally see it used in low-voltage bridge rectifiers because you subtract only 0.25 V instead of the usual 0.7 V for each diode when using the second approximation. In a low-voltage supply, this lower diode voltage drop is an advantage.

1.7 The Varactor

- The Varactor (also called the voltage-variable capacitance, varicap, epicap, and tuning diode) is widely used in television receivers, FM receivers, and other communications equipment because it can be used for electronic tuning.

1.7.1 Basic Idea

- In Figure-19a, the depletion layer is between the p region and the n region. The p and n regions are like the plates of a capacitor, and the depletion layer is like the dielectric.
- When a diode is reverse biased, the width of the depletion layer increases with the reverse voltage. Since the depletion layer gets wider with more reverse voltage, the capacitance becomes smaller.
- It's as though you moved apart the plates of a capacitor. The key idea is that capacitance is controlled by reverse voltage.

1.7.2 Equivalent Circuit and Symbol

- Figure-19b shows the ac-equivalent circuit for a reverse-biased diode. In other words, as far as an ac signal is concerned, the Varactor acts the same as a variable capacitance.
- Figure-19c shows the schematic symbol for a Varactor. The inclusion of a capacitor in series with the diode is a reminder that a Varactor is a device that has been optimized for its variable-capacitance properties.

1.7.3 Capacitance Decreases at Higher Reverse Voltages

- Figure-19d shows how the capacitance varies with reverse voltage. This graph shows that the capacitance gets smaller when the reverse voltage gets larger.

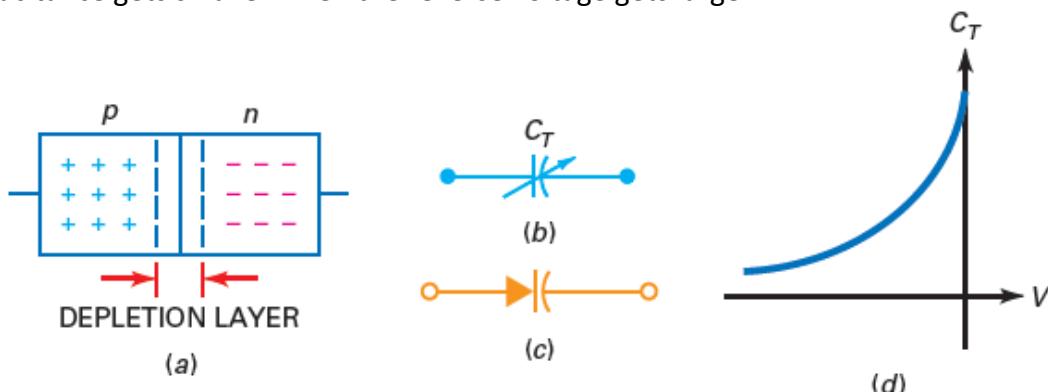


Figure-19 Varactor.(a) Doped regions are like capacitor plates separated by a dielectric; (b) ac-equivalent circuit; (c) schematic symbol; (d) graph of capacitance versus reverse voltage

- The really important idea here is that reverse dc voltage controls capacitance. How is a Varactor used? It is connected in parallel with an inductor to form a parallel resonant circuit. This circuit has only one frequency at which maximum impedance occurs. This frequency is called the resonant frequency.
- If the dc reverse voltage to the Varactor is changed, the resonant frequency is also changed. This is the principle behind electronic tuning of a radio station, a TV channel, and so on.

1.7.4 Varactor Characteristics

- Because the capacitance is voltage controlled, Varactors have replaced mechanically tuned capacitors in many applications such as television receivers and automobile radios. Data sheets for Varactors list a reference value of capacitance measured at a specific reverse voltage, typically 23 V to 24 V.
- Figure-20 shows a partial data sheet for an MV209 Varactor diode. It lists a reference capacitance C_t of 29 pF at -3 V.

	C_t , Diode Capacitance $V_R = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$ pF			Q , Figure of Merit $V_R = 3.0 \text{ Vdc}$ $f = 50 \text{ MHz}$	C_R , Capacitance Ratio C_3/C_{25} $f = 1.0 \text{ MHz}$ (Note 1)	
Device	Min	Nom	Max	Min	Min	Max
MMBV109LT1, MV209	26	29	32	200	5.0	6.5

1. C_R is the ratio of C_t measured at 3 Vdc divided by C_t measured at 25 Vdc.

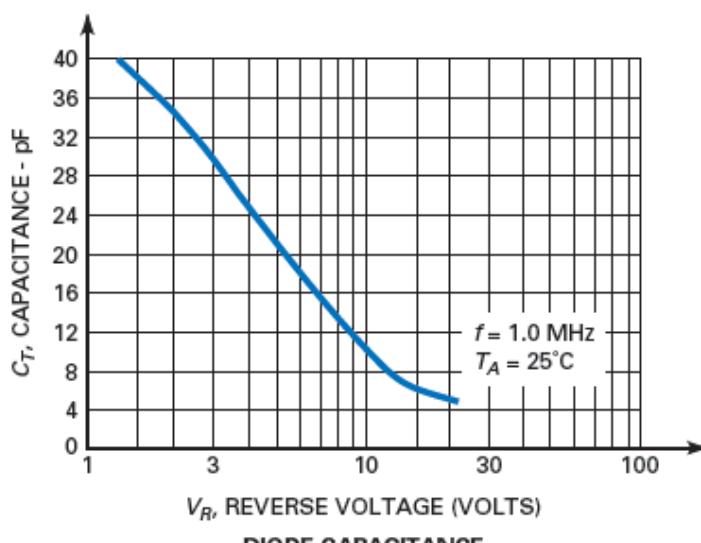


Figure-20 MV209 Partial Data Sheet. (Used with permission from SCILLC dba ON Semiconductor.)

- In addition to providing the reference value of capacitance, data sheets normally list a capacitance ratio C_R , or tuning range associated with a voltage range.
- For example, along with the reference value of 29 pF, the data sheet of an MV209 shows a minimum capacitance ratio of 5:1 for a voltage range of -3 V to -25 V.

- This means that the capacitance, or tuning range, decreases from 29 to 6 pF when the voltage varies from -3 V to -25 V. The tuning range of a Varactor depends on the doping level.
- For instance, Figure-21a shows the doping profile for an abrupt-junction diode (the ordinary type of diode).

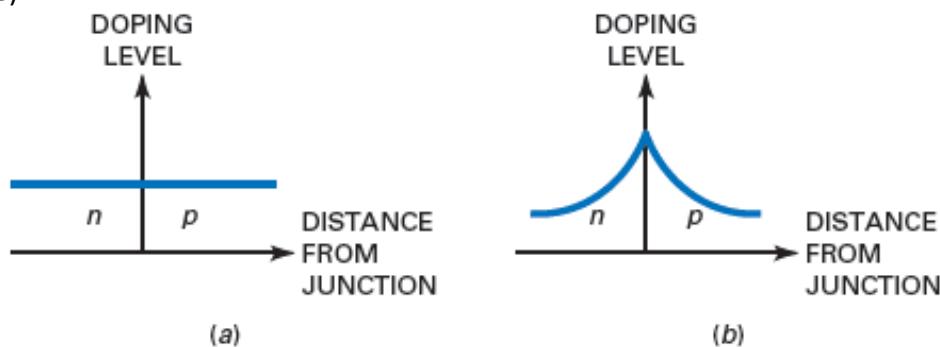


Figure-21 Doping profiles. (a) Abrupt junction; (b) hyper abrupt junction

- The profile shows that the doping is uniform on both sides of the junction. The tuning range of an abrupt-junction diode is between 3:1 and 4:1. To get larger tuning ranges, some Varactors have a hyper abrupt junction, one whose doping profile looks like Figure-21b.
- This profile tells us that the doping level increases as we approach the junction. The heavier doping produces a narrower depletion layer and a larger capacitance.
- Furthermore, changes in reverse voltage have more pronounced effects on capacitance. A hyper abrupt Varactor has a tuning range of about 10:1, enough to tune an AM radio through its frequency range of 535 to 1605 kHz. (Note: You need a 10:1 range because the resonant frequency is inversely proportional to the square root of capacitance.)

1.8 Other Diodes

- Besides the special-purpose diodes discussed so far, there are others you should know about. Because they are so specialized, only a brief description follows.

1.8.1 Varistors

- Lightning, power-line faults, and transients can pollute the ac line voltage by superimposing dips and spikes on the normal 120 V rms. Dips are severe voltage drops lasting microseconds or less. Spikes are very brief over voltages up to 2000 V or more.
- In some equipment, filters are used between the power line and the primary of the transformer to eliminate the problems caused by ac line transients. One of the devices used for line filtering is the Varistor (also called a transient suppressor).
- This semiconductor device is like two back-to-back Zener diodes with a high breakdown voltage in both directions. Varistors are commercially available with breakdown voltages from 10 to 1000 V. They can handle peak transient currents in the hundreds or thousands of amperes.
- For instance, a V130LA2 is a Varistor with a breakdown voltage of 184 V (equivalent to 130 V rms) and a peak current rating of 400 A. Connect one of these across the primary winding as shown in Figure-22, and you don't have to worry about spikes. The Varistor will clip all spikes at the 184-V level and protect your power supply.

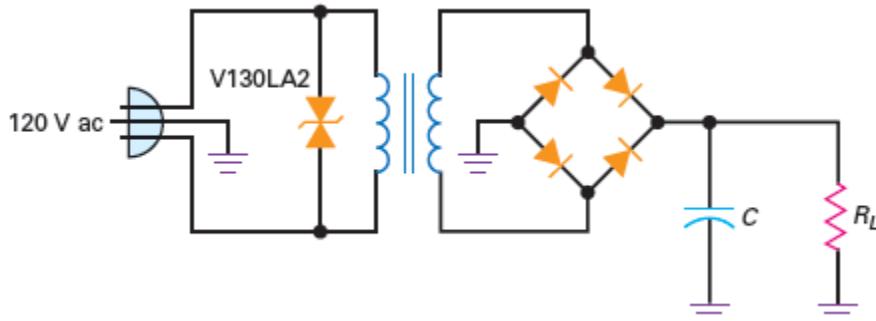


Figure-22 Varistor protects primary from ac line transients

1.8.2 Tunnel Diodes

- By increasing the doping level of a back diode, we can get breakdown to occur at 0 V. Furthermore, the heavier doping distorts the forward curve, as shown in Figure-23a.

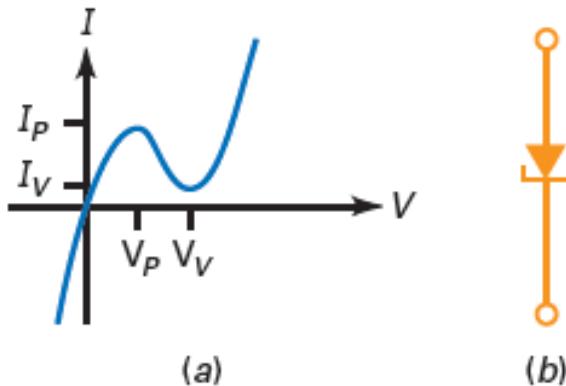


Figure-23 Tunnel diode. (a) Breakdown occurs at 0 V; (b) schematic symbol

- A diode with this graph is called a tunnel diode. Figure-23b shows the schematic symbol for a tunnel diode. This type of diode exhibits a phenomenon known as negative resistance.
- This means that an increase in forward voltage produces a decrease in forward current, at least over the part of the graph between V_P and V_V . The negative resistance of tunnel diodes is useful in high-frequency circuits called oscillators.
- These circuits are able to generate a sinusoidal signal, similar to that produced by an ac generator. But unlike the ac generator that converts mechanical energy to a sinusoidal signal, an oscillator converts dc energy to a sinusoidal signal.

1.8.3 PIN Diodes

- A PIN diode is a semiconductor device that operates as a variable resistor at RF and microwave frequencies. Figure-24a shows its construction. It consists of an intrinsic (pure) semiconductor material sandwiched between p-type and n-type materials.
- Figure-24b shows the schematic symbol for the PIN diode. When the diode is forward biased, it acts like a current-controlled resistance.
- Figure-24c shows how the PIN diode's series resistance R_S decreases as its forward current increases. When reverse biased, the PIN diode acts like a fixed capacitor. The PIN diode is widely used in modulator circuits for RF and microwave applications.

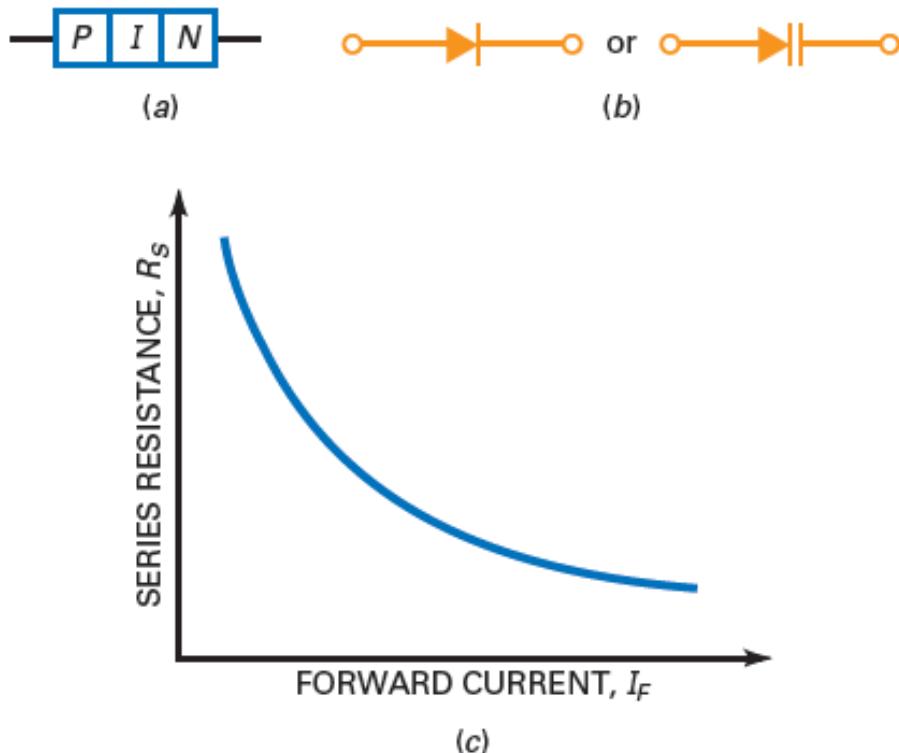


Figure-24 PIN diode. (a) Construction; (b) schematic symbol; (c) series resistance

1.9 Solar Cells

- In recent years, there has been increasing interest in the solar cell as an alternative source of energy. When we consider that the power density received from the sun at sea level is about 100 mW/cm² (1 kW/m²), it is certainly an energy source that requires further research and development to maximize the conversion efficiency from solar to electrical energy.
- The basic construction of a silicon p-n junction solar cell appears in figure-25. As shown in the top view, every effort is made to ensure that the surface area perpendicular to the sun is a maximum.

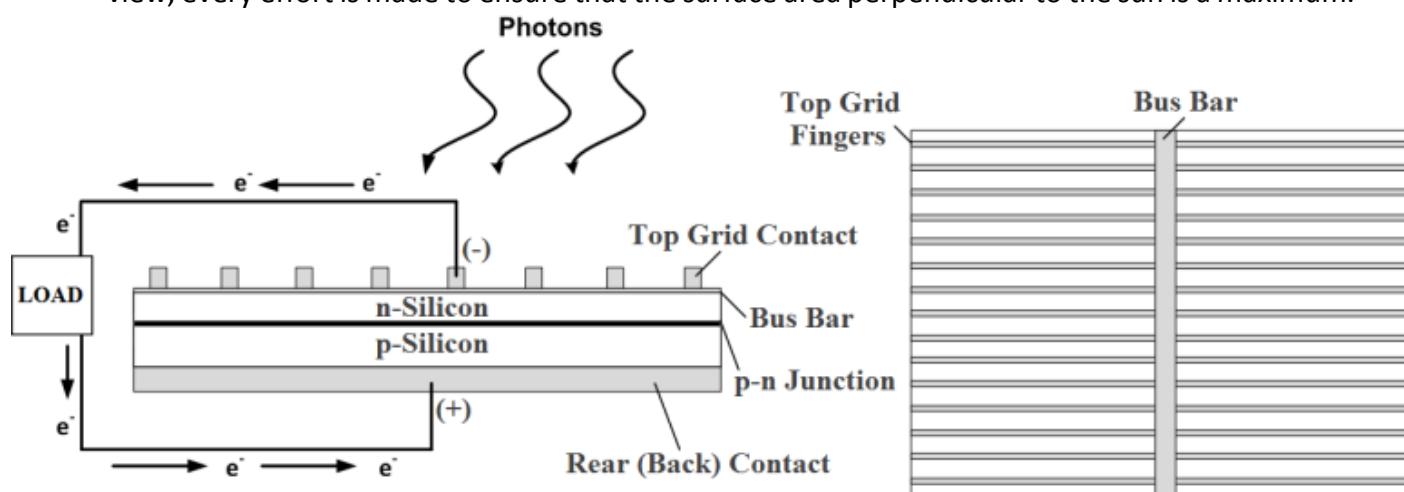
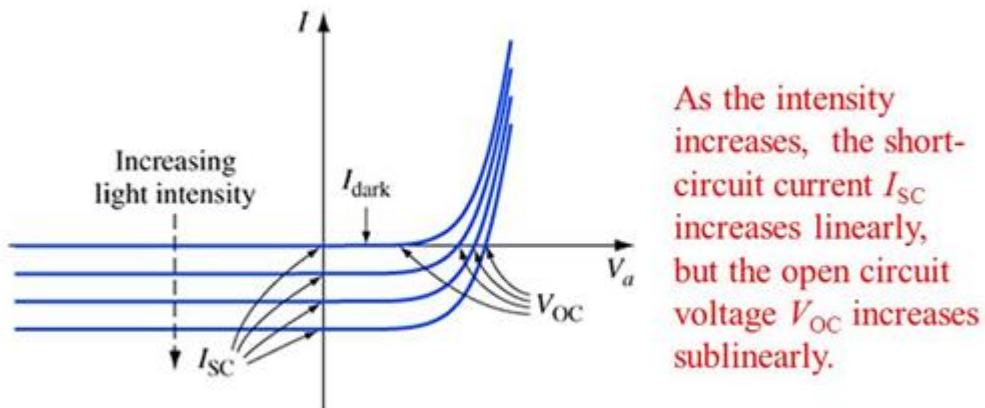


Figure-25 Basic construction of a silicon p-n junction solar cell

- Also, note that the metallic conductor connected to the p-type material and the thickness of the p-type material are such that they ensure that a maximum number of photons of light energy will reach the junction.
- A photon of light energy in this region may collide with a valence electron and impart to it sufficient energy to leave the parent atom. The result is a generation of free electrons and holes.
- This phenomenon will occur on each side of the junction. In the p-type material, the newly generated electrons are minority carriers and will move rather freely across the junction as explained for the basic p-n junction with no applied bias.
- A similar discussion is true for the holes generated in the n-type material. The result is an increase in the minority-carrier flow, which is opposite in direction to the conventional forward current of a p-n junction.
- This increase in reverse current is shown in Figure-26. Since $V = 0$ anywhere on the vertical axis and represents a short-circuit condition, the current at this intersection is called the short-circuit current and is represented by the notation I_{SC} .
- Under open-circuit conditions ($i_d = 0$), the photovoltaic voltage V_{OC} will result.

I-V characteristics & Efficiency



The I - V characteristics of a solar cell with varying illumination as a parameter.

Figure-26 Short-circuit current and open-circuit voltage versus light intensity for a solar cell

- This is a logarithmic function of the illumination, as shown in Figure-27. V_{OC} is the terminal voltage of a battery under no-load (open-circuit) conditions.
- Note, however, in the same figure that the short-circuit current is a linear function of the illumination. That is, it will double for the same increase in illumination (fC1 and 2fC1 in Figure-27) while the change in V_{OC} is less for this region.
- The major increase in V_{OC} occurs for lower-level increases in illumination. Eventually, a further increase in illumination will have very little effect on V_{OC} , although I_{SC} will increase, causing the power capabilities to increase.

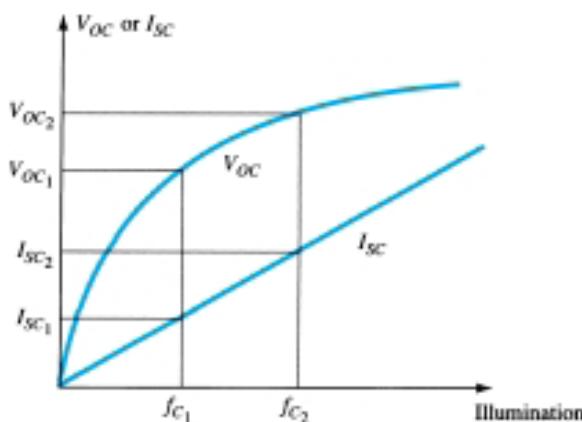


Figure-27 V_{oc} and I_{sc} versus illumination for a solar cell

- Selenium and silicon are the most widely used materials for solar cells, although gallium arsenide, indium arsenide, and cadmium sulfide, among others, are also used.

1.10 Phototransistors

- The fundamental behavior of photoelectric devices was introduced earlier with the description of the photodiode. This discussion will now be extended to include the phototransistor, which has a photosensitive collector-base p-n junction.
- The current induced by photoelectric effects is the base current of the transistor. If we assign the notation I_λ for the photo induced base current, the resulting collector current, on an approximate basis, is

$$I_C = h_{fe} I_\lambda \quad \text{--- (8)}$$

- A representative set of characteristics for a phototransistor is provided in Figure-28 with the symbolic representation of the device. Note the similarities between these curves and those of a typical bipolar transistor.

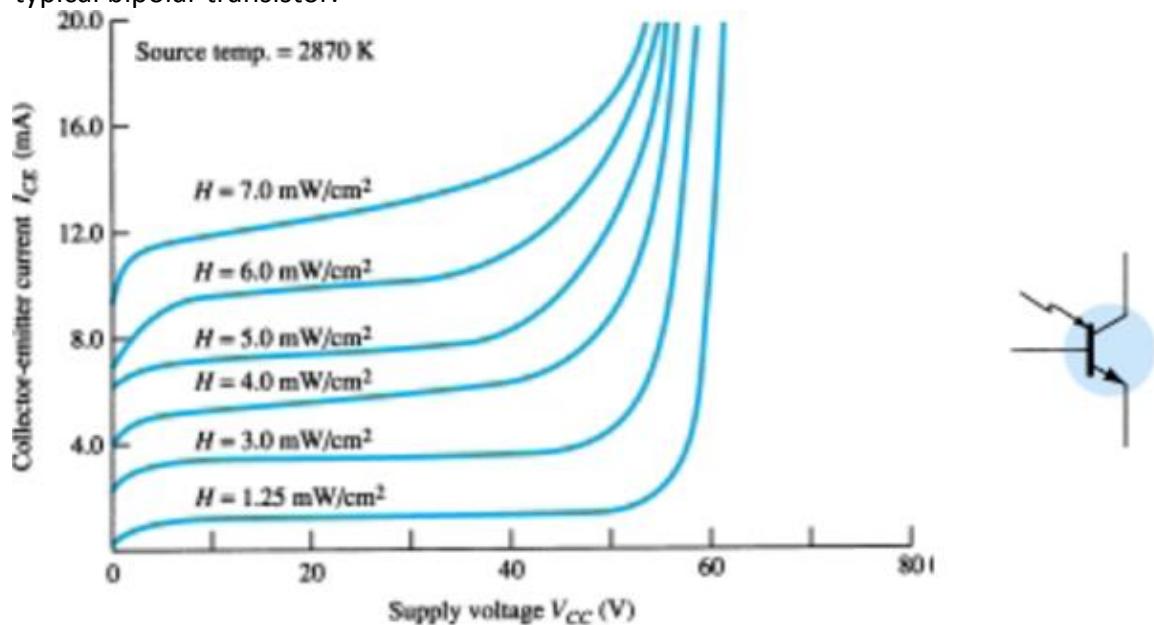


Figure-28 Phototransistor: collector characteristics (MRD300) and symbol. (Courtesy Motorola, Inc.)

- As expected, an increase in light intensity corresponds with an increase in collector current. To develop a greater degree of familiarity with the light-intensity unit of measurement, milliwatts per square centimeter, a curve of base current versus flux density appears in Figure-29.

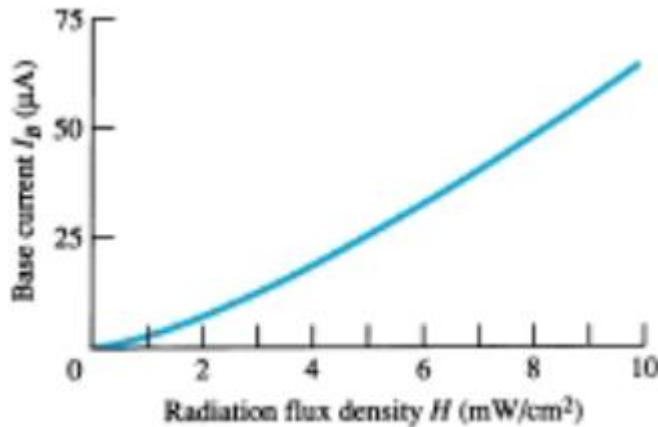


Figure-29 Base current versus flux density

- Note the exponential increase in base current with increasing flux density.
- Some of the areas of application for the phototransistor include punch-card readers, computer logic circuitry, lighting control (highways, etc.), level indication, relays, and counting systems.
- A high-isolation AND gate is shown in Figure-30 using three phototransistors and three LEDs (light-emitting diodes). The LEDs are semiconductor devices that emit light at an intensity determined by the forward current through the device.

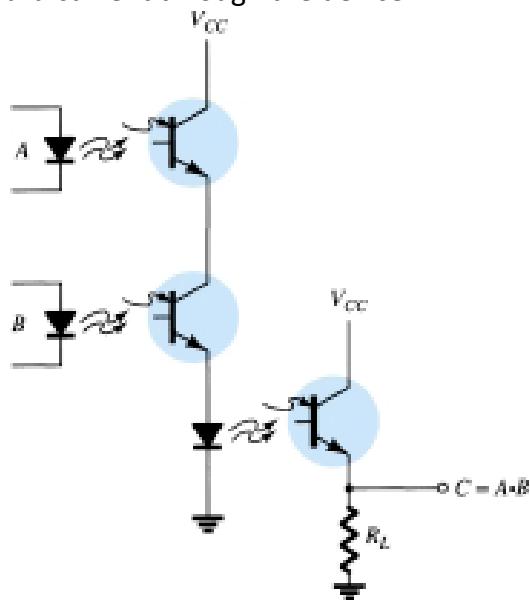


Figure-30 High-isolation AND gate employing phototransistors and light-emitting diodes (LEDs)

- With the aid of discussions in Chapter 1, the circuit behavior should be relatively easy to understand. The terminology high isolation simply refers to the lack of an electrical connection between the input and output circuits.

1.11 Sixteen-segment display

- A sixteen-segment display (SISD) is a type of display based on 16 segments that can be turned on or off according to the graphic pattern to be produced. Figure-31 shows sixteen segment display. It is an extension of the more common seven-segment display, adding four diagonal and two vertical segments and splitting the three horizontal segments in half.
- Other variants include the fourteen-segment display which does not split the top or bottom horizontal segments, and the twenty two-segment display that allows lower-case characters with descenders.
- Often a character generator is used to translate 7-bit ASCII character codes to the 16 bits that indicate which of the 16 segments to turn on or off.
- Sixteen-segment displays were originally designed to display alphanumeric characters (Latin letters and Arabic digits). Later they were used to display Thai numerals and Persian characters. Non-electronic displays using this pattern existed as early as 1902.
- Before the advent of inexpensive dot-matrix displays, sixteen and fourteen-segment displays were some of the few options available for producing alphanumeric characters on calculators and other embedded systems. However, they are still sometimes used on VCRs, car stereos, microwave ovens, telephone Caller ID displays, and slot machine readouts
- Sixteen-segment displays may be based on one of several technologies, the three most common optoelectronics types being LED, LCD and VFD. The LED variant is typically manufactured in single or dual character packages, to be combined as needed into text line displays of a suitable length for the application in question.

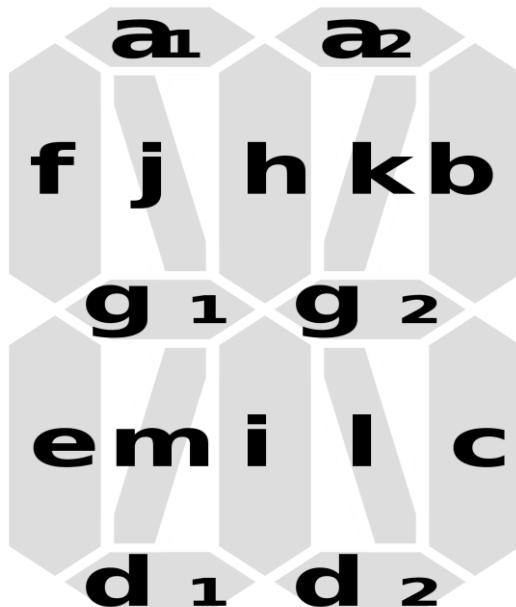


Figure-31 Sixteen segment display

- As with seven and fourteen-segment displays, a decimal point and/or comma may be present as an additional segment, or pair of segments; the comma (used for triple-digit groupings or as

a decimal separator in many regions) is commonly formed by combining the decimal point with a closely 'attached' leftwards-descending arc-shaped segment.

- This way, a point or comma may be displayed between character positions instead of occupying a whole position by itself, which would be the case if employing the bottom middle vertical segment as a point and the bottom left diagonal segment as a comma.
- Such displays were very common on pinball machines for displaying the score and other information, before the widespread use of dot-matrix display panels.

1.12 Dot-matrix LED display

- A dot-matrix display is an electronic digital display device that displays information on machines, clocks and watches, public transport departure indicators and many other devices requiring a simple display device of limited resolution.
- The display consists of a dot matrix of lights or mechanical indicators arranged in a rectangular configuration (other shapes are also possible, although not common) such that by switching on or off selected lights, text or graphics can be displayed. A dot matrix controller converts instructions from a processor into signals which turns on or off lights in the matrix so that the required display is produced.
- Light emitting diodes aligned in a form of matrix constitute a dot matrix display. It is commonly used to display time, temperature, news updates and many more on digital billboards.
- Dot Matrix Display is manufactured in various dimensions like 5x7, 8x9, 128x16, 128x32 and 128x64 where the numbers represent LEDs in rows and columns, respectively.
- Arrangement of the LEDs in the matrix pattern is made in either of the two ways: row anode-column cathode or row cathode-column anode.
- In row anode-column cathode pattern, the entire row is anode while all columns serve as cathode and vice-versa pattern is there in row cathode-column anode. LED wafers are glued to the bottom of the segments and glow when powered ON.
- The interesting part is that 35 LEDs are controlled by using a combination of 14 pins. Conductor tracks are laid all over the board to power each LED.

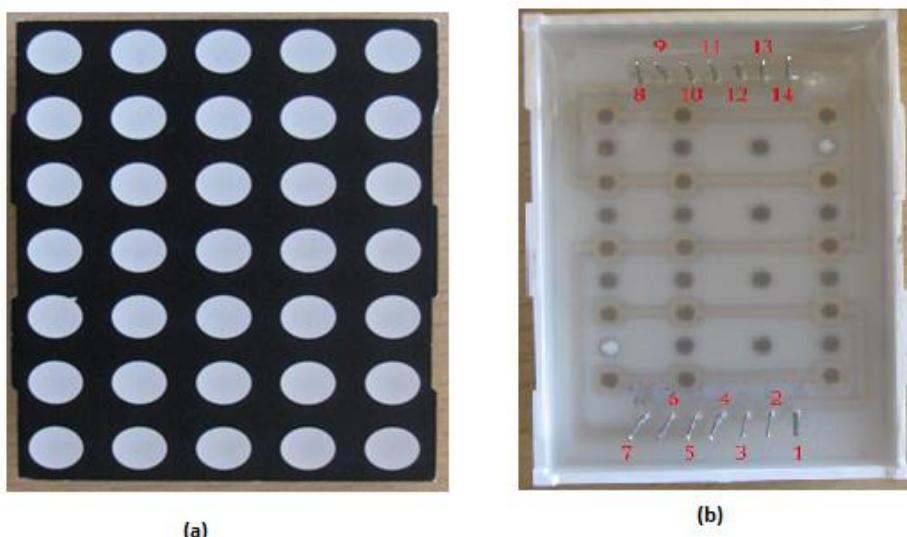


Figure-32 5x7 LED Dot-matrix display (a) Front view; (b) Rear view

- Figure-32 shows a 5x7 LED Dot-matrix display with front and rear views. A total of 35 LEDs are visible as dots on the front of the dot matrix display. The LEDs are illuminated when their respective terminals are powered.
- Back side of the display shows the in-built tracks and the pins. A total of 14 pins serve as a terminal for 35 LED's. Numbering of the pins varies depending upon the manufacturer. In this version of dot matrix display, 13, 3, 4, 11, 10 & 6 are the pin terminals for the column and rest for the row.

1.13 Question Bank

- 1) Explain the construction and working of LED.
- 2) Explain V-I characteristic of Zener diode.
- 3) **Describe Zener diode as a voltage regulator. (MIMP)**
- 4) Write a short note on photo diode.
- 5) **Write a short note on solar cell. (MIMP)**
- 6) Write a short note on PIN diode.
- 7) Write a short note on Varactor diode.
- 8) Write a short note on Schottky diode.
- 9) Write a short note on Tunnel diode.
- 10) Write a short note on Variastor.
- 11) Write a short note on seven segment display.
- 12) Write a short note on sixteen segment display.
- 13) Write a short note on dot-matrix LED display.
- 14) Write a short note on Phototransistor.
- 15) **Write a short note on Optocoupler. (MIMP)**

Unit-4

AC Analysis of BJT Circuits & Small Signal Amplifier

Basic Electronics

(3110016)

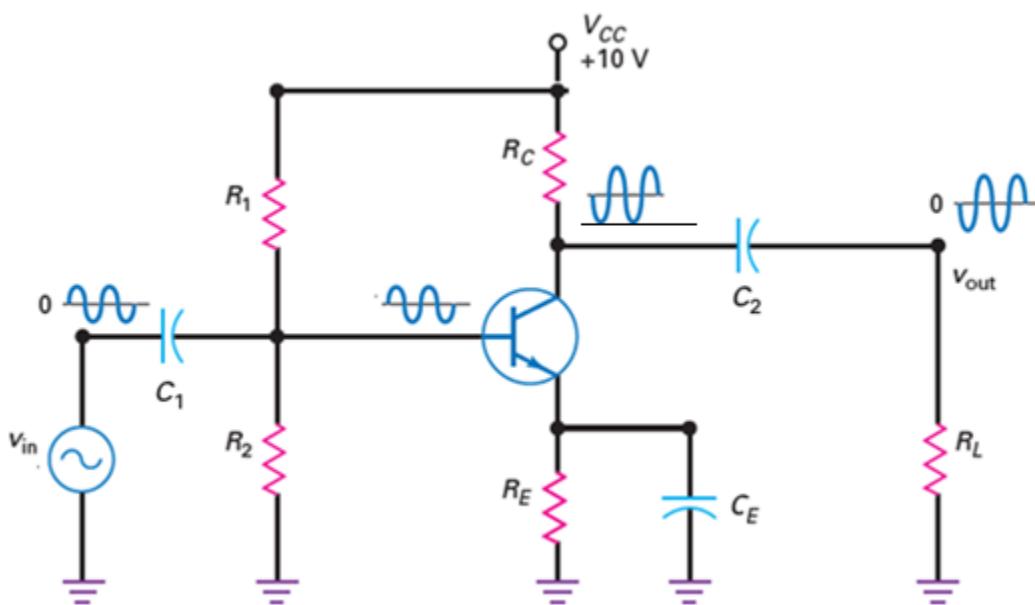
2nd Semester
Computer/Electrical Engineering

4.1 Transistor as an Amplifier (RC coupled transistor CE amplifier with coupling and bypass capacitor)

Amplification is a process of increasing the signal strength by increasing the amplitude of a given signal without changing its characteristics. A single stage RC coupled CE amplifier using NPN transistor is as shown in figure.

R_1 and R_2 resistors are used for providing proper biasing to the bipolar transistor. R_1 and R_2 form a voltage divider biasing network which provides necessary base voltage to drive the transistor in active region.

Input ac signal, required to be amplified is connected to the base of transistor through a coupling capacitor.



Coupling capacitor:

The capacitors C_1 and C_2 are called the coupling capacitors. A coupling capacitor passes an ac signal from one side to the other. At the same time, it does not allow the DC voltage to pass through. Hence, it is also called a DC blocking capacitor. Coupling capacitor removes unwanted DC component which may be inserted due to biasing voltage. So that only actual ac input signal can be amplified properly.

Bypass capacitor:

Capacitor connected in parallel with emitter resistance R_E is called emitter bypass capacitor. The capacitor C_E works as a bypass capacitor. It provides low resistance path to ac signal. It bypasses all the ac currents from the emitter to the ground. If the capacitor C_E is not put in the circuit then ac voltage developed across R_E will affect the input ac voltage and may reduce ac gain, because of negative feedback. Bypass capacitor avoids reduction in ac voltage gain.

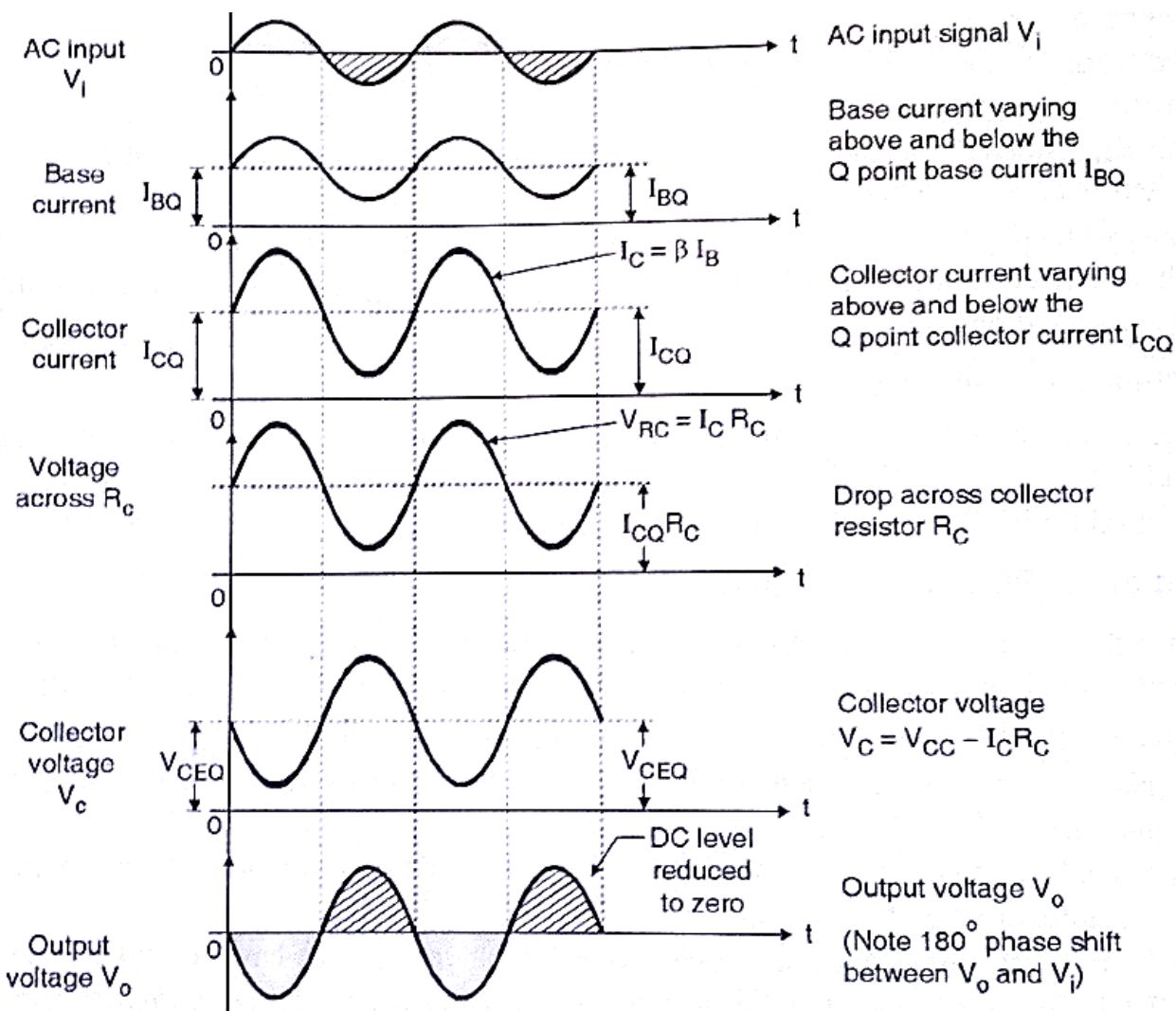
Working of transistor amplifier:

When ac input signal is not applied and only dc biasing voltage is connected the dc base current I_B , collector current I_{CQ} and V_{CEQ} voltage corresponding to Q point will be established. Q point can be stabilized at the middle of dc load line using voltage divider biasing circuit.

Now, when small ac signal which is applied to the input of transistor through coupling capacitor, then ac base current will be established. This ac base current will ride/superimposed on dc base current. Hence ac base current varies above and below Q point value of base current.

This variation in base current results in proportional variation in collector current because collector current $I_C \approx \beta I_B$. Hence if I_B increases then I_C will also increase and if I_B decreases then I_C will also decrease. So I_B and I_C are in same phase but I_C is amplified/magnified version of I_B .

The collector-emitter voltage V_{CE} is given by equation $V_{CE} = V_{CC} - I_C R_C$. Hence if I_C increase then V_{CE} will decrease and if I_C decrease then V_{CE} will increase. So I_C and V_{CE} are in opposite phase (180° out of phase). Various voltage and current waveform at different points are shown in figure.



Features of CE amplifier:

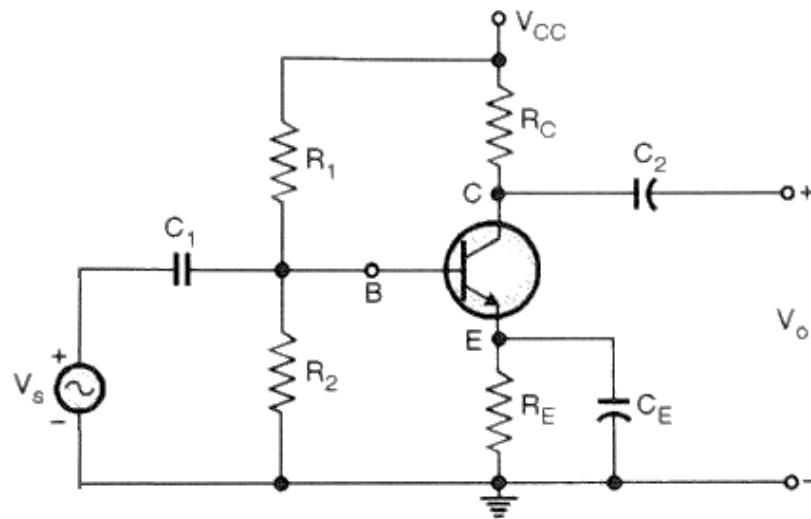
- High voltage gain as well as high current gain
- Moderate/high input impedance
- Low output impedance
- There is phase shift of 180° between input and output.

4.2 Selection of Q point in transistor for faithful amplification and effect of Q point position.

Faithful Amplification

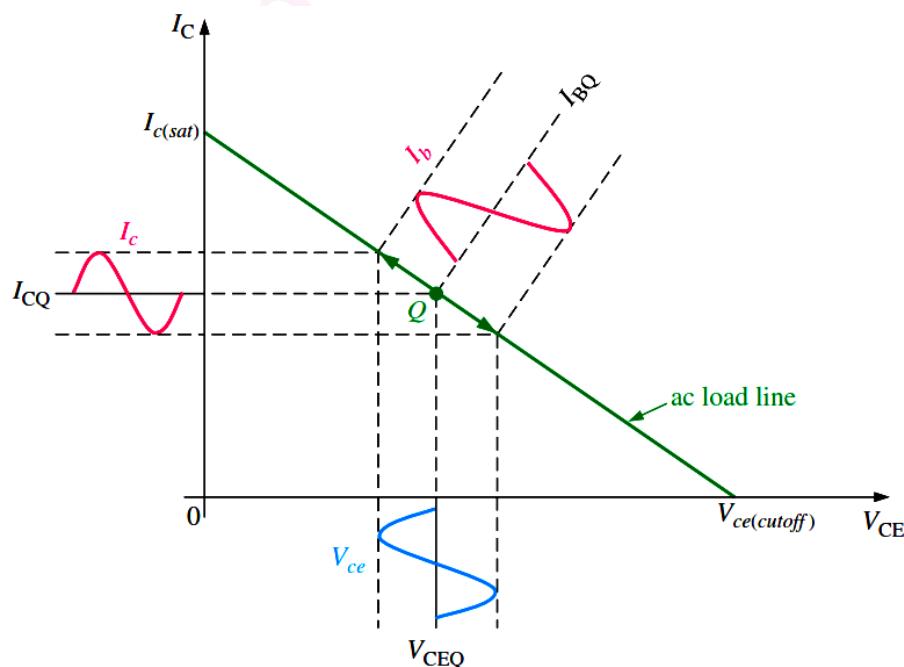
The process of increasing the signal strength is called as Amplification. *This amplification when done without any loss in the components of the signal, it is called Faithful amplification.*

Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input.

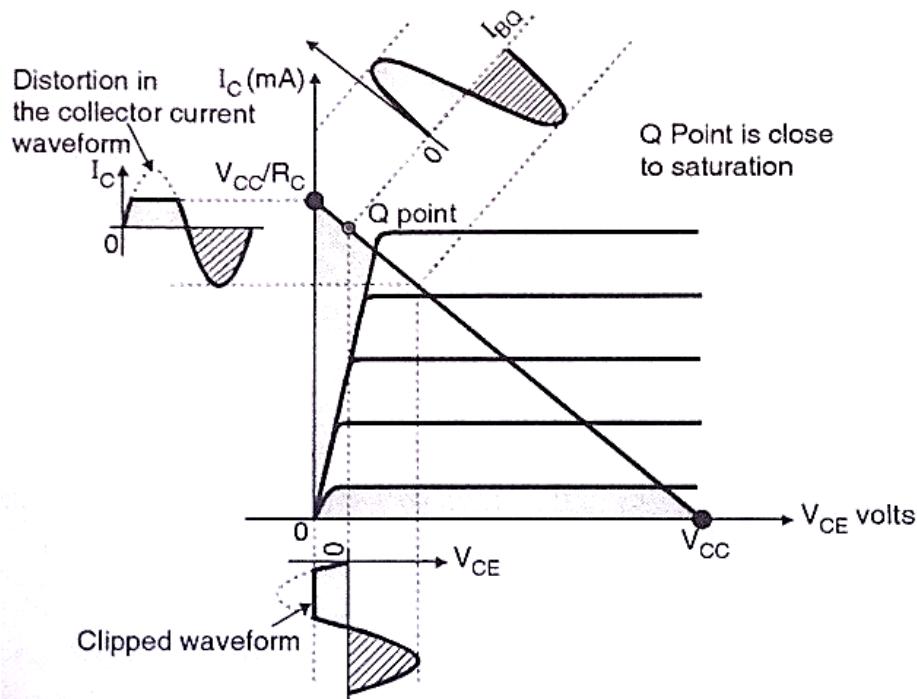


As shown in first graph, the input signal applied is completely amplified and reproduced without any losses. This can be considered as *Faithful Amplification*.

The operating point is so chosen that it lies in the **active region/middle of the DC load line** and it helps in the reproduction of complete signal without any loss.

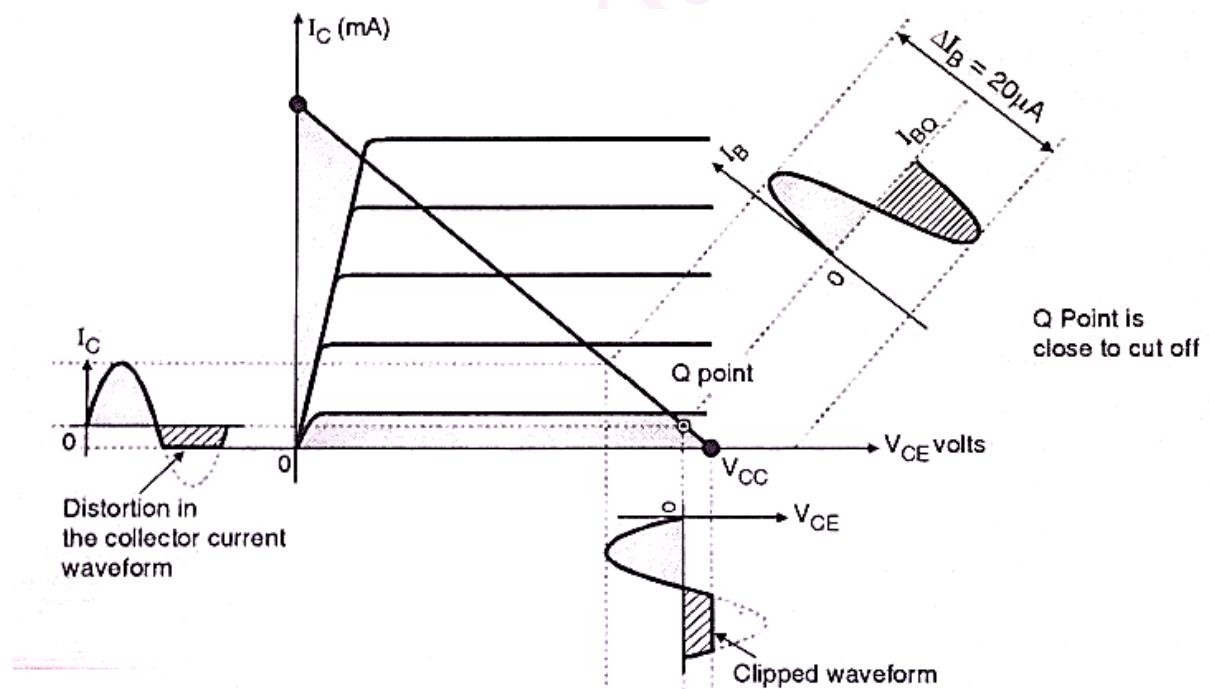


If the operating point is considered **near saturation point**, then the amplification will be as follows:



When Q point is set near saturation, then negative half cycle of output voltage gets distorted/clipped as shown in graph.

If the operation point is considered **near cut off point**, then the amplification will be as follow:

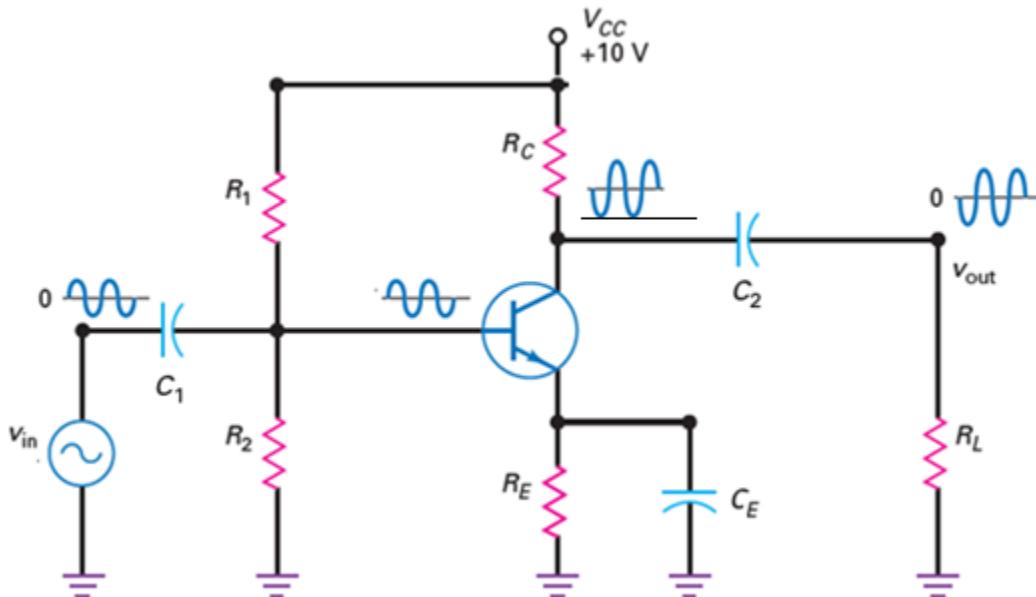


When Q point is set near cut-off, then positive half cycle of output voltage gets distorted/clipped as shown in graph.

4.3 Concept of AC load line. Derivation of AC Load Line for transistor CE amplifier and comparison with DC Load Line

A single stage RC coupled CE amplifier using NPN transistor is as shown in figure.

R_1 and R_2 resistors are used for providing proper biasing to the bipolar transistor. R_1 and R_2 form a voltage divider biasing network which provides necessary base voltage to drive the transistor in active region. Input ac signal, required to be amplified is connected to the base of transistor through a coupling capacitor. Output is taken across load resistor R_L .



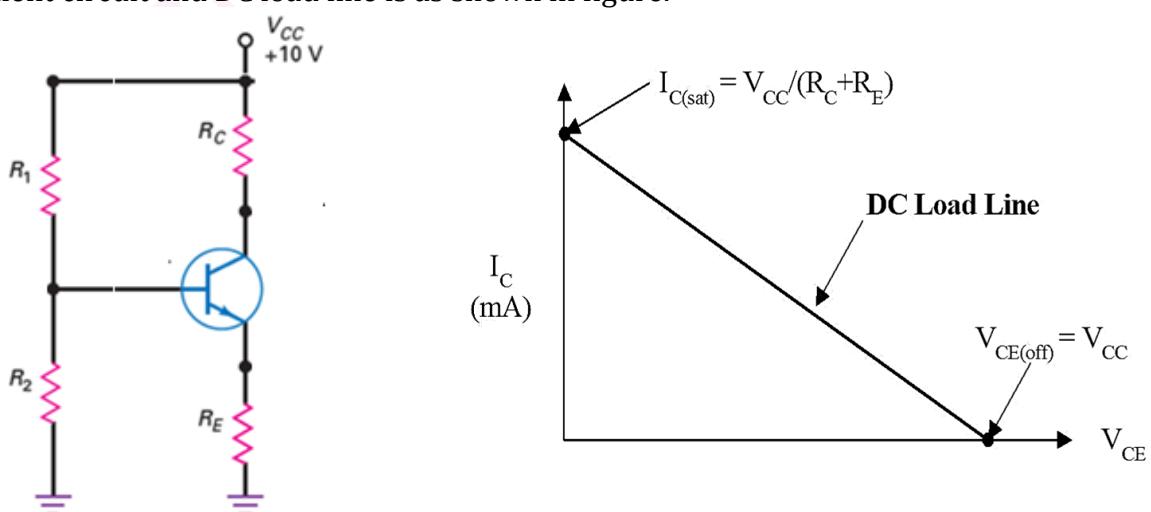
For the circuit shown in figure, both DC and AC currents flows through it. DC current is due to the biasing/battery voltage. AC signal is applied at the input. AC signal will superimpose/ride on the DC. Hence Load lines can be used separately for both DC and AC analysis.

The DC load line is the load line of the *DC equivalent circuit*, which can be derived by

- Reducing all AC source to zero
- Replacing capacitors by open circuits and inductors by short circuits.

It is used to determine the correct DC operating point, often called the Q point.

DC equivalent circuit and DC load line is as shown in figure.

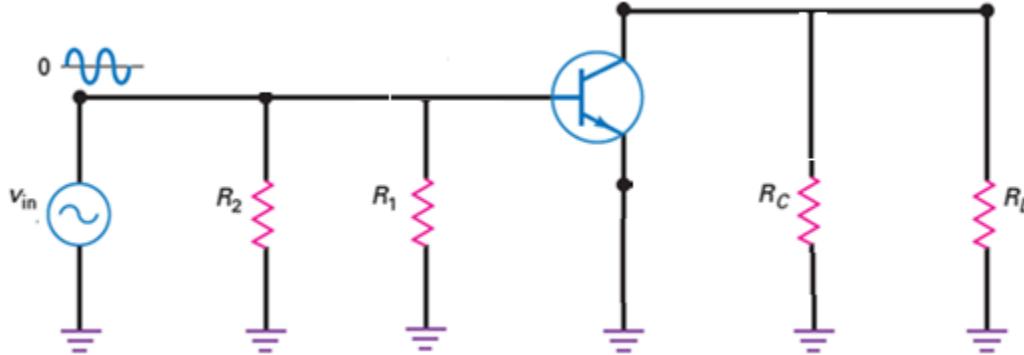


The AC load line is the load line of the *AC equivalent circuit*, which can be derived by

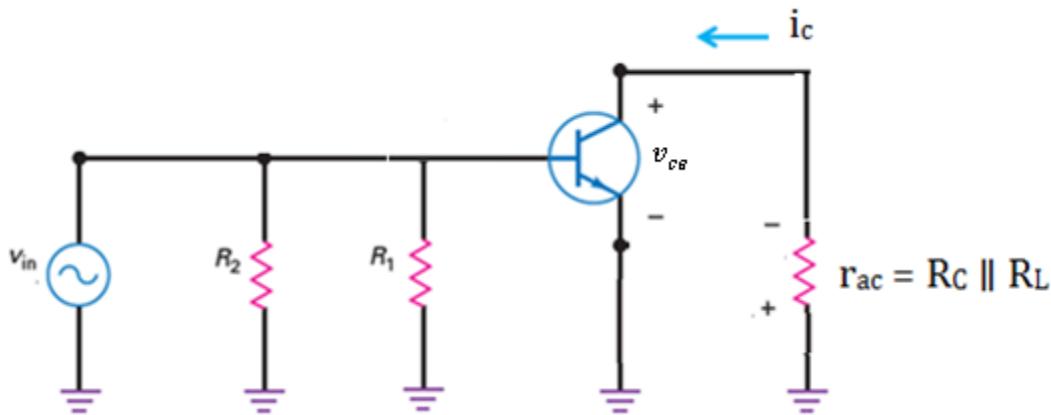
- Reducing all DC source to zero
- Replacing capacitors by short circuits.

AC load line will also pass through the same Q point.

AC equivalent circuit is as shown in figure.



AC equivalent circuit can be simplified to



For ac equivalent circuit, if we apply KVL at output loop

$$i_c r_{ac} + v_{ce} = 0 \quad \text{---- (1)}$$

As per superposition theorem, total current in the circuit is sum of current due to AC and DC. Hence total current is

$$i_c = i_c + I_{CQ} \quad \text{---- (2)}$$

and

$$v_{CE} = v_{ce} + V_{CEQ} \quad \text{---- (3)}$$

Where,

i_c is total collector current

v_{CE} is total collector emitter voltage

i_c is ac collector current

v_{ce} is ac collector emitter voltage

I_{CQ} is dc collector current for Q point

V_{CEQ} is dc collector emitter voltage for Q point

Now, if we put the value of ac collector current i_c and ac collector emitter voltage v_{ce} from equation (2) and (3) into equation (1) then

Equation (1) can be written as

$$[i_C - I_{CQ}] r_{ac} + [v_{CE} - V_{CEQ}] = 0 \quad \dots\dots (4)$$

Rearranging equation (4)

$$i_C r_{ac} - I_{CQ} r_{ac} + v_{CE} - V_{CEQ} = 0$$

$$i_C = I_{CQ} + \frac{V_{CEQ}}{r_{ac}} - \frac{v_{CE}}{r_{ac}} \quad \dots\dots (5)$$

Equation (5) is the equation of **AC Load Line**.

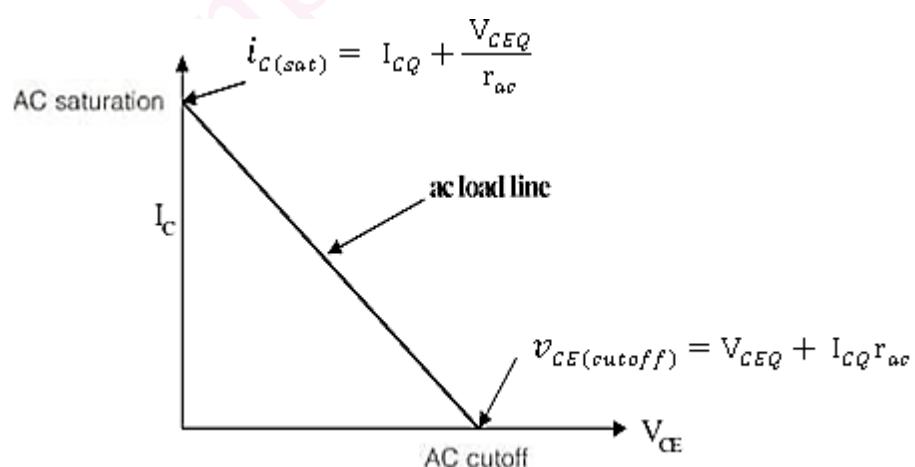
In equation (5) when $v_{CE} = 0$, then i_C is maximum. which is saturation point for ac load line and can be written as

$$i_{C(max)} = i_{C(saturation)} = I_{CQ} + \frac{V_{CEQ}}{r_{ac}} \quad \dots\dots (6)$$

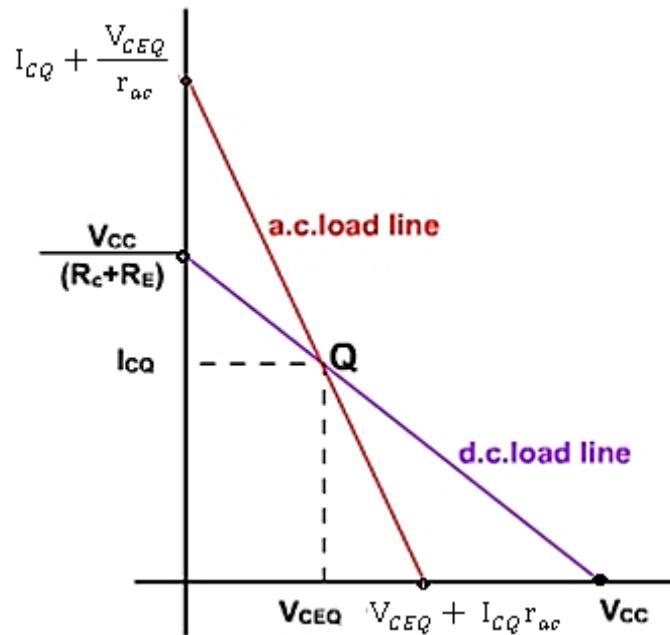
In equation (5) when $i_C = 0$, then v_{CE} is maximum. which is cut-off point for ac load line and can be written as

$$v_{CE(max)} = v_{CE(cut-off)} = V_{CEQ} + I_{CQ} r_{ac} \quad \dots\dots (7)$$

Line joining cut-off and saturation is called AC Load Line



Now, comparison of DC and AC load line is as shown in following graph.



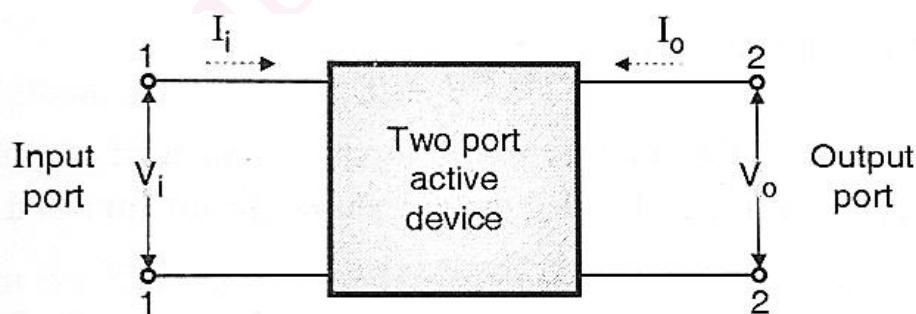
4.4 Various methods/models used for transistor AC analysis

Various Models/Methods used for transistor ac analysis are

- (i) Small signal r_e model
- (ii) Small signal hybrid model (h parameters model)
- (iii) Small signal hybrid Π model

4.5 Two port network and Hybrid Model (h parameter model).

A two port network can represented as follow



Where,

input current at port 1 is $I_1 = I_i$

output current at port 2 is $I_2 = I_o$

input voltage at port 1 is $V_1 = V_i$

output voltage at port 2 is $V_2 = V_o$

There are four variables. Any variable can be represented in terms of other two known variable, then one of the possible set/pair of equation are

$$V_i = h_{11} I_i + h_{12} V_o \quad \text{---- (1)}$$

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \text{---- (1)}$$

$$I_o = h_{21} I_i + h_{22} V_o \quad \text{---- (2)}$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \text{---- (2)}$$

Where, coefficients $h_{11}, h_{12}, h_{21}, h_{22}$ are called hybrid parameters (h parameters).

Expression for various h parameters:

(1) Expression for h_{11}

In equation (1) when V_2 is set to zero, by short circuiting output terminal, then h_{11} is derived as follow:

$$h_{11} = \frac{V_1}{I_1} \quad V_2=0$$

h_{11} is called the **Input Impedance** which is the ratio of input voltage V_1 and input current I_1 . It's unit is ohm Ω .

(2) Expression for h_{12}

In equation (1) when I_1 is set to zero, by open circuiting input terminal, then h_{12} is derived as follow:

$$h_{12} = \frac{V_1}{V_2} \quad I_1=0$$

h_{12} is called the **Reverse voltage gain** which is the ratio of input voltage V_1 and output voltage V_2 . It is unit less.

(3) Expression for h_{21}

In equation (2) when V_2 is set to zero, by short circuiting output terminal, then h_{21} is derived as follow:

$$h_{21} = \frac{I_2}{I_1} \quad V_2=0$$

h_{21} is called the **Forward current gain** which is the ratio of output current I_2 and input current I_1 . It is unit less.

(4) Expression for h_{22}

In equation (2) when I_1 is set to zero, by open circuiting input terminal, then h_{22} is derived as follow:

$$h_{22} = \frac{I_2}{V_2} \quad I_1=0$$

h_{22} is called the **Transconductance or Output Admittance** which is the ratio of output current I_2 and output voltage V_2 . It's unit is mho O .

Why h parameters are called hybrid parameters?

The four parameters associated with this model are Input impedance, Reverse voltage gain, Forward current gain and Output admittance. Since unit of these parameters are completely different from each other, this set of parameters are called hybrid parameters.

Merits and Demerits of h parameters.

Merits of hybrid model/h parameters:

- h parameters can be easily measured.
- Can be calculated also from static characteristic of transistor.
- Manufacturer provides h parameters in data sheets.
- Can be used easily and conveniently in circuit analysis and design.

Demerits of hybrid model/h parameters:

- h parameters are defined only for a particular set of operating conditions.

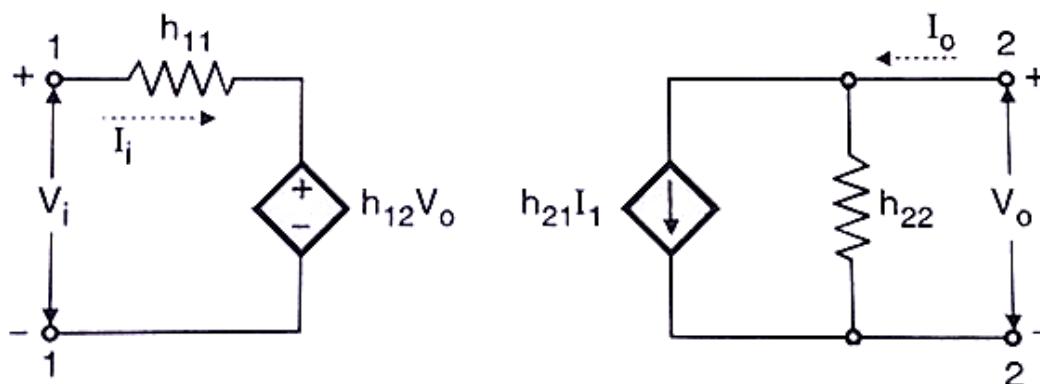
4.6 Hybrid equivalent circuit.

Based on equations, the equivalent circuit for input as well as output can be derived as follows.

set/pair of equation are

$$V_i = h_{11} I_i + h_{12} V_o \quad \text{---- (1)}$$

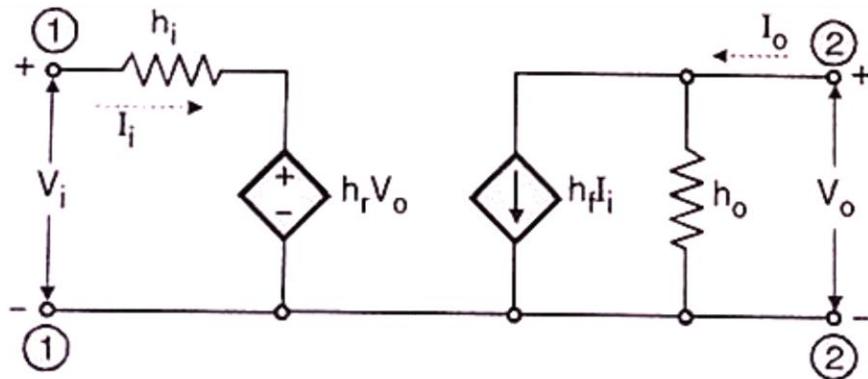
$$I_o = h_{21} I_i + h_{22} V_o \quad \text{---- (2)}$$



Alternate way of representing h parameters is

- | | |
|--------------------------|------------------------|
| $h_{11} \rightarrow h_i$ | (input impedance) |
| $h_{12} \rightarrow h_r$ | (reverse voltage gain) |
| $h_{21} \rightarrow h_f$ | (forward current gain) |
| $h_{22} \rightarrow h_o$ | (output admittance) |

Now, h parameter model can be also represented as follow

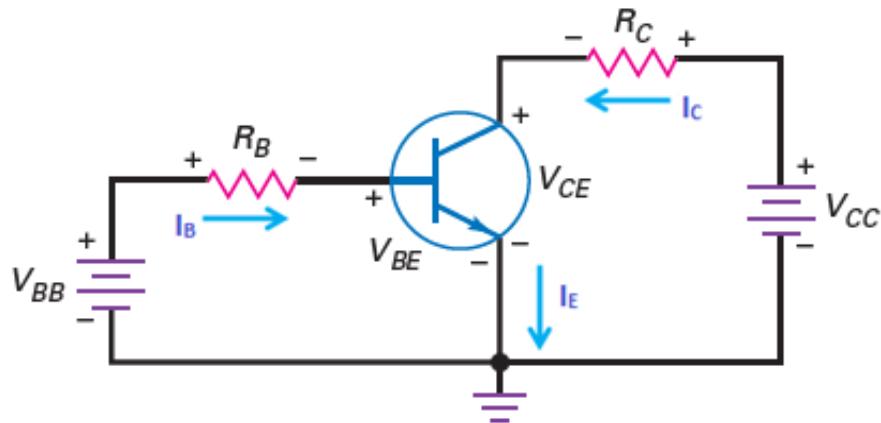


***h* parameters for different configuration:**

Sr. No.	Parameters	CB	CE	CC
1	Input impedance	h_{ib}	h_{ie}	h_{ic}
2	Reverse voltage gain	h_{rb}	h_{re}	h_{rc}
3	Forward current gain	h_{fb}	h_{fe}	h_{fc}
4	Output admittance	h_{ob}	h_{oe}	h_{oc}

4.7 Transistor Hybrid Model.

(1) Hybrid model for CE configuration:



For CE configuration of transistor

input current is $I_i = I_b$

output current is $I_o = I_c$

input voltage is $V_i = V_{be}$

output voltage is $V_o = V_{ce}$

Hence set/pair of equation are

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \quad \text{---- (1)}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \quad \text{---- (2)}$$

Expression for various h parameters for CE configuration:

(1) Expression for h_{ie}

In equation (1) when V_{ce} is set to zero, by short circuiting output terminal, then h_{ie} is derived as follow:

$$h_{ie} = \frac{V_{be}}{I_b} \quad V_{ce}=0$$

h_{ie} is called the **Input Impedance** which is the ratio of input voltage V_{be} and input current I_b . It's unit is ohm Ω .

(2) Expression for h_{re}

In equation (1) when I_b is set to zero, by open circuiting input terminal, then h_{re} is derived as follow:

$$h_{re} = \frac{V_{be}}{V_{ce}} \quad I_b=0$$

h_{re} is called the **Reverse voltage gain** which is the ratio of input voltage V_{be} and output voltage V_{ce} . It is unit less.

(3) Expression for h_{fe}

In equation (2) when V_{ce} is set to zero, by short circuiting output terminal, then h_{fe} is derived as follow:

$$h_{fe} = \frac{I_c}{I_b} \quad V_{ce}=0$$

h_{fe} is called the **Forward current gain** which is the ratio of output current I_c and input current I_b . It is unit less.

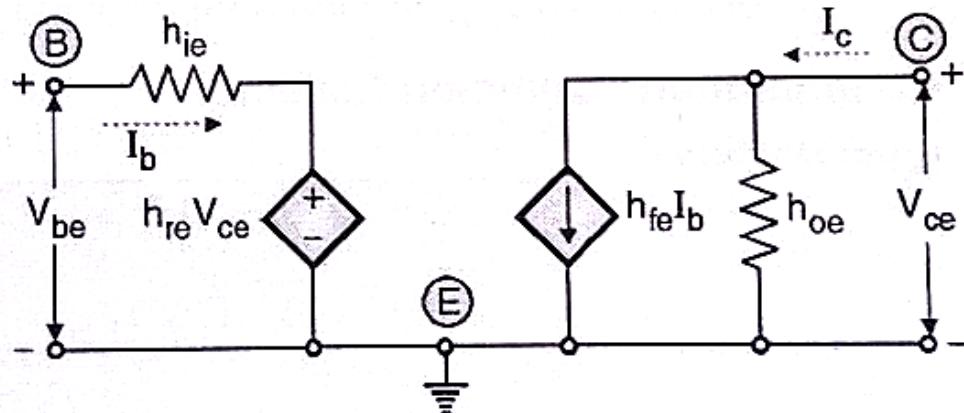
(4) Expression for h_{oe}

In equation (2) when I_b is set to zero, by open circuiting input terminal, then h_{oe} is derived as follow:

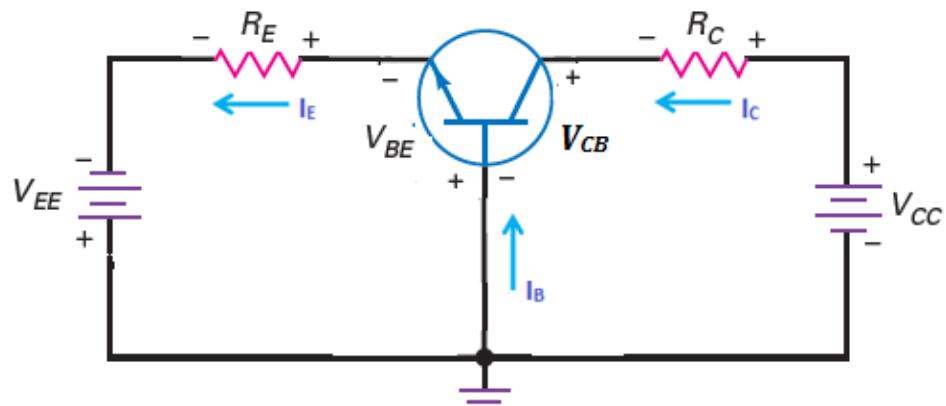
$$h_{oe} = \frac{I_c}{V_{ce}} \quad I_b=0$$

h_{oe} is called the **Transconductance or Output Admittance** which is the ratio of output current I_c and output voltage V_{ce} . It's unit is mho Ω .

Hybrid equivalent circuit for CE configuration is



(2) Hybrid model for CB configuration:



For CB configuration of transistor

input current is $I_i = I_e$

output current is $I_o = I_c$

input voltage is $V_i = V_{eb}$

output voltage is $V_o = V_{cb}$

Hence set/pair of equation are

$$V_{eb} = h_{ib} I_e + h_{re} V_{cb} \quad \text{--- (1)}$$

$$I_c = h_{fb} I_e + h_{oe} V_{cb} \quad \text{--- (2)}$$

Expression for various h parameters for CB configuration:

(1) Expression for h_{ib}

In equation (1) when V_{cb} is set to zero, by short circuiting output terminal, then h_{ib} is derived as follow:

$$h_{ib} = \frac{V_{eb}}{I_e} \quad V_{cb}=0$$

h_{ib} is called the **Input Impedance** which is the ratio of input voltage V_{eb} and input current I_e . Its unit is ohm Ω .

(2) Expression for h_{rb}

In equation (1) when I_e is set to zero, by open circuiting input terminal, then h_{rb} is derived as follow:

$$h_{rb} = \frac{V_{eb}}{V_{cb}} \quad I_e=0$$

h_{rb} is called the **Reverse voltage gain** which is the ratio of input voltage V_{eb} and output voltage V_{cb} . It is unit less.

(3) Expression for h_{fb}

In equation (2) when V_{cb} is set to zero, by short circuiting output terminal, then h_{fb} is derived as follow:

$$h_{fb} = \frac{I_c}{I_e} \quad V_{cb}=0$$

h_{fb} is called the **Forward current gain** which is the ratio of output current I_c and input current I_e . It is unit less.

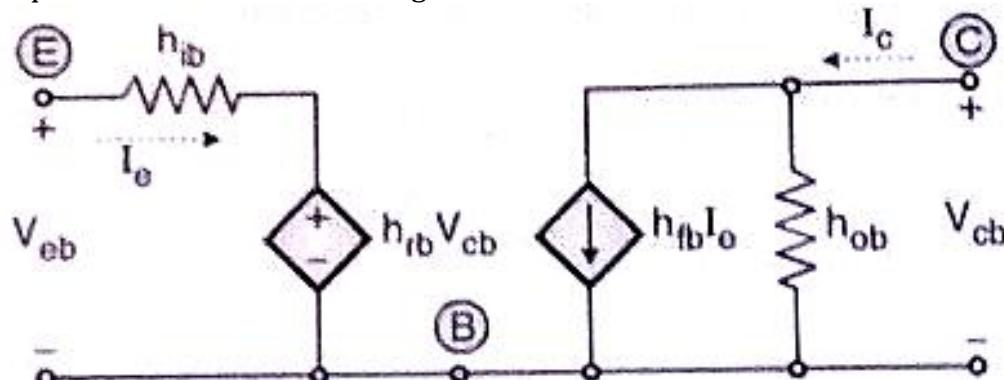
(4) Expression for h_{ob}

In equation (2) when I_e is set to zero, by open circuiting input terminal, then h_{ob} is derived as follow:

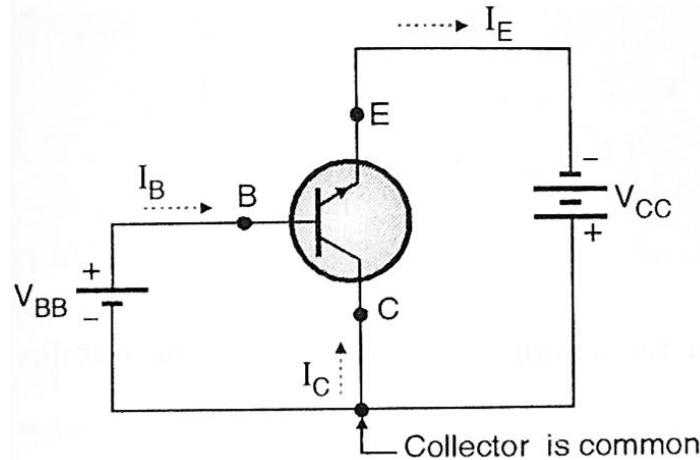
$$h_{ob} = \frac{I_c}{V_{cb}} \quad I_e=0$$

h_{ob} is called the **Transconductance or Output Admittance** which is the ratio of output current I_c and output voltage V_{cb} . Its unit is mho Ω .

Hybrid equivalent circuit for CB configuration is



(3) Hybrid model for CC configuration:



For CC configuration of transistor

input current is $I_i = I_b$

input voltage is $V_i = V_{bc}$

output current is $I_o = I_e$

output voltage is $V_o = V_{ec}$

Hence set/pair of equation are

$$V_{bc} = h_{ic} I_b + h_{rc} V_{ec} \quad \text{--- (1)}$$

$$I_e = h_{fc} I_b + h_{oc} V_{ec} \quad \text{--- (2)}$$

Expression for various h parameters for CC configuration:

(1) Expression for h_{ic}

In equation (1) when V_{ec} is set to zero, by short circuiting output terminal, then h_{ic} is derived as follow:

$$h_{ic} = \frac{V_{bc}}{I_b} \quad V_{ec}=0$$

h_{ic} is called the **Input Impedance** which is the ratio of input voltage V_{bc} and input current I_b . It's unit is ohm Ω .

(2) Expression for h_{rc}

In equation (1) when I_b is set to zero, by open circuiting input terminal, then h_{rc} is derived as follow:

$$h_{rc} = \frac{V_{bc}}{V_{ec}} \quad I_b=0$$

h_{rc} is called the **Reverse voltage gain** which is the ratio of input voltage V_{bc} and output voltage V_{ec} . It is unit less.

(3) Expression for h_{fc}

In equation (2) when V_{ec} is set to zero, by short circuiting output terminal, then h_{fc} is derived as follow:

$$h_{fc} = \frac{I_e}{I_b} \quad V_{ec}=0$$

h_{fc} is called the **Forward current gain** which is the ratio of output current I_e and input current I_b . It is unit less.

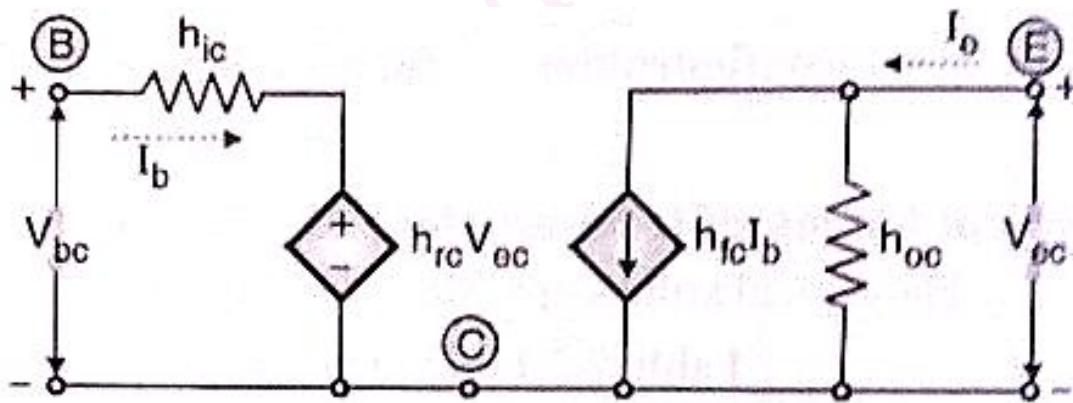
(4) Expression for h_{oc}

In equation (2) when I_b is set to zero, by open circuiting input terminal, then h_{oc} is derived as follow:

$$h_{oc} = \frac{I_c}{V_{ec}} \quad I_b=0$$

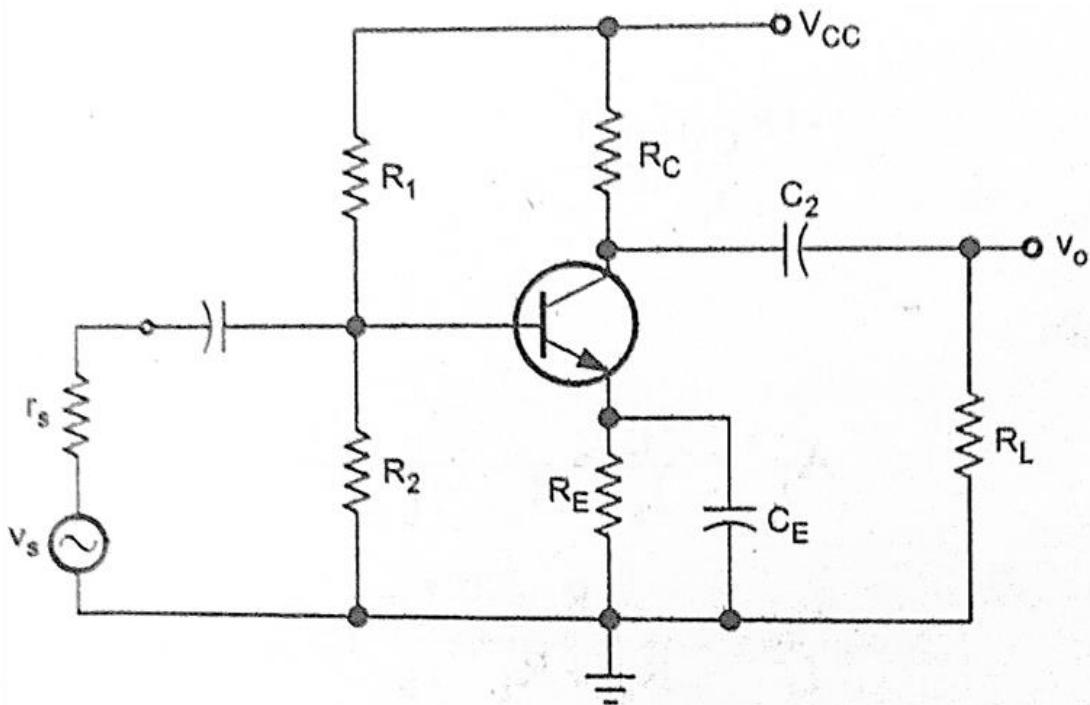
h_{oc} is called the **Transconductance or Output Admittance** which is the ratio of output current I_e and output voltage V_{ec} . Its unit is mho Ω .

Hybrid equivalent circuit for CC configuration is

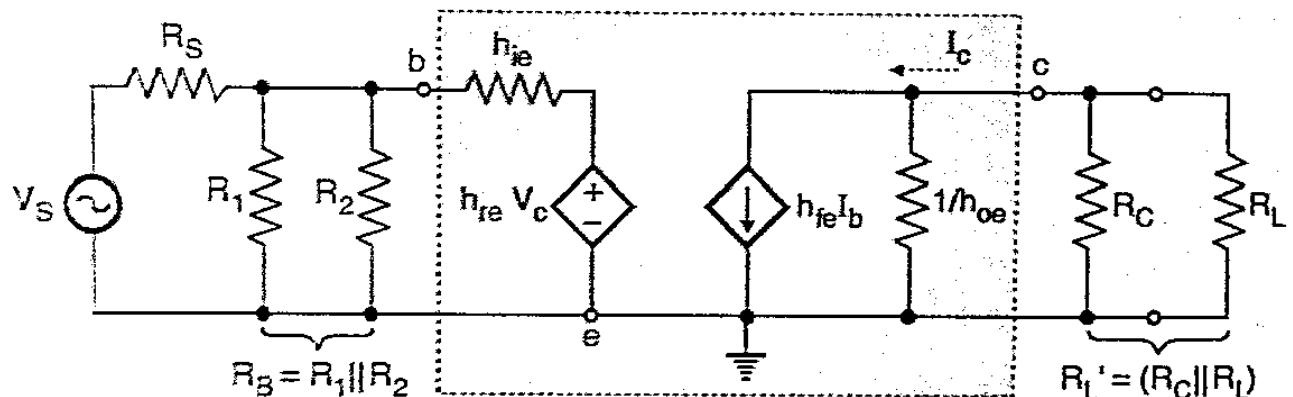


4.8 Analysis of transistor CE configuration of amplifier using Hybrid Model (h parameter model) and derivation of Input impedance, output impedance, voltage gain and current gain

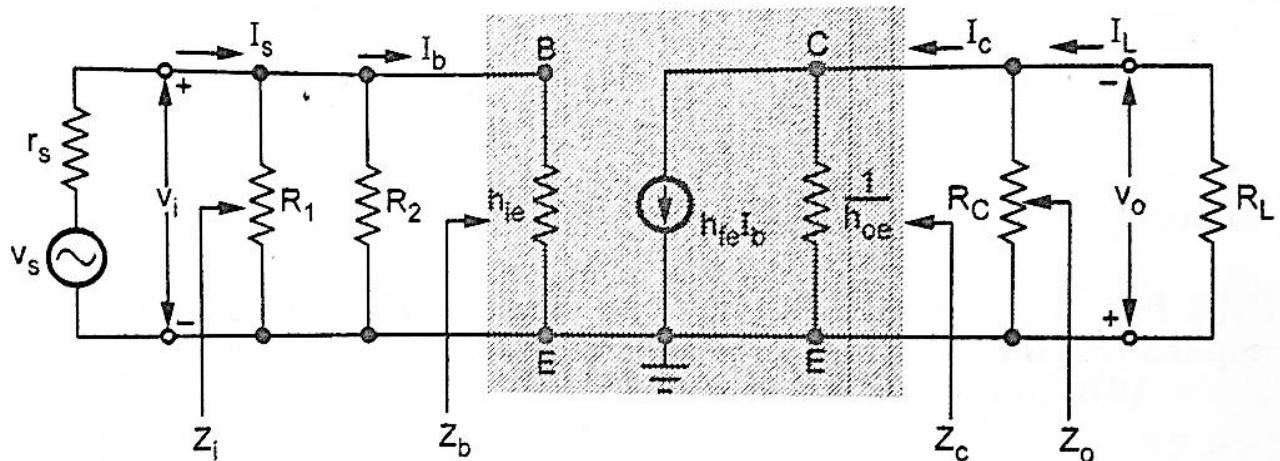
The circuit diagram of CE amplifier is as shown in figure.



h parameter equivalent circuit (ac equivalent circuit) for CE configuration is derived as



As value of h_{re} is very small and can be neglected. Then approximate equivalent circuit will be



(a) Input impedance

From the equivalent circuit, it has been observed that resistance observed at the base is h_{ie} . Hence input impedance looking from input terminal of overall circuit is

$$\boxed{\mathbf{Z}_{in} = R_1 \parallel R_2 \parallel h_{ie}} \quad \text{---- (1)}$$

(b) output impedance

From the equivalent circuit, it has been observed that impedance observed at the collector terminal is $1/h_{oe}$.

Hence output impedance looking from output terminal of overall circuit is

$$\boxed{\mathbf{Z}_o = R_c \parallel \frac{1}{h_{oe}}} \quad \text{---- (2)}$$

(c) Voltage Gain

Voltage gain is the ratio of output voltage V_o and input voltage V_i .

From the equivalent circuit, it has been observed that output voltage is

$$V_o = -I_c (R_c \parallel R_L)$$

and input voltage is

$$V_{in} = I_b h_{ie}$$

Hence voltage gain is

$$\boxed{A_V = \frac{-I_c (R_c \parallel R_L)}{I_b h_{ie}}} \quad \text{--- (3)}$$

but as we know that

$$\mathbf{h}_{fe} = \frac{I_c}{I_b}$$

So, equation (3) can be written as

$$\boxed{A_V = \frac{-h_{fe} (R_c \parallel R_L)}{h_{ie}}} \quad \text{--- (4)}$$

Negative sign indicates that output voltage V_o is 180° out of phase with input voltage.

(d) Current Gain

Current gain is the ratio of output current I_L and input current I_S .

$$A_{is} = \frac{I_L}{I_s}$$

Also,

$$A_{is} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$$

Let, parallel resistance in equivalent circuit is ($R_1 \parallel R_2$) = R_B

Now, current gain is

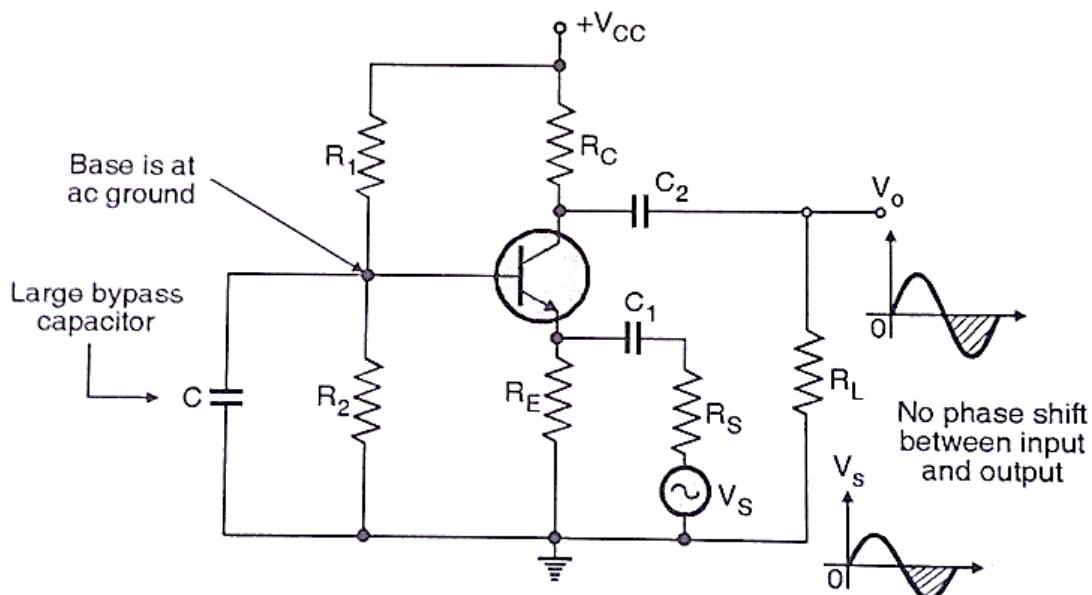
$$A_{is} = \frac{-R_c}{R_c + R_L} \times h_{fe} \times \frac{R_B}{R_B + h_{ie}}$$

$$A_{is} = \frac{-h_{fe} R_c R_B}{(R_c + R_L) (R_B + h_{ie})}$$

---- (5)

4.9 Common Base Amplifier circuit (CB amplifier)

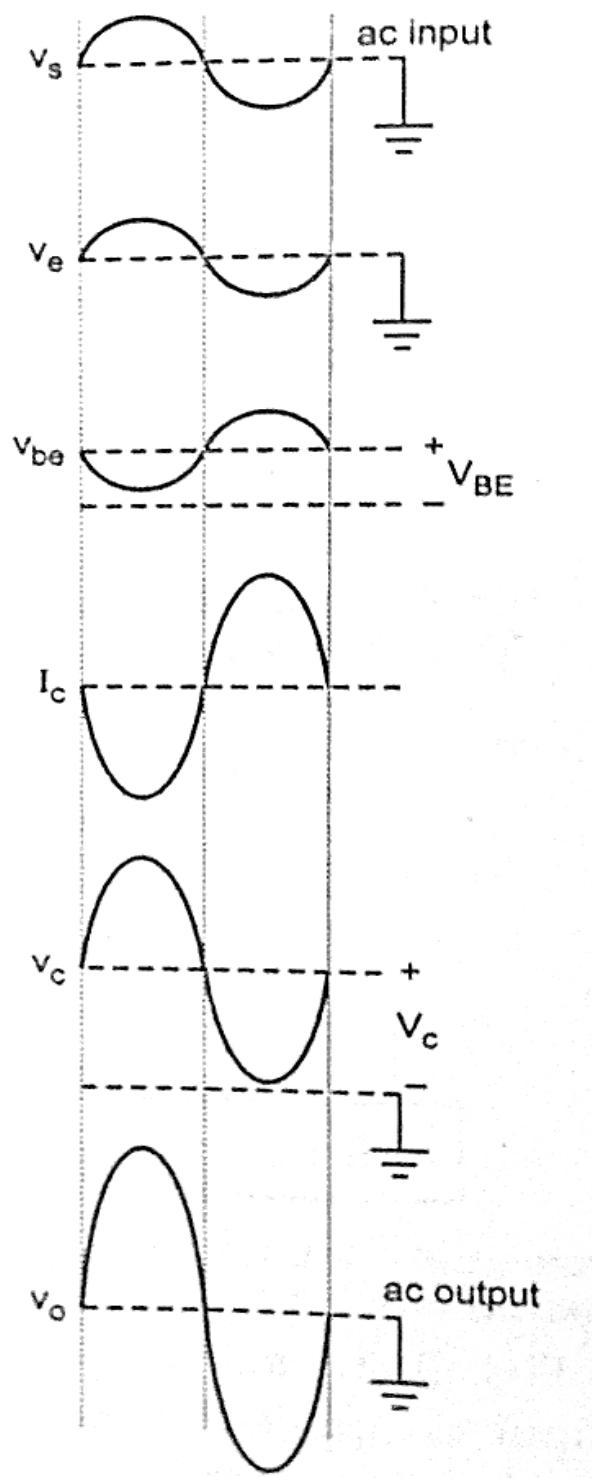
The circuit diagram of CB amplifier is as shown in figure. AC signal source is connected to emitter through coupling capacitor C_1 and load is connected at collector. Base terminal is ac grounded through capacitor C . In given circuit R_1 and R_2 are biasing resistor and C_1 are well as C_2 are coupling capacitors.



Working of CB amplifier:

Input signal V_s is applied at emitter terminal. When input voltage increases, base voltage V_{BE} decreases because base is negative with respect to emitter. So base current I_B will decrease and it results in decrease in collector current also. If collector current I_c decrease then voltage at collector V_c and output voltage V_o will increase.

Thus increase in input voltage results in increase in output voltage also. Hence output voltage is in same phase with input voltage in CB amplifier.



Features of CB amplifier:

- It has very low input impedance almost (20Ω).
- It has very high output impedance almost ($1 M\Omega$).
- It has a current gain of unity or (< 1).
- It has a large voltage gain.

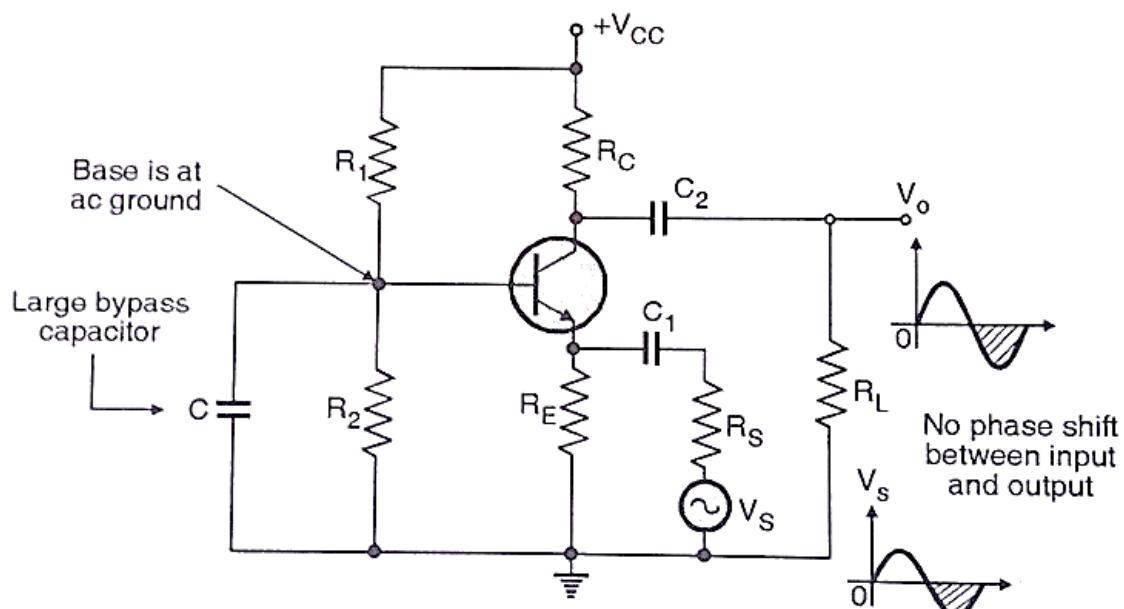
- It has no phase reversal between output and input.

Application of CB amplifier:

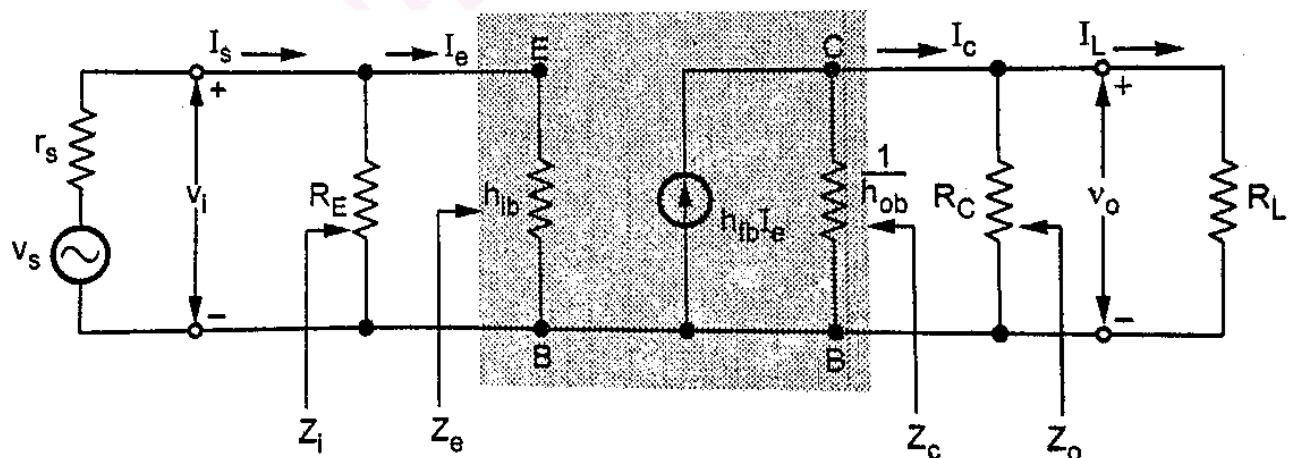
- It is used as a preamplifier in communication circuit.

4.10 Analysis of transistor CB configuration of amplifier using Hybrid Model (h parameter model) and derivation of Input impedance, output impedance, voltage gain and current gain

The circuit diagram of CB amplifier is as shown in figure.



As value of h_{rb} is very small and can be neglected. Then approximate equivalent circuit can be redrawn as shown in figure. h parameter equivalent circuit (ac equivalent circuit) for CB configuration is derived as



(a) Input impedance

From the equivalent circuit, it has been observed that resistance observed at the emitter base is h_{ib} . Hence input impedance looking from input terminal of overall circuit is

$$Z_{in} = R_E \parallel h_{ib}$$

---- (1)

(b) output impedance

From the equivalent circuit, it has been observed that impedance observed at the collector terminal is $1/h_{oe}$.

Hence output impedance looking from output terminal of overall circuit is

$$Z_o = R_c \parallel \frac{1}{h_{oe}} \quad \text{---- (2)}$$

(c) Voltage Gain

Voltage gain is the ratio of output voltage V_o and input voltage V_i .

From the equivalent circuit, it has been observed that output voltage is

$$V_o = I_c (R_c \parallel R_L)$$

and input voltage is

$$V_{in} = I_e h_{ib}$$

Hence voltage gain is

$$A_V = \frac{I_c (R_c \parallel R_L)}{I_b h_{ie}} \quad \text{--- (3)}$$

but as we know that

$$h_{fb} = \frac{I_c}{I_e}$$

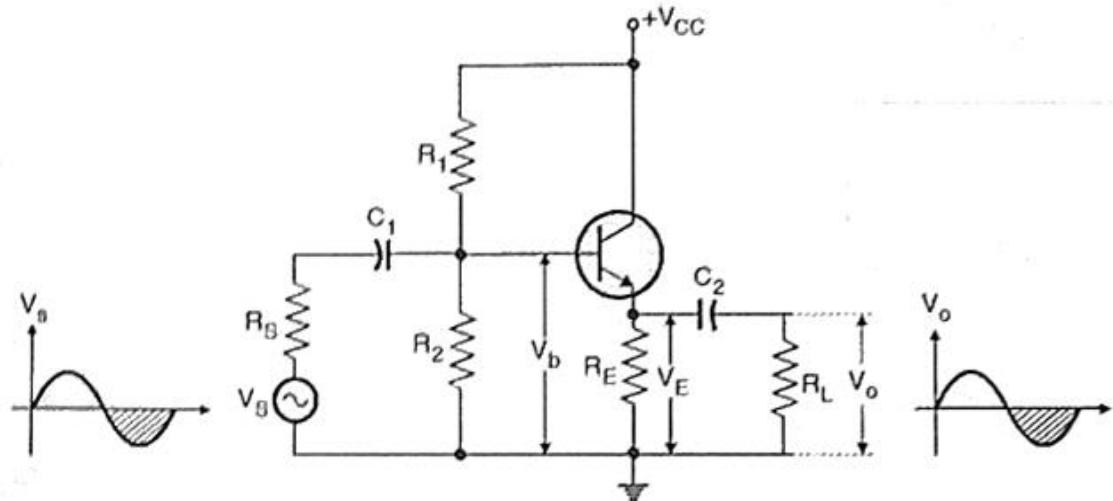
So, equation (3) can be written as

$$A_V = \frac{h_{fb} (R_c \parallel R_L)}{h_{ib}} \quad \text{--- (4)}$$

4.11 Common Collector Amplifier circuit (CC amplifier)/Emitter Follower:

The circuit diagram of CC amplifier is as shown in figure. AC signal source is connected to base through coupling capacitor C_1 and load is connected at emitter through coupling capacitor. In given circuit R_1 and R_2 are biasing resistor and C_1 are well as C_2 are coupling capacitors.

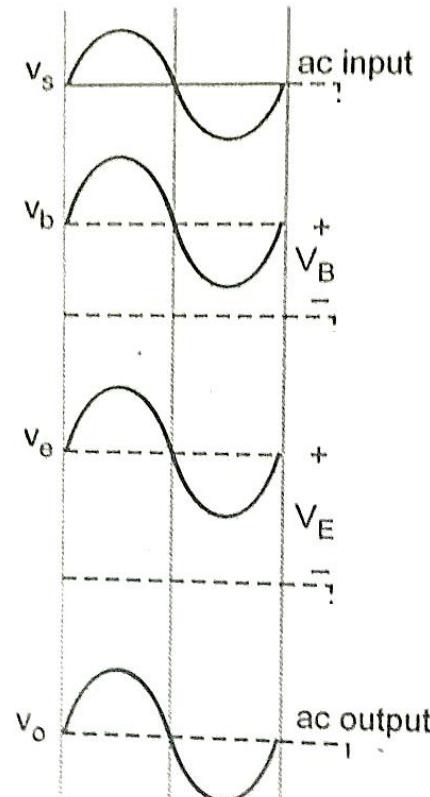
It is also known as Emitter follower circuit because output voltage at emitter is approximately same as input voltage at base. Thus output follows the input, hence called Emitter follower.



Working of CC amplifier:

Input signal V_s is applied at base terminal through coupling capacitor. When input voltage increases, base voltage V_{BE} will also increase. It results in increase in base current and subsequently increase in collector current also. Increase in collector current causes emitter current to increase. Hence voltage at emitter output terminal also increases.

Thus increase in input voltage results in increase in output voltage also. Hence output voltage is in same phase with input voltage in CC amplifier. Also output voltage at emitter is approximately same as input voltage at base. Thus output follows the input, hence called Emitter follower. So voltage gain in CC configuration is approximately unity.



Features of CC amplifier:

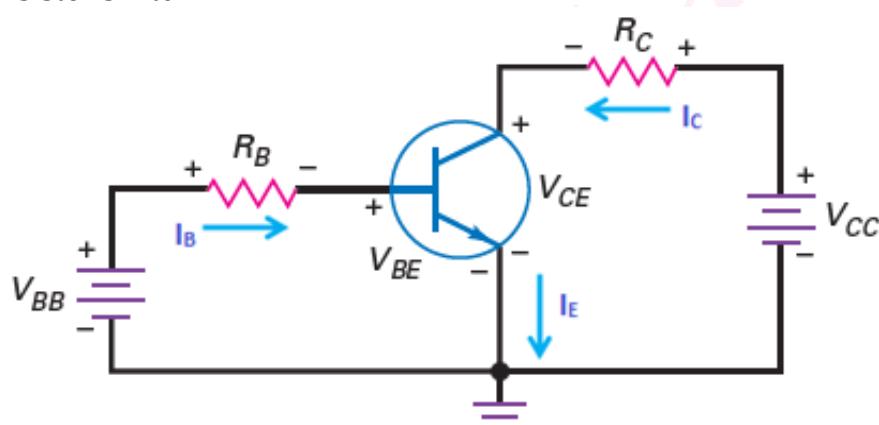
- It has very high input impedance almost ($1 \text{ M}\Omega$).
- It has very low output impedance almost (200Ω).
- It has a voltage gain of unity or (< 1).
- It has a large current gain.
- It has no phase reversal between output and input.

Application of CC amplifier:

- It is used as an impedance matching circuit in communication system.

4.12 Application of transistor as a Switch.

A transistor can be operated in three modes, active region, saturation region and cut-off region. In the active region, transistor works as an amplifier. The two operating regions of transistor **Saturation Region** (fully-ON) and the **Cut-off Region** (fully-OFF) are used to operate a transistor switch.



For the given circuit, applying KVL law at output loop,

$$V_{CC} = I_C R_C + V_{CE} \quad \dots (1)$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

Rearranging equation (1)

$$I_C = \left(-\frac{1}{R_C} \right) (V_{CE}) + \left(\frac{V_{CC}}{R_C} \right) \quad \dots (2)$$

Equation (2) is like the equation of straight line i.e. $y = mx + C$

The straight line represented by equation (2) is called **DC Load Line**.

In equation (2) when $V_{CE} = 0$,

$$I_C = \frac{V_{CC}}{R_C}$$

This is maximum possible current through transistor. Hence

$$I_{C(max)} = \frac{V_{CC}}{R_C} \quad \text{---- (3)}$$

Equation (3) is maximum possible current through transistor. So it is called **Saturation** point. Hence

$$I_{C(saturation)} = \frac{V_{CC}}{R_C}$$

Now, in equation (2) when $I_C = 0$,

$$V_{CE} = V_{CC}$$

This is maximum possible voltage across transistor. Hence

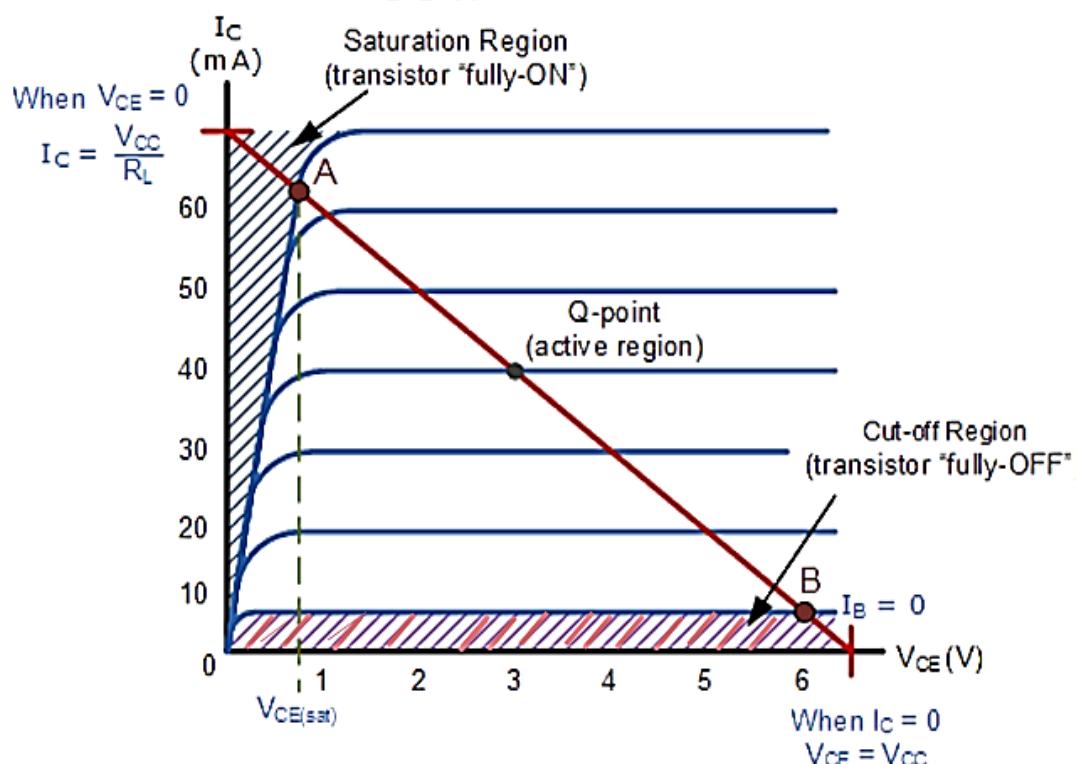
$$V_{CE(max)} = V_{CC} \quad \text{---- (4)}$$

Equation (4) is maximum possible voltage across transistor. So it is called **cut-off** point. Hence

$$V_{CE(cut-off)} = V_{CC}$$

Line joining the Saturation and cut-off point is called **DC Load Line**. It is a straight line as shown in figure. Any point/value corresponding to I_C and V_{CE} will be on this DC Load Line

The DC Load Line is shown with output characteristic of transistor.



Cut-off Region (OFF Switch):

The operating conditions of the transistor are zero input base current ($I_B=0$), zero output collector current($I_C=0$), and maximum collector voltage (V_{CE}) which results in a large depletion layer and no current flowing through the device. Therefore the transistor is switched to "Fully-OFF". Hence transistor behaves as an OFF switch.

Cut-off Characteristics:

- The input and Base are grounded (0 v)
- Base-Emitter voltage $V_{BE} < 0.7v$
- Base-Emitter junction is reverse biased
- Base-Collector junction is reverse biased
- Transistor is "fully-OFF" (Cut-off region)
- No Collector current flows ($I_C = 0$)
- $V_{OUT} = V_{CE} = V_{CC}$
- Transistor operates as an "Open switch"/ OFF Switch

Saturation Region (ON Switch):

In this region, the transistor will be biased so that the maximum amount of base current (I_B) is applied, resulting in maximum collector current ($I_C=V_{CC}/R_L$) and then resulting in the minimum collector-emitter voltage ($V_{CE} \sim 0$) drop. At this condition, the depletion layer becomes as small as the possible and maximum current flowing through the transistor. Therefore the transistor is switched "Fully-ON". Hence transistor behaves as an ON switch.

Saturation Characteristics

- The input and Base are connected to V_{CC}
- Base-Emitter voltage $V_{BE} > 0.7 v$
- Base-Emitter junction is forward biased
- Base-Collector junction is forward biased
- Transistor is "fully-ON" (saturation region)
- Max Collector current flows ($I_C = V_{CC}/R_L$)
- $V_{CE} = 0$ (ideal saturation)
- $V_{OUT} = V_{CE} = "0"$
- Transistor operates as a "Closed switch" / ON Switch

Exercise: Question Bank Unit-4

		Marks
Q:1	Explain the importance of coupling and bypass capacitor in transistor amplifier circuit.	4
Q:2	<i>Draw the circuit diagram of single stage RC coupled CE amplifier and explain it in detail with necessary waveforms and importance of coupling and bypass capacitor.</i>	7
Q:3	<i>What is AC load line? Derive the equation of AC load line and draw it. Also compare AC load line with DC load line.</i>	7
Q:4	What do you mean by faithful amplification? Explain the effect of shifting the location of operating point Q towards cut-off and saturation in transistor amplifier.	7
Q:5	What is two port network? Derive h parameters for two port network.	7
Q:6	<i>Why h parameters are called hybrid parameters. Enlist merits and demerits of h parameters.</i>	4
Q:7	Draw h parameter equivalent/hybrid equivalent circuit for two port network.	3
Q:8	<i>How transistor can be used as a two port network? Draw and explain h parameter model for CE amplifier.</i> <i>OR</i> <i>Derive h parameters for transistor CE amplifier. Also Draw and explain h parameter equivalent model for CE amplifier.</i>	7
Q:9	Draw and explain h parameter model for CB configuration.	4
Q:10	Draw and explain h parameter model for CC configuration.	4
Q:11	<i>Derive the equation of Input Impedance, Output Impedance, Voltage Gain and Current Gain for CE amplifier.</i> <i>OR</i> <i>Draw h parameter equivalent circuit for CE amplifier and derive the equation of Input Impedance, Output Impedance, Voltage Gain and Current Gain.</i> <i>OR</i> <i>Explain transistor AC analysis using h parameter model.</i>	7
Q:12	Draw and explain the operation of CB amplifier circuit with necessary waveforms.	7
Q:13	<i>Draw and explain the operation of CC amplifier circuit with necessary waveforms.</i> <i>OR</i> <i>Draw and explain the operation of Emitter Follower circuit with necessary waveforms</i>	7

Q:14	<p>Derive the expressions of Input Impedance, Output Impedance and Voltage Gain for Common Base circuit (CB amplifier).</p> <p style="text-align: center;">OR</p> <p>Draw h parameter equivalent circuit for CB amplifier and derive the equation of Input Impedance, Output Impedance and Voltage Gain.</p>	7
Q:15	<p>Derive the expressions of Input Impedance, Output Impedance and Voltage Gain for Common Collector circuit (CC amplifier).</p> <p style="text-align: center;">OR</p> <p>Draw h parameter equivalent circuit for CC amplifier and derive the equation of Input Impedance, Output Impedance and Voltage Gain.</p>	7
Q:16	<p><i>Write short note on transistor as a switch.</i></p> <p style="text-align: center;"><i>OR</i></p> <p><i>Explain the operation transistor as a Switch with necessary diagram/waveforms.</i></p>	7

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1.1 Introduction

- The bipolar junction transistor (BJT) relies on two types of charge: free electrons and holes. This is why it is called bipolar: the prefix bi stands for “two.”
- This chapter discusses another kind of transistor called the field-effect transistor (FET). This type of device is unipolar because its operation depends on only one type of charge, either free electrons or holes.
- In other words, an FET has majority carriers but not minority carriers. For most linear applications, the BJT is the preferred device.
- But there are some linear applications in which the FET is better suited because of its high input impedance and other properties. Furthermore, the FET is the preferred device for most switching applications. Why?
- Because there are no minority carriers in an FET. As a result, it can switch off faster since no stored charge has to be removed from the junction area.
- There are two kinds of unipolar transistors: JFETs and MOSFETs. The first part of this chapter discusses the junction field-effect transistor (JFET) and its applications. In later part, we discuss the metal-oxide semiconductor FET (MOSFET) and its applications.

1.2 Basic Ideas

- Figure-1a shows a piece of n-type semiconductor. The lower end is called the source, and the upper end is called the drain. The supply voltage V_{DD} forces free electrons to flow from the source to the drain.

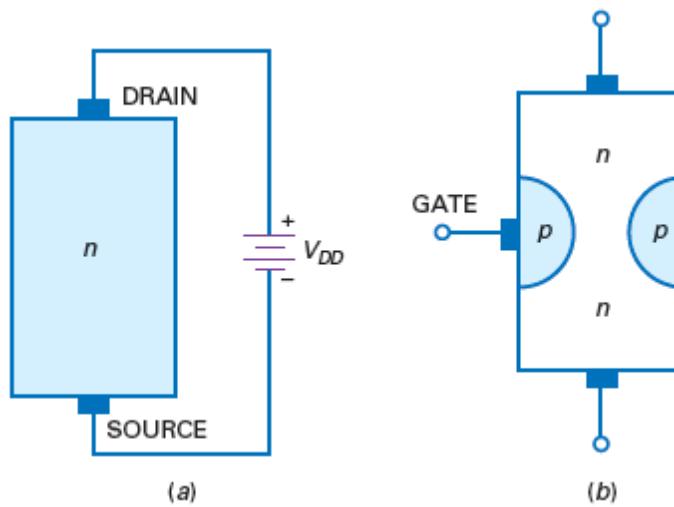


Figure-1 (a) Part of JFET; (b) single-gate JFET

- To produce a JFET, a manufacturer diffuses two areas of p-type semiconductor into the n-type semiconductor, as shown in Figure-1b. These p regions are connected internally to get a single external gate lead.

1.2.1 Field Effect

- Figure-2 shows the normal biasing voltages for a JFET. The drain supply voltage is positive, and the gate supply voltage is negative.

- The term field effect is related to the depletion layers around each p region. These depletion layers exist because free electrons diffuse from the n regions into the p regions. The recombination of free electrons and holes creates the depletion layers shown by the colored areas.

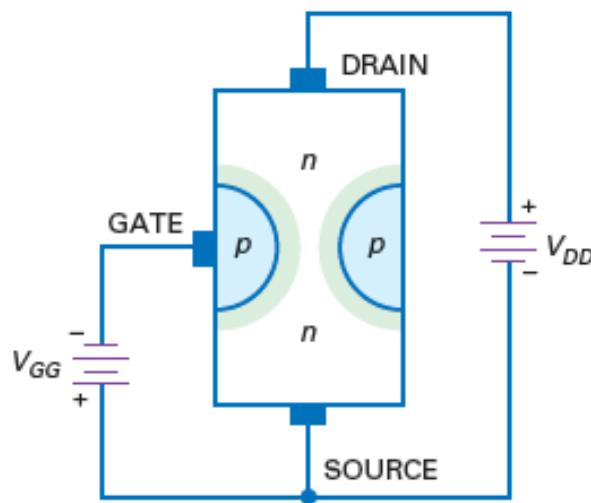


Figure-2 Normal biasing of JFET

1.2.2 Reverse Bias of Gate

- In Figure-2, the p-type gate and the n-type source form the gate-source diode. With a JFET, we always reverse-bias the gate-source diode.
- Because of reverse bias, the gate current I_G is approximately zero, which is equivalent to saying that the JFET has an almost infinite input resistance.
- A typical JFET has an input resistance in the hundreds of mega-ohms. This is the big advantage that a JFET has over a bipolar transistor. It is the reason that JFETs excel in applications in which a high input impedance is required.
- One of the most important applications of the JFET is the source follower, a circuit like the emitter follower, except that the input impedance is in the hundreds of mega-ohms for lower frequencies.

1.2.3 Gate Voltage Controls Drain Current

- In Figure-2, electrons flowing from the source to the drain must pass through the narrow channel between the depletion layers. When the gate voltage becomes more negative, the depletion layers expand and the conducting channel becomes narrower. The more negative the gate voltage, the smaller the current between the source and the drain.
- The JFET is a voltage-controlled device because an input voltage controls an output current. In a JFET, the gate-to-source voltage V_{GS} determines how much current flows between the source and the drain.
- When V_{GS} is zero, maximum drain current flows through the JFET. This is why a JFET is referred to as a normally on device. On the other hand, if V_{GS} is negative enough, the depletion layers touch and the drain current is cut off.

1.2.4 Schematic Symbol

- The JFET of Figure-2 is an n-channel JFET because the channel between the source and the drain is an n-type semiconductor. Figure-3a shows the schematic symbol for an n-channel JFET. In many low-frequency applications, the source and the drain are interchangeable because you can use either end as the source or the other end as the drain.
- The source and drain terminals are not interchangeable at high frequencies. Almost always, the manufacturer minimizes the internal capacitance on the drain side of the JFET.
- In other words, the capacitance between the gate and the drain is smaller than the capacitance between the gate and the source. You will learn more about internal capacitances and their effect on circuit action in a later chapter.
- Figure-3b shows an alternative symbol for an n-channel JFET. This symbol with its offset gate is preferred by many engineers and technicians. The offset gate points to the source end of the device, a definite advantage in complicated multistage circuits.
- There is also a p-channel JFET. The schematic symbol for a p-channel JFET, shown in Figure-3c, is similar to that for the n-channel JFET, except that the gate arrow points in the opposite direction.
- The action of a p-channel JFET is complementary; that is, all voltages and currents are reversed. To reverse-bias a p-channel JFET, the gate is made positive in respect to the source. Therefore, V_{GS} is made positive.

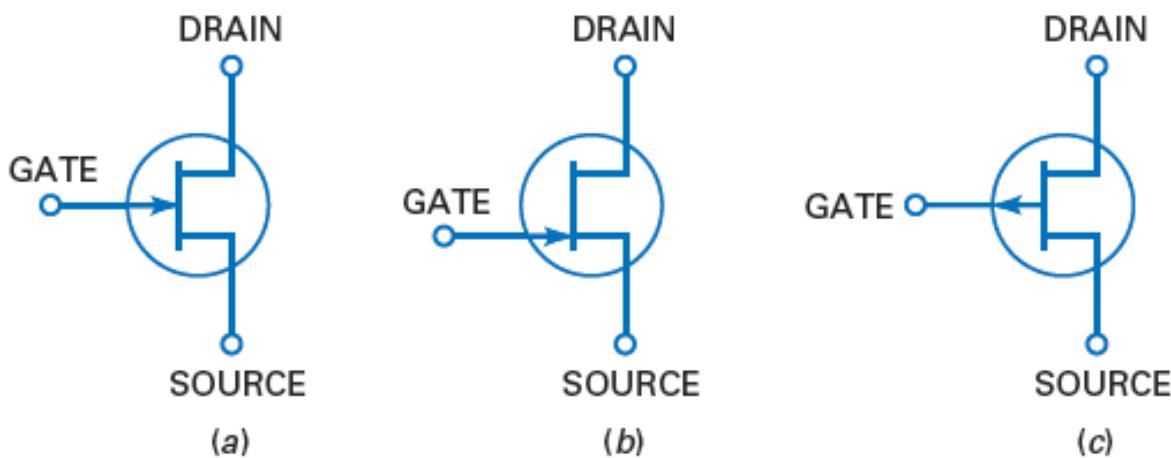


Figure-3 (a) Schematic symbol; (b) off-set-gate symbol; (c) p-channel symbol

Example-1

A 2N5486 JFET has a gate current of 1 nA when the reverse gate voltage is 20 V. What is the input resistance of this JFET?

SOLUTION

Use Ohm's law to calculate:

$$R_{in} = \frac{20\text{ V}}{1\text{ nA}} = 20,000\text{ M}\Omega$$

PRACTICE PROBLEM 11-1

In Example-1, calculate the input resistance if the JFET's gate current is 2 nA.

1.3 Difference between BJT and FET

Bipolar Junction Transistor (BJT)	Field Effect Transistor (FET)
Bipolar device. In BJT, the operation depends upon both minority and majority current carriers. Thus it is known as Bipolar device.	Unipolar device. In FET, the operation depends upon the flow of majority carriers only i.e. holes for P-Channel FET and electrons for N-Channel FET. Therefore they are called as Unipolar devices.
Lower switching speed. BJT suffers from minority carrier storage effects. So it has lower switching speed and cut off frequencies.	Higher switching speed FET does not suffer from minority carrier storage effects. So it has higher switching speed and cut off frequencies.
Current controlled device. In BJT, the base current controls the output current.	Voltage controlled device. In FET, the Gate voltage controls the output current.
Less input impedance. The input circuit of BJT is forward biased. So BJT has low input impedance.	High input impedance The input circuit of FET is reverse biased. So FET exhibits much higher input impedance ($>100\text{Mohms}$) and lower output impedance. As they have high degree of isolation between input and output, FET acts as a buffer amplifier.
Comparatively BJT has more noisy operation.	Less noisy FET don't have junctions and the current conduction is happening through N-type or P-type semiconductor material. So its operation is less noisy.
Relatively more affected by radiations Due to reduction in minority carrier lifetime, the performance of BJT is degraded by neutron radiation.	Less affected. As FET operation does not depend upon the minority carriers, they can tolerate much higher level of radiation.
Lesser thermal stability. BJT has a positive temperature coefficient at high current levels. It leads to thermal breakdown.	More thermal stability. FET has a negative temperature coefficient at high current levels. It prevents the FET from thermal breakdown issue.
In IC fabrication, BJTs are occupying more space.	FETs are easier to fabricate and occupying less space.
BJTs are cheaper to produce.	Comparatively FETs are more costly.

1.4 Drain Curves

- Figure-4a shows a JFET with normal biasing voltages. In this circuit, the gate-source voltage V_{GS} equals the gate supply voltage V_{GG} , and the drain-source voltage V_{DS} equals the drain supply voltage V_{DD} .

1.4.1 Maximum Drain Current

- If we short the gate to the source, as shown in Figure-4b, we will get maximum drain current because $V_{GS} = 0$. Figure-4c shows the graph of drain current I_D versus drain-source voltage V_{DS} for this shorted-gate condition.
- Notice how the drain current increases rapidly and then becomes almost horizontal when V_{DS} is greater than V_P .

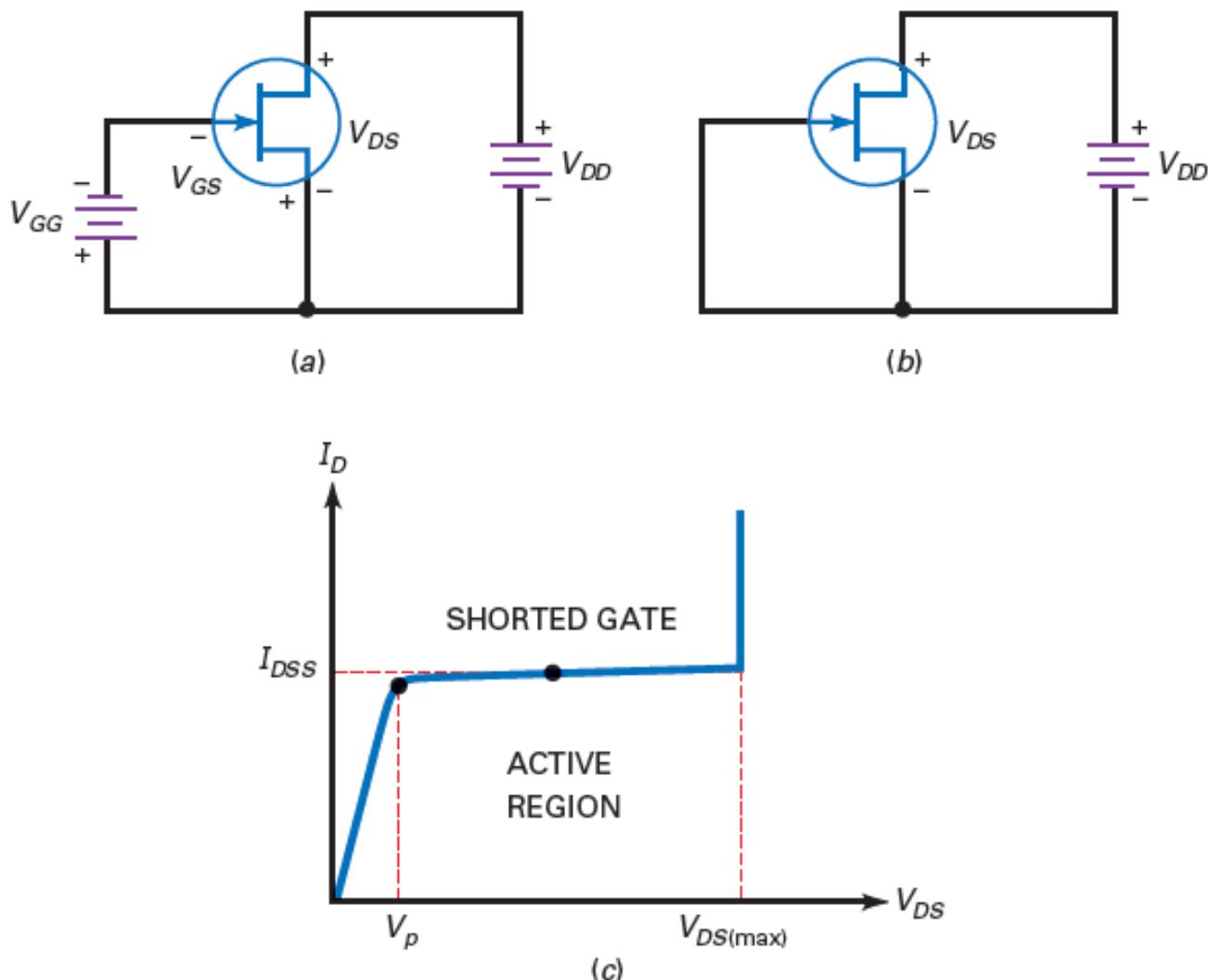


Figure-4 (a) Normal bias; (b) zero gate voltage; (c) shorted gate drain current

- Why does the drain current become almost constant? When V_{DS} increases, the depletion layers expand. When $V_{DS} = V_P$, the depletion layers are almost touching. The narrow conducting channel therefore pinches off or prevents a further increase in current.

- This is why the current has an upper limit of I_{DSS} . The active region of a JFET is between V_P and $V_{DS(max)}$. The minimum voltage V_P is called the pinch-off voltage, and the maximum voltage $V_{DS(max)}$ is the breakdown voltage. Between pinch-off and breakdown, the JFET acts like a current source of approximately I_{DSS} when $V_{GS} = 0$.
- I_{DSS} stands for the current drain to source with a shorted gate. This is the maximum drain current a JFET can produce. The data sheet of any JFET lists the value of I_{DSS} .
- This is one of the most important JFET quantities, and you should always look for it first because it is the upper limit on the JFET current.

1.4.2 The Ohmic Region

- In Figure-5, the pinch-off voltage separates two major operating regions of the JFET. The almost-horizontal region is the active region. The almost-vertical part of the drain curve below pinch-off is called the ohmic region.

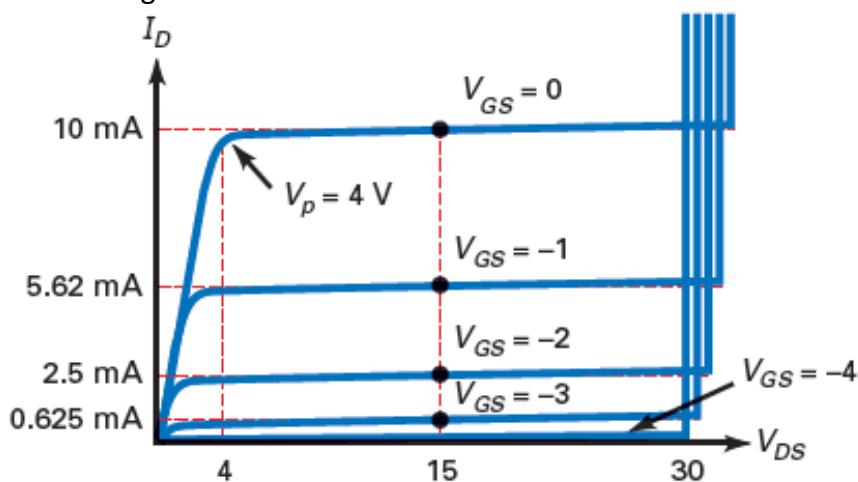


Figure-5 Drain Curves

- When operated in the ohmic region, a JFET is equivalent to a resistor with a value of approximately:

$$R_{DS} = \frac{V_P}{I_{DSS}} \quad \dots \quad (1)$$

- R_{DS} is called the ohmic resistance of the JFET. In Figure-5, $V_P = 4$ V and $I_{DSS} = 10$ mA. Therefore, the ohmic resistance is:

$$R_{DS} = \frac{4 \text{ V}}{10 \text{ mA}} = 400\Omega$$

- If the JFET is operating anywhere in the ohmic region, it has an ohmic resistance of 400 Ω .

1.4.3 Gate Cutoff Voltage

- Figure-5 shows the drain curves for a JFET with an I_{DSS} of 10 mA.
- The top curve is always for $V_{GS} = 0$, the shorted-gate condition. In this example, the pinch-off voltage is 4 V and the breakdown voltage is 30 V. The next curve down is for $V_{GS} = -1$ V, the next for $V_{GS} = -2$ V, and so on. As you can see, the more negative the gate-source voltage, the smaller the drain current.

- The bottom curve is important. Notice that a V_{GS} of -4 V reduces the drain current to almost zero. This voltage is called the gate-source cutoff voltage and is symbolized by $V_{GS(\text{off})}$ on data sheets.
- At this cutoff voltage, the depletion layers touch. In effect, the conducting channel disappears. This is why the drain current is approximately zero.
- In Figure-5, notice that $V_{GS(\text{off})} = -4 \text{ V}$ and $V_P = 4 \text{ V}$
- This is not a coincidence. The two voltages always have the same magnitude because they are the values where the depletion layers touch or almost touch. Data sheets may list either quantity, and you are expected to know that the other has the same magnitude. As an equation:

$$V_{GS(\text{off})} = -V_P \quad \text{--- (2)}$$

1.5 The Transconductance Curve

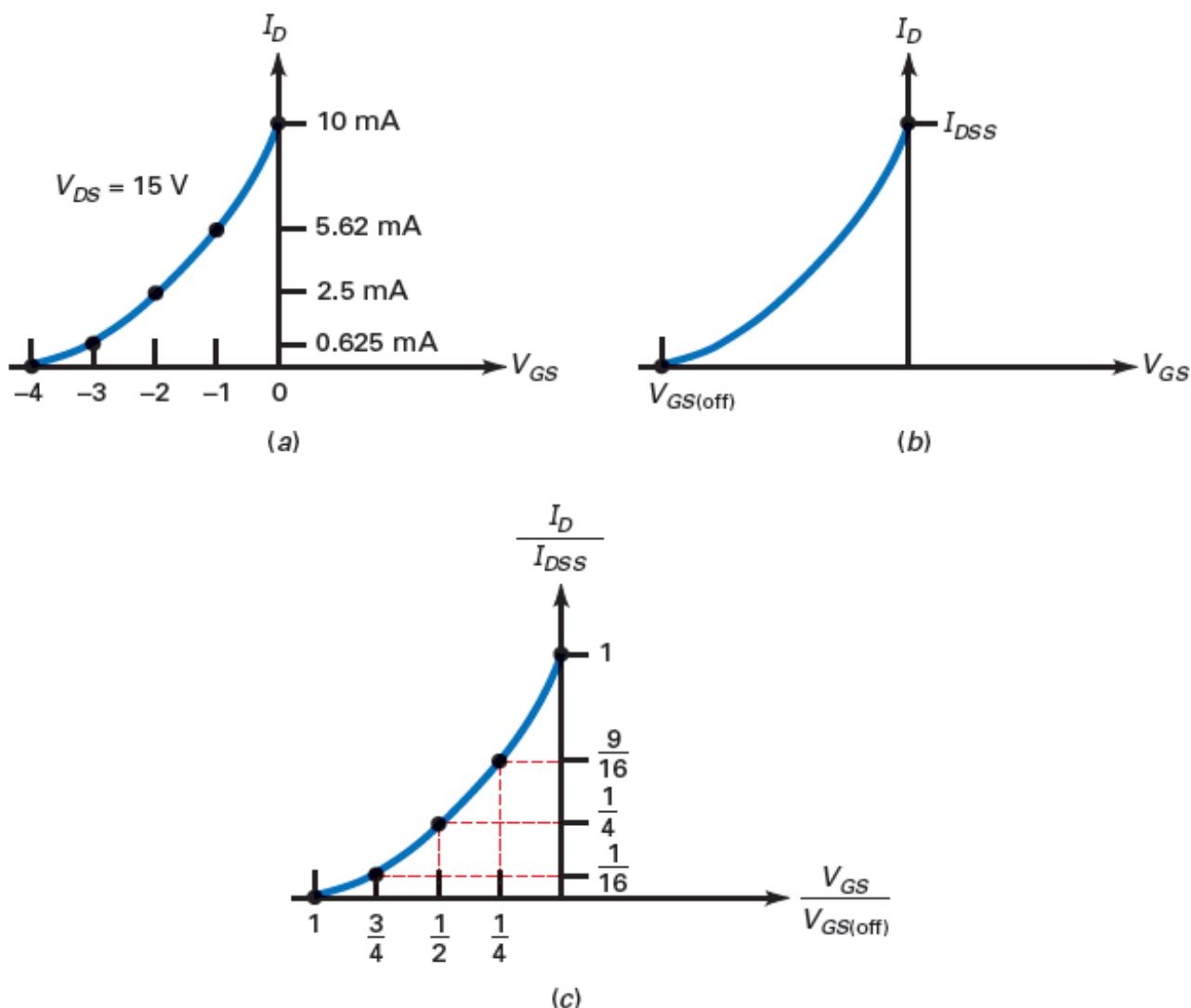


Figure 6 Transconductance curve

- The transconductance curve of a JFET is a graph of I_D versus V_{GS} . By reading the values of I_D and V_{GS} of each drain curve in Figure-5, we can plot the curve of Figure-6a. Notice that the curve is nonlinear because the current increases faster when V_{GS} approaches zero.

- Any JFET has a transconductance curve like Figure-6b. The end points on the curve are $V_{GS(off)}$ and I_{DSS} . The equation for this graph is:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 \quad \dots \quad (3)$$

- Because of the squared quantity in this equation, JFETs are often called square-law devices. The squaring of the quantity produces the nonlinear curve of Figure-6b.
- Figure-6c shows a normalized transconductance curve. Normalized means that we are graphing ratios like I_D/I_{DSS} and $V_{GS}/V_{GS(off)}$.
- In Figure-6c, the half-cutoff point

$$\frac{V_{GS}}{V_{GS(off)}} = \frac{1}{2}$$

Produces a normalized current of:

$$\frac{I_{DS}}{I_{DSS}} = \frac{1}{4}$$

- In words: When the gate voltage is half the cutoff voltage, the drain current is one quarter of maximum.

1.6 Biasing in the Ohmic Region

- The JFET can be biased in the ohmic or in the active region. When biased in the ohmic region, the JFET is equivalent to a resistance. When biased in the active region, the JFET is equivalent to a current source. In this section, we discuss gate bias, the method used to bias a JFET in the ohmic region.

1.6.1 Gate Bias

- Figure-7a shows gate bias. A negative gate voltage of $-V_{GG}$ is applied to the gate through biasing resistor R_G . This sets up a drain current that is less than I_{DSS} .
- When the drain current flows through R_D , it sets up a drain voltage of:

$$V_D = V_{DD} - I_D R_D \quad \dots \quad (4)$$

- Gate bias is the worst way to bias a JFET in the active region because the Q point is too unstable.
- For example, a 2N5459 has the following spreads between minimum and maximum: I_{DSS} varies from 4 to 16 mA, and $V_{GS(off)}$ varies from -2 to -8 V.
- Figure-7b shows the minimum and maximum transconductance curves. If a gate bias of -1 V is used with this JFET, we get the minimum and maximum Q points shown. Q_1 has a drain current of 12.3 mA, and Q_2 has a drain current of only 1 mA.

1.6.2 Hard Saturation

- Although not suitable for active-region biasing, gate bias is perfect for ohmic region biasing because stability of the Q point does not matter. Figure-7c shows how to bias a JFET in the ohmic region. The upper end of the dc load line has a drain saturation current of:

$$I_{D(sat)} = \frac{V_{DD}}{R_D}$$

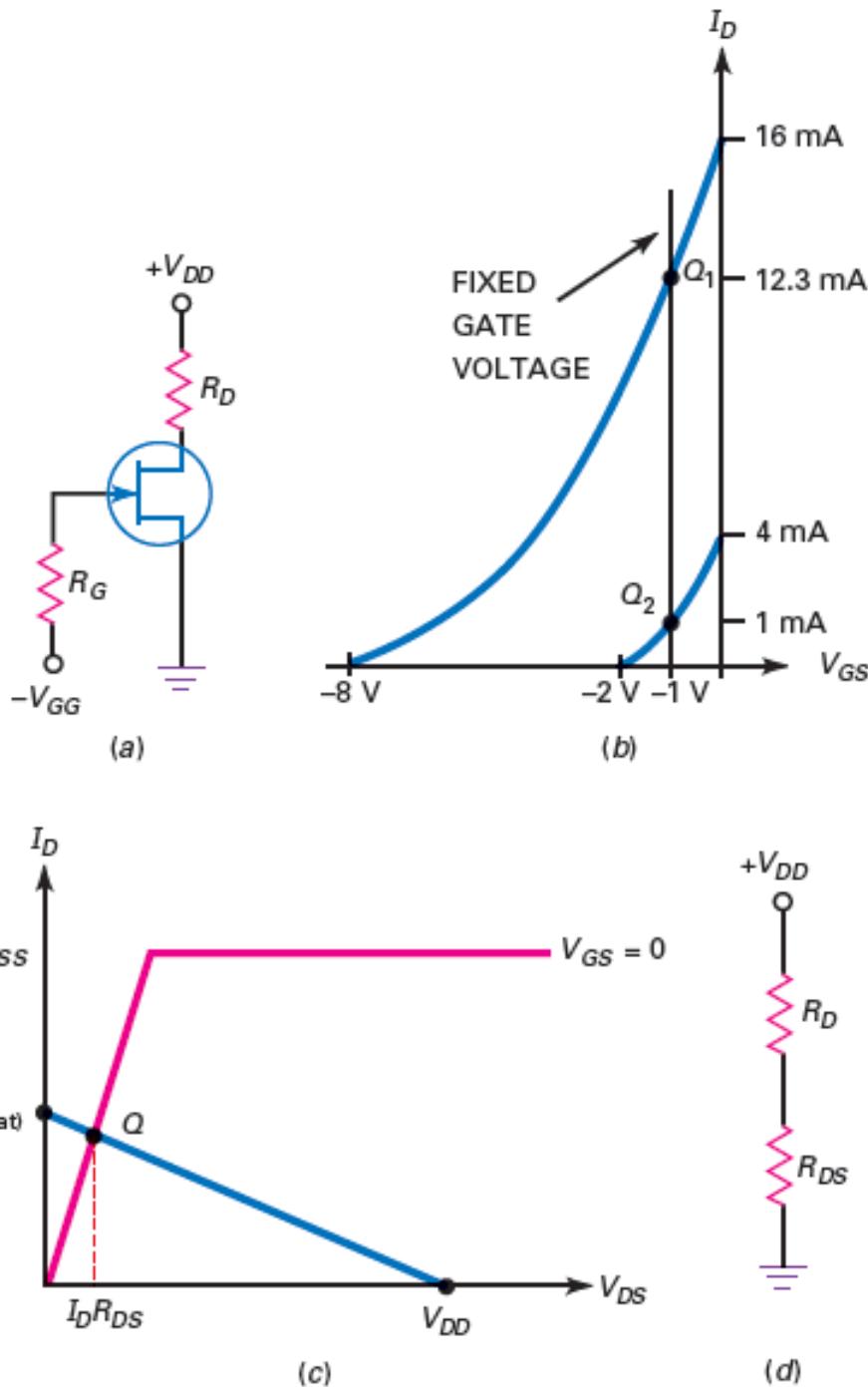


Figure-7 (a) Gate bias; (b) Q point unstable in active region; (c) biased in ohmic region; (d) JFET is equivalent to resistance

- To ensure that a JFET is biased in the ohmic region, all we need to do is use $V_{GS} = 0$ and:

$$I_{D(sat)} \ll I_{DSS} \quad \text{--- (5)}$$

- The symbol \ll means “much less than.” This equation says that the drain saturation current must be much less than the maximum drain current. For instance, if a JFET has $I_{DSS} = 10 \text{ mA}$, hard saturation will occur if $V_{GS} = 0$ and $I_{D(sat)} = 1 \text{ mA}$.

- When a JFET is biased in the ohmic region, we can replace it by a resistance of R_{DS} , as shown in Figure-7d. With this equivalent circuit, we can calculate the drain voltage. When R_{DS} is much smaller than R_D , the drain voltage is close to zero.

1.7 Biasing in the Active Region

- JFET amplifiers need to have a Q point in the active region. Because of the large spread in JFET parameters, we cannot use gate bias. Instead, we need to use other biasing methods. Some of these methods are similar to those used with bipolar junction transistors.
- The choice of analysis technique depends on the level of accuracy needed. For example, when doing preliminary analysis and troubleshooting of biasing circuits, it is often desirable to use ideal values and circuit approximations.
- In JFET circuits, this means that we will often ignore V_{GS} values. Usually, the ideal answers will have an error of less than 10 percent. When closer analysis is called for, we can use graphical solutions to determine a circuit's Q point.
- If you are designing JFET circuits or need even greater accuracy, you should use a circuit simulator like Multisim.

1.7.1 Self-Bias

- Figure-8a shows self-bias. Since drain current flows through the source resistor R_S , a voltage exists between the source and ground, given by:

$$V_S = I_D R_S \quad \text{--- (6)}$$

- Since V_G is zero:

$$V_{GS} = -I_D R_S \quad \text{--- (7)}$$

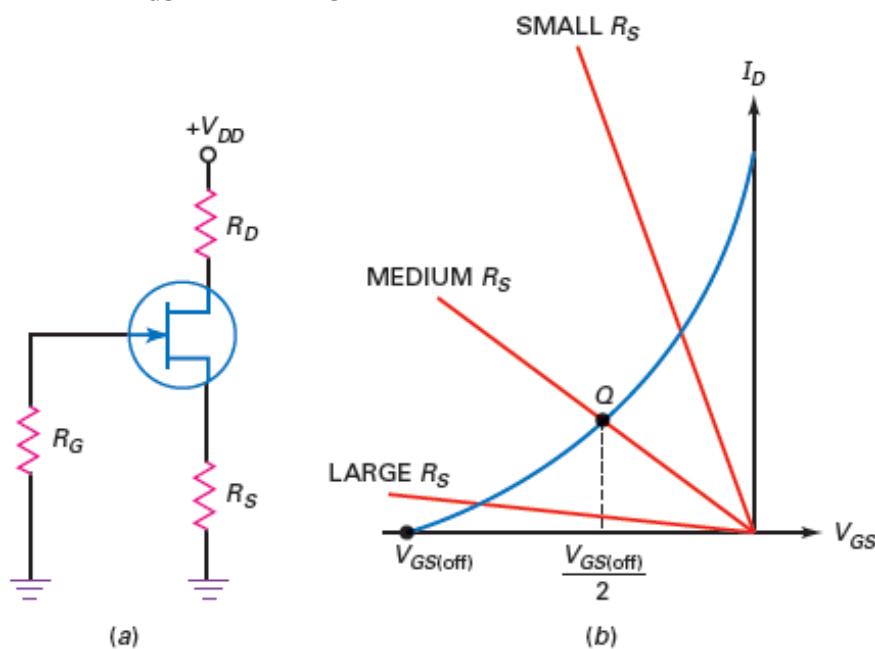


Figure-8 Self Bias

- This says that the gate-source voltage equals the negative of the voltage across the source resistor.

- Basically, the circuit creates its own bias by using the voltage developed across R_s to reverse-bias the gate. Figure-8b shows the effect of different source resistors. There is a medium value of R_s at which the gate-source voltage is half of the cutoff voltage. An approximation for this medium resistance is:

$$R_s \approx R_{DS} \quad \dots \dots \dots \quad (8)$$

- This equation says that the source resistance should equal the ohmic resistance of the JFET. When this condition is satisfied, the V_{GS} is roughly half the cutoff voltage and the drain current is roughly one-quarter of I_{DSS} .
- When a JFET's transconductance curves are known, we can analyze a self-bias circuit using graphical methods. Suppose a self-bias JFET has the transconductance curve shown in Figure-9.

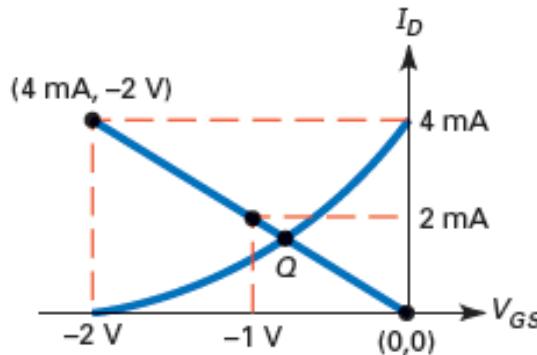


Figure-9 Self bias Q point

- The maximum drain current is 4 mA, and the gate voltage has to be between 0 and -2 V. By graphing Eq. (7), we can find out where it intersects the transconductance curve and determine the values of V_{GS} and I_D . Since Eq. (7) is a linear equation, all we have to do is plot two points and draw a line through them.
- Suppose the source resistance is 500 Ω. Then Eq. (7) becomes:

$$V_{GS} = -ID (500 \Omega)$$

- Since any two points can be used, we choose the two convenient points corresponding to

$$I_D = -(0)(500 \Omega) = 0$$

Therefore, the coordinates for the first point are (0, 0), which is the origin. To get the second point, find V_{GS} for $I_D = I_{DSS}$. In this case, $I_D = 4$ mA and $V_{GS} = -(4 \text{ mA})(500 \Omega) = -2$ V; therefore, the coordinates of the second point are at (4 mA, -2 V).

- We now have two points on the graph of Eq. (7). The two points are (0, 0) and (4 mA, -2 V). By plotting these two points as shown in Figure-9, we can draw a straight line through the two points as shown.
- This line will, of course, intersect the transconductance curve. This intersection point is the operating point of the self-biased JFET. As you can see, the drain current is slightly less than 2 mA, and the gate-source voltage is slightly less than -1 V.
- In summary, here is a process for finding the Q point of any self-biased JFET, provided you have the transconductance curve. If the curve is not available, you can use the and I_{DSS} rated values, along with the square law equation (3), to develop one:

 - Multiply I_{DSS} by R_s to get V_{GS} for the second point.
 - Plot the second point (I_{DSS} , V_{GS}).

3. Draw a line through the origin and the second point.
 4. Read the coordinates of the intersection point.
- The Q point with self-bias is not extremely stable. Because of this, self-bias is used only with small-signal amplifiers. This is why you may see self-biased JFET circuits near the front end of communication receivers where the signal is small.

1.7.2 Voltage-Divider Bias

- Figure-10a shows voltage-divider bias. The voltage divider produces a gate voltage that is a fraction of the supply voltage.

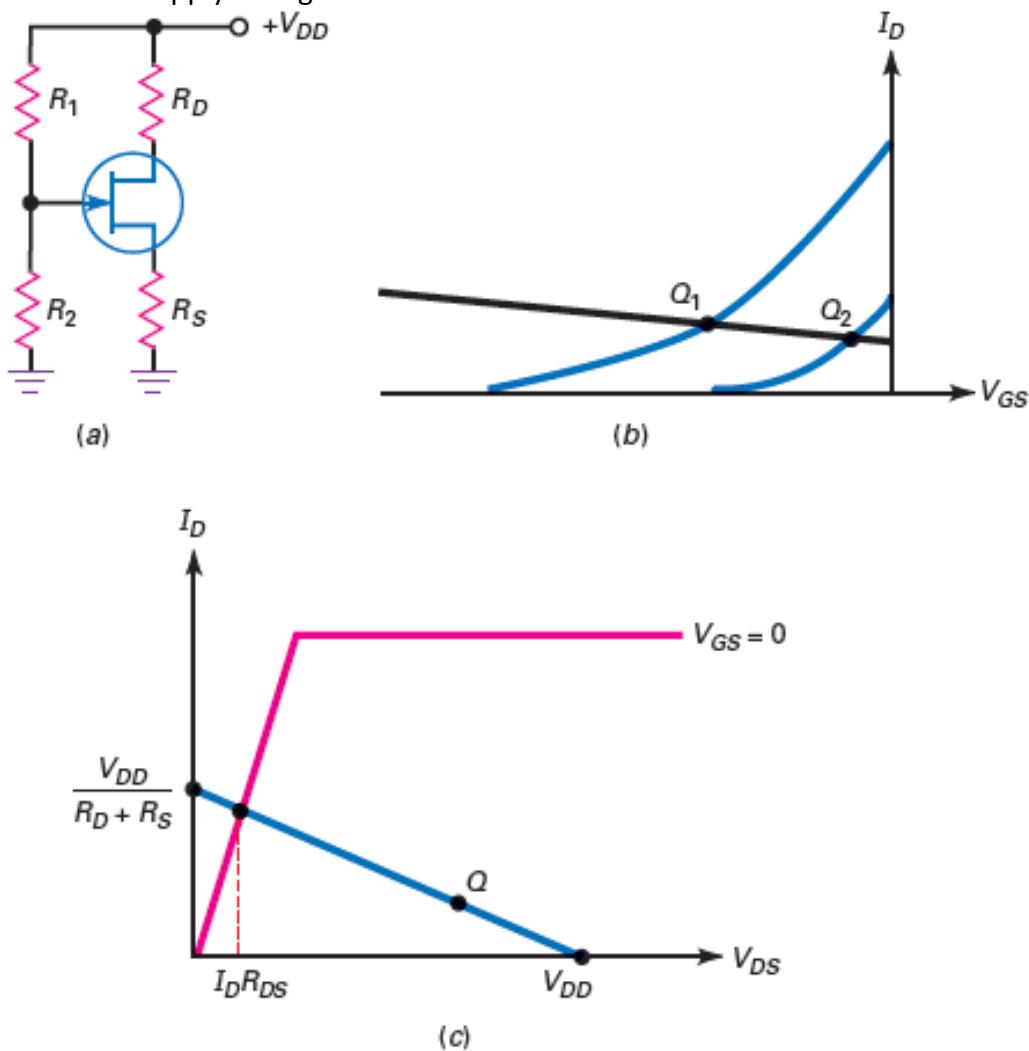


Figure-10 Voltage-divider bias

- By subtracting the gate-source voltage, we get the voltage across the source resistor:
- $$V_S = V_G - V_{GS} \quad \dots \quad (9)$$
- Since V_{GS} is a negative, the source voltage will be slightly larger than the gate voltage. When you divide this source voltage by the source resistance, you get the drain current:

$$I_D = \frac{V_G - V_{GS}}{R_S} \approx \frac{V_G}{R_S} \quad \dots \quad (10)$$

- When the gate voltage is large, it can swamp out the variations in V_{GS} from one JFET to the next. Ideally, the drain current equals the gate voltage divided by the source resistance. As a result, the drain current is almost constant for any JFET, as shown in Figure-10b.
- Figure-10c shows the dc load line. For an amplifier, the Q point has to be in the active region. This means that V_{DS} must be greater than $I_D R_{DS}$ (ohmic region) and less than V_{DD} (cutoff).
- When a large supply voltage is available, voltage-divider bias can set up a stable Q point. When more accuracy is needed in determining the Q point for a voltage divider bias circuit, a graphical method can be used.
- This is especially true when the minimum and maximum V_{GS} values for a JFET vary several volts from each other. In Figure-10a, the voltage applied to the gate is:

$$V_G = \frac{R_2}{R_1+R_2} (V_{DD}) \quad (11)$$

- Using transconductance curves, as in Figure-11, plot the V_G value on the horizontal, or x-axis, of the graph. This becomes one point on our bias line.

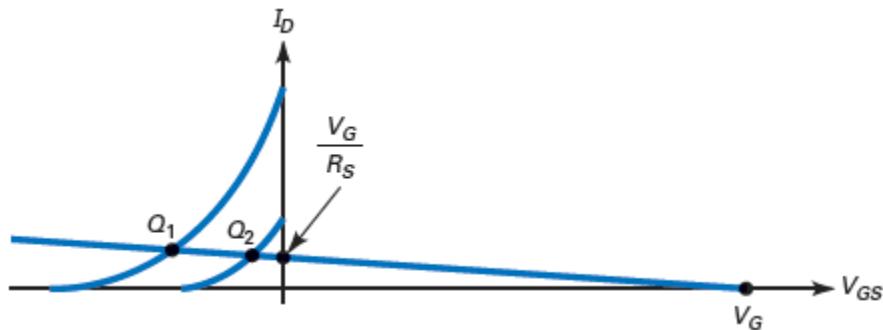


Figure-11 VDB Q point

- To get the second point, use Eq. (10) with $V_{GS} = 0$ V to determine I_D . This second point, where $I_D = V_G/R_S$, is plotted on the vertical, or y-axis, of the transconductance curve.
- Next, draw a line between these two points and extend the line so it intersects the transconductance curves. Finally, read the coordinates of the intersection points.

1.7.3 Two-Supply Source Bias

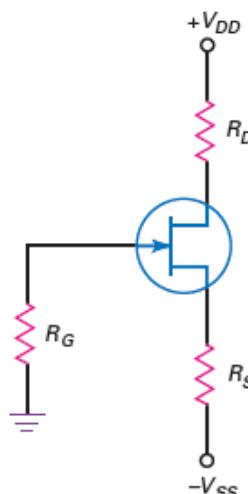


Figure-12 Two-supply source bias

- Figure-12 shows two-supply source bias. The drain current is given by:

$$I_D = \frac{V_{SS} - V_{GS}}{R_S} \approx \frac{V_{SS}}{R_S} \quad \dots \dots \dots \quad (12)$$

- Again, the idea is to swamp out the variations in V_{GS} by making V_{SS} much larger than V_{GS} . Ideally, the drain current equals the source supply voltage divided by the source resistance.
- In this case, the drain current is almost constant in spite of JFET replacement and temperature change.

1.7.4 Current-Source Bias

- When the drain supply voltage is not large, there may not be enough gate voltage to swamp out the variations in V_{GS} . In this case, a designer may prefer to use the current-source bias of Figure-13a. In this circuit, the bipolar junction transistor pumps a fixed current through the JFET. The drain current is given by:

$$I_D = \frac{V_{EE} - V_{BE}}{R_E} \quad \dots \dots \dots \quad (13)$$

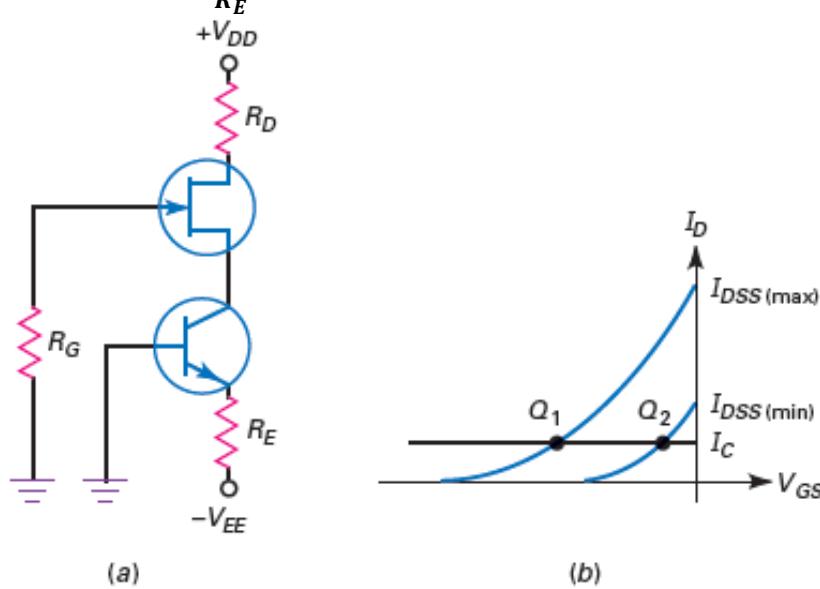


Figure-13 Current-source bias

- Figure-13b illustrates how effective current-source bias is. Both Q points have the same current. Although V_{GS} is different for each Q point, V_{GS} no longer has an effect on the value of drain current.

1.8 Transconductance

- To analyze JFET amplifiers, we need to discuss transconductance, designated gm and defined as:

$$g_m = \frac{i_d}{v_{gs}} \quad \dots \dots \dots \quad (14)$$

- This says that transconductance equals the ac drain current divided by the ac gate-source voltage. Transconductance tells us how effective the gate-source voltage is in controlling the drain current. The higher the transconductance, the more control the gate voltage has over the drain current.

- For instance, if $i_d = 0.2 \text{ mA}_{\text{p-p}}$ when $v_{gs} = 0.1 \text{ V}_{\text{p-p}}$, then:

$$g_m = \frac{0.2 \text{ mA}}{0.1 \text{ V}} = 2(10^{-3})\text{V} = 2000 \mu\text{V}$$

- On the other hand, if $i_d = 1 \text{ mA}_{\text{p-p}}$ when $v_{gs} = 0.1 \text{ V}_{\text{p-p}}$, then:

$$g_m = \frac{1 \text{ mA}}{0.1 \text{ V}} = 10,000 \mu\text{V}$$

- In the second case, the higher transconductance means that the gate is more effective in controlling the drain current.

1.8.1 Siemen

- The unit mho is the ratio of current to voltage. An equivalent and modern unit for the mho is the Siemen(S), so the foregoing answers can be written as 2000 μS and 10,000 μS . On data sheets, either quantity (mho or Siemen) may be used. Data sheets may also use the symbol g_{fs} instead of g_m .
- As an example, the data sheet of a 2N5451 lists a g_{fs} of 2000 μS for a drain current of 1 mA. This is identical to saying that the 2N5451 has a g_m of 2000 μmho for a drain current of 1 mA.

1.8.2 Slope of Transconductance Curve

- Figure-14a brings out the meaning of g_m in terms of the transconductance curve. Between points A and B, a change in V_{GS} produces a change in I_D . The change in I_D divided by the change in V_{GS} is the value of g_m between A and B.
- If we select another pair of points farther up the curve at C and D, we get a bigger change in I_D for the same change in V_{GS} . Therefore, g_m has a larger value higher up the curve. Stated another way, g_m is the slope of the transconductance curve. The steeper the curve is at the Q point, the higher the transconductance.

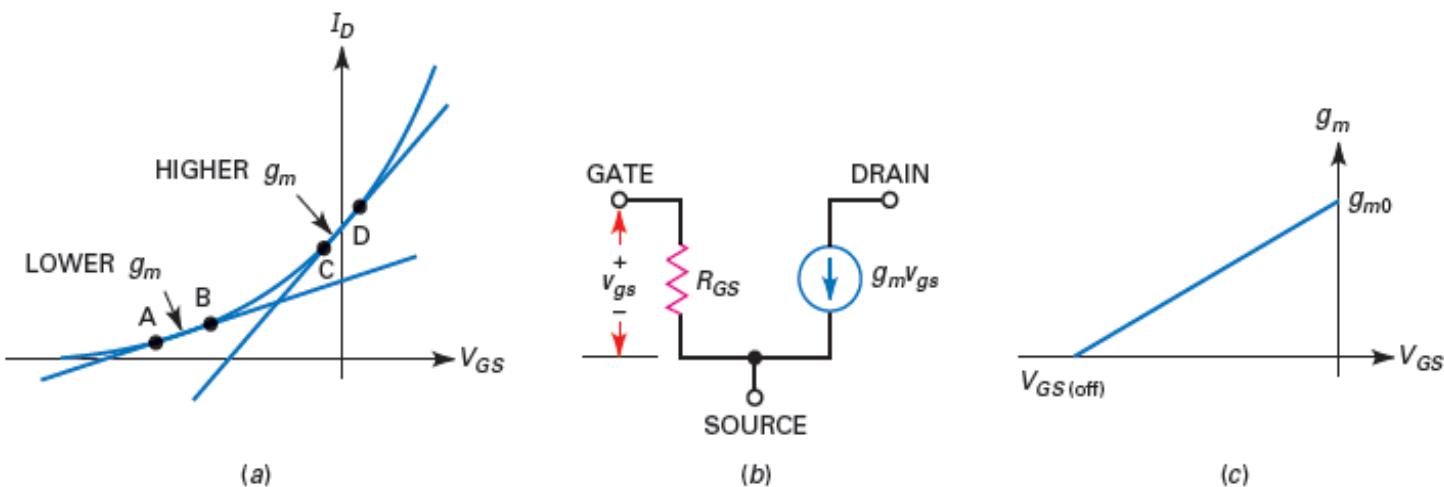


Figure-14 (a) Transconductance; (b) ac-equivalent circuit; (c) variation of g_m

- Figure-14b shows an ac-equivalent circuit for a JFET. A very high resistance R_{GS} is between the gate and the source. The drain of a JFET acts like a current source with a value of $g_m v_{gs}$. Given the values of g_m and v_{gs} , we can calculate the ac drain current.

1.8.3 Transconductance and Gate-Source Cutoff Voltage

- The quantity $V_{GS(off)}$ is difficult to measure accurately. On the other hand, I_{DSS} and g_{m0} are easy to measure with high accuracy. For this reason, $V_{GS(off)}$ is often calculated with the following equation:

$$V_{GS(off)} = \frac{-2I_{DSS}}{g_{m0}} \quad (15)$$

- In this equation, g_{m0} is the value of transconductance when $V_{GS} = 0$. Typically, a manufacturer will use the foregoing equation to calculate the value of $V_{GS(off)}$ for use on data sheets.
- The quantity g_{m0} is the maximum value of g_m for a JFET because it occurs when $V_{GS} = 0$. When V_{GS} becomes negative, g_m decreases. Here is the equation for calculating g_m for any value of V_{GS} :

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right) \quad (16)$$

- Notice that g_m decreases linearly when V_{GS} becomes more negative, as shown in Figure-14c. Changing the value of g_m is useful in automatic gain control, which is discussed later.

1.9 JFET Amplifiers

- Figure-15a shows a common-source (CS) amplifier. The coupling and bypass capacitors are ac shorts. Because of this, the signal is coupled directly into the gate. Since the source is bypassed to ground, all of the ac input voltage appears between the gate and the source.

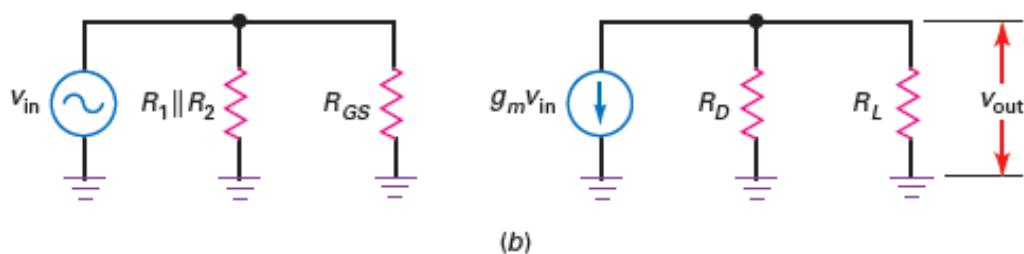
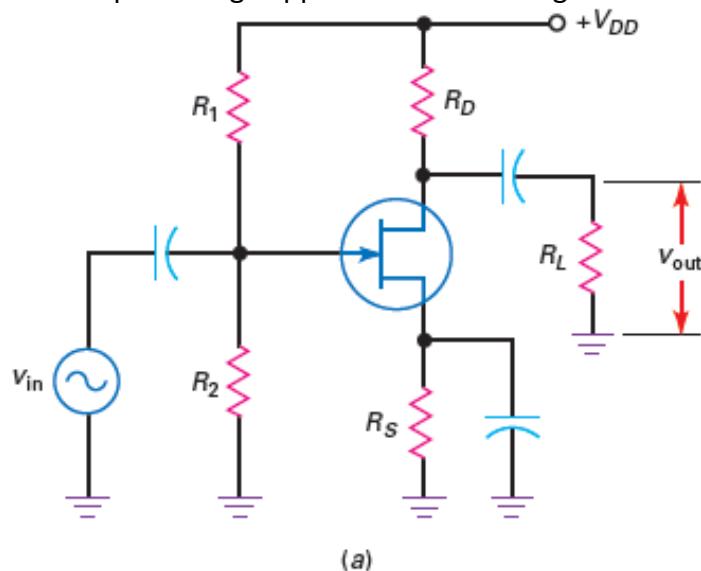


Figure-15 (a) CS amplifier; (b) ac-equivalent circuit

- This produces an ac drain current. Since the ac drain current flows through the drain resistor, we get an amplified and inverted ac output voltage. This output signal is then coupled to the load resistor.

1.9.1 Voltage Gain of CS Amplifier

- Figure-15b shows the ac-equivalent circuit. The ac drain resistance r_d is defined as:

$$r_d = R_D \parallel R_L$$

- The voltage gain is:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_m V_{in} r_d}{V_{in}}$$

- which simplifies to:

$$A_v = g_m r_d \quad \dots \quad (17)$$

- This says that the voltage gain of a CS amplifier equals the transconductance times the ac drain resistance.

1.9.2 Input and Output Impedance of CS Amplifier

- Since a JFET normally has a reverse biased gate-source junction, its input resistance at the gate R_{GS} is very large. R_{GS} can be approximated by using values taken
- from the JFET's data sheet and can be found by:

$$R_{GS} = \frac{V_{GS}}{I_{GSS}} \quad \dots \quad (18)$$

- As an example, if I_{GSS} is -2.0 nA when V_{GS} is -15 V, R_{GS} would equal 7500 MΩ. As shown in Figure-15b, the input impedance of the stage is:

$$Z_{in\ (stage)} = R_1 \parallel R_2 \parallel R_{GS}$$

- Because R_{GS} is normally very large, as compared to the input biasing resistors, the input impedance of the stage can be reduced to:

$$Z_{in\ (stage)} = R_1 \parallel R_2 \quad \dots \quad (19)$$

- In a CS amplifier, $Z_{out\ (stage)}$ looks back into the circuit from the load resistor R_L . In Figure-15b, the load resistance sees R_D in parallel with a constant current source, which ideally is an open. Therefore:

$$Z_{out\ (stage)} = R_D \quad \dots \quad (20)$$

1.9.3 Source Follower

- Figure-16a shows a common-drain (CD) amplifier, also known as a source follower. The input signal drives the gate, and the output signal is coupled from the source to the load resistor. Like the emitter follower, the source follower has a voltage gain less than 1.
- The main advantage of the source follower is its very high input resistance and its low output resistance. Often, you will see a source follower used at the front end of a system, followed by bipolar stages of voltage gain.
- In Figure-16b, the ac source resistance is defined as:

$$r_s = R_S \parallel R_L$$

- The voltage gain of a source follower is found by:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{i_d r_s}{v_{gs} + i_d r_s} = \frac{v_{gs} g_m r_s}{v_{gs} + v_{gs} g_m r_s}$$

Where $i_d = g_m v_{gs}$

Which reduces to:

$$A_v = \frac{g_m r_s}{1 + g_m r_s} \quad \text{--- (21)}$$

- Because the denominator is always greater than the numerator, the voltage gain is always less than 1.

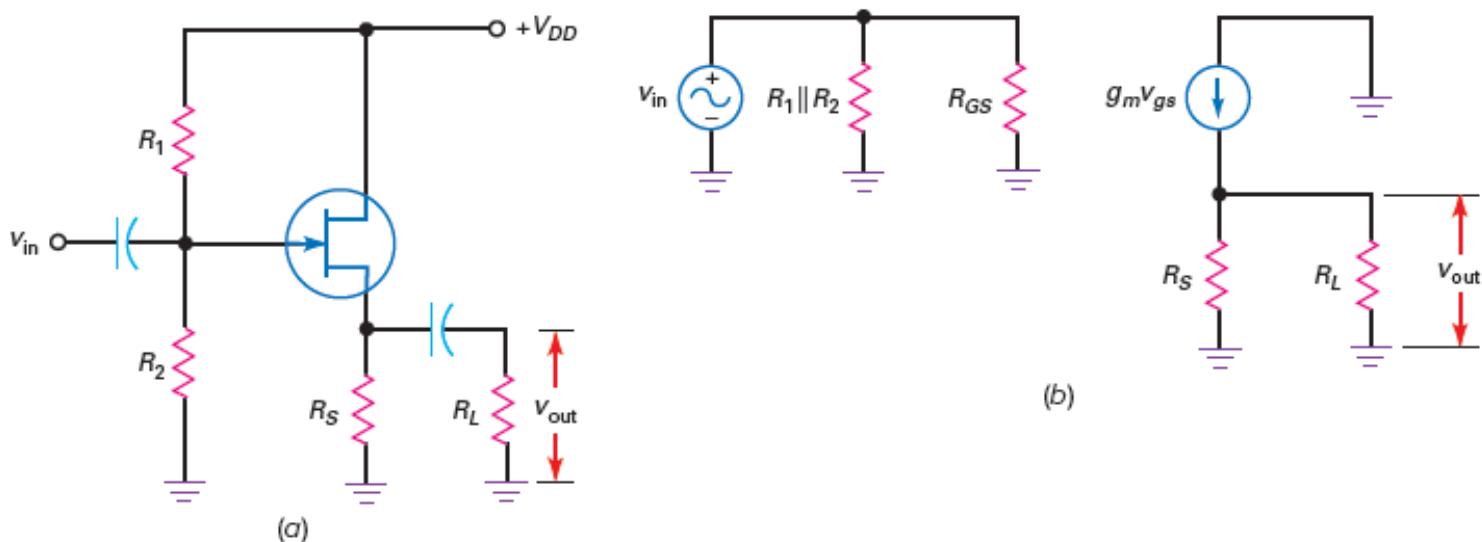


Figure-16 (a) Source follower (b) ac-equivalent

- Figure-16b shows that the input impedance of the source follower is the same as the CS amplifier:

$$Z_{in\ (stage)} = R_1 \parallel R_2 \parallel R_{GS}$$

- Which simplifies to:

$$Z_{in\ (stage)} = R_1 \parallel R_2$$

- The output impedance $Z_{out\ (stage)}$ is found by looking back into the circuit from the load:

$$Z_{out\ (stage)} = R_s \parallel R_{in\ (source)}$$

- The resistance looking into the JFET's source is:

$$R_{in\ (source)} = \frac{V_{source}}{I_{source}} = \frac{v_{gs}}{i_s}$$

Since, $v_{gs} = \frac{i_d}{g_m}$ and $i_d = i_s$ and $R_{in\ (source)} = \frac{\frac{i_d}{g_m}}{i_d} = \frac{1}{g_m}$

- Therefore, the output impedance of the source follower is:

$$Z_{out\ (stage)} = R_s \parallel \frac{1}{g_m} \quad \text{--- (22)}$$

1.10 The JFET Analog Switch

- Besides the source follower, another major application of the JFET is analog switching. In this application, the JFET acts as a switch that either transmits or blocks a small ac signal. To get this type of action, the gate-source voltage V_{GS} has only two values: either zero or a value that is greater than $V_{GS(off)}$. In this way, the JFET operates either in the ohmic region or in the cutoff region.

1.10.1 Shunt Switch

- Figure-17a shows a JFET shunt switch. The JFET is either conducting or cut off, depending on whether V_{GS} is high or low. When V_{GS} is high (0 V), the JFET operates in the ohmic region. When V_{GS} is low, the JFET is cut off. Because of this, we can use Figure-17b as an equivalent circuit.

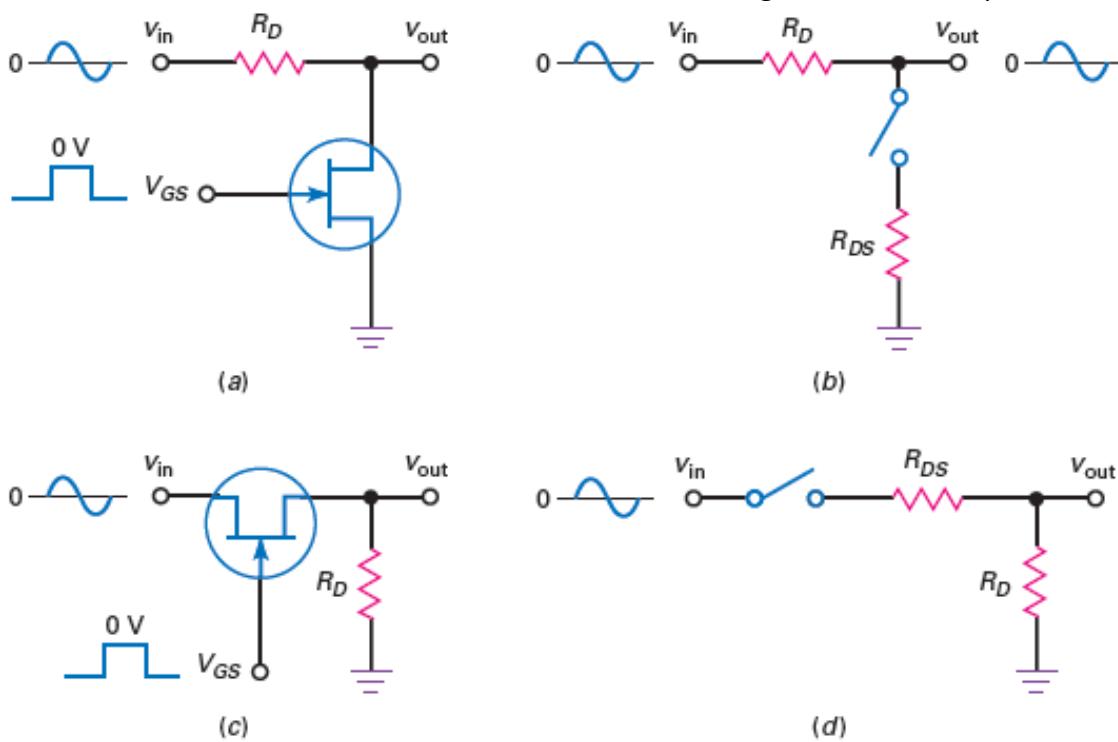


Figure-17 JFET analog switches: (a) Shunt type; (b) shunt-equivalent circuit; (c) series type; (d) series-equivalent circuit

- For normal operation, the ac input voltage must be a small signal, typically less than 100 mV. A small signal ensures that the JFET remains in the ohmic region when the ac signal reaches its positive peak. Also, R_D is much greater than R_{DS} to ensure hard saturation: $R_D \gg R_{DS}$
- When V_{GS} is high, the JFET operates in the ohmic region and the switch of Figure-17b is closed. Since R_{DS} is much smaller than R_D , V_{out} is much smaller than V_{in} . When V_{GS} is low, the JFET cuts off and the switch of Figure-17b opens. In this case, $V_{out} = V_{in}$. Therefore, the JFET shunt switch either transmits the ac signal or blocks it.

1.10.2 Series Switch

- Figure-17c shows a JFET series switch, and Figure-17d is its equivalent circuit. When V_{GS} is high, the switch is closed and the JFET is equivalent to a resistance of R_{DS} .

- In this case, the output approximately equals the input. When V_{GS} is low, the JFET is open and V_{out} is approximately zero. The on-off ratio of a switch is defined as the maximum output voltage divided by the minimum output voltage:

$$\text{On - Off Ratio} = \frac{V_{out(\max)}}{V_{out(\min)}} \quad \dots \quad (23)$$

- When a high on-off ratio is important, the JFET series switch is a better choice because its on-off ratio is higher than that of the JFET shunt switch.

1.10.3 Chopper

- Figure-18 shows a JFET chopper. The gate voltage is a continuous square wave that continuously switches the JFET on and off. The input voltage is a rectangular pulse with a value of V_{DC} . Because of the square wave on the gate, the output is chopped (switched on and off), as shown.

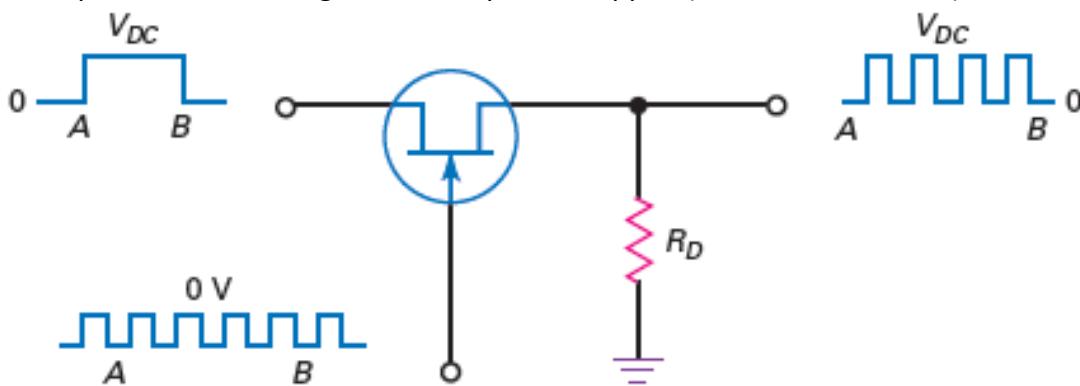


Figure-18 Chopper

- A JFET chopper can use either a shunt or a series switch. Basically, the circuit converts a dc input voltage to a square-wave output. The peak value of the chopped output is V_{DC} . As will be described later, a JFET chopper can be used to build a dc amplifier, a circuit that can amplify frequencies all the way down to zero frequencies.

1.11 Other JFET Applications

- A JFET cannot compete with a bipolar transistor for most amplifier applications. But its unusual properties make it a better choice in special applications. In this section, we discuss those applications where a JFET has a clear-cut advantage over the bipolar transistor.

1.11.1 Multiplexing

- Multiplex means “many into one.” Figure-19 shows an analog multiplexer, a circuit that steers one or more of the input signals to the output line.
- Each JFET acts like a series switch. The control signals (V_1 , V_2 , and V_3) turn the JFETs on and off. When a control signal is high, its input signal is transmitted to the output.
- For instance, if V_1 is high and the others are low, the output is a sine wave. If V_2 is high and the others are low, the output is a triangular wave. When V_3 is the high input, the output is a square wave.
- Normally, only one of the control signals is high; this ensures that only one of the input signals is transmitted to the output.

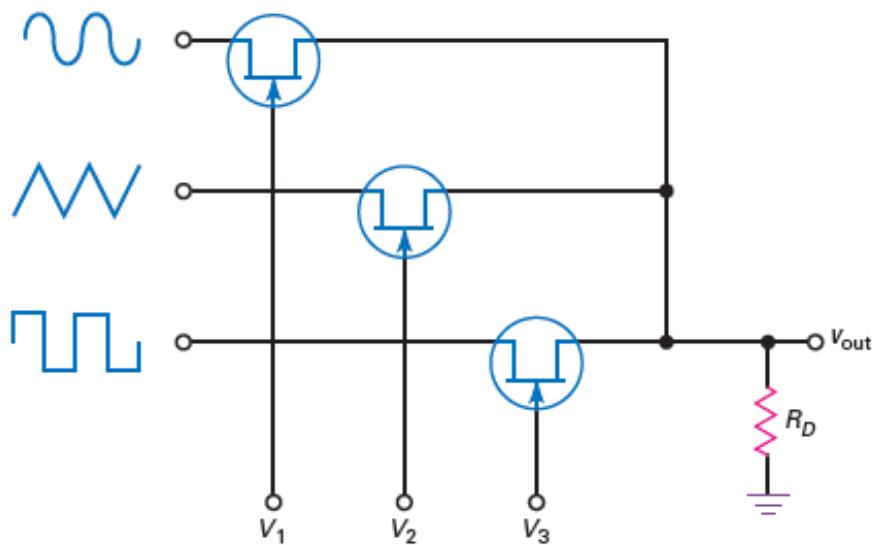
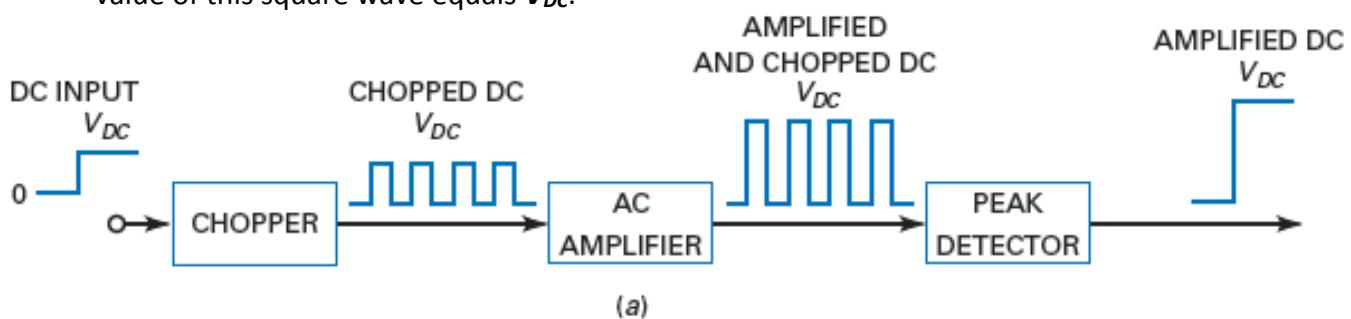


Figure-19 Multiplexer

1.11.2 Chopper Amplifiers

- We can build a direct-coupled amplifier by leaving out the coupling and bypass capacitors and connecting the output of each stage directly to the input of the next stage. In this way, dc voltages are coupled, as are ac voltages.
- Circuits that can amplify dc signals are called dc amplifiers. The major disadvantage of direct coupling is drift, a slow shift in the final dc output voltage produced by minor changes in supply voltage, transistor parameters, and temperature variations.
- Figure-20a shows one way to overcome the drift problem of direct coupling. Instead of using direct coupling, we use a JFET chopper to convert the input dc voltage to a square wave. The peak value of this square wave equals V_{DC} .



(a)



(b)

Figure-20 Chopper amplifier

- Because the square wave is an ac signal, we can use a conventional ac amplifier, one with coupling and bypass capacitors. The amplified output can then be peak detected to recover an amplified dc signal.
- A chopper amplifier can amplify low-frequency signals as well as dc signals. If the input is a low-frequency signal, it gets chopped into the ac waveform of Figure-20b. This chopped signal can be amplified by an ac amplifier.
- The amplified signal can then be peak-detected to recover the original input signal.

1.11.3 Buffer Amplifier

- Figure-21 shows a buffer amplifier, a stage that isolates the preceding stage from the following stage. Ideally, a buffer should have a high input impedance. If it does, almost all the Thevenin voltage from stage A appears at the buffer input.
- The buffer should also have a low output impedance. This ensures that all its output voltage reaches the input of stage B.

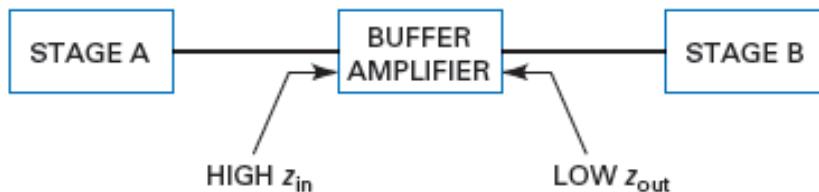


Figure-21 Buffer amplifiers isolates stages A and B

- The source follower is an excellent buffer amplifier because of its high input impedance (well into the mega-ohms at low frequencies) and its low output impedance (typically a few hundred ohms).
- The high input impedance means light loading of stage A. The low output impedance means that the buffer can drive heavy loads (small load resistances).

1.11.4 Low-Noise Amplifier

- Noise is any unwanted disturbance superimposed on a useful signal. Noise interferes with the information contained in the signal. For instance, the noise in television receivers produces small white or black spots on the picture.
- Severe noise can wipe out the picture altogether. Similarly, the noise in radio receivers produces crackling and hissing, which sometimes completely masks the signal.
- Noise is independent of the signal because it exists even when the signal is off. The JFET is an outstanding low-noise device because it produces much less noise than a bipolar junction transistor.
- Low noise is very important at the front end of receivers because the later stages amplify front-end noise along with the signal. If we use a JFET amplifier at the front end, we get less amplified noise at the final output.
- Other circuits near the front end of receivers include frequency mixers and oscillators. A frequency mixer is a circuit that converts a higher frequency to a lower one. An oscillator is a circuit that generates an ac signal.
- JFETs are often used for VHF/UHF amplifiers, mixers, and oscillators. VHF stands for “very high

- “frequencies” (30 to 300 MHz), and UHF, for “ultra high frequencies” (300 to 3000 MHz).

1.11.5 Voltage-Controlled Resistance

- When a JFET operates in the ohmic region, it usually has $V_{GS} = 0$ to ensure hard saturation. But there is an exception. It is possible to operate a JFET in the ohmic region with V_{GS} values between 0 and $V_{GS(off)}$. In this case, the JFET can act like a voltage-controlled resistance.
- Figure-22 shows the drain curves of a 2N5951 near the origin with V_{DS} less than 100 mV. In this region, the small-signal resistance r_{ds} is defined as the drain voltage divided by the drain current:

$$r_{ds} = \frac{V_{DS}}{I_D} \quad \text{--- (24)}$$

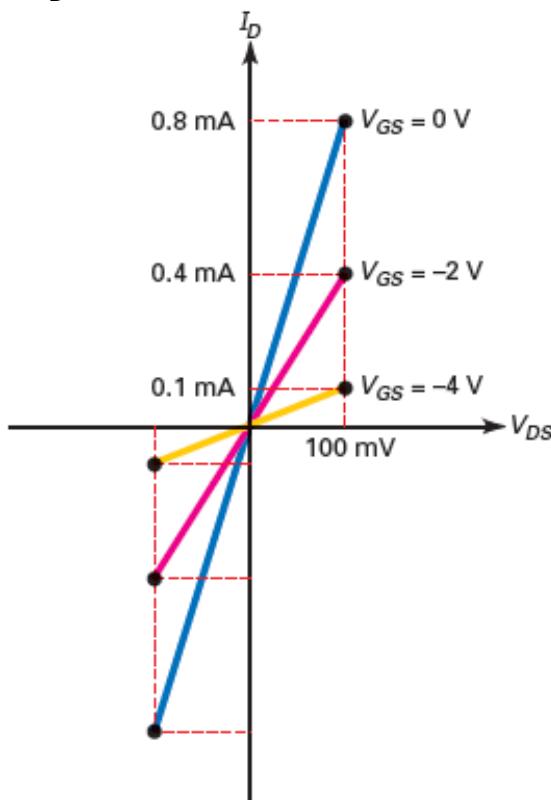


Figure-22 Small-signal r_{ds} is voltage controlled

- Recall that a JFET is a symmetrical device at low frequencies since either end can act like the source or the drain. This is why the drain curves of Figure-22 extend on both sides of the origin.
- This means that a JFET can be used as a voltage-controlled resistance for small ac signals, typically those with a peak-to-peak value of less than 200 mV. When it is used in this way, the JFET does not need a dc drain voltage from the supply because the small ac signal supplies the drain voltage.

1.11.6 Automatic Gain Control

- When a receiver is tuned from a weak to a strong station, the loudspeaker will blare (become loud) unless the volume is immediately decreased. The volume may also change because of fading, a decrease in signal caused by a change in the path between the transmitter and receiver.
- To prevent unwanted changes in the volume, most modern receivers use automatic gain control (AGC). Figure-23 illustrates the basic idea of AGC.

- An input signal V_{in} passes through a JFET used as a voltage-controlled resistance. The signal is amplified to get the output voltage V_{out} . The output signal is fed back to a negative peak detector.
- The output of this peak detector then supplies the V_{GS} for the JFET. If the input signal suddenly increases by a large amount, the output voltage will increase.
- This means that a larger negative voltage comes out of the peak detector. Since V_{GS} is more negative, the JFET has a higher ohmic resistance, which reduces the signal to the amplifier and decreases the output signal.
- On the other hand, if the input signal fades, the output voltage decreases and the negative peak detector produces a smaller output. Since V_{GS} is less negative, the JFET transmits more signal voltage to the amplifier, which raises the final output.
- Therefore, the effect of any sudden change in the input signal is offset or at least reduced by the AGC action.

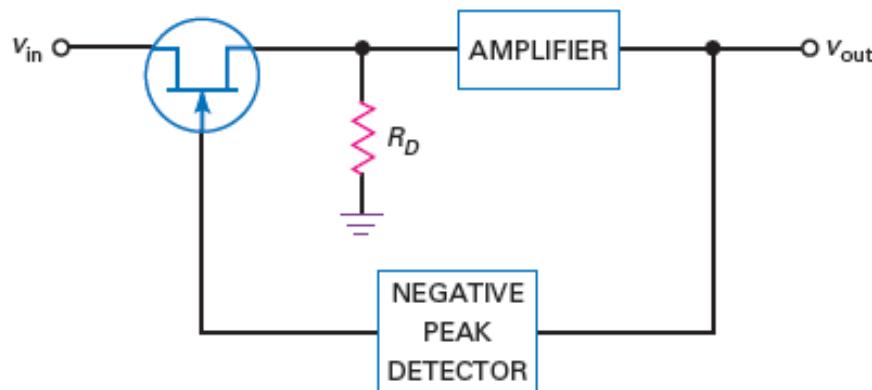


Figure-23 Automatic gain control

1.11.7 Cascode Amplifier

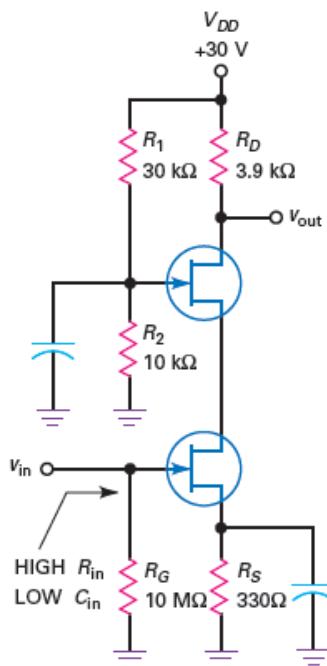


Figure-24 Cascode amplifier

- Figure-24 is an example of a cascode amplifier. It can be shown that the overall voltage gain of this two-FET connection is:
$$A_v = g_m r_d$$
- This is the same voltage gain as for a CS amplifier. The advantage of the circuit is its low input capacitance, which is important with VHF and UHF signals. At these higher frequencies, the input capacitance becomes a limiting factor on the voltage gain.
- With a cascode amplifier, the low input capacitance allows the circuit to amplify higher frequencies than are possible with only a CS amplifier.

1.11.8 Current Sourcing

- Suppose you have a load that requires a constant current. One solution is to use a shorted-gate JFET to supply the constant current. Figure-25a shows the basic idea. If the Q point is in the active region, as shown in Figure-25b, the load current equals I_{DSS} . If the load can tolerate the change in I_{DSS} when JFETs are replaced, the circuit is an excellent solution.

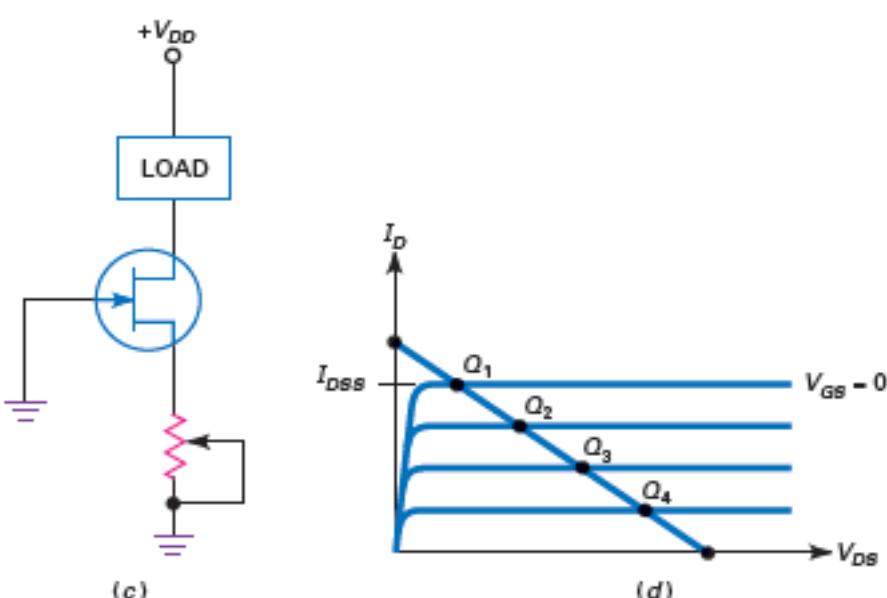
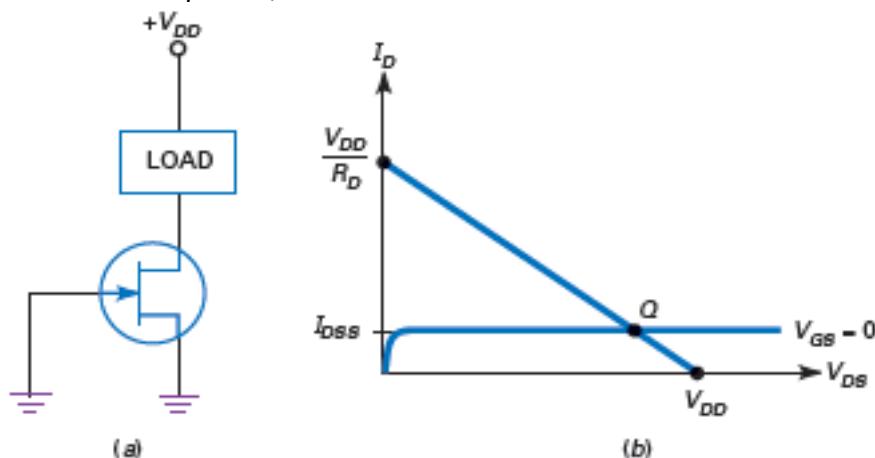


Figure-25 JFET used as current source

- On the other hand, if the constant load current must have a specific value, we can use an adjustable source resistor, as shown in Figure-25c. The self-bias will produce negative values of V_{GS} . By adjusting the resistor, we can set up different Q points, as shown in Figure-25d.
- Using JFETs like this is a simple way to produce a fixed load current, one that is constant even though the load resistance changes. In later chapters, we will discuss other ways to produce fixed load currents using op amps.

1.11.9 Current Limiting

- Instead of sourcing current, a JFET can limit current. Figure-26a shows how. In this application, the JFET operates in the ohmic region rather than the active region. To ensure operation in the ohmic region, the designer selects values to get the dc load line of Figure-26b.

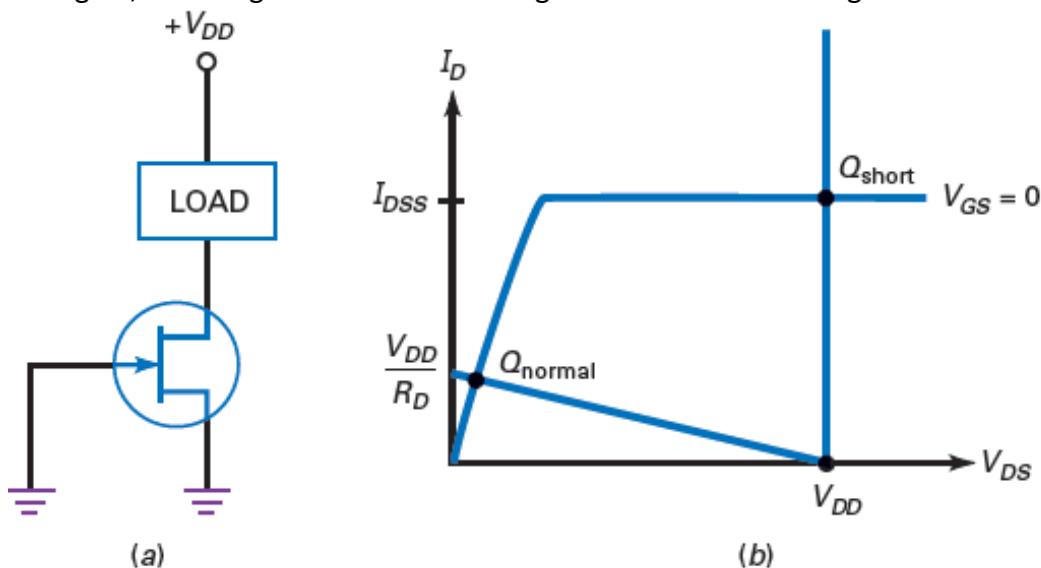


Figure-26 JFET limits current if load shorts

- The normal Q point is in the ohmic region, and the normal load current is approximately V_{DD}/R_D .
- If the load becomes shorted, the dc load line becomes vertical. In this case, the Q point changes to the new position shown in Figure-26b. With this Q point, the current is limited to I_{DSS} . The point to remember is that a shorted load usually produces an excessive current.
- But with the JFET in series with the load, the current is limited to a safe value.

1.12 MOSFETs

- The metal-oxide semiconductor FET, or MOSFET, has a source, gate, and drain. The MOSFET differs from the JFET, however, in that the gate is insulated from the channel. Because of this, the gate current is even smaller than it is in a JFET.
- There are two kinds of MOSFETs, the depletion-mode type and the enhancement-mode type. The enhancement-mode MOSFET is widely used in both discrete and integrated circuits.
- In discrete circuits, the main use is in power switching, which means turning large currents on and off. In integrated circuits, the main use is in digital switching, the basic process behind modern computers. Although their use has declined, depletion mode MOSFETs are still found in high-frequency front-end communications circuits as RF amplifiers.

1.13 The Depletion-Mode MOSFET

- Figure-27 shows a depletion-mode MOSFET, a piece of n material with an insulated gate on the left and a p region on the right. The p region is called the substrate.

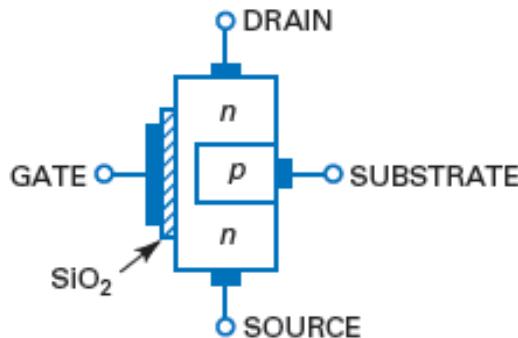


Figure-27 Depletion-mode MOSFET

- Electrons flowing from source to drain must pass through the narrow channel between the gate and the p substrate. A thin layer of silicon dioxide (SiO_2) is deposited on the left side of the channel.
- Silicon dioxide is the same as glass, which is an insulator. In a MOSFET, the gate is metallic. Because the metallic gate is insulated from the channel, negligible gate current flows even when the gate voltage is positive.
- Figure-28a shows a depletion-mode MOSFET with a negative gate voltage. The V_{DD} supply forces free electrons to flow from source to drain. These electrons flow through the narrow channel on the left of the p substrate.
- As with a JFET, the gate voltage controls the width of the channel. The more negative the gate voltage, the smaller the drain current. When the gate voltage is negative enough, the drain current is cut off. Therefore, the operation of a depletion-mode
- MOSFET is similar to that of a JFET when V_{GS} is negative. Since the gate is insulated, we can also use a positive input voltage, as shown in Figure-28b.
- The positive gate voltage increases the number of free electrons flowing through the channel. The more positive the gate voltage, the greater the conduction from source to drain.

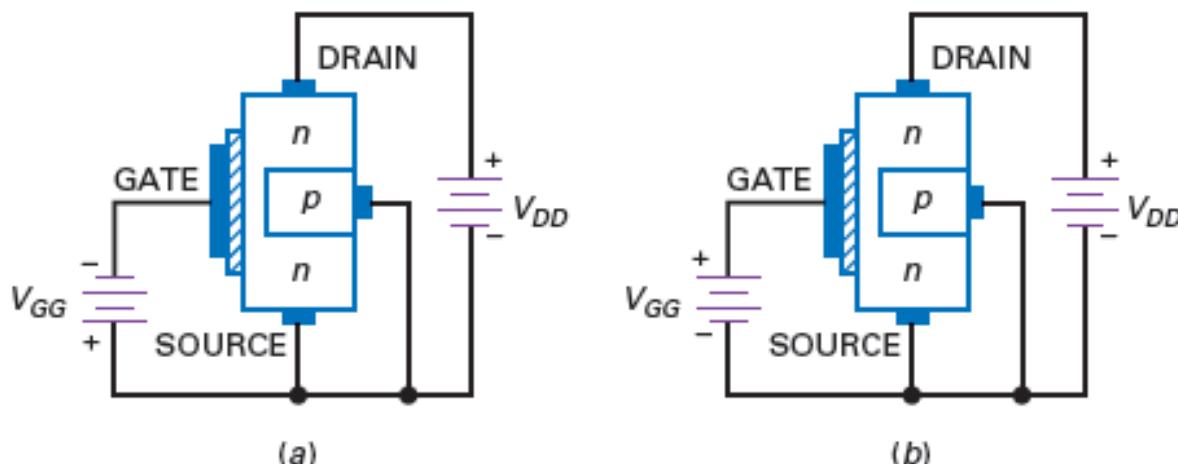


Figure-28 (a) D-MOSFET with negative gate; (b) D-MOSFET with positive gate

- There is also a p-channel D-MOSFET. It consists of a drain-to-source p-channel, along with an n-type substrate. Once again, the gate is insulated from the channel.
- The action of a p-channel MOSFET is complementary to the n-channel MOSFET. The schematic symbols for both n-channel and p-channel D-MOSFETs are shown in Figure-29.

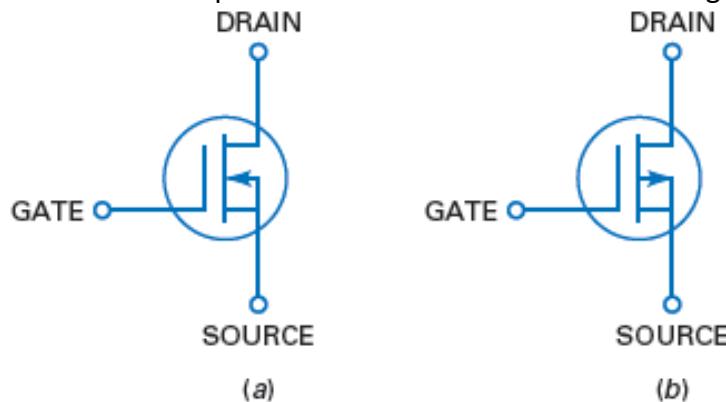


Figure-29 D-MOSFET schematic symbols: (a) n-channel; (b) p-channel

1.14 The Enhancement-Mode MOSFET

- The depletion-mode MOSFET was part of the evolution toward the enhancement mode MOSFET, abbreviated E-MOSFET. Without the E-MOSFET, the personal computers that are now so widespread would not exist.

1.14.1 The Basic Idea

- Figure-30a shows an E-MOSFET. The p substrate now extends all the way to the silicon dioxide. As you can see, there no longer is an n channel between the source and the drain. How does an E-MOSFET work? Figure-30b shows normal biasing polarities.

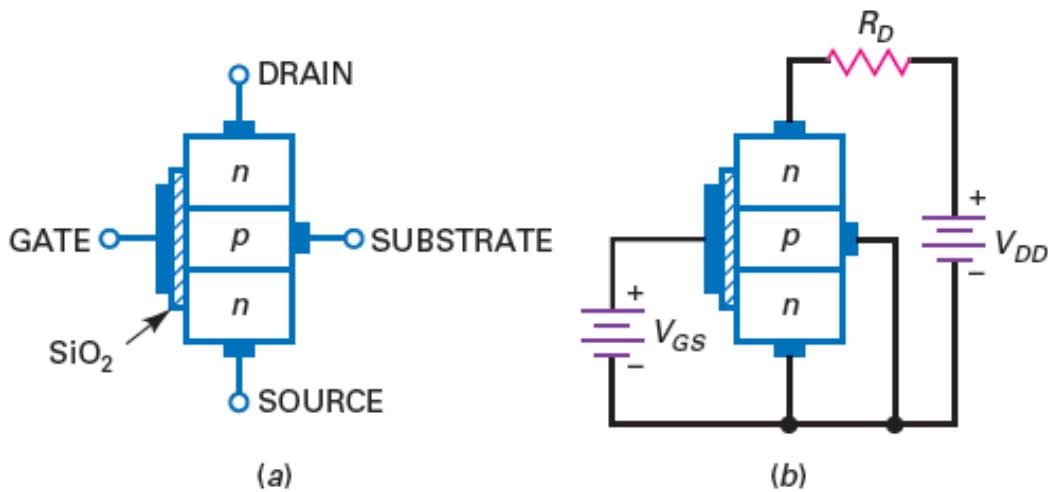


Figure-30 Enhancement-mode MOSFET: (a) Unbiased; (b) biased

- When the gate voltage is zero, the current between source and drain is zero. For this reason, an E-MOSFET is normally off when the gate voltage is zero.
- The only way to get current is with a positive gate voltage. When the gate is positive, it attracts free electrons into the p region.

- The free electrons recombine with the holes next to the silicon dioxide. When the gate voltage is positive enough, all the holes touching the silicon dioxide are filled, and free electrons begin to flow from the source to the drain.
- The effect is the same as creating a thin layer of n-type material next to the silicon dioxide. This thin conducting layer is called the n-type inversion layer. When it exists, free electrons can flow easily from the source to the drain.
- The minimum V_{GS} that creates the n-type inversion layer is called the threshold voltage, symbolized by $V_{GS(th)}$. When V_{GS} is less than $V_{GS(th)}$, the drain current is zero.
- When V_{GS} is greater than $V_{GS(th)}$, an n-type inversion layer connects the source to the drain and the drain current can flow. Typical values of $V_{GS(th)}$ for small-signal devices are from 1 to 3 V.
- The JFET is referred to as a depletion-mode device because its conductivity depends on the action of depletion layers. The E-MOSFET is classified as an enhancement-mode device because a gate voltage greater than the threshold voltage enhances its conductivity.
- ***With zero gate voltage, a JFET is on, whereas an E-MOSFET is off. Therefore, the E-MOSFET is considered to be a normally off device.***

1.14.2 Schematic Symbol

- When $V_{GS} = 0$, the E-MOSFET is off because there is no conducting channel between source and drain. The schematic symbol of Figure-31a has a broken channel line to indicate this normally off condition.
- As you know, a gate voltage greater than the threshold voltage creates an n-type inversion layer that connects the source to the drain.
- The arrow points to this inversion layer, which acts like an n channel when the device is conducting.
- There is also a p-channel E-MOSFET. The schematic symbol is similar, except that the arrow points outward, as shown in Figure-31b.
- The p-channel E-MOSFET is also a normally off enhancement-mode device. To turn on a p-channel E-MOSFET, the gate must be made negative with respect to the source.
- The $-V_{GS}$ value must reach or exceed the $-V_{GS(th)}$ value for conduction. When this occurs, a p-type inversion layer is formed with holes being the majority carriers.
- The n-channel E-MOSFET uses electrons as the majority carriers which have higher mobility than the p-channel holes. This results in a lower $R_{DS(on)}$ and higher switching speeds for the n-channel E-MOSFET.

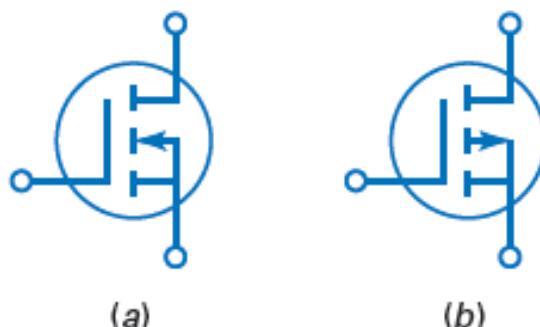


Figure-31 EMOS schematic symbols: (a) N-channel device; (b) p-channel device

1.15 CMOS

- With active-load switching, the current drain with a low output is approximately equal to $I_{D(sat)}$. This may create a problem with battery-operated equipment.
- One way to reduce the current drain of a digital circuit is with complementary MOS (CMOS). In this approach, the IC designer combines n-channel and p-channel MOSFETs.
- Figure-32a shows the idea. Q_1 is a p-channel MOSFET and Q_2 is an n-channel MOSFET. These two devices are complementary; that is, they have equal and opposite values of $V_{GS(th)}$, $V_{GS(on)}$, $I_{D(on)}$, and so on.
- The circuit is similar to a Class-B amplifier because one MOSFET conducts while the other is off.

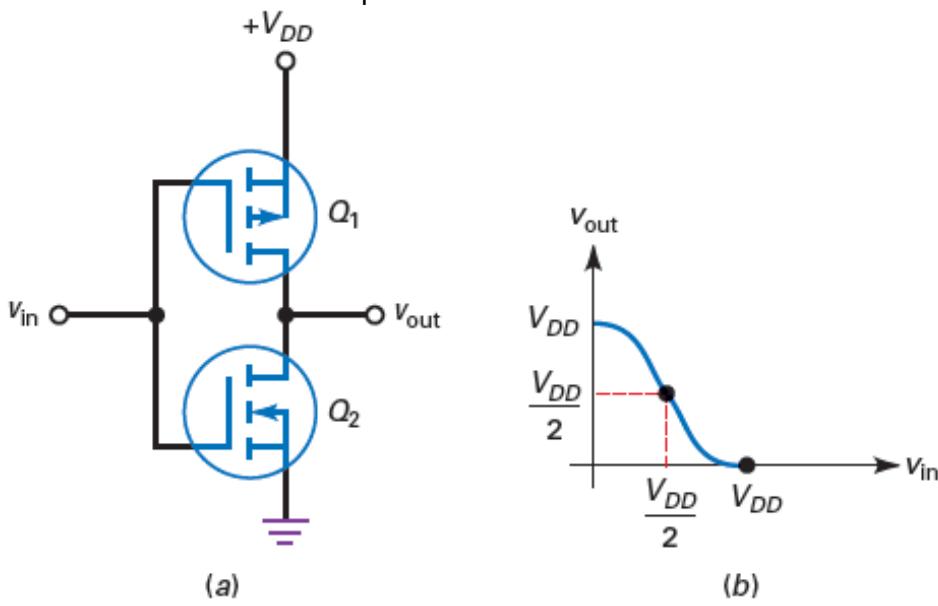


Figure-32 CMOS inverter: (a) Circuit; (b) input-output graph

1.15.1 Basic Action

- When a CMOS circuit like Figure-32a is used in a switching application, the input voltage is either high ($+V_{DD}$) or low (0 V). When the input voltage is high, Q_1 is off and Q_2 is on. In this case, the shorted Q_2 pulls the output voltage down to ground.
- On the other hand, when the input voltage is low, Q_1 is on and Q_2 is off. Now, the shorted Q_1 pulls the output voltage up to $+V_{DD}$. Since the output voltage is inverted, the circuit is called a CMOS inverter.
- Figure-32b shows how the output voltage varies with the input voltage. When the input voltage is zero, the output voltage is high. When the input voltage is high, the output voltage is low.
- Between the two extremes, there is crossover point where the input voltage equals $V_{DD}/2$. At this point, both MOSFETs have equal resistances and the output voltage equals $V_{DD}/2$.

1.15.2 Power Consumption

- The main advantage of CMOS is its extremely low-power consumption. Because both MOSFETs are in series in Figure-32a, the quiescent current drain is determined by the non-conducting device.

- Since its resistance is in the mega-ohms, the quiescent (idling) power consumption approaches zero. The power consumption increases when the input signal switches from low to high, and vice versa.
- The reason is this: At the midway point in a transition from low to high or vice versa, both MOSFETs are on. This means that the drain current temporarily increases.
- Since the transition is very rapid, only a brief pulse of current occurs. The product of the drain supply voltage and the brief pulse of current means that the average dynamic power consumption is greater than the quiescent power consumption.
- In other words, a CMOS device dissipates more average power when it has transitions than when it is quiescent. Since the pulses of current are very short, however, the average power dissipation is very low even when CMOS devices are switching states.
- In fact, the average power consumption is so small that CMOS circuits are often used for battery-powered applications such as calculators, digital watches, and hearing aids.

1.16 E-MOSFET Amplifiers

- As mentioned in previous sections, the E-MOSFET finds its use primarily as a switch. Applications do exist for this device to be used as an amplifier, however.
- These applications include front-end high-frequency RF amplifiers used in communications equipment and power E-MOSFETs used in Class-AB power amplifiers.
- With E-MOSFETs, V_{GS} has to be greater than $V_{GS(th)}$ for drain current to flow. This eliminates self-bias, current-source bias, and zero bias because all these will have depletion-mode operation.
- This leaves gate bias and voltage-divider bias. Both of these biasing arrangements will work with E-MOSFETs because they can achieve enhancement-mode operation.
- Figure-33 shows the drain curves and the transconductance curve for an n-channel E-MOSFET. The parabolic transfer curve is similar to that of D-MOSFET with some important differences.

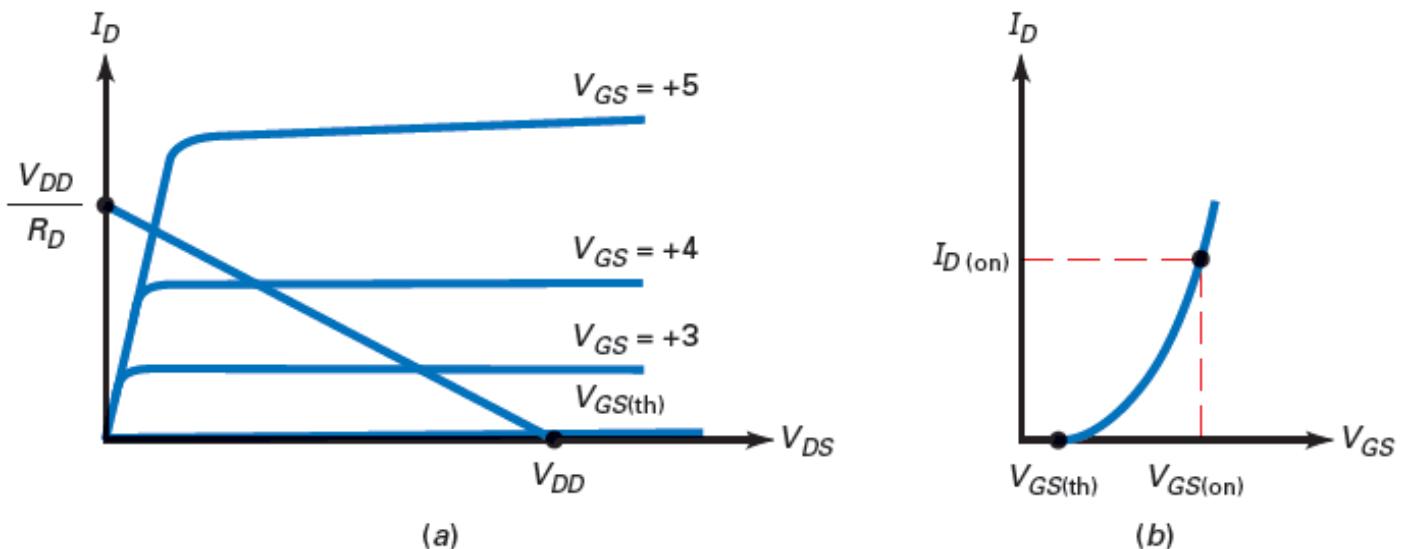


Figure-33 An n-channel E-MOSFET: (a) Drain curves; (b) transconductance curve

- The E-MOSFET operates only in the enhancement mode. Also, the drain current doesn't start until $V_{GS} = V_{GS(th)}$.

- Again, this demonstrates that the E-MOSFET is a voltage-controlled normally off device. Because the drain current is zero when $V_{GS} = 0$, the standard transconductance formula will not work with the E-MOSFET.
- The drain current can be found by:

$$I_D = k [V_{GS} - V_{GS(th)}]^2 \quad \dots \dots \dots (25)$$

Where k is a constant value for the E-MOSFET found by:

$$k = \frac{I_{D(on)}}{[V_{GS(on)} - V_{GS(th)}]^2} \quad \dots \dots \dots (26)$$

- Figure-34a shows another biasing method for E-MOSFETs called drain-feedback bias. This biasing method is similar to collector-feedback bias used with bipolar junction transistors.
- When the MOSFET is conducting, it has a drain current of $I_{D(on)}$ and a drain voltage of $V_{DS(on)}$. Because there is virtually no gate current, $V_{GS} = V_{DS(on)}$. As with collector-feedback, drain-feedback bias tends to compensate for changes in FET characteristics.
- For example, if $I_{D(on)}$ tries to increase for some reason, $V_{DS(on)}$ decreases. This reduces V_{GS} and partially offsets the original increase in $I_{D(on)}$.
- Figure-34b shows the Q point on the transconductance curve. The Q point has the coordinates of $I_{D(on)}$ and $V_{DS(on)}$. Data sheets for E-MOSFETs often give a value of $I_{D(on)}$ for $V_{GS} = V_{DS(on)}$.

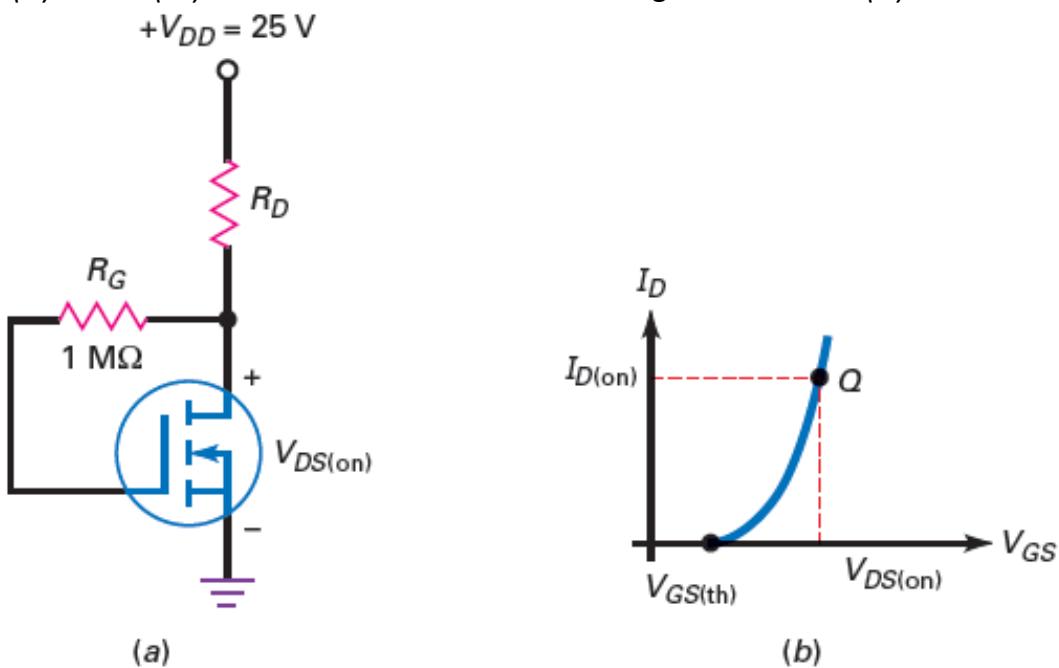


Figure-34 Drain-feedback bias: (a) Biasing method; (b) Q point

- When designing this circuit, select a value of R_D that produces the specified value of V_{DS} . This can be found by:

$$R_D = \frac{V_{DD} - V_{DS(on)}}{I_{D(on)}} \quad \dots \dots \dots (27)$$

- The transconductance value will vary, depending on the circuit's Q point, following the relationship of $I_D = k [V_{GS} - V_{GS(th)}]^2$ and $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ $\dots \dots \dots (28)$

1.17 MOSFET Testing

- MOSFET devices require special care when being tested for proper operation. As stated previously, the thin layer of silicon dioxide between the gate and channel can be easily destroyed when V_{GS} exceeds $V_{GS(max)}$.
- Because of the insulated gate, along with the channel construction, testing MOSFET devices with an ohmmeter or DMM is not very effective. A good way to test these devices is with a semiconductor curve tracer.
- If a curve tracer is not available, special test circuits can be constructed. Figure-35 shows a circuit capable of testing both depletion-mode and enhancement-mode MOSFETs. By changing the voltage level and polarity of V_1 , the device can be tested in either depletion or enhancement modes of operation.

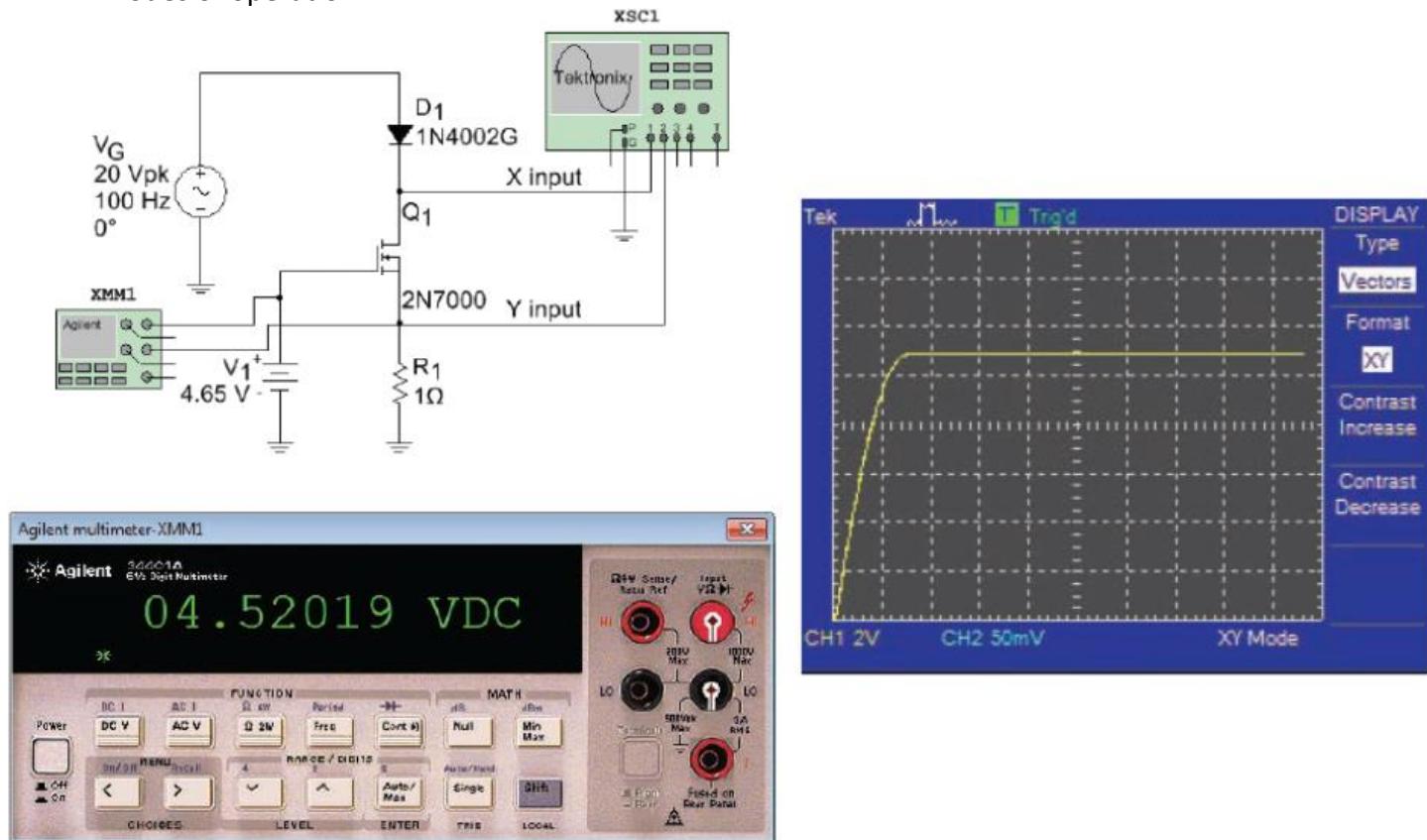


Figure-35 MOSFET testing

- The drain curve shown in Figure-35 shows the approximate drain current of 275 mA when, $V_{GS} = 4.52$ V. The y-axis is set to display 50 mA/div.
- An alternative to the aforementioned testing methods is to simply use component substitution. By measuring in-circuit voltage values, it is often possible to deduct that the MOSFET is defective. Replacing the device with a known good component should lead you to a final conclusion.

1.18 Question Bank

- 1) Compare BJT and FET. (MIMP)
- 2) With the help of diagram explain drain curves.
- 3) What is transconductance? Explain transconductance curve for JFET.
- 4) Describe and derive all necessary equations for voltage divider bias for JFET.
- 5) Explain Common-Source (CS) configuration for JFET amplifier with required derivations and advantages. (MIMP)
- 6) Explain JFET as analog switch.
- 7) Explain in brief applications of JFET.
- 8) Explain with neat sketch D-type and E-type MOSFET. (MIMP)
- 9) Explain working of CMOS with suitable diagrams.
- 10) Describe E-MOSFET as amplifier.

1.1 Introduction to Analog and Digital signals

Electronic systems usually deal with information. Representation of information is called a **signal**. Signal in electronics is generally in form of voltage or current. Value of a signal is proportional to some physical quantity and it gives information about it. For example, temperature represented in terms of voltage signal.

There are two types of signals which are different in terms of their characteristics with respect to time and value.

1. Analog Signals
2. Digital Signals

A signal whose value is defined at all instances of time is called continuous time signal. On the other hand signal whose values are defined only at discrete instances of time is called discrete time signal. Most of the signals that occur in nature are analog in form. A discrete time signal can be obtained from continuous time signal by process called sampling. This has been illustrated in Fig. 1.1.

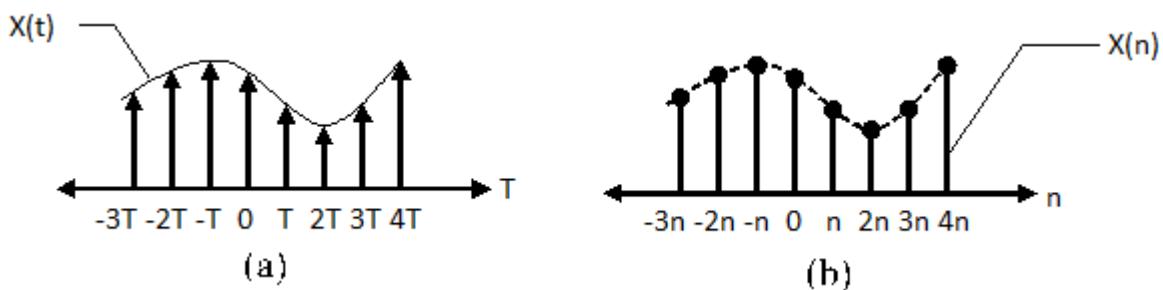


Fig. 1.1: (a) Continuous time signal $x(t)$ sampled at every T interval, (b) Resulting discrete time signal $x(n)$

Similarly if a signal can take any value in a given range between some minimum and maximum value then the signal is called continuous value signal. On the other hand if a signal takes only certain fixed values in a given range then it is called discrete value signal. The process of converting a continuous value signal to a discrete value signal is called quantization. This is illustrated in Fig. 1.2.

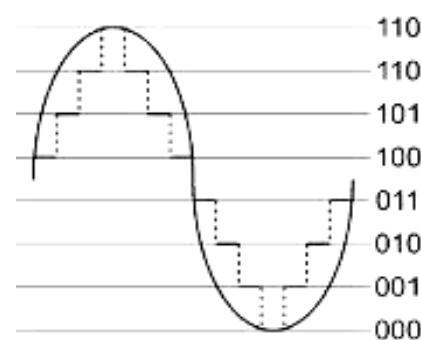


Fig. 1.2: Continuous value signal (solid line) and discrete value signal (dotted line)

Analog signal: Signals that are continuous in time and continuous in value are called analog signal.

Digital signal: Signals that are discrete in time and discrete in values are called digital signals. Digital signals are generally processed by digital systems like computers and hence their values are represented in terms of binary as shown in Fig. 1.2.

Analog signal being continuous in time will have infinite values in any given period of time. Practically a digital system like computer cannot handle infinite values due to limited physical resources and processing power. This is the reason why a continuous time signal has to be sampled and converted to discrete time signal.

Again analog signals are continuous in value and hence can take any value in a given range. Now ideally number of values in any given range will be infinite which cannot be represented by finite number of bits on a computer. For example, as shown in Fig. 1.2, with three bits used for representing values only eight different values can be represented. Thus a continuous value signal has to be quantized and converted to discrete value signal.

1.2 Introduction to Digital System.

A digital system uses a building blocks approach. Many small operational units are interconnected to make up the overall system. The most basic logical unit system is gate circuit. There are several different types of gates with each perform differently from other logic gates.

Digital signal consist of only two values, '0' and '1'. These two values have logical meaning i.e. '1' represents the existence of particular condition and '0' represents the absence of condition.

There are two types of tables used in digital system:

(i) Truth Table:

Truth table plots inputs and outputs in terms of 1s and 0s.

(ii) Function Table:

Function table plots inputs and outputs in term of HIGH and LOW voltage levels.

The design of digital system may be roughly divided into three stages;

(i) System Design:

It involves breaking the overall system into subsystem and specifying the characteristics of each subsystem. For example, the system design of a digital computers involves specifying the number and type of memory, ALU and i/p – o/p devices.

(ii) Logic Design:

It involves how to interconnect basic logic building blocks to perform specific function. For example, to make a flip flop different logic gates need to be connected in specific manner.

(iii) Circuit Design:

It involves specifying the interconnection of specific components like resistors, transistors, diodes, CMOS etc. to create a logic gates.

1.3 Comparison between Analog and Digital Systems

	Analog Systems	Digital Systems
1	Analog systems operate on continuous time and continuous value signals.	Digital systems operate on discrete time and discrete value signals generally represented in binary.
2	Analog systems are difficult to design.	Digital systems are easy to design as most of the components are in form of Integrated circuits (IC).
3	Analog systems are mostly custom made and less flexible.	Digital systems have high degree of flexibility.
4	Less efficient in storage of information.	More efficient in storage of information.
5	Analog signal processed by these systems are affected by noise very easily.	Digital signal are less affected by noise compared to analog signals.
6	Relatively costly compared to digital system	Low cost due to mass production of components.
7	Analog systems are more sensitive to parameter variation.	Digital systems are less sensitive to parameter variation
8	No conversion of input signals are required before processing	Input signals are converted from analog to digital form before it is processed
9	As no conversion of input signal is required, there is no loss of information.	Due to process of sampling and quantization, there is loss of information.
10	Analog systems are more efficient for real time processing	Digital systems may offer limitations for real time processing
11	Probability of error is more in Analog system	Probability of error is less in Analog system

1.4 Advantages of Digital Systems.

- (i) Digital systems are easier to design
- (ii) Digital systems have high degree of flexibility.
- (iii) Information storage is easy
- (iv) Digital circuits are less affected by noise
- (v) Probability of error is less
- (vi) Low cost and more reliable
- (vii) More digital circuitry can be fabricated on IC chips
- (viii) Digital systems are less sensitive to parameter variation
- (ix) Accuracy and precision are greater
- (x) Digital systems are based on Boolean algebra which is easy.
- (xi) Digital system concerned with only two logic levels.
- (xii) There are very few basic operations in digital and are very easy.

1.5 Logic Levels and Different types of Logics.

Digital system use the binary number system. Therefore, two-state devices are used to represent the two binary digits 1s & 0s by two different voltage levels, called HIGH and LOW. Normally, the binary 0 and 1 are represented by the logic voltage levels 0 V and +5 V.

Usually any voltage between 0 V to 0.8 V represents the logic 0 and any voltage between 2 V to 5 V represents the logic 1. This voltage levels can be varies according to the different logical systems.

There are three types of logics available in digital systems.

1. Positive Logic
2. Negative Logic
3. Mixed Logic

1. Positive Logic:

In positive logic high voltage level represents as logic 1 and low voltage level represents as logic 0.



Fig. 1.3: Illustration of positive logic

2. Negative Logic:

In positive logic high voltage level represent as logic 0 and low voltage level represents as logic 1.



Fig. 1.4: Illustration of negative logic

3. Mixed Logic:

This scheme uses positive logic in some portions (e.g inputs) of the system while applying negative logic (e.g. outputs) in other portion of the system.

Suppose some function $X = AB' + A'B$ for this function the representation of all the logics are as follow;

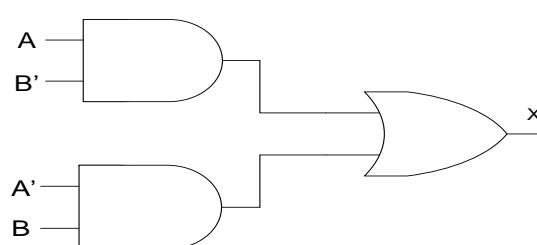


Fig. 1.5: Representation of function $X = AB' + A'B$

Truth table of the given function for all the logics is shown as follow;

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

Positive Logic

A	B	X
1	1	1
1	0	0
0	1	0
0	0	1

Negative Logic

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

Mixed Logic

1.6 Boolean Algebra

Boolean Algebra is the mathematics we use to analyze digital logic gates and circuits. We can use these “Laws of Boolean” to both reduce and simplify a complex Boolean expression in an attempt to reduce the number of logic gates required in digital system design.

Boolean Algebra is therefore a system of mathematics based on logic that has its own set of rules or laws which are used to define and reduce Boolean expressions.

The variables used in **Boolean Algebra** only have one of two possible values, a logic “0” and a logic “1”. *In Boolean algebra, variable do not represent numerical value but it has logical value.* In Boolean algebra an expression given can also be converted into a logic diagram using different logic gates like AND gate, OR gate and NOT gate, NOR gates, NAND gates, XOR gates, XNOR gates etc.

Some basic logical Boolean operations:

OR relations (Logical Addition)

A + A = A	0 + 0 = 0
A + \bar{A} = 1	0 + 1 = 1
A + 1 = 1	1 + 0 = 1
A + 0 = A	1 + 1 = 1

AND relations (Logical Multiplication)

A . A = A	0 . 0 = 0
A . \bar{A} = 0	0 . 1 = 0
A . 1 = A	1 . 0 = 0
A . 0 = 0	1 . 1 = 1

Complement Rule (Inversion)

A + \bar{A} = 1	0 = 1
A . \bar{A} = 0	1 = 0
$\bar{\bar{A}} = A$	

De-Morgan's Theorem:

(i) $\overline{A + B} = \bar{A} \cdot \bar{B}$

A	B	$A + B$	$\overline{A + B}$	\bar{A}	\bar{B}	$\bar{A} \cdot \bar{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Hence, from Truth Table it has been observed that L.H.S. = R.H.S.

(ii) $\overline{A \cdot B} = \bar{A} + \bar{B}$

A	B	$A \cdot B$	$\overline{A \cdot B}$	\bar{A}	\bar{B}	$\bar{A} + \bar{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Hence, from Truth Table it has been observed that L.H.S. = R.H.S

1.7 Logic Gates

Logic gates are the fundamental building blocks of digital systems. They are the physical devices that performs the basic Boolean operations of AND, OR and NOT. Input and outputs of logic gates (that is basically a voltage signal) can occur only in two levels. These two levels are termed as :

Logic 1	Logic 0
High Level	Low Level
True	False
ON	OFF

If in representation of higher of the two voltage levels are symbolized as 1 and lower symbolized as 0 then gate is said to be positive logic gate. However, if higher of the two voltage levels is symbolized as 0 and lower as 1 then it is said to be negative logic gate.

Input output behavior of a gate is generally represented using **truth table**. It is a table that lists output for all possible combinations of inputs.

There are total seven logic gates in which three are **basic logic gates** (AND, OR, NOT) and two are **universal logic gates** (NAND, NOR).

Various basic gates are discussed as follows;

1. NOT Gate:

NOT gate has one input and one output. The output becomes logic 1 when input is at logic 0 and output becomes logic 0 when the input is at logic 1. Thus it inverts or complements the logic available at input and hence called an **inverter or complement**.

It is represented by a bar over the variable “ $\bar{ }$ ” or with a symbol “ \prime ”. Thus, for example, $X = A'$ or $X = \bar{A}$ read as “X is equal to Not A or A bar or A complement”. NOT gate and its truth table are shown in fig. 1.6.

IC 7404 is Hex Inverter, consists of six NOT gates on a single chip.

Boolean Expression	Logic Diagram Symbol	Truth Table						
$X = A'$		<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>A</th><th>X</th></tr> <tr> <td>0</td><td>1</td></tr> <tr> <td>1</td><td>0</td></tr> </table>	A	X	0	1	1	0
A	X							
0	1							
1	0							

Fig. 1.6: Illustration of NOT gate

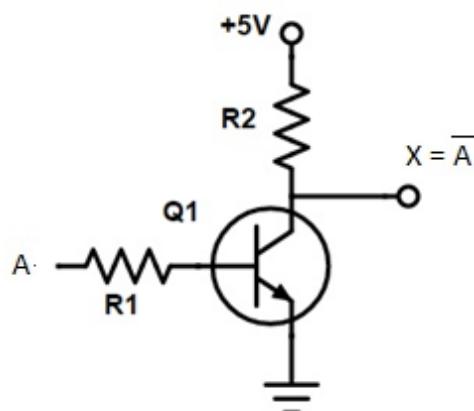


Fig. 1.7: Circuit diagram of NOT gate

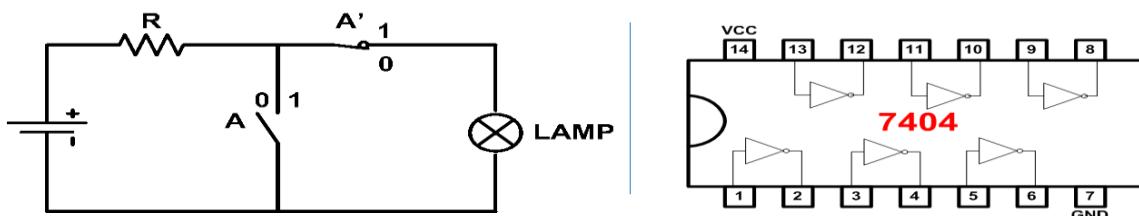


Fig. 1.8: NOT gate switching diagram and IC

2. AND Gate:

AND gate means all or nothing logic. AND gate has two or more inputs and one output. The output becomes logic 1 only when each one of its input is at logic 1. For all other input combinations it gives output logic 0. It is represented by a symbol \bullet . Thus, for example, $X = A$

- B (also written simply as $X = AB$) is read as “X is equal to A AND B”. Two input AND gate and its truth table is shown in fig. 1.9.

Boolean Expression	Logic Diagram Symbol	Truth Table															
$X = A \cdot B$		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A</th><th>B</th><th>X</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	X	0	0	0	0	1	0	1	0	0	1	1	1
A	B	X															
0	0	0															
0	1	0															
1	0	0															
1	1	1															

Fig. 1.9: Illustration of AND gate

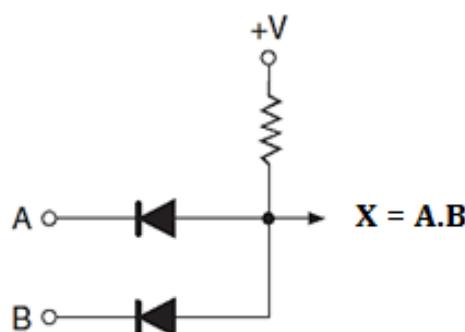
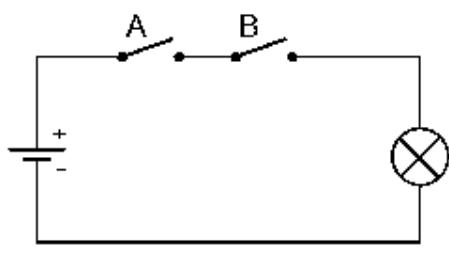


Fig. 1.10: Circuit diagram of AND gate



Switch A - Open = "0", Closed = "1"
 Switch B - Open = "0", Closed = "1"

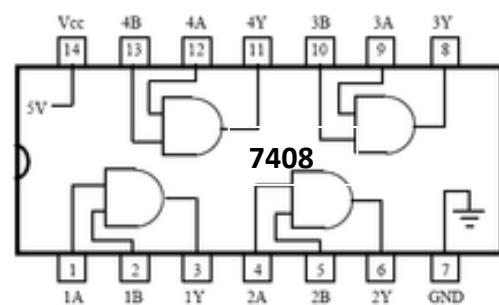


Fig. 1.11: AND gate switching diagram and IC

Working of AND gate circuit using Diode:

When $A=0$ and $B=0$, both the diodes are in forward biased condition. Hence current will flow through resistor and diode. So voltage will drop across resistor and output will be Zero, resulting in output Logic-0

When $A=0$ and $B=1$, or $A=1$ and $B=0$, one of the diodes is in forward biased condition. Which allows the current to pass through resistor and diode. So voltage will drop across resistor again and output will be Zero, resulting in output Logic-0.

When $A=1$ and $B=1$, both the diodes are in Reverse biased condition. Hence current will not flow through resistor and diode. So there is no voltage will drop across resistor and this voltage will be available at output, resulting in output Logic-1.

3. OR Gate:

OR gate means any or all logic. OR gate has two or more inputs and one output. The output becomes logic 1 when at least (minimum) one of the inputs is at logic 1. It is represented by a symbol $+$. Thus, for example, $X = A + B$ is read as "X is equal to A OR B". Two input AND gate and its truth table is shown in fig. 1.12.

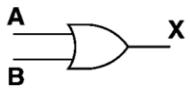
Boolean Expression	Logic Diagram Symbol	Truth Table															
$X = A + B$		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">A</th><th style="text-align: center;">B</th><th style="text-align: center;">X</th></tr> </thead> <tbody> <tr><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td></tr> <tr><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">1</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td></tr> </tbody> </table>	A	B	X	0	0	0	0	1	1	1	0	1	1	1	1
A	B	X															
0	0	0															
0	1	1															
1	0	1															
1	1	1															

Fig. 1.12: Illustration of AND gate

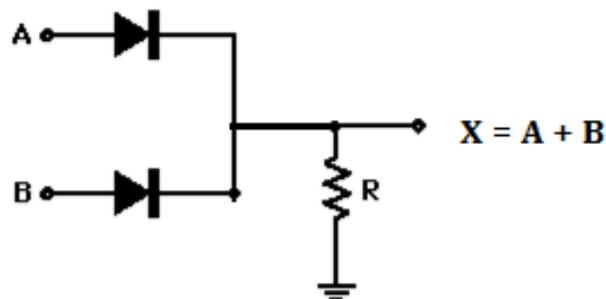


Fig. 1.13: Circuit diagram of OR gate

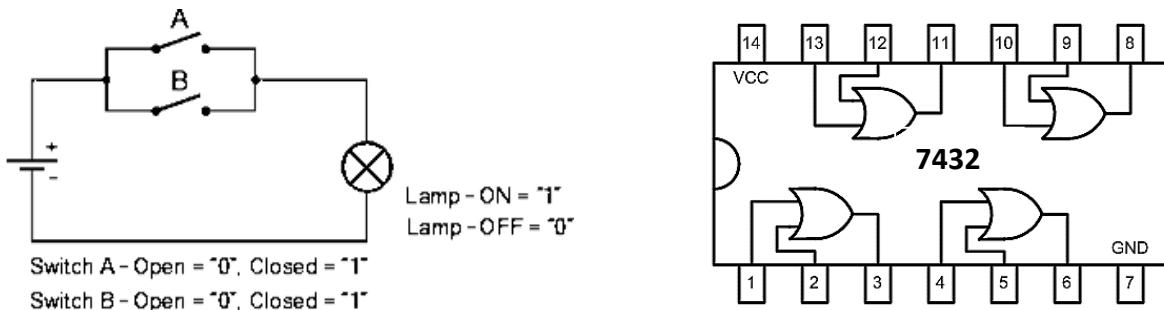


Fig. 1.14: OR gate switching diagram and IC

Working of OR gate circuit using Diode:

When $A=0$ and $B=0$, both the diodes are in reverse biased condition. Hence diode behaves as an OFF switch and current will not flow through diode and resistor. So output will be Zero, (Logic-0).

When $A=0$ and $B=1$, or $A=1$ and $B=0$, one of the diodes is in forward biased condition, which allows the current to pass through diode and resistor. Hence diode behaves as an ON switch. So there will be voltage drop across resistor which will be available as an Output, resulting in output Logic-1.

When $A=1$ and $B=1$, both the diodes are in forward biased condition. which allows the current to pass through diode and resistor. Hence diode behaves as an ON switch. So there will be voltage drop across resistor which will be available as an Output, resulting in output Logic-1.

4. Exclusive OR Gate (EX-OR):

It also means **Inequality detector** because it gives output high when both inputs are different. Exclusive OR gate give output equal to 1 when the two inputs are exclusively different. This is the reason why it is also known as inequality gate. The schematic symbol and truth table of the gate is shown in fig. 1.15. It is represented by a symbol \oplus . Thus, for example, $X = A \oplus B$ is read as "X is equal to A XOR B." The logic expression this gate in terms of AND, OR and NOT operation is $X = A \oplus B = \bar{A}B + A\bar{B}$.

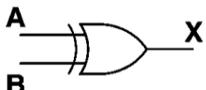
Boolean Expression	Logic Diagram Symbol	Truth Table															
$X = A \oplus B$		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A</th><th>B</th><th>X</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	X	0	0	0	0	1	1	1	0	1	1	1	0
A	B	X															
0	0	0															
0	1	1															
1	0	1															
1	1	0															

Fig. 1.15: Illustration of EX-OR gate

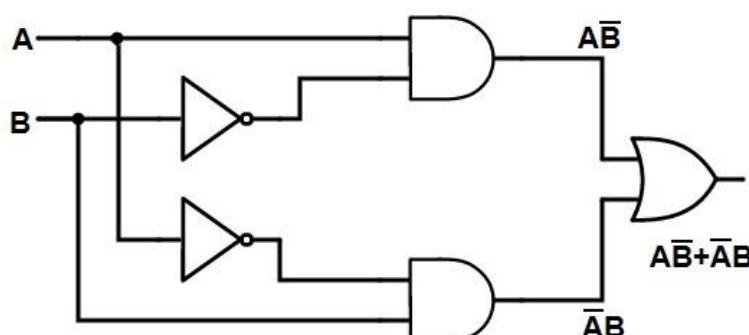


Fig. 1.16: Logic Circuit diagram of EX-OR gate

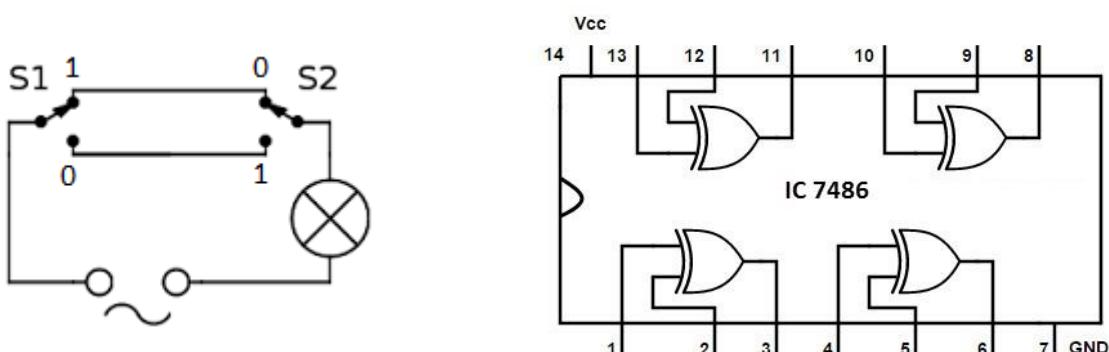


Fig. 1.17: EX-OR gate switching diagram and IC

5. Exclusive NOR Gate (EX-NOR):

It also means **equality detector** because it gives output high when both inputs are same. Exclusive NOR gate is XOR gate followed by inverter. Thus it is complement of XOR gate. This is the reason why it is also known as equality gate.

The schematic symbol and truth table of the gate is shown in fig. 1.18. It is represented by a symbol \odot . Thus, for example, $X = A \odot B$ is read as "X is equal to A XNOR B."

The logic expression this gate in terms of AND, OR and NOT operation is

$$X = A \odot B = AB + \bar{A}\bar{B}$$

or

$$X = AB + A'B'$$

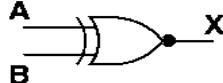
Boolean Expression	Logic Diagram Symbol	Truth Table															
$X = A \odot B$		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">A</th><th style="text-align: center;">B</th><th style="text-align: center;">X</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">1</td></tr> <tr> <td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td></tr> <tr> <td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td></tr> <tr> <td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td></tr> </tbody> </table>	A	B	X	0	0	1	0	1	0	1	0	0	1	1	1
A	B	X															
0	0	1															
0	1	0															
1	0	0															
1	1	1															

Fig. 1.18: Illustration of EX-NOR gate

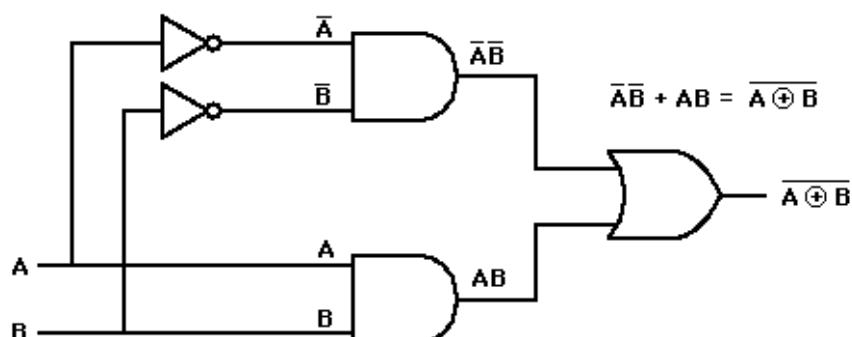


Fig. 1.19: Logic Circuit diagram of EX-NOR gate

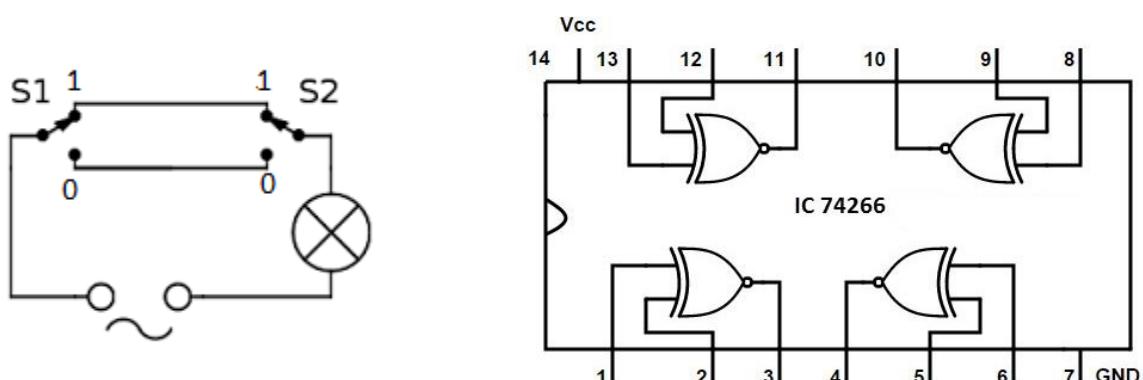


Fig. 1.20: EX-NOR gate switching diagram and IC

Universal Gates:

NAND and NOR gates are known as a universal gates because from these two gates all other gates can be constructed.

6. NAND Gate:

NAND gate represents combination of AND gate followed by NOT gate. It represents complement of AND operation. Schematic symbol of NAND gate and its truth table are shown in fig. 1.15. The logic expression is given as $X = \overline{(A \cdot B)}$ or $X = (A \cdot B)'$.

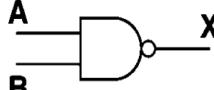
Boolean Expression	Logic Diagram Symbol	Truth Table															
$X = (A + B)'$		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A</th><th>B</th><th>X</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	X	0	0	1	0	1	1	1	0	1	1	1	0
A	B	X															
0	0	1															
0	1	1															
1	0	1															
1	1	0															

Fig. 1.21: Illustration of NAND gate

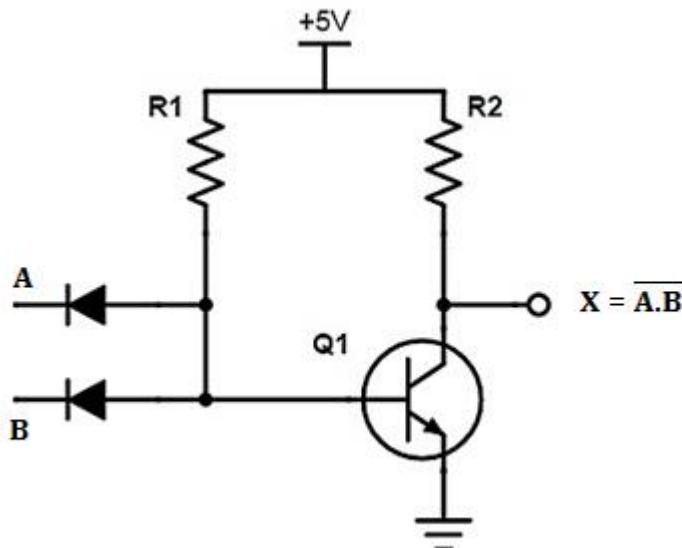


Fig. 1.22: Logic Circuit diagram of NAND gate

Working of NAND gate circuit:

When either $A=0$ or $B=0$, diode will be in forward biased condition. Hence diode behaves as an ON switch and current will flow through diode and Resistor R1. Which results in voltage drop across Resistor R1. So Base current to Transistor is zero and Output of Transistor will be Logic 1.

When $A=1$ and $B=1$, both the diodes are in reverse biased condition. Which do not allow the current to pass through diode and Resistor R1. Hence diode behaves as an OFF switch. So

there will be no voltage drop across resistor. Hence Base current is maximum (Logic-1), making Transistor ON switch and output of Transistor will be Logic-0.

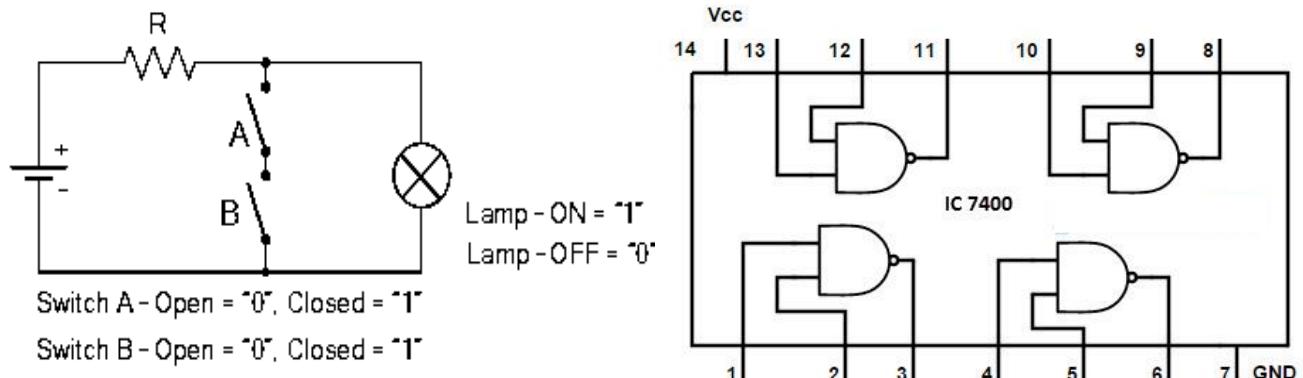
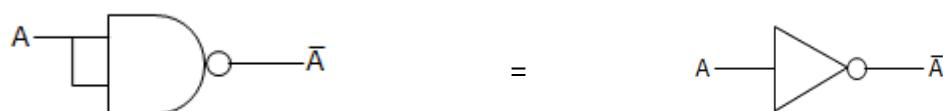


Fig. 1.23: NAND gate switching diagram and IC

NAND gate as Universal gate

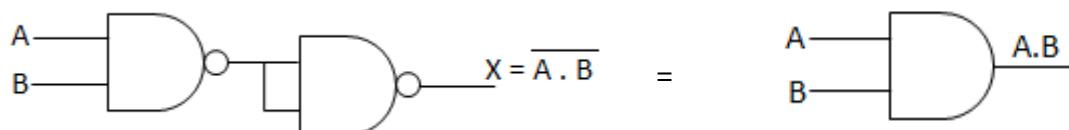
i. Implementing NOT gate

All NAND input pins connect to the input signal A gives an output A' .



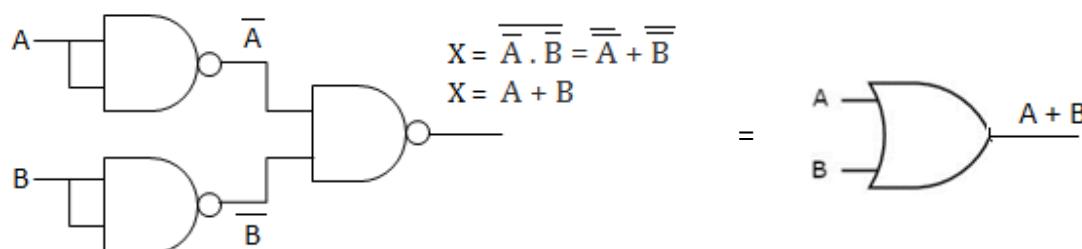
ii. Implementing AND gate

The AND is replaced by a NAND gate with its output complemented by a NAND gate inverter.



iii. Implementing OR gate

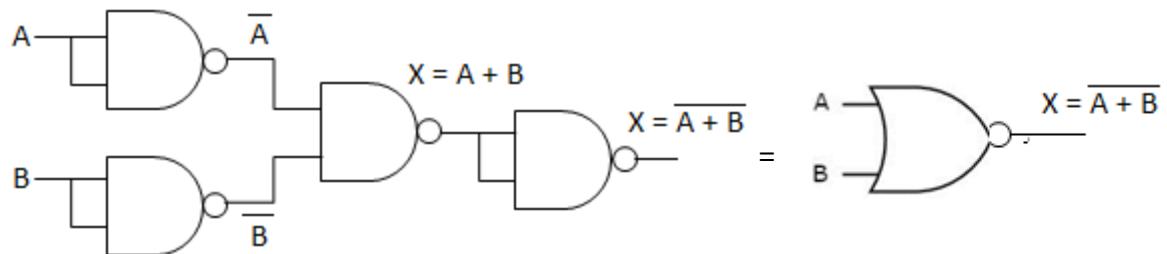
The OR gate is replaced by a NAND gate with all its inputs complemented by NAND gate inverters.



As per De-Morgan's Theorem $\overline{A \cdot B} = \overline{A} + \overline{B}$

For above diagram output $X = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$ (which equivalent to OR gate)

iv. Implementing NOR gate



7. NOR Gate:

NOR gate represents combination of OR gate followed by NOT gate. It represents complement of OR operation. Schematic symbol of NOR gate and its truth table are shown in fig. 4.16. The logic expression is given as $X = (A + B)'$ or $X = (A+B)'$.

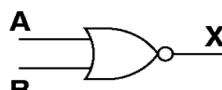
Boolean Expression	Logic Diagram Symbol	Truth Table															
$X = (A + B)'$		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A</th><th>B</th><th>X</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>0</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	X	0	0	1	0	1	0	1	0	0	1	1	0
A	B	X															
0	0	1															
0	1	0															
1	0	0															
1	1	0															

Fig. 1.24: Illustration of NOR gate

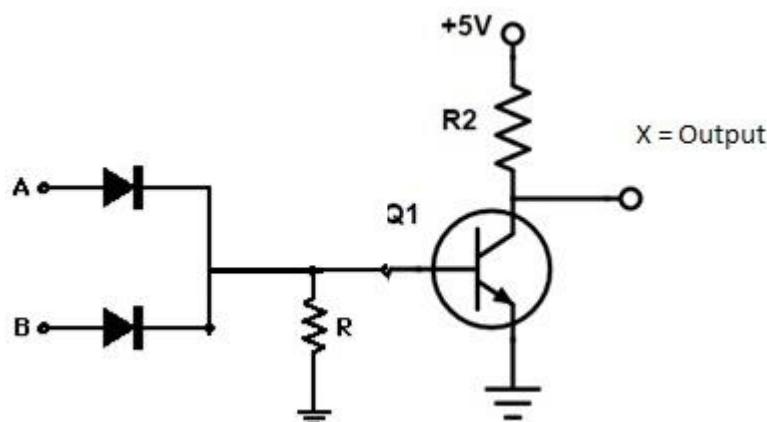


Fig. 1.25: Logic circuit diagram of NOR gate

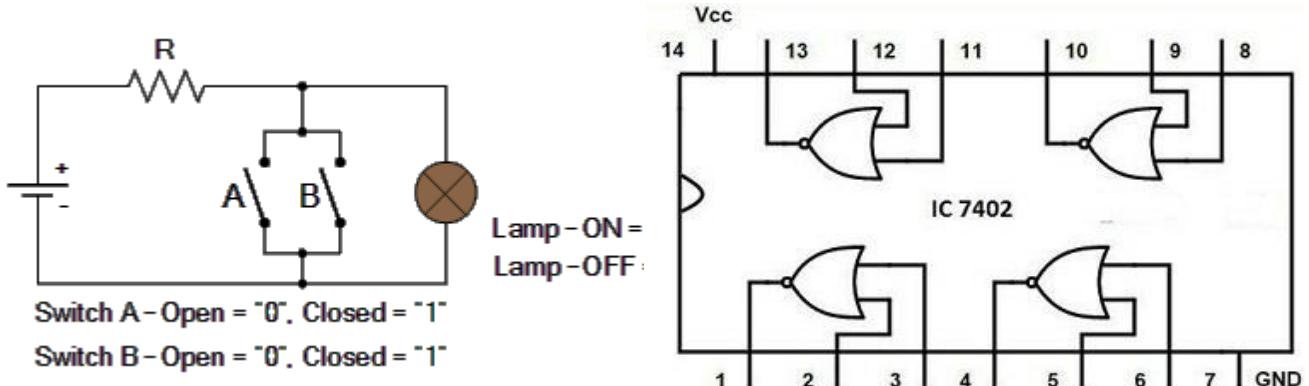


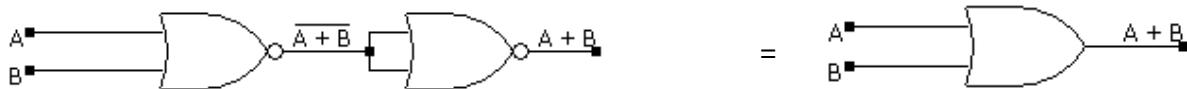
Fig. 1.26: NOR gate switching diagram and IC

NOR gate as Universal gate.

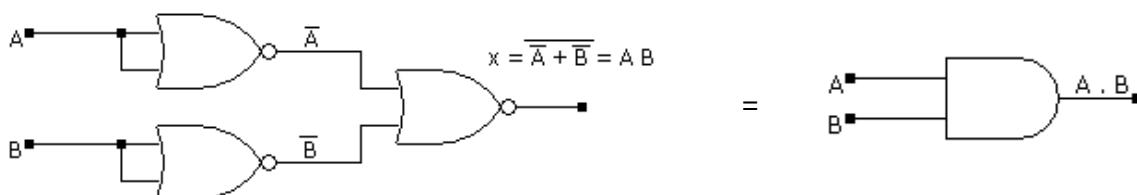
Implementation of NOT Gate:



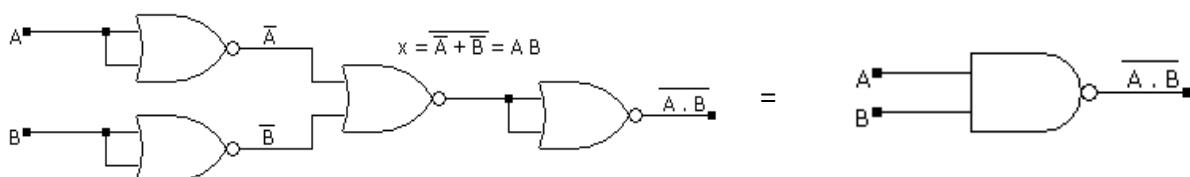
Implementation of OR Gate:



Implementation of AND Gate:



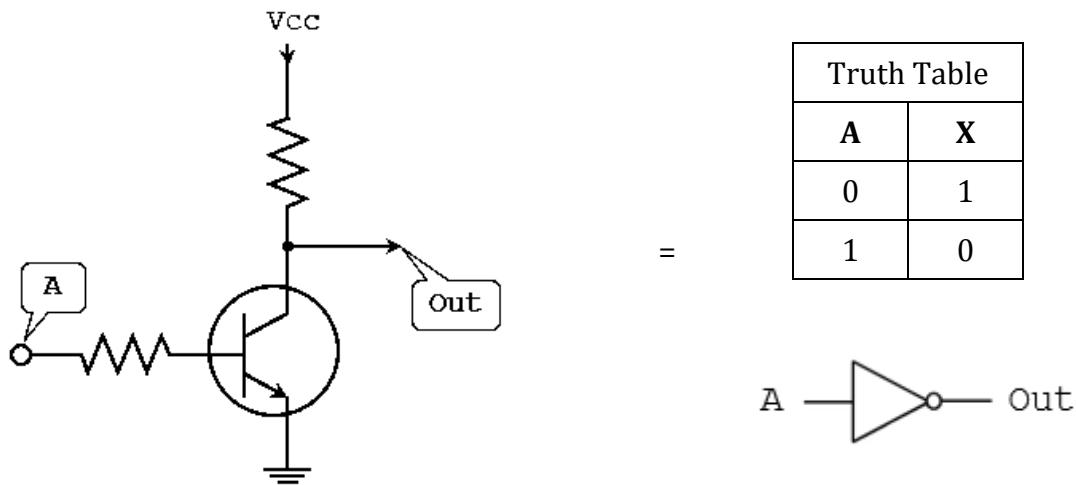
Implementation of NAND Gate:



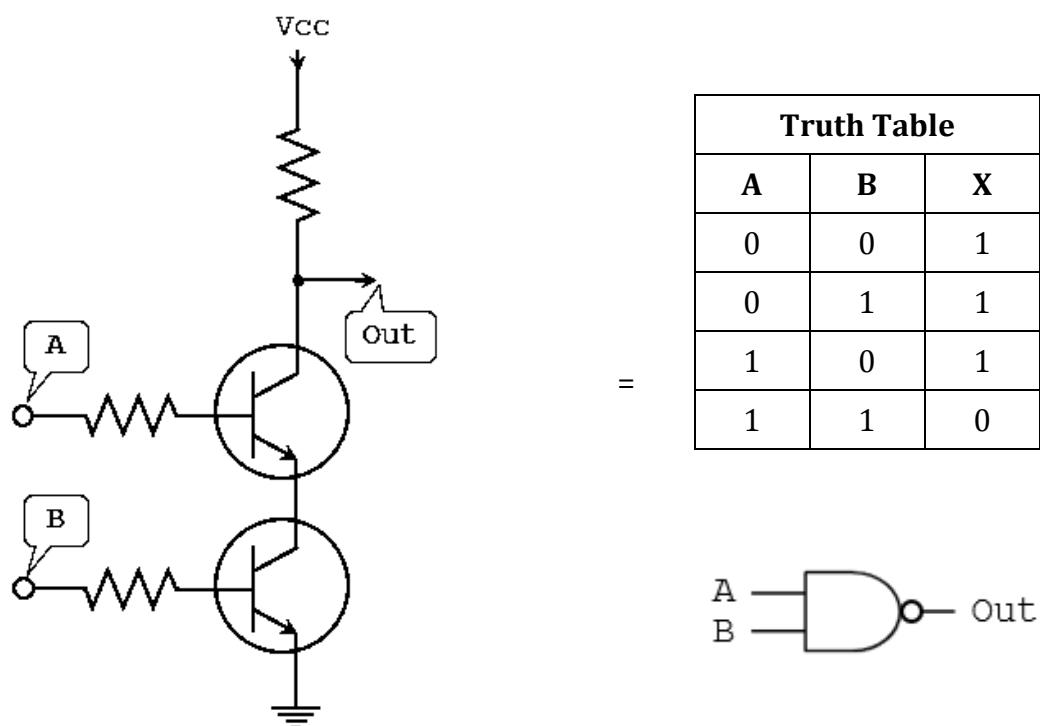
1.8 Construct Logic Gates using Transistors.

A transistor is a device that acts, depending on the voltage level of an input signal, either as a wire that conducts electricity or as a resistor that blocks the flow of electricity. A transistor acts like a switch.

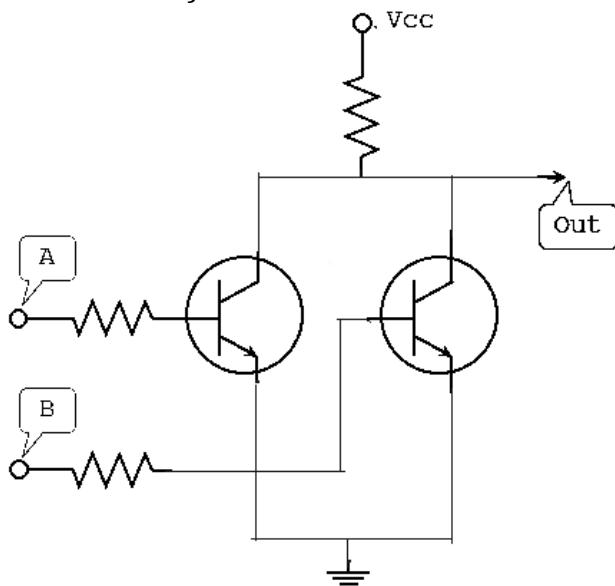
Implementation of NOT Gate:



Implementation of NAND Gate:



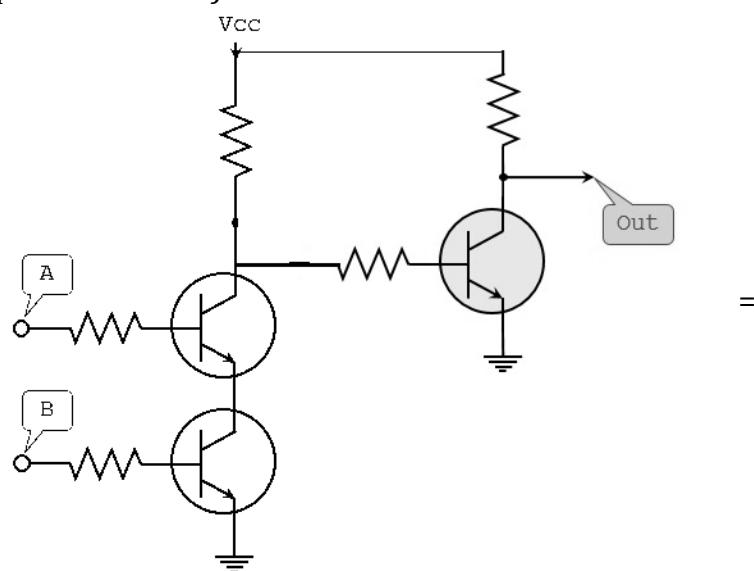
Implementation of NOR Gate:



Truth Table		
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0



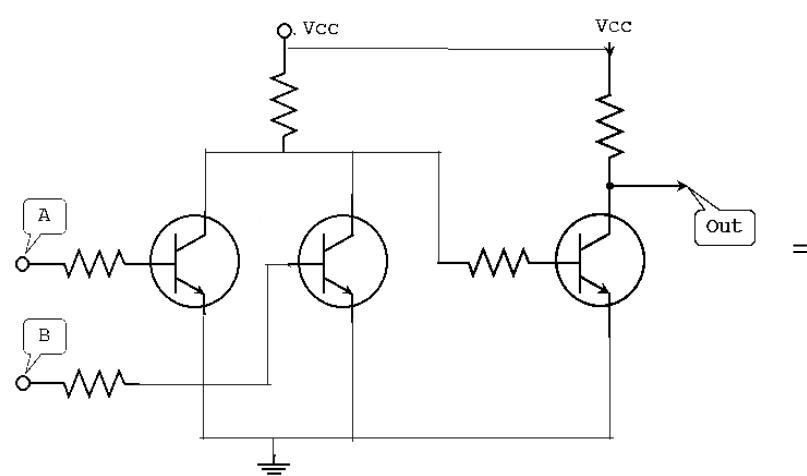
Implementation of AND Gate:



Truth Table		
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1



Implementation of OR Gate



Truth Table		
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1



1.8 Introduction to Logic Families:

It is a circuit configuration or approach used to produce a type of digital integrated circuit. The entire range of digital ICs is fabricated using either bipolar devices or MOS devices or a combination of the two.

Different logic families falling in the first category are called bipolar families, and these include

- Diode Logic (DL)
- Resistor Transfer Logic (RTL)
- Diode Transistor Logic (DTL)
- Transistor Transistor Logic (TTL)
- Emitter Coupled Logic (ECL)
- Integrated Injection Logic (I^2L)

The logic families that use MOS devices as their basis are known as MOS families, and the prominent members belonging to this category are

- PMOS Family (using P-channel MOSFETs)
- NMOS Family (using N-channel MOSFETs)
- CMOS Family (using both N- and P-channel devices)
- Bi-MOS Logic Family uses both Bipolar and MOS devices

From all the logic families listed above, the first three, i.e. DL, RTL and DTL have become obsolete

- Diode Logic used diode & resistors and in fact was never implemented in integrated circuits
- RTL Family used resistors and bipolar transistors
- DTL Family used resistors, diodes and bipolar transistors.

PMOS and I^2L logic families, which were mainly intended for use in custom large-scale integrated (LSI) circuit devices, have also become more or less obsolete.

Logic families that are still in widespread use include TTL, CMOS, ECL, NMOS and Bi-CMOS.

(1) Diode Logic (DL)

Some logic gates can be produced with just Diodes and Resistors are called Diode resistor logic or Diode Logic. Diode logic was used extensively in the construction of early computers.

While diode logic has the advantage of simplicity, the lack of an amplifying stage in each gate limits its application. Not all logical functions can be implemented in diode logic alone. Only the logical AND and logical OR functions can be realized by diode gate.

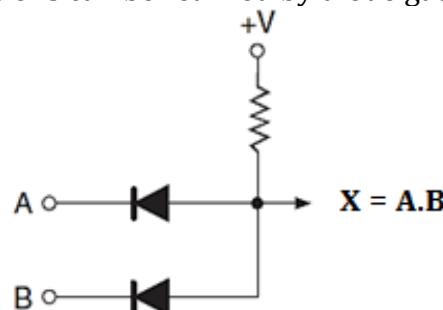


Fig. 1.27: Diode Logic for AND function

(2) Resistor Transistor Logic (RTL)

Digital circuits built using resistors as the input network and bipolar junction transistors (BJTs) as switching devices is known as **Resistor Transistor Logic (RTL)**.

A bipolar transistor switch is the simplest RTL gate (inverter or NOT gate). With two or more base resistors instead of one, the inverter becomes a two-input RTL NOR gate as shown in fig.1.28.

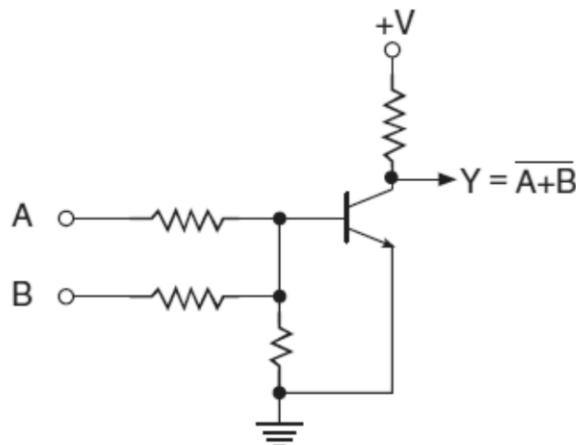


Fig. 1.28: Resistor Transistor Logic for NOR function

The multi-transistor RTL implementation is shown in Fig.1.29. It consists a set of parallel connected transistor switches driven by the logic inputs.

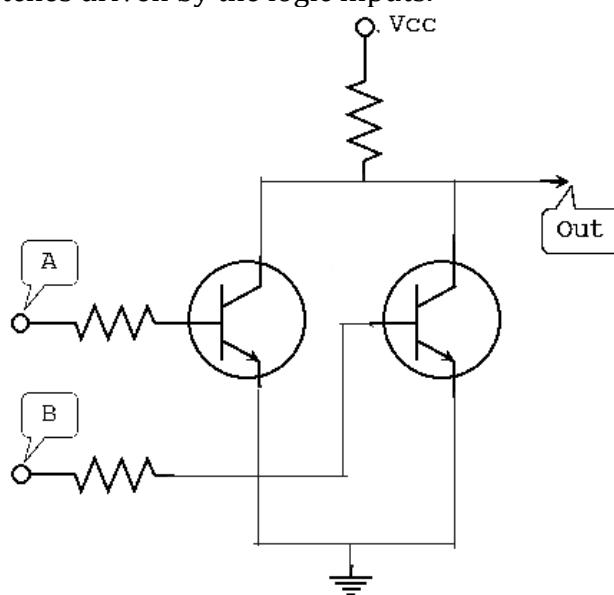


Fig. 1.29: Resistor Transistor Logic for NOR function

The primary advantage of RTL technology was that it used a minimum number of transistors. The disadvantage of RTL is its high power dissipation.

(3) Diode Transistor Logic (DTL)

Diode-Transistor Logic, or DTL, refers to the technology for designing and fabricating digital circuits in which logic gates employ both diodes and transistors.

DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed, especially in comparison to TTL

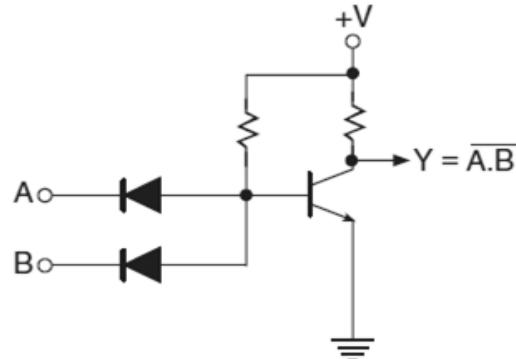


Fig. 1.30: Diode Transistor Logic for NAND function

(4) Transistor Transistor Logic (TTL)

Transistor Transistor Logic (TTL) is a logic family built from bipolar junction transistors. TTL integrated circuits (ICs) were widely used in applications such as computers, industrial controls, test equipment and instrumentation, consumer electronics, and synthesizer.

The multiple-emitter BJT can be used to implement NAND logic. The multiple-emitter BJT forms an integral part of the TTL NAND input circuitry (e.g. the 7400 series of integrated circuits).

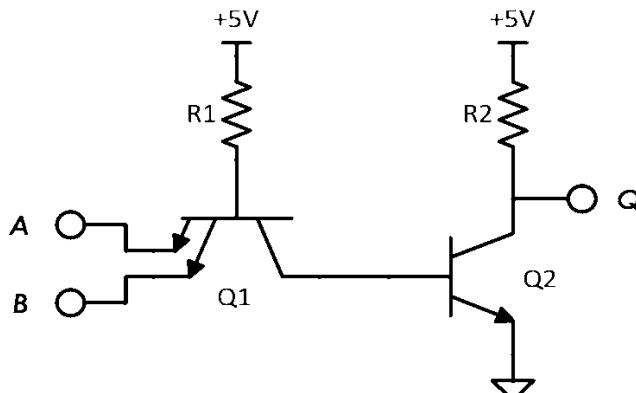


Fig. 1.31: Basic two input TTL NAND function

A two input Basic TTL NAND is shown in Fig.1.31 and two input TTL NAND gate with TOTEM POLE output is shown in Fig.1.32.

Operation of the TTL NAND gate with TOTEM POLE output:

When ***A and B both low***: both B-E junctions of T1 are forward biased. Hence BE junction of transistor Q1 will conduct and force the voltage at collector of Q1 to 0.7V. This voltage is insufficient to forward bias B-E junction of Q2 transistor. Hence Q2 remains OFF. Therefore its collector voltage rises to VCC. As Q3 is operating in emitter follower mode, output Y will be pulled up to high voltage Y= 1

When ***Either A or B low***: If any one input is connected to ground with other left open or connected to logic 1, the corresponding BE junction of transistor Q1 will conduct. This will pull down voltage at Collector of Q2 to 0.7V. This voltage is insufficient to turn on Q2 so it remains OFF. So collector voltage of Q2 will be equal to VCC. This voltage acts as base voltage for Q3. As Q3 acts as an emitter follower, output Y will be pulled to high voltage Y= 1

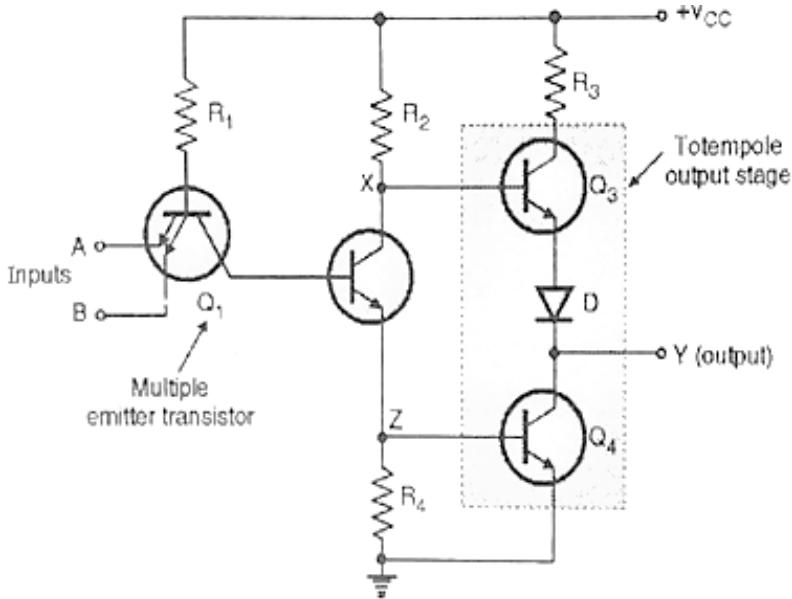


Fig. 1.32: TTL NAND function with TOTEM POLE output

When *A* and *B* both high: If both A and B are connected to logic 1 then both BE junction of transistor Q1 will be reverse biased and do not conduct. Therefore BC junction of Q1 is forward biased and base current is supplied to transistor Q2. As Q2 conducts, the voltage at X will drop down and Q3 will be OFF, whereas voltage at Z will increase to turn ON Q4. As Q4 goes into saturation, the output voltage Y will be pulled down to logic 0. $Y = 0$.

Diode D prevents conduction of Q3 when output is low. Voltage drop across D keeps emitter of Q3 reverse biased.

(5) Integration Injection Logic (I² L)

Integrated injection logic (IIL, I²L, or I2L) is a class of digital circuits built with multiple collector bipolar junction transistors (BJT). When introduced it had speed comparable to TTL yet was almost as low power as CMOS, making it ideal for use in VLSI (and larger) integrated circuits.

The heart of an I²L circuit is the common emitter open collector inverter. Typically, an inverter consists of an NPN transistor with the emitter connected to ground and the base biased with a forward current.

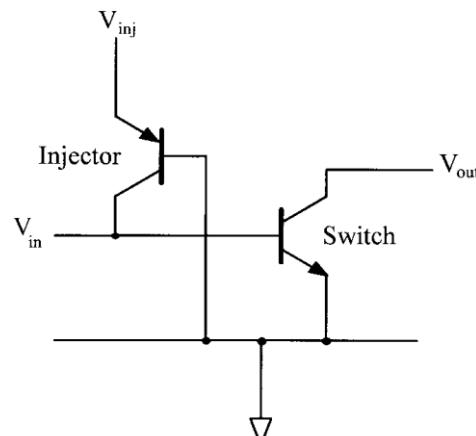


Fig. 1.33: Integration Injection Logic for NOT function

(6) Emitter Coupled Logic (ECL)

Emitter-coupled logic (ECL) is a BJT-based logic family which is generally considered as the fastest logic available. ECL achieves its high-speed operation by employing a relatively small voltage swing and preventing the transistors from entering the saturation region. It has low noise margin. It is preferred for high frequency application.

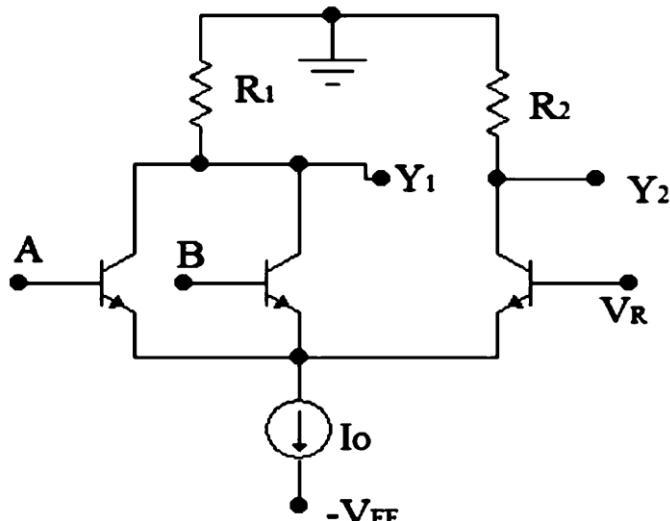


Fig. 1.34: Emitter coupled Logic for NOR/OR function

(7) CMOS (Complementary Metal Oxide Semiconductor) Logic

Complementary metal-oxide semiconductor CMOS is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. CMOS became the most used technology to be implemented in very-large-scale integration (VLSI) chips. (e.g. the 4000 series of integrated circuits).

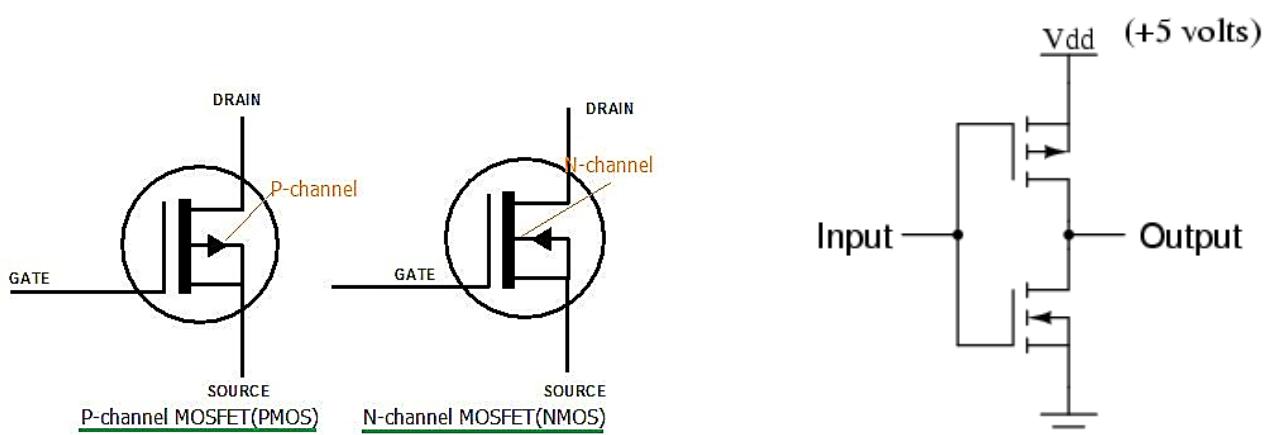


Fig. 1.35: CMOS Inverter/NOT function

1.9 Important terms related to Logic Families

(1) Fan-In:

Maximum number of inputs that can be applied to a single logic gate is known as its Fan-In. OR it is maximum number of inputs a gate can handle.

(2) Fan-Out

It is the number of similar Gates which can be driven by a single logic gate. High Fan-out is advantageous/preferred.

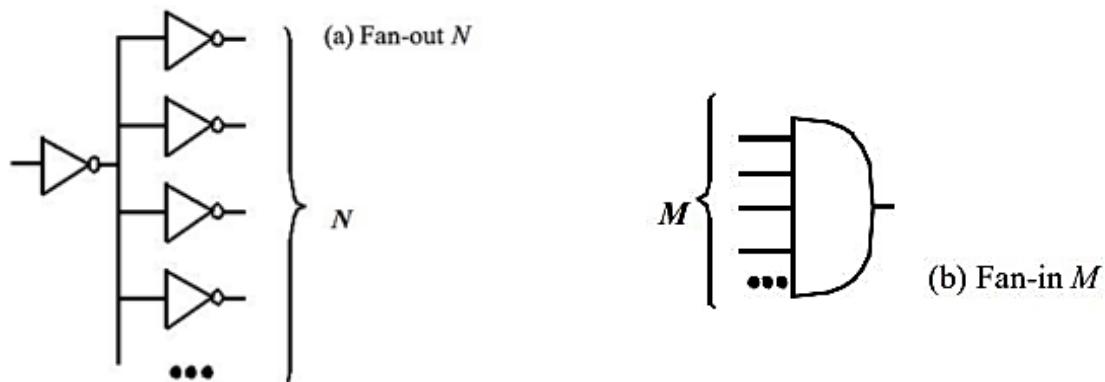


Fig. 1.36: Fan-out and fan-in

(3) Noise Margin

The circuit's ability to tolerate noise signal is referred to as the noise immunity. A quantitative measure of noise immunity is known as Noise Margin.

Noise margin specifies the maximum amplitude of noise pulse that will not change the state of the driven stage/logic gate. Noise margin can be evaluated from a consideration of the voltage levels V_{IHmin} , V_{ILmax} , V_{OHmin} and V_{OLmax}

$V_{ILmax} - V_{OLmax}$ is called **Low Level Noise Margin**

$V_{OHmin} - V_{IHmin}$ is called **High Level Noise Margin**

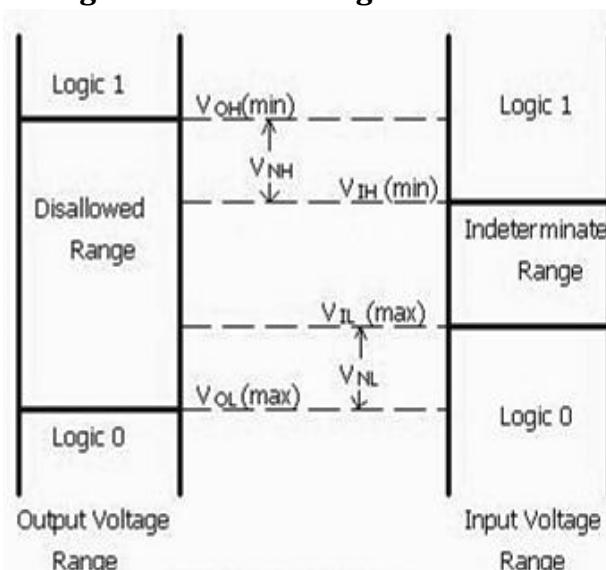


Fig. 1.36: Noise Margin Definition

(4) Propagation Delay Time

It is the time interval between application of data input signal and resulting change in output signal.

(5) Setup Time

It is the minimum time for which the control levels (Input signals) need to be maintained constant at input terminal of logic circuit prior to the arrival of triggering edge of clock pulse.

(6) Hold Time

It is the minimum time for which the control levels (Input signals) need to be maintained constant at input terminal of logic circuit after the arrival of triggering edge of clock pulse.

(7) Switching Time

Another quantity that is used to characterize switching circuits is the speed with which the device responds to the input changes.

For switching circuits, the graph of Fig. 1.37 shows different delay times. Different delay times are of an inverter gate.

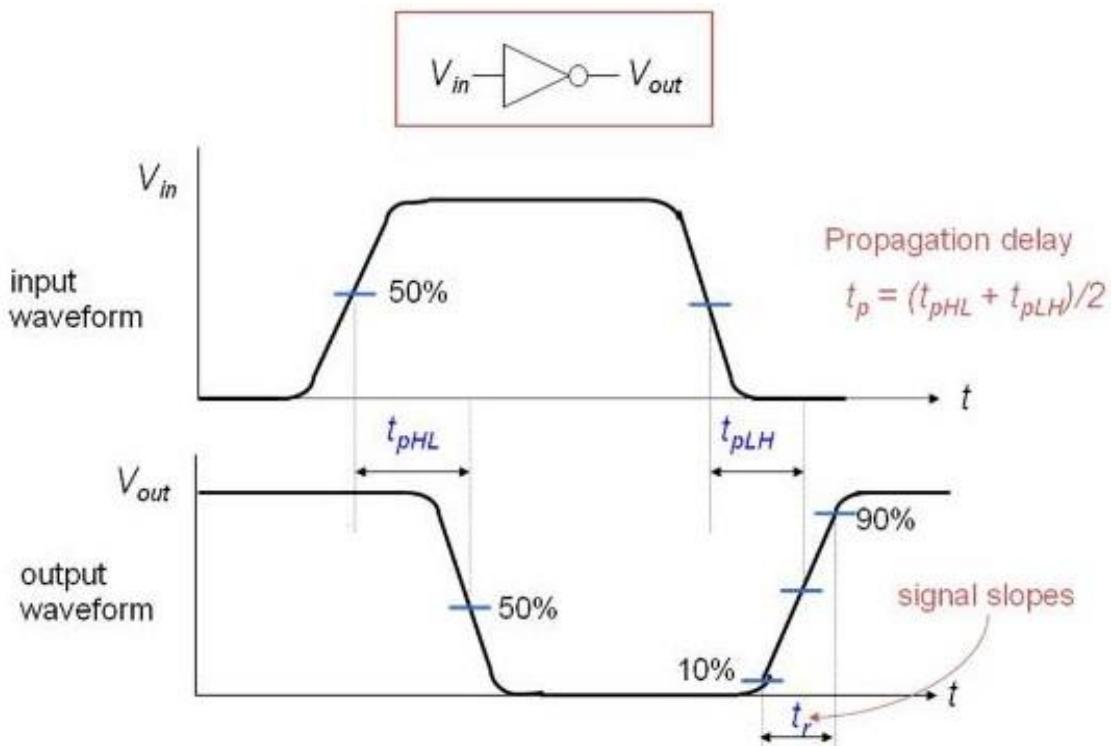


Fig. 1.37: Representation of switching time

Different definitions are as follows:

- **t_{pHL}** (propagation delay time for high to low transition): Difference in time between the point where V_{in} rises to 50% of its final value and the time when V_{out} falls to 50% level from its maximum value.

- **t_{pLH}** (propagation delay time for low to high transition): Time difference between 50% points of the trailing edges of the input and output signals
- **Propagation Delay** : The average of t_{pHL} and t_{pLH} , or

$$t_{pd} = \frac{t_{pHL} + t_{pLH}}{2}$$

- **Fall Time, t_f** : It is the time during which output voltage swing between upper and lower voltage level from 90% to 10% value. (OR time during which signal falls from 90% to 10% value)
- **Rise Time, t_r** : It is the time during which output voltage swing between lower and upper voltage level from 10% to 90% of its maximum value. (OR time during which signal rises from 10% to 90% value)

1.10 comparison of different Logic Families

Parameter	RTL	DTL	TTL	I ² L	ECL	CMOS
Basic Gate	NOR	NAND	NAND	NOR	NOR/OR	NOR/NAND
Power dissipation in mW per gate	12	8-12	10	6 nW – 70 μW	40-55	1
Fan Out	5	8	10	Depends on injector current	25	50
Noise Immunity	Normal	Good	Very Good	Poor	Poor	Very Good
Propagation delay in nS	12	30	10	25-250	2	70

Exercise: Question Bank Unit-6

		Marks
Q:1	Enlist the difference between Analog and Digital Systems	4
Q:2	Enlist the advantages of Digital system over Analog system	4
Q:3	State & Prove De-Morgan's Theorem.	4
Q:4	<p>Explain Basic Logic Gates with necessary Symbol, Truth Table, Logic circuit diagram and it's Boolean Equation.</p> <p style="text-align: center;">OR</p> <p>Draw Symbol, Truth Table and write Boolean equation of NOT gate, OR gate as well as AND gate.</p>	7
Q:5	Draw the circuit diagram of AND gate using Diode and explain it's working with necessary truth table.	4
Q:6	Draw the circuit diagram of OR gate using Diode and explain it's working with necessary truth table.	4
Q:7	Draw the Logic circuit diagram of EX-OR and EX-NOR gate using Basic Logic gates and explain it's working with necessary Symbol, Truth table and Boolean equation	7
Q:8	<p>Explain Universal Logic Gates in detail with necessary circuit diagram, Symbol, Truth Table and its Boolean equation.</p> <p style="text-align: center;">OR</p> <p>Explain NAND as well as NOR gate in detail with necessary circuit diagram, Symbol, Truth Table and its Boolean equation.</p>	7
Q:9	<p>Prove that NAND gate and NOR gate are Universal Logic gates.</p> <p style="text-align: center;">OR</p> <p>Design NOT gate, AND gate, OR gate as well as NOR gate using NAND gate only.</p> <p style="text-align: center;">OR</p> <p>Using NOR gate only, derive Basic Logic Gates.</p>	7
Q:10	Draw the circuit diagram of NOT, AND, OR, NAND, NOR gate using Transistor only.	7
Q:11	<p>Explain different Logic Families in detail</p> <p style="text-align: center;">OR</p> <p>Enlist the name of different Logic Families and explain any two in detail.</p> <p style="text-align: center;">OR</p> <p>Give comparison between Logic Families</p>	7
Q:12	<p>Write short note on TTL logic family.</p> <p style="text-align: center;">OR</p> <p>Draw TTL NAND gate and explain it.</p>	7
Q:13	Draw the circuit diagram of DTL NAND gate and explain.	4

14	<p>Define following terms</p> <ul style="list-style-type: none">(a) Fan-out(b) Fan-in(c) Noise Margin(d) Propagation Delay Time	4
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