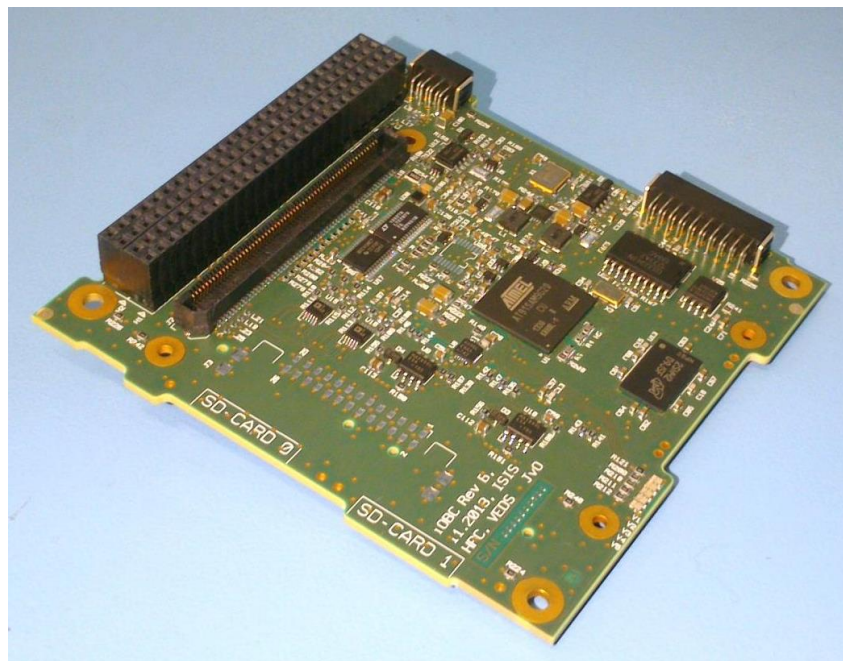


ISIS-OBC Datasheet

ISIS.ISIS-OBC.DS.1.1



Issue 1.2

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Applicable Documents

| | | | |
|------|--|--|--|
| AD01 | | | |
| AD02 | | | |
| AD03 | | | |
| AD04 | | | |

Reference Documents

| | | | |
|------|--------------------------------|---|--------------------|
| RD01 | ISIS-OBC QuickStart Guide v2.1 | iOBC QuickStart Guide | V2.1 |
| RD02 | UM10204 | NXP, I2C-bus specification and user manual, http://www.nxp.com/documents/user_manual/UM10204.pdf | Rev. 6, April 2014 |
| RD03 | | | |
| RD04 | | | |
| RD05 | | | |

TBD/TBC/TBW

| TBD/TBC/TBW | Responsible | Action | Page |
|-------------|-------------|--------|------|
| | | | |
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| | | | |



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List of Acronyms

| | |
|------------------|---|
| 1/2/3U | 1-Unit, 2-Unit, 3-Unit; commonly referring to the singles and multiples of the commercially available CubeSat sizes |
| AIV | Assembly, integration, verification |
| COTS | Commercial off the shelf |
| COM | Centre of Mass |
| EMC | Electro-Magnetic Compatibility |
| EMI | Electro-Magnetic Interference |
| ESD | Electrostatic discharge |
| I ² C | Inter integrated circuit communication bus. |
| iOBC | ISIS on-board computer |
| ISIS | Innovative Solutions In Space BV. |
| RH | Relative Humidity |
| N/A | Not Applicable |
| PWM | Pulse Width Modulation |
| TBC | To Be Confirmed |
| TBD | To Be Determined |
| TBW | To Be Written |
| UM | User Manual |



Table of Contents

| | | |
|----------|--|-----------|
| 1 | Overview | 1 |
| 2 | Functional Description | 2 |
| 3 | Development Environment..... | 5 |
| 4 | Daughterboard option..... | 8 |
| 5 | Connectors location and pin attribution | 12 |
| 6 | Electrical specifications | 21 |
| 7 | Mechanical Characteristics | 26 |
| 8 | Storage and Handling Information..... | 29 |

Table of Figures

| | |
|---|----|
| Figure 2-1: Block diagram. | 2 |
| Figure 3-1: Flight software layers diagram. | 6 |
| Figure 4-1: EM daughterboard assembly (top view). | 9 |
| Figure 4-2: EM daughterboard assembly (X+ side view). | 9 |
| Figure 4-3: EM daughterboard assembly (Y- side view). | 9 |
| Figure 4-4: EM daughterboard assembly (X- side view). | 9 |
| Figure 4-5: FM daughterboard assembly (with iOBC, top view). | 10 |
| Figure 4-6: FM daughterboard (bottom view). | 10 |
| Figure 4-7: FM daughterboard assembly (X+ side view). | 10 |
| Figure 4-8: FM daughterboard assembly (Y- side view). | 10 |
| Figure 4-9: FM daughterboard assembly (X- side view). | 10 |
| Figure 5-1: Connectors location (top). | 13 |
| Figure 5-2: Connectors location (bottom). | 13 |
| Figure 5-3: Stress relief soldered connection. | 14 |
| Figure 5-4: EM daughterboard connector location (top). | 16 |
| Figure 5-5: FM daughterboard connector location (bottom, through view from top). | 19 |
| Figure 7-1: Motherboard outline (top view). | 26 |
| Figure 7-2: Drills, mounting points, J2 centre and H1 pin1 location (top view). | 27 |
| Figure 7-3: Drill sizes. | 27 |
| Figure 7-4: Recommended daughterboard outline [mm] (top view). | 28 |
| Figure 7-5: Height of components on motherboard [mm] (top view). | 28 |

Table of Tables

| | |
|---|----|
| Table 1-1: Overall specifications. | 1 |
| Table 4-1: Daughterboard connector options (mating with J2). | 11 |
| Table 5-1: CSKB pin attribution. | 14 |
| Table 5-2: Breakout wires. | 14 |



| | |
|--|----|
| Table 5-3: J1 pin attribution..... | 14 |
| Table 5-4: J2 pin attribution..... | 15 |
| Table 5-5: J3 pin attribution..... | 16 |
| Table 5-6: J5 pin attribution..... | 17 |
| Table 5-7: J6 pin attribution..... | 17 |
| Table 5-8: J7 pin attribution..... | 18 |
| Table 5-9: J8 pin attribution..... | 18 |
| Table 5-10: J9 pin attribution..... | 18 |
| Table 5-11: J5 pin attribution..... | 19 |
| Table 5-12: J6 pin attribution..... | 20 |
| Table 5-13: J7 pin attribution..... | 20 |
| Table 5-14: J8 pin attribution..... | 20 |
| Table 5-15: J9 pin attribution..... | 20 |
| Table 6-1: Detailed electrical specifications for each net. | 21 |
| Table 6-2: Power on/off requirements. | 25 |
| Table 6-3: Power consumption..... | 25 |

1 Overview

The iOBC is a CubeSat standard compatible On-Board Computer designed specifically for use in Nano-Satellites. It provides a large variety of interfacing options as well as processing capability while still being very power efficient. At the same time, the ability to plug in a daughterboard allows for a great degree of flexibility. Table 1-1 show the general characteristics of the OBC.

Table 1-1: Overall specifications.

| | |
|---------------------------------------|--|
| Processor | 400MHz, 32-bit ARM9 (AT91SAM9G20) |
| RAM | 32MB SDRAM |
| Non-volatile data storage | 2x2GB SD-Cards with FAT32 file system 256kB FRAM (high endurance and fast read/writes) |
| Code storage | 1MB NOR-Flash |
| Timing | 2 redundant real-time Clocks |
| Watchdog | External on-board watchdog and power supervisor |
| On-board sensing | Temperature, current and voltage measurements with over-current protection |
| Interfaces | 1x I ² C (master or slave, Fast-mode, ≤400kbit/s) 1x SPI: Up to 8 slaves (≤10Mbit/s) 2x UARTs (≤10Mbit/s, depending configuration): <ul style="list-style-type: none"> - 1x LVCMOS or RS232 levels (hardware configuration) - 1x RS232 or RS422/485 levels (software configuration) 1x ADC: 8 input channels, 8 or 10-bit modes PWM: 6 output channels GPIO: 27 pins USB: 1x Host and 1x Device (≤12Mbit/s) 1x Image Sensor Interface for directly interfacing with CMOS image sensors (shared with GPIOs) |
| Programming and debug capabilities | JTAG for programming and debugging, Additional debug UART for console user-interface, 4xLEDs |
| Average power consumption | 380mW, typical usage @ 3.3V supply |
| Qualified operating temperature range | -25°C to +65°C |
| Storage temperature range | -40°C to +80°C (RH < 60%) |
| Dimensions | 96 x 90 x 12.4mm (including FM daughterboard) |
| Mass | 106g (including daughterboard) |

2 Functional Description

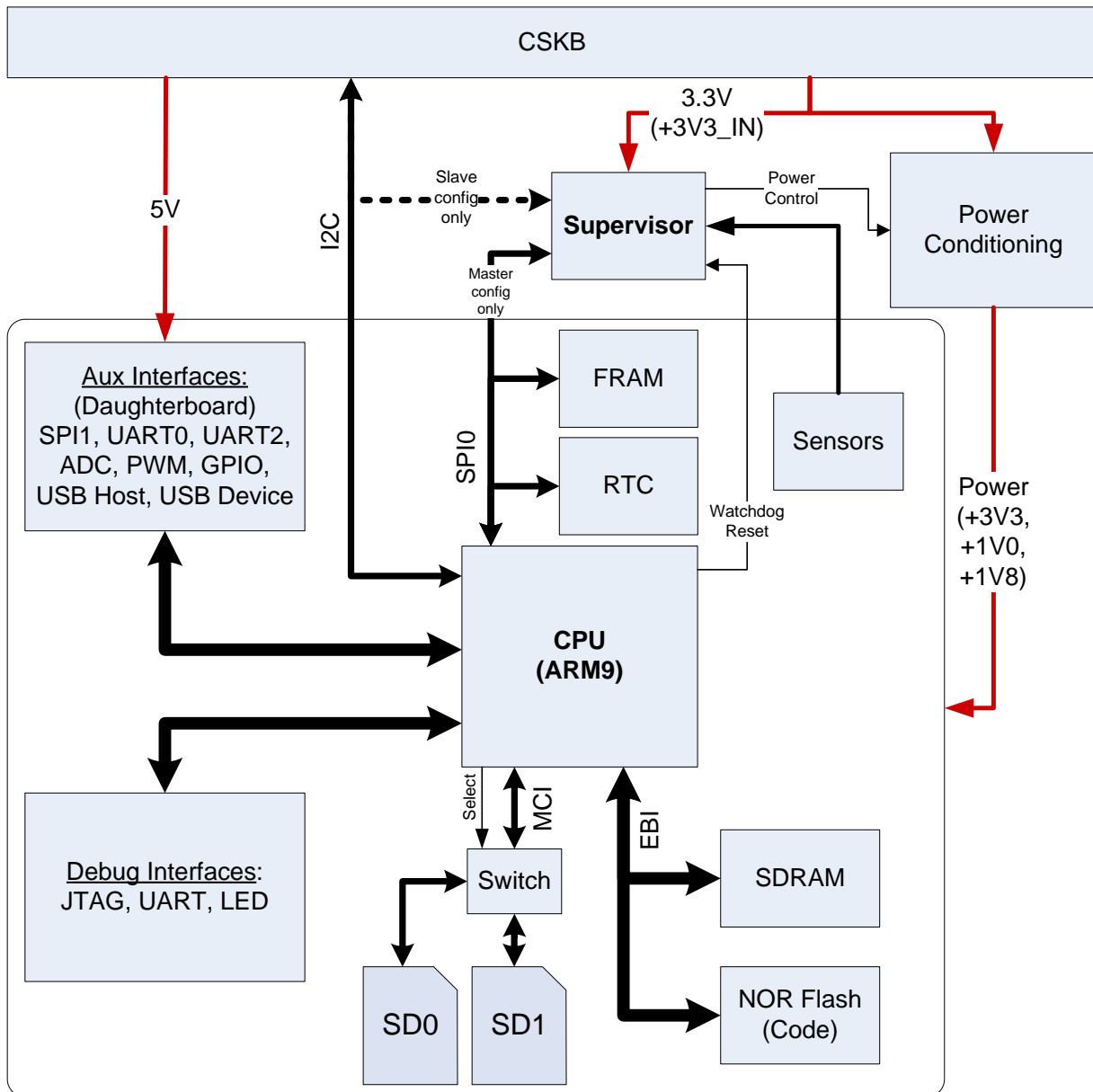


Figure 2-1: Block diagram.

CPU: The iOBC uses a 32-bit ARM9 microprocessor from Atmel (AT91SAM9G20) as its main CPU. Although quite powerful at 400MHz core speed, the processor is quite low-power as it uses 1.0V as its core voltage. The CPU has a number of interfaces to the outside world that are described later.

Supervisor: The supervisor is a PIC microcontroller that controls the power distribution across the board. It can individually switch on/off the CPU along with the other components of the board but separately controls the power of the RTC in order to keep the time on the satellite while the rest of the OBC is power-cycled. The power conditioning circuit includes overcurrent protection.

It also serves the crucial role of an external watchdog for the CPU. This is a window

(frequency) based watchdog: If the CPU toggles the Watchdog-Reset line too frequently or not frequently enough, both cases will lead to the Supervisor power-cycling the OBC.

The Supervisor also has several sensors for Temperature, Voltage and Current measurement. These measurements can be read out by the CPU using the SPI bus. When the iOBC is in a slave configuration, the master OBC can also read this data over the I2C satellite bus.

RAM: The CPU executes its code from this 32MB, low-power SDRAM. Volatile data is also stored here.

Code Storage: The 1MB parallel NOR Flash is used for storing code. When the OBC boots up, the code is copied to the RAM for faster execution.

Critical Data Storage: The OBC has a 256kB FRAM connected to the CPU over an SPI bus. FRAM is a Non-Volatile storage medium that is more robust than Flash or EEPROM memories. It can sustain Trillions of writes (10^{14}) and retain data for >151 years at 65°C (~20 years for typical Flash). It has fast accesses (no delay writes) and it does not require page-erase cycles like a Flash. At the same time, the memory cells are not susceptible to Single Event Upsets (SEU) due to radiations, compared to SRAM cells (note that the memory controller is still susceptible to SEU). Therefore, it should be used for storing critical and changing data such as flight parameters, flight plans etc.

Mass Data Storage: The OBC can use 2x 2GB SD-Cards for mass non-volatile storage of data. ISIS uses high quality industrial SD-Cards with Single Level Cell (SLC) Flash memory to improve reliability of the SD-Cards. Nevertheless, there are 2 cards for redundancy. While one card is in use, the other card is kept off to keep it safe from SEUs and for power-efficiency. Both cards are kept off until they are needed. The OBC uses the FAT32 file system for data storage. FAT32 is chosen for its widespread use and simplicity. However, it is not a journaling file system, making it susceptible to data corruption on power-loss. Therefore, FRAM is provided for storing critical data or data that is updated very often.

Programming and Debug Capabilities: The OBC contains a JTAG interface for programming and debugging of code. 4 LEDs present on the board can be controlled by the CPU for quick debug indication. In addition, a dedicated UART interface is present for user-interface console.

Timing: The OBC contains two Real Time Clocks. The external RTC is an advanced Real Time Clock that is accurate as it compensates for clock-drift due to temperature variations (± 3.5 ppm over temperature range and an additional ± 5 ppm of aging over 10 years). In addition, the CPU contains its own Real Time Timer as well. The timing driver from ISIS uses both these clocks for redundancy.

Interfaces: The iOBC has a very large variety of interfacing options as it was designed to be useable with a variety of payloads and subsystems.

I²C: The I²C bus is the de-facto standard for inter-subsystem communication in CubeSats. The iOBC can be used in Master or Slave configuration and drivers are provided for both. The maximum transfer speed is 400kbit/s (fast-mode), depending on the line capacitance and pull-up resistors. See RD02 for more details.

SPI: Although the CPU has 2 SPI buses, SPI0 is used solely for communication

within the board and SPI1 is used solely for external communication. This is done to keep traffic on one bus from affecting the other, and prevents electrical disturbance from outside factors affecting the board. Both Master and Slave configurations are supported on SPI1. Up to 8 chip select lines are available.

UARTs: The OBC has 2 UART interfaces with a variety of signalling options available. See Table 6-1 for the speed limitations for all configurations.

UART0 can be used as 3.3V TTL signalling or RS232 signalling depending on the configuration requested in the Option Sheet.

UART2 uses a dynamically reconfigurable chip (via software) to support either RS232 (with RTS/CTS flow control) or full-duplex RS422/485 differential bus.

Please note that the UART1 bus of the CPU is not available as those pins are already in use by other functions.

USB: The OBC simultaneously supports both USB host and device as two separate buses at 12Mbits/s. A demo driver for the device mode of USB is provided with the OBC. USB host drivers are not provided with the OBC but can be purchased separately.

ADC: The OBC has an 8-channel, 10-bit ADC which can sample at the maximum rates of 250ksamples/s (8-bit mode) or 75ksamples/s (10-bit mode). The ADC driver supports continuous periodic sampling and uses DMA for efficient operation. The input voltage range is 0V to 2.5V due to the use of an accurate voltage reference (0.1%, $\leq 50\text{ppm}/^{\circ}\text{C}$).

PWM: The OBC supports 6 PWM output channels whose duty-cycles can be controlled individually.

GPIO: The OBC supports 27 GPIO pins. Some of the GPIO pins are also exposed on the CSKB connector for harness free interfacing to other subsystems on the satellite bus. In addition, some of the GPIO pins can also be used alternatively as an Image Sensor Interface which can connect directly to CMOS camera sensors.

Drivers are provided by ISIS for all the interfaces available on the OBC. The drivers for bus interfaces (I2C, SPI, UART) use DMA for efficient transfer and employ FreeRTOS queues for flexibility and maintaining atomicity of transactions while servicing transfer requests from any number of tasks operating in parallel.

Note that freeRTOS is configured to not perform pre-emptive task switching to remove requirements for data contention management. Task switching by freeRTOS is performed once a task yields control through calling the `vTaskDelay` function.

3 Development Environment

The iOBC comes bundled with a Software Development Kit. The SDK can be set up using a convenient installation process.

The SDK consists of the following parts:

1. Eclipse Integrated Development Environment which can be used for developing, compiling and debugging code.
2. ARM GCC compiler which is used directly from Eclipse.
3. FreeRTOS for simple multi-tasking of software on the OBC.
4. Atmel SAM-BA for flashing code to the OBC.
5. PuTTY console for interfacing to the OBC.
6. Libraries from Atmel for basic interfacing to the CPU.
7. FAT32 file system for SD-Cards.
8. ISIS Hardware Abstraction Layer along with code examples to help users getting started quickly.

The Hardware Abstraction Layer (HAL) consists of the following drivers provided by ISIS in addition to the libraries from Atmel and FAT32 file system: I²C, SPI, UART, ADC, PWM, GPIO, LED, FRAM, Timing, Watchdog and Reset, Supervisor interface.

Please see the ISIS OBC QuickStart Guide RD01 for instructions on how to set up your development environment.

3.1 Additional Software

The Hardware Abstraction Layer of the OBC allows for easy, efficient and robust interfacing. However, software for an entire mission involves some additional effort.

Figure 3-1 depicts the several layers of design needed for the OBC Flight Software. ISIS has developed additional libraries that can help in completing this task. These libraries are called the Satellite Subsystem Interface and Mission Support Package.

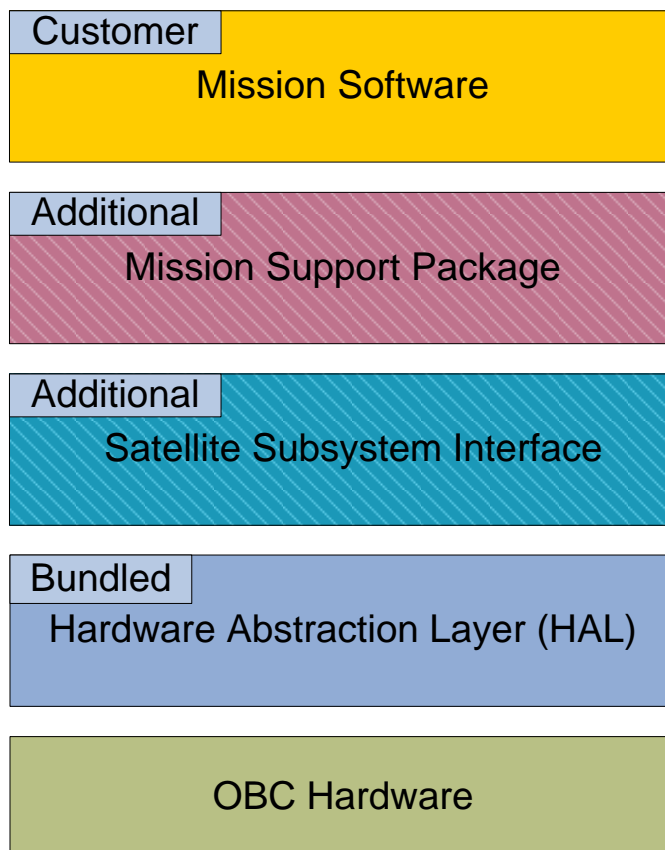


Figure 3-1: Flight software layers diagram.

Satellite Subsystem Interface

This library implements interfaces to a variety of subsystems that can be used on a nanosatellite bus. These interfaces include: ISIS Antenna System, ISIS TRXUV Comm System, ISIS Solar Panels and GomSpace Electrical Power Supply.

ISIS will continue to grow its portfolio of interfaces supported in this library. If you purchase any ISIS subsystem not listed above along with this library, ISIS can support inclusion of that subsystem into this library. Support for specific 3rd party subsystems can be added upon request by customers. Contact support@isispace.nl for additional information.

Mission Support Package

This library provides additional building blocks needed for robust and efficient OBC flight software. The following libraries are currently available as a part of this package:

Parameters Storage: Flight parameters are the key variables used to control the behaviour of the satellite. The parameters storage system keeps these variables in FRAM (which is inherently very robust). In addition, it uses data protection and duplication schemes to provide additional reliability.

Robust Hierarchical Logging: Much of the data acquired by the satellite is stored in non-volatile memory for later retrieval when the satellite passes over the ground



station. Housekeeping data, error logs are some common examples. For simple missions this can also be used to store periodical payload data. This logging mechanism will store the latest data in reliable FRAM and older data in SD-Cards that have more capacity.

ISIS will continue to add several more capabilities into the Mission Support Package. Contact support@isispace.nl for the latest information.

4 Daughterboard option

The ISIS OBC uses a unique combination of a Motherboard and Daughterboard in its design. This approach has several advantages:

1. The daughterboard design is quite flexible and can be built to match different applications while keeping the motherboard the same. This allows customers to add additional interfacing capabilities as required for their application.
2. The daughterboard provides additional fan-out area for connectors and harness for the large variety interfaces supported by the OBC.

When the iOBC is fitted with a daughterboard, it does not use more volume than a standard CSKB board. Therefore, the flexibility of design is achieved without occupying any additional volume on the satellite.

Different types of daughterboards are available from ISIS. Their specifications are described in section 4.1, 4.2, 5.2 and 5.3.

In addition customers can design their own daughterboards or request ISIS for a custom design. Note that specific requirements on the design of the daughterboard have to be followed. This is described in section 4.3.

The daughterboard is mounted with 4x M2 screws to the motherboard. Dedicated spacers are provided as well.

CAUTION: The daughterboard must be mated and de-mated with care in order not to damage any board or connectors. Keep both boards parallel during the process. When fastening the mounting screws, a special attention should be taken in order not to generate any metallic particles that could short traces or exposed pads on the motherboard. Note that it is particularly difficult to see and remove any particle that would go below the BGA package of the CPU or the memory.

4.1 EM Daughterboard

The EM daughterboard is designed for easy use within the laboratory environment. It exposes all the interfaces above the board as standard 2.54mm pin headers which can be probed easily. In addition, standard A and B USB connectors are placed for the host and device USB interface.

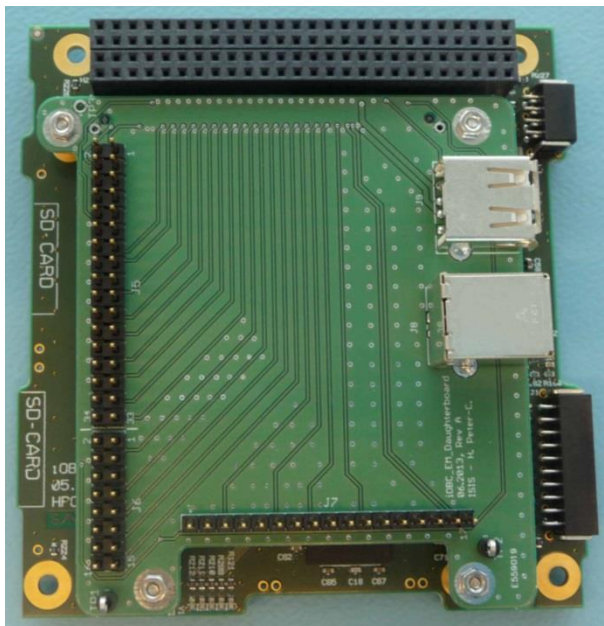


Figure 4-1: EM daughterboard assembly (top view).

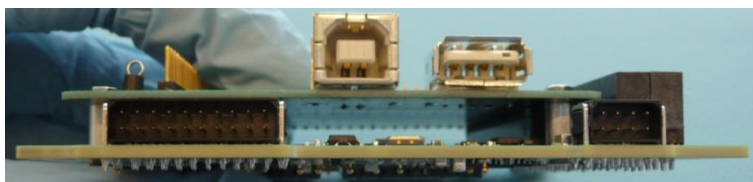


Figure 4-2: EM daughterboard assembly (X+ side view).

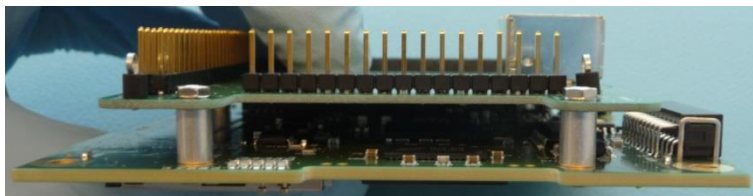


Figure 4-3: EM daughterboard assembly (Y- side view).

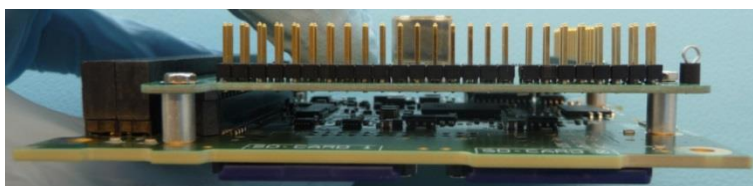


Figure 4-4: EM daughterboard assembly (X- side view).

4.2 FM Daughterboard

In contrast to the EM daughterboard, the FM daughterboard exposes all the signals below the board. This means all the connectors are placed in-between the motherboard and daughterboard which allows for high space efficiency within the satellite. All the connectors can be mated and de-mated from the sides. This makes it easy to alter the connections in an integrated stack. The connectors also have a higher reliability compared to the EM daughterboard.

In order to have the smallest mated height possible, the FM daughterboard uses a

SAMTEC ERM8-060-02.0-S-DV-TR connector to mate with J2. All components are placed on the bottom side of the daughterboard. The PCB thickness is 1mm. The mounting holes have a countersunk and the mounting screws have a flat countersunk head in order to fit within the height of the PCB.

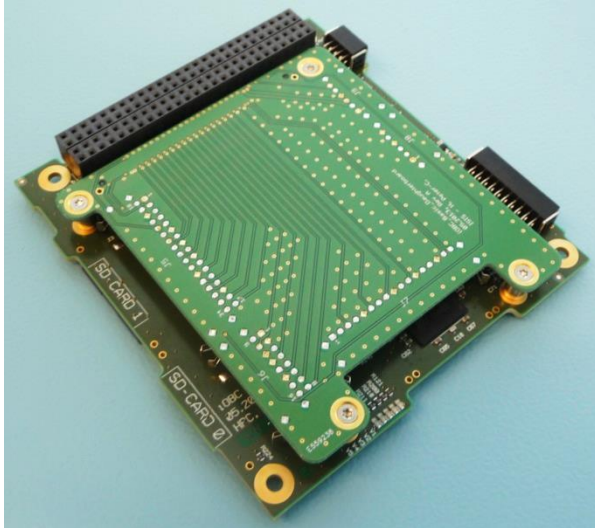


Figure 4-5: FM daughterboard assembly (with iOBC, top view).

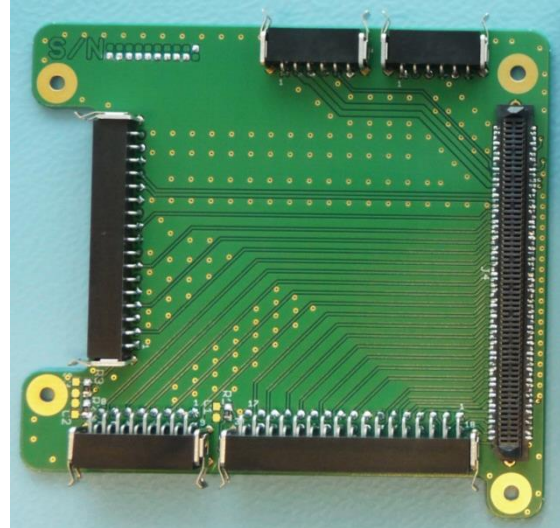


Figure 4-6: FM daughterboard (bottom view).

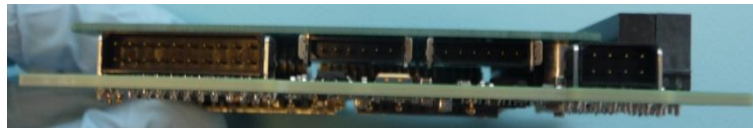


Figure 4-7: FM daughterboard assembly (X+ side view).

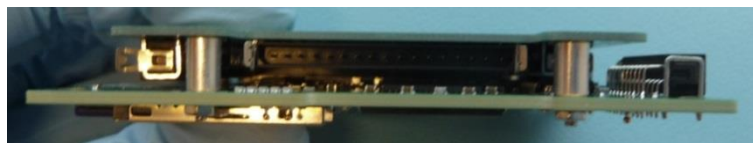


Figure 4-8: FM daughterboard assembly (Y- side view).

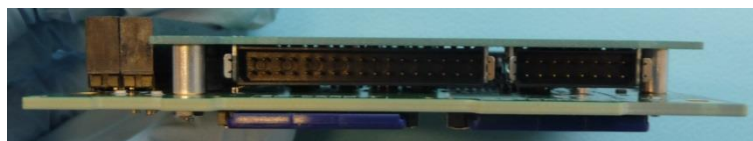


Figure 4-9: FM daughterboard assembly (X- side view).

4.3 Custom Daughterboard

A custom daughterboard can be built in order to take advantage of the full processing power and functionalities offered by the iOBC.

J2 connects the motherboard to the daughterboard. Its pin attribution is described in Table 5-4 while the electrical specifications of the different signals are described in Table 6-1.

There are several options for the mating connector on the daughterboard providing



a choice of distances in between the top of the motherboard and the bottom of the daughterboard. The options are described in Table 4-1.

Table 4-1: Daughterboard connector options (mating with J2).

| Daughterboard connector | Mated height [mm] | Comments |
|------------------------------|----------------------|------------------------------------|
| SAMTEC ERM8-060-02.0-S-DV-TR | 7 | Used on EM and FM daughterboards |
| SAMTEC ERM8-060-05.0-S-DV-TR | 10 | |
| SAMTEC ERM8-060-08.0-S-DV-TR | 13 | Require additional height in stack |
| SAMTEC ERM8-060-09.0-S-DV-TR | 14 | Require additional height in stack |

There are firm limitations in order not to interfere with any component on the motherboard. Detailed mechanical drawings are presented in section 7 for this purpose.

5 Connectors location and pin attribution

5.1 Motherboard

Figure 5-1 and Figure 5-2 show the location of the different connectors on the iOBC motherboard. The 2 SD-cards are placed on the bottom of the board.

Table 5-1 to Table 5-5 show the part number and pin attribution for each connector. The CSKB breakout connections described in Table 5-2 provide pads required to solder wires in order to connect to a different stack (via an in-line connector for example). The wire has to pass through the stress relief hole as shown in Figure 5-3 and then soldered. Epoxy must then be applied to secure the wire in place.

Note that the pins having the same net name on the CSKB (Table 5-1) are **always** connected together electrically, even when they are not used by the iOBC for any internal connection (for example, when the check box corresponding to the respective pin has been left un-ticked in the option sheet).

Note that the Debug LEDs are not described in the pin attribution because they use dedicated output pins on the CPU and have no other connection. Their interface is provided in the HAL library.

A programming and debug adapter connecting to J1 (Table 5-3) is provided by ISIS: it converts to a standard JTAG 20-pin connector and provides a UART over USB for debug purposes. **This adapter disables the supervisor watchdog feature when it is plugged into J1 AND when the SAM-ICE is connected to the 20-pin JTAG connector.**

Note that J3 (Table 5-5) is an optional connector. Normally, it cannot be placed together with a daughterboard since the nets are shared with J2 and because of its height preventing components on the daughterboard on this area. The purpose of this connector is to provide a simple and reliable connector that can be used for flight, in case only a subset of the peripherals is required (SPI1, UART0 and some GPIO). It is possible to use a wired connection in this case without the use of a daughterboard.

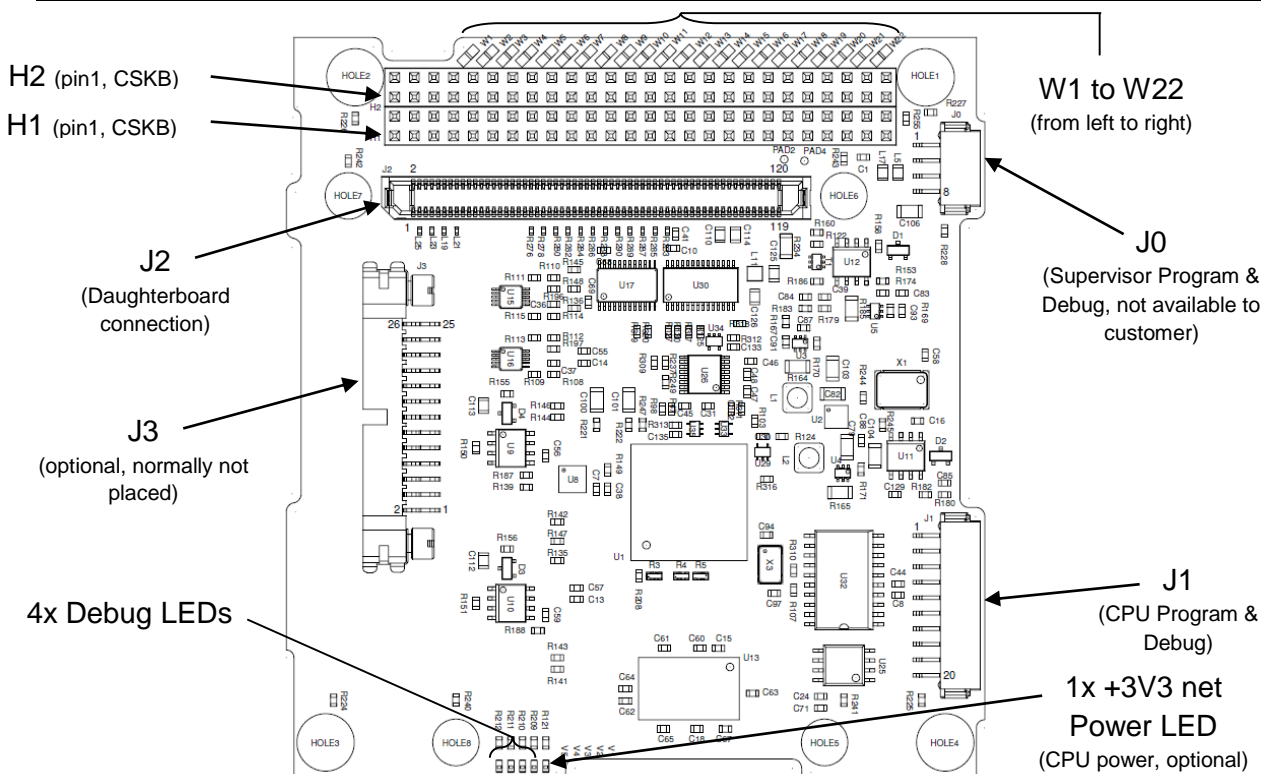


Figure 5-1: Connectors location (top).

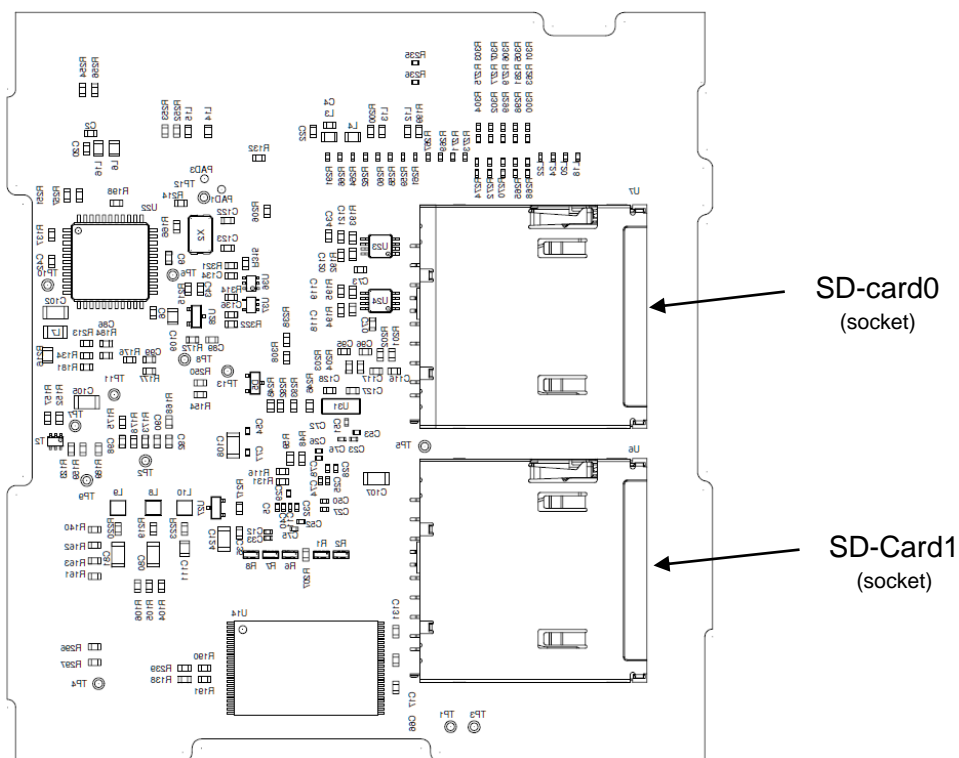


Figure 5-2: Connectors location (bottom).

Table 5-1: CSKB pin attribution.

| Cubesat Kit connector (CSKB) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|---|---|---|---|----|----|----|----|----|----|----------|----------|-----|---------|-----|-----|----|----|----|----|----|-----|---------|---------------|---------------|---------|--|
| ESQ-126-39-G-D or ESQ-126-38-G-D or SSQ-126-21-G-D or TSW-126-07-G-D (Female part of the connector is on top of the board) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H2 | | | | | | | | | | | DRXD | | +5V | +3V3_H2 | GND | GND | | | | | | | VBAT | | GPIO 24 | GPIO 26 | |
| | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | 34 | 36 | 38 | 40 | 42 | 44 | 46 | 48 | 50 | 52 | |
| | | | | | | | | | | | DTXD | | +5V | +3V3_H2 | GND | | | | | | | | VBAT | | | GPIO 25 | |
| | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | 27 | 29 | 31 | 33 | 35 | 37 | 39 | 41 | 43 | 45 | 47 | 49 | 51 | |
| H1 | | | | | | | | | | | | | | | | | | | | | | | GPIO 23 | +3V3_SW1 (al) | +3V3_SW2 (al) | | |
| | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | 34 | 36 | 38 | 40 | 42 | 44 | 46 | 48 | 50 | 52 | |
| | | | | | | | | | | | SCL (al) | SDA (al) | | | | | | | | | | SDA | SCL | GPIO 22 | +5V_SW1 | +5V_SW2 | |
| | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | 27 | 29 | 31 | 33 | 35 | 37 | 39 | 41 | 43 | 45 | 47 | 49 | 51 | |

Table 5-2: Breakout wires.

| Breakout wires | | |
|----------------|---------------|--------------------|
| # | Net name | Comment |
| W1 | DTXD | |
| W2 | DRXD | |
| W3 | GND | |
| W4 | SCL (al) | |
| W5 | SDA (al) | |
| W6 | GND | |
| W7 | +5V | |
| W8 | +5V | |
| W9 | +3V3_H2 | |
| W10 | +3V3_H2 | |
| W11 | GND | |
| W12 | SDA | |
| W13 | SDA | |
| W14 | GND | |
| W15 | SCL | |
| W16 | SCL | |
| W17 | VBAT | Breakout wire only |
| W18 | VBAT | Breakout wire only |
| W19 | +5V_SW1 | Breakout wire only |
| W20 | +3V3_SW1 (al) | |
| W21 | +5V_SW2 | Breakout wire only |
| W22 | +3V3_SW2 (al) | |

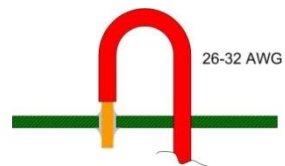


Figure 5-3: Stress relief soldered connection.

Table 5-3: J1 pin attribution.

| J1 | | | | | |
|-------------------------------|----------|----|----------------|---|--|
| CPU (ARM) programming / Debug | | | | | |
| Harwin M80-8412042 | | | | | |
| # | Net name | # | Net name | Comments | |
| 1 | 1 +3V3 | 2 | 11 +3V3 | This is an OUTPUT! Do NOT connect a 3.3V supply here (or it would damage the board). Can source little current. For voltage sensing only. Provides the power to the I/O of the JTAG programmer. | |
| 3 | 2 NTRST | 4 | 12 GND | | |
| 5 | 3 TDI | 6 | 13 GND | | |
| 7 | 4 TMS | 8 | 14 GND | | |
| 9 | 5 TCK | 10 | 15 GND | | |
| 11 | 6 RTCK | 12 | 16 GND | | |
| 13 | 7 TDO | 14 | 17 GND | | |
| 15 | 8 NRST | 16 | 18 GND | | |
| 17 | 9 DRXD | 18 | 19 GND | | |
| 19 | 10 DTXD | 20 | 20 EN_WATCHDOG | Connect to GND to disable supervisor watchdog. Leave open to enable supervisor watchdog. | |



ISIS-OBC Datasheet

Doc ID: ISIS.ISIS-OBC.DS.1.1

Issue: 1.2

Date: 2016-02-10

Page: 15 of 30

Table 5-4: J2 pin attribution.

| J2, Daughterboard I/O, SAMTEC ERF8-060-05.0-S-DV-TR | | | |
|---|--------------|-----|---------------|
| # | Net name | # | Net name |
| 1 | GND | 2 | GND |
| 3 | AIN0 | 4 | AIN1 |
| 5 | GND | 6 | GND |
| 7 | AIN2 | 8 | AIN3 |
| 9 | GND | 10 | GND |
| 11 | AIN4 | 12 | AIN5 |
| 13 | GND | 14 | GND |
| 15 | AIN6 | 16 | AIN7 |
| 17 | GND | 18 | GND |
| 19 | SPI1_NPCS0 | 20 | SPI1_NPCS1 |
| 21 | GND | 22 | GND |
| 23 | SPI1_NPCS2 | 24 | SPI1_SPCK |
| 25 | GND | 26 | GND |
| 27 | SPI1_MOSI | 28 | SPI1_MISO |
| 29 | GND | 30 | GND |
| 31 | GPIO0/D8 | 32 | GPIO1/D9 |
| 33 | GND | 34 | GND |
| 35 | GPIO2/D10 | 36 | GPIO3/D11 |
| 37 | GND | 38 | GND |
| 39 | GPIO4/D0 | 40 | GPIO5/D1 |
| 41 | GND | 42 | GND |
| 43 | GPIO6/D2 | 44 | GPIO7/D3 |
| 45 | GND | 46 | GND |
| 47 | GPIO8/D4 | 48 | GPIO9/D5 |
| 49 | GND | 50 | GND |
| 51 | GPIO10/D6 | 52 | GPIO11/D7 |
| 53 | GND | 54 | GND |
| 55 | GPIO12/PCK | 56 | GPIO13/VSYNC |
| 57 | GND | 58 | GND |
| 59 | GPIO14/HSYNC | 60 | GPIO15/MCK |
| 61 | GND | 62 | GND |
| 63 | GPIO16 | 64 | GPIO17 |
| 65 | GND | 66 | GND |
| 67 | GPIO18 | 68 | GPIO19 |
| 69 | GND | 70 | GND |
| 71 | GPIO20 | 72 | GPIO21 |
| 73 | GND | 74 | GND |
| 75 | PWM0/TC0 | 76 | PWM1 |
| 77 | GND | 78 | GND |
| 79 | PWM2/TC1 | 80 | PWM3 |
| 81 | GND | 82 | GND |
| 83 | PWM4/TC2 | 84 | PWM5 |
| 85 | GND | 86 | GND |
| 87 | RX0 | 88 | TX0 |
| 89 | GND | 90 | GND |
| 91 | RX2/RX+ | 92 | TX2/TX+/TRX+ |
| 93 | CTS2/RX- | 94 | RTS2/TX-/TRX- |
| 95 | GND | 96 | GND |
| 97 | USBD_DP | 98 | USBH_DP |
| 99 | USBD_DM | 100 | USBH_DM |
| 101 | GND | 102 | GND |
| 103 | USBD_VBUS | 104 | USBH_VBUS |
| 105 | GND | 106 | GND |
| 107 | +5V | 108 | +5V |
| 109 | +3V3_IN | 110 | +3V3_IN |
| 111 | +3V3 | 112 | +3V3 |
| 113 | GND | 114 | GND |
| 115 | +5V_SW1 | 116 | +5V_SW1 |
| 117 | test pad 1 | 118 | test pad 2 |
| 119 | test pad 3 | 120 | test pad 4 |

Table 5-5: J3 pin attribution.

| J3 | | | |
|--|---------------|----|---------------|
| Optional, normally not placed. Cannot be placed together with a daughterboard. | | | |
| Harwin M80-5S22605MQ | | | |
| # | Net name | # | Net name |
| 25 | 13 GND | 26 | 26 GND |
| 23 | 12 SPI1_NPCS0 | 24 | 25 SPI1_NPCS1 |
| 21 | 11 GND | 22 | 24 GND |
| 19 | 10 SPI1_NPCS2 | 20 | 23 SPI1_SPCK |
| 17 | 9 GND | 18 | 22 GND |
| 15 | 8 SPI1_MOSI | 16 | 21 SPI1_MISO |
| 13 | 7 GND | 14 | 20 GND |
| 11 | 6 GPIO0/D8 | 12 | 19 GPIO1/D9 |
| 9 | 5 GND | 10 | 18 GND |
| 7 | 4 GPIO2/D10 | 8 | 17 GPIO3/D11 |
| 5 | 3 GND | 6 | 16 GND |
| 3 | 2 RX0 | 4 | 15 TX0 |
| 1 | 1 GND | 2 | 14 GND |

Mechanical SMD pads are connected to GND.

5.2 EM Daughterboard

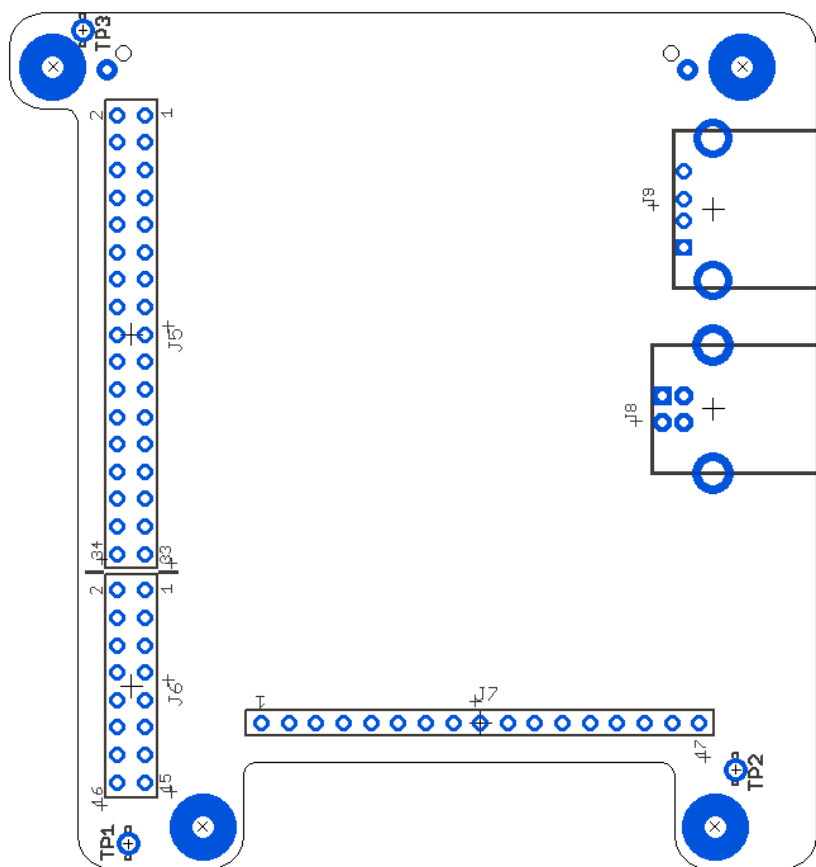


Figure 5-4: EM daughterboard connector location (top).

Figure 5-4 provides the location of the different connectors on the EM daughterboard. Table 5-6 to Table 5-10 provide the part number and pin attribution of the different connectors.

Note that TP1, TP2 and TP3 are connected to GND.

Note that in Table 5-10, USBH_VBUS is 3.3V and not 5V as in a typical USB. Moreover it is not intended to provide power to a device, but should only be used as a power sensing pin, since a 1kohm resistor is placed in serie (see end of Table 6-1 for more details.)

Table 5-6: J5 pin attribution.

| J5 | | | |
|------------------------|------------------|----|--------------|
| 2.54mm male pin header | | | |
| SAMTEC TSW-117-07-F-D | | | |
| # | Net name | # | Net name |
| 2 | 18 AIN0 | 1 | 1 GND |
| 4 | 19 AIN2 | 3 | 2 AIN1 |
| 6 | 20 GND | 5 | 3 AIN3 |
| 8 | 21 AIN5 | 7 | 4 AIN4 |
| 10 | 22 AIN7 | 9 | 5 AIN6 |
| 12 | 23 SPI1_NPCS0 | 11 | 6 GND |
| 14 | 24 SPI1_NPCS2 | 13 | 7 SPI1_NPCS1 |
| 16 | 25 SPI1_SPCK | 15 | 8 GND |
| 18 | 26 SPI1_MISO | 17 | 9 SPI1_MOSI |
| 20 | 27 GPIO0/D8 | 19 | 10 GND |
| 22 | 28 GPIO2/D10 | 21 | 11 GPIO1/D9 |
| 24 | 29 GND | 23 | 12 GPIO3/D11 |
| 26 | 30 GPIO5/D1 | 25 | 13 GPIO4/D0 |
| 28 | 31 GPIO7/D3 | 27 | 14 GPIO6/D2 |
| 30 | 32 GPIO8/D4 | 29 | 15 GND |
| 32 | 33 GPIO10/D6 | 31 | 16 GPIO9/D5 |
| 34 | 34 +3V3_SENSE_J5 | 33 | 17 GPIO11/D7 |

Table 5-7: J6 pin attribution.

| J6 | | | |
|------------------------|------------------|----|----------------|
| 2.54mm male pin header | | | |
| SAMTEC TSW-108-07-F-D | | | |
| # | Net name | # | Net name |
| 2 | 9 GPIO12/PCK | 1 | 1 GND |
| 4 | 10 GPIO13/VSYNC | 3 | 2 GND |
| 6 | 11 GND | 5 | 3 GPIO14/HSYNC |
| 8 | 12 GND | 7 | 4 GPIO15/MCK |
| 10 | 13 GPIO17 | 9 | 5 GPIO16 |
| 12 | 14 GND | 11 | 6 GPIO18 |
| 14 | 15 GPIO20 | 13 | 7 GPIO19 |
| 16 | 16 +3V3_SENSE_J6 | 15 | 8 GPIO21 |

Table 5-8: J7 pin attribution.

| J7 | |
|-------------------------------|-----------------|
| 2.54mm male pin header | |
| SAMTEC TSW-117-07-F-S | |
| # | Net name |
| 1 | +3V3_SENSE_J7 |
| 2 | PWM0/TC0 |
| 3 | PWM1 |
| 4 | PWM2/TC1 |
| 5 | GND |
| 6 | PWM3 |
| 7 | PWM4/TC2 |
| 8 | PWM5 |
| 9 | GND |
| 10 | RX0 |
| 11 | TX0 |
| 12 | GND |
| 13 | RX2/RX+ |
| 14 | CTS2/RX- |
| 15 | GND |
| 16 | TX2/TX+/TRX+ |
| 17 | RTS2/TX-/TRX- |

Table 5-9: J8 pin attribution.

| J8 | |
|--------------------------|-----------------|
| USB-B Connector | |
| FCI 61729-0010BLF | |
| # | Net name |
| 1 | USBD_VBUS |
| 2 | USBD_DM |
| 3 | USBD_DP |
| 4 | GND |

Table 5-10: J9 pin attribution.

| J9 | |
|--------------------------|-----------------|
| USB-A Connector | |
| FCI 87520-0010BLF | |
| # | Net name |
| 1 | USBH_VBUS |
| 2 | USBH_DM |
| 3 | USBH_DP |
| 4 | GND |

5.3 FM Daughterboard

The location of the connectors on the FM daughterboard is shown in Figure 5-5. The part number and pin attribution for all the respective connectors are described in Table 5-11 to Table 5-15.

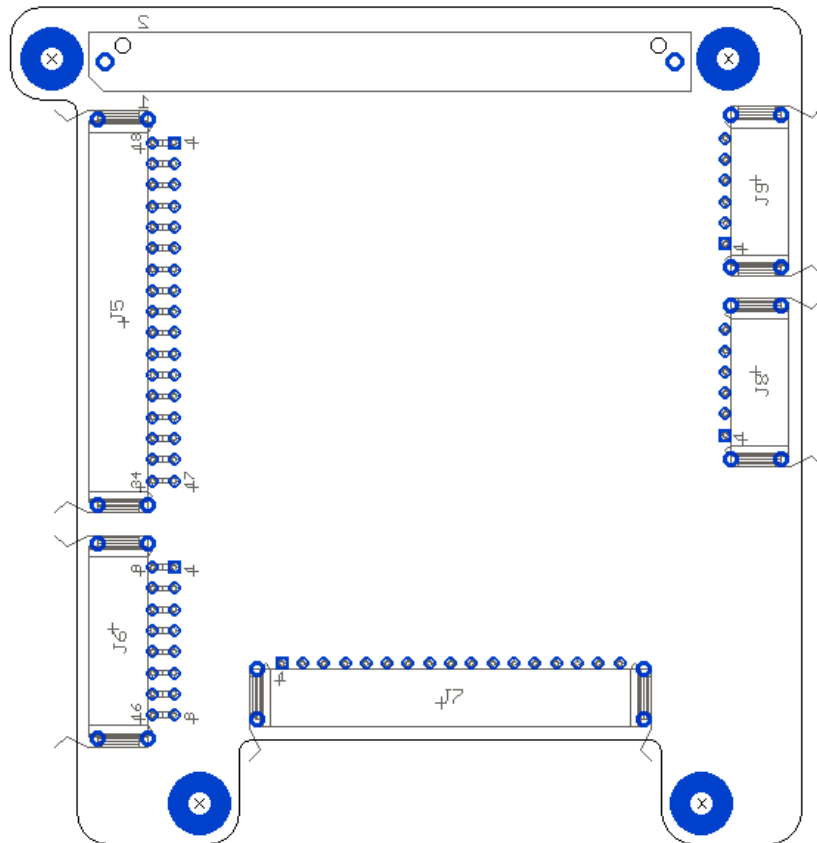


Figure 5-5: FM daughterboard connector location (bottom, through view from top).

Table 5-11: J5 pin attribution.

| J5 | | | |
|------------------------------|--------------|----|------------------|
| Harwin M80-8513442 | | | |
| Mate with Harwin M80-8883405 | | | |
| # | Net name | # | Net name |
| 1 | 1 GND | 2 | 18 AIN0 |
| 3 | 2 AIN1 | 4 | 19 AIN2 |
| 5 | 3 AIN3 | 6 | 20 GND |
| 7 | 4 AIN4 | 8 | 21 AIN5 |
| 9 | 5 AIN6 | 10 | 22 AIN7 |
| 11 | 6 GND | 12 | 23 SPI1_NPCS0 |
| 13 | 7 SPI1_NPCS1 | 14 | 24 SPI1_NPCS2 |
| 15 | 8 GND | 16 | 25 SPI1_SPCK |
| 17 | 9 SPI1_MOSI | 18 | 26 SPI1_MISO |
| 19 | 10 GND | 20 | 27 GPIO0/D8 |
| 21 | 11 GPIO1/D9 | 22 | 28 GPIO2/D10 |
| 23 | 12 GPIO3/D11 | 24 | 29 GND |
| 25 | 13 GPIO4/D0 | 26 | 30 GPIO5/D1 |
| 27 | 14 GPIO6/D2 | 28 | 31 GPIO7/D3 |
| 29 | 15 GND | 30 | 32 GPIO8/D4 |
| 31 | 16 GPIO9/D5 | 32 | 33 GPIO10/D6 |
| 33 | 17 GPIO11/D7 | 34 | 34 +3V3_SENSE_J5 |

Table 5-12: J6 pin attribution.

| J6 | | | |
|------------------------------|----------------|----|------------------|
| Harwin M80-8511642 | | | |
| Mate with Harwin M80-8881605 | | | |
| # | Net name | # | Net name |
| 1 | 1 GND | 2 | 9 GPIO12/PCK |
| 3 | 2 GND | 4 | 10 GPIO13/VSYNC |
| 5 | 3 GPIO14/HSYNC | 6 | 11 GND |
| 7 | 4 GPIO15/MCK | 8 | 12 GND |
| 9 | 5 GPIO16 | 10 | 13 GPIO17 |
| 11 | 6 GPIO18 | 12 | 14 GND |
| 13 | 7 GPIO19 | 14 | 15 GPIO20 |
| 15 | 8 GPIO21 | 16 | 16 +3V3_SENSE_J6 |

Table 5-13: J7 pin attribution.

| J7 | |
|--|---------------|
| Harwin M80-8421742 | |
| Mate with Harwin M80-8981705. Use AWG24 (Harwin M80-9230099) for ~106Ω differential impedance with twisted cables. | |
| # | Net name |
| 1 | +3V3_SENSE_J7 |
| 2 | PWM0/TC0 |
| 3 | PWM1 |
| 4 | PWM2/TC1 |
| 5 | GND |
| 6 | PWM3 |
| 7 | PWM4/TC2 |
| 8 | PWM5 |
| 9 | GND |
| 10 | RX0 |
| 11 | TX0 |
| 12 | GND |
| 13 | RX2/RX+ |
| 14 | CTS2/RX- |
| 15 | GND |
| 16 | TX2/TX+/TRX+ |
| 17 | RTS2/TX-/TRX- |

Table 5-14: J8 pin attribution.

| J8 | |
|--|-----------|
| Harwin M80-8420642 | |
| Mate with Harwin M80-8990605 (large bore). Use AWG22 (Harwin M80-9220099) for ~97Ω differential impedance with twisted cables. | |
| # | Net name |
| 1 | GND |
| 2 | USBD_DP |
| 3 | USBD_DM |
| 4 | GND |
| 5 | USBD_VBUS |
| 6 | GND |

Table 5-15: J9 pin attribution.

| J9 | |
|--|-----------|
| Harwin M80-8420642 | |
| Mate with Harwin M80-8990605 (large bore). Use AWG22 (Harwin M80-9220099) for ~97Ω differential impedance with twisted cables. | |
| # | Net name |
| 1 | GND |
| 2 | USBH_DP |
| 3 | USBH_DM |
| 4 | GND |
| 5 | USBH_VBUS |
| 6 | GND |



6 Electrical specifications

The electrical specifications for all the nets exposed on the connectors are presented in Table 6-1. Table 6-2 and Table 6-3 show additional power supply requirements.

Table 6-1: Detailed electrical specifications for each net.

| Connector name | Net name | Function | Direction | VIL [V] | | VIH min [V] | | VOL [V] | | VOH [V] | | Total serie resistance [Ω]*1 | Pull up/down resistance [Ω] *2 | Speed | Configuration option | Comments |
|------------------|---------------|------------------|-----------|---------|-----|-------------|-----|---------|-----|---------|---------|------------------------------|--------------------------------|-------------|---|--|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | | Typ | | | |
| W3/W6/W11/W14/H2 | GND | Ground | I | 0 | 0 | - | - | - | - | - | - | - | - | - | - | Power supply return, ground |
| W9/W10/H2 | +3V3_H2 | 3.3V power input | I | - | - | 3.1 | 3.5 | - | - | - | - | - | - | - | HW | Default power input, becomes +3V3_IN if used. |
| W20/H1 | +3V3_SW1 (al) | 3.3V power input | I | | | | | | | | | | | | HW | Optional power input, becomes +3V3_IN if used. |
| W22/H1 | +3V3_SW2 (al) | 3.3V power input | I | | | | | | | | | | | | HW | Optional power input, becomes +3V3_IN if used. |
| | +3V3_IN | Main power input | I | | | | | | | | | | | | | Main power input for CPU and supervisor. |
| J2 | +3V3 | CPU power supply | O | - | - | - | - | 0 | - | - | +3V3_IN | - | - | - | - | This is an OUTPUT . Derived internally from +3V3_IN via a current limiting switch. It is the CPU power supply (I/O and DCDC converters for core and memory voltages, and daughterboard). Will go to 0V if the supervisor switches of the CPU (i.e. because of the watchdog trigger). On the daughterboard, supports only typically ~20mA to 30mA (Higher current is possible depending on which peripherals of the CPU are used). Use or sense this power supply on the daughterboard in order to avoid any I/O leakage to the CPU. |
| W7/W8/H2 | +5V | 5.0V input | I/O | - | - | 4.5 | 5.5 | - | - | - | - | - | - | - | - | Not used by iOBC, but available as breakout. Provided to daughterboard. |
| W19/H1/J2 | +5V_SW1 | 5.0V input | I/O | - | - | - | - | - | - | - | - | - | - | - | HW | Switched line on GomSpace EPS, not used by iOBC, but available as breakout and on daughterboard. |
| W21/H1 | +5V_SW2 | 5.0V input | I/O | - | - | - | - | - | - | - | - | - | - | - | HW | Switched line on GomSpace EPS, not used by iOBC, but available as breakout. |
| W17/W18/H2 | VBAT | Battery bus | I/O | - | - | - | - | - | - | - | - | - | - | - | - | Not used by iOBC, but available as breakout. |
| W15/W16/H1 | SCL | I2C clock | I/O | -0.5 | 0.9 | 2.52 | 5.5 | 0 | 0.2 | - | 5.5 | - | - | ≤ 400kbit/s | HW | 5V tolerant. Buffered (with full I2C levels |
| W4/H1 | SCL (al) | | | | | | | | | | | | | | HW | compliance for 3.3V or 5V); a voltage can be |
| W12/W13/H1 | SDA | HW | | | | | | | | | | | | | applied when board is off. ESD protection 5.5kV | |
| W5/H1 | SDA (al) | HW | | | | | | | | | | | | | HBM. | |

*1 : Includes the maximum guaranteed serie resistance of the output buffer and any serie resistor on the line

*2 : "SW, Up" mean that an optional internal pull-up can be configured in software. The pull-up resistance values is 40kΩ ≤ R ≤ 190kΩ. No weak pull-down can be configured. IMPORTANT: the pull-up resistor is ALWAYS enabled during boot and can be disabled afterwards. If it is necessary that the level remains low at during boot, a ≤ 4.7kohm external pull-down resistor must be used.



ISIS-OBC Datasheet

Doc ID: ISIS.ISIS-OBC.DS.1.1

Issue: 1.2

Date: 2016-02-10

Page: 22 of 30

| Connector name | Net name | Function | Dire- ction | VIL [V] | | VIH min [V] | | VOL [V] | | VOH [V] | | Total serie resistance [Ω] ^{*1} | Pull up/down resistance [Ω] ^{*2} | Speed | Configu- ration option | Comments |
|----------------|-------------|------------------------------|----------------|---------|------|-------------|------------|---------|-----|---------|------|--|--|--|------------------------------|--|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | | Typ | | | |
| W1/H2/J1 | DTXD | Debug UART transmit | O | - | - | - | - | 0 | - | - | +3V3 | 380 | SW, Up | 2Mbit/s typ | HW | Optional on H2, available as breakout. Schmitt trigger buffer, 5V tolerant. No leakage in +3V3 when iOBC is off or VIH > +3V3. |
| W2/H2/J1 | DRXD | Debug UART receive | I | -0.5 | 0.89 | 2.25 | 5.5 | - | - | - | - | 330 | 10k, Up | | HW | Optional on H2, available as breakout. Schmitt trigger buffer, 5V tolerant. No leakage in +3V3 when iOBC is off or VIH > +3V3. |
| J1 | +3V3 | JTAG target voltage | O | - | - | - | - | 0 | - | - | +3V3 | - | - | - | - | Used as power for the I/O of the JTAG emulator here. Do not use that pin to power anything else. |
| | NTRST | JTAG reset | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | - | - | +3V3 | - | 1k, Up | - | - | |
| | TDI | JTAG data input | I | -0.3 | 0.8 | 2 | +3V3 + 0.3 | - | - | - | - | | 100k, Up | - | - | |
| | TMS | JTAG mode set | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | - | - | +3V3 | | 100k, Up | - | - | |
| | TCK | JTAG clock | I | -0.3 | 0.8 | 2 | +3V3 + 0.3 | - | - | - | - | | 10k, Up | - | - | |
| | RTCK | JTAG return test clock | O | - | - | - | - | 0 | - | - | +3V3 | - | - | - | - | |
| | TDO | JTAG data output | O | - | - | - | - | 0 | - | - | +3V3 | - | - | - | - | |
| | NRST | Target CPU reset signal | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | - | - | +3V3 | - | 3k3, Up | - | - | |
| | EN_WATCHDOG | Enable watchdog | I | -0.3 | 0.8 | 2 | +3V3 + 0.3 | - | - | - | - | - | 3k3, Up | - | - | Connect to GND to disable watchdog. Leave open to enable watchdog. |
| H1 | GPIO22 | General purpose I/O | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | - | - | +3V3 | 330 - 380 | SW, Up | - | HW | |
| | GPIO23 | | | | | | | | | | | | | | HW | |
| H2 | GPIO24 | | | | | | | | | | | | | | HW | |
| | GPIO25 | | | | | | | | | | | | | | HW | |
| | GPIO26 | | | | | | | | | | | | | | HW | |
| J2 | AIN0 | Analog input | I | 0 | - | - | 2.5 | - | - | - | - | - | - | ≤125kHz signal bandwidth (1 analog channel only, 8 bit mode) | - | Inputs have 1uA leakage max, 40pF typ input capacitance. Note that the ADC uses a 2.5V reference with 0.43% overall accuracy. |
| J2 | AIN1 | | | | | | | | | | | | | | | |
| J2 | AIN2 | | | | | | | | | | | | | | | |
| J2 | AIN3 | | | | | | | | | | | | | | | |
| J2 | AIN4 | | | | | | | | | | | | | | | |
| J2 | AIN5 | | | | | | | | | | | | | | | |
| J2 | AIN6 | | | | | | | | | | | | | | | |
| J2 | AIN7 | | | | | | | | | | | | | | | |
| J2 | SPI1_NPCS0 | SPI chip select | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | - | - | +3V3 | 150 | SW, Up | - | SW | Via level shifter; an external pull-down will not guarantee a low level at boot. The level will set high during boot. Output only: used for SPI master only. |
| J2 | SPI1_NPCS1 | | O | | | | | | | | | 125 | - | | SW | |
| J2 | SPI1_NPCS2 | | 125 | | | | | | | | | - | SW | | | |
| J2 | SPI1_SPCK | SPI clock | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | - | - | +3V3 | 100 - 150 | SW, Up | ≤10Mbit/s | SW | |
| J2 | SPI1_MOSI | SPI data master out slave in | | | | | | | | | | | | | SW | |
| J2 | SPI1_MISO | SPI data master in slave out | | | | | | | | | | | | | SW | |



ISIS-OBC Datasheet

Doc ID: ISIS.ISIS-OBC.DS.1.1

Issue: 1.2

Date: 2016-02-10

Page: 23 of 30

| Connector name | Net name | Function | Direction | VIL [V] | | VIH min [V] | | VOL [V] | | VOH [V] | | Total series resistance [Ω] ^{*1} | Pull up/down resistance [Ω] ^{*2} | Speed | Configuration option | Comments |
|----------------|-------------|------------------------------------|-----------|---------|-----|-------------|------------|---------|-----|---------|------|---|---|-------|----------------------|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | | Typ | | | |
| J2 | GPIO0/D8 | Image sensor data | I | -0.3 | 0.8 | 2 | +3V3 + 0.3 | - | - | - | - | 100 | SW, Up | - | SW | |
| J2 | GPIO1/D9 | | | | | | | | | | | | | | SW | |
| J2 | GPIO2/D10 | | | | | | | | | | | | | | SW | |
| J2 | GPIO3/D11 | | | | | | | | | | | | | | SW | |
| J2 | GPIO4/D0 | | | | | | | | | | | | | | SW | |
| J2 | GPIO5/D1 | | | | | | | | | | | | | | SW | |
| J2 | GPIO6/D2 | | | | | | | | | | | | | | SW | |
| J2 | GPIO7/D3 | | | | | | | | | | | | | | SW | |
| J2 | GPIO8/D4 | | | | | | | | | | | | | | SW | |
| J2 | GPIO9/D5 | | | | | | | | | | | | | | SW | |
| J2 | GPIO10/D6 | | | | | | | | | | | | | | SW | |
| J2 | GPIO11/D7 | | | | | | | | | | | | | | SW | |
| J2 | GPIO12/PCK | Image sensor pixel clock | I | -0.3 | 0.8 | 2 | +3V3 + 0.3 | - | - | - | - | 100 | SW, Up | - | SW | |
| J2 | GPIO13/VSYN | Image sensor vertical sync | | | | | | | | | | | | | SW | |
| J2 | GPIO14/HSYN | Image sensor pixel horizontal sync | | | | | | | | | | | | | SW | |
| J2 | GPIO15/MCK | Image sensor clock to sensor | O | - | - | - | - | 0 | - | - | +3V3 | 150 | SW, Up | - | SW | |
| J2 | GPIO0/D8 | General purpose I/O | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | - | - | +3V3 | 100 - 150 | SW, Up | - | SW | Optional SW chip select for SPI1: SPI1_NPCS3_SW |
| J2 | GPIO1/D9 | | | | | | | | | | | | | | SW | Optional SW chip select for SPI1: SPI1_NPCS4_SW |
| J2 | GPIO2/D10 | | | | | | | | | | | | | | SW | Optional SW chip select for SPI1: SPI1_NPCS5_SW |
| J2 | GPIO3/D11 | | | | | | | | | | | | | | SW | Optional SW chip select for SPI1: SPI1_NPCS6_SW |
| J2 | GPIO4/D0 | | | | | | | | | | | | | | SW | Optional SW chip select for SPI1: SPI1_NPCS7_SW |
| J2 | GPIO5/D1 | | | | | | | | | | | | | | SW | |
| J2 | GPIO6/D2 | | | | | | | | | | | | | | SW | |
| J2 | GPIO7/D3 | | | | | | | | | | | | | | SW | |
| J2 | GPIO8/D4 | | | | | | | | | | | | | | SW | |
| J2 | GPIO9/D5 | | | | | | | | | | | | | | SW | |
| J2 | GPIO10/D6 | | | | | | | | | | | | | | SW | |
| J2 | GPIO11/D7 | | | | | | | | | | | | | | SW | |
| J2 | GPIO12/PCK | | | | | | | | | | | | | | SW | |
| J2 | GPIO13/VSYN | | | | | | | | | | | | | | SW | |
| J2 | GPIO14/HSYN | | | | | | | | | | | | | | SW | |
| J2 | GPIO15/MCK | | | | | | | | | | | | | | SW | |
| J2 | GPIO16 | | | | | | | | | | | | | | SW | |
| J2 | GPIO17 | | | | | | | | | | | | | | SW | |
| J2 | GPIO18 | | | | | | | | | | | | | | SW | |
| J2 | GPIO19 | | | | | | | | | | | | | | SW | |
| J2 | GPIO20 | | | | | | | | | | | | | | SW | |
| J2 | GPIO21 | | | | | | | | | | | | | | SW | |



ISIS-OBC Datasheet

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Issue: 1.2

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Page: 24 of 30

| Connector name | Net name | Function | Dire- ction | VIL [V] | | VIH min [V] | | VOL [V] | | VOH [V] | | Total serie resistance [Ω] ^{*1} | Pull up/down resistance [Ω] ^{*2} | Speed | Configu- ration option | Comments |
|----------------|---------------|---|----------------|---|------|-------------|------------|---|-----|---------|------|--|--|--|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | | Typ | | | |
| J2 | PWM0/TC0 | PWM output | O | - | - | - | - | 0 | - | - | +3V3 | 150 | SW, Up | ≤33MHz | SW | Via level shifter; an external pull-down will not garantee a low level at boot. The level will set high during boot. Output only. |
| J2 | PWM1 | | | | | | | | | | | 125 | - | | - | |
| J2 | PWM2/TC1 | | | | | | | | | | | 150 | SW, Up | | SW | |
| J2 | PWM3 | | | | | | | | | | | 125 | - | | - | |
| J2 | PWM4/TC2 | | | | | | | | | | | 150 | SW, Up | | SW | |
| J2 | PWM5 | | | | | | | | | | | 125 | - | | - | |
| J2 | PWM0/TC0 | Timer counter input | I | -0.3 | 0.8 | 2 | +3V3 + 0.3 | - | - | - | - | 100 | SW, Up | TBD | SW | Timer counter / capture functionality not implemented in HAL yet. |
| J2 | PWM2/TC1 | | | | | | | | | | | | | | SW | |
| J2 | PWM4/TC2 | | | | | | | | | | | | | | SW | |
| J2 | RX0 | UART receive | I | -0.5 | 0.89 | 2.25 | 5.5 | - | - | - | - | 100 | 100k, Up | ≤500kbit/s TBC (SW limited) | HW | Schmitt trigger buffer, 5V tolerant. Small leakage via 100kohm into +3V3 when iOBC is off or VIH > +3V3. |
| J2 | TX0 | UART transmit | O | - | - | - | - | 0 | - | - | +3V3 | 150 | SW, Up | | HW | |
| J2 | RX0 | RS232 receive | I | -25 | 0.6 | 2.4 | 25 | - | - | - | - | - | 5k, Down | ≤500kbit/s (SW limited), ≥250kbit/s | HW | ESD protection +-15kV HBM. |
| J2 | TX0 | RS232 transmit | O | - | - | - | - | -13.2 | -5 | 5 | 13.2 | - | - | | HW | |
| J2 | RX2/RX+ | RS232 receive | I | -15 | 0.5 | 2.5 | 15 | - | - | - | - | - | 5k, Down | typ @ 1000pF //3kΩ load | SW | ESD protection +-26kV HBM. |
| J2 | CTS2/RX- | RS232 clear to send | | | | | | | | | | | | | SW | |
| J2 | TX2/TX+/TRX+ | RS232 transmit | O | - | - | - | - | -7.5 | -5 | 5 | 7.5 | - | - | | SW | |
| J2 | RTS2/TX-/TRX- | RS232 ready to send | | | | | | | | | | | | | SW | |
| J2 | RX2/RX+ | RS485 full duplex receive | I | +-15V absolute voltage max, +6V differential max, +0.2V threshold max | | | | +6V differential max, +- 0.2V differential min, +3V common mode voltage max | | | | - | 125k, Down | SW | ESD protection +-26kV HBM. Software enabled 120ohm differential termination. 120ohm differential impedance. | |
| J2 | CTS2/RX- | RS485 full duplex transmit | O | | | | | | | | | | | SW | | |
| J2 | TX2/TX+/TRX+ | | I/O | | | | | | | | | | | SW | | |
| J2 | RTS2/TX-/TRX- | | | | | | | | | | | | | SW | | |
| J2 | TX2/TX+/TRX+ | RS485 single duplex transmit receive | | | | | | | | | | | | TBD | SW | Functionality not implemented in HAL yet. |
| J2 | TX2/TX+/TRX- | | | | | | | | | | | | | | SW | |
| J2 | USB_DP | USB data | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | 0.3 | 2.8 | 3.6 | - | - | ≤12Mbit/s | - | 90ohm differential impedance. |
| J2 | USB_DM | | | | | | | | | | | | | | - | |
| J2 | USB_VBUS | USB connection sense | I | -0.5 | 0.89 | 2.25 | 5.5 | - | - | - | - | - | 27k, Down | - | - | Schmitt trigger buffer, 5V tolerant. No leakage into +3V3 when iOBC is off or VIH > +3V3. |
| J2 | USBH_DP | USB data | I/O | -0.3 | 0.8 | 2 | +3V3 + 0.3 | 0 | 0.3 | 2.8 | 3.6 | - | - | ≤12Mbit/s | - | 90ohm differential impedance. |
| J2 | USBH_DM | | | | | | | | | | | | | | - | |
| J2 | USBH_VBUS | USB connection sense | O | - | - | - | - | 0 | - | - | +3V3 | 1k | - | - | - | Connected to +3V3 via 1kohm. |
| J5, J6, J7 | +3V3_SENSE_Jx | Sense power of DMU | | | | | | | | | | | | | | |

Table 6-2: Power on/off requirements.

| +3V3_IN Input voltage rate [V/ms] | | | |
|-----------------------------------|-----|-----|---|
| | Min | Max | Comments |
| Rise rate (at power-on) | 0.2 | 5 | Higher slew rate than the maximum specified might damage EMI filters on the iOBC or create brownout issues due to the large amount of capacitance present on the board. |
| Fall rate (at power-off) | - | - | No requirement |

Table 6-3: Power consumption.

| Configu- ration | State description ⁽¹⁾ | Parameter | Unit | Value for +3V3_IN net | | | Comments |
|------------------------|---|-----------------|--------------|-----------------------|--------------------|--------------------|---|
| | | | | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽⁴⁾ | |
| - | All | +3V3_IN voltage | V | 3.1 | 3.3 | 3.5 | |
| Master and slave | CPU ON, typical usage ⁽⁵⁾ | Average current | mA | 64.5 | 116 | 158 | Depending on peripherals used and processing load. Without any I/O sourcing current. |
| | | Average power | mW | 200 | 383 | 551 | |
| | CPU ON, using SD- Card | Average current | mA | - | 95 | - | |
| | | At CPU power on | Peak current | mA | - | 530 | - |
| Master | IDLE (CPU IDLE) | Average current | mA | 61 | 64.5 | 75.3 | |
| | | Average power | mW | 188 | 213 | 263 | |
| Slave | IDLE (CPU off) | Average current | mA | 7.2 | 8.4 | 10.9 | |
| | | Average power | mW | 22 | 28 | 38 | |

⁽¹⁾ Note that the supervisor is powered on in all configurations and all cases. It cannot be switched off.

⁽²⁾ Over full temperature and input voltage range.

⁽³⁾ At 20°C and 3.30V input voltage.

⁽⁴⁾ Over full temperature and input voltage range and including 5% margin from measured value.

⁽⁵⁾ Typical situation using SDRAM, SD-Card, SPI, PWM, ...

7 Mechanical Characteristics

Figure 7-2 and Figure 7-3 provides the position of the different mounting holes on the motherboard. The centre of J2 are pin 1 of H1 are also indicated.

The mounting pads are plated through holes (they cannot be threaded). They are normally connected to GND but can be disconnected on request. The mounting pads are:

- Motherboard: 3.2mm drill, 7.4mm diameter pad (for typical 6mm diameter spacer).
- Daughterboard: 2.2mm drill, 6mm diameter pad (for typical 5mm diameter spacer).

Figure 7-4 shows the recommended daughterboard outline for custom daughterboards. Figure 7-5 shows the height of the different components on the motherboard per area. Table 4-1 shows the different mating height options for the daughterboard. These values constrain the design of the daughterboard, in order not to clash with any component on the motherboard.

Note: it is highly recommended to keep at least 1.5mm of clearance in between any component on the motherboard and the custom daughterboard. This is necessary since the boards bend due to the vibrations in the launch environment.

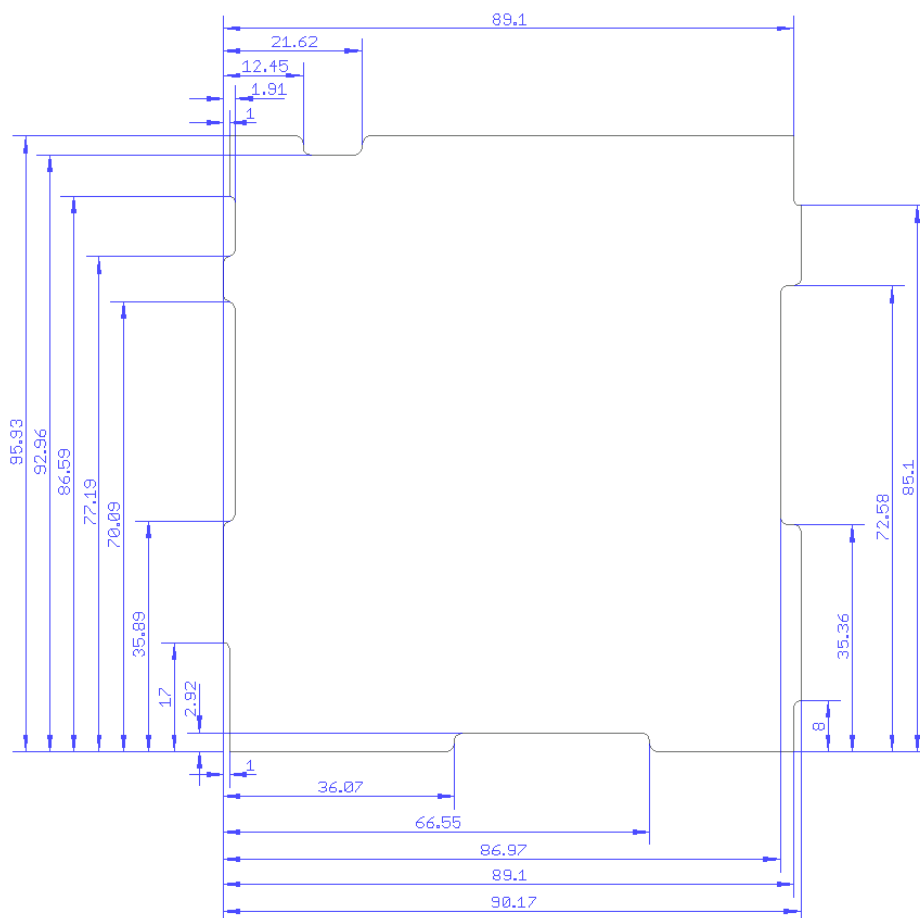
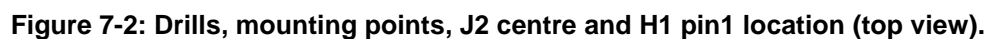


Figure 7-1: Motherboard outline (top view).





 Daughterboard mounting holes
 Motherboard mounting holes

Figure 7-3: Drill sizes.

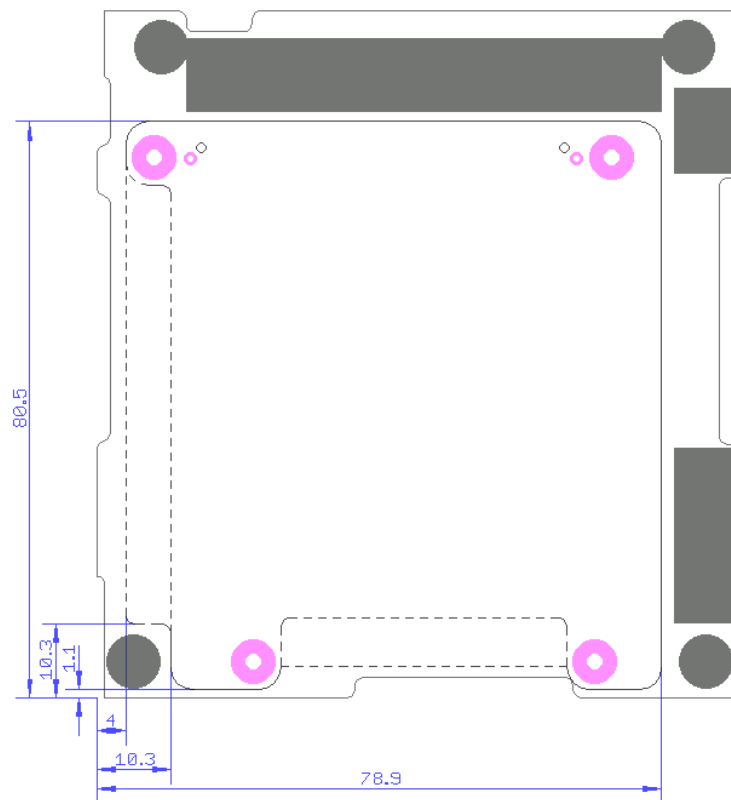


Figure 7-4: Recommended daughterboard outline [mm] (top view).

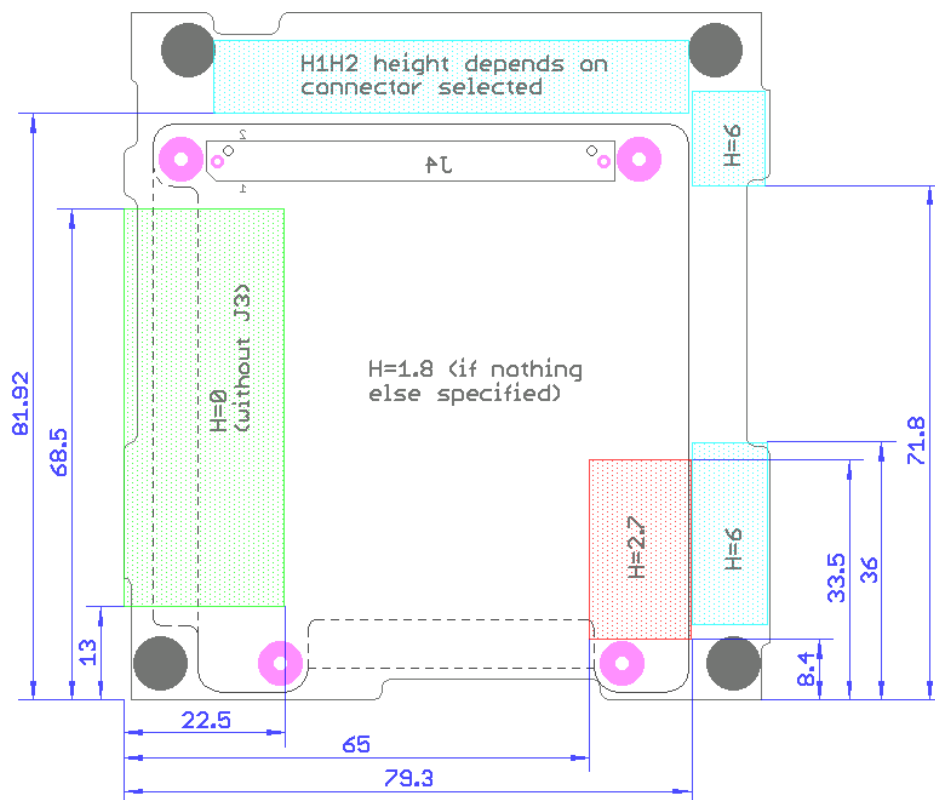


Figure 7-5: Height of components on motherboard [mm] (top view).

8 Storage and Handling Information

8.1 Handling



Note that the iOBC is sensitive to Electro Static Discharge (ESD).

8.1.1 Electrostatic discharge ESD

CAUTION



The printed circuit board can be damaged by electrostatic discharge. Do not touch any of the boards unless it is absolutely necessary. If you must handle them, wear a grounded wrist strap and take other antistatic precautions. Wear a grounded wrist strap any time you must handle the board.

8.1.2 Exposed Voltages

WARNING



Handling the board with an active power supply connection is not recommended. The board itself could be damaged and there is a possibility of electric shock hazard

In the event of Emergency, disconnect the power supply and proceed, if required, with first aid activities.

8.1.3 Current Limit protection

CAUTION



Ensure that over-current protection to a level of 1A or less is present when connecting to external power supplies.

8.1.4 Operation Conditions

CAUTION



Limit the number of connector mating cycles to less than 50 (about 10 cycles are used during functional testing)

CAUTION

The IOBC is supplied with final functional test results. Operating it outside its prescribed operating conditions may impede functionality.

Ensure that the system is always operated within its qualification temperature range.

CAUTION

This system does not have a protective housing and is therefore not intended for outdoor use as the board electronics might be damaged.

8.2 Storage

CAUTION

Store the IOBC inside a sealed ESD bag and in an environment controlled area.

The absolute maximum ratings for storage temperature are from -40 to +80°C with a Relative Humidity <60%

8.3 Disposal

WARNING

This product contains materials that can be harmful for the Environment and as such it should not be disposed of with conventional waste but treated according to WEEE regulations (UE Directives 2002/96/EC and further amendments) and brought to an appropriate recycling facility.