1. Description

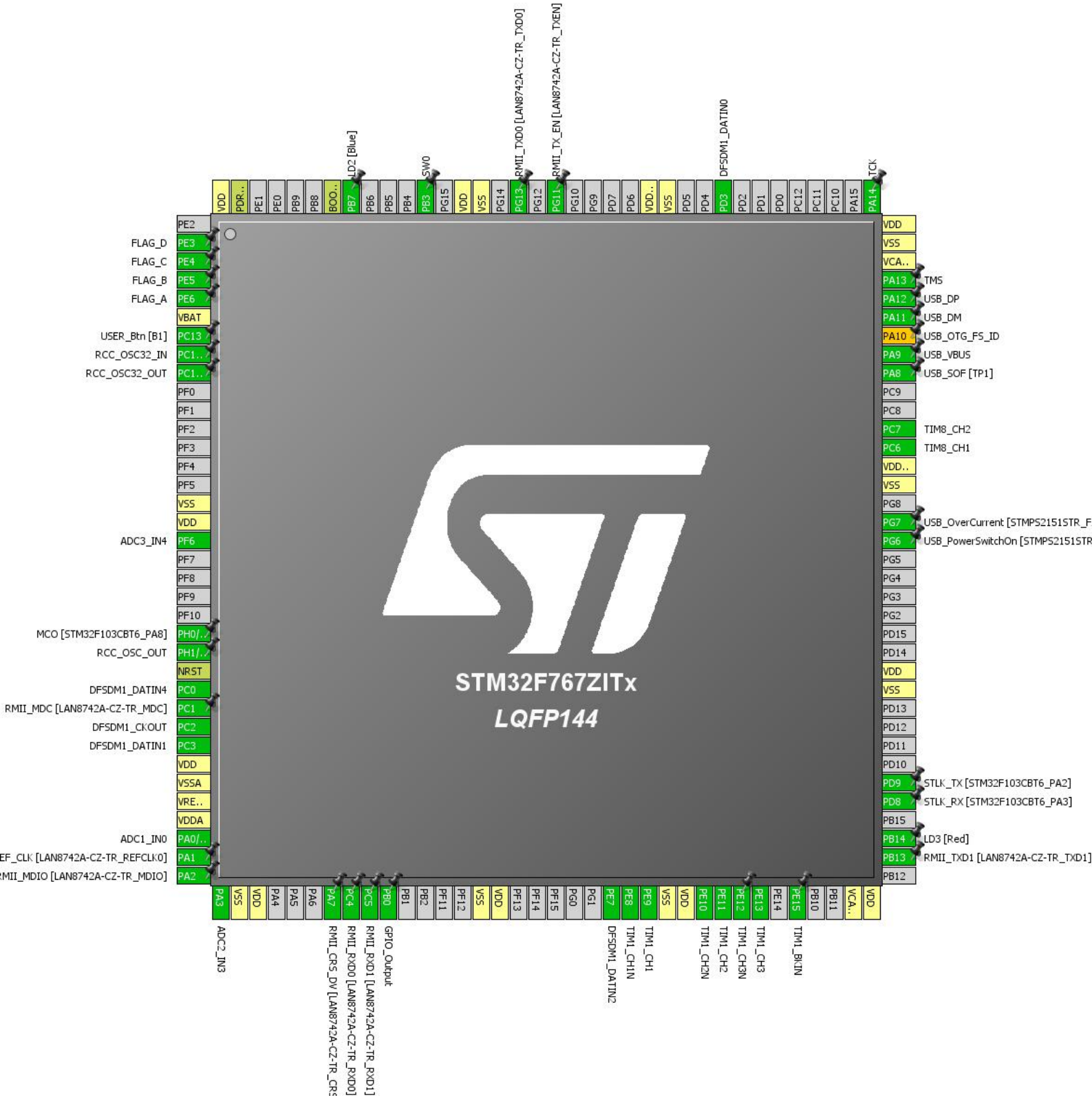
1.1. Project

Project Name	STM32F7T1
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 4.21.0
Date	07/30/2017

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3 *	I/O	GPIO_Output	FLAG_D
3	PE4 *	I/O	GPIO_Output	FLAG_C
4	PE5 *	I/O	GPIO_Output	FLAG_B
5	PE6 *	I/O	GPIO_Output	FLAG_A
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	ADC3_IN4	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	DFSDM1_DATIN4	
27	PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ-TR_MDC]
28	PC2	I/O	DFSDM1_CKOUT	
29	PC3	I/O	DFSDM1_DATIN1	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	ADC1_IN0	
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
36	PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
37	PA3	I/O	ADC2_IN3	
38	VSS	Power		
39	VDD	Power		
43	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
44	PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]

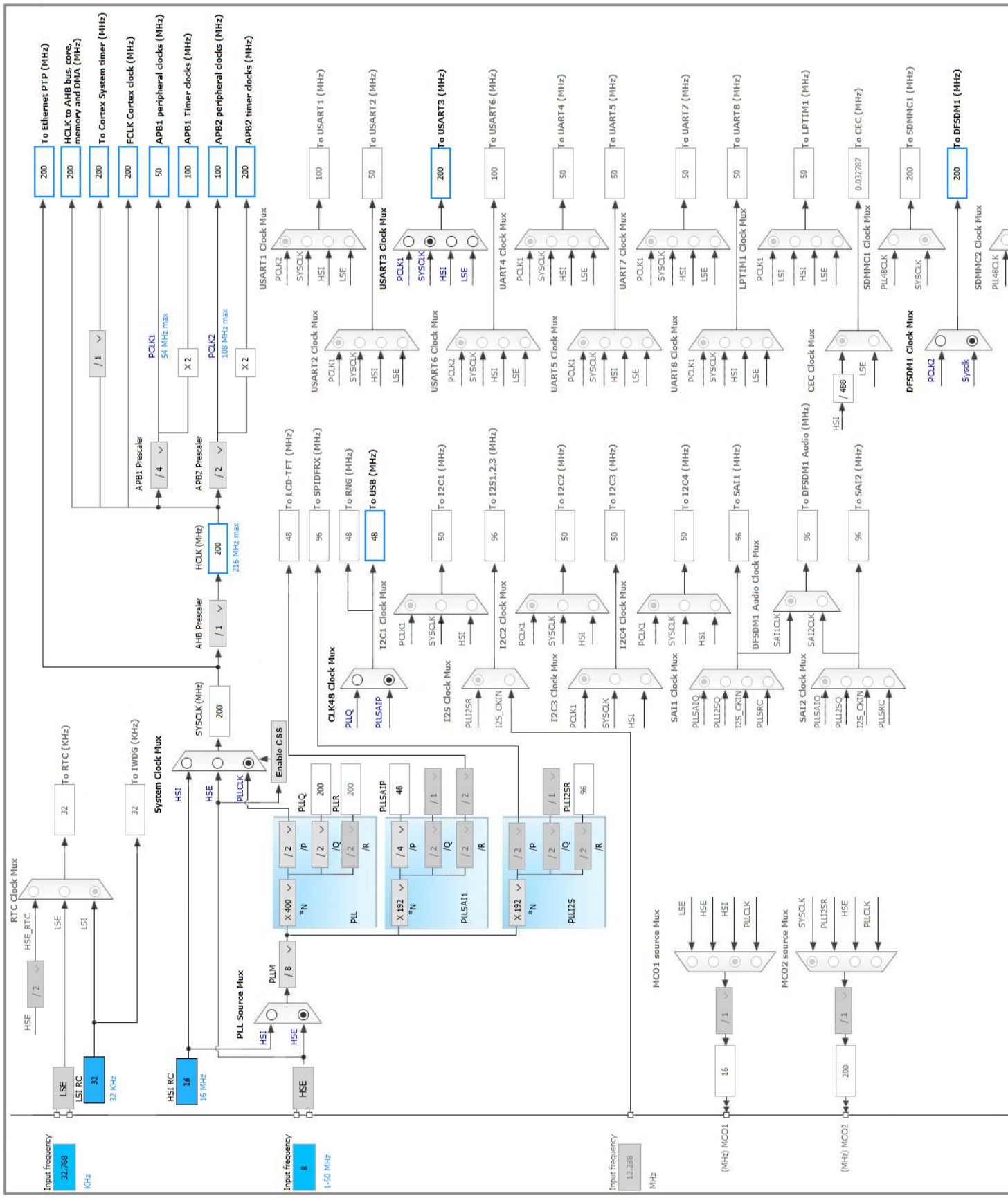
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
45	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
46	PB0 *	I/O	GPIO_Output	
51	VSS	Power		
52	VDD	Power		
58	PE7	I/O	DFSDM1_DATIN2	
59	PE8	I/O	TIM1_CH1N	
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	TIM1_CH2N	
64	PE11	I/O	TIM1_CH2	
65	PE12	I/O	TIM1_CH3N	
66	PE13	I/O	TIM1_CH3	
68	PE15	I/O	TIM1_BKIN	
71	VCAP_1	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
83	VSS	Power		
84	VDD	Power		
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM8_CH1	
97	PC7	I/O	TIM8_CH2	
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 **	I/O	USB_OTG_FS_ID	
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
117	PD3	I/O	DFSDM1_DATIN0	
120	VSS	Power		
121	VDDSDMMC	Power		
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
128	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SYS_JTDO-SWO	SW0
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN3

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN4

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. DFSDM1

mode: PDM/SPI input from ch0 and internal clock
mode: PDM/SPI input from ch1 and internal clock
mode: PDM/SPI input from ch2 and internal clock
mode: PDM/SPI input from ch4 and internal clock
mode: CKOUT

5.4.1. Filter 0:

regular channel selection:

regular channel selection	**Channel 0 ***
Continuous Mode	Continuous Mode
Trigger to start regular conversion	Software trigger
Fast Mode	**Enable ***
Dma Mode	Disable

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

Filter parameters:

Sinc Order	**Sinc 3 filter type ***
Fosr	**32 ***

Iosr	1

5.4.2. Filter 1:

regular channel selection:

regular channel selection	**Channel 1 ***
Continuous Mode	Continuous Mode
Trigger to start regular conversion	Software trigger
Fast Mode	**Enable ***
Dma Mode	Disable

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

Filter parameters:

Sinc Order	**Sinc 3 filter type ***
Fosr	**32 ***
Iosr	1

5.4.3. Filter 2:

regular channel selection:

regular channel selection	**Channel 2 ***
Continuous Mode	Continuous Mode
Trigger to start regular conversion	Software trigger
Fast Mode	**Enable ***
Dma Mode	Disable

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable

Channel7 as injected channel	Disable

Filter parameters:

Sinc Order	**Sinc 3 filter type ***
Fosr	**32 ***
Iosr	1

5.4.4. Filter 3:

regular channel selection:

regular channel selection	**Channel 4 ***
Continuous Mode	Continuous Mode
Trigger to start regular conversion	Software trigger
Fast Mode	**Enable ***
Dma Mode	Disable

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

Filter parameters:

Sinc Order	**Sinc 3 filter type ***
Fosr	**32 ***
Iosr	1

5.4.5. Output Clock:

Output Clock parameters:

Selection	Source for ouput clock is system clock
Divider	**256 ***

5.4.6. Channel 0:

Channel 0 parameters:

Type	SPI with rising edge
Spi Clock	Internal SPI clock

Offset	0
Right Bit Shift	**0x00 ***

Analog watchdog parameters:

Filter Order	**Sinc 3 filter type ***
Oversampling	**32 ***

5.4.7. Channel 1:

Analog watchdog parameters:

Filter Order	**Sinc 3 filter type ***
Oversampling	**32 ***

Channel 1 parameters:

Type	SPI with rising edge
Spi Clock	Internal SPI clock
Offset	0
Right Bit Shift	**0x00 ***

5.4.8. Channel 2:

Analog watchdog parameters:

Filter Order	**Sinc 3 filter type ***
Oversampling	**32 ***

Channel 2 parameters:

Type	SPI with rising edge
Spi Clock	Internal SPI clock
Offset	0
Right Bit Shift	**0x00 ***

5.4.9. Channel 4:

Analog watchdog parameters:

Filter Order	**Sinc 3 filter type ***
Oversampling	**32 ***

Channel 4 parameters:

Type	SPI with rising edge
Spi Clock	Internal SPI clock
Offset	0
Right Bit Shift	

	0x00 *

5.5. ETH

Mode: RMII

5.5.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

5.5.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***

Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x10 ***
PHY Speed mask	**0x0002 ***
PHY Duplex mask	**0x0004 ***
PHY Interrupt Source Flag register Offset	**0x000B ***
PHY Link down inturrupt	**0x000B ***

5.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.7. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM6

5.8. TIM1

Clock Source : Internal Clock
Channel1: PWM Generation CH1 CH1N
Channel2: PWM Generation CH2 CH2N
Channel3: PWM Generation CH3 CH3N
Channel4: Output Compare No Output
mode: Activate-Break-Input

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 16 bits value)	**4999 ***
Internal Clock Division (CKD)	**Division by 4 ***
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	**Enable (sync between this TIM (Master) and its Slaves (through TRGO)) ***
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	**Output Compare (OC6REF) ***

Break And Dead Time management - BRK Configuration:

BRK State	**Disable ***
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	**Disable ***
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	**Enable ***
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	**50 ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	**30 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	**13 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	**18 ***
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare No Output Channel 4:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	**400 ***
CH Polarity	High
CH Idle State	Reset

5.9. TIM3

Slave Mode: External Clock Mode 1
Trigger Source: ITR0

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**3 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	**Update Event ***

5.10. TIM7

mode: Activated

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**19 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.11. TIM8

Clock Source : Internal Clock
Channel1: Output Compare CH1
Channel2: Output Compare CH2

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 2:

Mode	Frozen (used for Timing base)

Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

5.12. USART3

Mode: Asynchronous

5.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.13. USB_OTG_FS

Mode: Device_Only

mode: Activate_SOF

mode: Activate_VBUS

5.13.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes

Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

5.14. FREERTOS

mode: Enabled

5.14.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled

USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	**6 ***

5.14.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

5.15. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

5.15.1. Parameter Settings:

Basic Parameters:

VirtualMode	Cdc
USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USBD_CDC_INTERVAL (Number of micro-frames interval)	1000

5.15.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
SERIALNUMBER_STRING (Serial number)	**22345112 ***
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA3	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PF6	ADC3_IN4	Analog mode	No pull-up and no pull-down	n/a	
DFSDM1	PC0	DFSDM1_DATIN4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC2	DFSDM1_CKOUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC3	DFSDM1_DATIN1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE7	DFSDM1_DATIN2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	DFSDM1_DATIN0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SW0
TIM1	PE8	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE12	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE15	TIM1_BKIN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD8	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	STLK_TX [STM32F103CBT6_PA2]
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	USB_VBUS
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP
Single Mapped Signals	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE3	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Medium ***	FLAG_D
	PE4	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Medium ***	FLAG_C
	PE5	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Medium ***	FLAG_B
	PE6	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Medium ***	FLAG_A

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	**n/a**	USER_Btn [B1]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM1 update interrupt and TIM10 global interrupt	true	6	0
TIM1 capture compare interrupt	true	6	0
TIM3 global interrupt	true	6	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
USB On The Go FS global interrupt	true	6	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
USART3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM7 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		
DFSDM1 filter0 global interrupt	unused		
DFSDM1 filter1 global interrupt	unused		
DFSDM1 filter2 global interrupt	unused		
DFSDM1 filter3 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev3

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STM32F7T1
Project Folder	E:\STM32\workspace_f4\STM32F7T1
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.7.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No