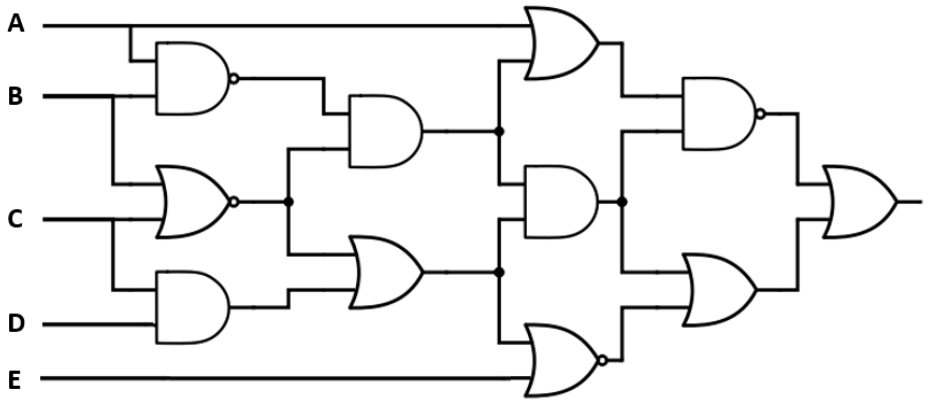
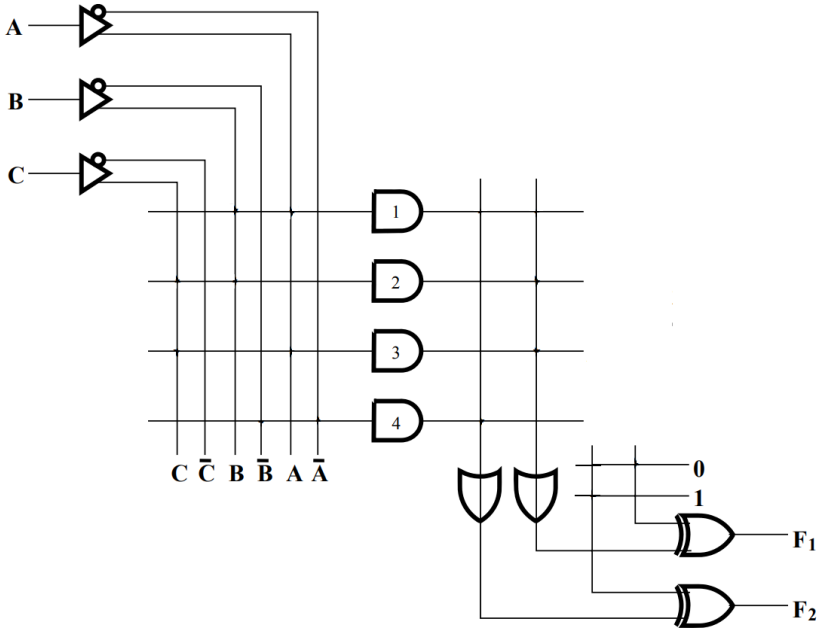
1077710 CS 516000 FPGA Architecture & CAD

Homework 1(Due: 10/4/2018)

1. Please describe what ASIC is and what FPGA is. What are their advantages (at least 2 for each)?
2. What is the advantage of making a large FPGA by interconnecting smaller FPGA chips using an interposer (2.5D FPGAs)? What is the difference if we use smaller silicon bridge between adjacent FPGAs instead of a big interposer connecting all FPGAs?
3. Consider the following circuit, what is the minimum number of 4-input LUTs needed to implement the circuit? How? Please draw it.



4. A student claimed that the two XOR gates in following PLA design could be removed to reduce area and delay with nothing to lose. Is he correct? Why?



5. Consider the MUX-based logic cell below. Prove that if the AND gate and OR gate are removed, the set of functions that can be implemented will become a proper subset of what it is now.