

Commercial Examples (Part 2) Microsemi(Actel) Antifuse- based & Flash-based FPGAs

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Topics

- Antifuse-based FPGA
 - Actel SX-A and Axcelerator (AX) families
- Flash-based FPGA
 - Actel ProASIC3 and IGLOO families

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Actel SX-A and AX Overview

- Antifuse-based FPGA
- Metal-to-metal programmable antifuses
- Mux-based logic elements

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SX-A Logic Element

- Mix two types of logic modules
 - Combinatorial cell (C-cell)
 - can implement more than 4000 different functions of ≤ 5 inputs.
 - Register cell (R-cell)
 - contains a flip-flop.

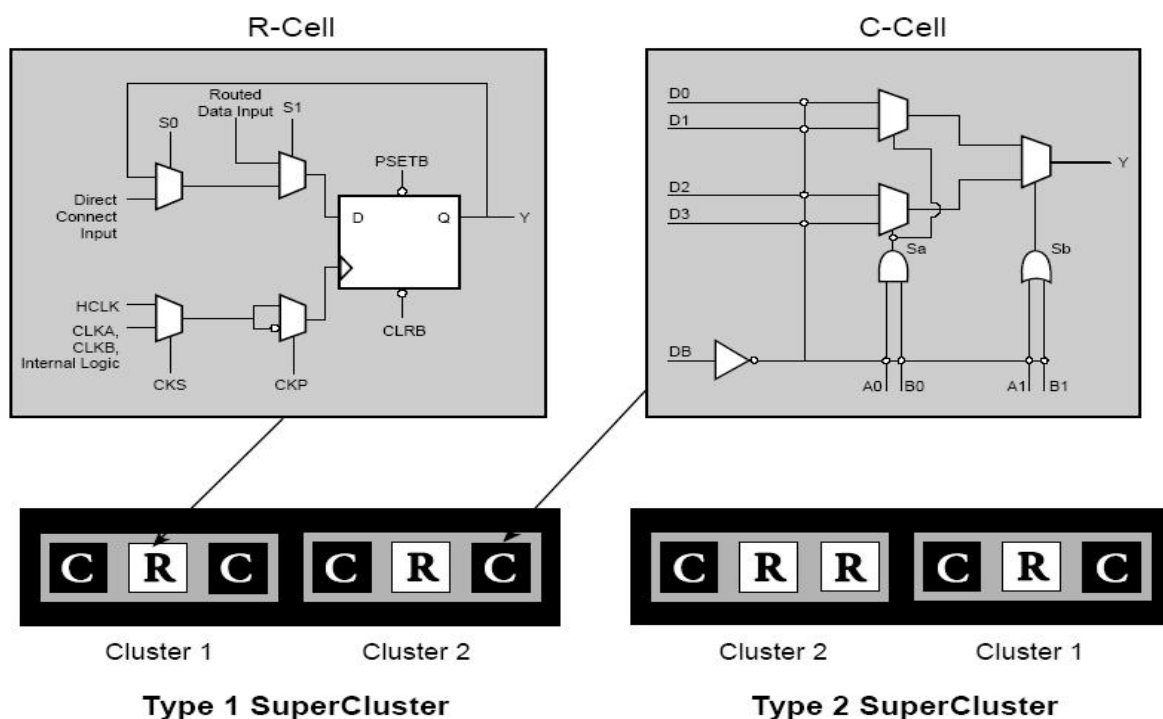
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Clusters and Superclusters (1/2)

- C/R cells organized into clusters.
 - Type 1 cluster: CRC.
 - Type 2 cluster: CRR.
- Clusters grouped into superclusters.
 - Type 1: two type 1 clusters.
 - Type 2: one type 1, one type 2.
 - Majority is Type 1 superclusters

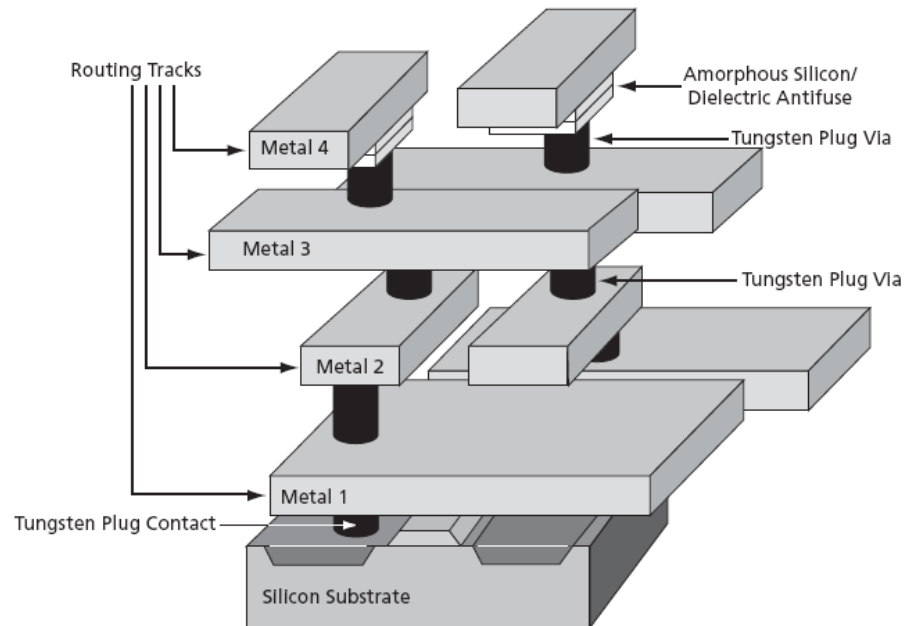
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Clusters and Superclusters (2/2)



SX-A Routing

- Programmable antifuses between the top two metal layers



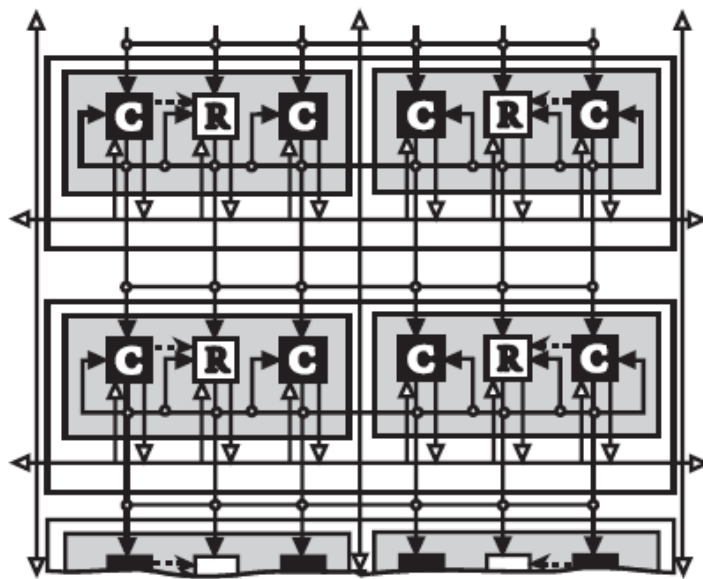
Source: Actel Corp.

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Routing Architecture (1/2)

- Local routing resources
 - DirectConnect is within a supercluster
 - connects C-cell to R-cell neighbor.
 - FastConnect provides horizontal connections between logic modules
 - within a supercluster.
 - to the supercluster below.
- Generic global wiring in segmented channels.

Routing Architecture (2/2)



- ➔ DirectConnect
 - No Antifuses
 - 0.1 ns Maximum Routing Delay
- ➔ FastConnect
 - One Antifuse
 - 0.3 ns Maximum Routing Delay
- ➔ Routing Segments
 - Typically Two Antifuses
 - Max. Five Antifuses

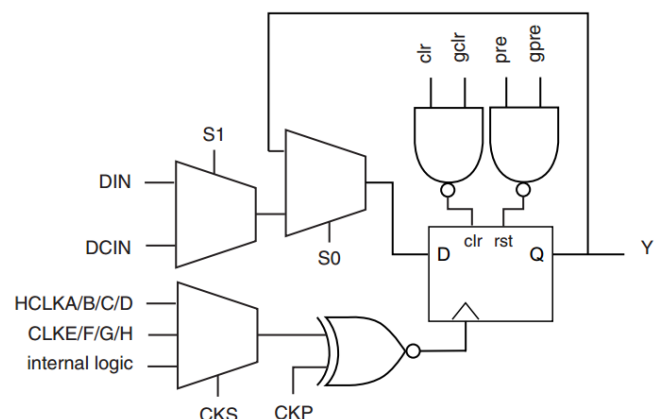
Source: Actel Corp.

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Axcelerator (AX) Family

■ Successor of SX-A

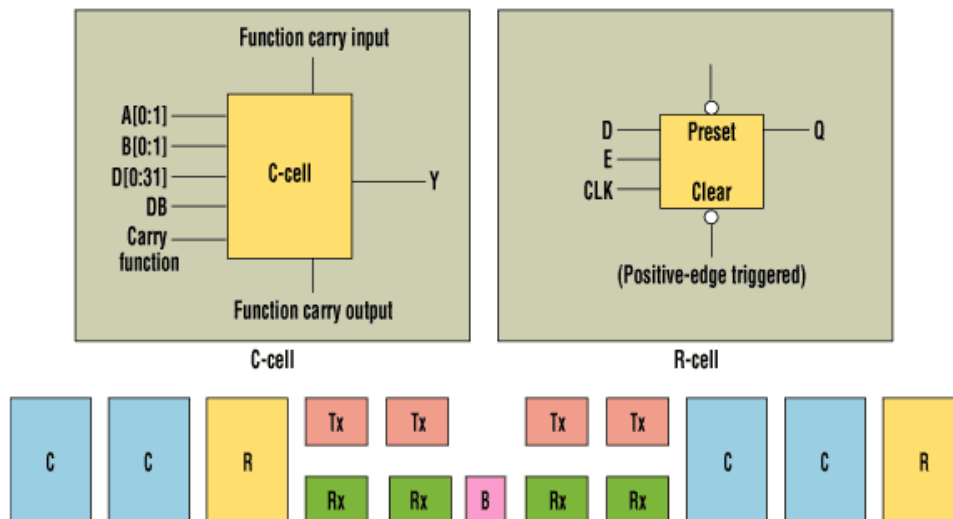
- Higher capacity, 7 metal layers, 8 I/O banks, embedded SRAM
- Enhance C-cell with addition of carry-chain logic
- Modified R-cell



- Use pattern CCR in all clusters

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SuperCluster in AX Architecture

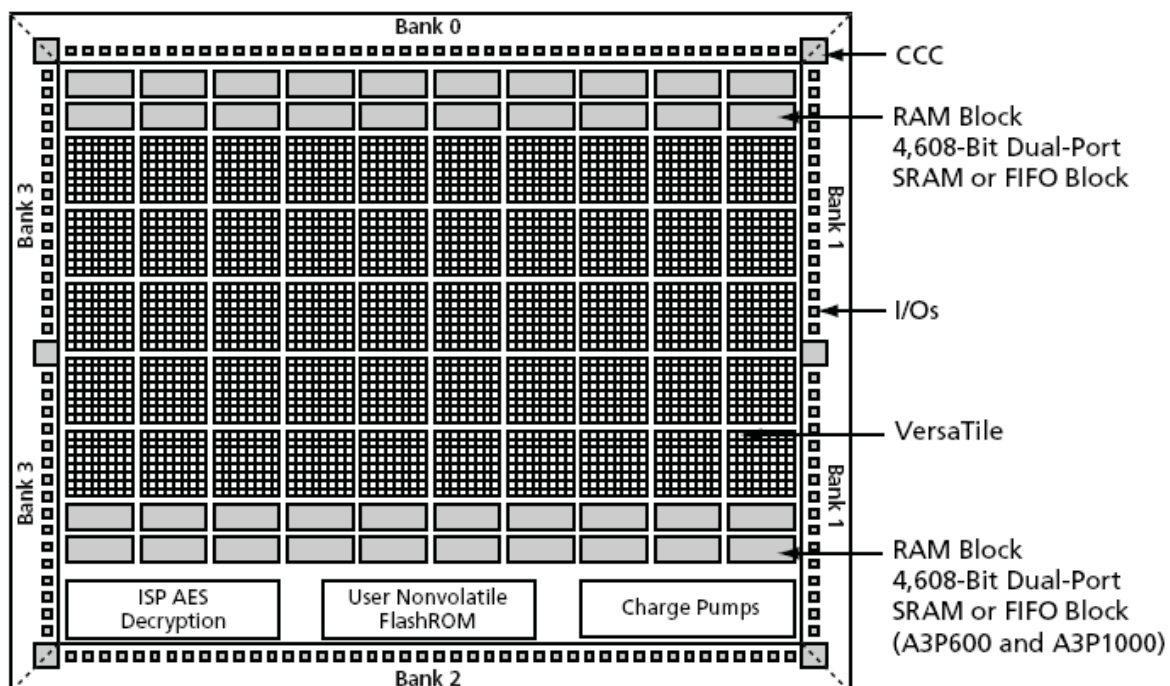


- Cluster = CCR + 2 transmit buffers + 2 receive buffers
- SuperCluster = 2 clusters + an additional buffer

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ProASIC3 and IGLOO Overview

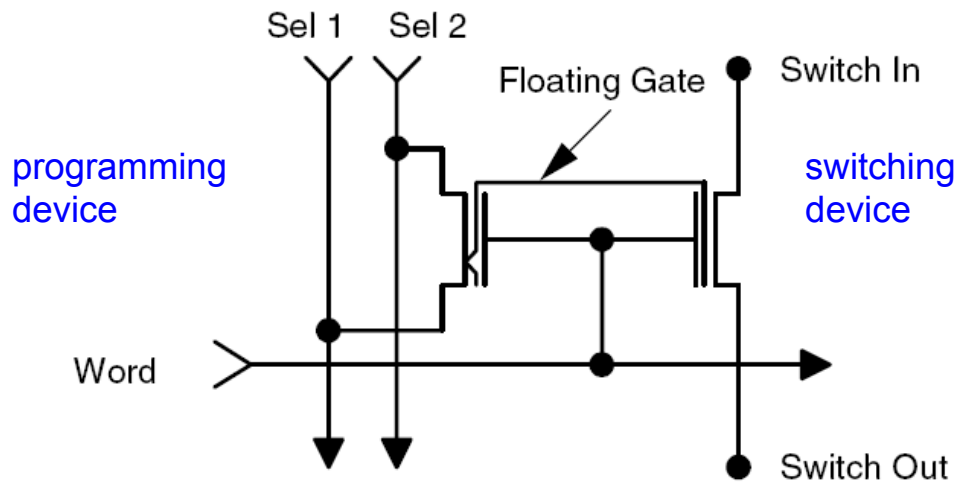
Flash-based FPGAs



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Flash-based Switch

- Each switch has two transistors sharing the floating gate.
- One transistor as programming device and the other as switching device.

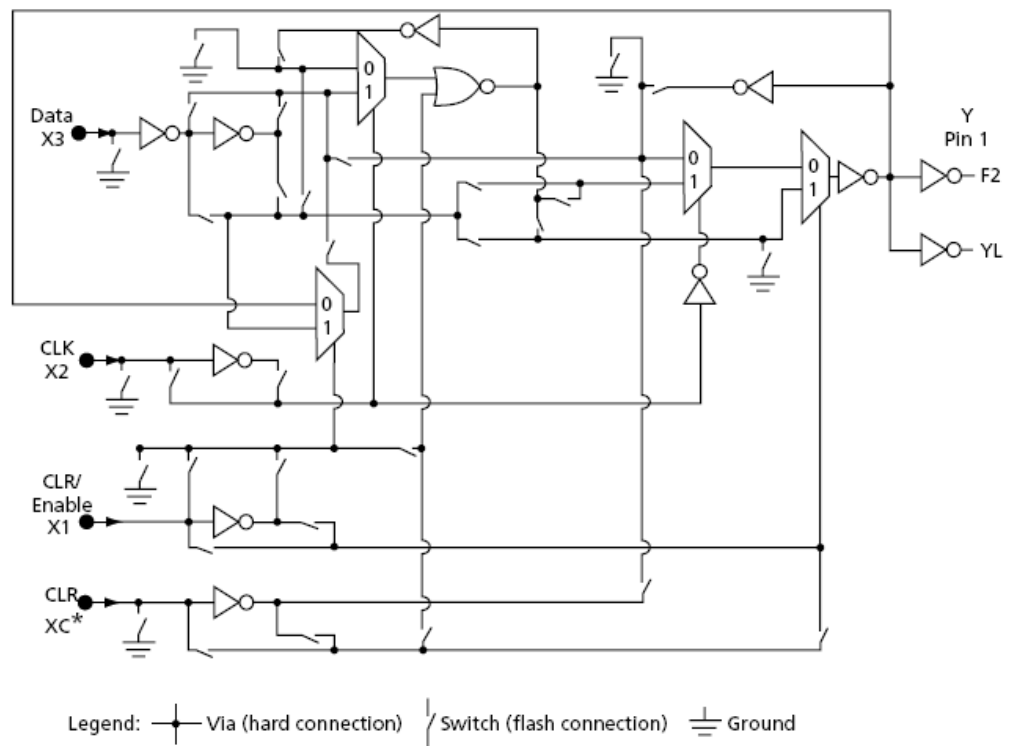


Source: Actel Corp.

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Logic Cell (1/2)

- Logic element is a 4-input cell



* This input can only be connected to the global clock distribution network.

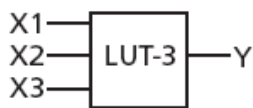
Source: Actel Corp.

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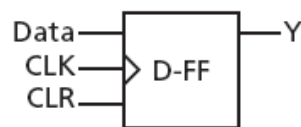
Logic Cell (2/2)

- Each logic cell can be configured as
 - any 3-input function
 - latch
 - D-flip-flop with or without enable

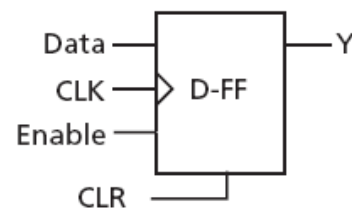
LUT-3 Equivalent



D-Flip-Flop with Clear or Set



Enable D-Flip-Flop with Clear or Set



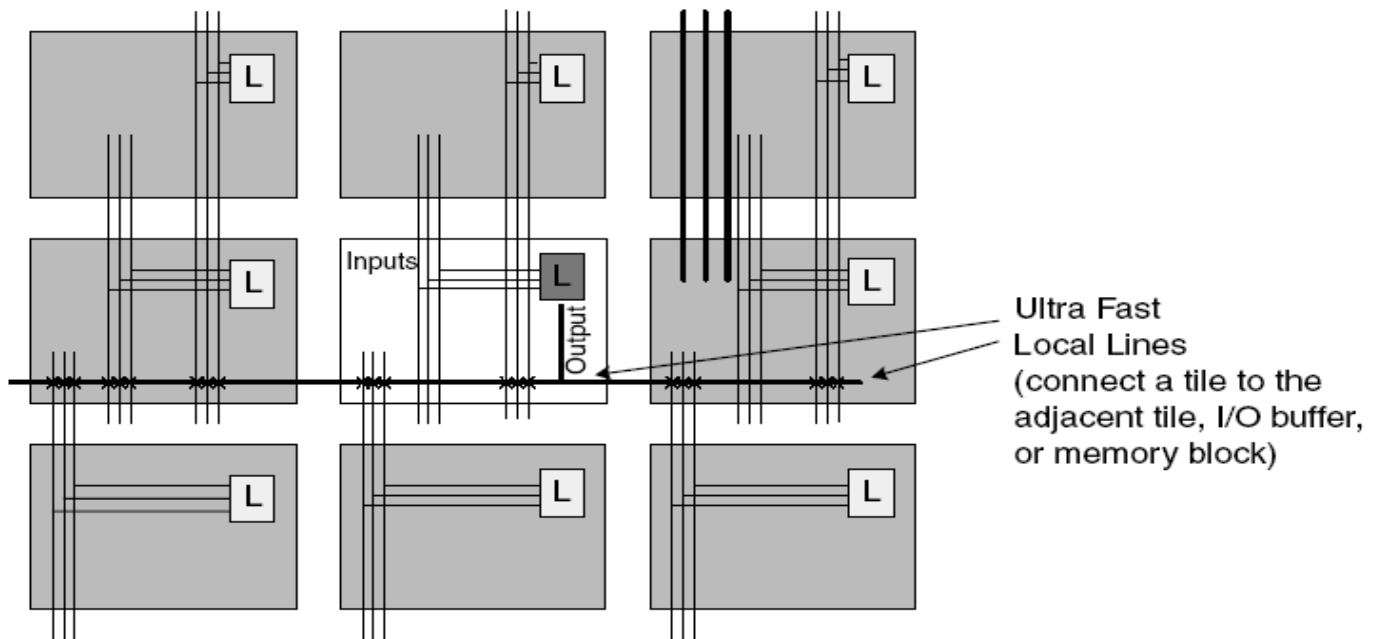
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Routing Architecture

- Fast local lines
 - from a tile to eight surrounding tiles
- Long lines
 - span 1/2/4 tiles vertically or horizontally
- Very long lines
 - span the entire device vertically or horizontally
- Global network
 - global trees
 - for clock and other very high fanout nets

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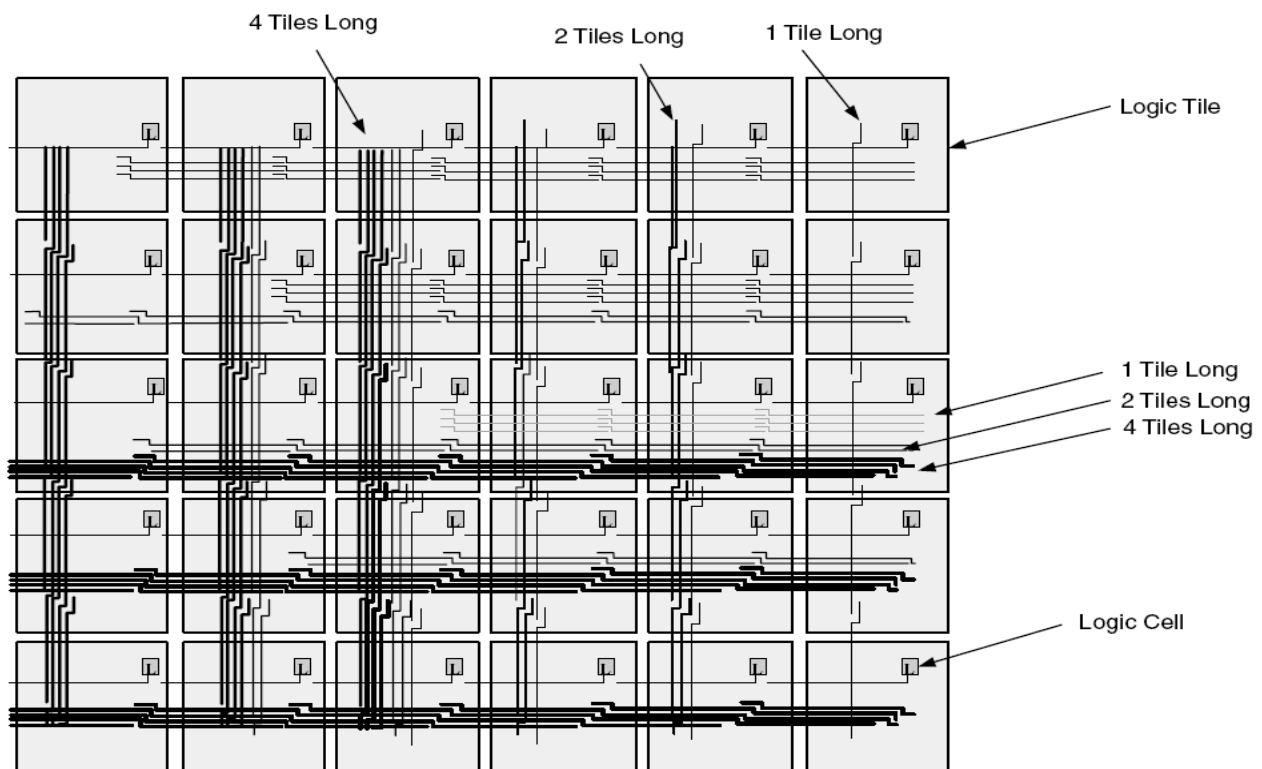
Routing Architecture: Fast Local Lines



Source: Actel Corp.

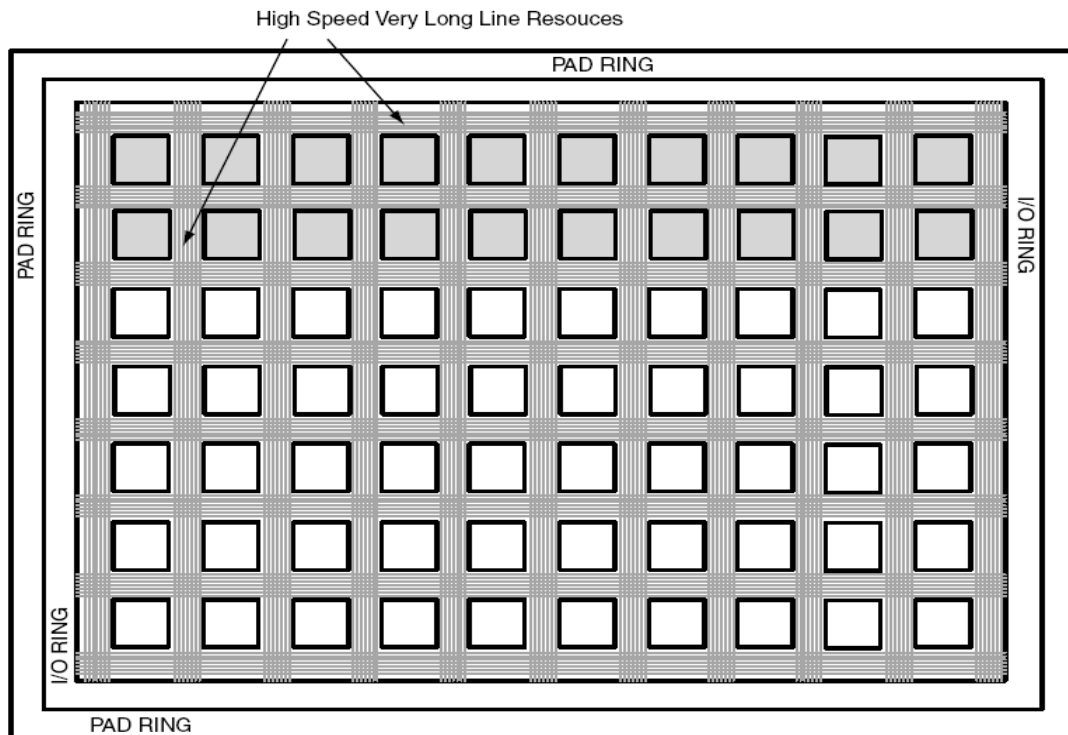
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Routing Architecture: Long Lines



Source: Actel Corp.²⁰

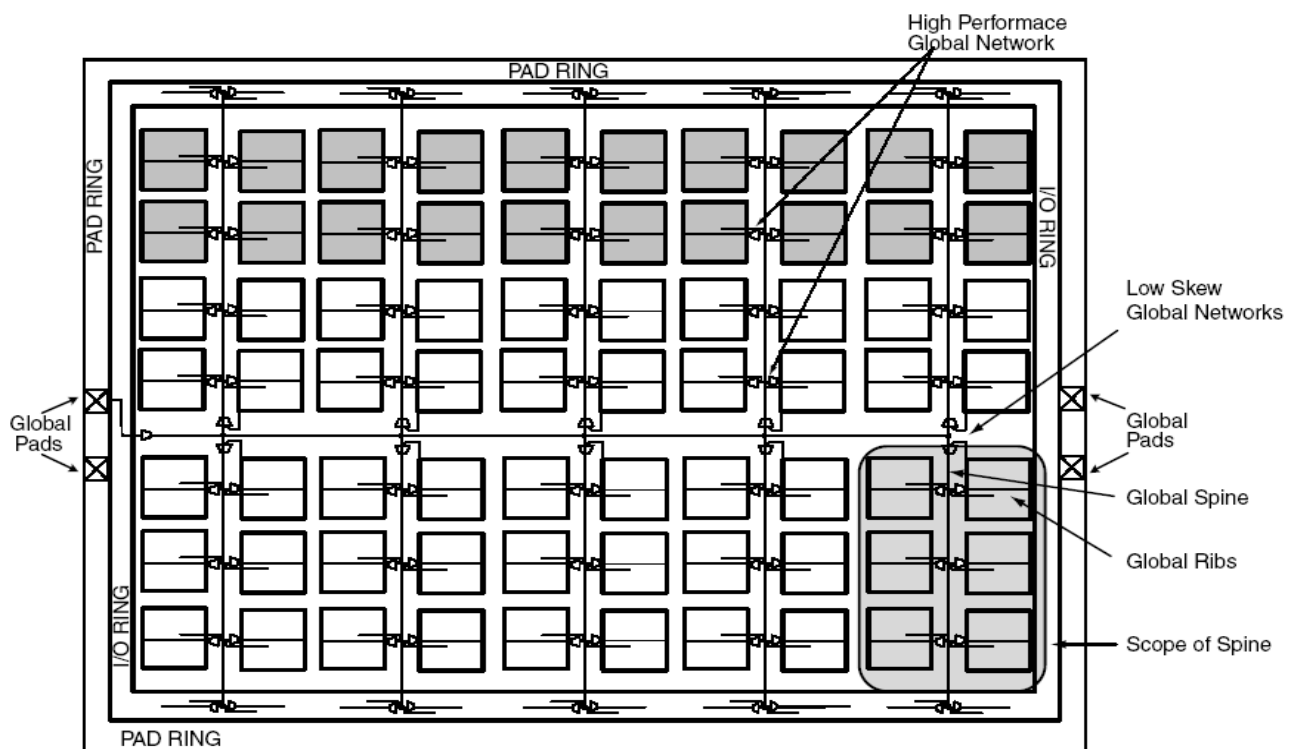
Routing Architecture: Very Long Lines



Source: Actel Corp.

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Routing Architecture: Global Network



Source: Actel Corp.

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Appendix: Security

