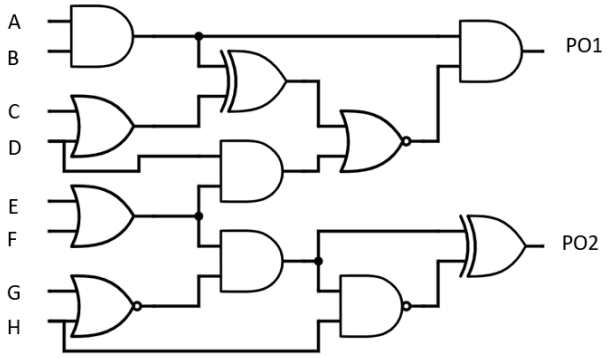
1077710 CS 516000 FPGA Architecture & CAD

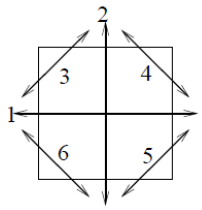
Homework 2(Due: 10/22/2018)

1. Refer to the hybrid design of a 16-to-1 MUX shown on p.13 of Unit 8.
   (a) Consider an alternative hybrid design where the first level is made up of four 4-to-1 encoded MUXes and the second level is made up of one 4-to-1 decoded MUX. Draw the alternative design and compute the total number of transistors it requires including those in the configuration SRAMs and level-restoring buffer.
   (b) How does the alternative hybrid design compare with the original hybrid design in terms of transistor count and delay?
2. Consider technology mapping of the circuit below (assume no node duplication and no further logic optimization is performed).
   (a) For a FPGA made up of 6-LUTs, how many 6-LUTs are required to map the circuit?
   (b) For a FPGA made up of Adaptive Logic Modules (ALMs) (p.21 of Unit 8), how many ALMs are required to map the circuit?

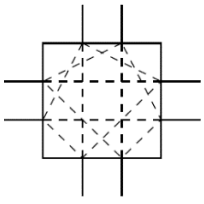


3. Assume there are six types of connections through a switch box as shown in figure (I).

(I)



(II)



Let n*i* denote the number of type-*i* connections we want to make and we call (n1, n2, n3, n4, n5, n6) a routing requirement vector.
(a) Argue that the routing requirement vector (2,0,1,0,0,0) is not routable for any switch box with exactly two wire segments on each of its four sides.
(b) Hence, write down four inequalities in terms of n1, n2, n3, n4, n5, n6, and W that represent the necessary condition for a routing requirement vector (n1, n2, n3, n4, n5, n6) to be routable for a switch box with W wire segments on each of its four sides.

(c) Give a specific routing requirement vector that satisfies the necessary condition in (b) but is still not routable for the switch box design shown in figure (II) (there are two wire segments on each of its four sides and the dotted lines show the programmable connections between wire segments) .