

Lab 7 Digital

Ejercicio 1:

Link NO DISPONIBLE DEBIDO A ERRORES EN TINKERCAD: Adjunto el archivo exportado

The image displays two screenshots of digital logic design software. The top screenshot shows the Logic Friday interface with two truth tables and their corresponding minimized Boolean expressions and circuit diagrams.

Left Logic Friday Window:

Función	Inputs	Outputs	True	False	DC	PI	Gates
FSB1-F...	3	2	2,1	4,5	2,2	Unmini...	Not mapped
FSB1-F...	3	2	4,4	4,4	0,0	5	3

Entered by truth table:
 $FSB1 = SB1' \cdot SB0 \cdot BO + SB1 \cdot SB0' \cdot BO' + SB1 \cdot SB0' \cdot BO + SB1 \cdot SB0 \cdot BO'$
 $FSB0 = SB1' \cdot SB0' \cdot BO + SB1' \cdot SB0 \cdot BO' + SB1 \cdot SB0' \cdot BO + SB1 \cdot SB0 \cdot BO'$

Minimized:
 $FSB1 = SB1 \cdot SB0' + SB1 \cdot BO' + SB1' \cdot SB0 \cdot BO$
 $FSB0 = SB0 \cdot BO' + SB0' \cdot BO$

Right Logic Friday Window:

Función	Inputs	Outputs	True	False	DC	PI	Gates
L1-L3	2	3	1,2,3	3,2,1	0,0,0	3	2

Entered by truth table:
 $L1 = SB1 \cdot SB0$
 $L2 = SB1 \cdot SB0' + SB1 \cdot SB0$
 $L3 = SB1' \cdot SB0 + SB1 \cdot SB0' + SB1 \cdot SB0$

Minimized:
 $L1 = SB1 \cdot SB0$
 $L2 = SB1$
 $L3 = SB0 + SB1$

The bottom screenshot shows the Tinkercad interface with a breadboard circuit simulation. The circuit implements the logic from the Logic Friday windows using logic gates. A multimeter is connected to the output of the circuit, showing a reading of 125.0 mA. The Tinkercad interface includes a component list, a code editor, and a simulation button.

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Ejercicio 2:

Link:

<https://www.tinkercad.com/things/3094XZbNIUU-ejercicio1lab7digi2/editel?sharecode=HfgNa3su2jOUDsICo2XqX2YxEvYwKpb8k2P0f4d64wA>

The image displays two windows from the Tinkercad environment. The top window is the Logic Friday logic editor, and the bottom window is the Tinkercad breadboard simulator.

Logic Friday Window:

- Left Panel:** Shows a truth table for functions FSB1-M2 and FSB1-F... with inputs SB1, SB0, CCW, and CW. The minimized logic equations are:
$$FSB1 = SB0' \cdot CCW \cdot CW' + SB1;$$
$$FSB0 = SB1' \cdot CCW' \cdot CW + SB0;$$
- Right Panel:** Shows a truth table for functions F0 and F1 with inputs A and B. The entered logic equations are:
$$F0 = A \cdot B';$$
$$F1 = A' \cdot B;$$

Tinkercad Window:

- Shows a breadboard circuit with two integrated circuits (ICs) connected to a power supply and ground.
- A right-hand panel titled "Lógica" (Logic) lists various logic components available for use, including:
 - 74HC00: Puerta NAND cuádruple
 - 74HC132: Desencadenador NAND Schmitt...
 - 74HC11: Puerta triple AND
 - 74HC08: Puerta AND cuádruple
 - 74HC10: Puerta triple NAND de 3...
 - 74HC20: Puerta doble

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Ejercicio 3

Link: <https://www.tinkercad.com/things/2M1lber4iLm-lab7digi1ej3/editel?sharecode=s-BoPPRy5KM3y-owHBsim5IyeVv6CTJXvjNXQ39T8dO>

Logic Friday

File Operation TruthTable Equation Gates View Help

Función	Inputs	Outputs	True	False	DC	PI	Gates
FSB1-Y2	4	4	8, 8, ...	8, 8, ...	0, 0, ...	4	Not mapped

Entered by truthtable:

$FSB1 = SBI' \cdot SBO' \cdot P1 \cdot P2' + SBI' \cdot SBO' \cdot P1 \cdot P2 + SBI' \cdot SBO \cdot P1 \cdot P2' + SBI' \cdot SBO \cdot P1 \cdot P2 + SBI \cdot SBO' \cdot P1 \cdot P2' + SBI \cdot SBO' \cdot P1 \cdot P2 + SBI \cdot SBO \cdot P1 \cdot P2' + SBI \cdot SBO \cdot P1 \cdot P2$

$FSBO = SBI' \cdot SBO' \cdot P1' \cdot P2 + SBI' \cdot SBO' \cdot P1 \cdot P2 + SBI' \cdot SBO \cdot P1' \cdot P2 + SBI' \cdot SBO \cdot P1 \cdot P2 + SBI \cdot SBO' \cdot P1' \cdot P2 + SBI \cdot SBO' \cdot P1 \cdot P2 + SBI \cdot SBO \cdot P1' \cdot P2 + SBI \cdot SBO \cdot P1 \cdot P2$

$Y1 = SBI' \cdot SBO' \cdot P1 \cdot P2' + SBI' \cdot SBO' \cdot P1 \cdot P2 + SBI' \cdot SBO \cdot P1 \cdot P2' + SBI' \cdot SBO \cdot P1 \cdot P2 + SBI \cdot SBO' \cdot P1 \cdot P2' + SBI \cdot SBO' \cdot P1 \cdot P2 + SBI \cdot SBO \cdot P1 \cdot P2' + SBI \cdot SBO \cdot P1 \cdot P2$

$Y2 = SBI' \cdot SBO' \cdot P1' \cdot P2 + SBI' \cdot SBO' \cdot P1 \cdot P2 + SBI' \cdot SBO \cdot P1' \cdot P2 + SBI' \cdot SBO \cdot P1 \cdot P2 + SBI \cdot SBO' \cdot P1' \cdot P2 + SBI \cdot SBO' \cdot P1 \cdot P2 + SBI \cdot SBO \cdot P1' \cdot P2 + SBI \cdot SBO \cdot P1 \cdot P2$

Minimized:

$FSB1 = P1$;
 $FSBO = P2$;
 $Y1 = P1$;
 $Y2 = P2$;

Ready

Escribe aquí para buscar

Reflexión entrega x Circuit design Eje x Circuit design Eje x Circuit design Lab x Circuit design Co x Recibidos (2.819) x limit of x to infity x G xor truth table - B x

tinkercad.com/things/2M1lber4iLm-lab7digi1ej3/editel

Lab7_Digi1_Ej3

Guardando...

Código ▶ Iniciar simulación Exportar Compartir

Componentes
Todos

and

Lógica

74HC00 74HC05
Puerta NAND cuádruple Puerta AND cuádruple
74HC132 74HC18
Desencadenador NAND Schmitt... Puerta triple NAND de 3...
74HC11 74HC20
Puerta triple AND Puerta doble

Mostrar todo

Ejercicio1_Lab7_Di...brd

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