AN5122
Application note

STM32MP1 Series DDR memory routing guidelines

Introduction

This application note gives guidance on how to implement a DDR3, DDR3L, LPDDR2, LPDDR3 memory interface on STM32MP1 Series application PCBs. It provides interface schematics, layout implementation rules and best practices.

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1 Design interface constraints

STM32MP1 Series are STM32 32-bit devices based on Arm®(a) Cortex® processors.

STM32MP1 Series memory interface can address different types of memory:

- DDR3 and DDR3L with a data rate speed at 1066 Mbps, voltage at 1.5 V for DDR3 and 1.35 V for DDR3L. More information on DDR3 SDRAM can be found on JEDEC DDR3 SDRAM Standard JESD79-3F.
- LPDDR2 and LPDDR3 with a data rate speed at 1066 Mbps, voltage at 1.2 V. More information on LPDDR2 and LPDDR3 can be found on JEDEC LPDDR2 Standard JESD209-2F and JEDEC LPDDR3 Standard JESD209-3C.

Low voltage and high data rate speed contribute to narrower tolerances in terms of read eye opening, and greater risk of system instability.

As a result, there are many constraints and design sensitivities to take into account when working with memory interfaces. For example:

Most signals are single-ended, only the clocks are differential signals.

Signals can be connected point-to-point or in fly-by topology.

There are challenges in designing a DDR interface owing to continuous board-size reductions, which can impose performance limitations on the interface.

In addition, because the DDR connections on both the STM32MP1 Series and memory device interface are fixed, there is very limited flexibility possible in terms of physical layout.

- There is a minimum amount of signal routing required cannot be reduced further.
- There are impedance constraints to be managed.

Basic design rules regarding trace isolation, length equalization, power distribution and decoupling and impedance matching, must be respected to ensure correct signal and power integrity.

This document lists the rules that must be applied in order to implement a state-of-the-art memory interface in 4-layer PCBs.

ST highly recommends to reuse the layout of the ST reference designs.

These layout have been tested and have been proven stable.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and or elsewhere.

2 Memory architecture options

Several options are possible linked to the package and the type of memory:

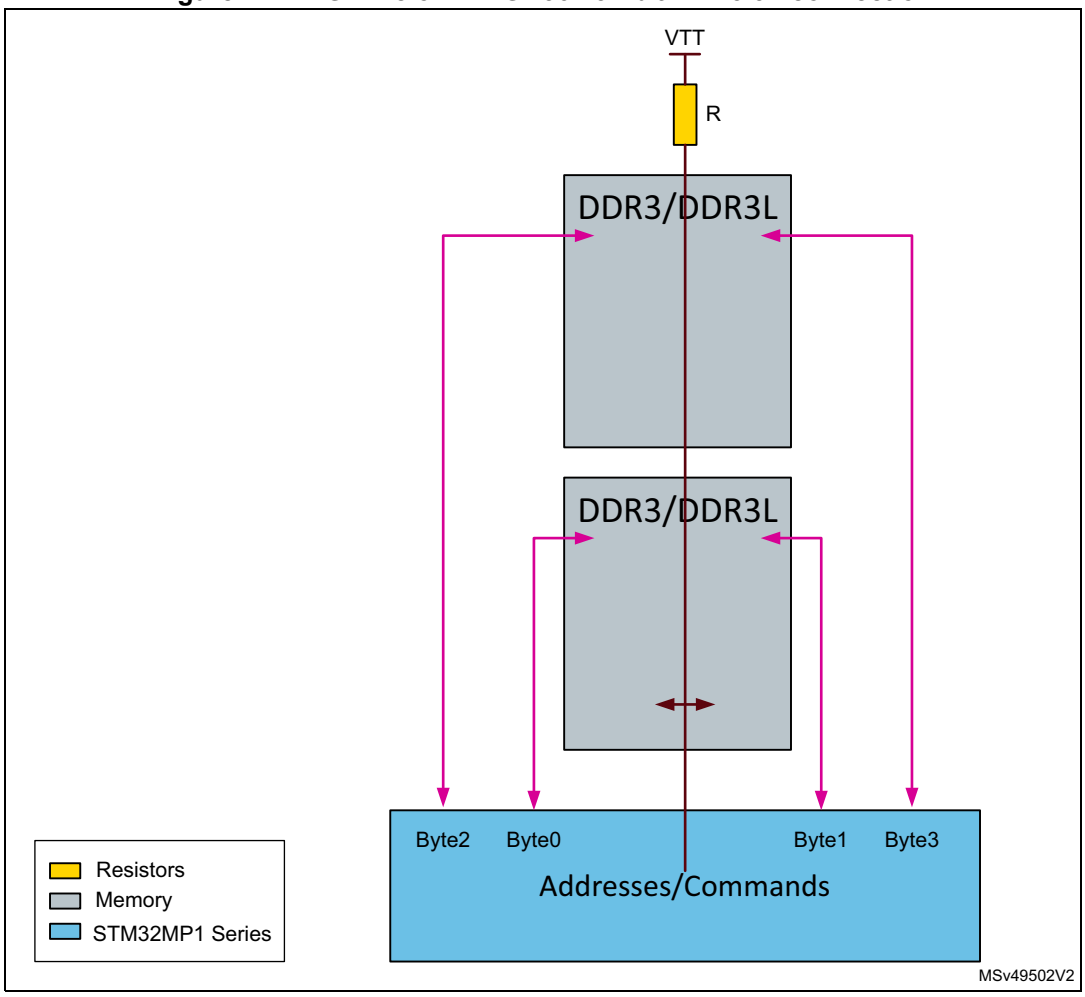
Table 1. Package summary of STM32MP1 Series

Package type	TFBGA257 (10 × 10 mm)	LFBGA354 (16 × 16 mm)	TFBGA361 (12 × 12 mm)	LFBGA448 (18 × 18 mm)
16/32-bit interface	-	-	X	X
16-bit interface	X	X	-	-

2.1 32-bit DDR3/DDR3L interface

For 32-bit DDR3 or DDR3L interface, two 16-bit DDR3/3L are used in fly-by topology.

Figure 1. LFBGA448 or TFBGA361 32-bit DDR3/3L connection



The advantage of this design is that it drives up to 1 GByte memory (2 *4 Gbits) but it does require a larger PCB footprint.

2.2 16-bit DDR3/DDR3L interface

For 16-bit DDR3 or DDR3L interface, one 16-bit DDR3/3L is used.

With this configuration it can drive up to 1 GByte memory (1 * 8 Gbits).

On 32-bit interface, only bytes 0 and 1 are used, let bytes 2 and 3 not connected.

Figure 2. LFBGA448 or TFBGA361 16-bit DDR3/3L connection

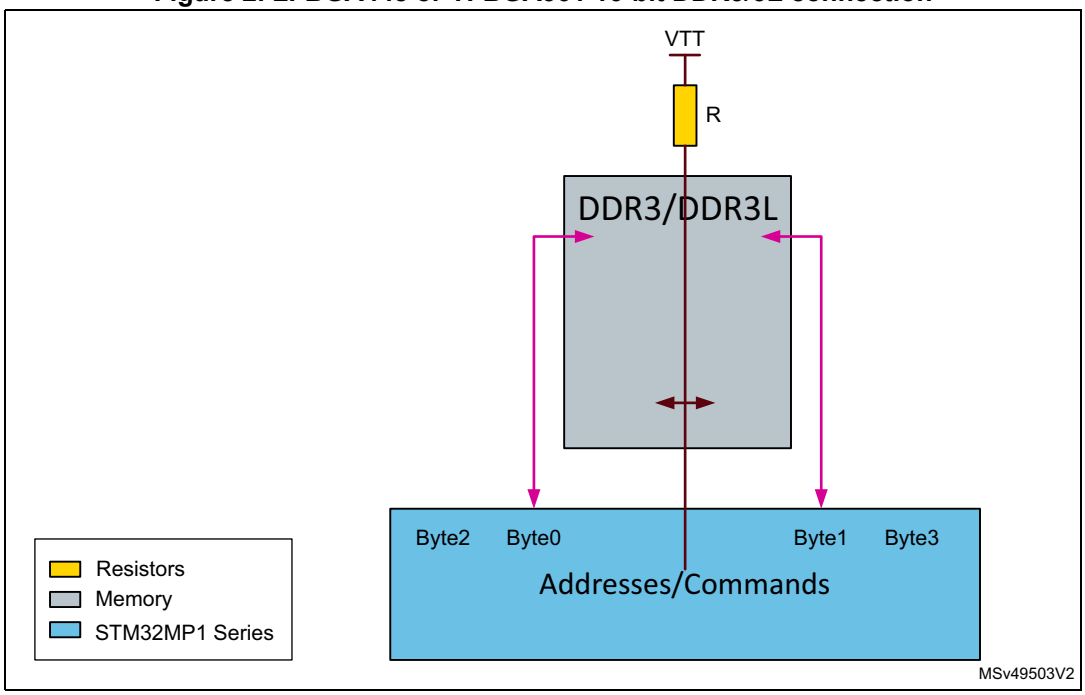
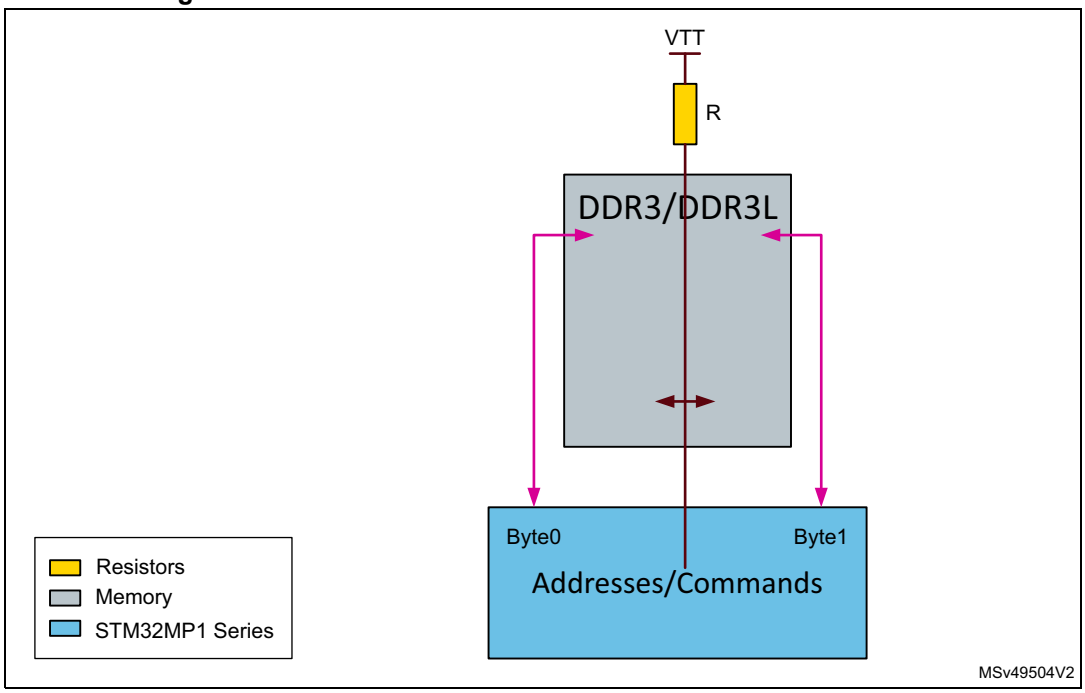


Figure 3. LFBGA354 or TFBGA257 16-bit DDR3/3L connection



Other possibility to connect one DDR3/3L if termination resistors are not used, connect serial resistor on each address and command lines close to STM32MP1 Series.

Figure 4. LFBGA448 or TFBGA361 16-bit DDR3/3L connection with serial resistors

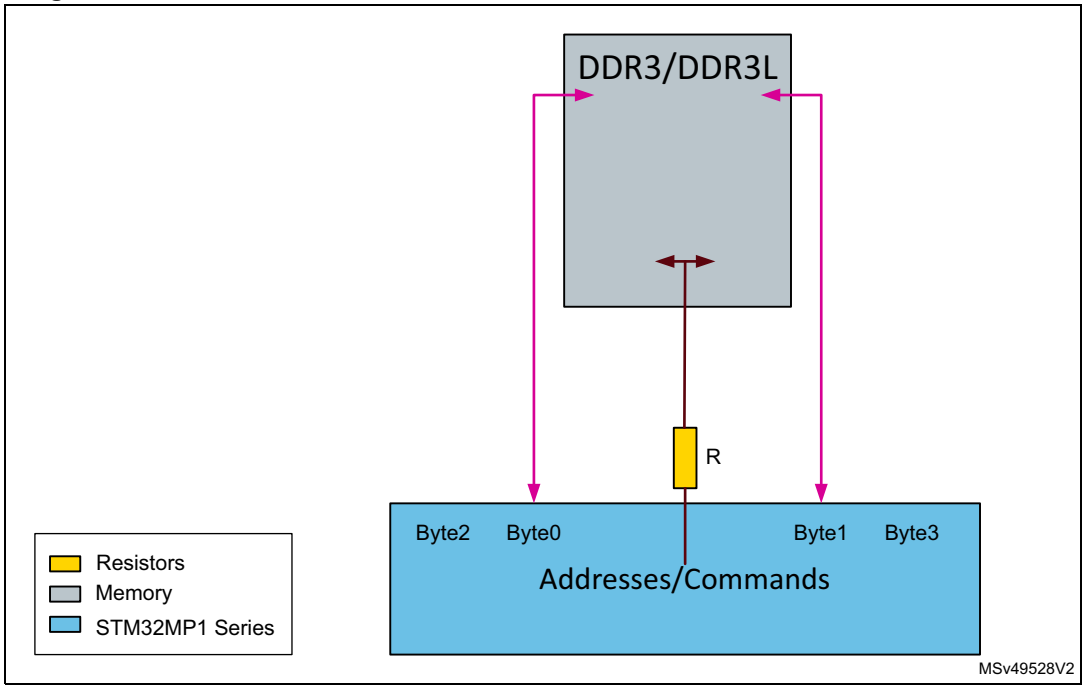
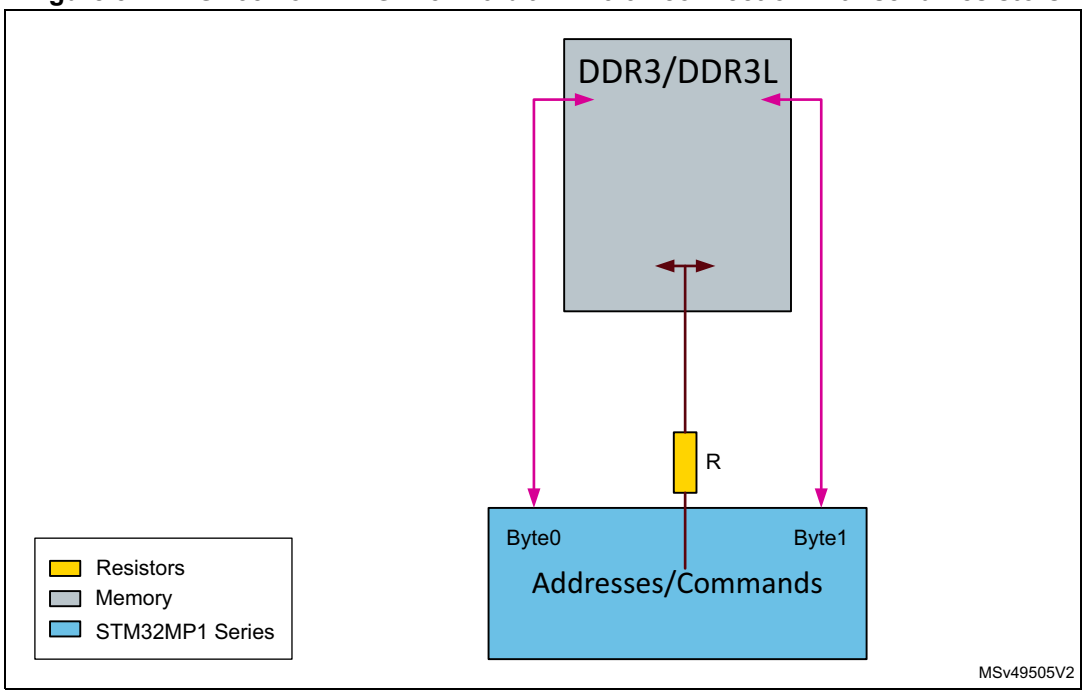


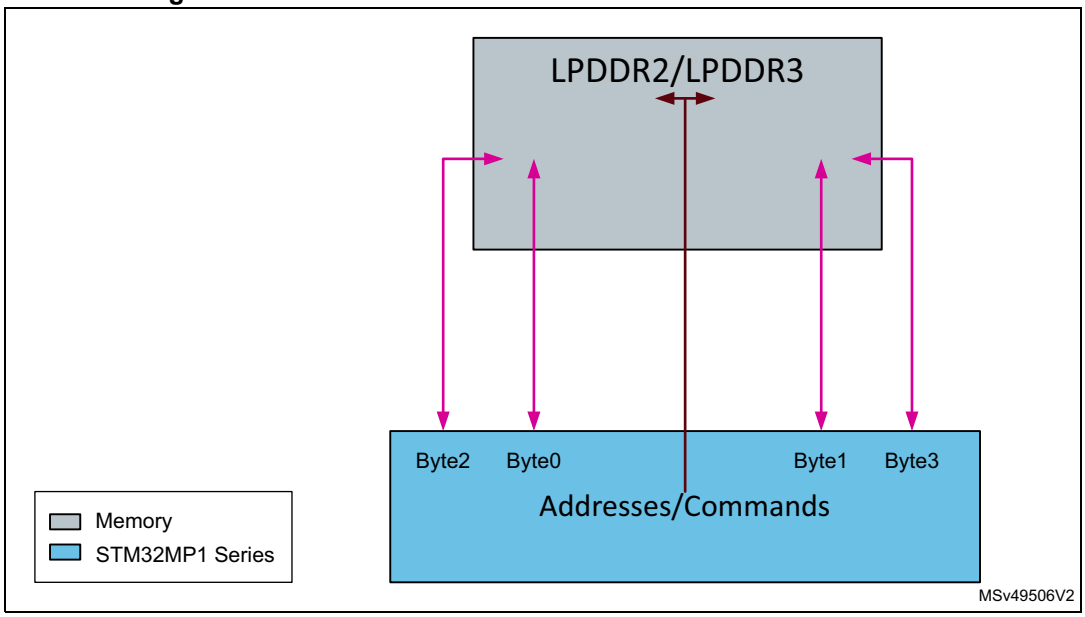
Figure 5. LFBGA354 or TFBGA257 16-bit DDR3/3L connection with serial resistors



2.3 32-bit LPDDR2/LPDDR3 interface

For 32-bit LPDDR interface, one 32-bit LPDDR2/3 is used in point-to-point connection.

Figure 6. LFBGA448 or TFBGA361 32-bit LPDDR2/3 connection



2.4 16-bit LPDDR2/LPDDR3 interface

For 16-bit LPDDR interface, one 16-bit LPDDR2/3 is used in point-to-point connection.

On 32-bit interface, only bytes 0 and 1 are used, let bytes 2 and 3 not connected.

Figure 7. LFBGA448 or TFBGA361 16-bit LPDDR2/3 connection

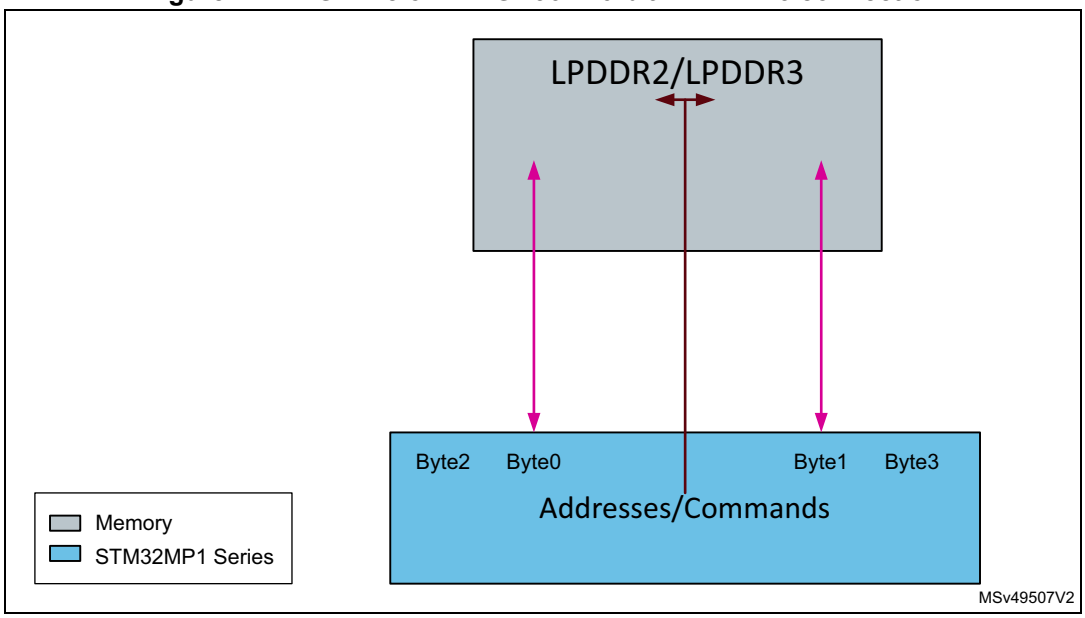
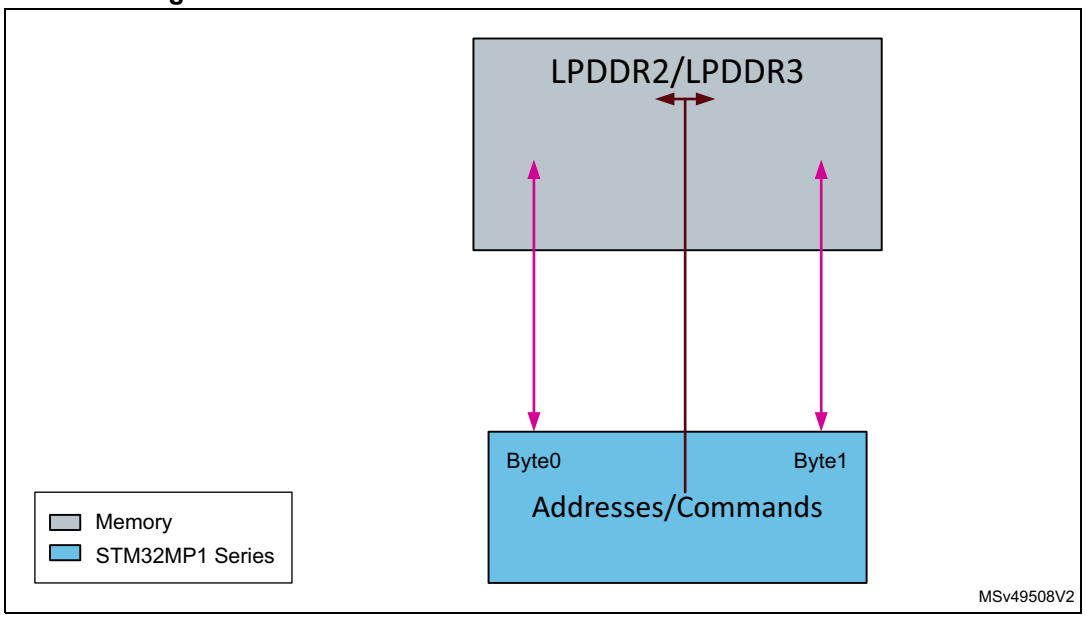


Figure 8. LFBGA354 or TFBGA257 16-bit LPDDR2/3 connection



3 DDR3/DDR3L schematic implementation

A DDR implementation should be comprised of the following elements.

3.1 Standard fly-by topology

A standard fly-by topology is comprised of:

- A distributed A/C bus with 56 Ω on-board termination at VTT (VDD_DDR/2)
- A differential clock, distributed to all of the DDR devices
  - Implement a differential termination of the CLK_N/CLK_P signals using one 100 Ω resistor.
- There must be a point-to-point connection of the data bus (4 swappable bytes, and swappable bits in the same byte), including:
  - 32 data signal bits (DQ)
  - 4 data mask signals (DQMx)
  - 4 differential clocks (DQSx_N/DQSx_P)

3.2 Cost-optimized point-to-point topology

This topology can be used when there is a single DDR chip interface. It is comprised of:

- A point-to-point connection of every A/C bus, with no termination on-board
- 33 Ω serial resistors are recommended for every A/C of the DDR chip, in order to reduce reflection
- The CLK_N/CLK_P signals are terminated differentially, by one 100 Ω resistor.
- Point-to-point connection of the data bus (2 swappable bytes, and swappable bits in the same byte):
  - 16 data signal bits (DQ)
  - 2 data mask signals (DQMx)
  - 2 differential clocks (DQSx_N/DQSx_P)

3.3 Miscellaneous signals

In addition, the following signals should be included in the schematic:

- DDR_RESETN
  DDR_RESETN is an asynchronous low speed reset signal from DDR controller to DDR devices. A 10 kΩ pull-down resistor is required. The signal is driven low during the

power-on or when a reset is required. Otherwise, the signal should be driven high by default.

- ZQ
  This signal requires, for DDR impedance calibration, that resistors are placed between the signal balls and ground as follows:
  – a 240 Ω (+/- 1%) resistor must be placed between the ZQ ball on each DDR chip and the GND plane.
  – a 240 Ω (+/- 1%) resistor must also be placed between the ZQ ball of STM32MP1 Series and the GND plane.
- CKE
  CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. A 10 kΩ pull-down resistor is required.

3.4 Power supply and reference voltages

The following power supply and reference voltage components must be provided:

- VREF reference voltage (equal to VDD_DDR /2)
  This is the reference voltage required by STM32MP1 Series and DDR3/3L devices, in order to properly sample A/C and data signals. Its noise level must remain very low, as described in the JEDEC standard.

  Two solutions proposed:
  – Independent VREF generators (VREFCA, VREFDQ) for each device.
    Each VREF generator is based on a 2 kΩ (+/- 1%) resistance bridge from VDD_DDR plus a local 100 nF decoupling capacitor.
    The reference voltage, VREF, should be generated as close as possible to its corresponding ball.
  – Common VREF for each device.
    VREF generator from external IC is delivered to each device with a local 100 nF decoupling capacitor. STPMIC can deliver VREF.
- VTT power supply (equal to VDD_DDR /2)
  The VTT power supply is only used in DDR3/3L interfaces using fly-by topology.
  This is the termination voltage for address and control (A/C) signals.
  External VTT voltage generator recommended. STPMIC can deliver VTT.
  Strong VTT decoupling required, as close as possible to termination resistors.
- VDD_DDR power plane
  This is the DDR interface power supply, equal to 1.5 V (1.425-1.575 V) for DDR3 or 1.35 V (1.283-1.45 V) for DDR3L.
  This plane requires mandatory decoupling capacitors relative to the GND plane with bulk capacitors and HF capacitors close to each of the power supply pins for DDR and STM32MP1 Series.

4 LPDDR2/LPDDR3 schematic implementation

A LPDDR2/3 implementation should be comprised of the following elements.

4.1 Point-to-point topology

A standard point-to-point topology is comprised of:

- A distributed 12 A/C signals
- A differential clock with differential termination of the CLK_N/CLK_P signals using one 100 Ω resistor.
- There must be a point-to-point connection of the data bus (4 bytes with 32-bit LPDDR2/3 or 2 bytes with 16-bit LPDDR2/3), including:
  - 32 data signal bits (DQ). Byte 0 of LPDDR2/3 must be connected to byte 0 of STM32MP1 Series but there is no possibility to swap bits in this byte. The 3 others bytes are swappable, and bits in the same byte are swappable.
  - 4 data mask signals (DQMx).
  - 4 differential clocks (DQSx_N/DQSx_P).

4.2 Miscellaneous signals

In addition, the following signals should be included in the schematic:

- ZQ
  This signal requires, for LPDDR2/3 impedance calibration, that resistors are placed between the signal balls and ground as follows:
  - a 240 Ω (+/- 1%) resistor must be placed between the ZQ ball on LPDDR2/3 chip and the GND plane.
  - a 240 Ω (+/- 1%) resistor must also be placed between the ZQ ball of STM32MP1 Series and the GND plane.
- CKE
  CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. A 10 kΩ pull-down resistor is required.

4.3 Power supply and reference voltages

The following power supply and reference voltage components must be provided:

- VREF reference voltage (equal to VDD2_DDR /2)
  This is the reference voltage required by STM32MP1 Series and LPDDR2/3, in order to properly sample A/C and data signals. Its noise level must remain very low, as described in the JEDEC standard.

  Two solutions proposed:
  - Independent VREF generators (VREFCA, VREFDQ).
    Each VREF generator is based on a 2 kΩ (+/- 1%) resistance bridge from VDD2_DDR plus a local 100 nF decoupling capacitor.

The reference voltage, VREF, should be generated as close as possible to its corresponding ball.

– Common VREF (VREFCA, VREFDQ).
VREF generator from external IC is delivered to LPDDR2/3 with a local 100 nF decoupling capacitor. STPMIC can deliver VREF.

- VDD2_DDR power plane
This is the LPDDR2/3 interface power supply, equal to 1.2 V (1.14-1.30 V).
This plane requires mandatory decoupling capacitors relative to the GND plane with bulk capacitors and HF capacitors close to each of the power supply pins for LPDDR2/3 and STM32MP1 Series.
- VDD1_DDR power supply
This is the core power supply of LPDDR2/3, equal to 1.8 V (1.7-1.95 V).

5 PCB design considerations

The basic PCB design considerations to take into account are detailed in the following sections. This is a non-exhaustive list of good practices to follow for sensitive-signal designs.

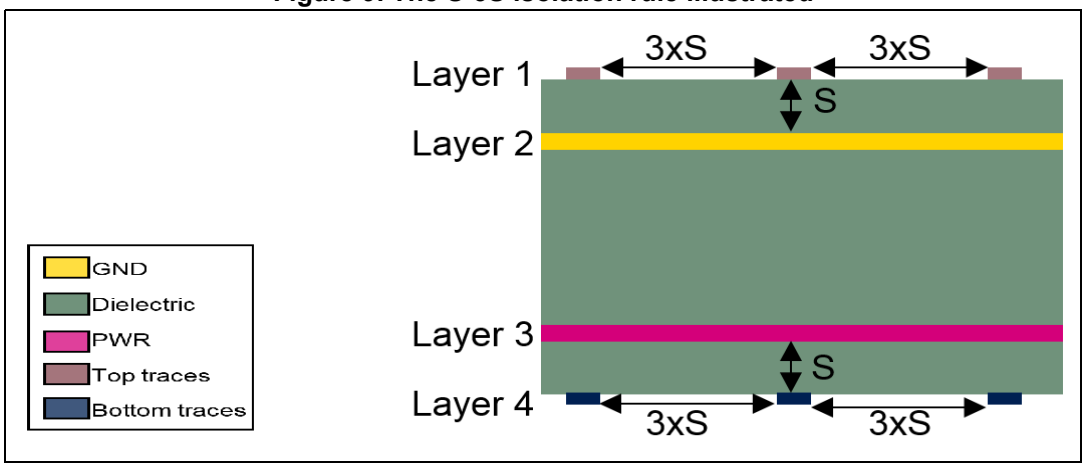
5.1 Trace isolation distance

A minimum isolation distance must be provided around every trace, in order to reduce crosstalk, glitches and jitter caused by neighboring traces (sometimes referred to as ‘aggressors’).

S-3S isolation rule

If S is the distance between a trace and its reference plane (the GND plane for top-layer traces, and the PWR plane for bottom-layer traces), a trace is said to be isolated if the distance between it and its direct neighbors is greater or equal than 3 x S. *Figure 9* shows this rule in practice.

Figure 9. The S-3S isolation rule illustrated



In other words, S-3S is the minimum isolation/spacing rule.

If more space between traces is available, it must be used to dispatch signals (S-4S, S-10S…).The more space there is between traces, the better the signal isolation and noise immunity is.

The S-3S rule is not applicable below BGA devices (memory and STM32MP1 Series) because of fan-out constraints.

When the S-3S rule is not applicable, the length of the segments that are in conflict with the rule, must be minimized.

Layouts using an S-1S layout must be avoided as often as possible. If the S-3S rule is not applicable, maximizing the distance between traces as much as possible (S-2S rule) is preferable to using an S-1S layout.

5.2 Length equalization

Signals of the same group must have matched setup and hold timings when they arrive at their destination. Owing to this, trace length equalization may be required, so that these timing constraints are met.

The whole signal path must be considered (from the STM32MP1 Series die to the memory chip), taking into account the package and PCB lengths.

For data signals, internal delay adjustment capability may allow the removal or reduction of length equalization requirements.

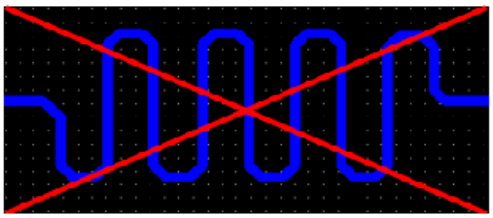
Length equalization patterns

When routing traces to equalize lengths, some patterns should be preferred over others. For example, serpentines are not recommended, as they can provoke orthogonal propagation which compromises signal integrity.

Switchback patterns are preferred.

Figure 10. Length equalization patterns

Switchback pattern



Serpentine pattern

The S-3S isolation rule must also be applied within the equalization pattern, meaning that the minimum distance between sections of the same trace should be greater or equal to S-3S.

In the case of differential signals:

- Intra-pair length equalization is not allowed
- The spacing between N and P must be constant
- The mean value length of N and P signals should be considered for a differential pair:

$$Lsig = \frac{LsigN + LsigP}{2}$$

ST templates and length equalization tables can be used to help simplify the task of equalizing signal trace lengths. These tables include the trace lengths of the packages. Please contact your local ST sales representative to obtain these.

5.3 Impedance

In general, driver impedance (ZDRV) is usually 34 Ω or 40 Ω, while on-die termination impedance (ZODT) is usually 60 Ω.

Board impedance must be controlled in order to guarantee proper transmission line setup, in accordance with trace geometry (width and spacing) and the stack-up of the board.

For DDR3/3L, LPDDR2/3 interfaces, ST recommends the following impedances:

- For single-ended signals: 55 Ω +/- 10%.
- For differential signals: 100 Ω differential +/- 10%.

5.4 Layer allocation for 4-layer boards

Layers must be allocated and implemented as detailed below, without exception:

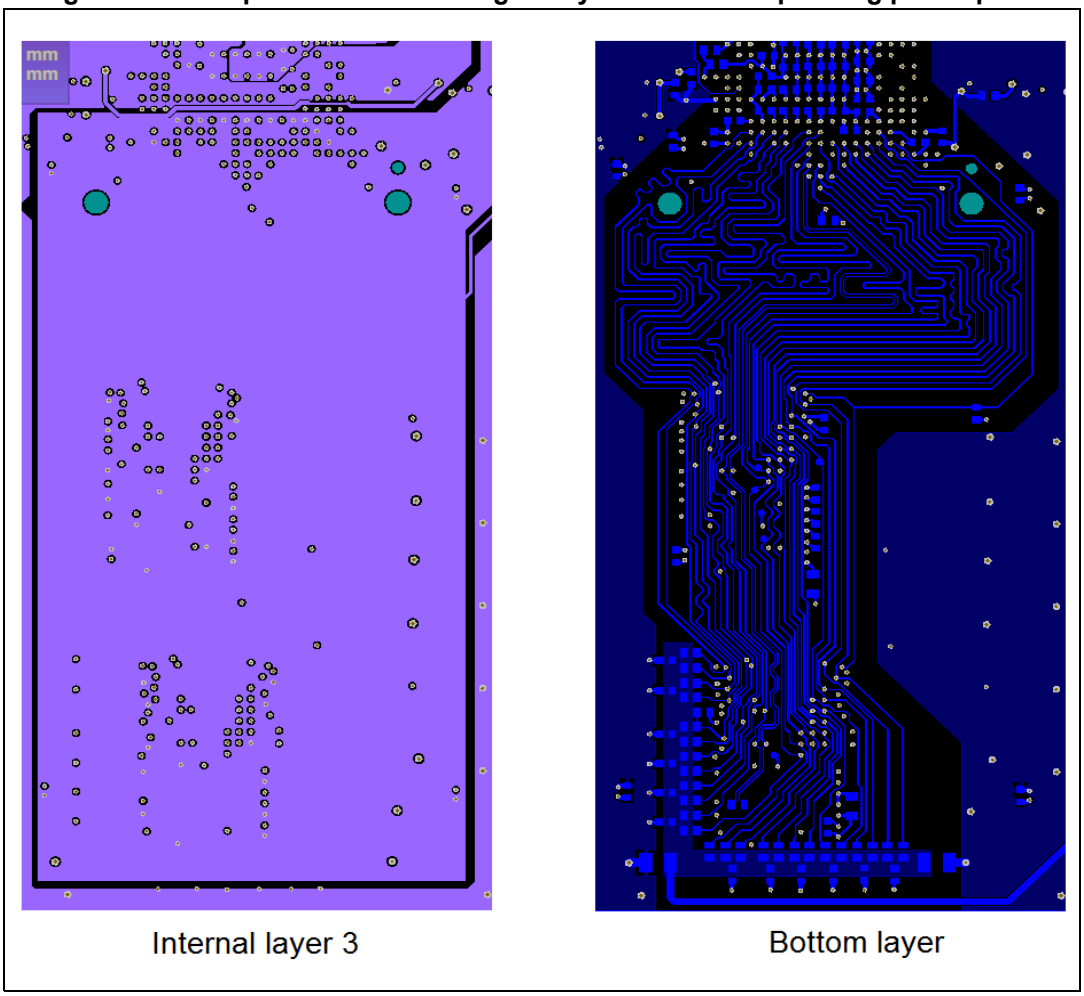
- Top layer
  - This layer is dedicated to those traces with the highest sensitivity.
  - The traces are referenced to the unified, internal ground (GND) plane.
  - There are no impedance breaks.
  - There is no coupling allowed to noisy power supplies.
- Layer 2 (GND) internal layer
  - This is the unified internal ground plane.
  - It must be connected by a matrix of vias to the top and bottom GND areas.
- Layer 3 (VDD_DDR for DDR3/3L or VDD_DDR2 for LPDDR2/3) internal layer
  - This is the dedicated power supply plane, which supplies on board power distribution.
- Bottom layer
  - This is a second signal layer used for traces. It is possible to have impedance breaks in this layer, due to the discontinuity of the reference power supply plane.

5.5 VDD_DDR power plane specification

In normal practice, A/C signals are laid out on the bottom layer of the 4-layer PCB.

The internal layer 3 must be a unified VDD_DDR (VDD_DDR2 for LPDDR2/3) power plane, which fully overlaps the memory bottom-layer signals, in order to avoid any impedance breaks due to traces referenced to multiple power planes.

Figure 11. Example of DDR3L A/C signal layout and corresponding power plane



5.6 Layer change capacitors

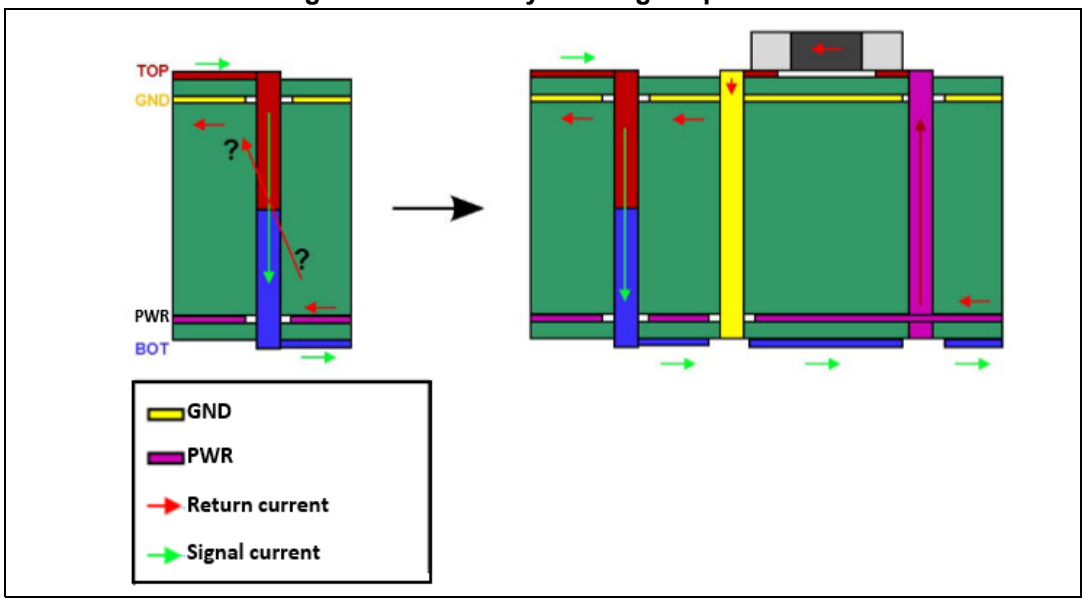
When a sensitive signal moves from the top layer of the PCB to the bottom layer (or vice versa), a 100 nF capacitor must be placed as close as possible to the signal via.

It should be connected from one side to the layer 2 (GND), and from the other side, to the layer 3 (VDD_DDR for DDR3/3L, VDD_DDR2 for LPDDR2/3).

This design requirement is absolutely necessary in order to provide an HF return current reference path to the signal.

The capacitor can be placed on either the bottom or top layer (as shown in *Figure 12*).

Figure 12. Use of layer change capacitors



In practice, when multiple signals are changing layers in the same area of the PCB (such as in the case of A/C bus distribution), it may become impossible to place a single capacitor close to each via.

The solution in this case is to add a single capacitor for a group of vias. You should try to use as many capacitors as is practical for your board design, and these should be placed as close to the via area as possible.

5.7 Types of decoupling capacitors

Power integrity is essential for avoiding voltage drops and by consequence, eye closure and erroneous data transmission.

Core and sensitive power supplies (like VDD_DDR) must be laid out using internal power planes, using maximum width, in order to minimize distribution impedance.

In addition to this, decoupling capacitors are required. There are two types:

- Bulk capacitors
  These capacitors provide an on-board energy tank for low-frequency, high-current needs. Capacitance values can range from 10 µF to 100 µF. You should refer to ST reference design to choose a capacitor value appropriate for your power supply.
  Bulk capacitors do not need to be placed very close to their destination.
- HF capacitors
  HF (high frequency) capacitors provide a local energy tank for high-frequency current bursts. HF capacitors must be placed as close as possible to the destination (power pins or balls).It is better practice to implement fewer capacitors, but placed in optimum position, in order to reduce connection inductance.

5.8 Minimizing connection inductance with HF capacitors of decoupling capacitors

Decoupling capacitor placement must ensure minimum connection inductance.

The closer the capacitor is to its destination, the more efficient it is. This is particularly true for HF capacitors.

Another factor is whether the capacitor is place on the top or bottom layer.

Putting capacitors on the top layer can provide far better decoupling efficiency than placement on the bottom layer.

However, the choice of where capacitors are located can be constrained by BGA fan-out.

For this reason, we look at best practices for capacitor placement in order to minimize connection inductance and improve decoupling efficiency, for both top and bottom layers.

5.8.1 Placing capacitors on the top layer

Capacitors placed on the top layer of PCBs cannot be very close to BGA balls, due to package constraints.

However, if a capacitor is connected by a direct top-layer power trace to the BGA ball, its connection inductance remains smaller than if the capacitor is located much closer, but on the bottom layer, owing to the GND layer position in the stack-up (the GND is the return current layer).

The amount of connection inductance that results is directly linked to the area of the current loop.

Therefore top layer placement offers:

- Pros
  - a small current loop area, resulting in low connection inductance and good decoupling capability.
  - It allows free space on the bottom layer for other signal layouts. As memory A/C trace layouts are usually on the bottom layer, this allows more flexibility for A/C length equalization/spacing requirements.
- Cons
  - Placement of capacitors on the top layer is very often not possible for main BGA decoupling because of fan-out constraints.

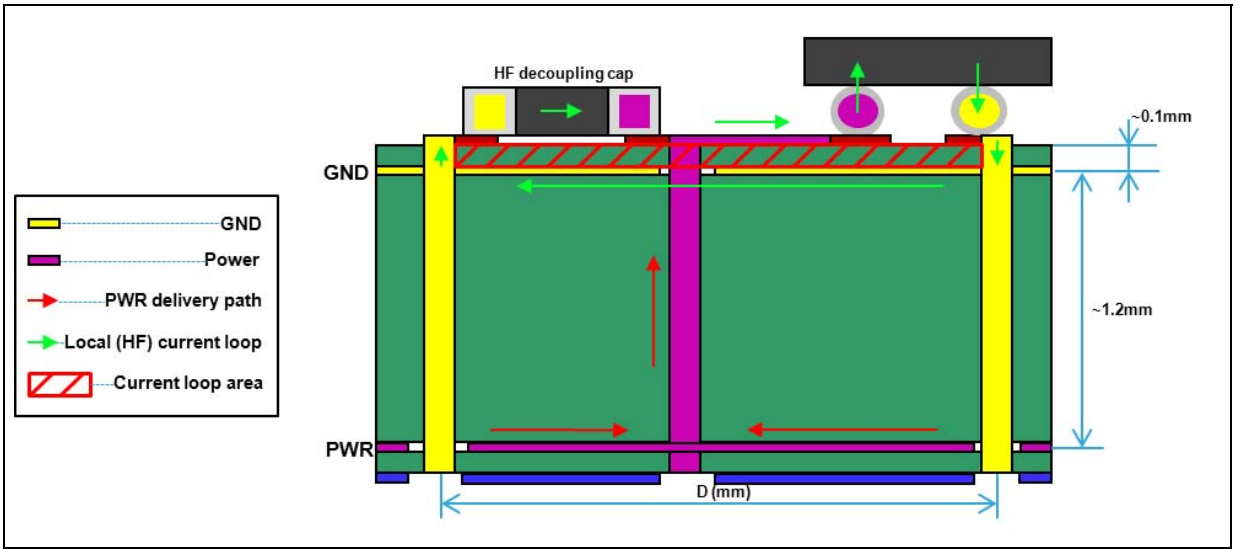
When possible, try to place an HF capacitor on the top layer, with a top-layer direct power connection. The layer 2 (GND) provides a close return path, which results in a small current loop area and optimal decoupling efficiency.

For example, in the layout shown in *Figure 13*, the resulting current loop area is:

$$\text{Current loop area} = 0.1 \times D$$

So, if D equals 5 mm, the current loop area is in the region of 0.5 mm².

Figure 13. Placement of an HF capacitor on the top layer

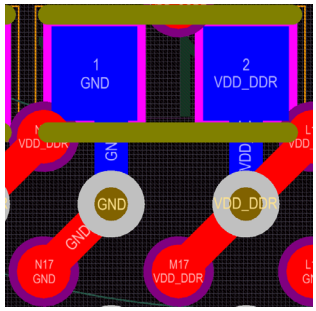


5.8.2 Placing capacitors on the bottom layer

When top-layer decoupling is not possible, placement of capacitors must be on the bottom layer.

While the connection inductance is higher than for top-layer capacitor placement, due to the bigger current loop area, bottom layer placement remains most of the time the only decoupling option for main BGA. Following some basic implementation rules allow for an optimization of this placement. For best results, place the capacitor right below the BGA balls.

Figure 14. HF capacitor on bottom layer



When placing HF capacitors on the bottom layer, aim to have the shortest possible connections, and a good via placement directly below the BGA, as shown in *Figure 14*.

In the following example, the resulting current loop area is:

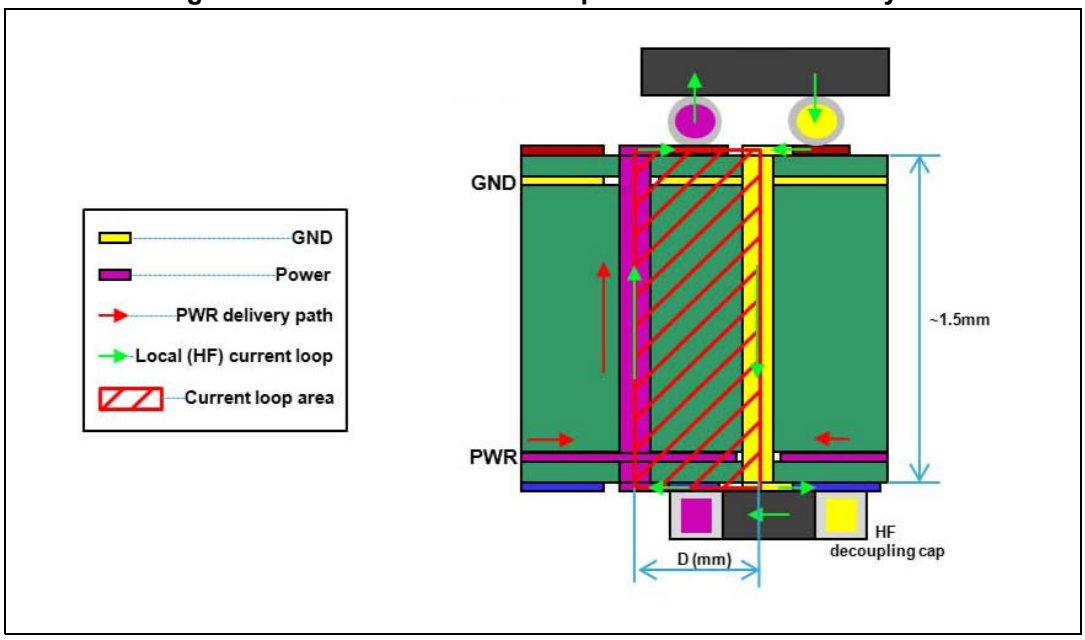
$$\text{Current loop area} = 1.5 \times D$$

If D equals 1.0 mm, the resulting current loop area is 1.5 mm², as compared to 0.5 mm² for a top-layer placement at a 5 mm distance.

In other words, a capacitor situated on the top layer, 15 mm from the power ball, would have the same efficiency as a capacitor situated on the bottom layer, directly below the power ball.

This illustrates the higher efficiency of top-layer capacitor placement relative to bottom-layer placement.

Figure 15. Placement of an HF capacitor on the bottom layer



6 Memory layout rules

Based on the basic PCB design rules, here is a code of best practice rules that should be applied, by signal type, on memory interface.

6.1 Data signal rules for 32-bit memory interfaces

There are four different/independent signal groups over 4 bytes:

- Byte0 = DQ[7:0], DQM0, DQS0_N and DQS0_P,
- Byte1 = DQ[15:8], DQM1, DQS1_N and DQS1_P,
- Byte2 = DQ[23:16], DQM2, DQS2_N and DQS2_P,
- Byte3 = DQ[31:24], DQM3, DQS3_N and DQS3_P,

For these data signals, please apply the following rules:

- These data signals should only be routed on the top layer of the PCB.
- Apply the S-3S isolation rule as a minimum, wherever possible.
  The only exceptions should be made when signals are very close to the memory chip or STM32MP1 Series, due to the constraints of high via density and BGA pitch.
  When the S-3S rule is not applicable, the layout must be designed to optimize the isolation rule (S-2S, S-1.5S…). Segments, where S-1S is the only option, must be as short as possible.
- For DDR3 and DDR3L, as fly-by topology is used with two 16-bit DDR3/3L, do not apply the same length equalization on-board for all bytes, but apply the rule below to the bytes of first DDR3/3L together and to the bytes of second DDR3/3L together:
  - DQ or DQM to DQS_N/DQS_P +/- 40 mils (1.016 mm)
  - Length of DQS_N/DQS_P must be from 0 to 590 mils (14.986 mm) shorter than CLK_N / CLK_P length (CLK_N/CLK_P must be the longest traces).
  - Length of the bytes of second DDR3/3L compared to length of the bytes of first DDR3/3L 1300 mils (33.02 mm) max
- For LPDDR2 and LPDDR3, as point-to-point topology is used, apply the rule below to each byte:
  - DQ or DQM to DQS_N/DQS_P +/- 40 mils (1.016 mm)
  - Length of DQS_N/DQS_P must be from 0 to 590 mils (14.986 mm) shorter than CLK_N / CLK_P length (CLK_N/CLK_P must be the longest traces).

Trace length = substrate length + via length + board track length

$$\text{Differential trace length (DSQS\_N/DQS\_P)} = \frac{\text{Trace length N} + \text{Trace length P}}{2}$$

– Always refer to the ST reference design for signal ordering, BGA fan-out and layout examples.

6.2 Data signal rules for 16-bit memory interfaces

There are two different/independent signal groups over 2 bytes:

- Byte0 = DQ[7:0], DQM0, DQS0_N and DQS0_P
- Byte1 = DQ[15:8], DQM1, DQS1_N and DQS1_P

With one 16-bit DDR3/3L or LPDDR2/3, the rules below are applied to both bytes:

- DQ or DQM to DQS_N/DQS_P +/- 40 mils (1.016 mm)
- Length of DQS_N/DQS_P must be from 0 to 590 mils (14.986 mm) shorter than CLK_N / CLK_P length (CLK_N/CLK_P must be the longest traces).

With two 8-bit DDR3/3L in fly-by topology, the rules below are applied to byte 0 and byte 1, for sure track lengths of byte 0 are not the same than track lengths of byte 1:

- DQ/DQM to DQS_N/DQS_P +/- 40 mils (1.016 mm)
- Length of DQS_N/DQS_P must be from 0 to 590 mils (14.986 mm) shorter than CLK_N / CLK_P length (CLK_N/CLK_P must be the longest traces).
- Length of byte 1 compared to length of byte 0 1300 mils (33.02 mm) max

6.3 Address and control (A/C) signal rules

The following signals are included in these groups:

- For DDR3/3L A[15:0], BA[2:0], RASN, CASN, WEN, CSN, CKE, ODT, CLK_N, CLK_P
- For LPDDR2/3 A[9:0], CSN, CKE, CLK_N, CLK_P

The following design rules should be applied for A/C signals:

- The PCB bottom layer must be used for A/C distribution to memory devices. The top layer is reserved for connections to the memory chip (stubs) and A/C bus crossing.
- Apply the S-3S isolation rule as a minimum, wherever possible.
  The only exceptions should be made when signals are very close to the memory chip or STM32MP1 Series, due to the constraints of high via density and BGA pitch.
  When the S-3S rule is not applicable, the layout must be designed to optimize the isolation rule (S-2S, S-1.5S…). Segments, where S-1S is the only option, must be as short as possible.
- Length equalization rules:
  Length of A/C must be from 0 to 40 mils (1.016 mm) shorter than CLK_N / CLK_P length
  CLK_N / CLK_P maximum length 4.72 inch (12 cm)

$$\text{Trace length} = \text{substrate length} + \text{via length} + \text{board track length}$$

$$\text{Differential trace length (CLK\_N/CLK\_P)} = \frac{\text{Trace length N} + \text{Trace length P}}{2}$$

- In case of fly-by topology used for DDR3/3L:
  Length of A/C, CLK_N/CLK_P of first DDR3/3L compared to length of A/C, CLK_N/CLK_P of second DDR3/3L1300 mils (33.02 mm) max.

  Always refer to the ST reference design for signal ordering, BGA fan-out and layout examples.

6.4 ZQ signal

This signal should be laid out so that the trace from the ball to the reference resistor is as short as possible. Care should be taken to ensure good isolation from any noisy aggressor signals.

6.5 Power plane rules

Power planes must be designed in accordance with the following rules.

6.5.1 VDD_DDR (VDD_DDR2 for LPDDR2/3) power plane

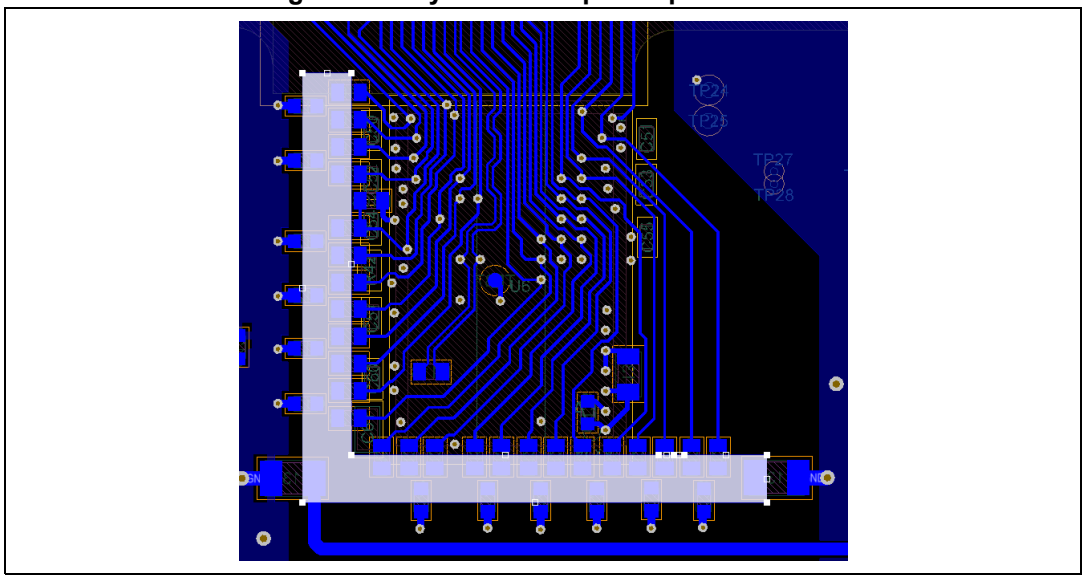
- It should be a unified power plane at layer 3.
- This power plane must overlap every DDR3/3L (LPDDR2/3) trace on the bottom layer, in order to avoid impedance discontinuities.
- The VDD_DDR power plane's connection to the VDD_DDR power supply, to the STM32MP1 Series and to each memory device, must be done by multiple vias.
- Standard decoupling rules must be applied:
  - Bulk capacitors must be placed between the voltage regulator and the STM32MP1 Series and memory devices
  - HF decoupling capacitors must be placed as close as possible to each of the power pins, following the low-connection-induction recommendations outlined in *Section 5.8*.

6.5.2 VTT power plane rule

The VTT power supply is only used in DDR3/3L interfaces using fly-by topology.

- The VTT termination voltage must be considered as a power supply.
- Due to VDD_DDR constraints (an unified plane in layer 3, overlapping the DDR area), the VTT layout has to be managed as an island on the bottom layer. See *Figure 16*.
- The VTT regulator should be located close to the RTT terminations.
- One HF capacitor must be reserved for two RTT termination resistors and must be placed as close as possible to them.
- Bulk capacitors can be placed anywhere between VTT regulator and terminations.
- Leave sufficient spacing around the VTT island, to reduce crosstalk.

Figure 16. Layout of VTT power plane island



Revision history

Table 2. Document revision history

Date	Revision	Changes
31-Jan-2018	1	Initial version
1-Feb-2019	2	Replaced: -STM32MP15 Series by STM32MP1 Series Updated: -*Section 6.1*, *Section 6.2* and *Section 6.3* regarding data, address and control signal rules
6-Feb-2019	3	Replaced: -STPMU1 by STPMIC